Design with QorIQ T2081 and T1040 Processor Families

APF-SNT-T1360

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External Use

Session Introduction

- This session is relevant for customers designing with Freescale T2081 and T1040 family of QorIQ processors
  - Details the commonalities and differences
  - Examines the problems and solutions of common board design and migration from T1040 to T2081
  - Provides practical examples based on existing Freescale designs

Session Objectives

- After completing this session you will be able to:
  - Identify the design collateral that exists to assist with T1040 and T2081 designs
  - Recognize the major design issues for the common board design and how they can be overcome
  - Use our design tips for high-speed interface design (eSDHC and SerDes)
  - Know where to go for assistance

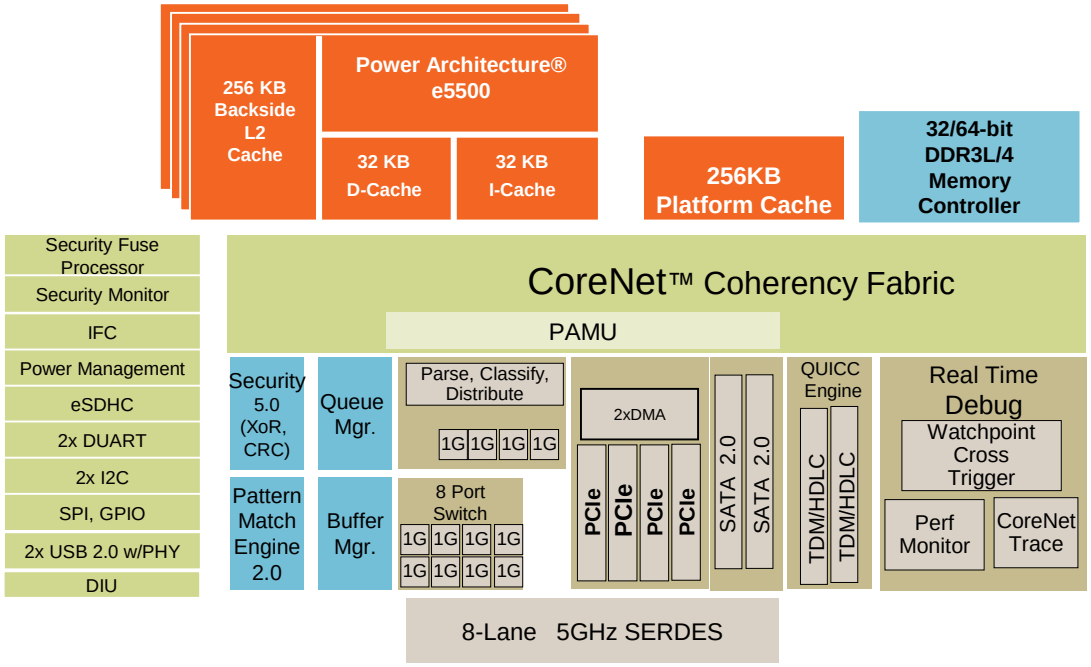
Agenda

- T1040 and T2081 Overview
- Hardware Compatibility
- Software Compatibility
- Pinout Comparison
- Supporting Tools
- Reference Documentation

Agenda

- T1040 and T2081 Overview
  - T1040 Block Diagram
  - T2081 Block Diagram
  - Device Comparison
  - Commonalities and Differences

T1040



Device

- 780-pin FC-PBGA package
- 23x23mm, 0.8mm pitch

Power targets

- Enable Convection cooled system design

Datapath Acceleration

- SEC- crypto acceleration
- PME- Reg-ex Pattern Matcher

Processor

- 4x e5500, 64b, up to 1.4GHz
- Each with 256KB backside L2 cache
- 256KB Shared Platform Cache w/ECC
- Supports up to 64GB addressability (36 bit physical addressing)

Memory Subsystem

- 32/64b DDR3L/4 Controller up to 1600MHz

CoreNet Switch Fabric

High Speed Serial IO

- 4x PCIe Gen2 (5Gbps) Controllers
- 2x SATA 2.0, 3Gbps
- 2x USB 2.0 with PHY

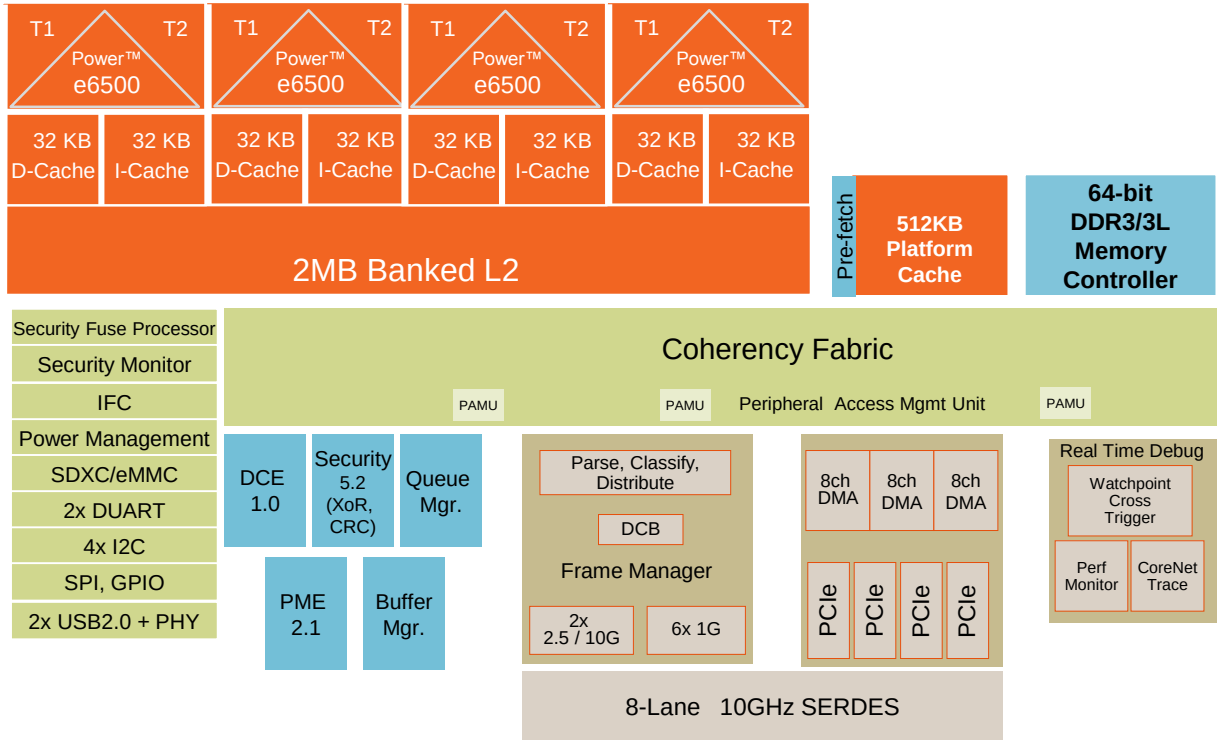
Network IO

- FMan packet Parse/Classify/Distribute
- Lossless Flow Control, IEEE 1588
- Up to 4x 10/100/1000 Ethernet Controllers
- **8-Port Gigabit Ethernet Switch**
- QUICC Engine
  - HDLC, 2x TDM

Green Energy Operation

- Fanless operation quad-core 1.4GHz
- Packet lossless deepsleep
  - Programmable wake-on-packet
  - Wake-on-timer/GPIO/USB/IRQ

QorIQ T2081 Block Diagram



Datapath Acceleration

- **SEC**- crypto acceleration 10Gbps
- **DCE** - Data Compression Engine 17.5Gbps
- **PME** – Pattern Matching Engine to 10Gbps

Processor

- 4x e6500, 64b, 1.5 - 1.8GHz
- Dual threaded, with 128b AltiVec
- 2MB shared L2; 256KB per thread

Memory Subsystem

- 512KB Platform Cache w/ECC
- 1x DDR3/3L Controllers up to 2.1GHz
- Up to 1TB addressability (40 bit physical addressing)
- HW Data Pre-fetching

Switch Fabric

High Speed Serial IO

- 4 PCIe Controllers: one at Gen3, three at Gen2
  - 1 with SR-IOV support
  - x8 Gen2
- 2 USB 2.0 with PHY

Network IO

- Up to 25Gbps Simple PCD each direction
- 8 MACs multiplexed over:
  - 2x 10GE, 2x 2.5Gb/s SGMII, 7x GE
  - XFI, 10GBase-KR, SGMII, RGMII, 1000Base-KX

Device

- TSMC 28HPM Process
- 23x23mm, 780pins, 0.8mm pitch, pin compatible with T1042
- Power estimated at 18.7– 24.4W (thermal) depending on frequency

Schedule: samples: 2H-2014; qual Q1-15

Device Comparison – T1040 and T2081

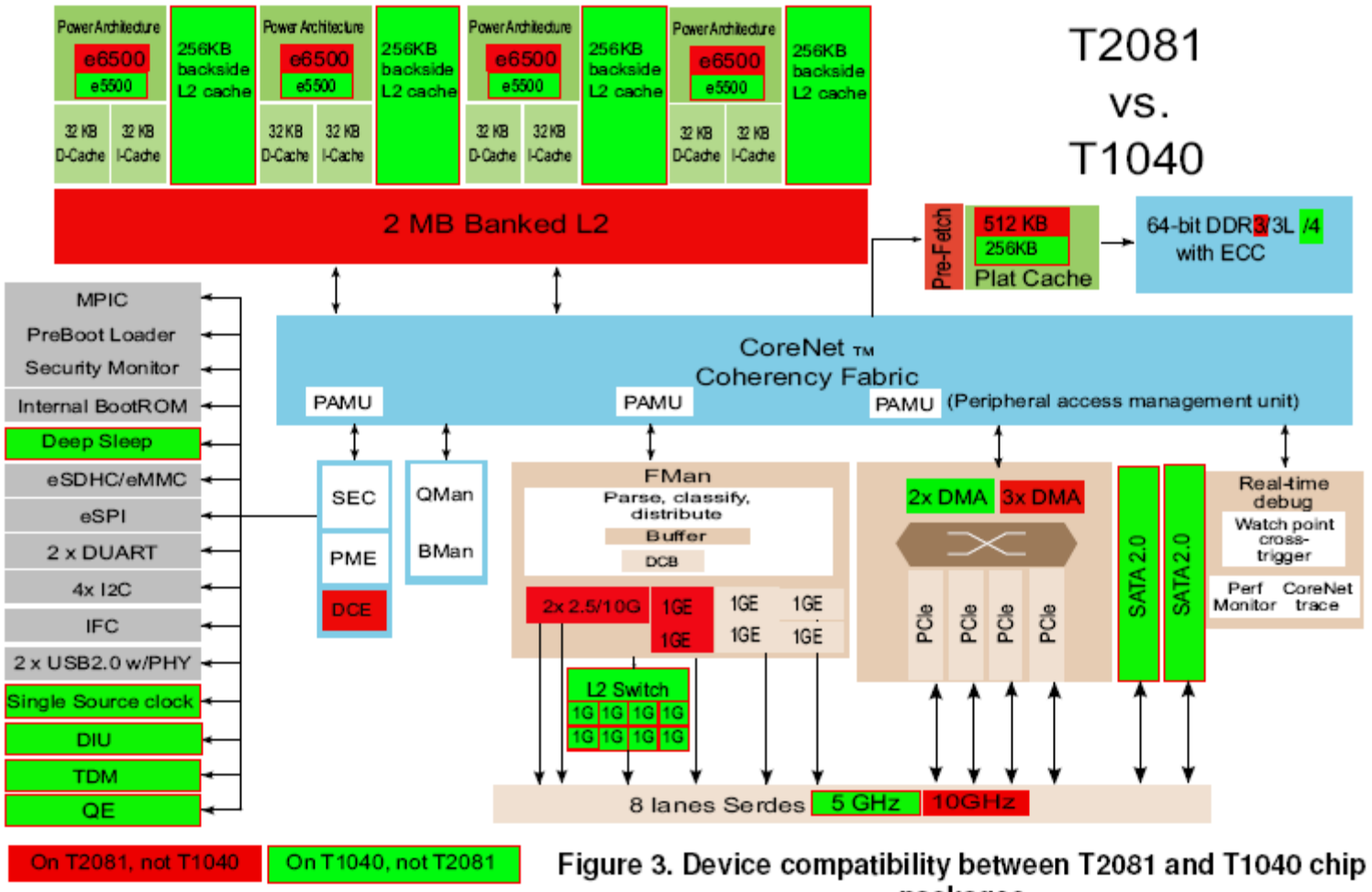


Figure 3. Device compatibility between T2081 and T1040 chip packages

Commonalities and Differences

Features	T2081	T1040	T1042
Cores			
Number of cores	4 × e6500 dual threaded Power Architecture	4 × e5500 Power Architecture	4 × e5500 Power Architecture
Architecture width	64-bit	64-bit	64-bit
Max frequency (MHz)	1800	1400	1400
DMIPS/MHz	6	3	3
Memory Size			
L1 Cache	32KB I/D	32KB I/D	32KB I/D
L2 Cache	2 MB shared	256KB / core backside	256KB / core backside
CPC	512KB frontside	256KB frontside	256KB front side
Cache line size	64 Bytes	64 Bytes	64 Bytes
Memory Type	DDR3/3L @2133 MT/s	DDR3L/4 @1600 MT/s	DDR3L/4 @1600 MT/s
Maximum size of main memory	32 GB (1Gbit x8 device)	32 GB (1Gbit x8 device)	32 GB (1Gbit x8 device)

Commonalities and Differences (contd…)

Features	T2081	T1040	T1042
I/O			
Ethernet controllers	2× XFI 6x SGMII 2x 2.5Gbps SGMII 2x RGMII	2× 5Gbps QSGMII 6x 1Gbps SGMII 2x RGMII 1x MII	6x 1Gbps SGMII 2x 2.5Gbps SGMII 2x RGMII 1x MII
SerDes lanes	8 lanes at up to 10GHz	8 lanes at up to 5 GHz	8 lanes at up to 5 GHz
PCI Express controllers	3 × Gen 2.0 controllers 1 × Gen 3.0 controllers	4 × Gen 2.0 controllers	4 × Gen 2.0 controllers
SATA	None	2 x SATA controllers	2 x SATA controllers
TDM	None	Full duplex serial	Full duplex serial
DIU	None	12 bit RGB	12 bit RGB
CoreNet	700MHz at 256 bits	600MHz at 128 bits	600MHz at 128 bits
Ethernet switch	None	8 port	None
QE	None	HDLC, UART, TDM/SI	HDLC, UART, TDM/SI

Commonalities and Differences (contd…)

Features	T2081	T1040	T1042
I/O			
Integrated Flash Controller (IFC)	8-/16-bit data width, 32-bit address width	8-/16-bit data width, 32-bit address width	8-/16-bit data width, 32-bit address width
Clocking			
Single source clocking	None	Diff_SYSCLK/DIFF_SYSCLK_B supported	Diff_SYSCLK/DIFF_SYSCLK_B supported
Power Management			
Deep Sleep	None	Supported	Supported
Package			
780 FC-PBGA	23 mm x 23 mm	23 mm x 23 mm	23 mm x 23 mm

Agenda

- T1040 and T2081 Overview
- Hardware Compatibility
  - Identical Interfaces
  - DDR Controller
  - eSDHC Controller
  - TEST_SEL _B pin
  - Sense Pins
  - Power Sequencing
  - Power Supply
  - Clock Difference

Identical Interfaces

The following interfaces are identical between the T2081 and T1040:

- **Integrated Flash Controller (IFC)**
- **Enhanced SPI Controller (eSPI)**
- **DUART Controller**
- **USB Controller**

DDR Controller

- T2081 supports DD3/3L DDR controller.
- T1040 supports DDR3L/4.
- As DDR3L is common to both devices, it should be used for the common board design.

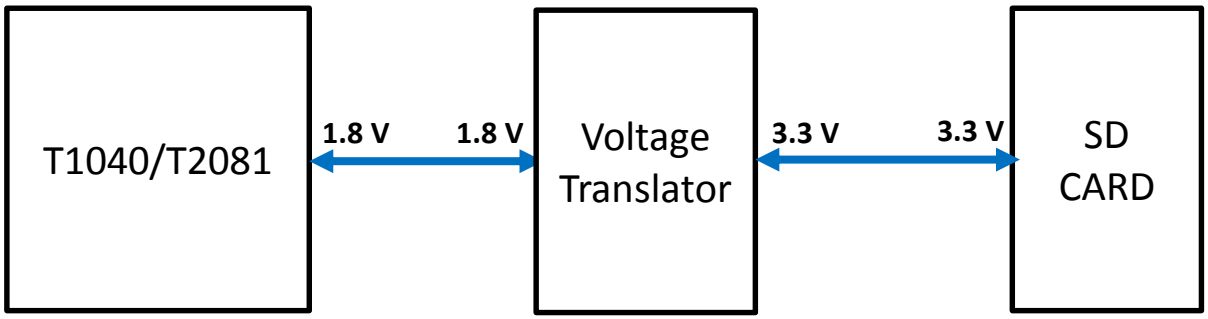
DDR Calibration Resistor Values

	MDIC [0]	MDIC[1]
T1040	162 ohm 1%	162 ohm 1%
T2081	187 ohm 1%	187 ohm 1%

eSDHC Controller

- eSDHC Controller Recommendations
- Both T1 and T2 supports SD 3.0 specification introducing higher capacity up to 2 TB and frequency up to 208 MHz.
- A dynamic switching of I/O voltage from 3.3 V to 1.8V is required.
- T2081 doesn’t support the dynamic switch, so the board level shifters are required for common board design.

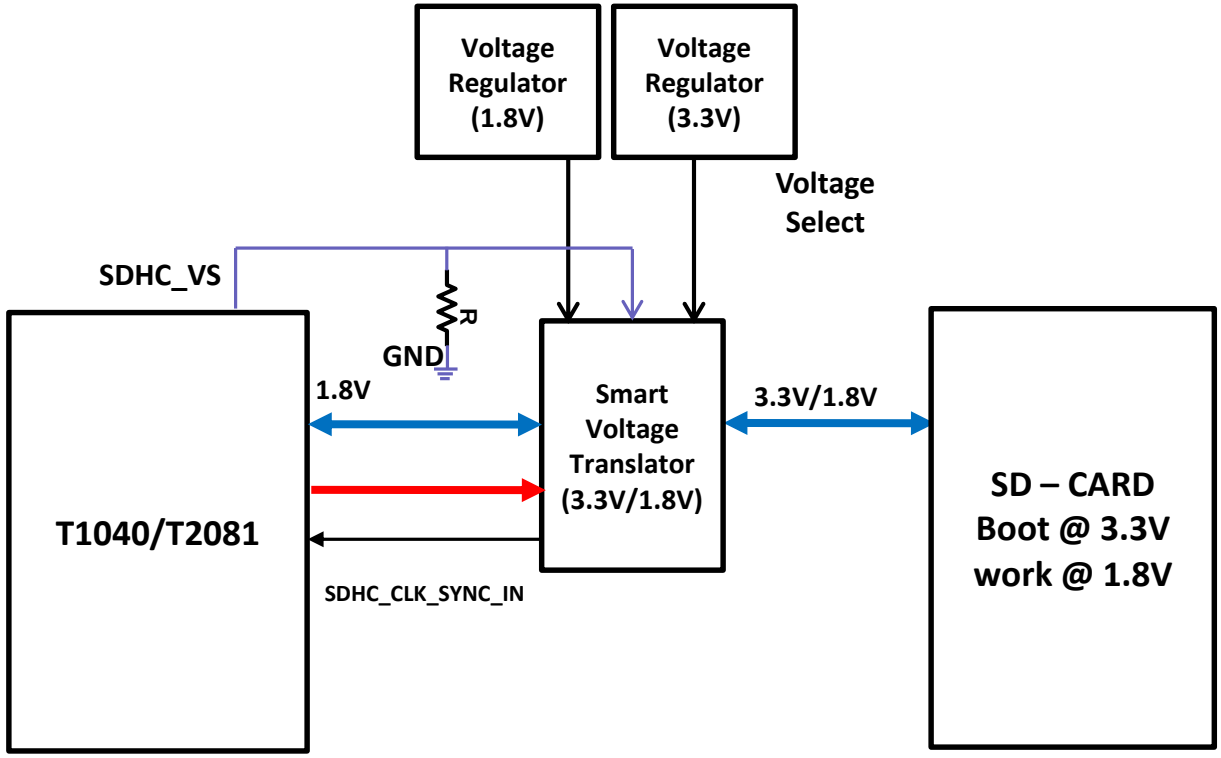
SD Card Connections for T1/T2 Compatibility (DS and HS Modes)



CMD, DAT[0], DAT[1:3], CLK, CD_B, WP

- Other signals should be left NC
- SYNC_OUT should be pulled-down with a weak resistor or the pin should be configured for alternate functionality

SD Connections for T1/T2 Compatibility (SDR12, 25, 50, 104 and DDR50 Modes)



- R = 10k
- Resistor R is only needed when RCW loading is required to be done from SD card

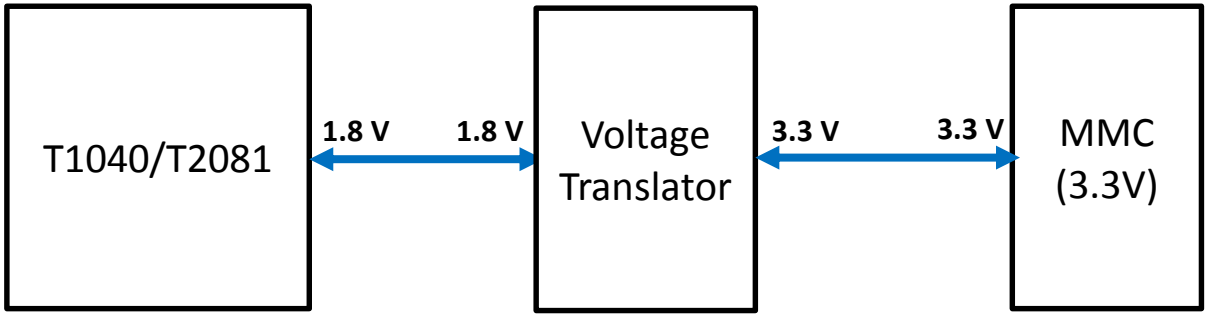
CMD, DAT[0], DAT[1:3], CLK, CD_B, WP

DIR

- Other signals should be left NC
- SYNC_OUT should be pulled-down with a weak resistor or the pin should be configured for alternate functionality

- SYNC_IN connection is needed in SDR50, DDR50 mode only.
- In SDR50, DDR50 mode all the input signals are sampled with respect to SYNC_IN

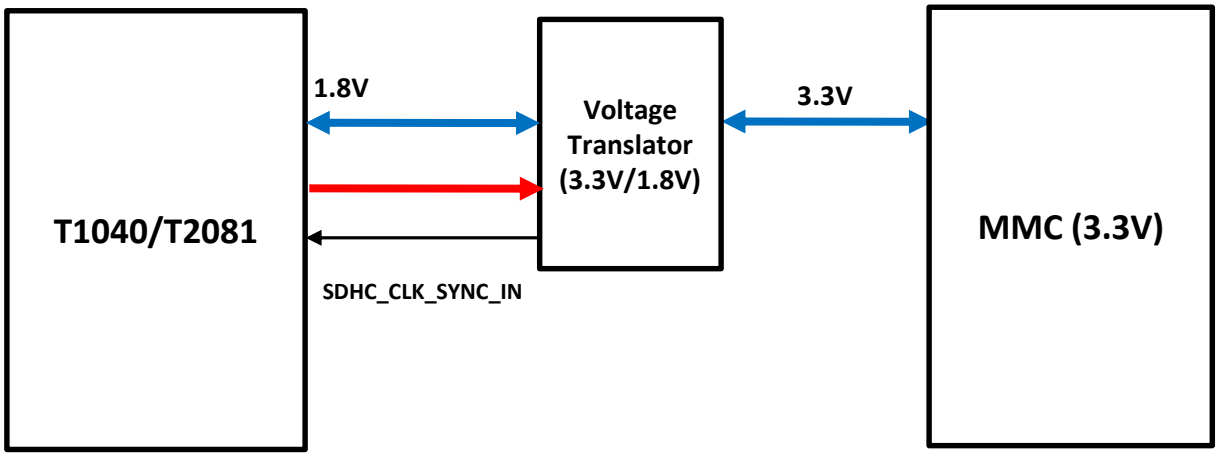
MMC Card Connections for T1/T2 Compatibility (DS, HS, HS200 Modes)



CMD, DAT[0], DAT[1:7], CLK, CD

- Other signals should be left NC
- SYNC_OUT should be pulled-down with a weak resistor or the pin should be configured for alternate functionality
- Voltage translator is not needed for 1.8V MMC.

MMC (3.3V) Connections for T1/T2 Compatibility (DDR Mode)



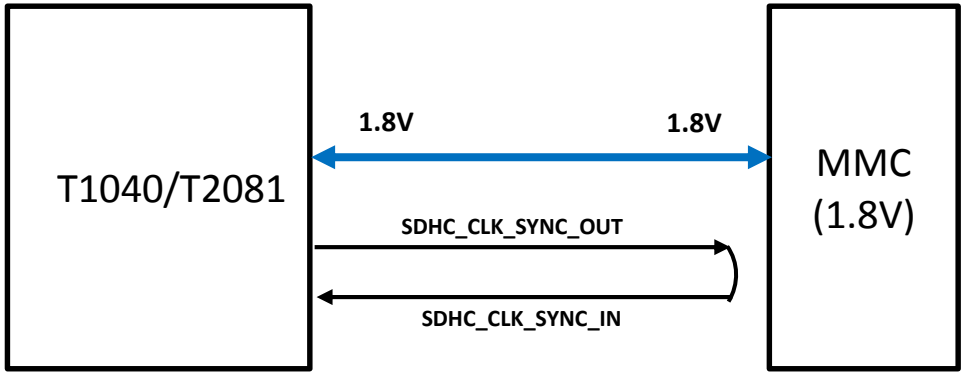
CMD, DAT[0], DAT[1:3], CLK, CD

DIR

- In DDR mode all the input signals are sampled with respect to SYNC_IN

- Other signals should be left NC
- SYNC_OUT should be pulled-down with a weak resistor or the pin should be configured for alternate functionality
- Voltage translator is not needed for 1.8V MMC.

MMC (1.8V) Connections for T1/T2 Compatibility (DDR Mode)



CMD, DAT[0], DAT[1:7], CLK, CD

- Other signals should be left NC
- In DDR mode all the input signals are sampled wrt SYNC_IN

TEST_SEL_B Pin

- The requirement is different for T1040 and T2081.

Device	TEST_SEL_B Requirement
T1040, T1042	Pull up to O1VDD
T1020, T1022	Pull down to GND
T2081	Pull up to OVDD

Sense Pins

- If the sense pins are used for the regulators, SENSEVDD should be used. SENSEVDDC can be left floating.

Ball Location	T2081	T1040
G19	SENSEVDD	SENSEVDD
AB9	RSVD28	SENSEVDDC

Power sequencing requirements

- T1040 requires its power rails to rampup in a specific sequence, whereas T2081 has no such requirement.
- Common board should follow T1040 hardware specification for the Power sequencing requirements.

Case: Power ON

Step 1 I/O supplies should ramp up (1.8V, 2.5V, 3.3V).

- *PORESET should be asserted when VDDC/VDD rampup*

Step 2 Core supplies (1.0V), USB_SVDD

- *I/O power should ramp before core power*

Step 3 DDR supplies (G1VDD, X1VDD)

- *VDD should ramp before G1VDD*

Power Supply for Core

- Core Power Island Requirements
- T1040 has VDD and VDDC power domains for core and platform.
- T2081 has only VDD power domain for core and platform.
- The common board design should use a single rail for VDD and VDDC in T1040.

T2081	T1040	Recommendation
VDD	VDD, VDDC	VDD and VDD should be connected to a common rail.

Power Supply for I/O

Supply	T2081	T1040	Recommendation for a common board design	Interface wise recommendation	Interfaces
$O1V_{DD}$	—	1.8V	Use Single regulator for OV_{DD} and $O1V_{DD}$ on T1040 at 1.8V	eSDHC interface of T2081 is on OV_{DD} supply while IO power supply of eSDHC in T1040 is fed by EV_{DD}. If eSDHC is used, EV_{DD} and OV_{DD} should be connected to 1.8V. On board level shifters are required to support SD 3.0 modes.	Common: MPIC, GPIO, System Control, Debug, Clocks, JTAG I/O, IFC, RTC and power management I/O's, T2081 only: eSDHC
OV_{DD}	1.8V	1.8V			
DV_{DD}	2.5V 1.8V	3.3V 2.5V 1.8V	Use 2.5V or 1.8V only for DV_{DD} supply	DIU and TDM are supported at 3.3V so voltage translators may be required on a common board. QE interface is supported at 2.5V and 3.3V, restricting DV_{DD} to 2.5V for common board.	Common: DUART, I2C, DMA, MPIC T1040 only: QE, TDM, DIU
CV_{DD}	2.5V 1.8V	3.3V 1.8V	Use 1.8V for CV_{DD} supply	—	Common: eSPI, SDHC_DAT[4:7]
EV_{DD}	—	3.3V 1.8V	Use OV_{DD} supply for EV_{DD}	SDHC_DAT[0:3], SDHC_CMD and SDHC_CLK are the signals on EV_{DD} supply in T1040. These signals are on OV_{DD} supply in T2081. See OV_{DD} supply for details.	Common: eSDHC See Note
$G1V_{DD}$	1.5V 1.35V	1.35V 1.2V	Use $G1V_{DD}$ at 1.35V	Use DDR3L only	Common:DDR3L T1040: DDR4 T2081: DDR3
$L1V_{DD}$	—	3.3V 2.5V 1.8V	Use Single regulator for LV_{DD} and $L1V_{DD}$ on T1040 It can support 2.5V or 1.8V	Use RGMII interface at 2.5V only.	Common:GPIO, RGMII@2.5V T1040: MII, RGMII@1.8V
LV_{DD}	2.5V 1.8V	3.3V 2.5V 1.8V			

Clocking Difference

- T1040 supports the differential pair of SYSCLK, the common board design leaves it as floating or connect through 10K Ohm resistor to GND.

Clocking scheme	T2081	T1040	Recommendation
Single Reference clock mode	No	Yes	T1040: Supported through DIFF_SYSCLK/DIFF_SYSCLK_B clock input pair
Multiple reference clock mode	Yes	Yes	Through separate oscillators for SYSCLK, DDRCLK, USBCLK, SDREF_CLKn inputs. Recommended mode for common board design.

Exceptions

Product	PCIe	MII on EC1	QE (TDM HDLC)	Starlite TDM	QSGMII	GE Switch	XFI	SATA	DIU	Deep Sleep
T1040	4 Gen 2	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes
T2081	1 Gen3 3 Gen 2	NO	NO	NO	NO	NO	Yes	NO	NO	NO

Agenda

- T1040 and T2081 Overview
- Hardware Compatibility
- Software Compatibility
  - e6500 and e5500 Compatibility
  - RGMII
  - SerDes Configuration
  - RCW
  - Difference in driver

e6500 and e5500 Compatibility

- User code runs equally well on e6500 or e5500
  - Interrupts per thread
  - Soft reset per thread (hard reset per core only)
  - Debug state per thread
- Changes are hidden by OS
  - L2 initialization uses a different register
  - Cache locking controlled differently
- Additional enablement for new features not present on e5500:
  - 64b, drowsy power manager, Altivec

e5500/e6500 Caching Structure Differences

	e5500	e6500	Implication
L1	32KB. Can lock per core	32kB. Can lock per core	e6500 doesn't lock per thread
L2	128KB per core	2MB shared	There will be a somewhat different latency profile, overall improved for e6500
L3	256KB	512kB	

- Cache changes are transparent to user application
- L1 locking is less granular in e6500

RGMII

- The two RGMII interfaces are pin compatible, the configurations for RGMII mode are different between the T2081 and T1040 devices.

- T1040 also supports MII interface on EC1 Interface. When using MII interface, L1VDD and LVDD are restricted to 3.3V and RGMII cannot be supported on EC1 or EC2.

Configuration	RGMII assignment		
	T2081	T1040	
RCW[EC1] = 0b00	FMan MAC3	FMan MAC4	MAC2_GMII_SEL = 0b0
		FMan MAC2	MAC2_GMII_SEL = 0b1
RCW[EC2] = 0b00	FMan MAC4	FMan MAC5	—
RCW[EC2] = 0b01	FMan MAC10	—	

T1/T2 compatible Serdes Configurations

T1040 SRDS_PRCTL_S1	A	B	C	D	E	F	G	H	T2081 SRDS_PRTCL_S1
0x00 (2 RGMII; FMAN MAC4 & MAC5)	PEX1 (5/2/5)				PEX2 (5/2.5)				0xAA (2 RGMII; FMAN MAC3 & MAC4/10)
	PEX3 (5/2.5)				PEX4 (8/5/2.5)				
0x40 (2 RGMII; FMAN MAC4 & MAC5)	PEX1 (5/2.5)		sg.m1 (1.25)	sg.m2 (1.25)	PEX2 (5/2.5)				0xBC (2 RGMII; FMAN MAC3 & MAC4/10)
	PEX3 (5/2.5)		SG1 (1.25)	SG2 (1.25)	PEX4 (8/5/2.5)				
0xA5 (0 RGMII)	PEX1 (5/2.5)	sg.m3 (1.25)	sg.m1 (3.125)	sg.m2 (3.125)	PEX2 (5/2.5)		sg.m4 (1.25)	sg.m5 (1.25)	0xC8 (2 RGMII; FMAN MAC3 & MAC4)
	PEX3 (5/2.5)	SG10 (1.25)	SG1 (3.125)	SG2 (3.125)	PEX4 (5/2.5)		SG5 1.25)	SG6 (1.25)	
0xAA (0 RGMII)	PEX1 (5/2.5)	sg.m3 (1.25)	sg.m1 (3.125)	sg.m2 (3.125)	PEX2 (5/2.5)	PEX3 (5/2.5)	sg.m4 (1.25)	sg.m5 (1.25)	0xFA (2 RGMII; FMAN MAC3 & MAC4)
	PEX3 (5/2.5)	SG10 (1.25)	SG1 (3.125)	SG2 (3.125)	PEX4 (5/2.5)	PEX1 (5/2.5)	SG5 (1.25)	SG6 (1.25)	
0x85 (0 RGMII)	PEX1 (5/2.5)	sg.m3 (1.25)	sg.m1 (1.25)	sg.m2 (1.25)	PEX2 (5/2.5)		sg.m4 (1.25)	sg.m5 (1.25)	0xD6 (2 RGMII; FMAN MAC3 & MAC4)
	PEX3 (5/2.5)	SG10 (1.25)	SG1 (1.25)	SG2 (1.25)	PEX4 (8/5/2.5)		SG5 (1.25)	SG6 (1.25)	

T1/T2 compatible SerDes Configurations (continue)

T1040 SRDS_PRCTL_S1	A	B	C	D	E	F	G	H	T2081 SRDS_PRTCL_S1
0x87 (1 RGMII; FMAN MAC4)	PEX1 (5/2.5)	sg.m3 (1.25)	sg.m1 (1.25)	sg.m2 (1.25)	PEX2 (5/2.5)	PEX3 (5/2.5)	PEX4 (5/2.5)	sg.m5 (1.25)	0xF2 (2 RGMII; FMAN MAC3 & MAC4)
	PEX3 (5/2.5)	SG10 (1.25)	SG1 (1.25)	SG2 (1.25)	PEX4 (8/5/2.5)	PEX1 (5/2.5)	PEX2 (5/2.5)	SG6 (1.25)	
0xA7 (1 RGMII; FMAN MAC4)	PEX1 (5/2.5)	sg.m3 (1.25)	sg.m1 (3.125)	sg.m2 (3.125)	PEX2 (5/2.5)	PEX3 (5/2.5)	PEX4 (5/2.5)	sg.m5 (1.25)	0xF8 (2 RGMII; FMAN MAC3 & MAC4)
	PEX3 (5/2.5)	SG10 (1.25)	SG1 (3.125)	SG2 (3.125)	PEX4 (5/2.5)	PEX1 (5/2.5)	PEX2 (5/2.5)	SG6 (1.25)	
0x8D* (Using L2 switch) (2 RGMII; FMAN MAC4 & MAC5)	PEX1 (5/2.5)	sg.s3 (1.25)	sg.s1 (1.25)	sg.s2 (1.25)	PEX2 (5/2.5)	sg.s6 (1.25)	sg.s4 (1.25)	sg.s5 (1.25)	0xCA (1 RGMII; FMAN MAC3)
	PEX3 (5/2.5)	SG10 (1.25)	SG1 (3.125)	SG2 (3.125)	PEX4 (5/2.5)	SG4 (1.25)	SG5 1.25)	SG6 (1.25)	
0x06* (2 RGMII; FMAN MAC4 & MAC5)	PEX1 (5/2.5)				PEX2 (5/2.5)	PEX3 (5/2.5)	PEX4 (5/2.5)	SATA1	0xDE (2 RGMII; FMAN MAC3 & MAC4/10)
	PEX3 (5/2.5)				PEX4 (8/5/2.5)	PEX1 (5/2.5)	PEX2 (5/2.5)	SG6 (1.25)	
0x08* (2 RGMII; FMAN MAC4 & MAC5)	PEX1 (5/2.5)				PEX2 (5/2.5)	PEX3 (5/2.5)	SATA2	SATA1	0xE0 (2 RGMII; FMAN MAC3 & MAC4/10)
	PEX3 (5/2.5)				PEX4 (8/5/2.5)	PEX1 (5/2.5)	SG5 (1.25)	SG6 (1.25)	

Reset Configuration Word

- RCW are mostly compatible. Detail listed in T1040 and T2080 reference manual.

RCW bits	T1	T2	Notes
10-15	MEM_PLL_CFG		Cutoff frequencies for the T1 and T2 differ. 24:1 async mode setting is available for T1.
176-177	SRDS_DIV_PEX		T1: 00 Train up to 5G T2: 00 Train up to 8G
190-191	DDR_FDBK_ MUL	Reserved	
242	SYS_PLL_SPD	Reserved	
321	UC1_CTSB_ CDB_SEL	Reserved	
418-419	EC1		Using different MAC. T1: MAC #4 and #2 T2: MAC #3
420-421	EC2		Using different MAC. T1: MAC #5 T2: MAC #4, #10

Difference in driver

To limit driver configuration issues, take the following actions to simplifying the driver configuration.

- Number of cores
  - T1040: 4 single-threaded e5500 cores running at 1000MHz/1200MHz/1400MHz
  - T2080: 4 dual-threaded e6500 cores(8 virtual cores) running at 1200MHz/1533MHz/1800MHz

  Using 1200MHz for both core

- CPC size
  - T1040: 256-Kbyte, 8-way set associative, 64-byte coherency granule
  - T2080: 512-Kbyte, 16-way set associative, 64-byte coherency granule

  Use 256-Kbyte, 8-way set associative, 64-byte coherency granule

- L2 size
  - T1040: 256KB per e5500 core, total 1MB.
  - T2080: 2MB shared by 4 e6500 cores

  Use 256KB per thread

Difference in driver (continue…)

- DDR
  - T1040: one 32-/64-bit DDR3L/DDR4 SDRAM memory controller with ECC and interleaving support
  - T2080: one 32-/64-bit DDR3/3L SDRAM memory controller with ECC and interleaving support and Memory pre-fetch engine

  Select cfg_dram_type = 1 to choose DDR3L.

- Ethernet
  - T1040: 4 MACs from FMan and 8 MAC from Ethernet Switch. It supports two RGMII ports using MAC4 & MAC5.
  - T2080: 8 MACs from FMan(four 1G and four 1/2.5/10G) running with various combinations with different SerDes procotols. Two RGMII ports using MAC3 & MAC4, 4 XFI ports using MAC9,MAC10,MAC1,MAC2.

  Using RGMII requires the software driver to remap the different MACs between T1 and T2,

  choose a pin compatible configuration for SerDes option.

- PCIe
  - T1040: four PCI Express 2.0 controllers/ports running at up to 2.5/5GHz.
  - T2080: two PCI Express 2.0 running at 2.5/5GHz and two PCI Express 3.0 controllers/ports running at 2.5/5/8GHz.

  Using 2.5/5GHz only.

Difference in driver (continue…)

- SATA
  - T1040 and T2080 have same two SATA controllers supporting 1.5 and 3.0 Gbps operation, there is no defference in software configuration.

- QE
  - T1040: support QE with two TDM interfaces. u-boot doesn't support TDM.
  - T2080: no support.

- DIU
  - T1040: support LCD and HDMI interface (DIU) with 12 bit dual data rate.
  - T2080: no support.

Difference in driver (continue…)

- PAMU
  - no changes in S/W.
- DMA
  - 3 in T2081 vs 2 in T1040.
- GE switch
  - if used on board add if config, only for T1040.
- IFC
  - same so no changes.
- Single Source Clocking: USB considerations, only for T1040.
- Deep sleep: only for T1040.

Agenda

- T1040 and T2081 Overview
- Hardware Compatibility
- Software Compatibility
- Pinout Comparision
- Supporting Tools
- Reference Documentation

Pinout Comparison

This table details the differences in pinout between the T2081 and T1040 processor family and how to resolve this difference. Unless explicitly stated otherwise, the pins on the T2081 can be connected as if a T1040 is populated.

Pin	T2081	T1040	Compatible connection
Ethernet MI 2 pins			
L6	**EMI2_MDC**	RSVD10	All the Ethernet PHY's to be used with T1040 should be managed through the EMI1 interface.
M6	**EMI2_MDIO**	RSVD11	
Ethernet Cont. 1 pins			
AC4	RSVD34	**EC1_TX_ER**	EC1 Interface on T1040 also supports MII interface (**see Section 3.8, "Ethernet MACs options"**)This output pin can be left floating if not used.
AC2	RSVD33	**EC1_RX_ER**	Tie low through a 2-10 kohm resistor if not used.
AC1	RSVD32	**EC1_COL**	
Differential SYSCLK pins (see Section 4, "Internal clocking differences")			
G14	RSVD07	**DIFF_SYSCLK**	Differential SYSCLK input is available only in T1040. These can be left floating or connected to GND if unused.
F14	RSVD05	**DIFF_SYSCLK_B**	

Pinout Comparison

DMA/TDM pins			
U5	DMA1_DACK0_B/GIPIO4_05	DMA1_DACK0_B/GIPIO4_05/**TDM_TFS**	Additional TDM functionality is available in T1040 over DMA pins. When used, software needs to manage the interface on T2081
R5	DMA1_DDONE0_B/GPIO4_06	DMA1_DDONE0_B/GPIO4_06/**TDM_TCK**	
P5	DMA1_DREQ0_B/GPIO4_04	DMA1_DREQ0_B/GPIO4_04/**TDM_TXD**	
AA5	DMA2_DACK0_B/GIPIO4_08/EVT7_B	DMA2_DACK0_B/GIPIO4_08/EVT7_B/**TDM_RFS**	
Y5	DMA2_DDONE0_B/GPIO4_09/EVT8_B	DMA2_DDONE0_B/GPIO4_09/EVT8_B/**TDM_RCK**	
V5	DMA2_DREQ0_B/GPIO4_07	DMA2_DREQ0_B/GPIO4_07/**TDM_RXD**	
I2C 3 & 4 pins			
V2	IIC3_SCL/GPIO4_00	IIC3_SCL/GPIO4_00/**QE_SI1_STROBE0**	Additional QE functionality is available in T1040 over I2C pins.
W3	IIC3_SDA/GPIO4_01	IIC3_SDA/GPIO4_01/**QE_SI1_STROBE1**	
AA3	IIC4_SCL/GPIO4_02/EVT5_B	IIC4_SCL/GPIO4_02/EVT5_B/**DIU_HSYNC**	Additional DIU functionality is available in T1040 over I2C pins.
AB3	IIC4_SDA/GPIO4_03/EVT6_B	IIC4_SDA/GPIO4_03/EVT6_B/**DIU_VSYNC**	

Pinout Comparison

QE/DIU pins			
Pin	**T2081**	**T1040**	**Compatible connection**
P4	RSVD15	**CLK09/GPIO4_15/BRG02/DIU_D10**	QE and DIU are only available on T1040. If unused, configure the pins as GPIO and leave as NC
P3	RSVD14	**CLK10/GPIO4_22/BRG03/DIU_D11**	
N4	RSVD13	**CLK11/GPIO4_16/BRG04/DIU_DE**	
M4	RSVD12	**CLK12/GPIO4_23/BRG01/DIU_CLK_OUT**	
R2	RSVD17	**TDMA_RQ/GPIO4_14/DIU_D4/UC1_CDB_RXER**	
U1	RSVD23	**TDMA_RSYNC/GPIO4_11/DIU_D1/UC1_CTSB_RXDV**	
U2	RSVD24	**TDMA_RXD/GPIO4_10/DIU_D0/UC1_RXD7**	
R1	RSVD16	**TDMA_TSYNC/GPIO4_13/UC1_RTSB_TXEN/DIU_D3**	
T1	RSVD20	**TDMA_TXD/GPIO4_12/UC1_TXD7/DIU_D2**	
R4	RSVD19	**TDMB_RQ/GPIO4_21/DIU_D9/UC3_CDB_RXER**	
T3	RSVD21	**TDMB_RSYNC/GPIO4_18/DIU_D6/UC3_CTSB_RXDV**	
U4	RSVD25	**TDMB_RXD/GPIO4_17/DIU_D5/UC3_RXD7**	
R3	RSVD18	**TDMB_TSYNC/GPIO4_20/UC3_RTSB_TXEN/DIU_D8**	
T4	RSVD22	**TDMB_TXD/GPIO4_19/UC3_TXD7/DIU_D7**	

Pinout Comparison

LP_Trust pin			
R6	LP_TMP_DETECT_B	**RSVD15**	LP_Trust is only supported by T2081 Connect LP_TMP_DETECT_B to OVDD through a 10K resistor Pull up through a 10K resistor to 1.0V
P6	V_{DD}_LP	**RSVD13**	
SENSE pins			
AB9	RSVD28	**SENSEV$_{DDC}$**	Use SENSEV$_{DD}$ and SENSEGND
AB10	RSVD29	**SENSEGNDC**	
por_config pins			
D13	IFC_WE0_B	**cfg_eng_use[0]**	Used in T1040 for selection of single source clocking option. Do not use for common board.

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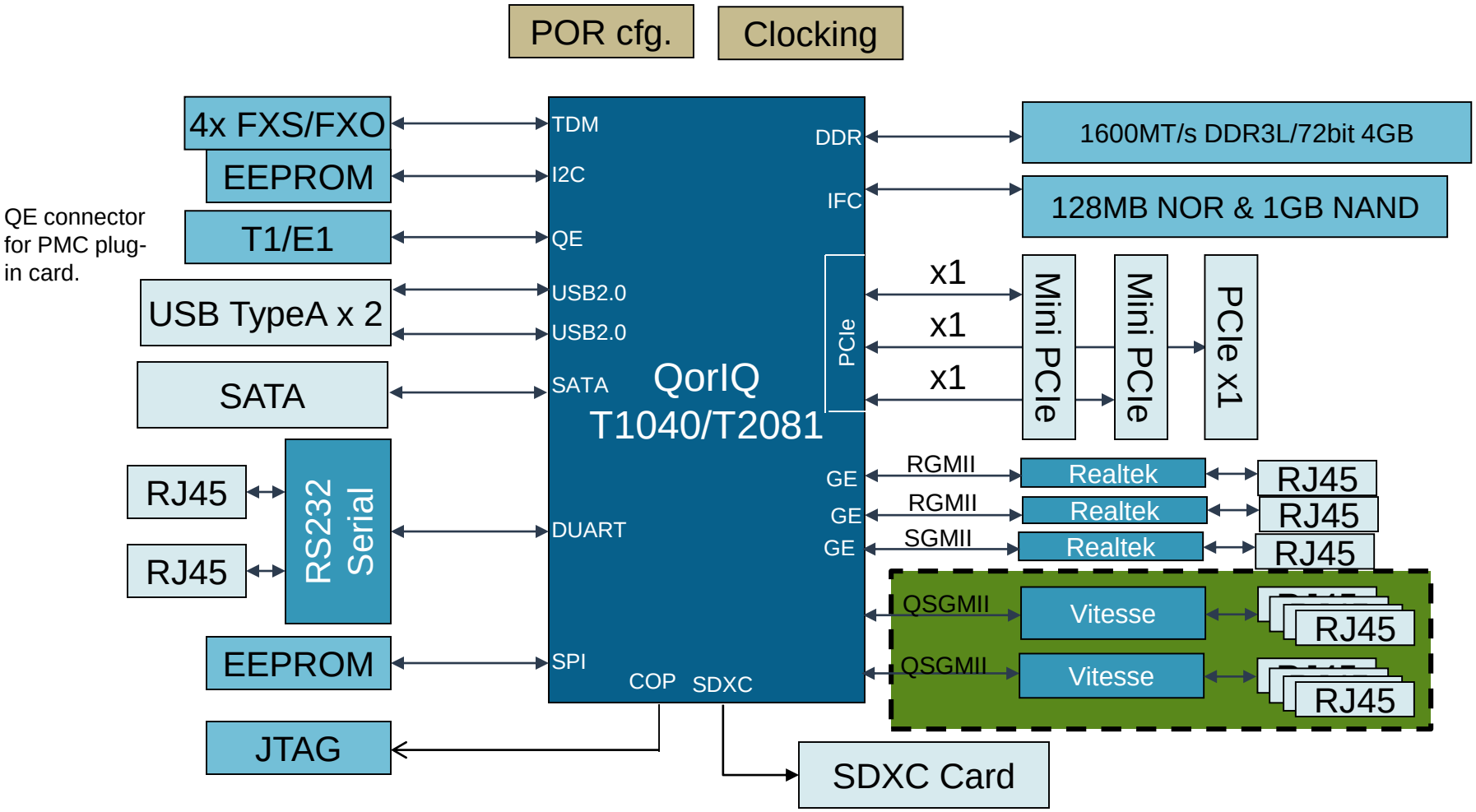
T1040/T2081 Software & Tools at a Glance

- Two Reference Design Boards
  - T1040RDB
  - T1042RDB
- Software Support
  - Yocto based SDK
  - SDK support includes
    - Legacy features (refer SDK 1.4 release notes)
    - New features
    - FMAN and QE microcode
    - Linux based QE drivers for TDM, UART and HDLC
- QorIQ Configuration Suite
- CodeWarrior based debugger, flash programmer

T1040/T2081 RDB System

T1040/T2081 RDB Block Diagram



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Reference Documentation

- T1040 Hardware Specification and Reference Manual
- T2081 Hardware Specification and Reference Manual
- Application Note (AN4733) T1040 to T2081 Migration Guide
- T1040/T2081 Design Checklist
- T1040 RDB User Manual
- T1040 RDB Schematic

Session Closing

- By now, you should be able to:
  - Use Freescale's design collateral to aid your own T1040 and T2081 designs
  - Understand the commonalities and differences between these devices
  - Understand the unique challenges facing T1040 and T2081 common design and the solutions to overcome them

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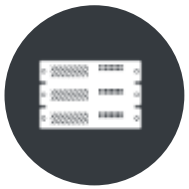

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- 4 PCIe Gen3 controllers, 1 with SR-IOV support
- 2 x SATA 3.0, 2 x USB 3.0 with PHY

Use a Common Board

- With the introduction of the T1040 and T2081, customers can now create common boards for both devices
  - T1040 and T2081 are pin compatible
  - One common board design would reduce design time and save cost
  - Make migration much faster and easier

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