Hardware Design Guidelines for S12 MagniV Mixed-Signal Microcontrollers

AMF-ACC-T1213

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freescale™

External Use

Agenda

- Introduction to MagniV
- Power Supply Pins
- Programming Interface
- External and internal RC Oscillator
- Programming Circuit
- CAN Physical Layer
- LIN Physical Layer
- High Current / High Voltage Pins
- Motor Control Interface
- MagniV in 24V Applications
- Summary

Introduction to MagniV MCUs

S12 MagniV: Integration Beyond the MCU

Our **S12 MagniV** portfolio simplifies system design with the integration on High-Voltage (HV) analog features onto MCUs for automotive applications

S12VR
Relay based DC Motors

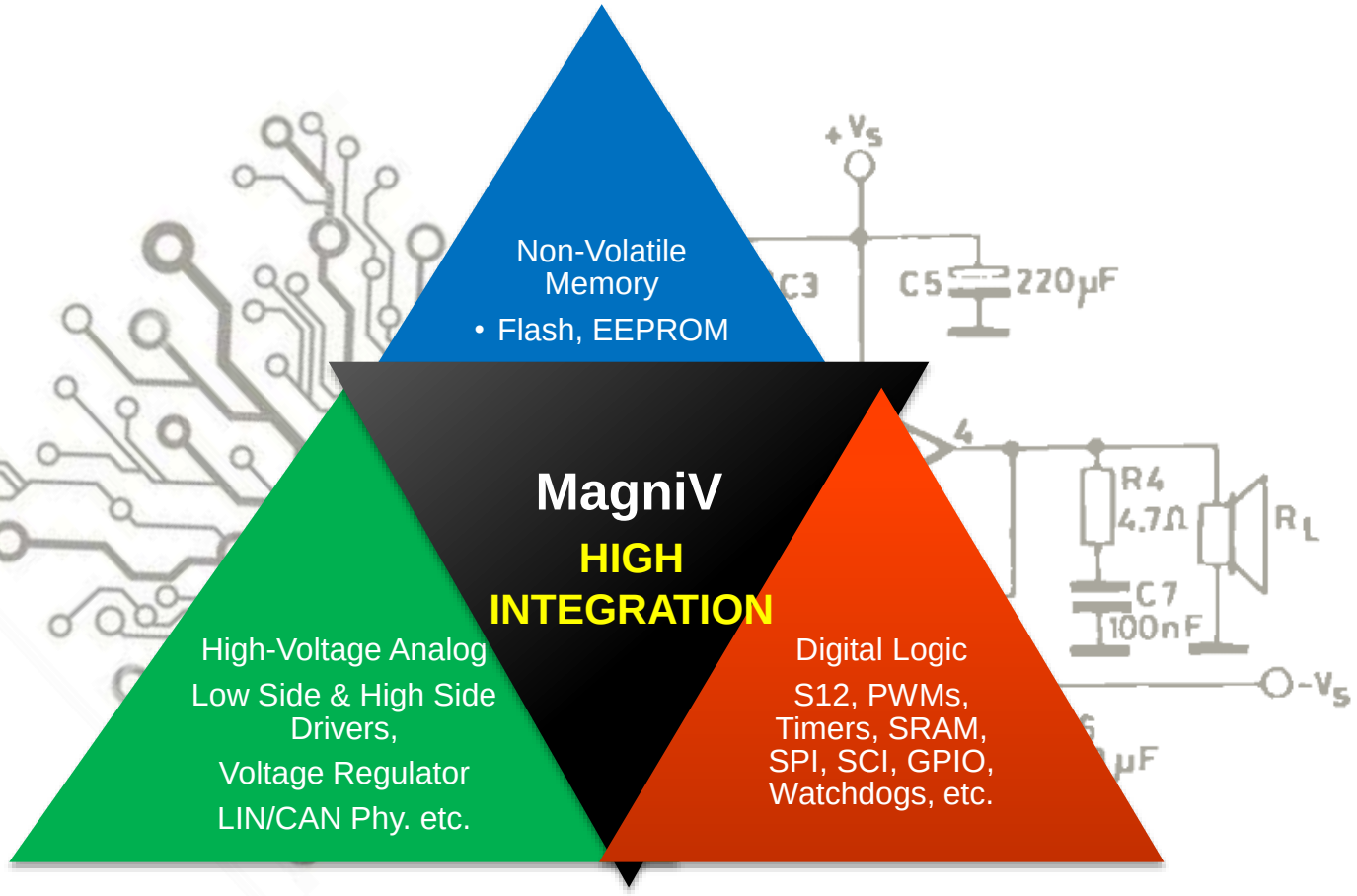
S12ZVM
BLDC Motor Control

S12ZVC
Small CAN nodes

S12ZVL
LIN Nodes

S12ZVH
Cluster Solutions

A Technology Sweet-spot for Sensor and Actuators



S12 MagniV Benefits

S12 MagniV solutions deliver optimal **system cost** **and physical footprint** for sensor and actuator applications.

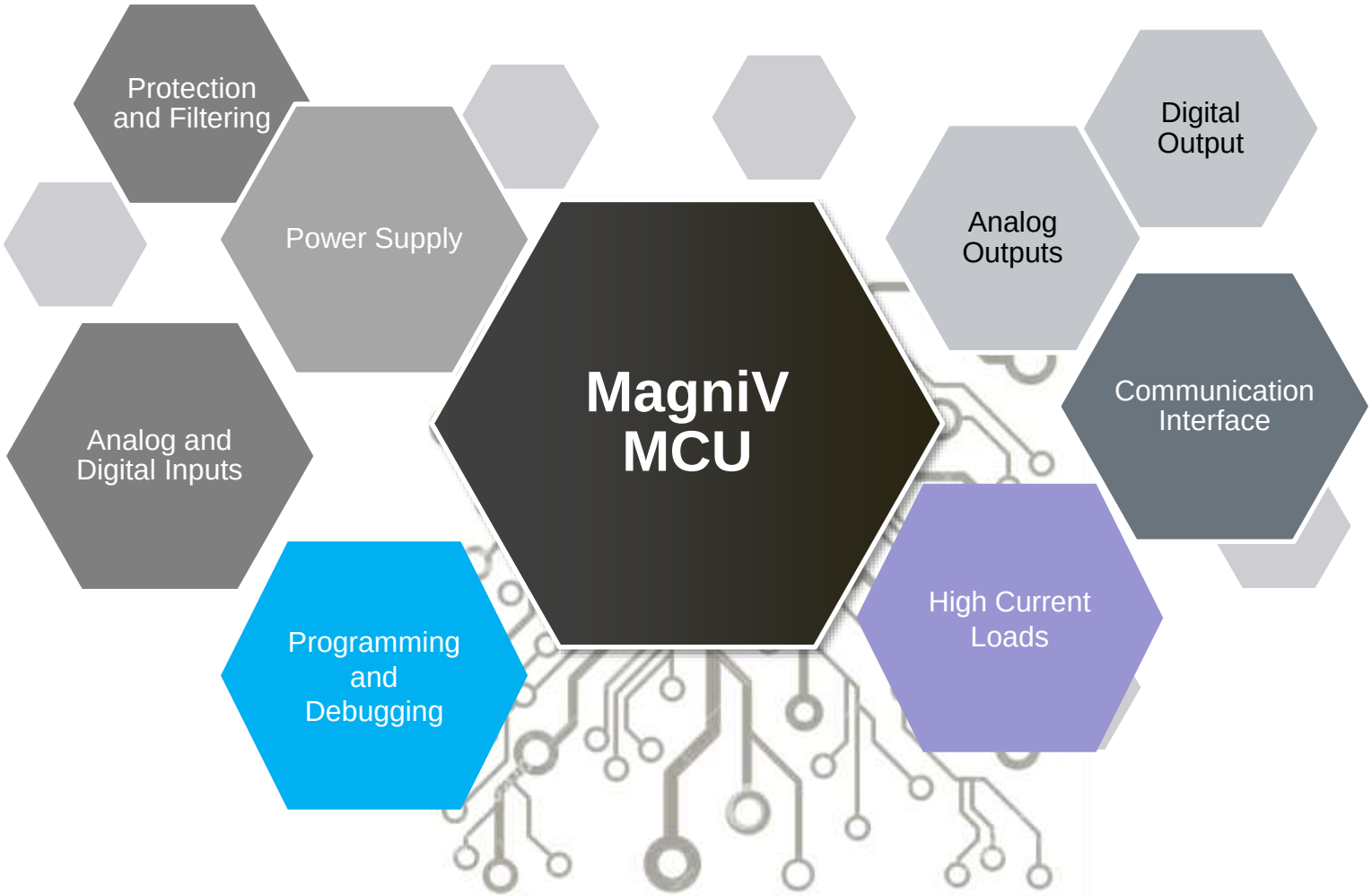
Reduced PCB Space
Up to 30%

Improved manufacturing efficiency
Replacing typically 3 IC by 1 MagniV reduces assembly and test cost while quality improves

Reduced Bill Of Material (BOM)
Fewer components to purchase, handle, store and qualify

Simplified motor control that speeds up time-to-market
Save up to 6 months on development, validation and ISO26262 implementation
- Abstract the complexity of 3-phase motor control software development
- Production ready Automotive quality SW and Tools
- SafeAssure program

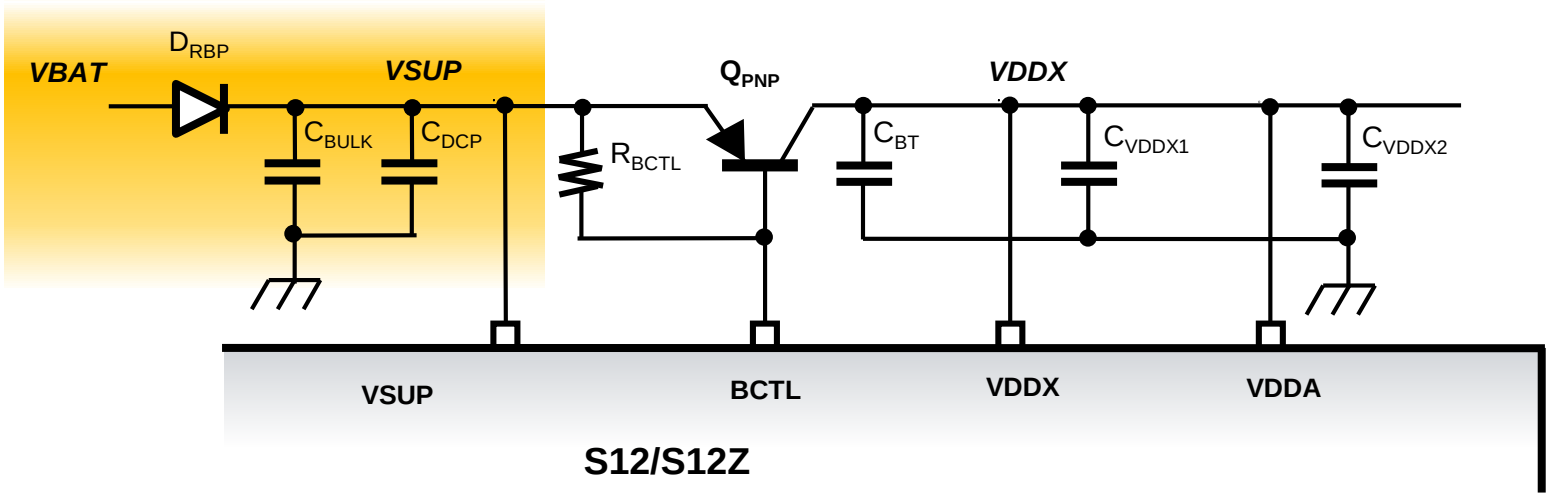
High Level Functional Application



Power Supply Pins

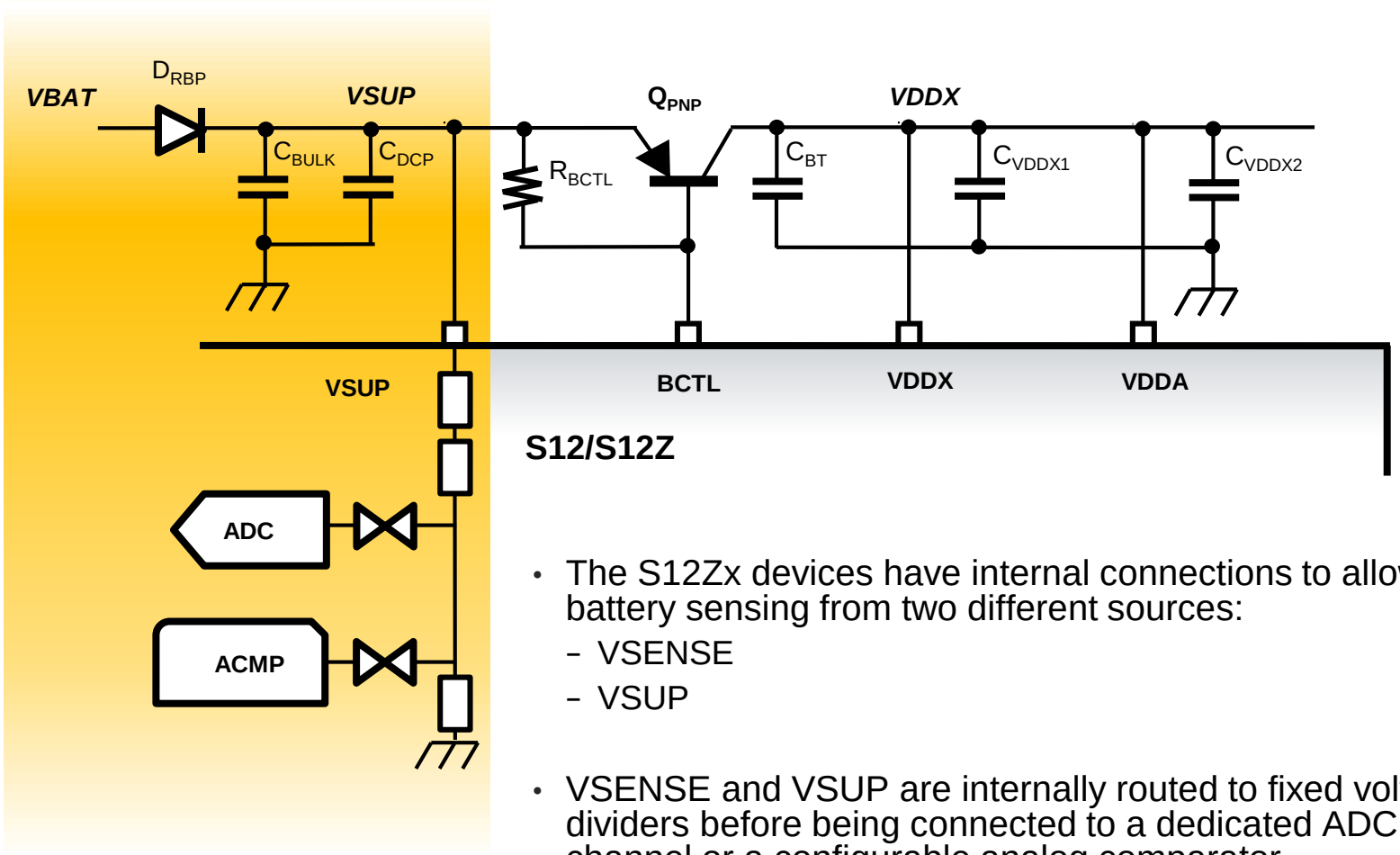
Battery sensing
PNP Ballast Transistor
Decoupling Capacitors

Power supply pins



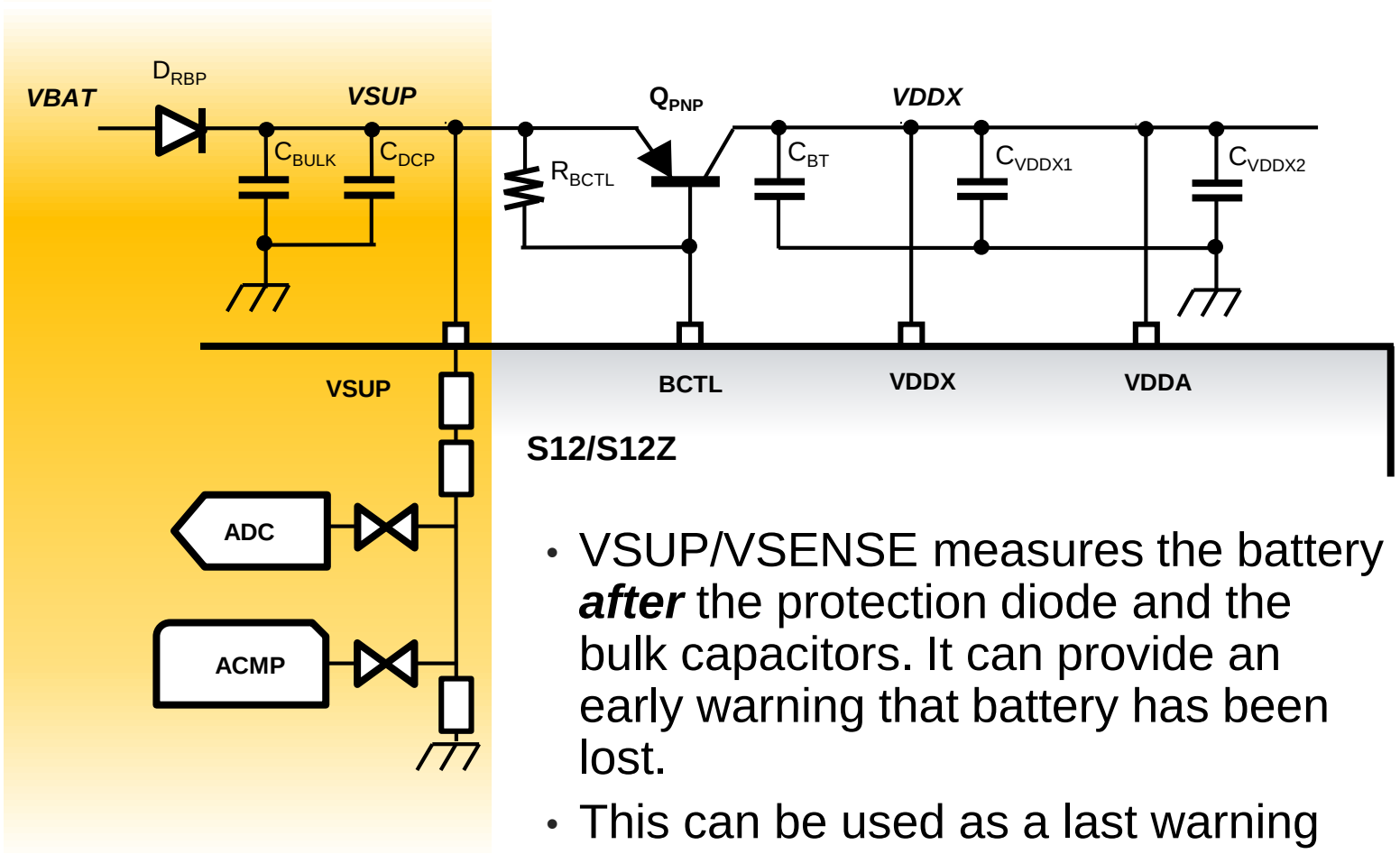
- VSUP is the 12V supply voltage pin for the on chip voltage regulator. This is the voltage supply input from which the voltage regulator generates the on chip voltage supplies.
- It must be protected externally against a reverse battery connection. The simplest protection against reverse battery protection is a diode in series with the battery.

Battery sensing



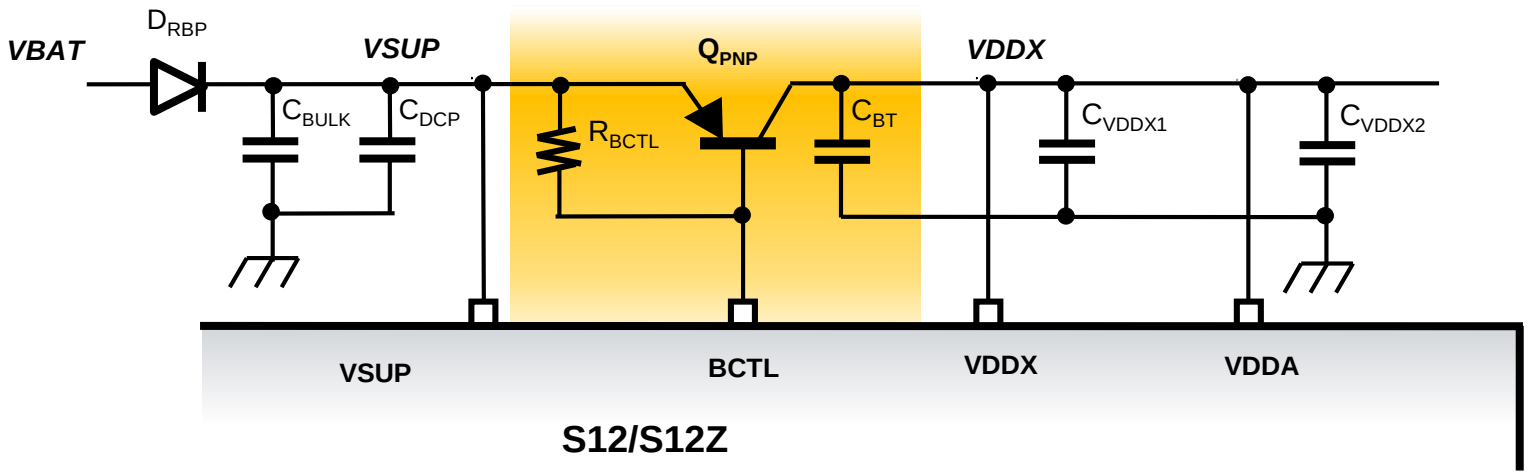
- The S12Zx devices have internal connections to allow battery sensing from two different sources:
  - VSENSE
  - VSUP
- VSENSE and VSUP are internally routed to fixed voltage dividers before being connected to a dedicated ADC channel or a configurable analog comparator.

Battery sensing



- VSUP/VSENSE measures the battery ***after*** the protection diode and the bulk capacitors. It can provide an early warning that battery has been lost.
- This can be used as a last warning that power is failing or ignition status.

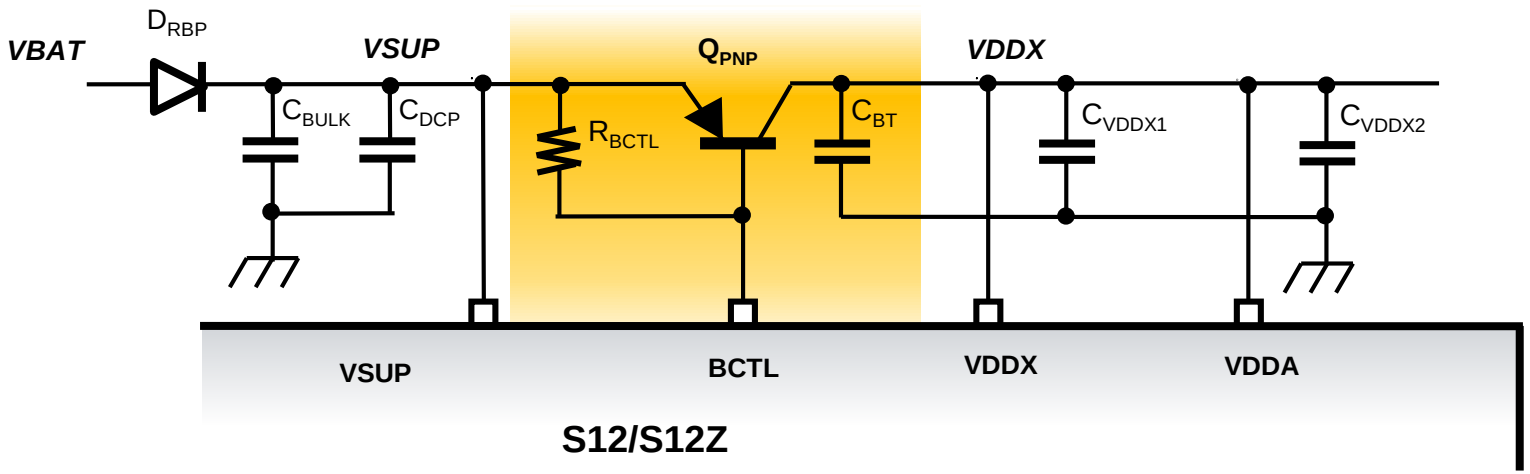
VDDX Ballast transistor



- The external ballast device function extends current capability and reduces internal power dissipation.

- **BCTL** - Base Control Pin for external PNP: BCTL is the ballast connection for the on chip voltage regulator. It provides the base current of an external BJT (PNP) of the VDDX and VDDA supplies. An additional 1 KΩ resistor between emitter and base of the BJT is required

VDDX Ballast transistor



- The maximum output current capability [I_{VDDX}] using a PNP External Ballast transistor [Q_{PNP}], must be determined by the allowed maximum power of the device. The designer should to consider that the maximum power dissipation of the transistor will depend mainly on the following factors:
  - Package type
  - Dissipation mounting pad area on the PCB
  - Maximum Ambient temperature (Application)

Power supply pins

6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air					
	BCP53		[1]	-	-	192	K/W
			[2]	-	-	125	K/W
			[3]	-	-	93	K/W
	BCX53		[1]	-	-	250	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm^2.

[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm^2.

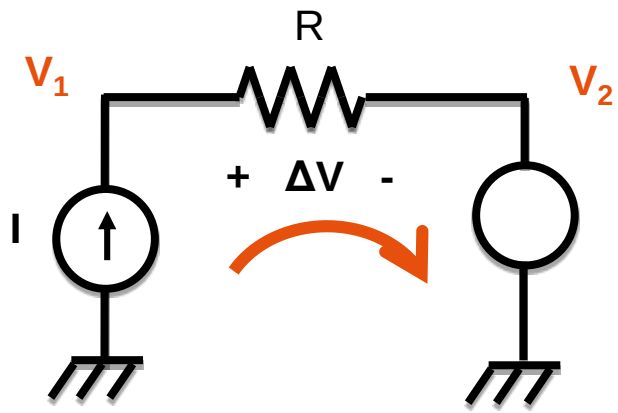
[4] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.

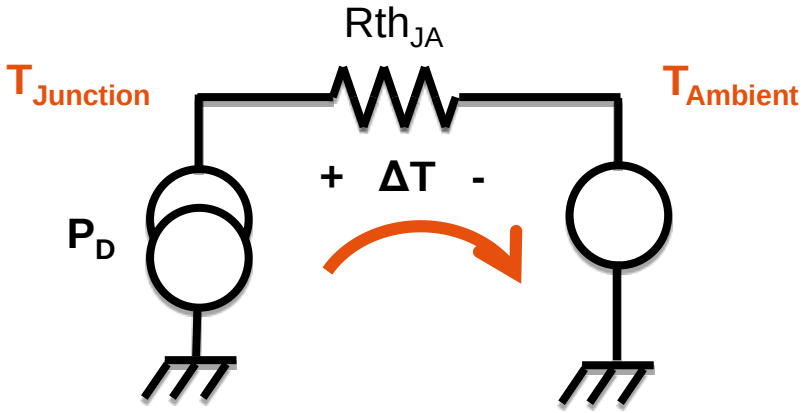
[5] Device mounted on an FR4 PCB, 4-layer copper, tin-plated, mounting pad for collector 1 cm^2

$$PWR_{MAX} = \frac{TJ_{MAX} - T_{AMB}}{Rth_{JA}}$$

PWR_{MAX} - Maximum power dissipation allowed.
TJMAX – Maximum junction temperatura
T_{AMB} – Ambient Temperature
Rth_{JA} – Thermal Resistance Junction to ambient

Electrical vs. Thermal DC Parameters





$\Delta V = (V_1 - V_2) = I * R$

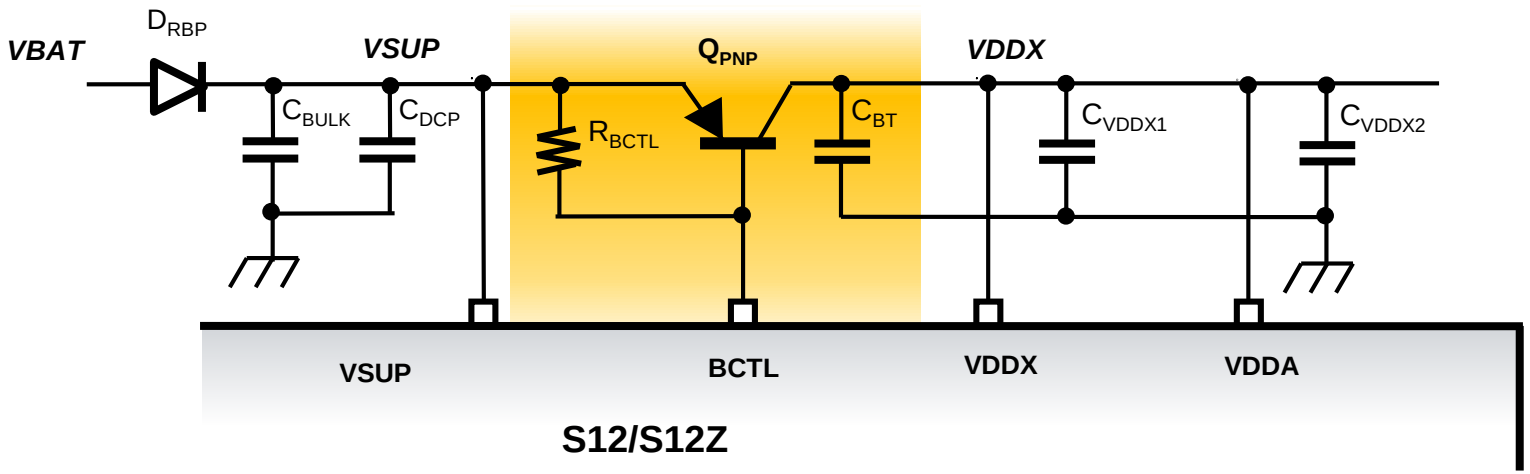
$\Delta T = (T_J - T_{AMB}) = P_D * R_{TH}$

R = Electrical Resistance (Ω)
V = Potential Difference (V)
I = Current (A)

R_{th} = Thermal Resistance (C/W)
ΔT = Temperature Difference (C)
P_D = Power Dissipated (W)

$$\mathbf{PWR_{MAX}} = \frac{\mathbf{TJ_{MAX}} - \mathbf{T_{AMB}}}{\mathbf{Rth_{JA}}}$$

Power supply pins



- **VBAT** = 12V
- **VFWD** = 0.7V
- **VSUP** = VBAT - VFWD = 11.3V
- **VDDX** = 5V
- **TJ** = +150 °C
- **TAMB** = +25°C
- **RthJA** = 125 K/W

$$PWR_{PNP} = \frac{\mathrm{TJ_{MAX}} - \mathrm{T_{AMB}}}{\mathrm{Rth_{JA}}} = \frac{(+150°\mathrm{C}) - (+25°\mathrm{C})}{125\,{}^{K}/_{W}}$$

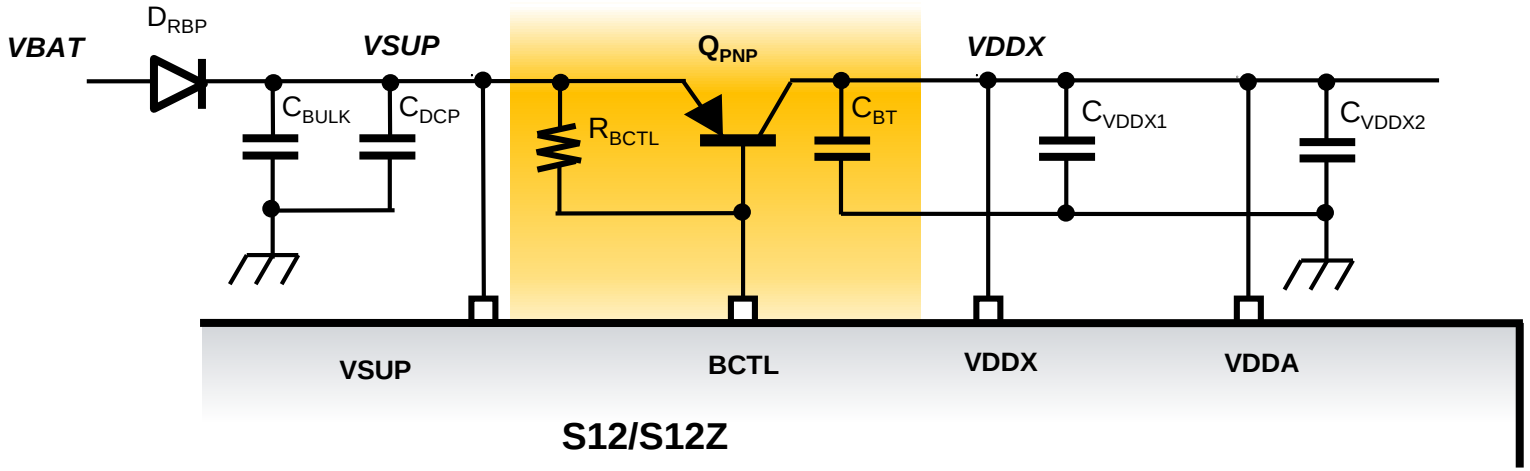
$$PWR_{PNP} = 1W$$

$$I\_VREG_{\mathrm{OUT}} = \frac{PWR_{PNP}}{VSUP - VDDX} = \frac{1W}{12V - 5V} = 142.85mA$$

$$I\_VREG_{\mathrm{OUT}} = 142.85mA$$

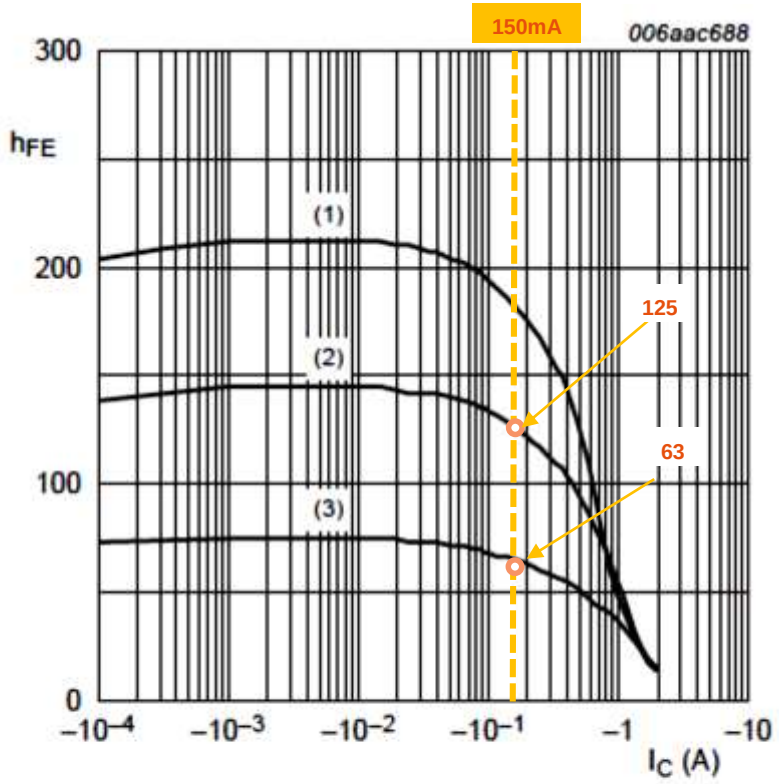
http://www.endmemo.com/convert/thermal%20resistance.php

Power supply pins



- Transistor specifications give the minimum and maximum gain.
- The worst case is usually significantly lower than the nominal figure on the transistor datasheet cover page. Furthermore, the datasheet values are usually given at room temperature (+25 °C).
- The required gain should be calculated at cold temperature, because a PNP/NPN transistor has minimum gain at low temperature.
- The worst case gain at cold temperature can be obtained from the transistor supplier or can be estimated using the graphs given in the transistor datasheet.

Power supply pins



V_{CE} = −2 V

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

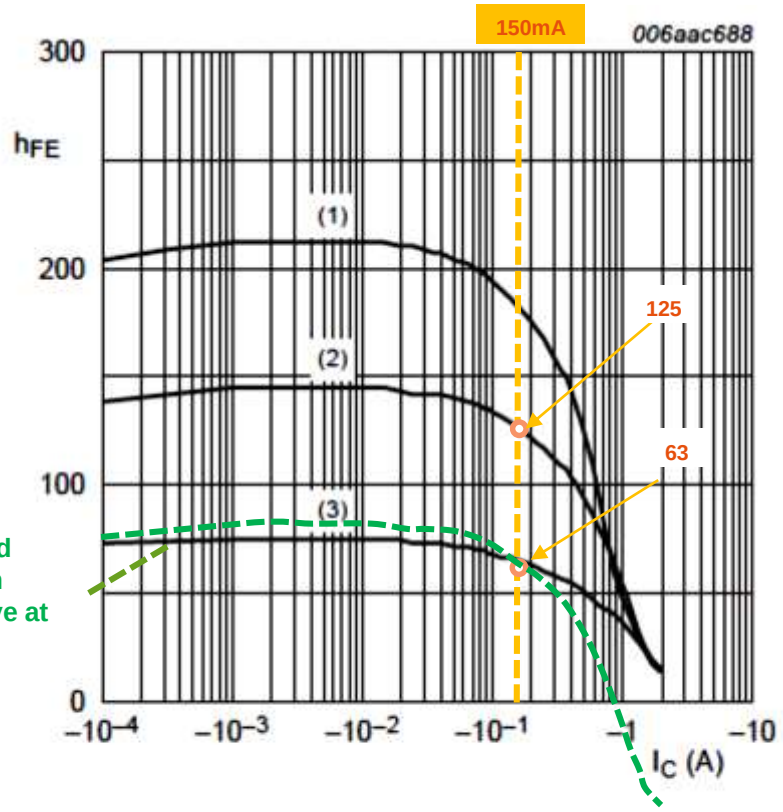
(3) T_{amb} = −55 °C

Quick reference data *...continued*

Parameter	Conditions	Min	Typ	Max	Unit
DC current gain	V_{CE} = −2 V; I_C = −150 mA	63	-	250	
h_{FE} selection -10	V_{CE} = −2 V; I_C = −150 mA	63	-	160	
h_{FE} selection -16	V_{CE} = −2 V; I_C = −150 mA	100	-	250	

Step1:
Estimate the minimum beta curve at 150mA +25C
Minimum beta is 63 at 150mA, 25C

Power supply pins



Estimated minimum beta curve at +25°C

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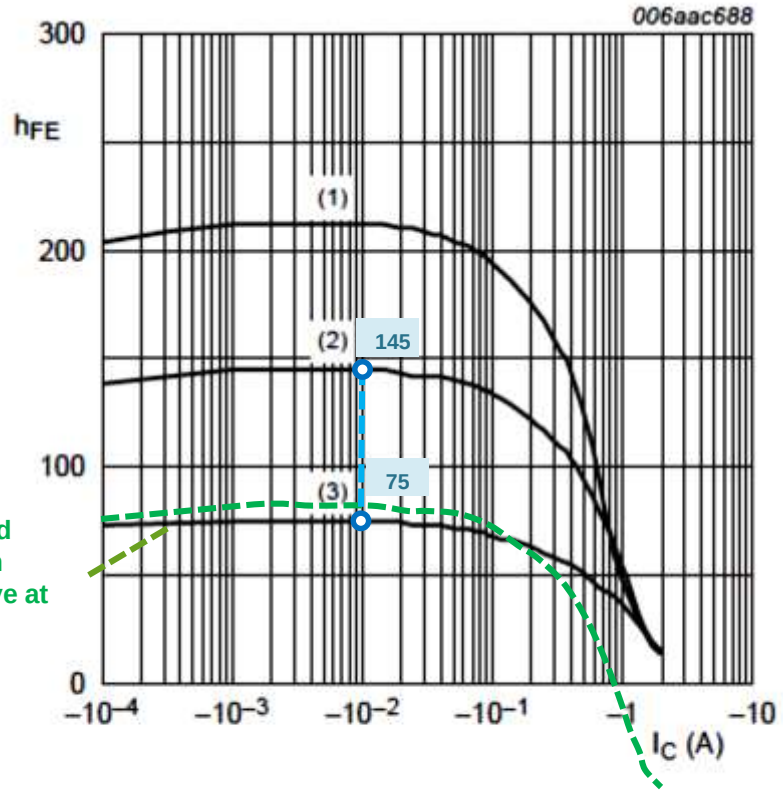

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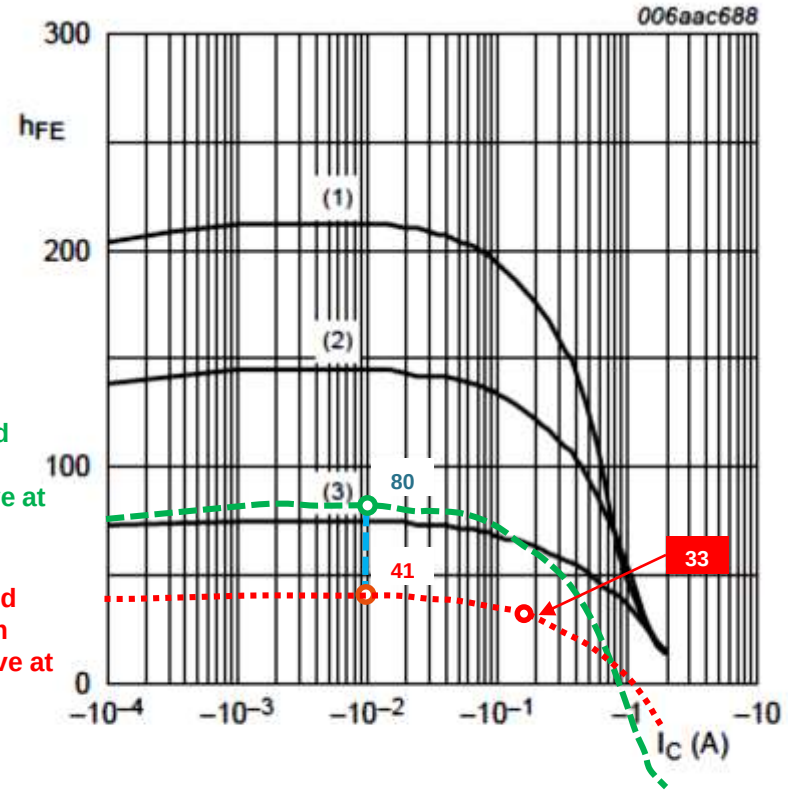
Minimum beta is 63 at 150mA, 25C

Step 2:
Determine temperature coefficient of beta at 10mA from data sheet.

$$= \frac{100\% \times \frac{(145-75)}{145}}{+25°C-(-55°C)} = \frac{48.275}{80} = 0.60\ \%/°C$$

Power supply pins



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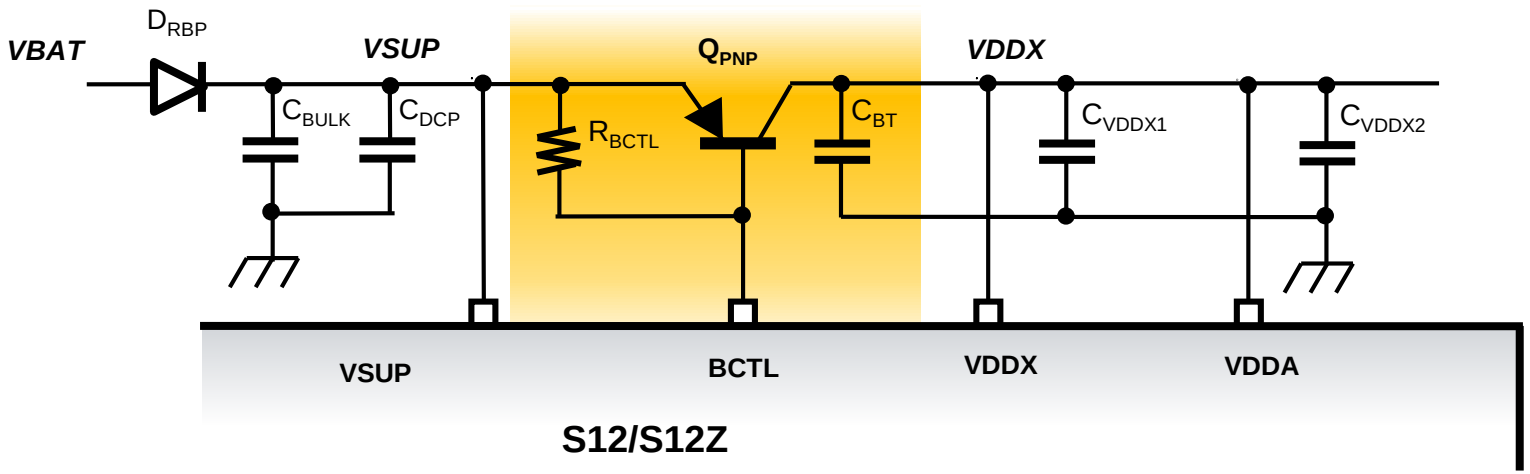
Minimum Beta at -40°C @ 10mA

$$= 80 - (0.60\,\%/{}^{\circ}C * (+25°C - (-40°C)))$$

$$= 80 - (0.60\,\%/{}^{\circ}C * (+60°C) = 41$$

Then we can estimate the minimum beta @150mA, **~33**

Power supply pins

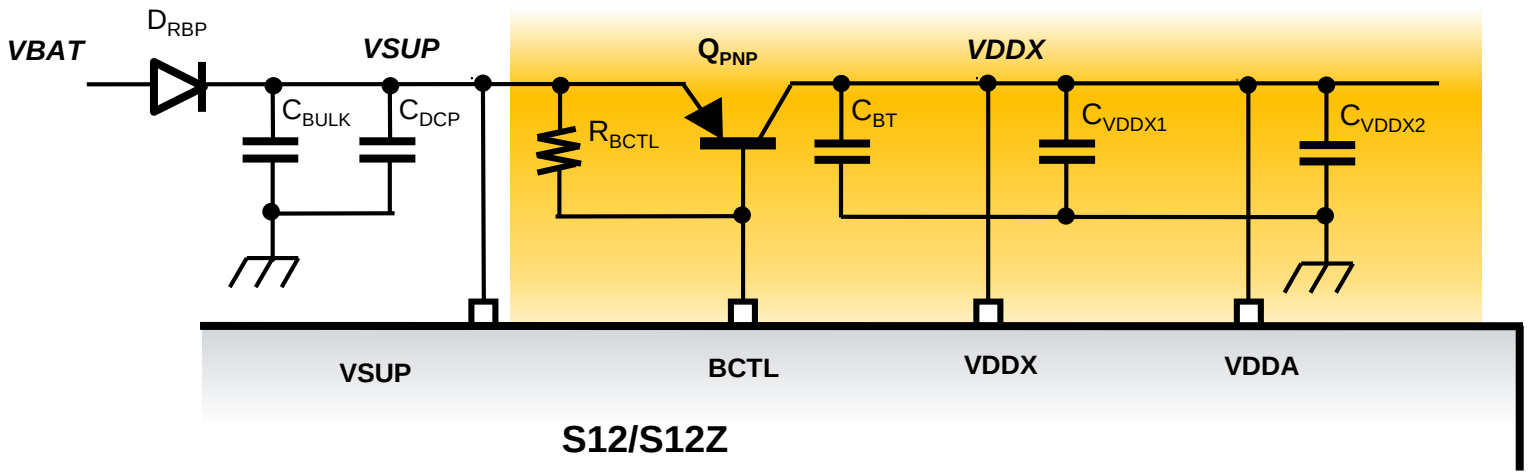


S12/S12Z

Part Number	Package Type	Manufacturer
BCP53	SOT- 223	NXP
		FAIRCHILD
2SB1260 / 2SB1181	SOT-89	ROHM
	DPAK	
2SA1952	DPAK	ROHM
2SB1181	SOT-89	ROHM
TBV	DPAK	

- Develop a Static Thermal Analysis, and select the appropriate package.
- VCEO parameter acording to the customer requirments.
- Avoid transistors with super betas or >500.
- Make sure worst case hFE at low temperature remains above 30 to avoid the quasi-saturation or saturation condition.

Power supply pins

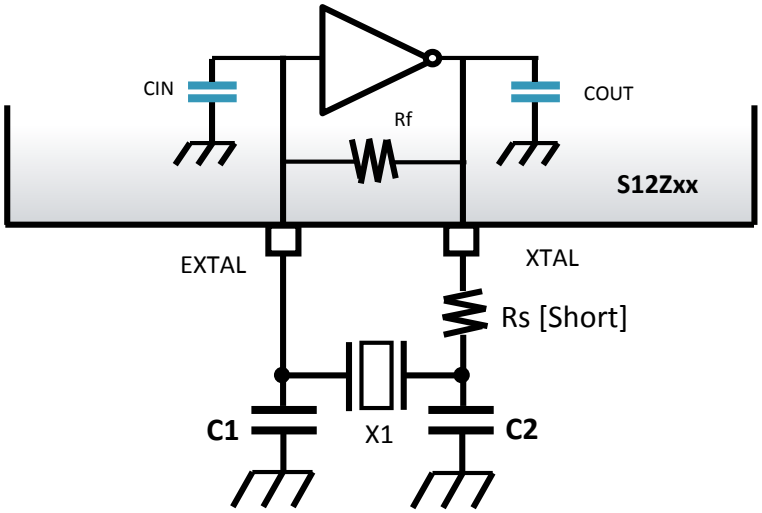


Symbol	Characteristic	Value
R_{BCTL}	Metal Film resistor	1 kΩ
C_{BCTL}	X7R Ceramic or Tantalum	10 uF
C_{VDDX1}	X7R Ceramic	220 nF
C_{VDDX2}	X7R Ceramic	220 nF

External and Internal RC Oscillator

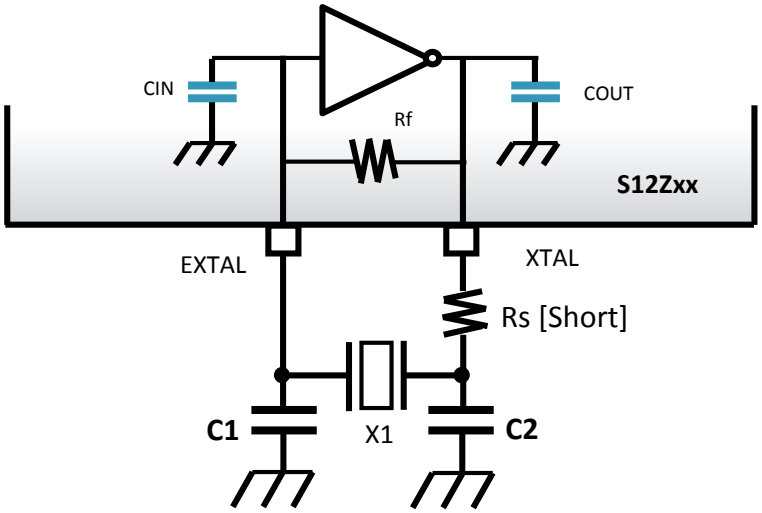
External and Internal RC Oscillator

- The S12Z devices have an internal 1 MHz internal RC oscillator with +/- 1.3% accuracy over rated temperature range.
- There is an alternative to add an external resonator or crystal, for higher and tighter tolerance frequencies.
- Oscillator pins shared with GPIO functionality
- The oscillation mode is selectable by software.



External and Internal RC Oscillator

- The effective load capacitance, CLOAD, appears to the crystal circuit as the series combination of C1 and C2. Correct CLOAD is important for proper operating frequency. Crystals are available with a variety of CLOAD values.
- It is recommended to select a fundamental mode parallel resonant type crystal having a C_{LOAD} of around 12 pF and ESR of 30 to 60 Ω.
- The actual discrete values required for C1 and C2 are generally up to 12 pf below the calculated load capacitance due to PCB traces and the input pin's stray capacitances; the board layout is quite important.



External and Internal RC Oscillator

The following formula may be used to calculate a parallel resonant crystal's external load capacitors:

$C_{LOAD} = ((C_1 \times C_2) / (C_1 + C_2)) + C_{STRAY}$

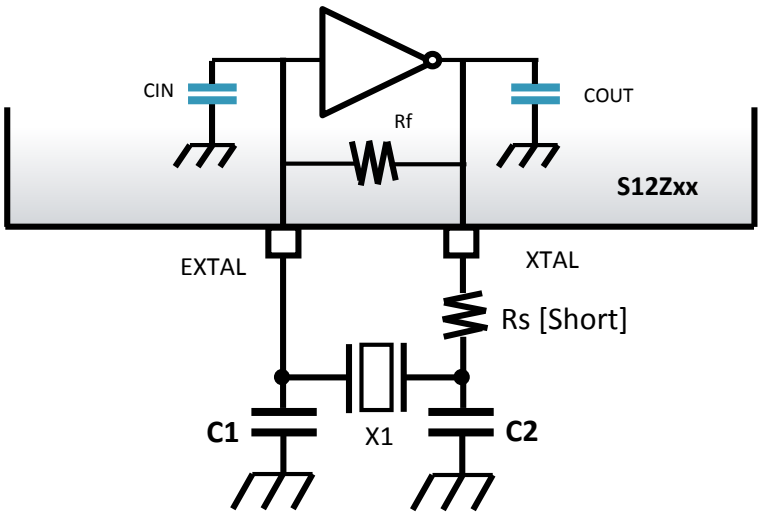
Where:
CL = the crystal load capacitance
Cstray = the stray capacitance in the oscillator circuit,

Which will normally be in the 2pF to 5pF range. Assuming that $C_1 = C_2$ then the equation becomes:

$C_{LOAD} = ((C_1 \times C_1) / (2 \times C_1)) + C_{STRAY}$
$C_{LOAD} = (C_1 / 2) + C_{STRAY}$

Rearranging the equation, we can find the external load capacitor value:

$C_{1,2} = 2(C_{LOAD} - Cstray)$

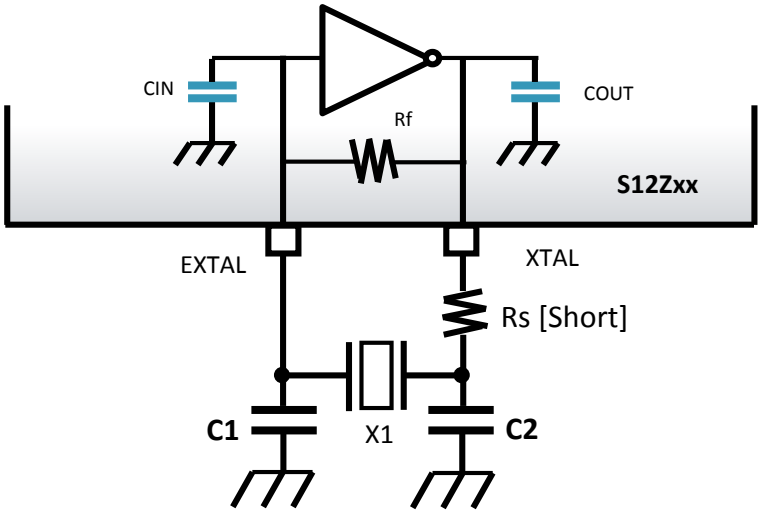


External and Internal RC Oscillator

For example, if the crystal load capacitance is 8pF, and assuming Cstray=3pF, then:

C1 = C2 = 2(8pF - 3pF) = 10pF

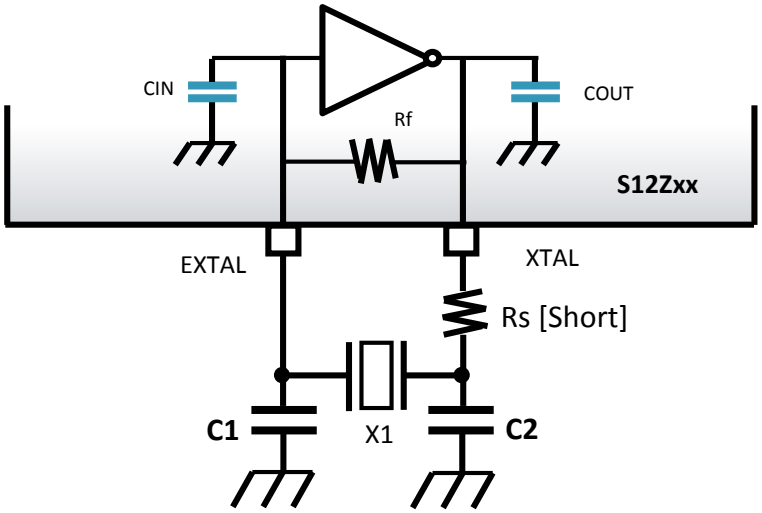
It is difficult to know exactly what the stray capacitance is, but if you find the oscillation frequency is too high, the load capacitor values can be increased. If the frequency is too low, the load capacitors can be decreased.



External and Internal RC Oscillator

- Resistance **Rs** is necessary for the prevention of abnormal oscillation.
- Install Resistance **Rs** on to the output side after checking the IC terminal function.
- Use the shortest distance for lines connecting parts, including ground lines, in order to prevent the inclusion of unnecessary stray capacitance.
- Do not allow any part of the oscillation circuit to cross over a signal line of any other circuit on the same circuit board.
- Normally, C1 and C2 should be **C0G / NP0** type ceramic capacitors for the best tolerance and temperature stability.

- NOTE: All quartz crystal oscillator and ceramic resonator circuits should be characterized by the supplier to make sure the oscillator/resonator is optimized to the particular IC, and that the required accuracy is achieved.



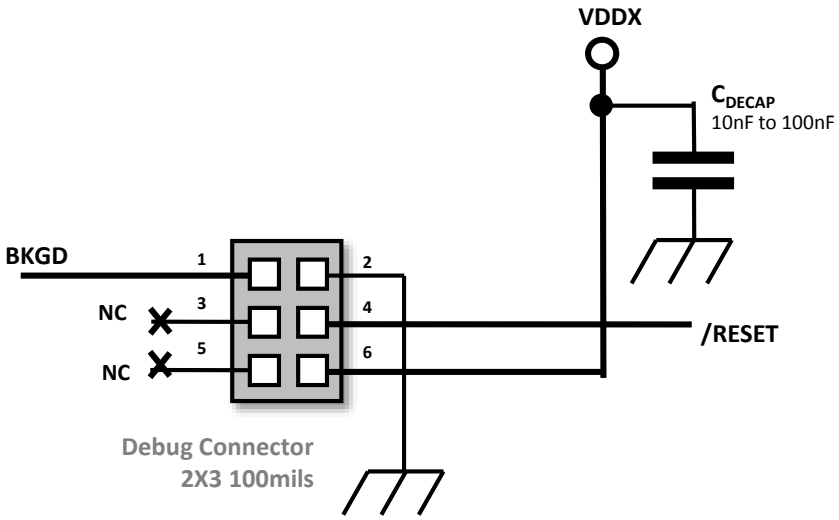
Programming Interface

BKGD pin

Reset pin

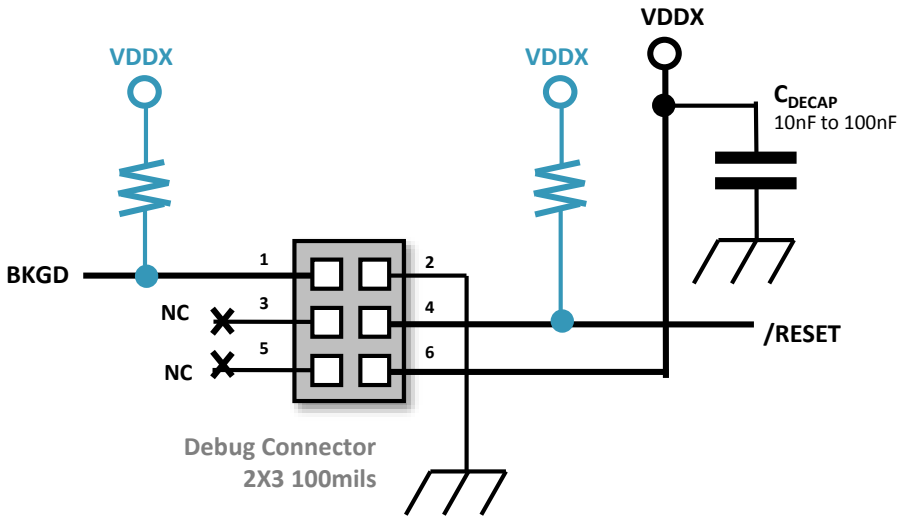
Programming Circuit

- The S12/S12Z family is programmed via the BDM protocol.
- The BDM protocol is a serial communication that is transmitted through the BKGD line.
- The standard BDM connector is a 2 by 3 pin header with 100 mil pitch.
- The BDM connector requires connection to the
  - **BKGD pin**
  - **RESET pin**
  - **VDDX Voltage**
  - **GND.**



Programming Circuit

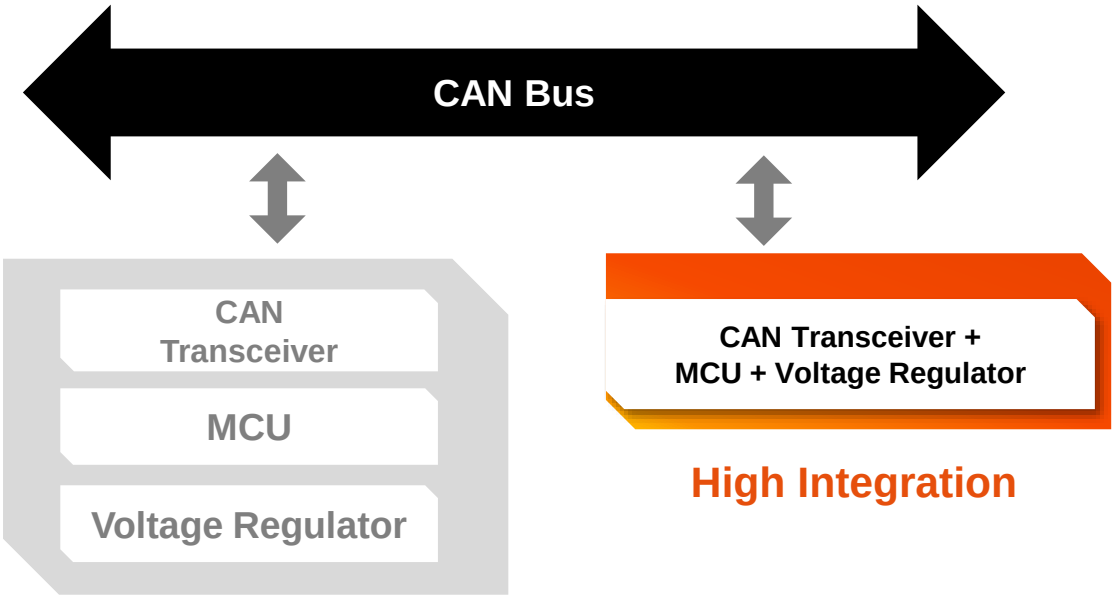
- It is recommended to add a ceramic capacitor to VDDX near the connector to reduce noise that could be injected by the programming circuitry to the power supply.
- The BKGD signal is used as a pseudo-open-drain signal for the background debug communication. **The BKGD pin has an internal pull-up device.**
- The RESET signal is an active low bidirectional control signal. It acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset. **The RESET pin has an internal pull-up device.**



CAN Interface

Hardware Design Guidelines for MagniV Mixed-Signal MCUs

CAN Physical Layer

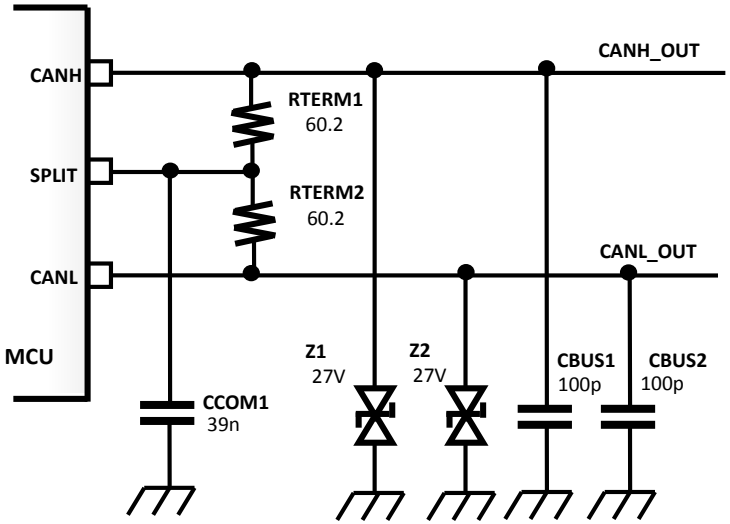


- Freescale offers a complete line of products to meet the needs of high-performance CAN embedded applications.

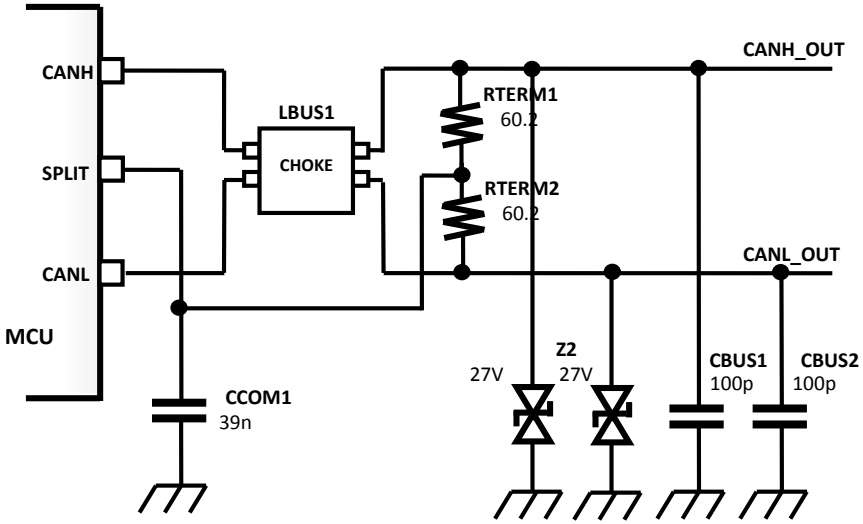
- MagniV MCUs as **S12ZVC** has an **on-chip** CAN physical transceiver and a dedicated power supply using an external ballast transistor for its. Having these modules on-chip helps reduce the total amount of components required to implement CAN communication.

CAN Physical Layer

- As any other CAN physical transceiver, the CANH, CANL and SPLIT pins are available for the designer to terminate bus depending on the application. The next figures show examples of CAN node termination:
  - CAN Physical transceiver circuit.
  - CAN Physical transceiver circuit with common mode choke.

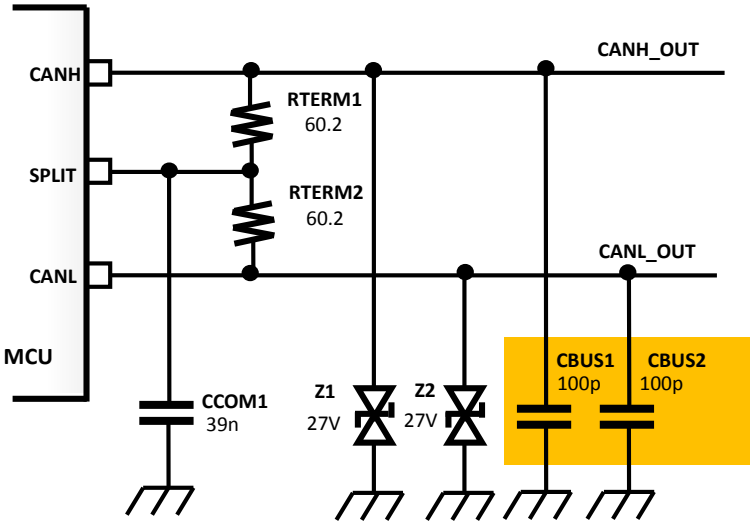


CAN Physical transceiver circuit.



CAN Physical transceiver circuit with common mode choke.

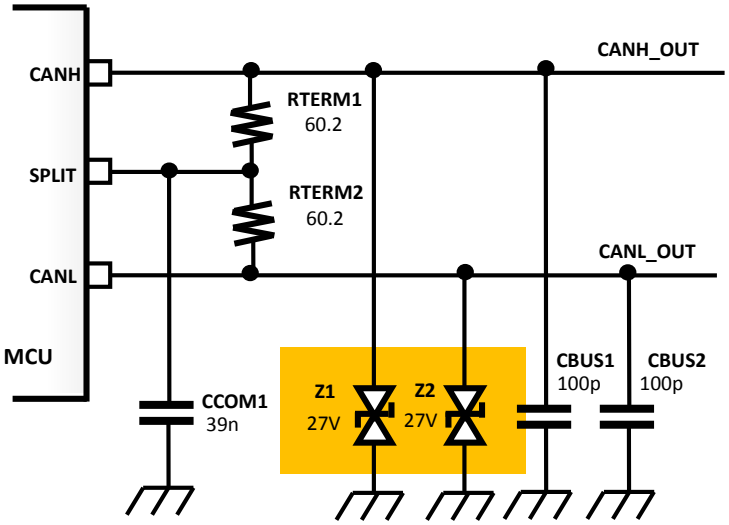
CAN Physical Layer



CAN Physical transceiver circuit.

Reference	Description
CBUS1 and CBUS2	The Capacitors CBUS1 and CBUS2 are not specifically required. They may be added for EMC reasons, in which case the maximum capacitance from either bus wire to ground must not exceed 300pF total. If zener stacks are also needed, the parasitic capacitance of the zener stacks must also be included in the total capacitance budget.
Z1 and Z2	The zener stacks Z1 and Z2 could be required to satisfy Automotive EMC requirements (ESD in particular). These devices should be placed close to the connector.

CAN Physical Layer



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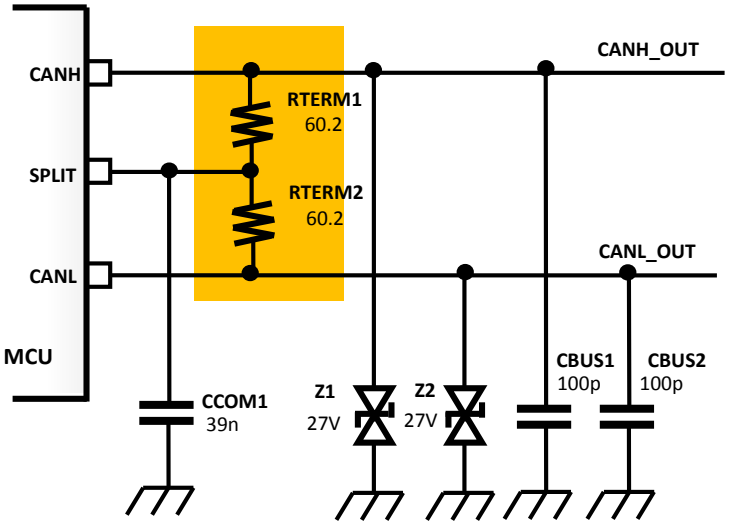
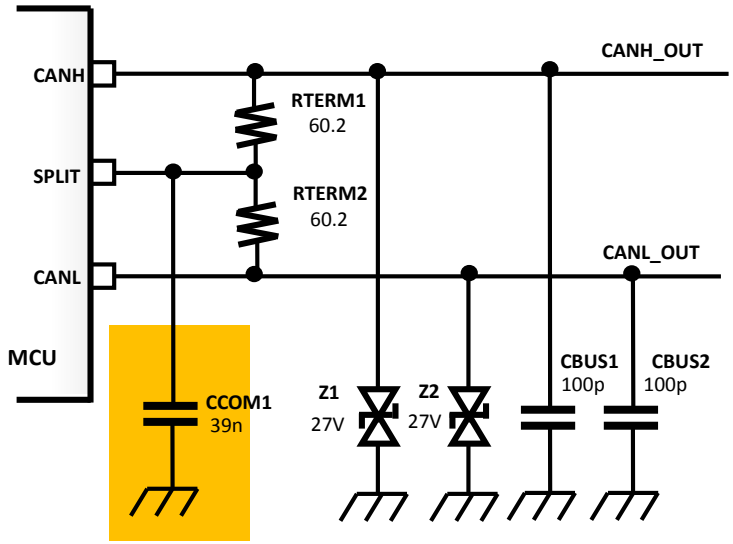


CAN Physical transceiver circuit.

Reference	Description
RTERM1 and RTERM2	Depending on the position of the node within the CAN network it might need a specific termination. $R_{TERM1,}$ R_{TERM2} and C_{COM1} must be that they assist in having an overall cable impedance. On a bus implementation of a CAN network only the two nodes on the two ends of the bus have terminator resistors. The nodes not placed on the end of the CAN bus do not have termination. A thorough analysis is required to maintain this requirement of the CAN networks.
CCOM1	The SPLIT pin on the transceiver is optional and the designer might choose not to use it. This pin helps stabilize the recessive state of the CAN bus and can be enabled or disabled by software when required.

CAN Physical Layer



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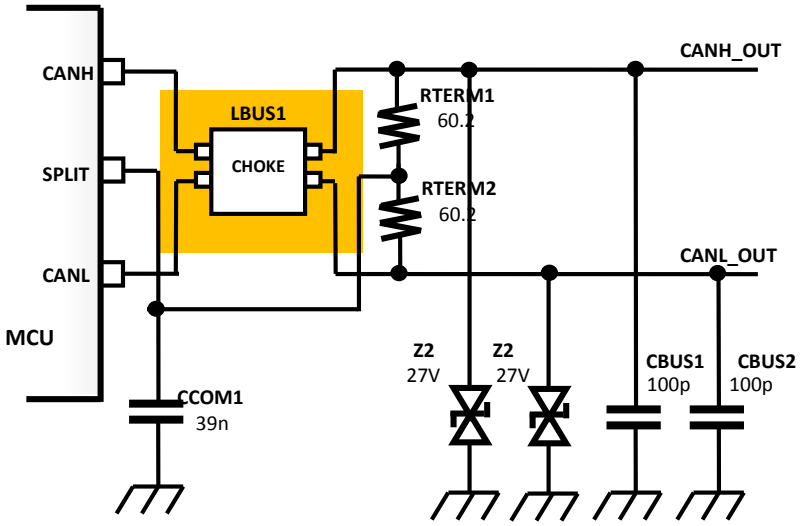


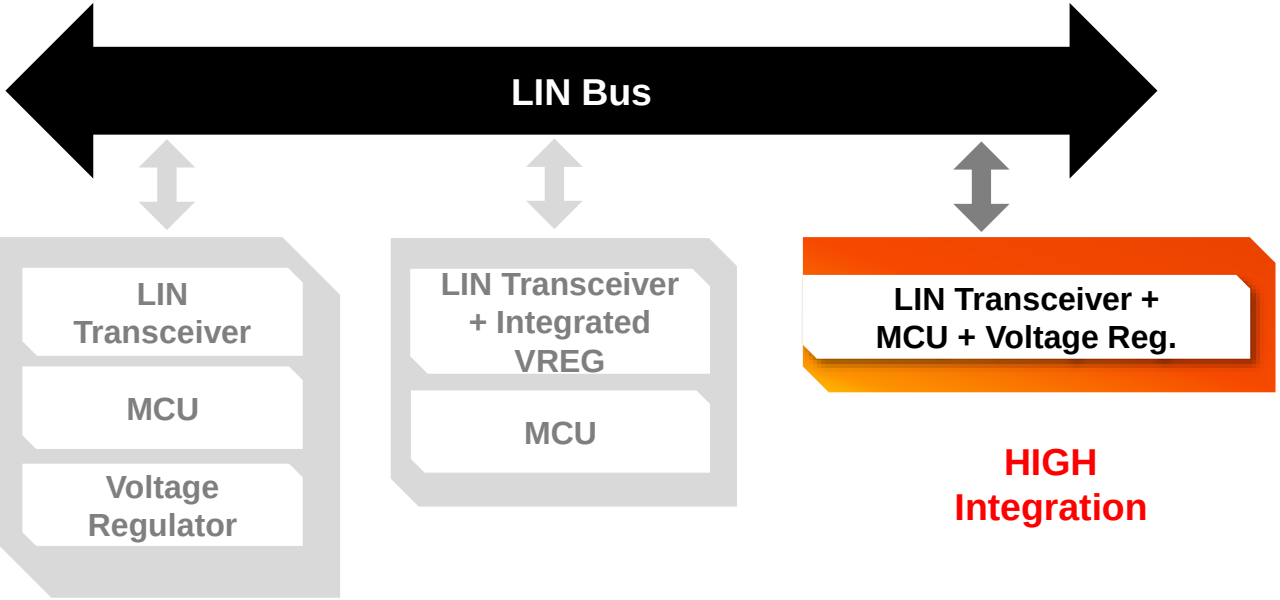
CAN Physical transceiver circuit with common mode choke.

Reference	Description
LBUS1 Common mode choke	A common node choke on the CANH and CANL lines can help reduce coupled electromagnetic interference and needed to satisfy Automotive EMC requirements. This choke, together with transient suppressors on the transceiver pins can greatly reduce coupled electromagnetic noise, and high-frequency transients.

LIN Interface

Hardware Design Guidelines for MagniV Mixed-Signal MCUs

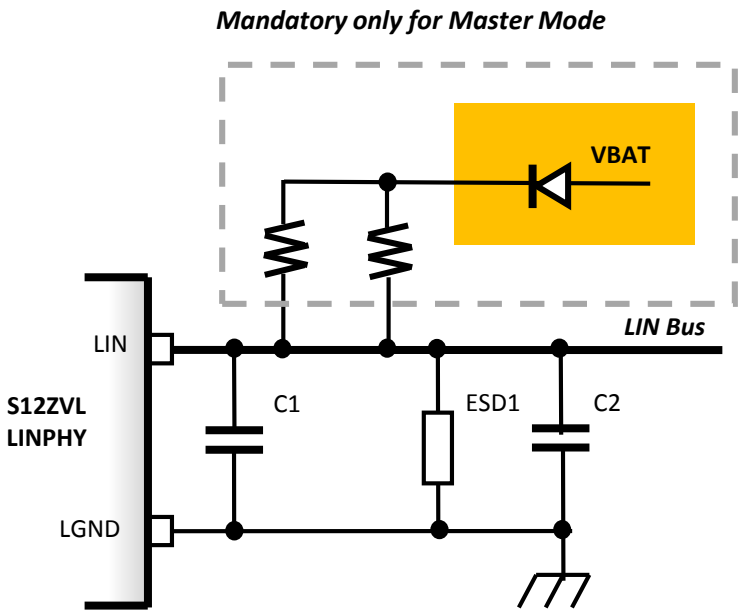
LIN Physical Layer



- Freescale offers a complete line of products to meet the needs of high-performance CAN embedded applications.

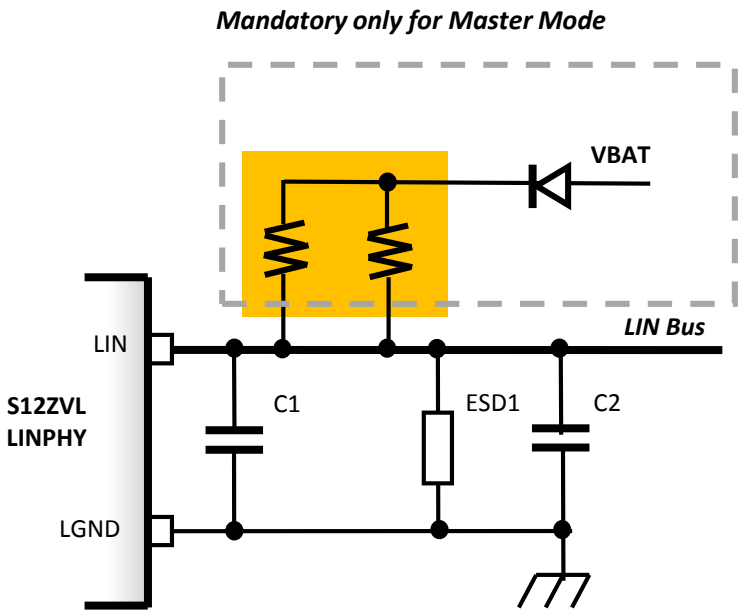
- MagniV MCUs as **S12ZVL** has an **on-chip** LIN physical transceiver and a dedicated power supply using an external ballast transistor for its. Having these modules on-chip helps reduce the total amount of components required to implement LIN communication.

LIN Interface



Reference	Part	Mounting	Remark
DMLIN	Diode	Mandatory only for master ECU	Reverse Polarity protection from LIN to VSUP.
RMLIN1 and RMLIN2	Resistor: 2kΩ Power Loss: 250mW Tolerance: 1% Package Size: 1206 Requirement: Min Power loss of the complete master termination has to be ≥ 500mW	Mandatory only for Master ECU	For Master ECU If more than 2 resistors are used in parallel, the values have to be chosen in a way that the overall resistance RM of 1kΩ and the minimum power loss of the complete master termination has to be fulfilled. For Slave ECU RMLIN1 and RMLIN2 are not needed on the PCB layout

LIN Interface



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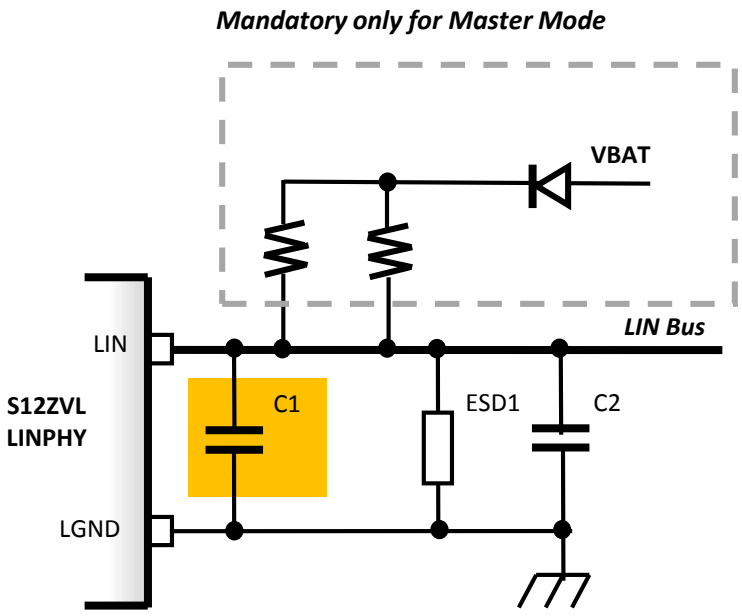
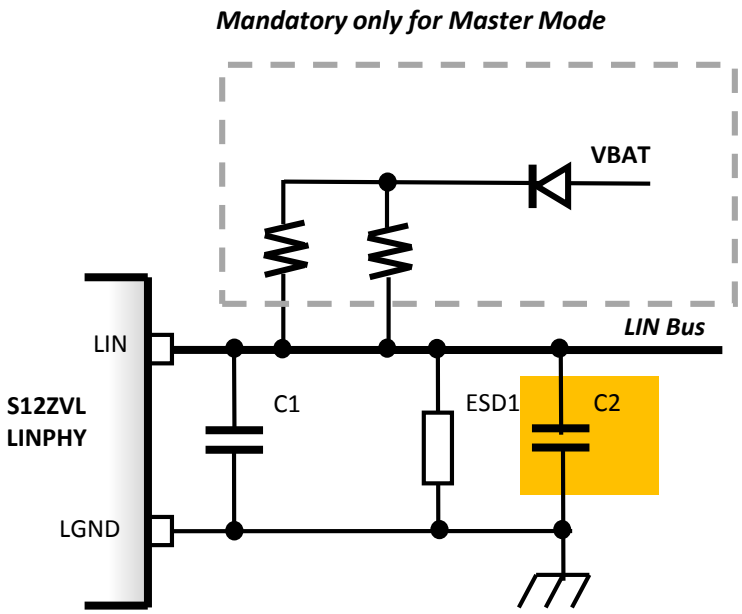
LIN Interface



Reference	Part	Mounting	Remark
C1	Capacitor: Master ECU: ≥560pF Slave ECU: 220pF Tolerance: 10% Package Size: 0805 Voltage: ≥50V	Mandatory	The value of the master node has to be chosen in a way that the LIN specification is fulfilled.
C2	Capacitor: Package Size: 0805	Optional	Mounting of the optional part only allowed if there is an explicit written permission of the respective OEM available. Placed close to the connector.

LIN Interface



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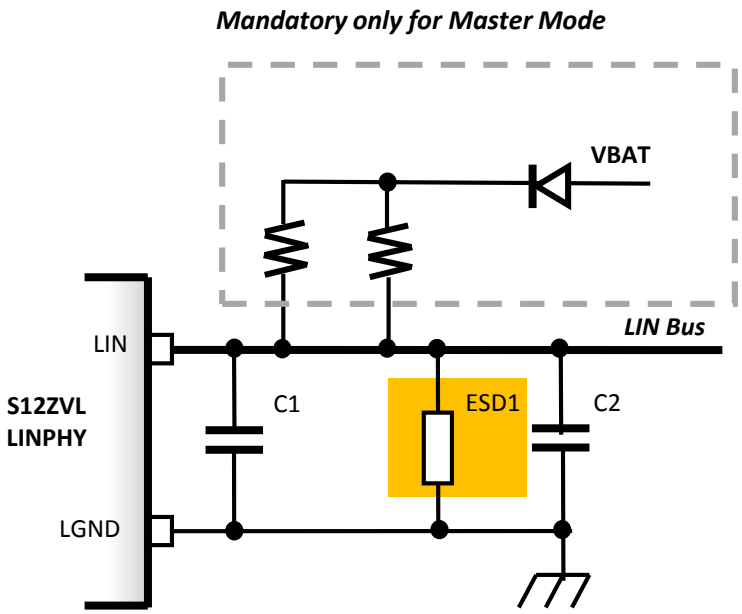
LIN Interface

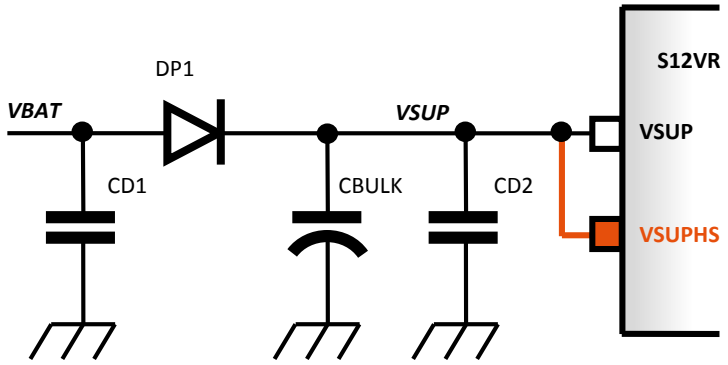


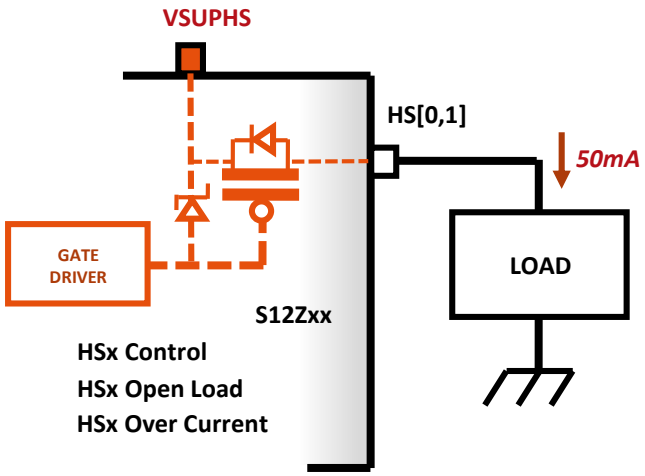
Reference	Part	Mounting	Remark
ESD	ESD Protection • Zener • MOV • TVS	Optional	Layout pad for an additional ESD protection part. Mounting of the optional part only allowed if there is an explicit written permission of the respective OEM available. Place close to the connector.

High Current / High Voltage Pins

High Side Drivers - HSDRV

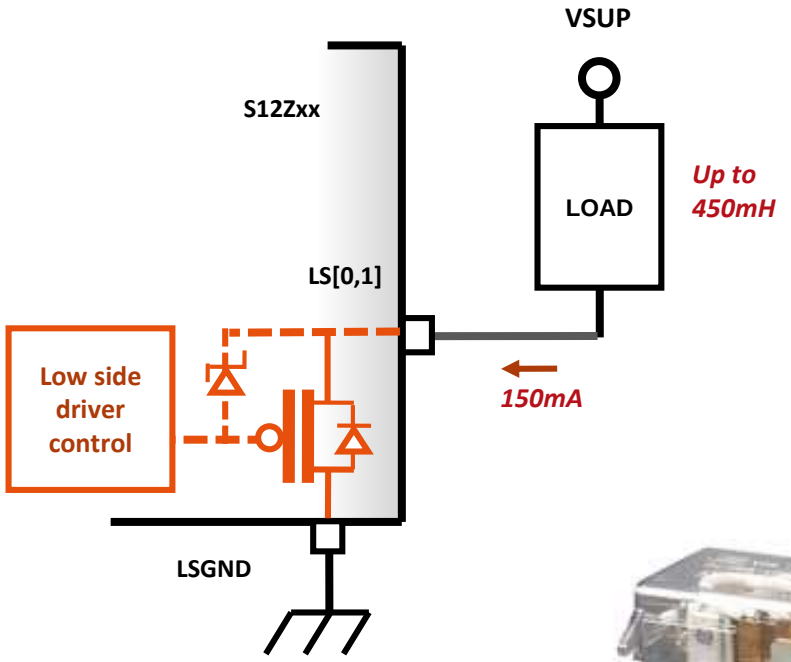
- The **HSDRV** module provides two high-side drivers. The nominal current for continuous operation to **50mA**. This value is valid for each HS-driver output.
- Both high-side drivers have a common high power supply **VSUPHS**. VSUPHS can support up to 18V.
- Selectable gate control of high-side switches:
  - HSDR[1:0] register bits,
  - PWM channel.
  - Timer channel.
- High-load resistance open-load detection when driver enabled and turned off.
- Over-current protection for the drivers, while they are enabled, including:
  - Interrupt flag generation.
  - Driver shutdown.

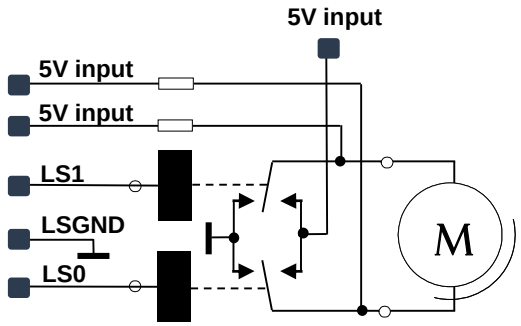




Low Side Drivers - LSDRV

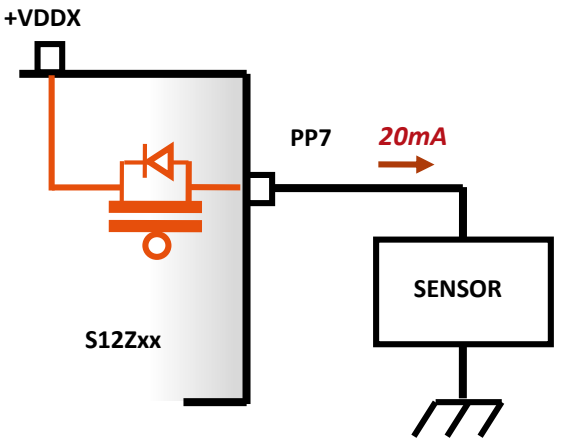
- The **LSDRV** module provides two low-side drivers typically used to drive inductive loads (relays). As inductive load up to **450mH**.
- The **LSDRV** module includes two independent low side drivers with common current sink.
- Selectable gate control of low-side switches:
  - LSDRx register bits,
  - PWM channel
  - Timer channel.
- Open-load detection while enabled
  - While driver off:
  - selectable high-load resistance
  - open-load detection
- **Over-current protection** with shutdown and interrupt while enabled.
- **Active clamp to protect the device against over-voltage** when the power transistor that is driving an inductive load (relay) is turned off.



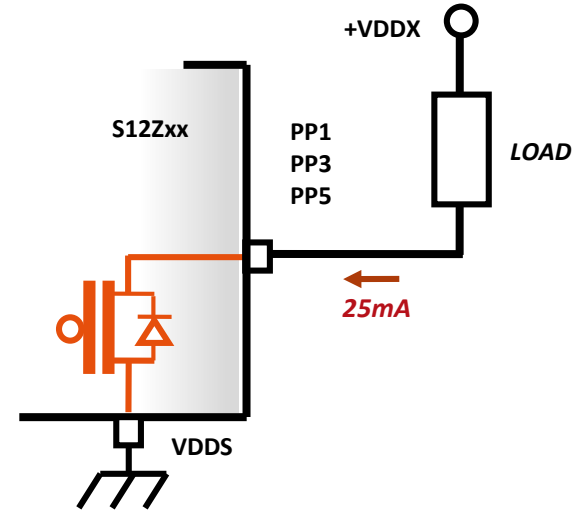


High Currents GPIOs

High-current capable high-side output with over-current interrupt

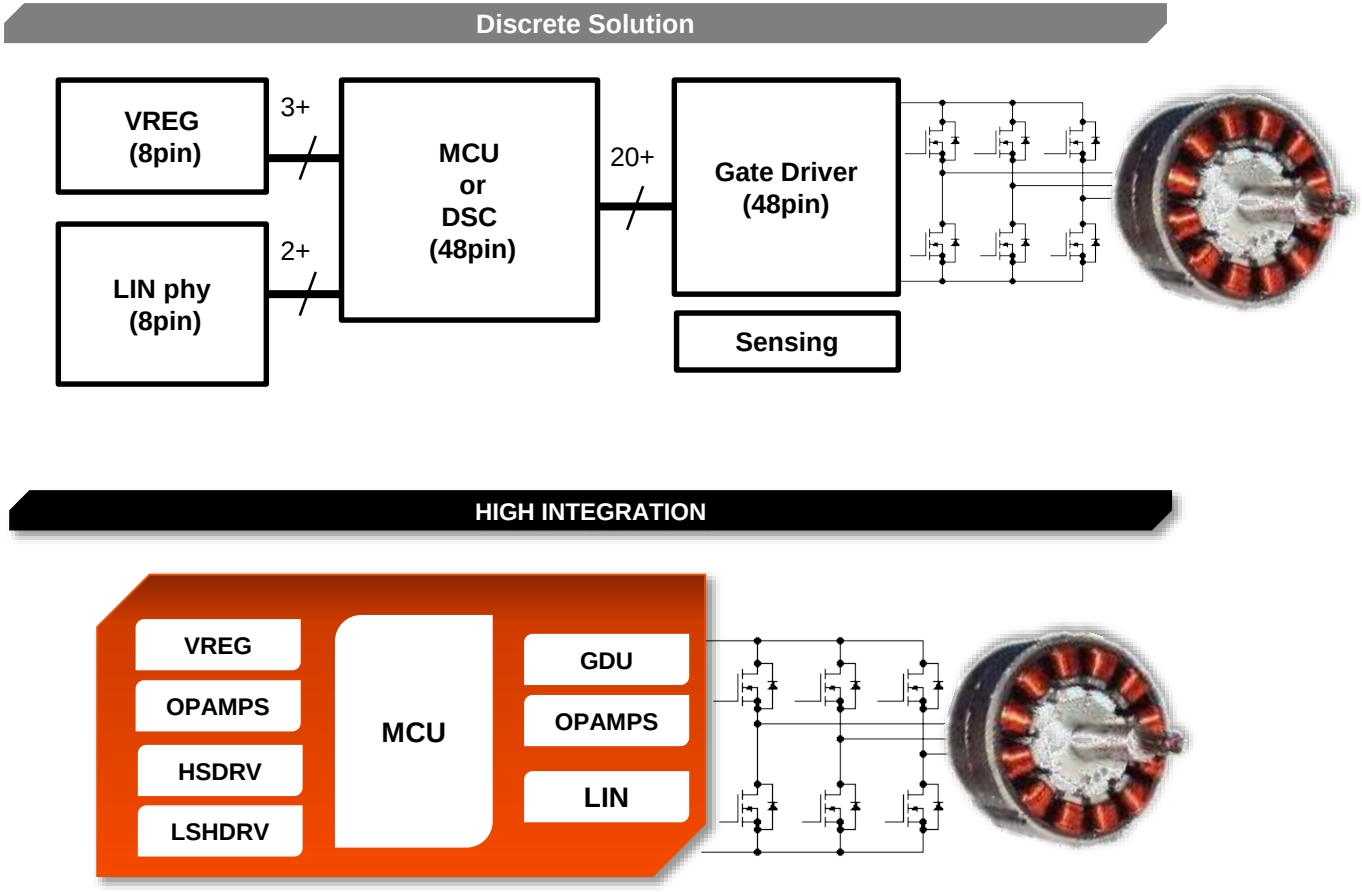


High-current capable low-side output with over-current interrupt



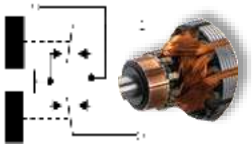
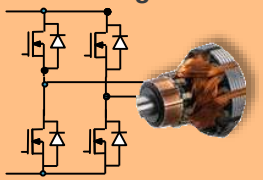
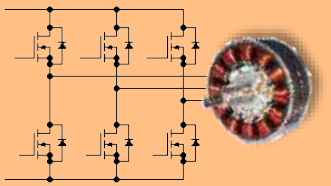
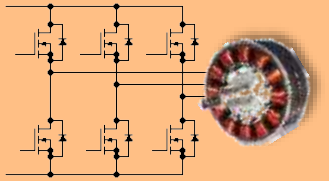
Motor Control with MagniV

S12ZVM for BLDC Motor Control



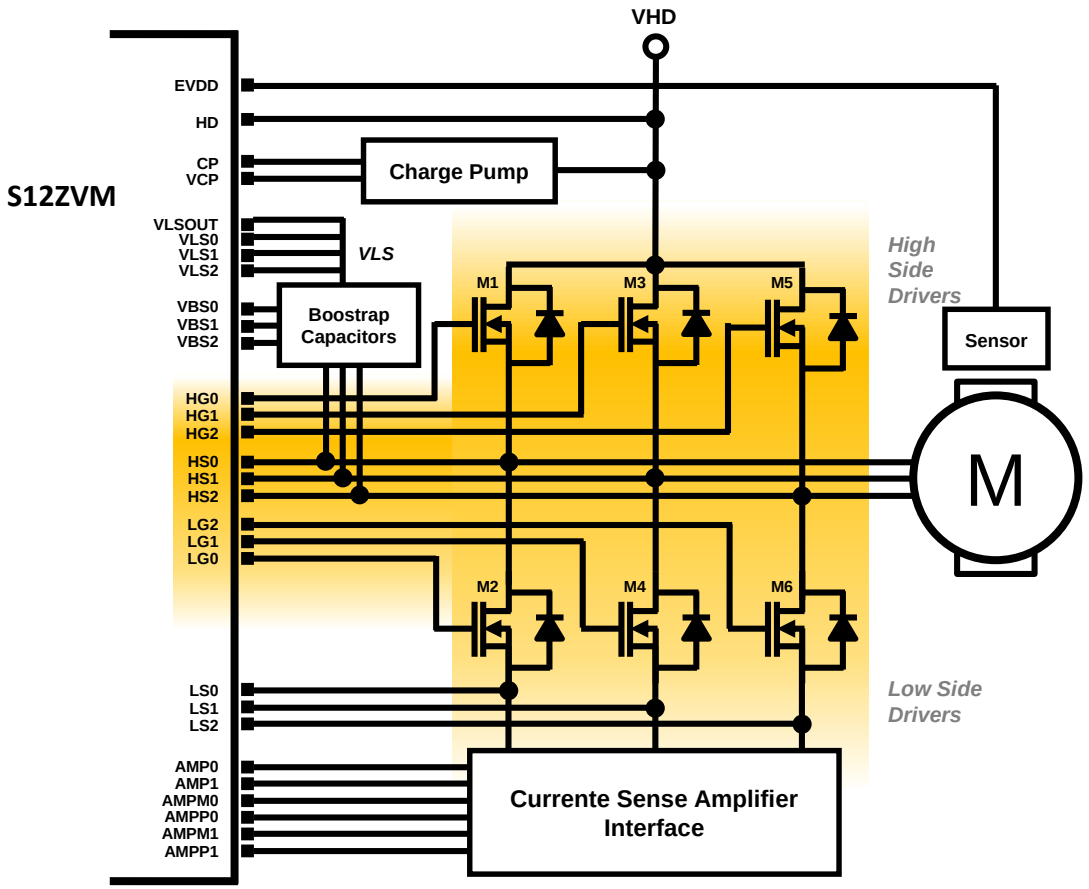
Motor categories

S12ZVM-target area

	Relay-driven DC-motors	*H-Bridge driven DC-motors*	*Brushless DC Motors (BLDC)*	*Permanent Magnet synchronous Motors (PMSM)*
Power Stage	**Relay** 	**H-Bridge** 	**3-phase** 	**3-phase** 
Mechanical construction	Permanent magnets placed on stator  Magnetic poles in rotor generated by current cunducted coil		Permanent magnets Placed on rotor  Current conducted coils in stator generate changing magnetic flux vector	
Commutation & Control Technique	Mechanical Commutation By brushes in the rotor		Electronic Commutation takes place in the stator 6-step / Block Commutation To produce trapezoidal Phase voltage	Sinusoidal / Vector control To produce Sinusoidal Phase voltage
Topology Advantage	Lowest cost	no mechanical component (reliability, electrification) No Relay noise PWM speed regulation	High Efficiency Power to weight ratio Reliability Noise	Best noise behavior High speed & precision Highest efficiency&torque Power to weight ratio

GDU – High/Low side FET Pre-Drivers

- The S12ZVM includes a GDU module, this module is a Field Effect Transistor (FET) pre-driver designed for three phase motor control applications.
- The pre-driver interface is connected directly to the external low-side and high-side power-MOSFETs. The primary function of a driver is to switch a MOSFET from off-state to on-state and vice versa, the pre-driver amplifies the control signals to required levels to drive the power MOSFET.
- To guarantee reliable operation, the low-side drivers are supplied by the VLS regulator while the high-side drivers are supplied directly by the bootstrap circuit. The gate charge that can be delivered to each external Power-MOSFETs is of 50nC and 75nC, depending of the GDU version.



GDU – High/Low side FET Pre-Drivers

HG[2:0] — High-Side Gate Pins

- The pins are the gate drives for the high-side power FETs. The drivers provide a high current with low impedance to turn on and off the high-side power FETs.

HS[2:0] — High-Side Source Pins

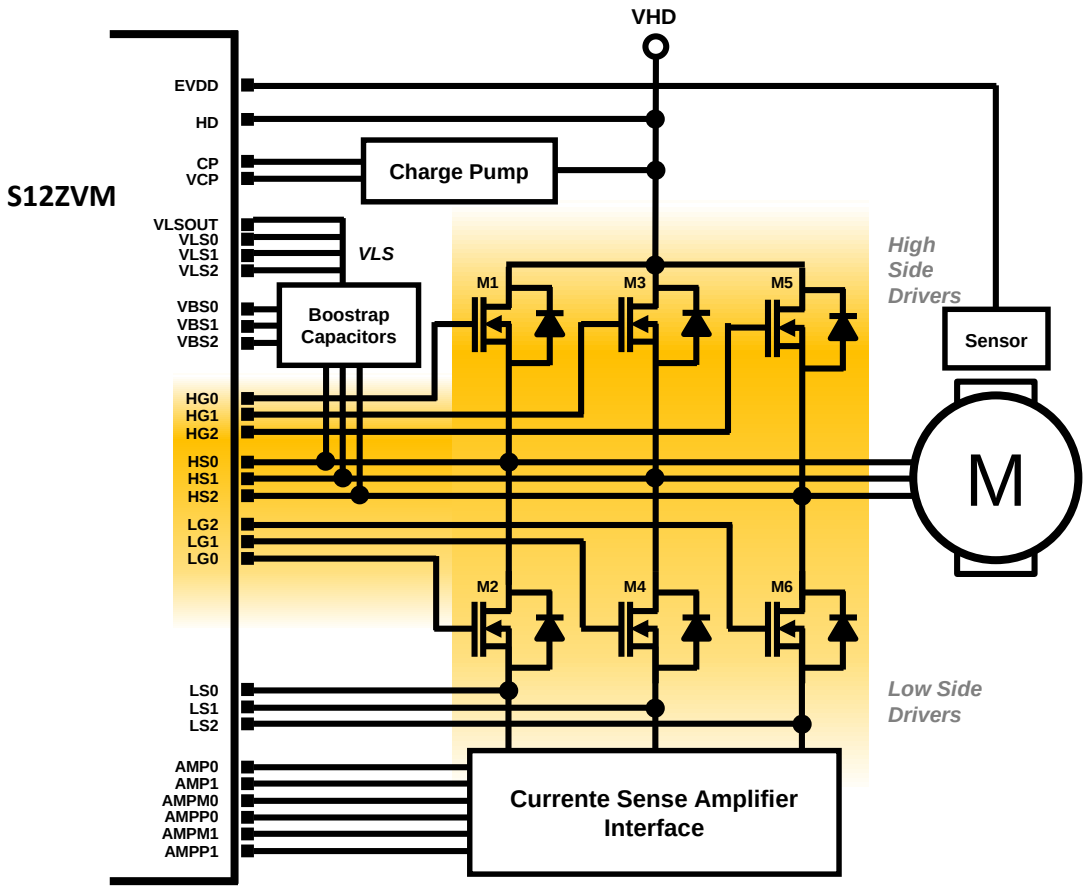
- The pins are the source connection for the high-side power FETs and the drain connection for the low-side power FETs. The low voltage end of the bootstrap capacitor is also connected to this pin.

LG[2:0] — Low-Side Gate Pins

- The pins are the gate drives for the low-side power FETs. The drivers provide a high current with low impedance to turn on and off the low-side power FETs.

LS[2:0] — Low-Side Source Pins

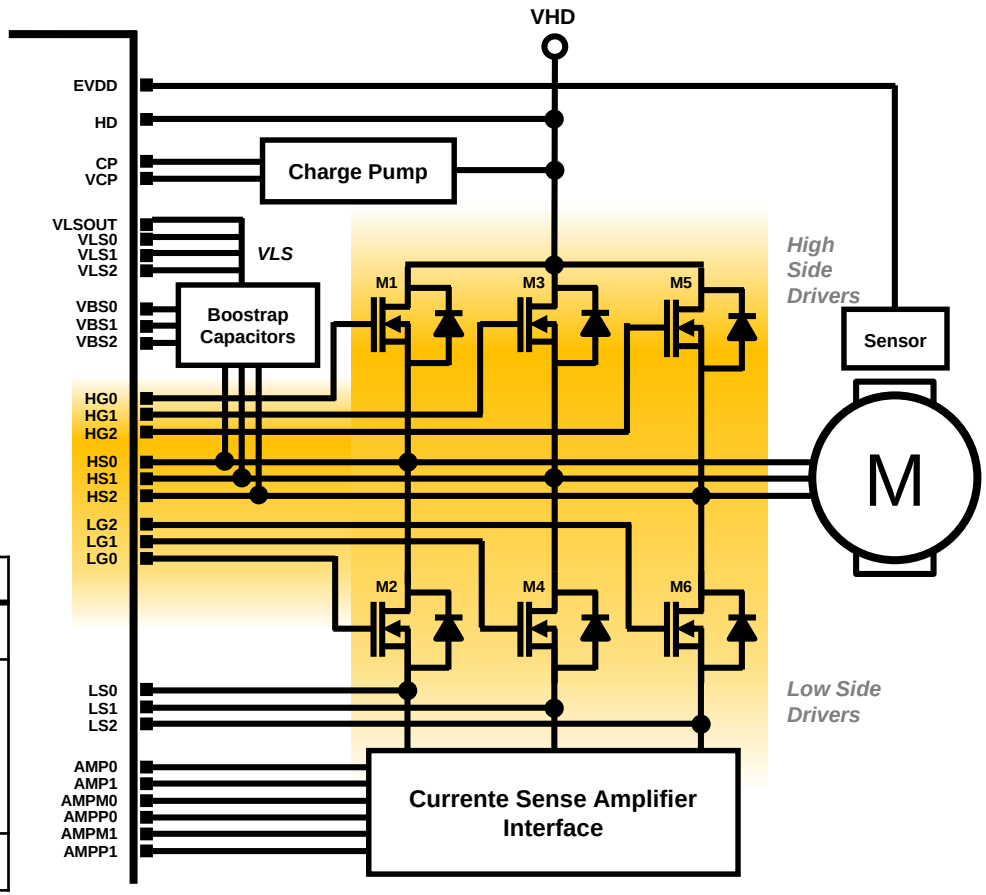
- The pins are the low-side source connections for the low-side power FETs. The pins are the power ground pins used to return the gate currents from the low-side power FETs.



GDU – High/Low side FET Pre-Drivers

- The bootstrap technique supplies the high instantaneous current needed for turning on the power devices, while the charge pump provides enough current to maintain bias voltage on the upper driver sections and MOSFETs. Since voltages on the upper bias supply pin “float” with the source terminals of the upper power switches.

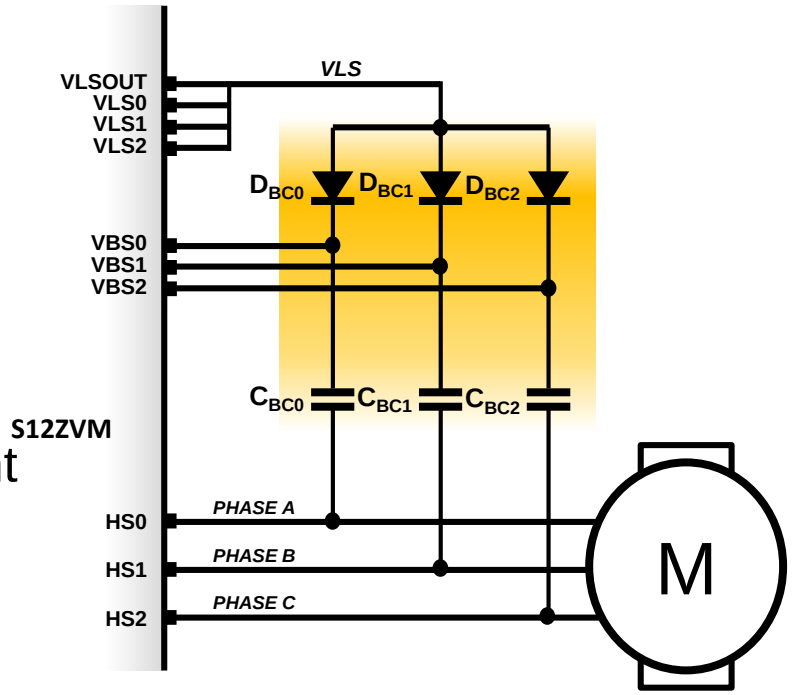
Part Number	Package Type	Manufacturer
BUK7Y3R5-40E	SOT669	NXP
AUIRF1018E AUIRF1018ES	D2PAK	IRF
AUIRF1010EZ AUIRF1010EZS	D2PAK	



GDU – Bootstrap Circuit

- The high side pre-driver must provide a sufficient gate-source voltage and sufficient charge for the gate capacitance of the external FETs. A bootstrap circuit is used to provide sufficient charge.

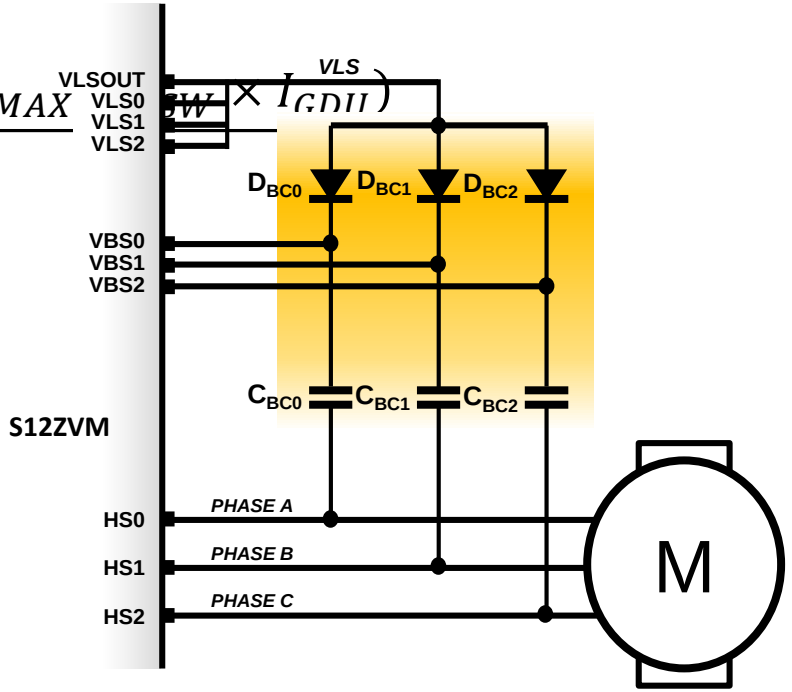
- The bootstrap circuit uses a set of external diodes and capacitors to provide a significant amount of current to turn on (Ohmic region) the top MOSFETS rapidly, the gate of each device must be driven approximately 8V more positive than the supply voltage. To achieve this an internal charge pump is used to provide the gate drive voltage.



GDU – Bootstrap Components selection.

The Bootstrap Capacitor value $C_{BS,}$ is determinated as:

$$C_{BSx} \geq \frac{Q_G + (D_{MAX} \times T_{SW} \times I_{GDU})}{\Delta V}$$



where:

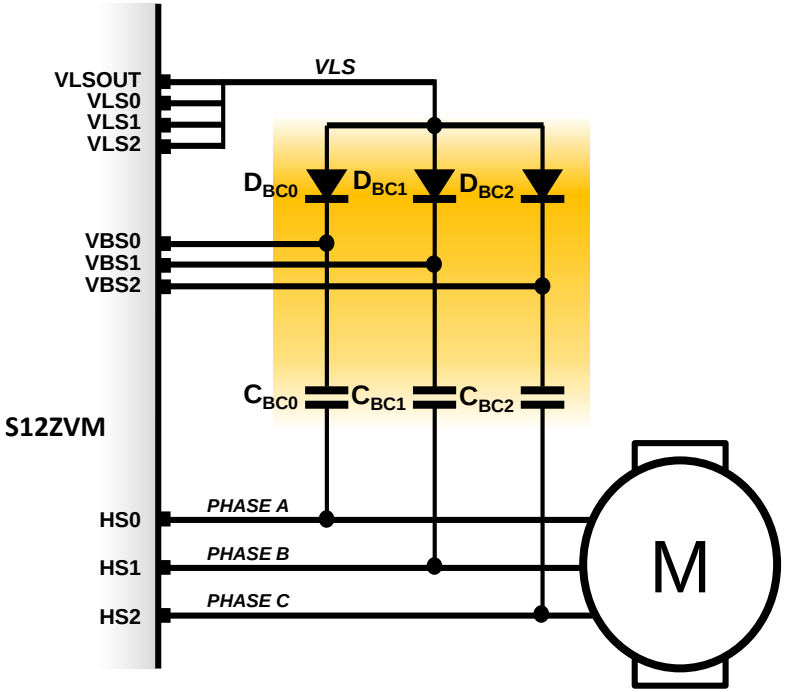
- **Q_G** - Total Gate charge of MOSFET
- **D_{MAX}** - Maximum Duty cycle
- **T_{SW}** - Switching Peri0d
- **I_{GDU}** - Current consumption of GDU
- **ΔV** - Voltage drop accepted on C_{BCX} at end of ON time

GDU – Bootstrap Components selection.

Example

Design Requirements:

- QG_MOSFET = 47nC
- TSW = 1/20 kHz = 50µs
- D_{MAX} = 90% = 0.9
- ΔV = 0.5V
- IGDU <= 600µA



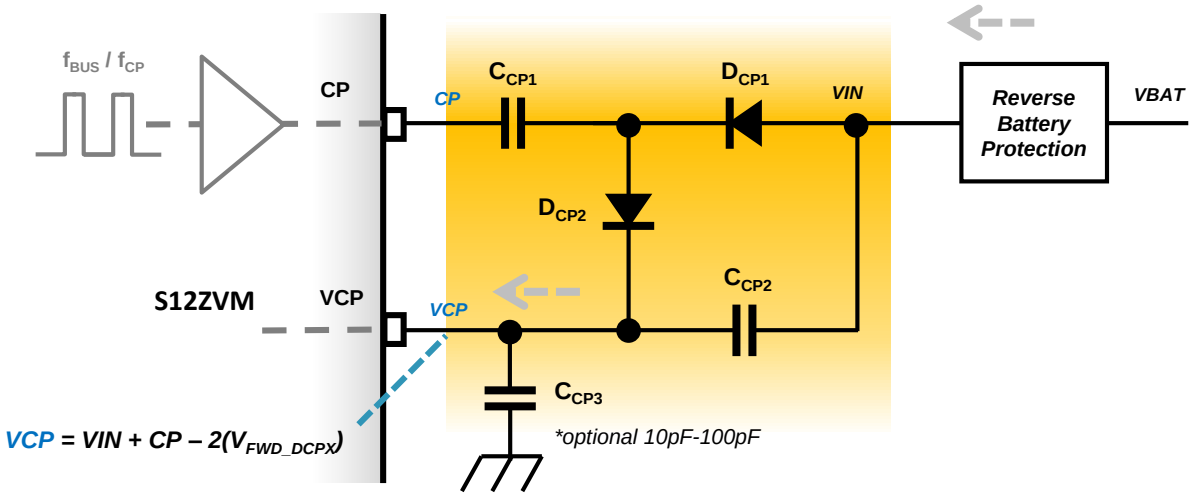
Solution

- $C_{BCx} \geq \frac{47nC+(0.9\times50\mu s\times600\mu A)}{0.5V} = 148nF$

- Considering lifetime and tolerances, an appropriate capacitor value would be 220nF. A low ESR, for example, a X7R capacitor is recommended for the bootstrap circuit and supports both the low-side driver and bootstrap recharge.

- The bootstrap diode must use a lower forward voltage drop and a switching time as soon as possible for fat recovery, such as ultra-fast.

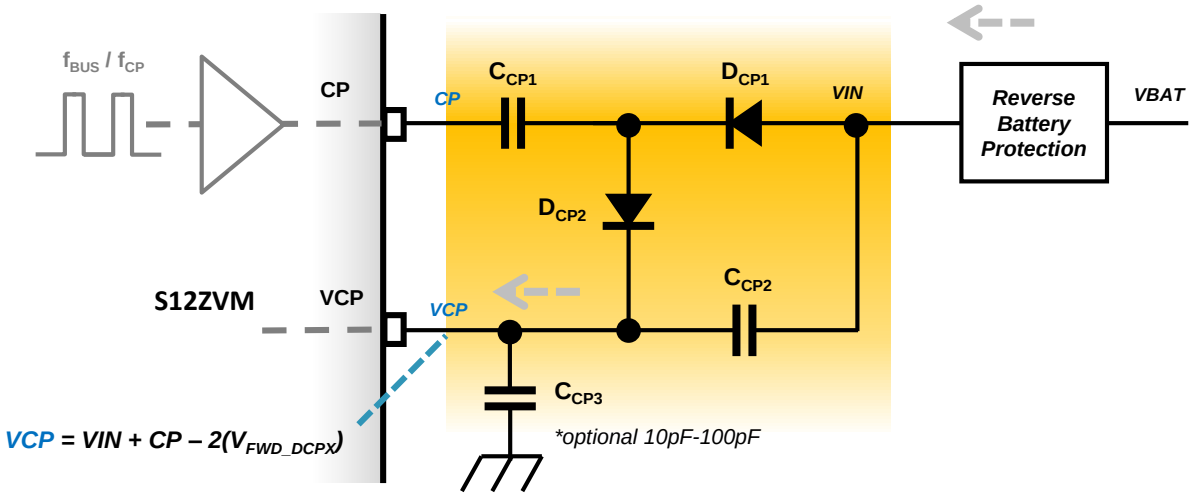
GDU – Charge Pump



A charge pump voltage is used to supply the high side FET pre-driver with enough current to maintain the gate source voltage. To generate this voltage an external charge pump is driven by the pin CP, switching between 0V and 11V. The pumped voltage is then applied to the pin VCP.

- The CP - Charge Pump In/Output Pin, is the switching node of the charge pump circuit. The supply voltage for charge pump driver is the output of the voltage regulator VLS. The output voltage of this pin switches typically between 0V and 11V. The pumped voltage is then applied to the pin VCP.
- The VCP - Charge Pump Input for High-Side Driver Supply pin is the pumped output signal which supplies the bootstrap cap and the high-side FET pre-driver supply VBS[2:0].

GDU – Charge Pump



The charge pump voltage VCP, is determinated as:

$$VCP = V_{IN} + CP - 2(Vfwd_{DCPX})$$

The charger pump capacitor value [C_{CP1}], depends of the energy required for the high side drivers, is determinated as:

$$C_{CP1} \geq \frac{\Delta Q_G \times N_{HSD}}{VCP}$$

The voltage ripple is minimum for C_{CP2} >> C_{CP1}, 10x is recommended.

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The voltage ripple is minimum for C_{CP2} >> C_{CP1}, 10x is recommended.

And the steady state of VCP is reached after 5τ (~99%); where the time constant is approximately:

$$\tau = \left(\frac{1}{fsw_{CP} \times C_{CP1}}\right)(C_{CP2} + C_{CP1})$$

where f_{SWCP} is the switching frequency configured by the GCPCD register.

Example

- Design requirements:
- $V_{IN} = 12V$
- $CP = 11V$
- $\Delta Q_G = 50nC$
- $N_{HSD} = 3\ Highside\ drivers$
- $Vfwd_{DCP} = 0.75V$

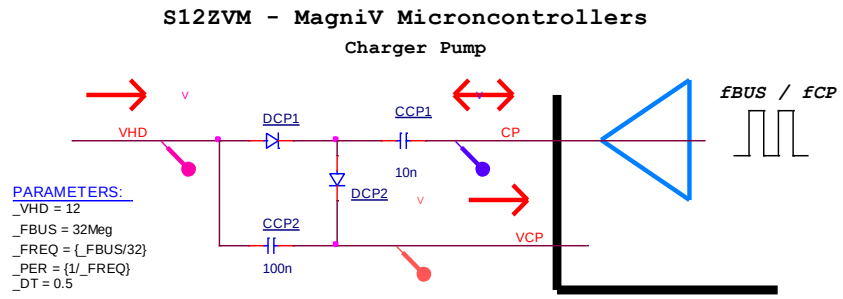
Solution

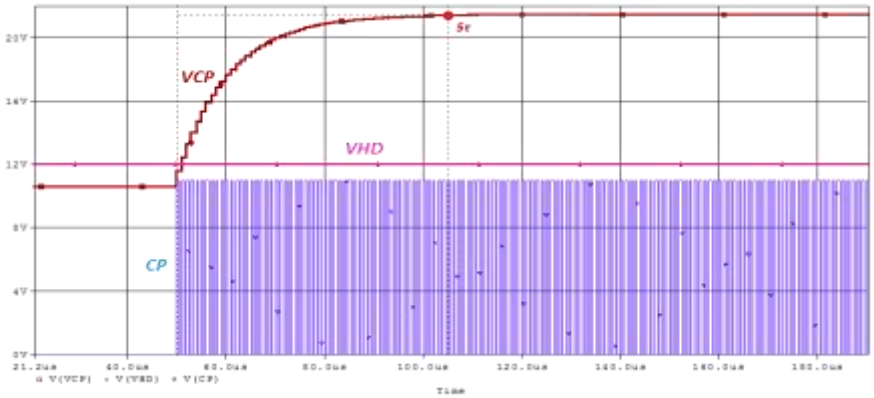
The minimum charge-pump capacitance percent is determined from EquationX.

$$C_{CP1} \geq \frac{50nC \times 3}{12V + 11V - (2 \times 0.75V)} = 7nF$$

Thus C_{CP1} = 10nF and C_{CP2} = 100nF would be the selected values.

GDU – Charge Pump





Example

- Design requirements:
- $V_{IN} = 12V$
- $CP = 11V$
- $\Delta Q_G = 50nC$
- $N_{HSD} = 3\ Highside\ drivers$
- $Vfwd_{DCP} = 0.75V$

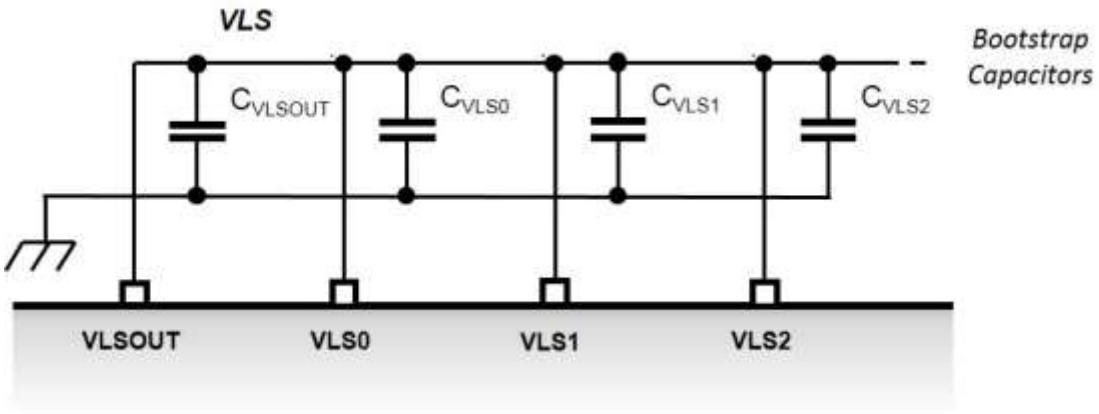
Solution

The minimum charge-pump capacitance percent is determined from EquationX.

$$C_{CP1} \geq \frac{50nC \times 3}{12V + 11V - (2 \times 0.75V)} = 7nF$$

Thus C_{CP1} = 10nF and C_{CP2} = 100nF would be the selected values.

GDU - Voltage Supply for Low-Side Pre-Drivers

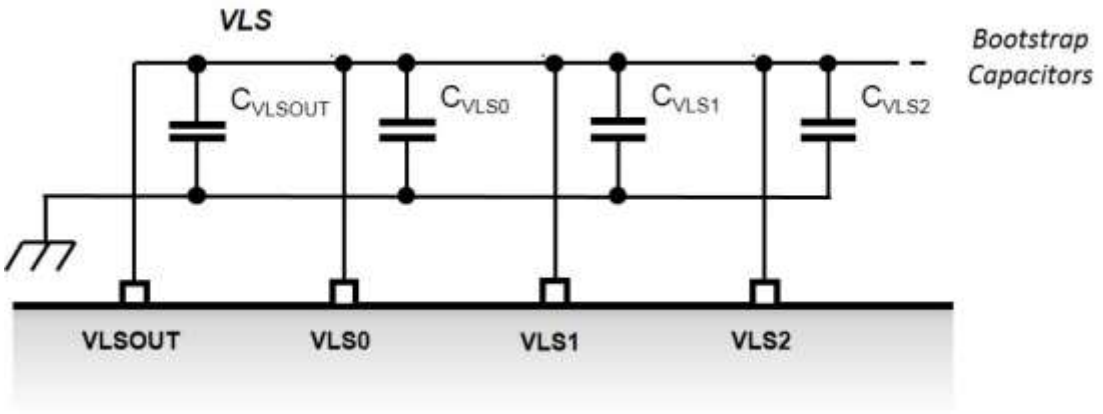


A dedicated low drop regulator is used to generate the VLS_OUT voltage from VSUP. The VLS_OUT voltage is used to supply the low side drivers and can be directly connected to the VLS inputs of each low side driver.

- The *VLS_OUT* — Voltage Regulator Output pin is the output of the integrated voltage regulator. The ouput voltage is typically VVLS=11V. The input voltage to the voltage regulator is the VSUP pin. A capacitor should be connected to this pin for stability of the voltage regulator output.

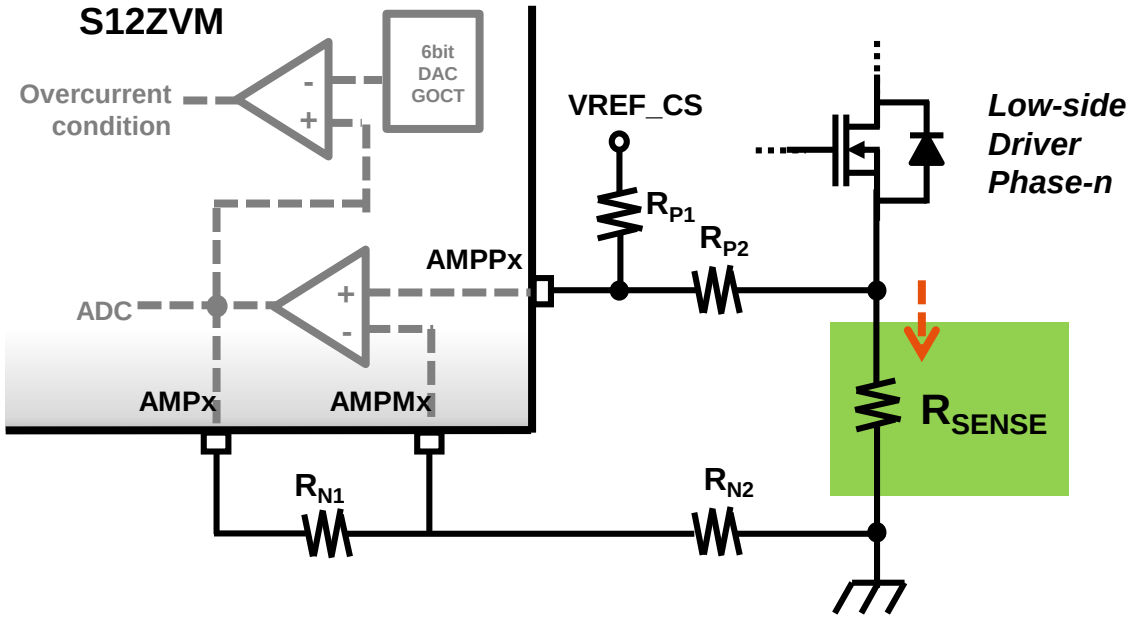
- The *VLS[2:0]* — Voltage Supply for Low-Side Pre-Drivers pins are the voltage supply pins for the three low-side FET pre-drivers. These pins should be connected to the voltage regulator output pin VLS_OUT. The output voltage on VLS_OUT pin is typically 11V. It is recommended to placed a ceramic capacitor as close as possible to each VLS pin.

GDU - Voltage Supply for Low-Side Pre-Drivers



Symbol	Characteristic	Value
C_{VLSOUT}	X7R Ceramic or Tantalum	4.7uF to 10uF
C_{VLS0}	X7R Ceramic	220 nF
C_{VLS2}	X7R Ceramic	220 nF
C_{VLS3}	X7R Ceramic	220 nF

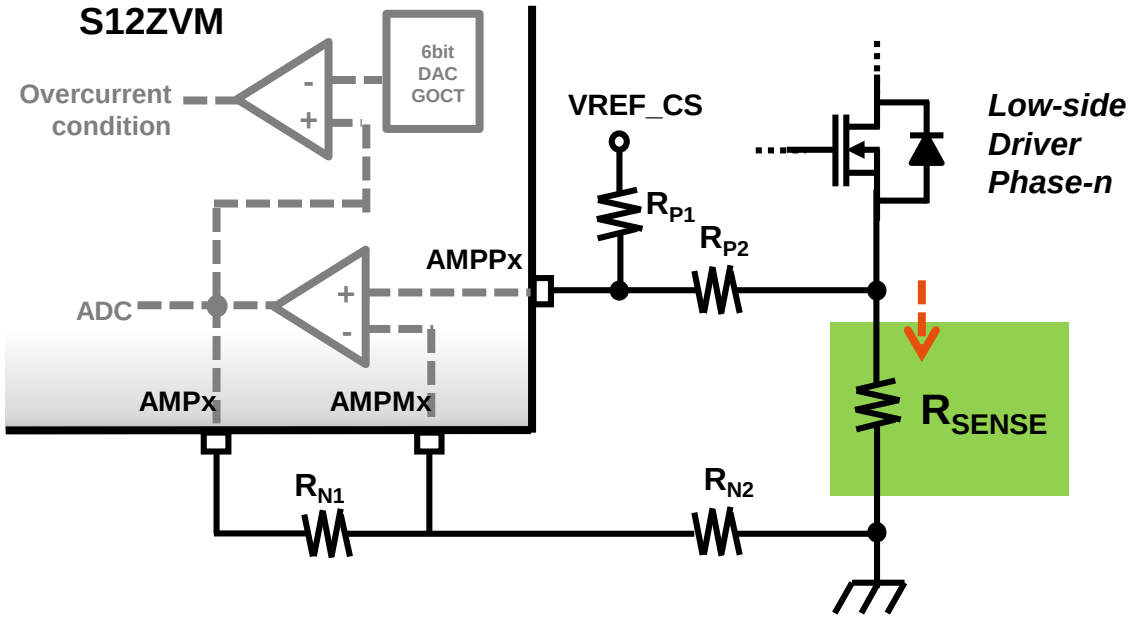
GDU - Current Sense Amplifier interface



- The current sense amplifier is integrated in the S12ZM microcontroller for low-side current measurements; the interface consists in two Op-Amps on-chip, each one linked to an independent ADC channel, for simultaneous measurement of two different currents.

- The current sense amplifier is usually connected as a differential amplifier. It senses the current flowing through the external power FET as a voltage across the current sense resistor Rsense.

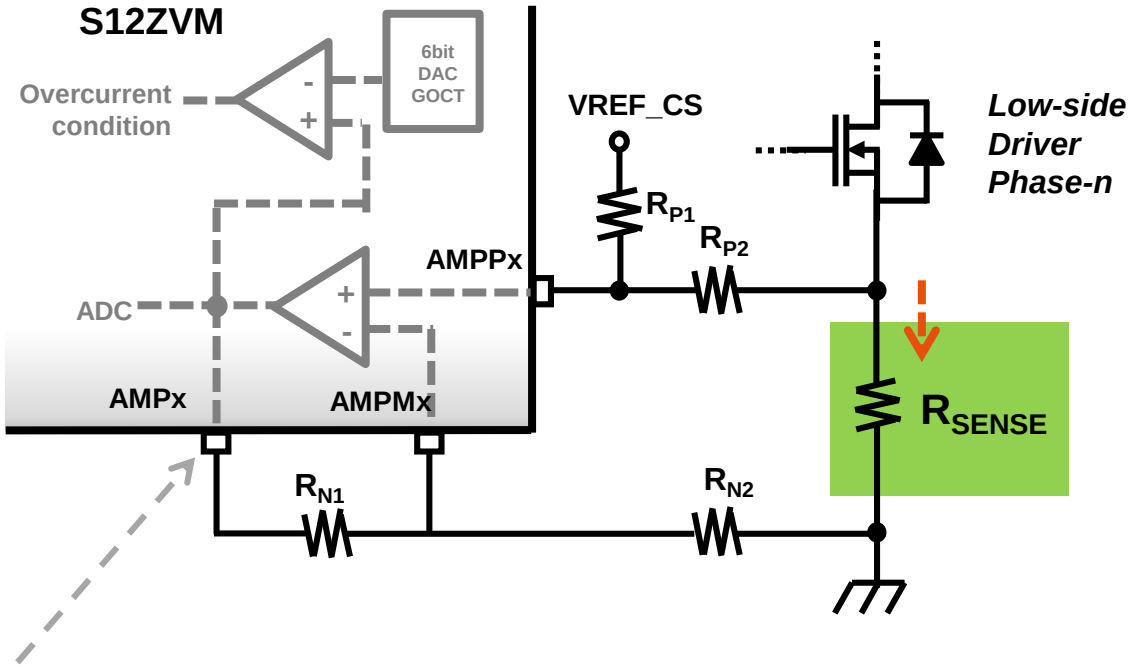
GDU - Current Sense Amplifier interface



- In order to measure both positive and negative currents, an external reference has to be used (VREF_CS).

- The voltage will be amplified with a gain selected using external resistor. The input offset voltage of the current sense amplifier can be adjusted by software. The output of the current sense amplifier is connected to the non inverting input of the overcurrent comparator.

GDU - Current Sense Amplifier interface



$$VAMP_X = \left(\frac{RN_1}{RN_2}\right)(ILoad_{MAX} \times R_{SENSE}) + V_{REF}$$

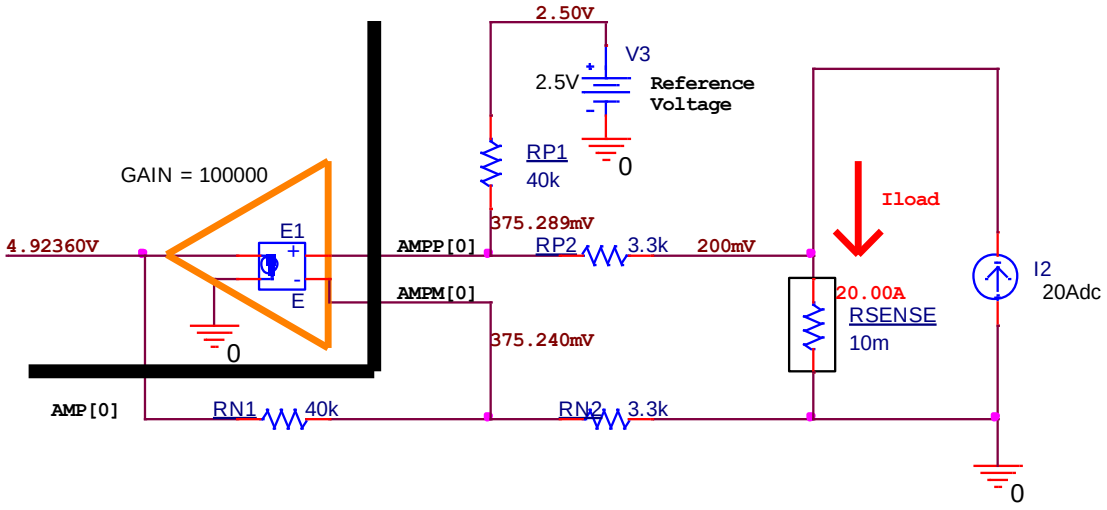
$$RP_1 = RN_1$$
$$RP_2 = RN_2$$

$$VAMP_X = A(ILoad_{MAX} \times R_{SENSE}) + V_{REF}$$

where the Gain is defined as:

$$A = Gain = \frac{RN_1}{RN_2}$$

GDU - Current Sense Amplifier interface



Example

$$ILoad_{MAX} = 20Amp$$

$$V_{REF} = 2.5V$$

$$R_{SENSE} = 10m\Omega$$

Analysis

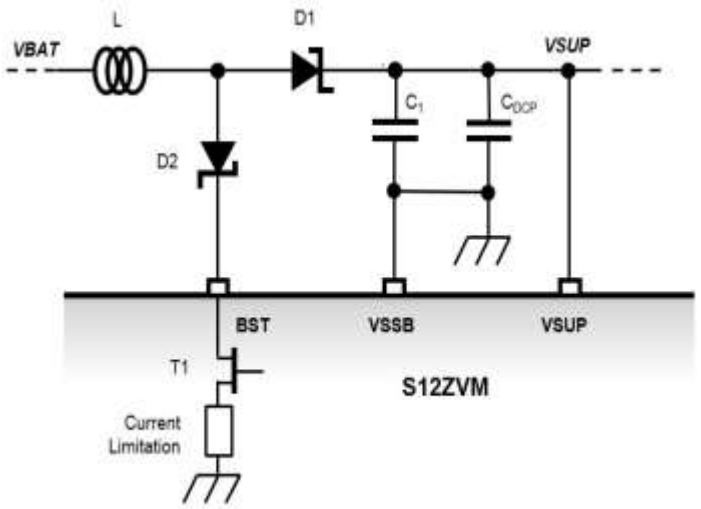
$$VAMP_X = \left(\frac{40k\Omega}{3.3k\Omega}\right)(20Amp \times 10m\Omega) + 2.5V$$

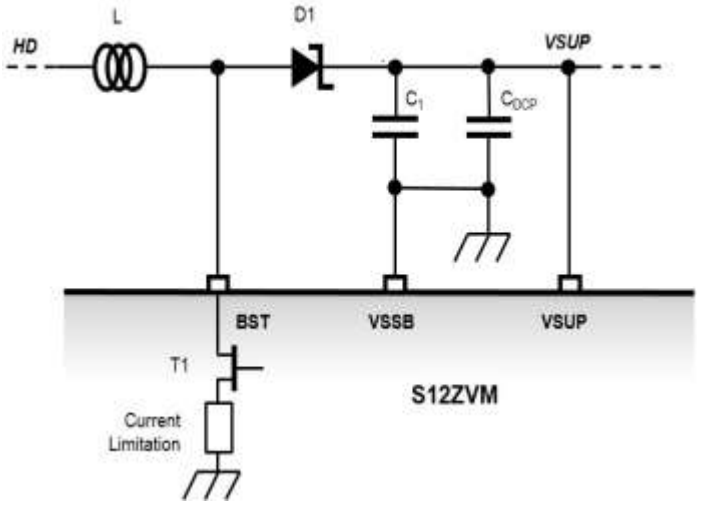
$$VAMP_X = (12.121)(200mV) + 2.5V$$

$$VAMP_X = (2.42mV) + 2.5V = 4.92V$$

GDU - Boost Converter

- The GDU module in the S12ZVM integrates a controller to implement a boost converter. This module implements a switch which is controlled by a selectable frequency of the bus. There are two possible setups for the Boost converter option.
  - Connect VBAT as input voltage to the boost converter, in this case an additional diode as VBAT reverse protection is required.
  - Connect a Reverse protected Voltage to the converter. In this option D2 is not required.
- The boost converter clock which is driving the transistor T1 is derived from the bus clock.. The boost converter also includes a circuit to limit the current through coil. This current limit can be adjusted with the bits GBCL[3:0] in the GDUBCL register.

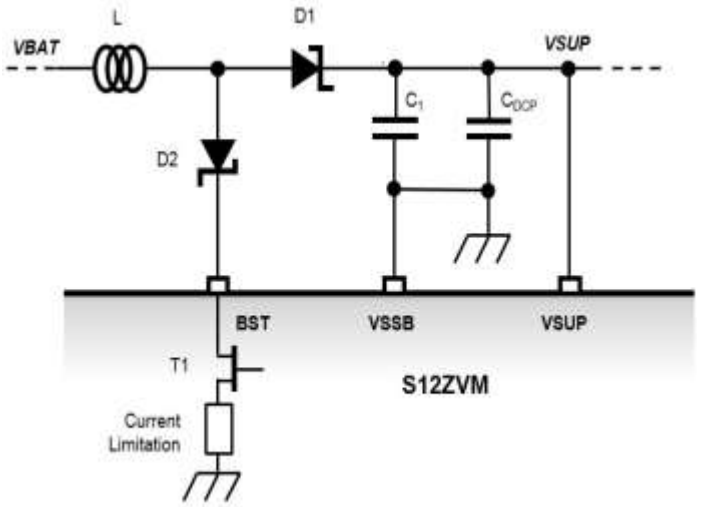




GDU - Boost Converter Components

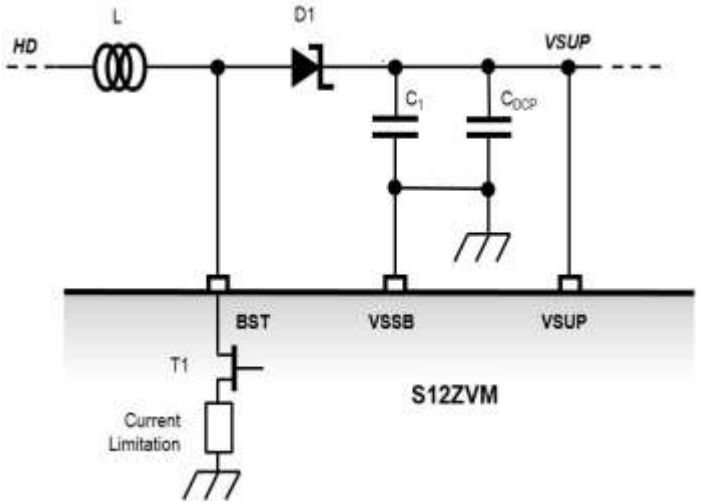
To provide relatively smooth DC voltage to the load, the output capacitor in a boost converter must absorb pulsating ripple current. For this to occur, the impedance of the capacitor at the switching frequency and the ESR of the capacitor must be low enough to keep the ripple voltage across the capacitor very small as compared to the average output voltage. The output capacitance in terms of output voltage ripple yields is defined as follows:

$$C_{OUT} = I_{OUT} \times \frac{D}{f_{SW}\,\Delta V_O}$$



The rectifier must be capable of handling the capacitor's peak input current and of dissipating the rectifier's average power—the rectifier voltage drop times the load current. The voltage breakdown of the device must be greater than the output voltage plus some margin.

The typical choice for a rectifier in applications with low output voltage is a low-capacitance diode. If the output voltage is high, a fast-recovery diode is an alternate possibility. For converters operating in CCM, a diode with a soft-recovery characteristic will minimize EMI.



GDU - Boost Converter

Example:

Design requirements:

- $V_{IN} = 3.5V$
- $V_{OUT} = 11V$
- $I_{OUT} = 70mA$
- $\%\Delta I_L = 20\%$
- $\%\Delta V_O = 0.01\%$
- $f_{SW} = 500kHz$

Solution:

First, determine the duty ratio from EquationX.

- $D = 1 - \frac{3.5V}{11V} = 0.6818$

If the switching frequency is selected at 25 kHz to be above the audio range, then the minimum inductance for continuous current is determined from EquationX.

- $L_{MIN} = \frac{11V}{70mA}\left(\frac{0.6818(1-0.6818)^2}{2(500kHz)}\right) = 10.847uH$

The minimum capacitance required to limit the output ripple voltage to 0.01 percent is determined from EquationX.

- $C_{OUT} = 70mA \times \frac{0.6818}{(500kHz)11mV} = 8.7uf$

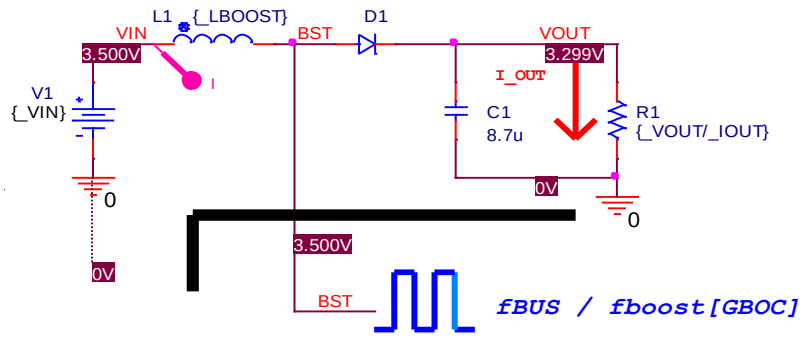
The average inductor current is determined from EquationX.

- $IL_{AVG} = 70mA \times \frac{11V}{3.5V} = 220mA$

The variation in inductor current to meet the 20 percent specification is then $\Delta I_L = 0.2(220mA) = 44mA$. The inductance is then determined from EquationX.

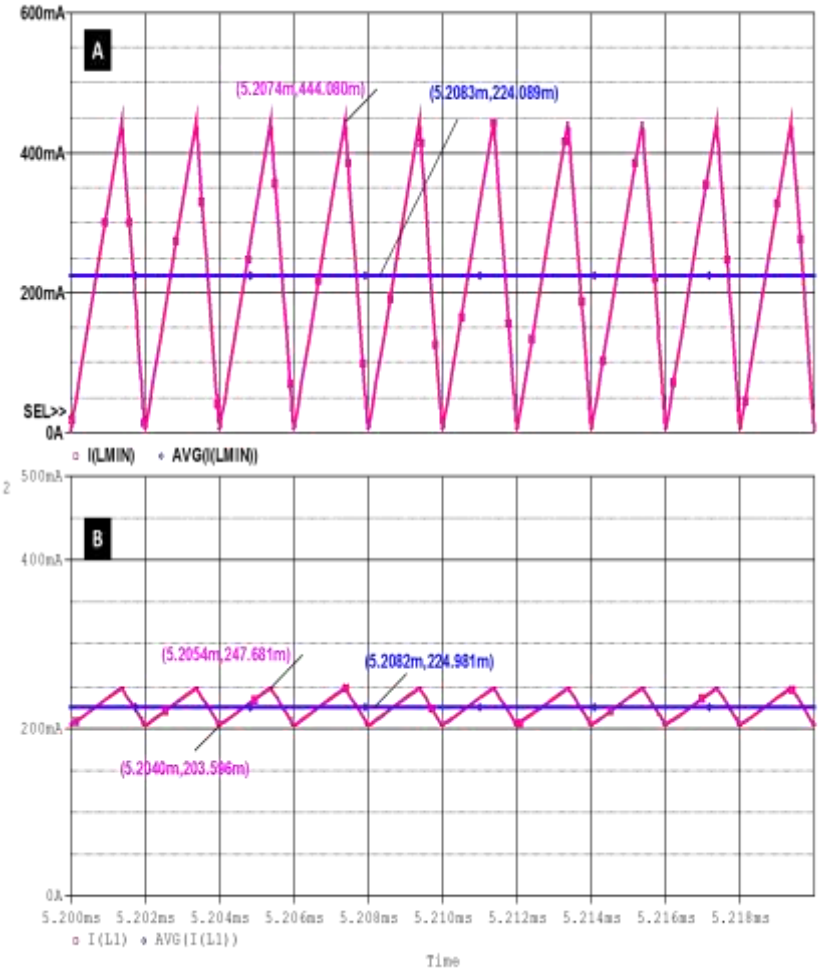
- $L = \frac{V_{IN}D}{\Delta I_L f_{SW}} = \frac{(3.5V)(0.6818)}{(44mA)(500kHz)} = 108.5uH$

GDU - Boost Converter



PARAMETERS:

_VIN = 3.5
_VOUT = 11
_IOUT = 70m
_FREQ = 500k
_PERIOD = {1/_FREQ}
_DT = 0.681818



BOOST Converter – Pspice Simulation A) Using a minimum inductor value, LMIN=10.874 uH and B) Using a a L=108.5 uH

MagniV in 24V Applications

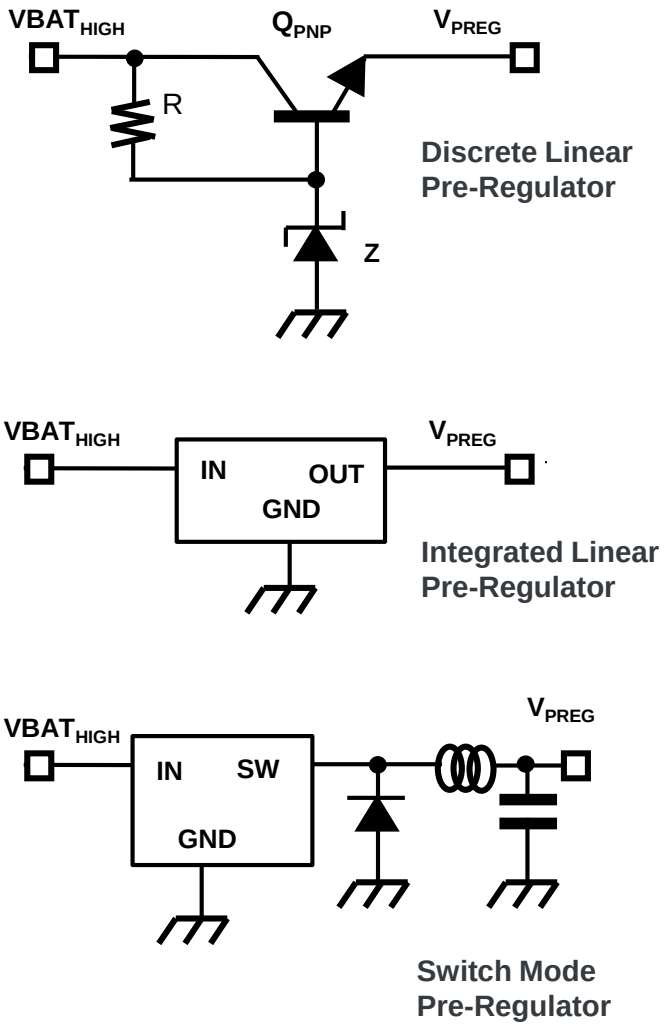
Enabling MagniV for Truck Applications

MagniV in 24V Applications

- This section introduces some considerations on how to enable MagniV family devices for 24V applications.
- In particular cases, the common PCB design can be used for both 12V and 24V applications (e.g. cars and trucks).
- The key approach is to add selected external components that extend the device's operational voltage range.

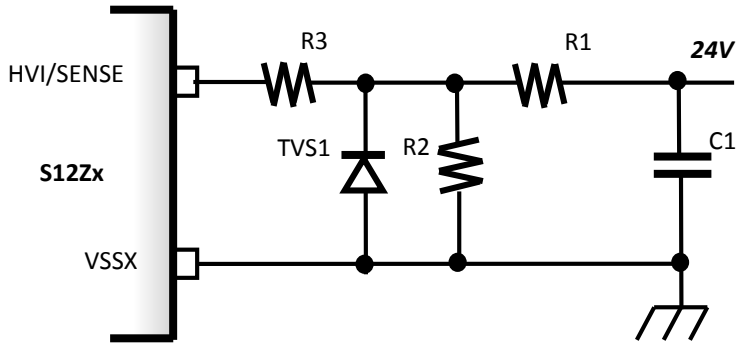
MagniV in 24V Applications

- The MagniV devices can operate from 5.5V to 18V. **The MagniV devices include a +5V regulator**, so there is no need to regulate the voltage precisely.
- Considering the minimal operating voltage of 10V (ISO16750-2 Norm), and keeping the pre-regulator and MagniV on-chip regulator power dissipation at a reasonable level, **the pre-regulator output voltage is regulated to 8V.**
- The discrete or integrated linear pre-regulator is recommended to use for power supply currents below 50mA. The higher currents are managed by a switching power supply as pre-regulator interface.



MagniV in 24V Applications

- The HVI and VSENSE pins are designed for operation in a 12V system. Additional external circuitry is needed when the requested operation as in the 24V system.
- The 24V HVI/VSENSE and 24V GND pins interface to the 24V network. The HVI/VSENSE and GND pins are connected to the MagniV device.
- The capacitor C1 suppresses the 24V network's shortest pulses. The C1 value equals units of nF. The resistor divider R1 and R2 divides the 24V HVI/VSENSE input voltage by two to fit the HVI/VSENSE pin voltage range.
- The TVS1 limits the pulses voltage. The TVS1 reverse stand-off voltage equals 20V. The resistor R3, value 10kOhm, protects the HVI/VSENSE pin.



Summary

MagniV building blocks

High-Voltage Components

- VREG for tot. supply:
  - 70mA w/o ext comp. or
  - 170mA with ext. ballast
- LIN-PHY
- CAN-PHY
- V-BAT SENSE
- V-SUP SENSE
- 1-4ch HVI (12V-input with wake-up and ADC)
- LS-drivers
- HS-drivers
- Charge Pump
- 4-6ch Gate Drive Unit for FET Qg=50-150nC

Digital Components

- MSCAN
- Sent
- SCI
- SPI
- IIC
- GPIO
- PGPIO 20mA
- NGPIO 25mA
- BDM/BDC
- Key Wakeups
- Win Wdog
- RTC
- Timer 16Bit (25-64MHz)
- PWM 8/16Bit (25-64MHz)
- Motorcontrol PWM With Fault protection
- Programmable Trigger Unit
- Sound Generator
- Segment LCD (4x40)
- Stepper Motor Driver with SSD

MCU Core and Memories

- S12- or S12Z-CPU 25/32/50MHz bus
- Flash (ECC) 8kB – 192kB
- EEPROM (ECC) 128B – 4kB
- RAM (ECC) 512B - 8kB

5V Analogue Components

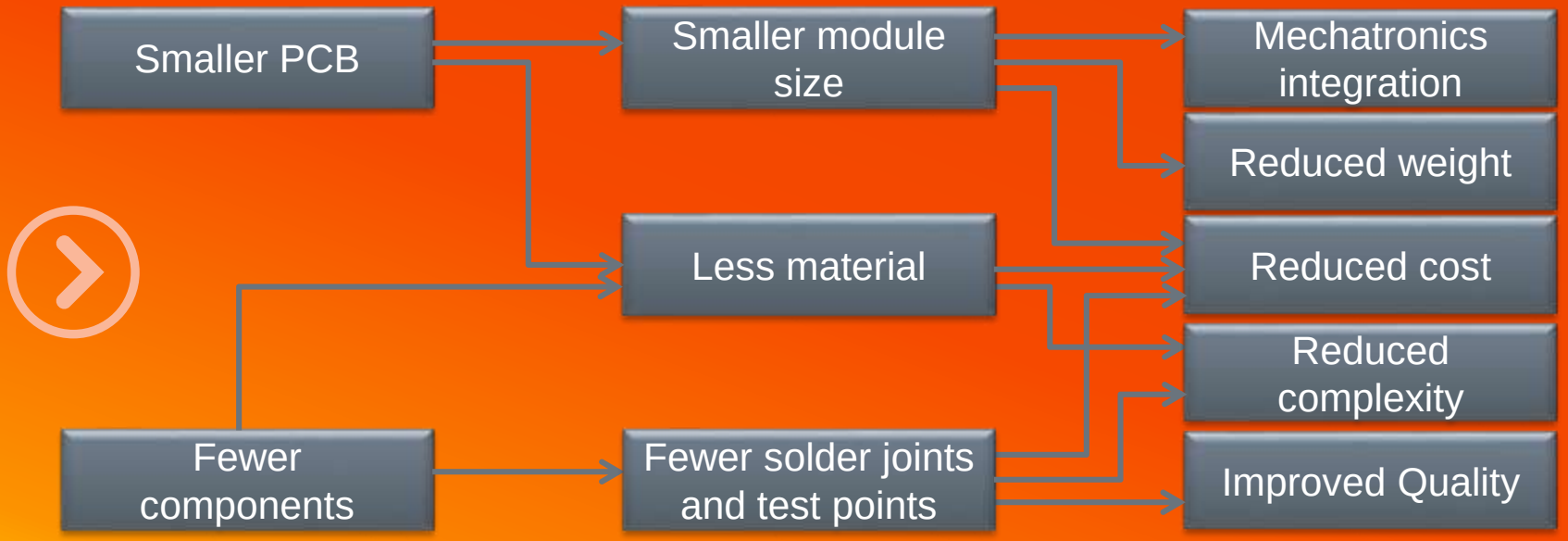
- List Based ADC 10-12Bit resolution 1-2 S/H-units Up to 16ch total
- Temp Sense
- Current Sense (2 x Op-Amp)
- PGA Up to 80x
- 2ch ACMP With 1x6-Bit-DAC
- Pierce Osc.
- 32kHz low power Osc
- RCosc. +/-1.3%
- PLL

Packaging

- LQFP: 32/48/64/100/144-pin
- LQFP-EP: 48/64-pin 

- QFN: 32-pin (5x5mm)

Manufacturing Efficiency



Additional references

- MagniV homepage
  - www.freescale.com/MagniV

- HW design guidelines documents
  - S12VR (Relay based motor control)
  - S12ZVL (LIN nodes)
  - S12ZVC (CAN nodes)
  - S12ZVH (Cluster, stepper motor, Segment display)
  - S12ZVM (Planned for Oct'15)
  - MagniV in 24V applications.

www.Freescale.com