FTF FREESCALE TECHNOLOGY FORUM 2015

Introduction to QorIQ LS1021A Tower Board and Configuration

FTF-SNT-F1282

Farshid Parandian | Sr. Applications Engineer
Richard Pern | Sr. Applications Engineer

J U N E . 2 0 1 5

freescale™

External Use

Agenda

- QorIQ LS1020/21/22A overview
- TWR-LS1021A development kit
- QorIQ LS1 CodeWarrior development tools

QorIQ TWR-LS1021A Development System
Training and Demo Goals

- The following material has been developed so you...

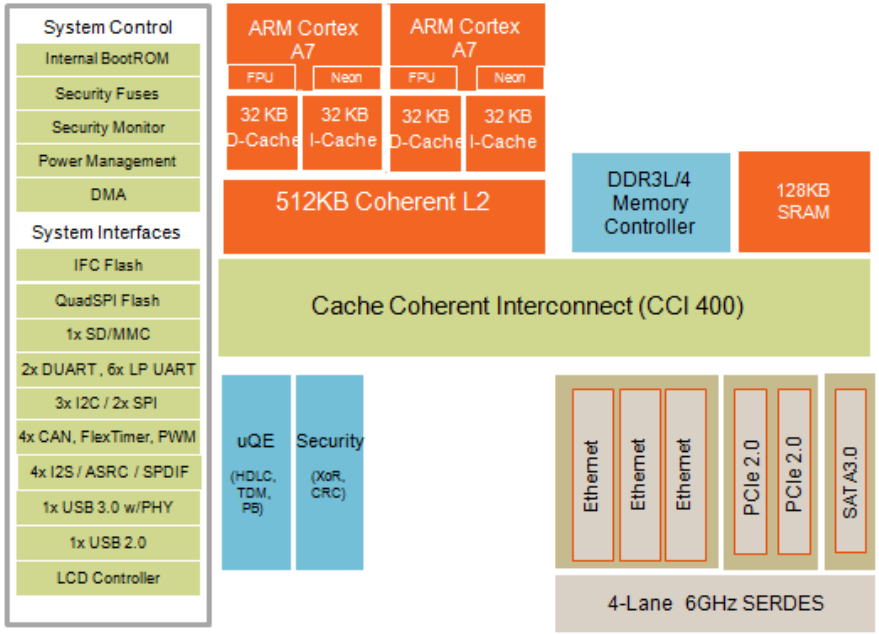
... become familiar with the QorIQ LS102x SoC family and the TWR-LS1021A development system kit

... Become familiar with basic CodeWarrior and QorIQ Configuration Suite tools

… Configure the TWR-LS1021A reference platform for your custom evaluation using the QCS tool and updating the RCW in ALTBANK

QorIQ LS1020/21/22A Block Diagrams

QorIQ LS1021A Processor



Key Architectural Features:

- ARM AMBA4 MPCore™ Virtualization
- DDR3L/4 32-bit with ECC support
- 3-port GigE with IEEE 1588
- 2x PCI Express Gen2
- Multi-protocol 4-Lane SerDes
  - PCIe-2, SATA3, SGMII
- QUICC Engine – HDLC/TDM/ProfiBUS
- EnergyStar support with fast wakeup
- **2Gbps IP forwarding**

Key System Integration Features:

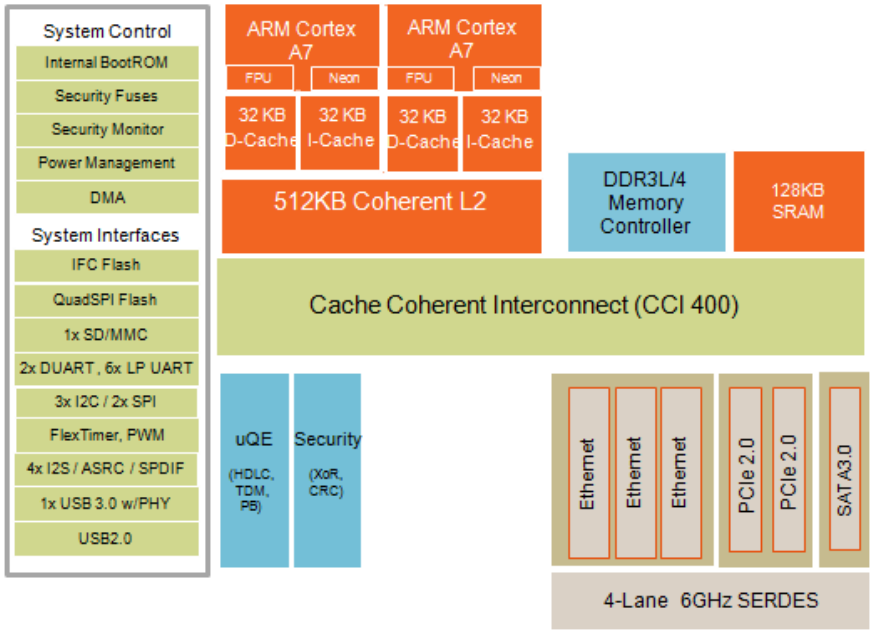
- Low-cost NAND/NOR flash systems
- Low-cost DRAM systems
- USB3 SuperSpeed
- Audio networking and motor control
- QorIQ Trust Architecture and ARM TrustZone support
- Alignment with Kinetis/Vybrid portfolio

- **Dual ARM® Cortex®-A7 cores up to 1.0 GHz**
  - ECC protected L1/L2 caches
  - DDR3L/4 up to 1.6GHz
- **Over 5,000 Coremark at under 3.7W (TDP power)**
- **Industry best Coremark / mW ratio**
- **Outstanding security and IP forwarding**
- **High integration reduces BOM costs for targeted applications:**
  - Industrial gateways
  - Industrial Automation
  - Printing & Imaging
  - HMI
  - M2M, Smart “X”

Package & Board:

Package:	525-pin, 19x19mm, 0.8mm ball pitch
Power:	~2.8W @1.0GHz Typical
Temp:	-40C (TA) to 105C (Tj)
Boards:	Tower low-cost board Freescale Linux BSPs

QorIQ LS1020A Processor



- **Dual ARM Cortex-A7 cores up to 1.0 GHz**
  - ECC protected L1/L2 caches
  - DDR3L/4 up to 1.6GHz
- **Over 5,000 Coremark at under 3.6W (TDP power)**
- **Industry best Coremark / mW ratio**
- **Secure Boot and Trust supported**
- **High integration reduces BOM costs for targeted applications:**
  - 802.11ac AP Routers
  - Line cards
  - Multi-service gateways
  - M2M, Smart "X"

Key Architectural Features:

- ARM AMBA4 MPCore™ Virtualization
- DDR3L/4 32-bit with ECC support
- 3-port GigE with IEEE 1588
- 2x PCI Express Gen2
- Multi-protocol 4-Lane SerDes
  - PCIe-2, SATA3, SGMII
- QUICC Engine – HDLC/TDM
- EnergyStar support with fast wakeup
- **2Gbps IP /1Gbps IPSec forwarding**

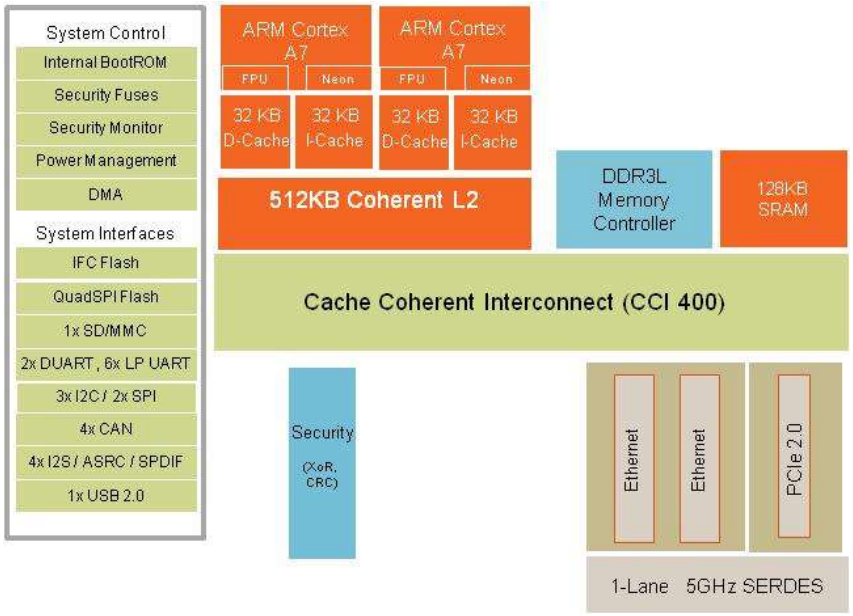
Key System Integration Features:

- Low-cost NAND/NOR flash systems
- Low-cost DRAM systems
- USB3.0 Super Speed (5GT/s)
- SATA III (6GT/s)
- Audio networking
- QorIQ Trust Architecture and ARM TrustZone support
- Alignment with Kinetis/Vybrid portfolio

Package & Board:

Package:	525-pin, 19x19mm, 0.8mm ball pitch
Power:	~2.6W @1.0GHz Typical
Temp:	-40C (TA) to 105C (Tj)
Boards:	Tower low-cost board Freescale Linux BSPs

QorIQ LS1022A Processor



Key Architectural Features:

- ARM AMBA4 MPCore™ Virtualization
- DDR3L 16-bit with ECC support
- 2-port GigE with IEEE 1588
- 1x PCI Express Gen2
- Advanced Security engine
- 4x CAN ports for industrial applications
- EnergyStar support with fast wakeup
- **2Gbps IP forwarding**

Key System Integration Features:

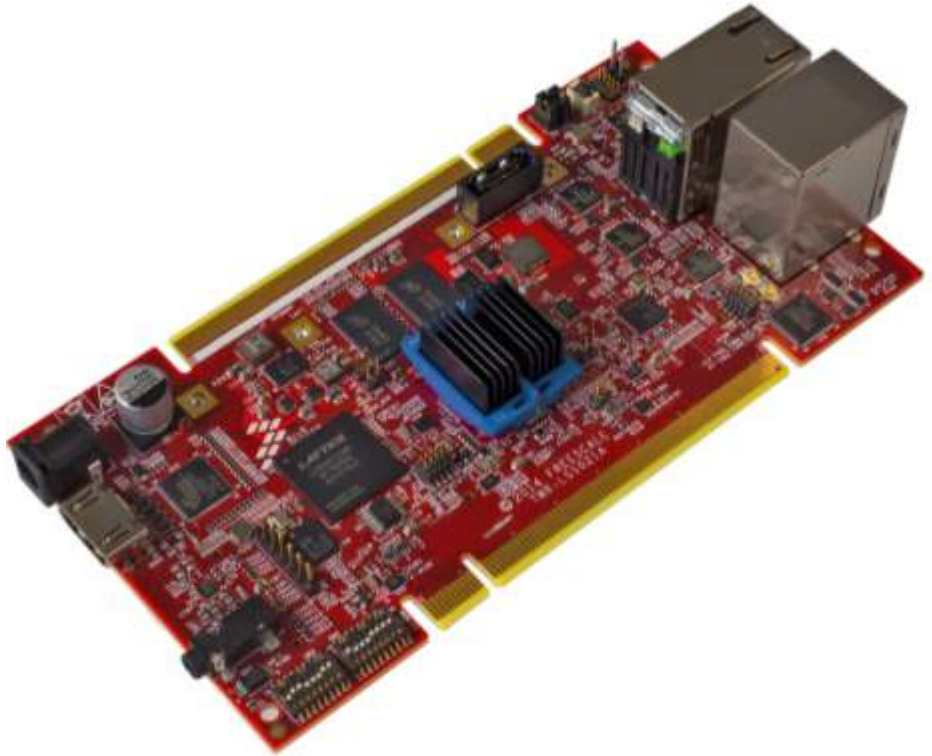
- Low-cost NAND/NOR flash systems
- Low-cost DRAM systems
- USB2.0
- QorIQ Trust Architecture and ARM TrustZone support
- Alignment with Kinetis/Vybrid portfolio

- **Dual ARM Cortex-A7 cores up to 600 MHz**
  - **Coherent 512KB L2 cache**
  - **DDR3L up to 1GHz**
- **Over 3,000 Coremarks at under 3W (TDP power)**
- **Outstanding Coremark / mW ratio: 1.1 Coremarks / mW**
- **Secure Boot and Trust supported**
- **Excellent IP forwarding**
- **Lowest power-to-performance ratio in class, ideal** for targeted applications:
  - Environmental control
  - Industrial controllers
  - M2M, Smart “X”

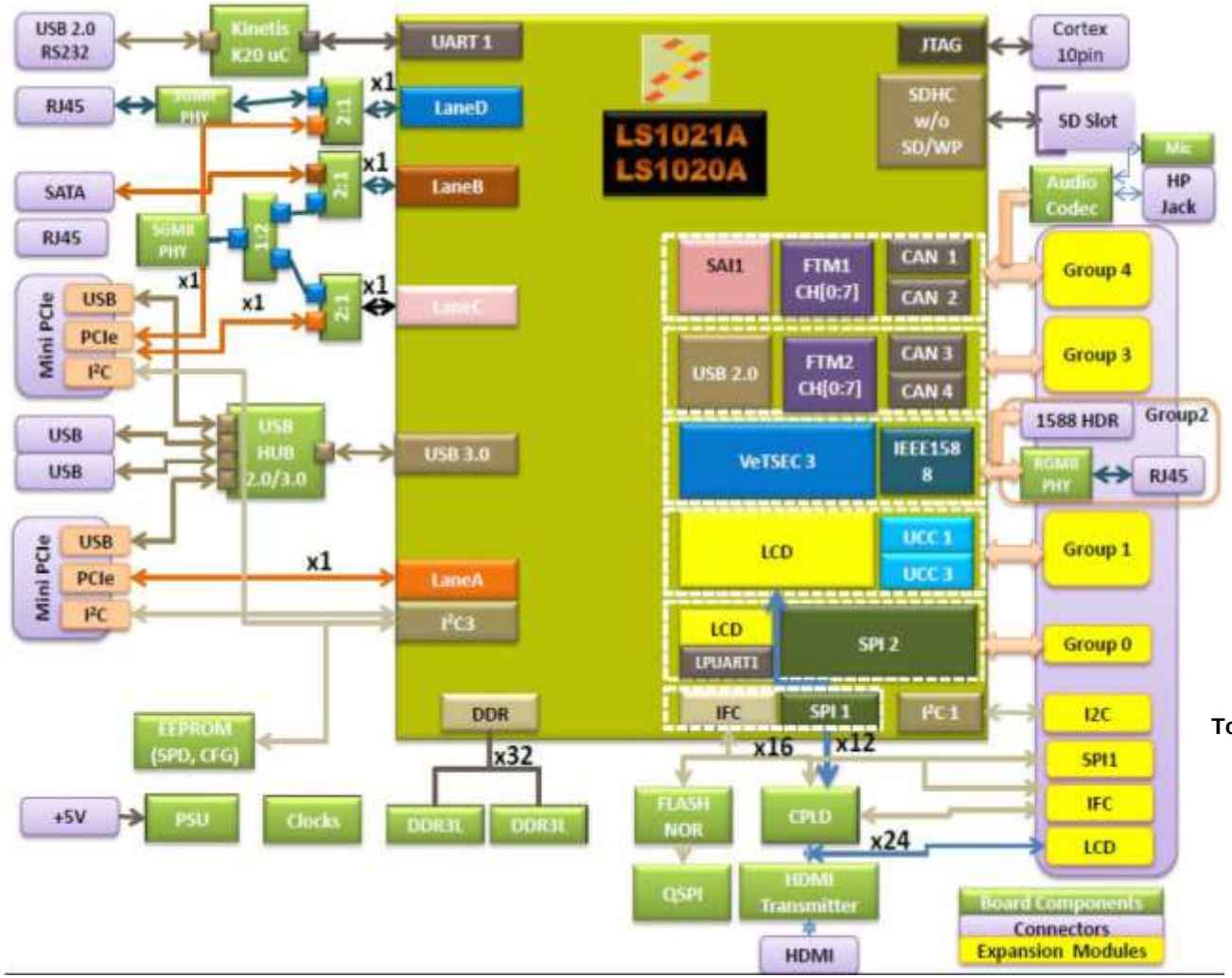
Package & Board:

Package:	525-pin, 19x19mm, 0.8mm ball pitch
Power:	~2W @ 600MHz Typical
Temp:	-40C (TA) to 105C (Tj)
Boards:	Tower low-cost board Freescale Linux BSPs

Introducing the TWR-LS1021A Development Kit



TWR-LS1021A: Block Diagram



Memory

- DDR3L 1GB
- Parallel NOR Flash 128MB
  or
  QuadSPI NOR Flash 16MB

Connections

- Up to 3 x RJ45 GigE
- 1 x SATA 3.0
- 2 x USB 3.0
- 2 x mini PCIe 2.0 (x1 + x1) or (x1 + x2)
- Display via HDMI or TWR-LCD or TWR-LCD-RGB
- Audio OUT via HDMI or Jack plug or TWR_EVEL
- Console port/JTAG via USB 2.0

Tower Boards supported via TWR-EVEL

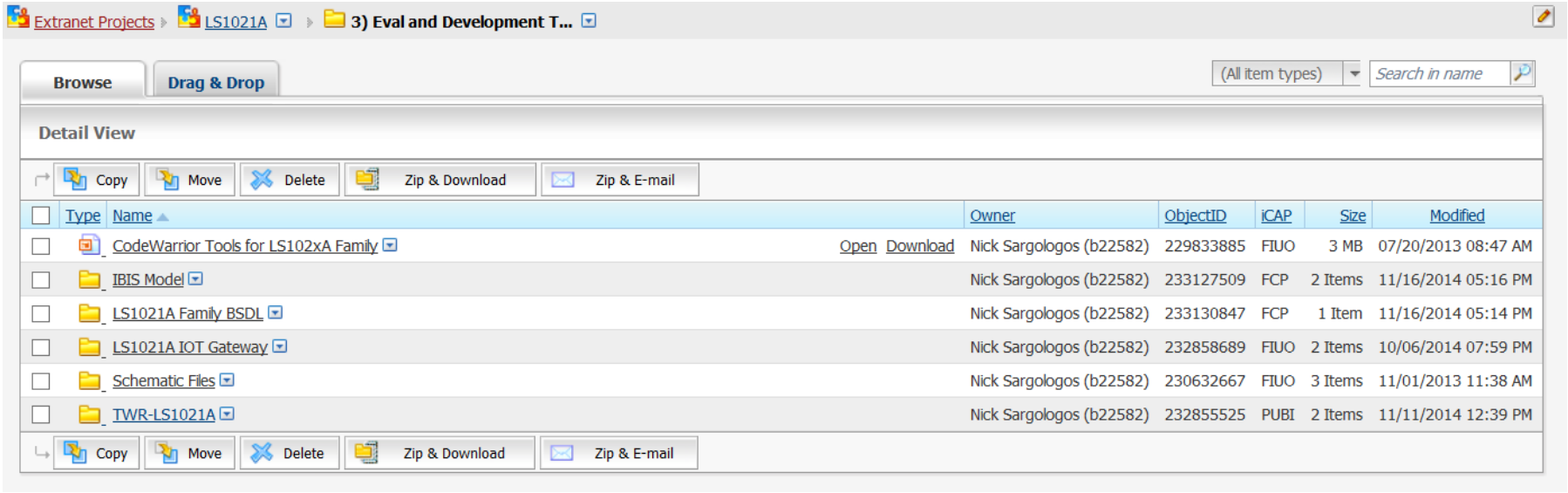
- TWR-IND-IO
  2 x CAN, RS485, RS232
  up to 2 boards supported
- TWR-LCD
- TWR-LCD-RGB
- TWR-ETHERCAT-SLV

TWR - Expansion Modules

TWR Module	Num	CAN				UCC		LPUART-1	SPI-2	I2C-3	GPIO	IRQ	FTM-1	USB-2.0	LCD	IFC
		1	2	3	4	1	3									
TWR-IND-IO	1st			•	•	•		•								
	2nd	•	•				•									
TWR-SER2	1													•		
TWR-EtherCAT-SLV	1								•	•	5	1				
TWR-MC-LV3PH	1								•	•	3	2	•			
TWR-LCD	1								•							•
TWR-LCD-RGB	1									•	2				•	

Full Documentation Available

- Full Tower board documentation available on the customer extranet, available under NDA: QorIQ LS Series - LS1021A/20A/22A



TWR-LS1021A Development Kit Setup

TWR-LS1021A: What's in the Box?

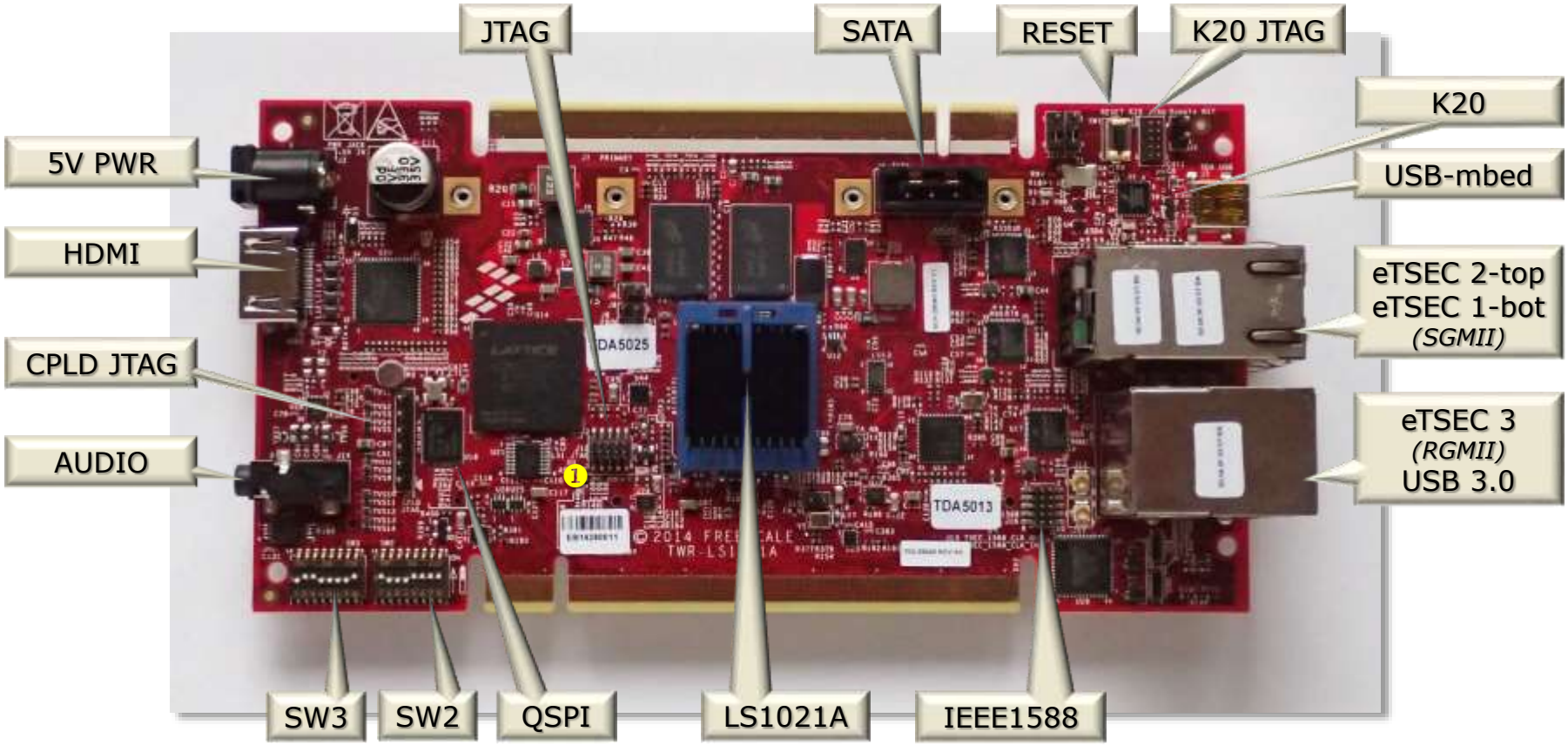
1. TWR-LS1021A kit
2. PSU + power cable
3. USB cable
4. Getting Started manual
5. SD card (Boot image)
6. USB stick with tech collateral
7. Warranty card


Freescale Semiconductor
Getting Started

TWR-LS1021A Getting Started

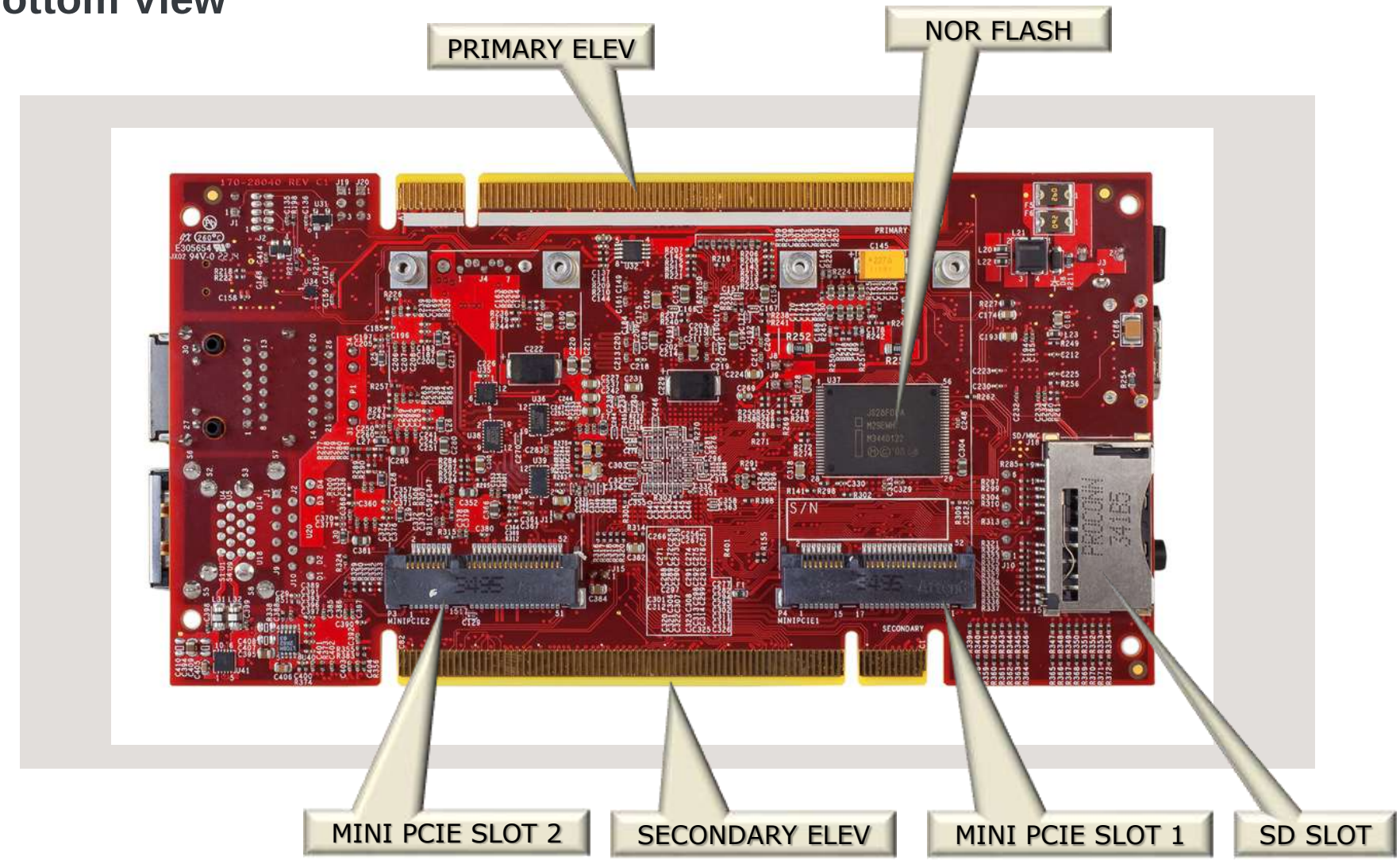
1 Introduction

TWR-LS1021A: Top View



See: *TWR-LS1021A QorIQ Tower System Reference Manual* - TWR-LS1021ARM - Rev. 0 - 09/2014

TWR-LS1021A
Bottom View



TWR-LS1021A Kit: H/W Config (Rev X3/X4 and Later)

SW 3 *(default)*

```
1 2 3 4 5 6 7 8
. o o . . . . o [ON=1]
o . . o o o o . [OFF=0]
```

```
SW3[1]   No 96MHz SYSCLK
SW3[2]   TEST_SEL = JTAG mode
SW3[3:4] CLKGEN_FS[0:1] = 100 MHz

SW3[5]   BANK_SEL = bank0
SW3[6]   MUX_SEL (see board RM)
SW3[7:8] CPU Personality : LS1021A
```

SW 2 *(default)*

```
1 2 3 4 5 6 7 8
o . . . o o o o [ON=1]
. o o o . . . . [OFF=0]
```

```
SW2[1]   NOR RCW enabled
SW2[2]   Hardcoded RCW disabled
SW2[3]   SDHC RCW disabled
SW2[4]   QSPI RCW disabled
SW2[5]   IFC enabled/QSPI disabled
SW2[6]   LVDD/L1VDD = 2.5V
SW2[7]   IFC_CS1 enabled/SPI1_PCS0 disabled
SW2[8]   ON  = USB serial console only
         OFF = USB serial console + MBED (JTAG)
```

J20

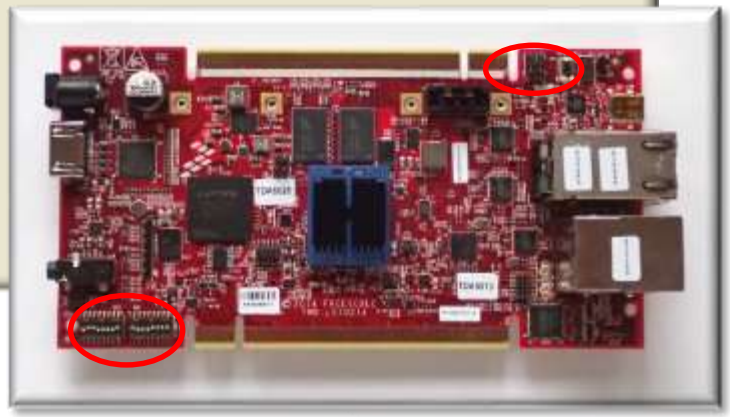
```
1 o
2 o
  |
3 o
```

J19

```
1 o
2 o
  |
3 o
```

(All other jumpers left open)

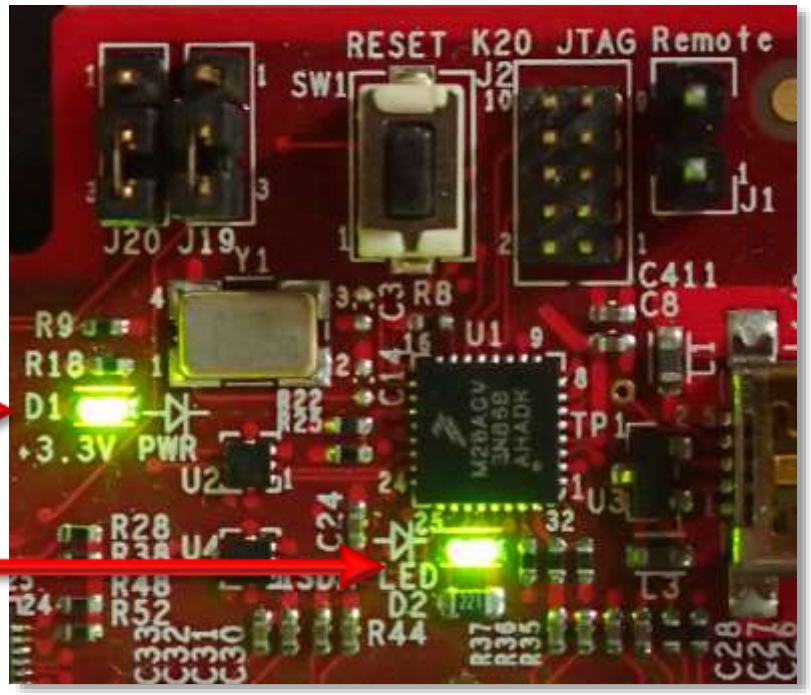
See : TWR-LS1021AGS Rev. B 08/2014 - Section 2



Initial TWR-LS1021A Development Kit Checkout

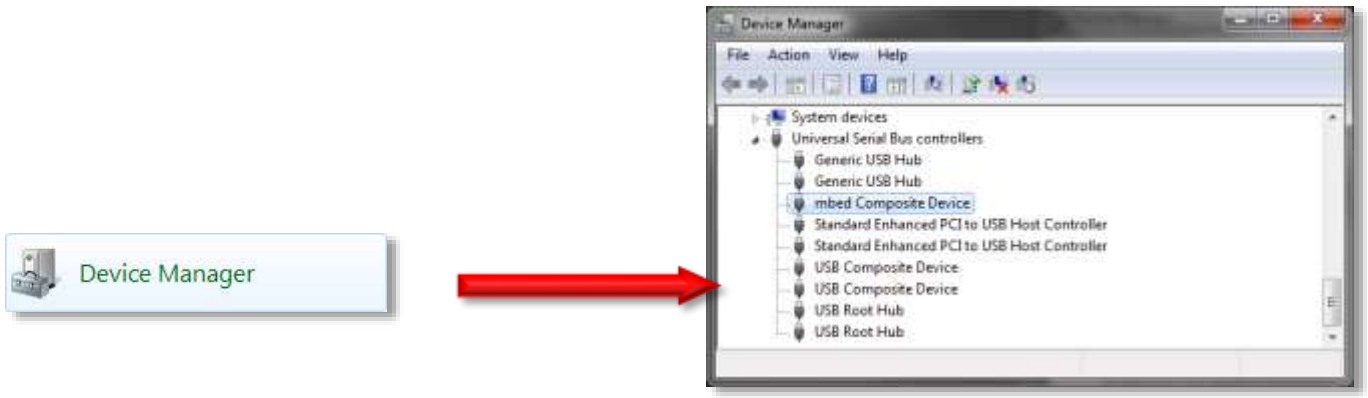
- Verify the default switch settings on TWR-LS1021A
- Connect the AC adapter to mains
- Plug in the 5V supply
- Connect the mini-USB port to the PC

- Check the LEDs:
- LED D1 = ON
  - 3.3V power is UP
- LED D2 = ON
  - MBED driver loaded



Initial TWR-LS1021A Development Kit Checkout (con't)

- Wait for Windows Device Manager to recognize and list an mbed Composite Device ... be patient

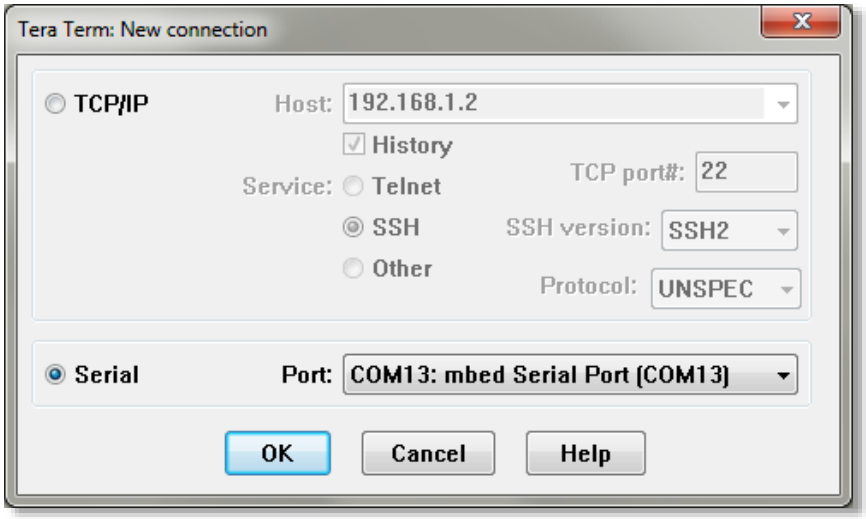


- Background info on how to re-install MBED firmware:
  see training section CMSIS-DAP Debug Support – Reinstallation

*CMSIS-DAP Cortex Microcontroller Software Interface Standard – Debug Access Port

Initial TWR-LS1021A Development Kit Checkout (con't)

- Open a TeraTerm Pro connection (115200-8-n-1) to COMx: mbed Serial Port (COMx)



- Hit the board reset button
- Check for u-boot startup in the serial console
- Interrupt the countdown by hitting any key

QorIQ LS1 Tools

CodeWarrior ARMv7 and JTAG Probe Options

QorIQ LS1 Software and Tools Enablement

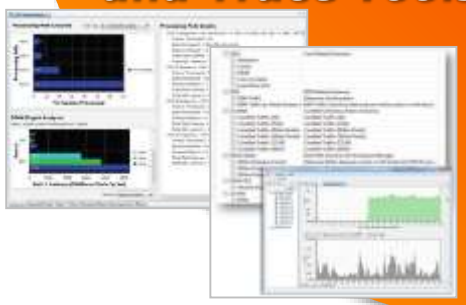
CodeWarrior Development Studio

Board Bring-up and SW Development Tools

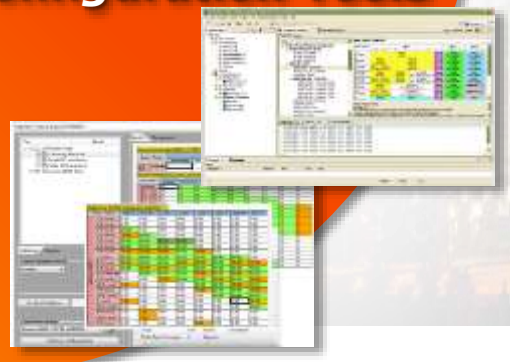
QorIQ Linux SDK

JTAG Run Control and Trace Probes

Performance Analysis and Trace Tools



QorIQ SoC Platform Configuration Tools



CodeWarrior Development Suites for Networked Applications www.freescale.com/CW4NET

CodeWarrior Development Suites for Networked Applications	LS Tower Level	Developer Level	Specialist Level	Architect Level
	$499 Annual Subscription Free Trial Available Buy	$2,999 Annual Subscription Free Trial Available Buy	$4,999 Annual Subscription Free Trial Available Buy	$9,999 Annual Subscription Free Trial Available Buy
Configuration Tools ***These software tools are unlicensed and will work even if you choose not to purchase any suite.***	RCW-PBL Configuration Linux Device Tree Configuration SerDes Configuration (**Coming soon**) Frame Distribution Wizard for DPAA (**Coming soon**) DDR Configuration			
ARMv7	Multicore Debugger for ARMv7 Flash Programming for Tower Board GCC for ARMv7 - Applications Compiler GCC for ARMv7 - Bare Metal Tower Boards ONLY Probe-less Debug Connection ONLY	Multicore Debugger for ARMv7 Flash Programming for ARMv7 GCC for ARMv7 - Applications Compiler GCC for ARMv7 - Bare Metal Debug any board		
CodeWarrior Specialist Tools Pack	Not included in this suite		SerDes Validation Tool (**Coming soon**) DDR Validation Tool STM-Debug Print (**Coming soon** for ARM-based tools) Scenarios Tool - Communications Peripheral Trace General Purpose Program ARM Trace (**Coming soon**)	

CodeWarrior Development Studio for QorIQ LS Series - ARM V7 ISA

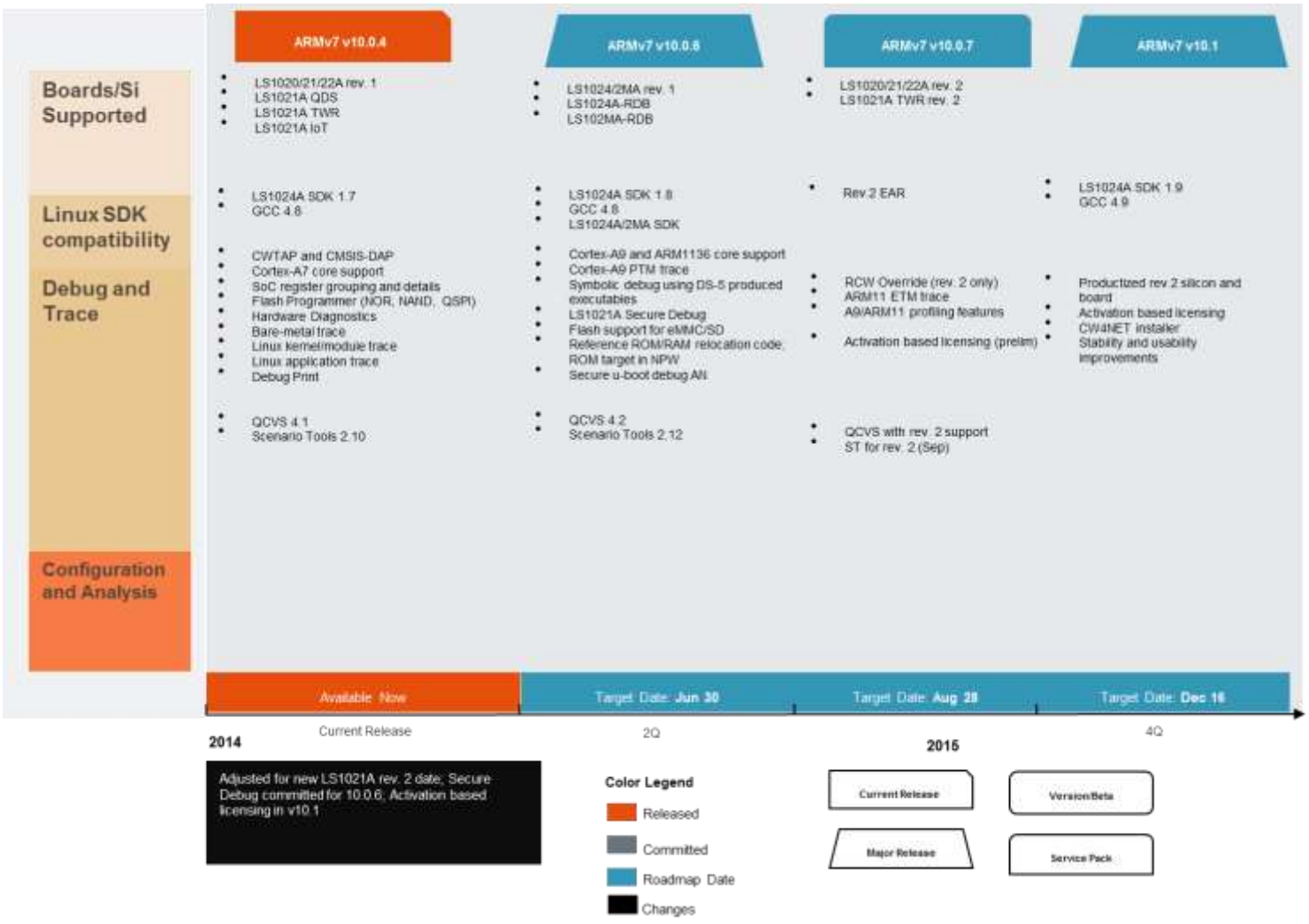
Available for public download and evaluation: freescale.com/CW4NET

- Current release:
- Version: 10.0.4
- Build Id: 141217

- SoC support:
  - LS1020A
  - LS1021A
  - LS1022A

- Reference Platform support:
  - LS1021ATWR
  - LS1021A-IOT

CodeWarrior for QorIQ LS Series, ARMv7 ISA Roadmap



CodeWarrior Development Studio: A Complete Development Environment Under Eclipse

- **Eclipse IDE**
  - Configuration Wizards
  - Plug-In Architecture
  - 3rd party community
- **Build Tools**
  - Linaro C/C++ Compiler
  - Linux and bare-metal ABI/runtimes
- **Initialization Tools**
  - SOC platform initialization and configuration
- **Run Control**
  - CW-TAP
  - CMSIS-DAP (TWR/IoT)

- **Debugger**
  - Cortex-A7, A9, ARM11
  - Multi-core aware
  - Cross-triggering
    - Run/Stop of targets simultaneously
  - Access to all on-chip resources
  - SoC register visibility and details
  - Secure/Non-Secure modes
  - Secure Debug
  - Flash
- **Trace & Profile**
  - Leverages extensive debug hooks on chip
    - Profiling Unit
    - In system trace buffering
  - Trace / Code / Performance Viewer
  - Off-line trace inspection
  - Debug Print

CodeWarrior Development Suites for Networked Applications: JTAG Probe Options

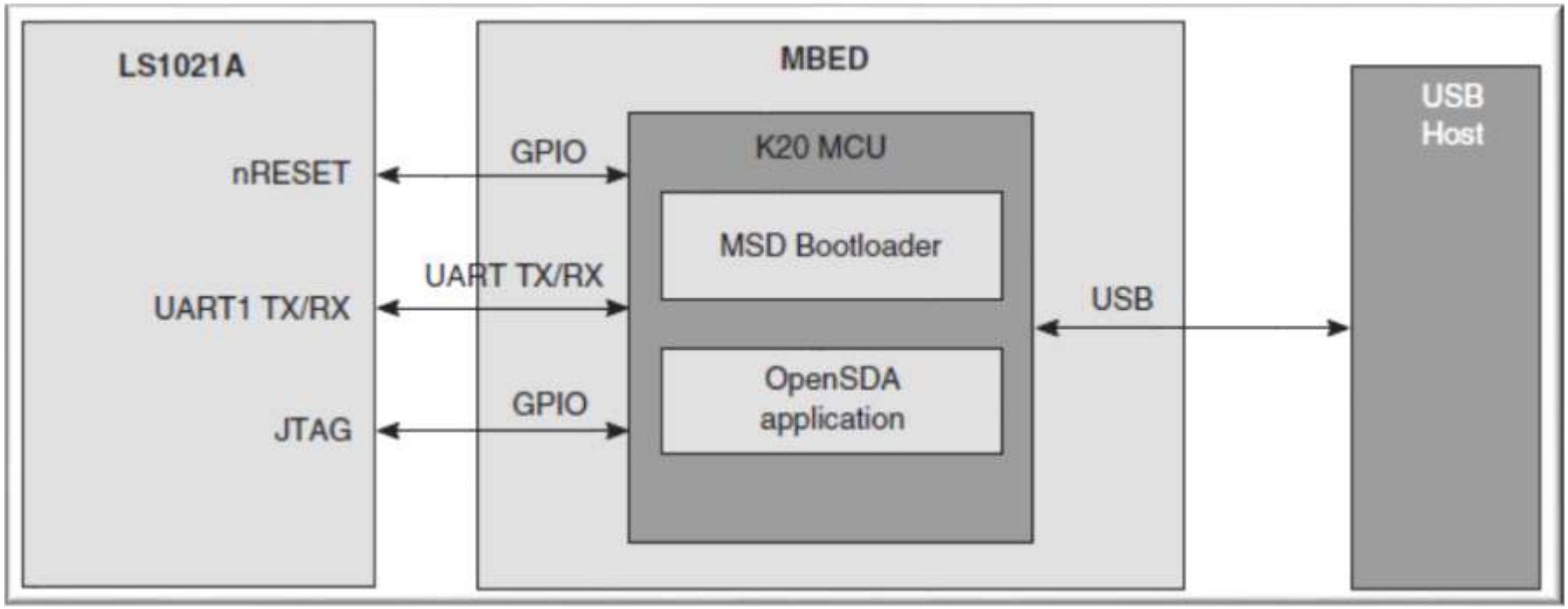
- mbed CMSIS-DAP*
  - TWR-LS1021A kit feature support at no additional cost
  - full CodeWarrior run control support
  - basic JTAG download speed
- CodeWarrior TAP
  - full CSS JTAG debug and CodeWarrior run control support
  - premium JTAG download speed
  - serial port pass through
  - operate locally over USB
  - operate remotely over Ethernet
  - buy separately (below $500)
- Reminder: no USB TAP support!

**CMSIS-DAP Cortex Microcontroller Software Interface Standard – Debug Access Port*

CodeWarrior Development Suites for Networked Apps JTAG Probe Options: CMSIS-DAP Debug Support

- Standard : mbed.org/handbook/CMSIS-DAP

- Manual : TWR-LS1021A Reference_Manual Rev0, Section 5.3 CMSIS-DAP debug support

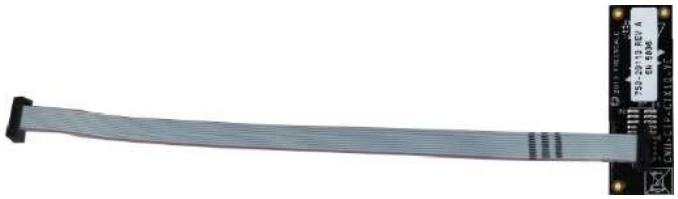


CodeWarrior Development Suites for Networked Apps JTAG Probe Options: CodeWarrior TAP

- CCS JTAG debugging and CodeWarrior run control requires:

Base Unit: (Part # CWH-CTP-BASE-HE)
www.freescale.com/webapp/sps/site/prod_summary.jsp?code=CW_TAP

... and Probe Tip: (Part # CWH-CTP-CTX10-YE)
www.freescale.com/webapp/sps/site/prod_summary.jsp?code=CWH-CTP-CTX10-YE



QorIQ LS1 Tools

Starting a CodeWarrior Bare Metal Project

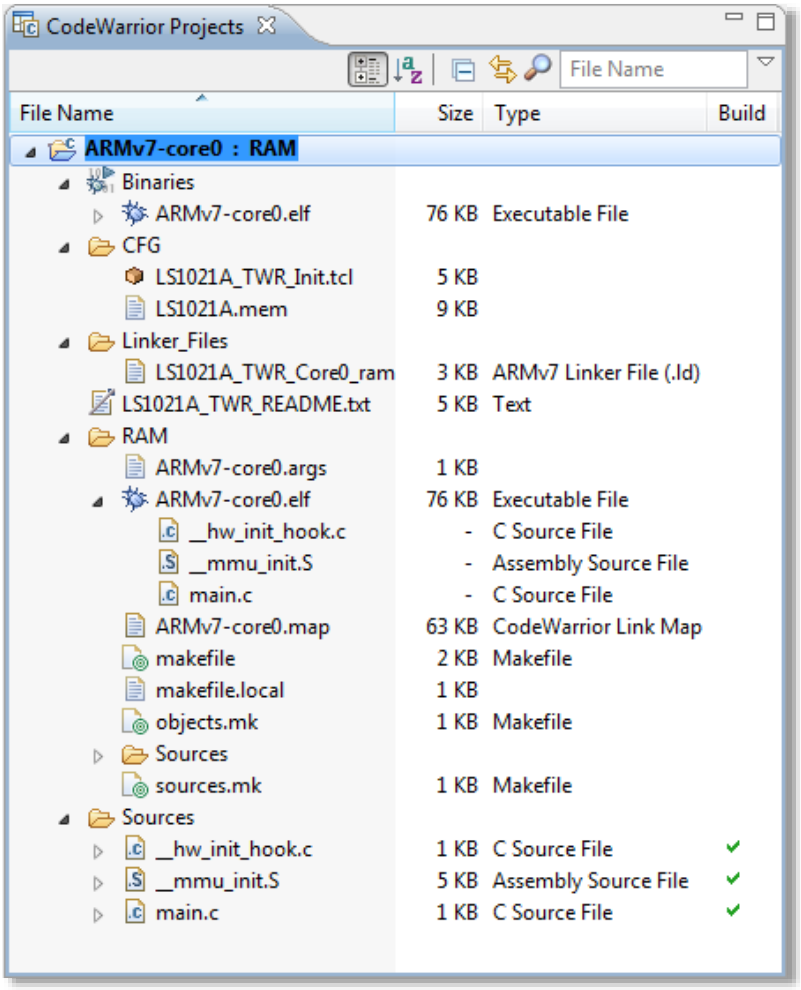
CodeWarrior Bareboard Debugging
Bareboard Debugging with CodeWarrior TAP Connection

- Launch CodeWarrior ARMv7 from the desktop, then proceed as follows:

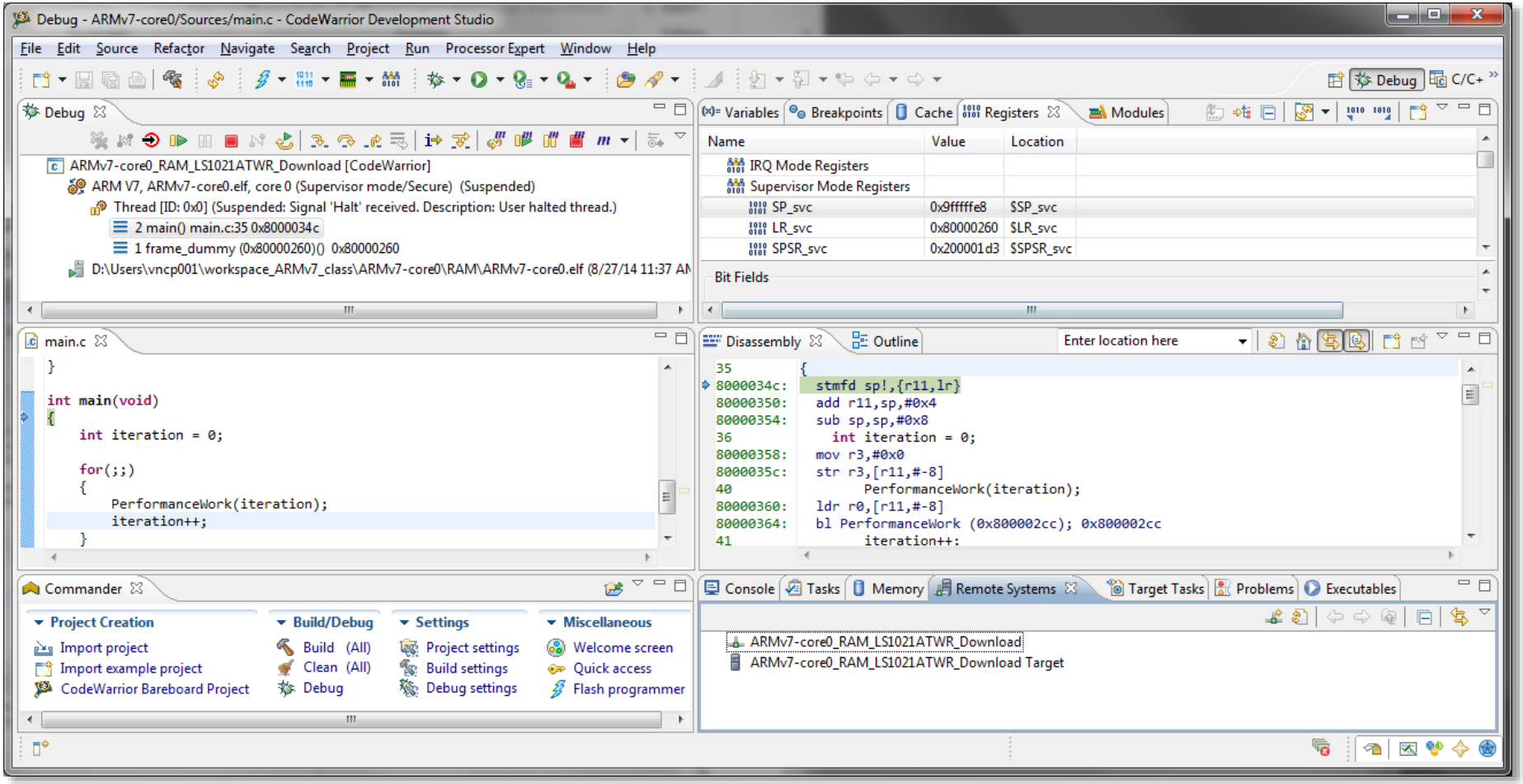
- Go to Workbench
- **File → New → CodeWarrior Bareboard Project**
- Enter a **Project Name**
- Choose:
  - **LS1021A** Processor
  - **LS1021ATWR** Hardware
  - **Download - Default**
  - **CodeWarrior TAP (over USB)** Connection Type
- Continue with **Next** then **Finish**

CodeWarrior Bareboard Debugging (con't)
Bareboard Debugging with CodeWarrior TAP Connection

- Select your project
- Do Build All (Ctrl + B)
- Do Run → Debug (F11)
  - Debug Perspective opens
  - ELF file is downloaded to the TWR-LS1021A
  - LED D2 will blink rapidly during activity
  - Debugger stops in core0 in main()
- View registers



CodeWarrior Bareboard Debugging (con't)
Bareboard Debugging with CodeWarrior TAP Connection



What if My Board is Corrupted or Blank?

- Highly recommended to use alternate bank in NOR flash for “experimental” programming.
- If both banks becomes corrupted, you can use Code Warrior to recover your board.
- Use the SD Card that comes with your LS1021A-TWR to recover your board

TWR-LS1021A

Freescale Linux SDK for LS1021A V1.7
Status and Roadmap

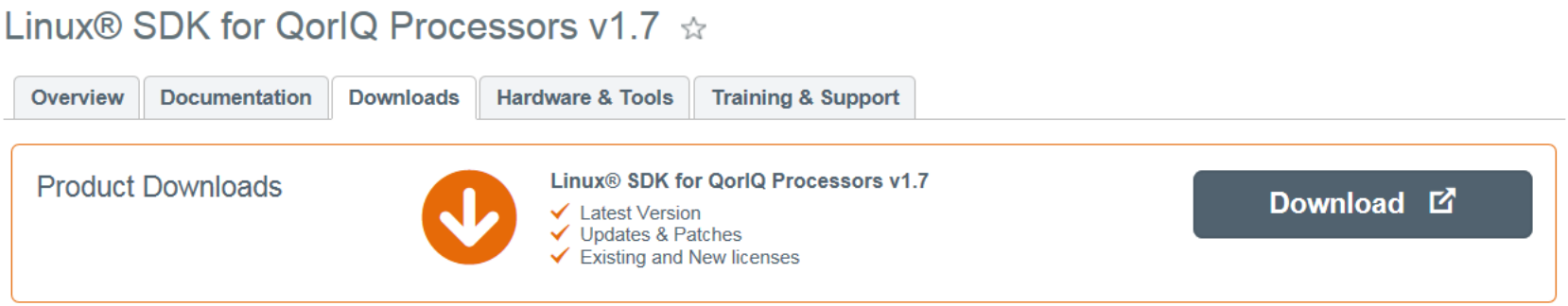
Freescale Linux SDK for QorIQ LS1021A V1.7

- A no-cost Software Development Kit for LS1021A platforms:

- Based off the Yocto ProjectTM (www.yoctoproject.org)
- GCC compiler tool chain
- u-boot boot loader
- Linux kernel and user space packages
- QorIQ LS1 specific s/w packages
- A build system and a package manager
- Support for TWR-LS1021A reference platform, providing known-good configurations and images

Freescale Linux SDK for LS1021A V1.7

- Will be included on USB stick in kit
- Available for free download on www.freescale.com/sdk



Freescale Linux SDK for LS1021A V1.7
LS1021A-SDK-V1.7-ARM Release Media

- IMAGE: QorIQ Linux SDK v1.7CORTEXA Yocto Image.iso
  - Yocto/bitbake + pre-built images (u-boot, kernel, RCW, rootfs, ucode)
  - Use to quickly deploy to/update a TWR-LS1021A without building images
- CACHE: QorIQ Linux SDK v1.7CORTEXA Yocto Cache.iso
  - Yocto/bitbake + prebuilt archives for all packages
  - Use on any build machine
  - Will pull source on-demand from the Internet
- SOURCE: QorIQ Linux V1.7SDK Yocto Source ISO.iso
  - Yocto/bitbake + full source for all packages (fast build PC advised)
  - Use for full development work or on standalone build machines
  - Documentation (PDFs not installed : access manually)

Freescale Linux SDK for LS1021A V1.7 Features

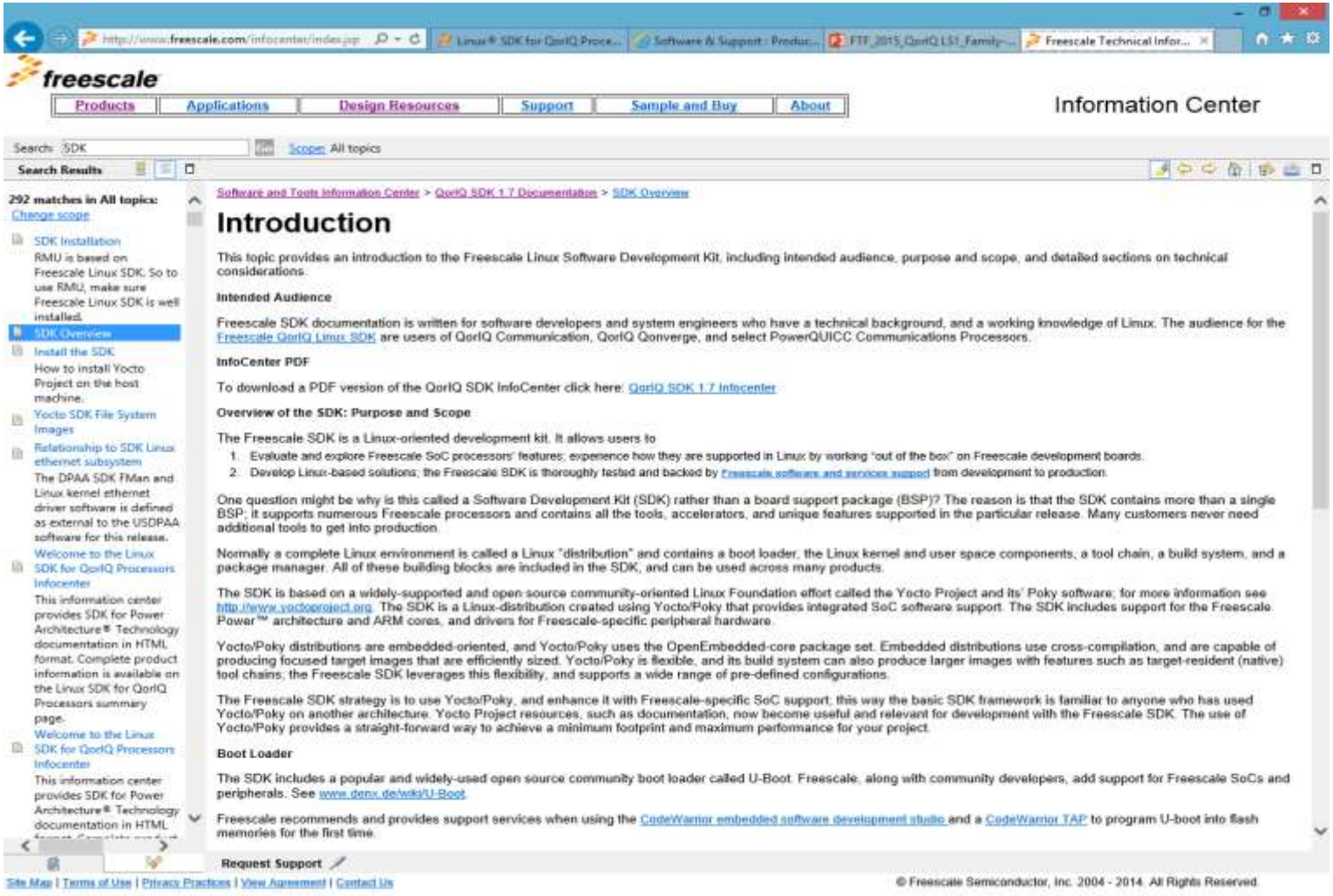
- U-Boot 2014.07
  - Boot from NOR, SDHC
  - Dcache enabled
  - DCU (TWR-LCD-RGB) (color bar demo)
  - DDR3 SPD
  - Flextimer testing command
  - I2C and EEPROM
  - Integrated Flash Controller (IFC) NOR
  - LPUART
  - QSPI
  - Read ID and MAC from EEPROM (except SD boot)
  - SATA basic support
  - Secure Boot
  - Secured Digital Host Controller (eSDHC)
  - UART
  - USB 2.0 on Synopsys controller/PHY
  - VeTSEC
  - Virtualization extension support
- Yocto
  - Yocto/Poky 1.7.1 "Daisy"
- GNU Toolchain
  - gcc-linaro-4.8-2014.04
  - binutils-linaro-2.24-r2014.04
  - eglibc-linaro-2.18-r2014.04
  - gdb-linaro-7.6.1-r2013.10
- Other Tools and Utilities
  - Power Consumption Monitor

Freescale Linux SDK for LS1021A V1.7 Features (con't)

- Linux kernel 3.12
  - ARM A7 core SMP support
  - ARM GIC
  - ARM General Virtual Timer
  - CAAM
  - CPU in HYP mode and virtualization extension support
  - DUART
  - DCU (TWR-LCD-RGB) and HDMI
  - eDMA & DMAMUX with limited functionality
  - Ethernet eTSEC (gianfar)
  - FlexTimer (PWM)
  - GPIO
  - I2C1 and I2C3 for LTC2945
  - IEEE1588
  - Integrated Flash Controller (IFC) NOR
  - LPUART
  - PCIe INTx and MSI
  - PHY support: RGMII, SGMII
  - Power Management (core state: wait and stop)
  - QSPI
  - Secured Digital Host Controller (eSDHC) and SD/MMC
  - USB 2.0 and 3.0 host and gadget on Synopsys controller/PHY

www.freescale.com/infocenter

The source for all SDK questions



SDK V1.7 LS1021A image.iso

- Mount the image.iso
- Familiarize yourself with the available image files:

```
Image.iso
├── flash-image
│   └── QorIQ_SDK_V1.7_LS1021ATWR_20141218_NOR_FLASH.bin          Tower  full NOR flash restore image
│       QorIQ_SDK_V1.7_LS1021AQDS_20141218_NOR_FLASH.bin          QDS  full NOR flash restore image
├── fsl-toolchain
│   └── LS1021A_SDK_V1.7_ARM_20141218_ROOTFS_Image.tar.gz         prebuilt toolchain
│       fsl-networking-eglibc-i686
├── full-rootfs
│   └── LS1021A_SDK_V1.7_ARM_20141218_ROOTFS_Image.tar.gz         rootfs for external storage devices
│                                                                 (USB stick, HDD, ...)
└──ls1021atwr
    │   fsl-image-core-ls1021atwr-<datetime>.rootfs.ext2.gz.u-boot   ramdisk rootfs (fits NOR flash)
    │   fsl-image-core-ls1021atwr-<datetime>.rootfs.jffs2           JFFS rootfs (NOR flash)
    │   u-boot-ls1021atwr_nor-2014.10+fslgit-r0.bin                 NOR flash u-boot image
    │   u-boot-with-spl-pbl-ls1021atwr_sdcard-2013.10+fslgit-r0.bin SDCard u-boot image
    │   uImage--3.12-r0-ls1021a-twr-<datetime>.dtb                  device tree blob (dtb)
    │   uImage--3.12-r0-ls1021atwr-<datetime>.bin                   Linux compressed binary kernel image
    │
    └──rcw                                                          SoC Reset Config Word images
        ├──RSR_PPS_70
        └──SSR_PPN_20                                               Default RCW 0x20
```

SDK V1.7 image.iso
RCW File Naming Conventions and Use Cases

RCW Folder legend: **abc_def_gg (ex: SSR_PPN_20)**

abc : eTSEC1/2/3 → **R** = RGMII | **S** = SGMII | **N**
de : PCIe@slot1/2# → **P** = PCIe | **N**
f : SATA → **S** = SATA | **N**
gg : SRDS_PRTCL → 2-digit hex value of serdes1 protocol

N = not used/not available

RCW filename convention :

rcw_<core_freq>[_<bootmode>][_<special setting>].bin

special setting → **lpuart** = used for lpuart
dcu = DCU test
sben = secure boot enabled

Example: rcw_1000.rcw = 1000Mhz core with NOR boot
rcw_1000_sd.rcw = 1000Mhz core with SD boot

TWR-LS1021A

SDK V1.7 Prebuilt u-boot Image

u-boot Startup Messages

- Reset the TWR-LS1021A, interrupt the countdown
- Review the u-boot output in the console window:

```
U-Boot 2014.07+lsl+g659b6a2 (Dec 23 2014 - 01:09:29)
CPU:   Freescale LayerScape LS1021E, Version: 1.0, (0x87081110)
Clock Configuration:
       CPU0(ARMV7):1000 MHz,
       Bus:300  MHz, DDR:800  MHz (1600 MT/s data rate),
Reset Configuration Word (RCW):
       00000000: 0608000a 00000000 00000000 00000000
       00000010: 20000000 00407900 e0025a00 21046000
       00000020: 00000000 00000000 00000000 00038000
       00000030: 00000000 881b7540 00000000 00000000
Board: LS1021ATWR
CPLD:  V2.2
PCBA:  V3.0
VBank: 0
I2C:   ready
DRAM:  1 GiB
Using SERDES1 Protocol: 32 (0x20)
```

u-boot: u-boot Startup Messages

```
Flash: 128 MiB
MMC:   FSL_SDHC: 0
EEPROM: NXID v1
Firmware 'Microcode version 0.0.0 for T1040 r1.0' for 1040 V1.0
QE: uploading microcode 'Microcode for T1040 r1.0'
In:    serial
Out:   serial
Err:   serial
Net:   eTSEC1 is in sgmii mode.
eTSEC2 is in sgmii mode.
eTSEC1 [PRIME], eTSEC2, eTSEC3
Hit any key to stop autoboot:  0
```

u-boot NOR Flash Map - Active and Alternate vBanks

- The TWR-LS1021A has 128MB of NOR flash located a 0x6000_0000

Address	Image	vBank	Size
0x6000_0000	RCW	0 - Active	128K
0x6002_0000	DTB	0 - Active	1M
0x6012_0000	Kernel	0 - Active	8M
0x6092_0000	RamDisk	0 - Active	54.25M
0x63F6_0000	*u-boot envvars*	*4 - Alternate*	*128K*
0x63F8_0000	*u-boot*	*4 - Alternate*	*512K*
0x6400_0000	*RCW*	*4 - Alternate*	*128k*
0x6402_0000	*DTB*	*4 - Alternate*	*1M*
0x6412_0000	*Kernel*	*4 - Alternate*	*8M*
0x6492_0000	*RamDisk*	*4 - Alternate*	*54,125 MB*
0x67f4_0000	QE microcode	N/A	128K
0x67F6_0000	u-boot envvars	0 - Active	128K
0x67F8_0000	u-boot	0 - Active	512K

u-boot NOR Flash Map - Active and Alternate vBanks

- The on-board CPLD can swap top and bottom flash halves on reset, allowing boot from either vBank
- Each vBank has a different boot configuration according to its RCW, u-boot image and jumper setting:
  - vBank0 : console via on-board UART
  - vBank1 : console via LPUART on TWR-SER2
- Provided you have a TWR-LS1021A configured with either:
  - optional elevator + TWR-SER2 boards + default NOR content
  - vBank1 RCW + u-boot copied from vBank0
- ... you can switch between the Active and Alternate vBank by:
  - flipping SW3[5] then h/w reset
    or issue u-boot command :
  - then check for the VBank: # in the

```
=> boot_bank 0 // default
=> boot_bank 1 // alternate
```

u-boot Environment Variables

```
=> print
baudrate=115200
bootargs=root=/dev/ram0 rw console=ttyS0,115200
bootcmd=setenv bootargs root=/dev/ram rw console=$consoledev,$baudrate $othbootargs;bootm 0x60120000 0x60920000 0x60020000
bootdelay=3
bootfile=ls1021atwr/uImage-ls1021atwr.bin
consoledev=ttyS0
dnsip=10.192.130.201
eth1addr=00:E0:0C:BC:E5:61
eth2addr=00:E0:0C:BC:E5:62
ethact=eTSEC1
ethaddr=00:E0:0C:BC:E5:60
ethprime=eTSEC1
fdt_high=0xcfffffff
fdtfile=ls1021atwr/ls1021a-twr.dtb
fileaddr=88000000
filesize=1245531
gatewayip=10.192.208.254
initrd_high=0xcfffffff
ipaddr=192.168.1.100
lcd_test_b1=mw 0x1570200 0xffffffff;mw 0x1570028 0x00000280;mw 0x2ce0054 0x27000000;mw 0x2ce0018 0x1e001001;mw 0x2ce001c
0x02488100;mw 0x2ce0020 0x02104000;mw 0x2ce0024 0x03000000;mw 0x2ce0010 0x03800000;
[...]
lcdinit=protect off all;erase 60000000 6001ffff;cp.b 63f00000 82000000 100;cp.b 82000000 60000000 100;
loadaddr=0x82000000
netmask=255.255.255.0
ramboot=dhcp 82000000 $bootfile;dhcp 8f000000 $fdtfile;dhcp 88000000 $ramdiskfile;bootm 82000000 88000000 8f000000
ramdiskfile=ls1021atwr/fsl-image-core-ls1021atwr.ext2.gz.u-boot
recover=set bootcmd;save;reset;
scsidevs=0
serverip=192.168.1.101
[...]
Environment size: 1385/131068 bytes
```

network configuration
image files
boot commands

u-boot Network Setup

- MAC address environment variables ethaddr, eth1addr and eth2addr are set by values stored in EEPROM.
  To manually change the EEPROM MAC addresses:

```
=> mac id
=> mac 0 00:e0:0c:bc:e5:60
=> mac 1 00:e0:0c:bc:e5:61
=> mac 2 00:e0:0c:bc:e5:62
=> mac save
Programming passed.
```

- Establishing network connectivity in your network environment:

```
=> setenv ipaddr <TWR-LS1021A IP>      ➔ IP address of TWR-LS1021A
=> setenv serverip <host IP>             ➔ IP address of TFTP server
=> setenv ethaddr '00:e0:0c:bc:e5:60'
=> ping $serverip
Speed: 1000, full duplex
Using eTSEC3 device
host 192.168.1.101 is alive
=> saveenv                               ➔ preserves envvars across boots
```

u-boot: NOR Copy Issues

- NOR→NOR copy issue:

  A direct cp.b from a source NOR address to destination NOR address results in all 0's in the destination flash sector.

  - Use case : copying between active alternate flash images
  - Workaround: copy source data to an intermediate DDR address first, then copy from DDR to NOR

- Odd byte count copy issue:

  cp.b of an odd byte count to a NOR address, writes the final odd byte 1 byte too far

- Use case: any manual cp command
- Workaround: round up byte count to copy to next even # of bytes

TWR-LS1021A

Examining the Pre-Boot Loader

The Pre-Boot Loader Demystified

What is a PBL?

The Pre-Boot Loader or “PBL” can be viewed as a non-programmable state machine which on RESET loads in the very basic configuration for the core to boot. Examples would be core PLL multipliers and SERDES configurations. There is also the capability for pre-loading core or IP registers throughout the memory map. This becomes a very powerful and flexible tool.

Helpful Chapters from the LS1021A Reference Manual, Revision F:

4.4.3.1 Reset configuration word (RCW) source

4.4.4 Reset Configuration Word

4.4.5 RCW Field Definitions

10.1 Pre-Boot Loader Overview

10.4.3 Required format of data structure used by PBL

Components of the PBL

1) The Reset Control Word or “RCW” – register contents loaded from an NV source which set PLL’s, I/O multiplexing, and other fixed system configuration.

- Example from uboot screen:

Reset Configuration Word (RCW):

00000000: 0608000a 00000000 00000000 00000000
00000010: 20000000 00407900 e0025a00 21046000
00000020: 00000000 00000000 00000000 00038000
00000030: 00000000 881b7540 00000000 00000000

2) The Pre-Boot Loader Instructions or “PBI” – these are optional register contents which can be loaded into register across the memory map.

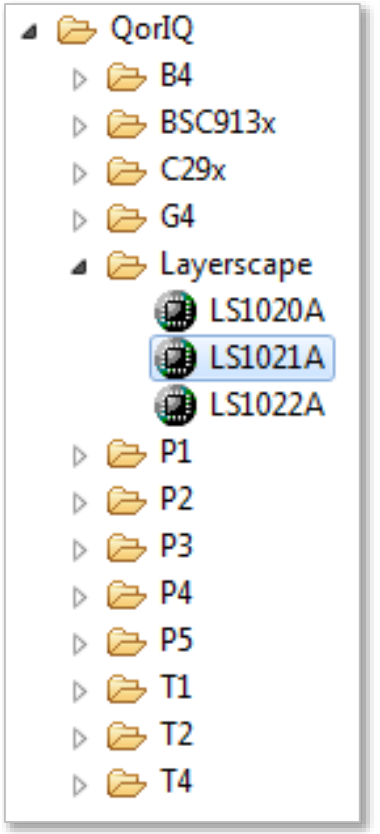
Do It the Easy Way – Use QorIQ Configuration Suite!

QorIQ LS1 Tools

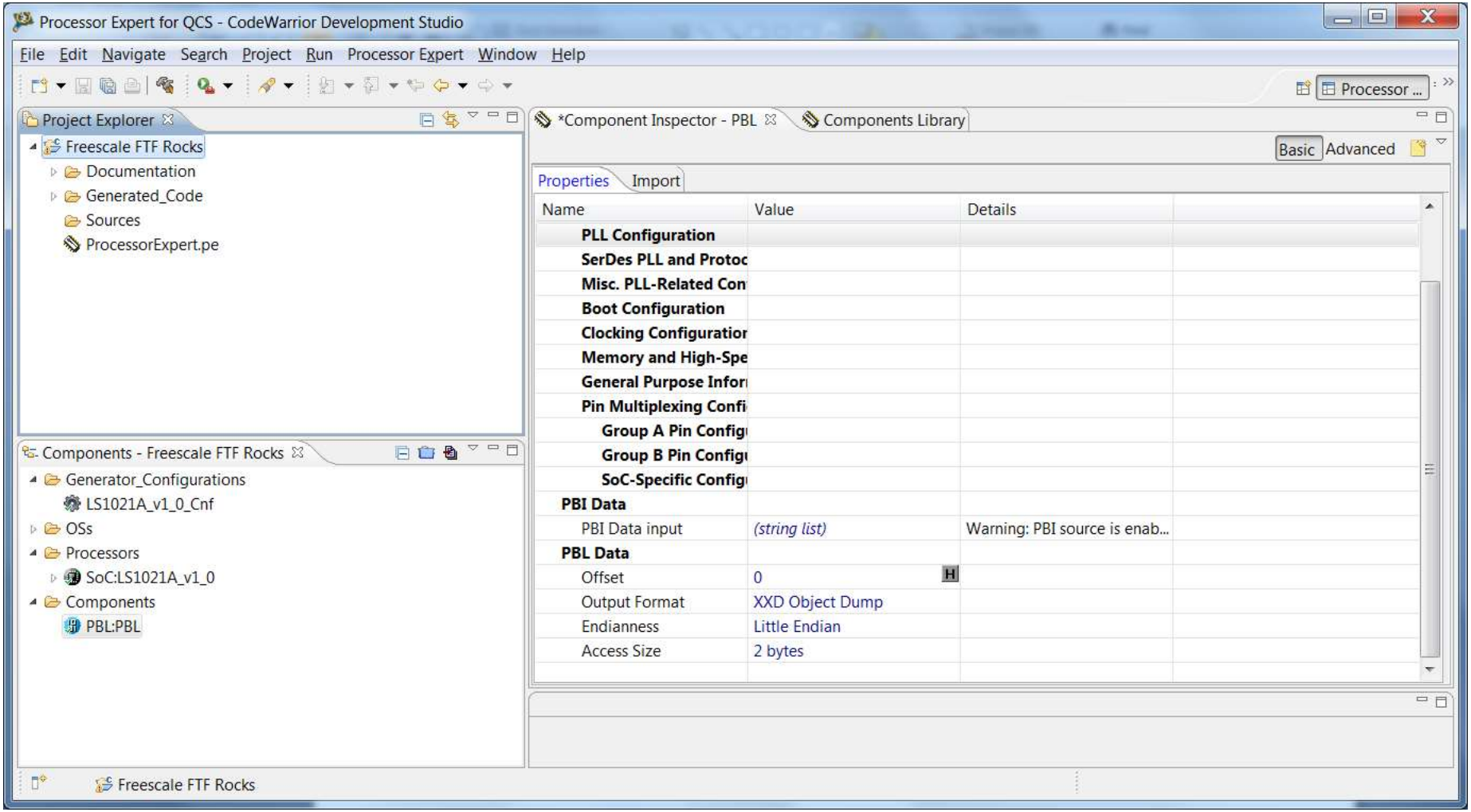
QorIQ Configuration and Validation Suite 4.2.0

QorIQ Configuration and Validation Suite QCVS 4.2.1 – Included in CodeWarrior 10.0.4

- No-cost configuration tool for all QorIQ platforms
- Tool components generate board init code and data:
  - PBL Pre-Boot Loader configuration
  - DDR controller configuration
  - HW Device Tree editor
- Current version supporting TWR-LS1021A:
  Version 4.2.0 / Build: 0001-20150403



QorIQ Configuration and Validation Suite Installed with Code Warrior ARMv7



QCVS

1. Create a new QCVS project for LS1021A
   - File → New → QorIQ Configuration Project
   - Check *PBL Configuration*
   - *Create default configuration*
2. Select *Components : PBL:PBL* to open the Inspector View
3. From UBOOT memory dump, import the current RCW file (Import tab), using:
   - Input Format : Binary
   - Endianness : Big Endian
4. In the Problems View:
   - Check the Errors and Warnings for IFC_GRP_E1_EXT
   - Check Ignore constraints and non-critical errors in the Inspector View Menu pull down (top right)

QCVS (con't)

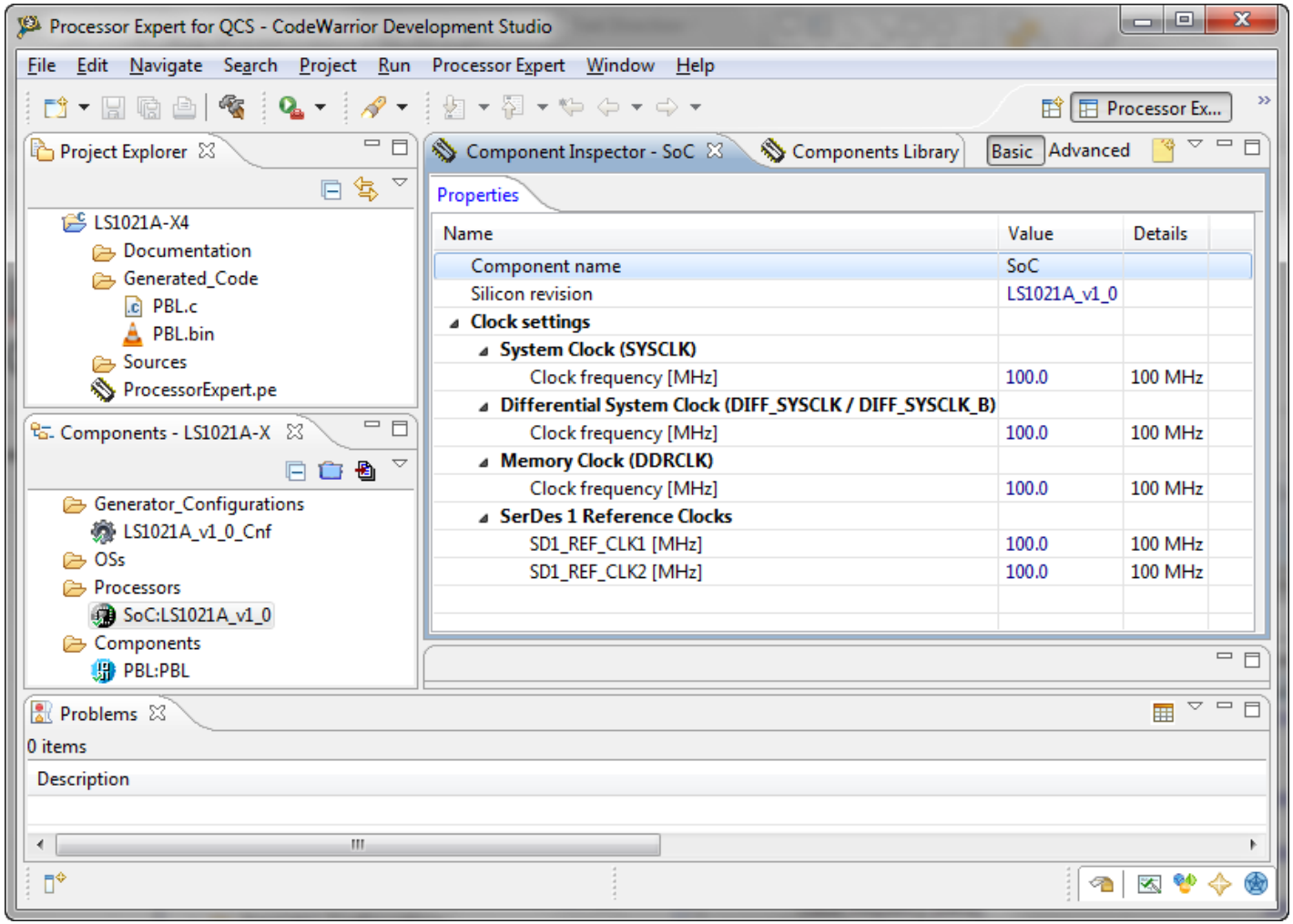
5. Adjust System Clock field to reflect new TWR-LS1021A hardware configuration

6. Compare PBL Inspector View info vs. u-boot output for:
   - clock and PLL frequencies
   - SERDES_PRTCL
   - I/O enabled by the SERDES_PRTCL

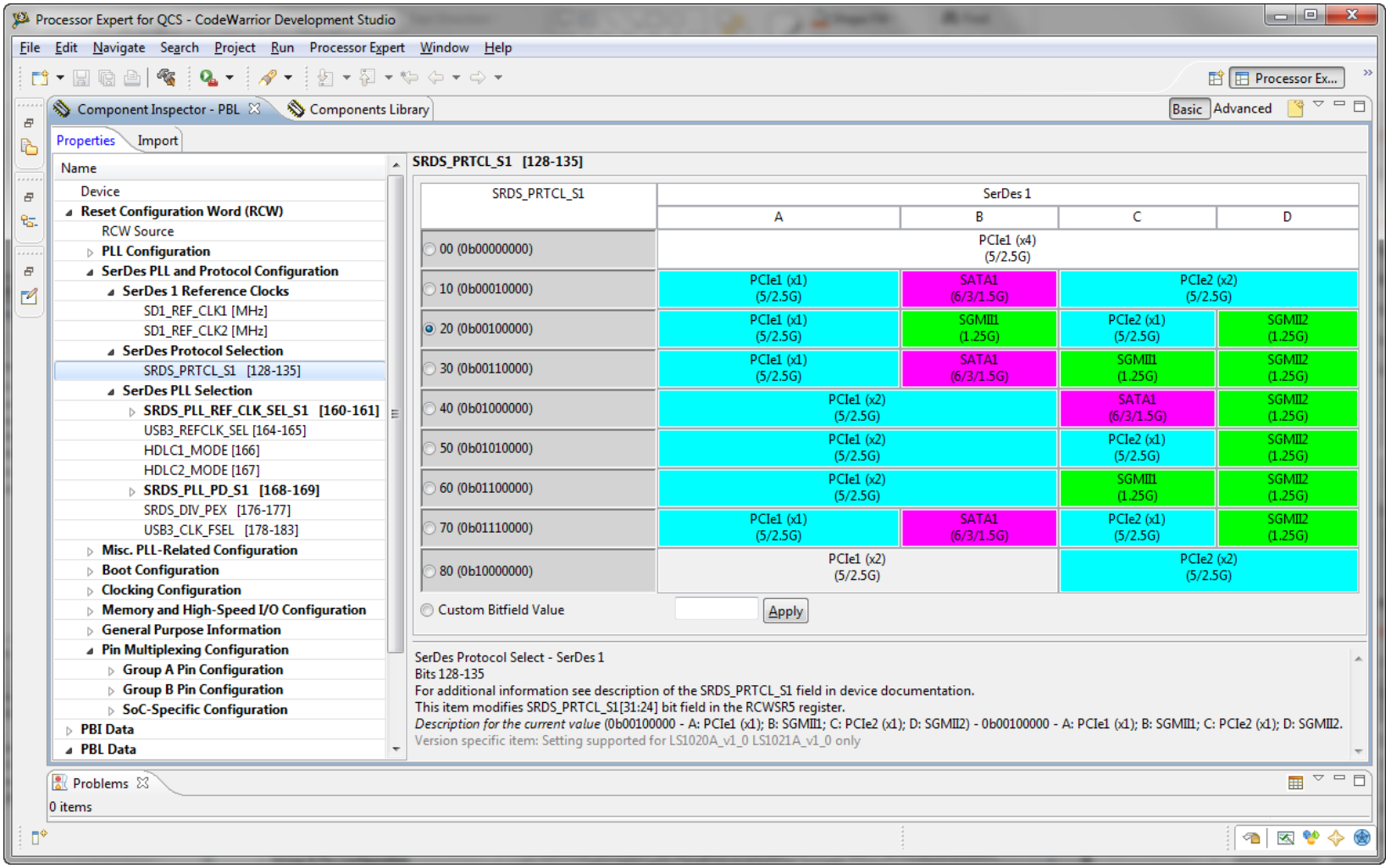
7. Generate a PBL output file of type *binary* and *u-boot* command
   - Output Format: Binary
   - Endianness: Big Endian (!)

8. Class discussion: How would you deploy either file?

QorIQ LS1: QCVS - SoC Inspector



QorIQ LS1: QCVS - PBL Component



TWR-LS1021A

Program in New RCW

TWR-LS1021A: Update NOR Flash Image to SDK V1.7

- Change to default switch setting

SW 3 *(default)*

```
1 2 3 4 5 6 7 8
. o o . . . . o [ON=1]
o . . o o o o . [OFF=0]
```

SW 2 *(default)*

```
1 2 3 4 5 6 7 8
o . . . o o o o [ON=1]
. o o o . . . . [OFF=0]
```

- Reset the TWR-LS1021A
- U-boot: Network Setup

```
=> setenv ipaddr <TWR-LS1021A IP>      ➔ IP address of TWR-LS1021A
=> setenv serverip <host IP>           ➔ IP address of TFTP server
=> setenv ethaddr '00:e0:0c:bc:e5:60'
=> ping $serverip
Speed: 1000, full duplex
Using eTSEC3 device
host 192.168.1.101 is alive
=> saveenv                             ➔ preserves envvars across boots
```

TWR-LS1021A: Copy RCW from NOR flash bank0 to bank1

```
Unprotect the sectors for RCW and uboot, and erase them:
=> protect off 0x64000000 0x6401ffff
Un-Protected 1 sectors

=> erase 0x64000000 0x6401ffff
. done
Erased 1 sectors

=> md 0x64000000 64
64000000: ffffffff ffffffff ffffffff ffffffff    ................


Copy the RCW from bank0 to our loadaddr DDR (0x82000000).
=> md.b $loadaddr 80
82000000: ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff    ................

⇒ cp.b 0x60000000 0x82000000 78

=> md.b $loadaddr 80
82000000: aa 55 aa 55 01 ee 01 00 06 08 00 0a 00 00 00 00    .U.U............

=> cp.b $loadaddr 0x64000000 78
Copy to Flash... 9done

⇒ cmp.b 0x60000000 0x64000000 80
   byte at 0x60000034 (0x0) != byte at 0x64000034 (0x20)
  Total of 52 byte(s) were the same
```

TWR-LS1021A - Recovery

SD card boot image for TWR-LS1021A recovery

TWR-LS1021A: Recovering a Bricked TWR-LS1021A

- Always work out of the ALTBANK so you can restore a known good working configuration

- When a returned TWR-LS1021A no longer boots, check this:
  - switch settings → return to default and retry
  - wrong/missing RCW image in flash prevents SoC initialization
  - bad/wrong/missing u-boot image prevents core from booting

- To recover:
  - change h/w configuration, flip *SW3[5]* to alternate bank and reset
    - Successful → proceed with full NOR flash update (previous slide) or selective image update
    - still bricked → boot TWR-LS1021A from SDCard into u-boot, then reprogram NOR flash

    or → Using JTAG and CW flash programmer connect to TWR-LS1021A reprogram RCW and UBOOT to NOR flash

Activity 7 - TWR-LS1021A
Program the Image to SD Card in u-boot

- Install the SD card on TWR-LS1021A
- Reset the TWR-LS1021A, interrupt the countdown
- u-boot: Network Setup
- Connect the TWR-LS1021A to the same LAN with the host. Make sure the host and the TWR-LS1021A can 'ping' each other successfully

```
=> setenv ipaddr <TWR-LS1021A IP>  ➔ IP address of TWR-LS1021A
=> setenv serverip <host IP>       ➔ IP address of TFTP server
=> setenv ethaddr '00:e0:0c:bc:e5:60'
=> ping $serverip
Speed: 1000, full duplex
Using eTSEC3 device
host 192.168.1.101 is alive
=> saveenv                         ➔ preserves envvars across boots
```

Activity 7 - TWR-LS1021A
Program the Image to SD Card in u-boot (con't)

- Start the tftpd64 utility from the Desktop
- Browse to desktop <Current Directory> to:

```
# Download rcw+uboot file from ls1021atwr folder
=> tftp 82000000 u-boot-with-pbl-ls1021atwr_sdcard.bin
Speed: 100, full duplex
Using eTSEC3 device
TFTP from server 10.81.44.180; our IP address is 10.81.44.0
Filename 'u-boot-with-pbl-ls1021atwr_sdcard.bin'.
Load address: 0x82000000
Loading: ############################
         934.6 KiB/s
done
Bytes transferred = 408716 (63c8c hex)

# Program SD card
=> mmc write 82000000 8 400
 MMC write: dev # 0, block # 8, count 1024 ... 1024 blocks write: OK

# Change the SW2 setting:
SW2[1:8]=0b'0010'1111

# Reset the TWR-LS1021A
```

Freescale Has World Class Support….and MORE

Global Technical Information Center
Design & Support Resource

Networking Applications Team
Depth of Expertise & Knowledge

Design With Freescale, Freescale Technology Forum
Training

Networking Software and Services Group

- Commercial Solutions
- Engineering Services
- Guaranteed Performance
- Service Level Agreement Support…and MORE

- Visit Pedestal 415 in the Technology Lab

Q&A

www.Freescale.com