FTF FREESCALE TECHNOLOGY FORUM 2015

Hardware Design Guidelines for S12 MagniV Mixed-Signal Microcontroller

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External Use

Agenda

- Introduction to MagniV
- Power Supply Pins
- Programming Interface
- External and internal RC Oscillator
- Programming Circuit
- CAN Physical Layer
- LIN Physical Layer
- High Current / High Voltage Pins
- Motor Control Interface
- MagniV in 24V Applications
- Summary

Introduction to MagniM MCUs

S12 MagniV: Integration Beyond the MCU

Our **S12 MagniV** portfolio simplifies system design with the integration on High-Voltage (HV) analog features onto MCUs for automotive applications

S12VR
Relay based DC Motors

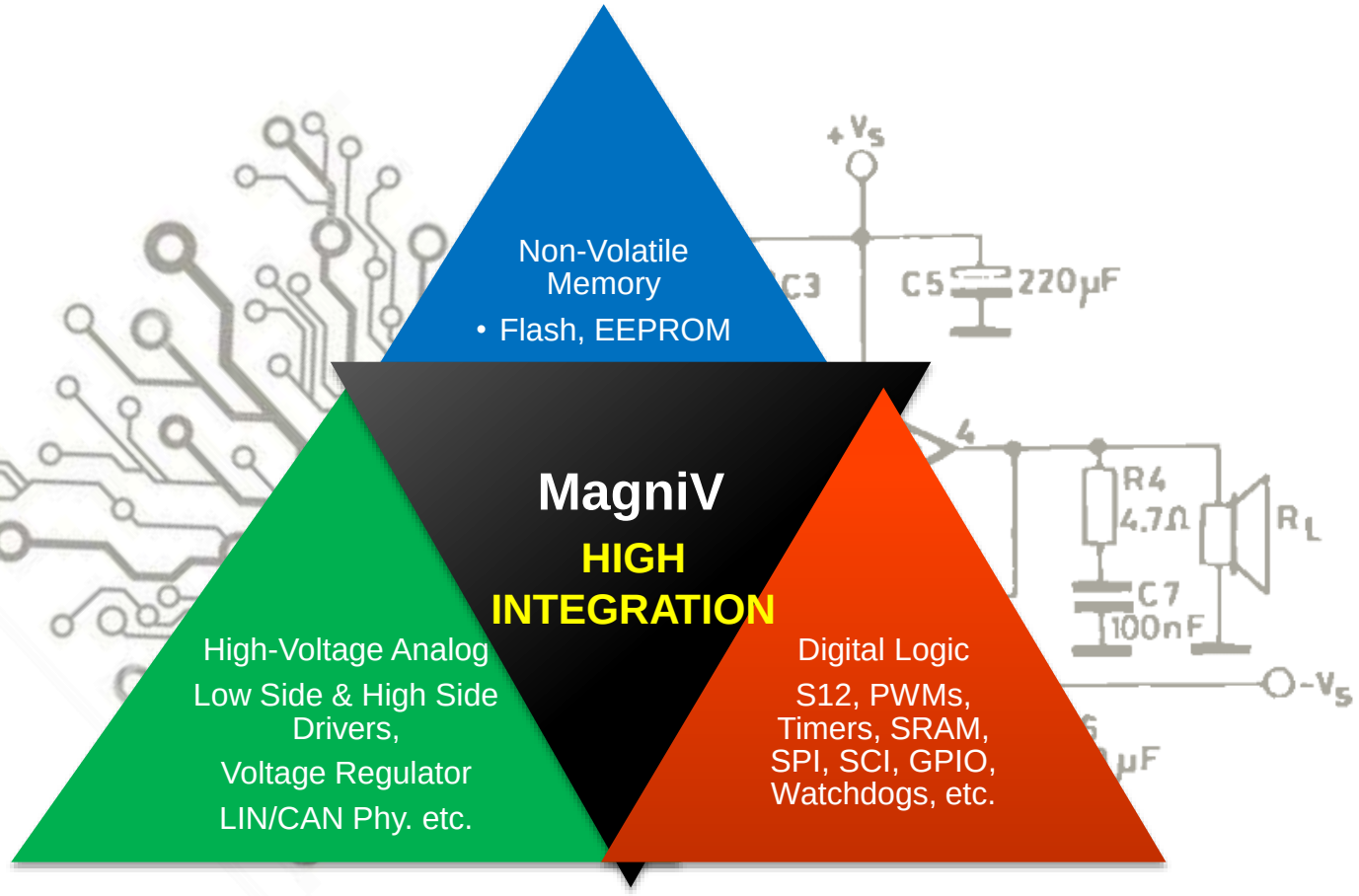
S12ZVM
BLDC Motor Control

S12ZVC
Small CAN nodes

S12ZVL
LIN Nodes

S12ZVH
Cluster Solutions

A Technology Sweet-spot for Sensor and Actuators



S12 MagniV Benefits

S12 MagniV solutions deliver optimal **system cost** **and physical footprint** for sensor and actuator applications.

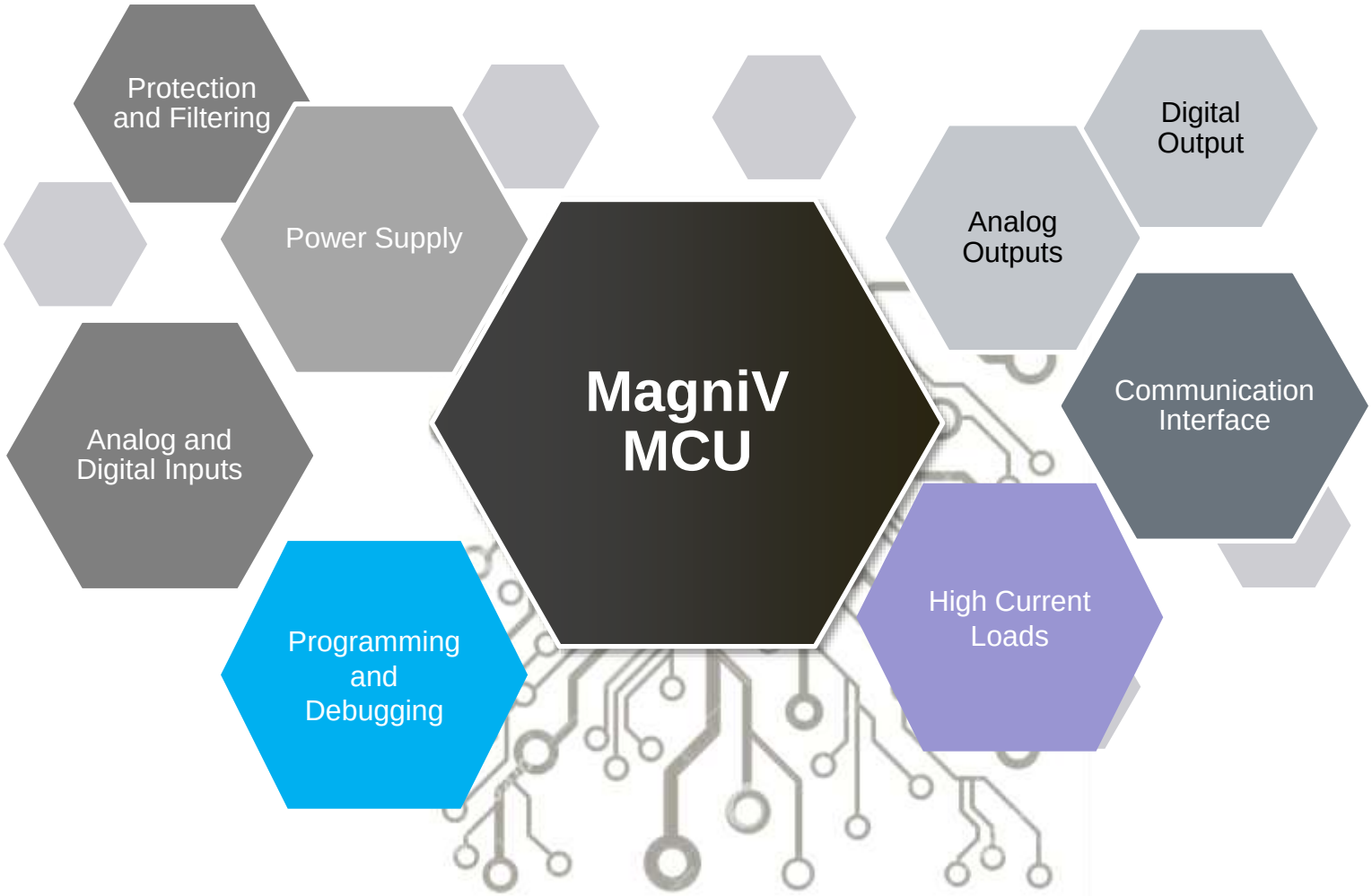
Reduced PCB Space
Up to 30%

Improved manufacturing efficiency
Replacing typically 3 IC by 1 MagniV reduces assembly and test cost while quality improves

Reduced Bill Of Material (BOM)
Fewer components to purchase, handle, store and qualify

Simplified motor control that speeds up time-to-market
Save up to 6 months on development, validation and ISO26262 implementation
- Abstract the complexity of 3-phase motor control software development
- Production ready Automotive quality SW and Tools
- SafeAssure program

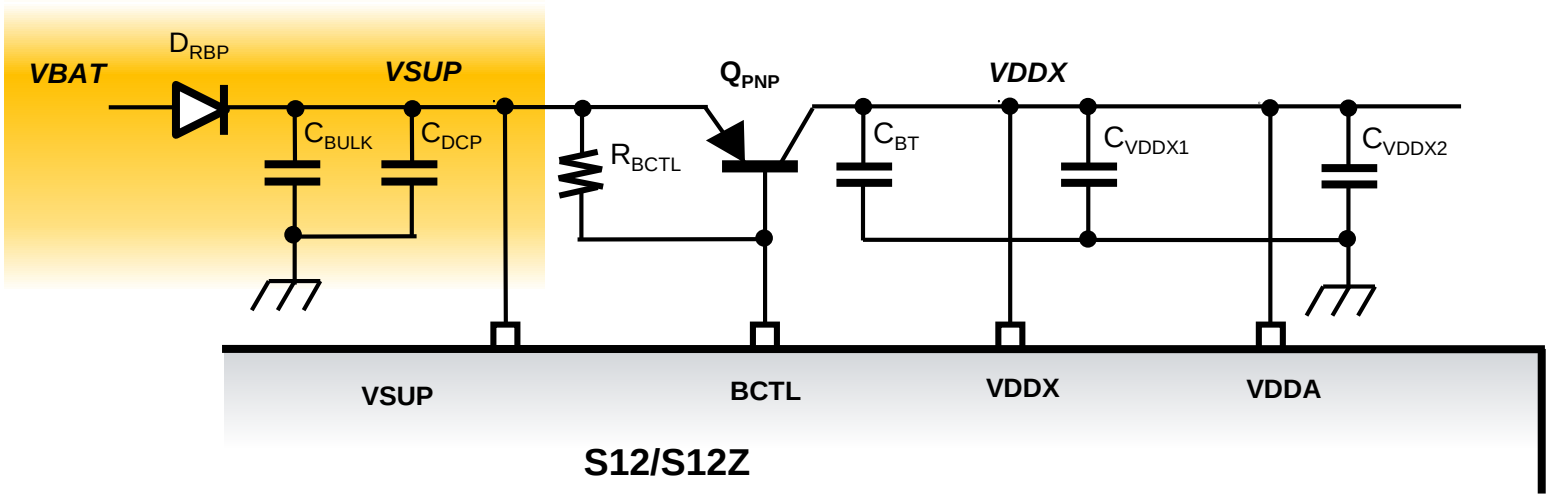
High Level Functional Application



Power Supply Pins

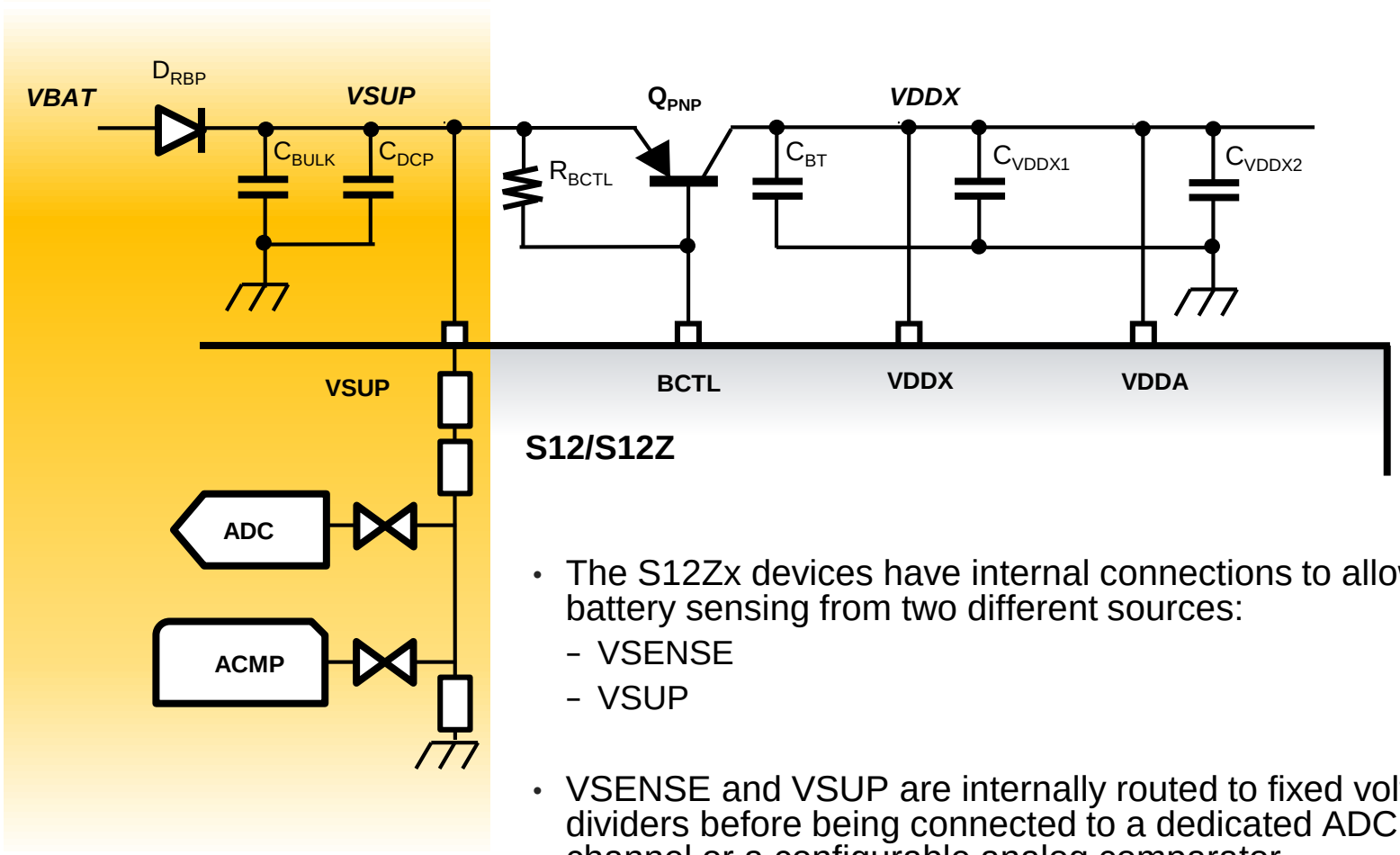
Battery sensing
PNP Ballast Transistor
Decoupling Capacitors

Power supply pins



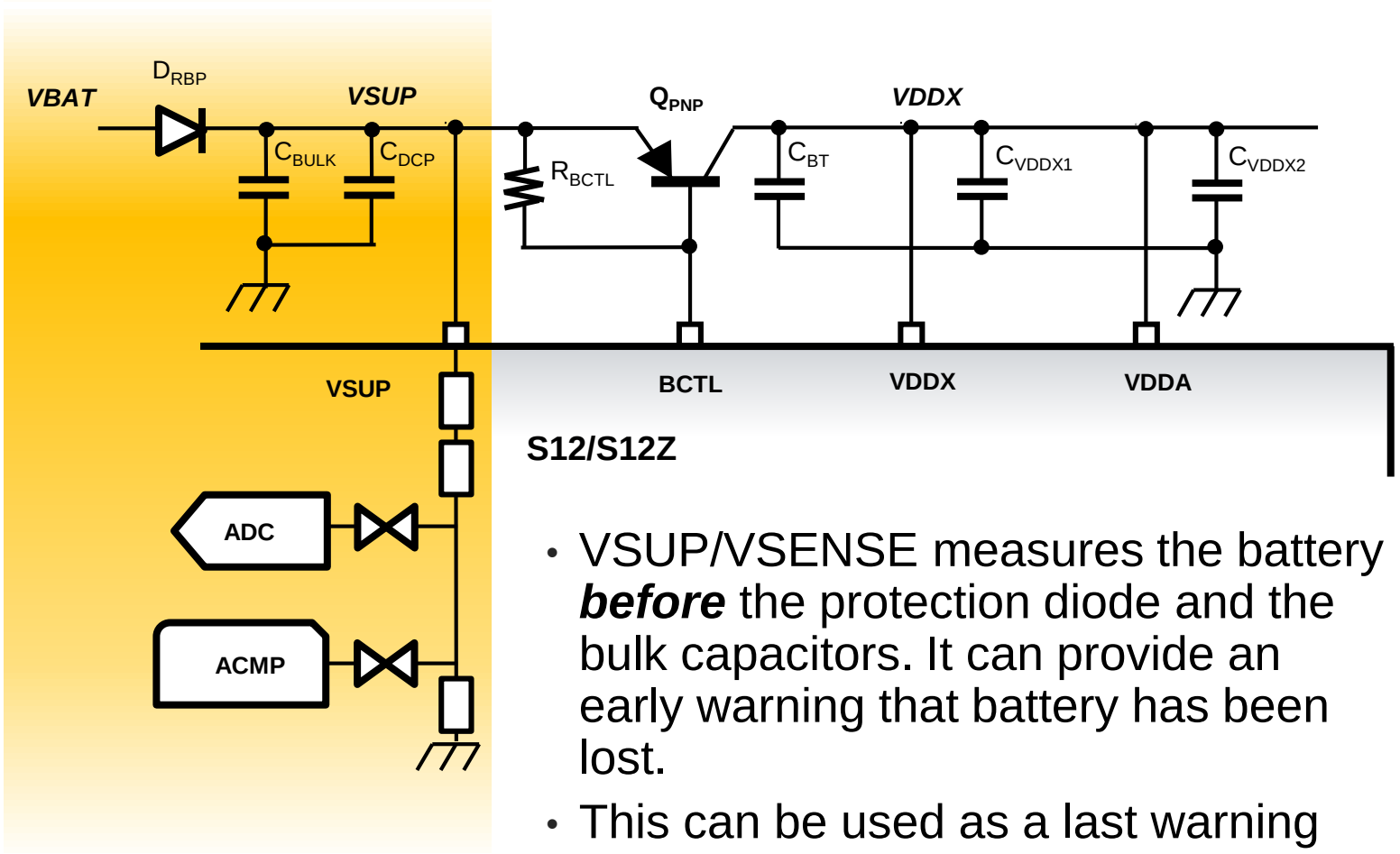
- VSUP is the 12V supply voltage pin for the on chip voltage regulator. This is the voltage supply input from which the voltage regulator generates the on chip voltage supplies.
- It must be protected externally against a reverse battery connection. The simplest protection against reverse battery protection is a diode in series with the battery.

Battery sensing



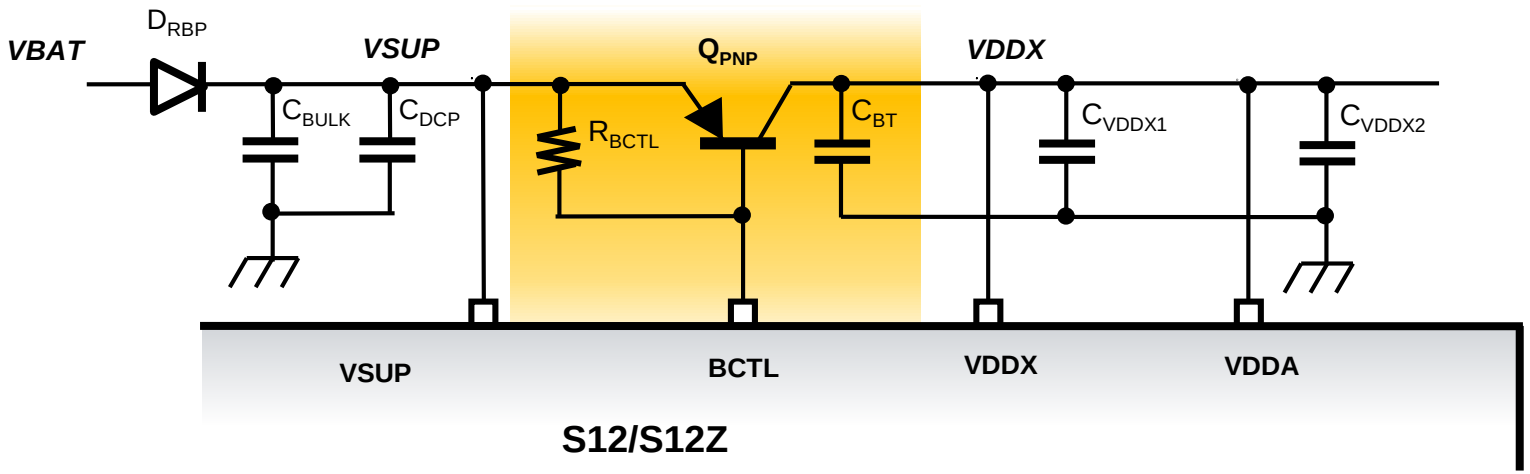
- The S12Zx devices have internal connections to allow battery sensing from two different sources:
  - VSENSE
  - VSUP
- VSENSE and VSUP are internally routed to fixed voltage dividers before being connected to a dedicated ADC channel or a configurable analog comparator.

Battery sensing



- VSUP/VSENSE measures the battery ***before*** the protection diode and the bulk capacitors. It can provide an early warning that battery has been lost.
- This can be used as a last warning that power is failing or ignition status.

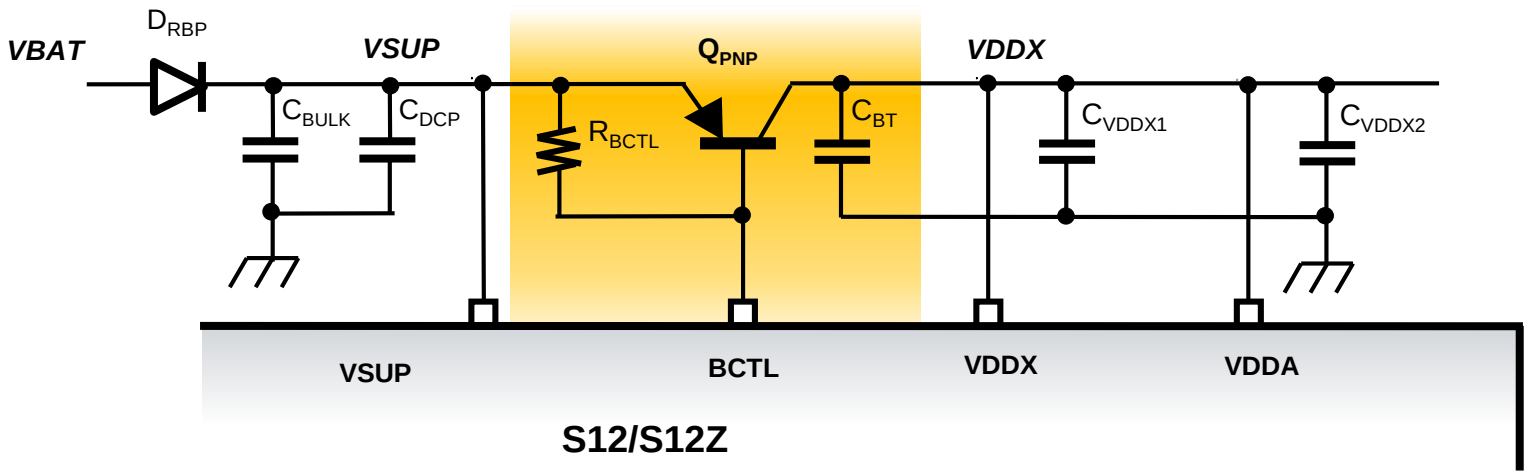
VDDX Ballast transistor



- The external ballast device function extends current capability and reduces internal power dissipation.

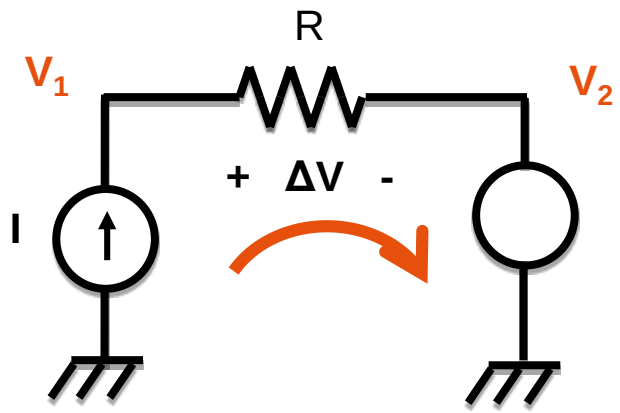
- **BCTL** - Base Control Pin for external PNP: BCTL is the ballast connection for the on chip voltage regulator. It provides the base current of an external BJT (PNP) of the VDDX and VDDA supplies. An additional 1 KΩ resistor between emitter and base of the BJT is required

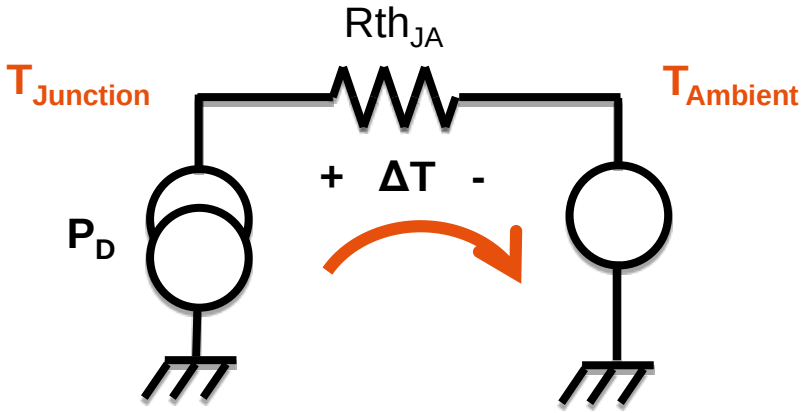
VDDX Ballast transistor



- The maximum output current capability [I_{VDDX}] using a PNP External Ballast transistor [Q_{PNP}], must be determined by the allowed maximum power of the device. The designer should to consider that the maximum power dissipation of the transistor will depend mainly on the following factors:
  - Package type
  - Dissipation mounting pad area on the PCB
  - Ambient temperature

Electrical vs. Thermal DC Parameters





$\Delta V = (V_1 - V_2) = I * R$

$\Delta T = (T_J - T_{AMB}) = P_D * R_{TH}$

R = Electrical Resistance (Ω)
V = Potential Difference (V)
I = Current (A)

R_{th} = Thermal Resistance (C/W)
ΔT = Temperature Difference (C)
P_D = Power Dissipated (W)

$$\mathbf{PWR_{MAX}} = \frac{\mathbf{TJ_{MAX}} - \mathbf{T_{AMB}}}{\mathbf{Rth_{JA}}}$$

Power supply pins

6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air					
	BCP53		[1]	-	-	192	K/W
			[2]	-	-	125	K/W
			[3]	-	-	93	K/W
	BCX53		[1]	-	-	250	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm^2.

[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm^2.

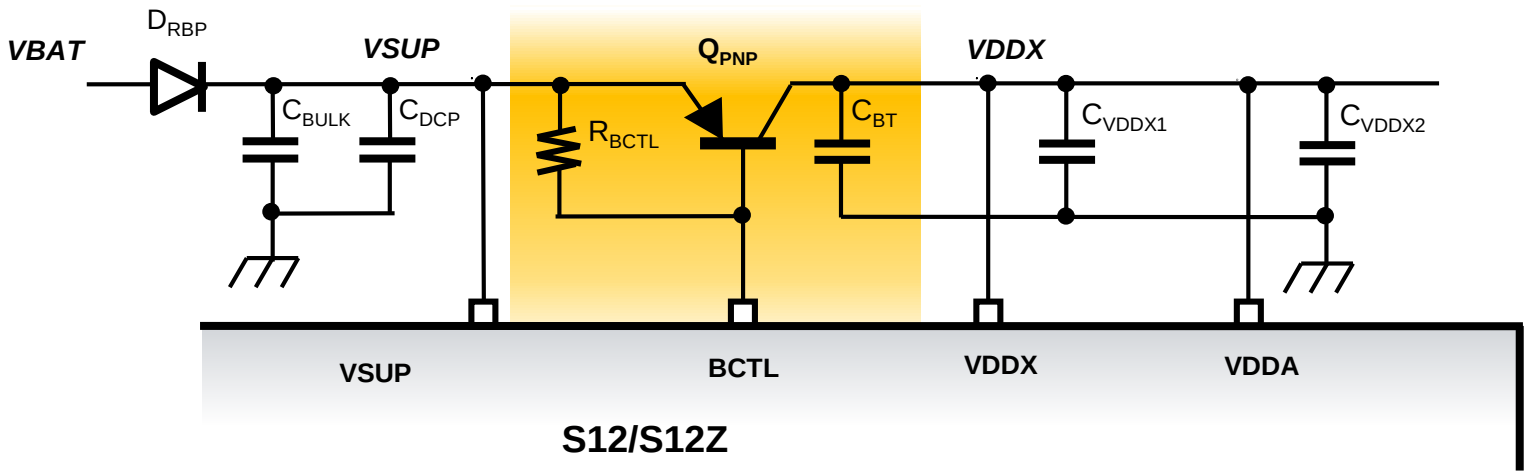
[4] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.

[5] Device mounted on an FR4 PCB, 4-layer copper, tin-plated, mounting pad for collector 1 cm^2

$$PWR_{MAX} = \frac{TJ_{MAX} - T_{AMB}}{Rth_{JA}}$$

PWR_{MAX} - Maximum power dissipation allowed.
TJMAX – Maximum junction temperatura
T_{AMB} – Ambient Temperature
Rth_{JA} – Thermal Resistance Junction to ambient

Power supply pins



- **VBAT** = 12V
- **VFWD** = 0.7V
- **VSUP** = VBAT - VFWD = 11.3V
- **VDDX** = 5V
- **TJ** = +150 °C
- **TAMB** = +25°C
- **RthJA** = 125 K/W

$$PWR_{PNP} = \frac{\mathrm{TJ_{MAX}} - \mathrm{T_{AMB}}}{\mathrm{Rth_{JA}}} = \frac{(+150°\mathrm{C}) - (+25°\mathrm{C})}{125\,{}^{K}/_{W}}$$

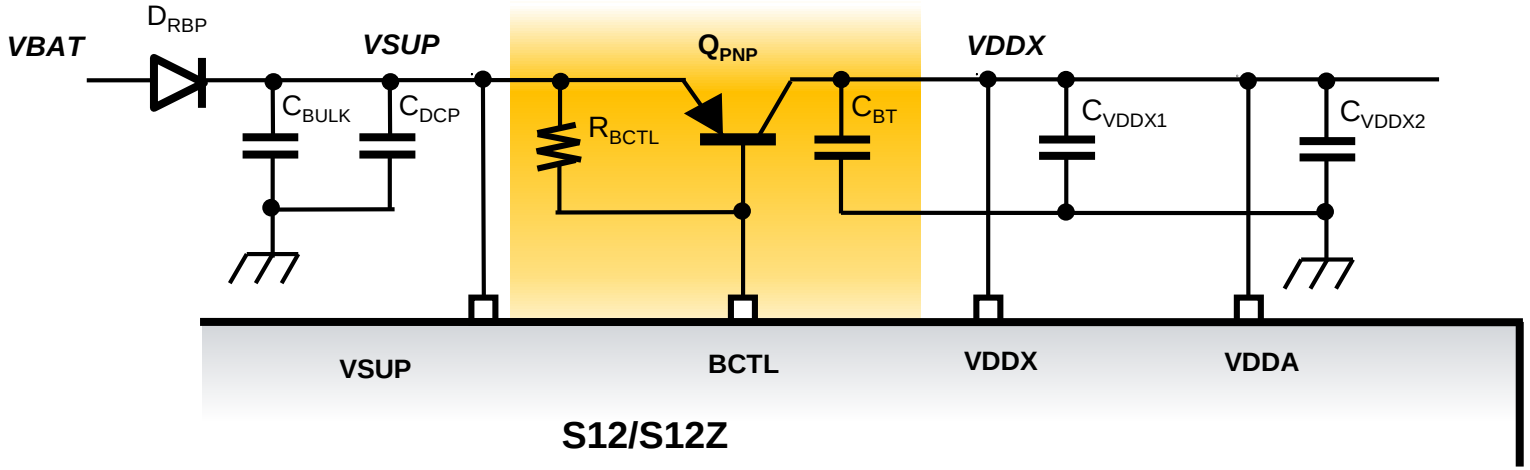
$$PWR_{PNP} = 1W$$

$$I\_VREG_{\mathrm{OUT}} = \frac{PWR_{PNP}}{VSUP - VDDX} = \frac{1W}{12V - 5V} = 142.85mA$$

$$I\_VREG_{\mathrm{OUT}} = 142.85mA$$

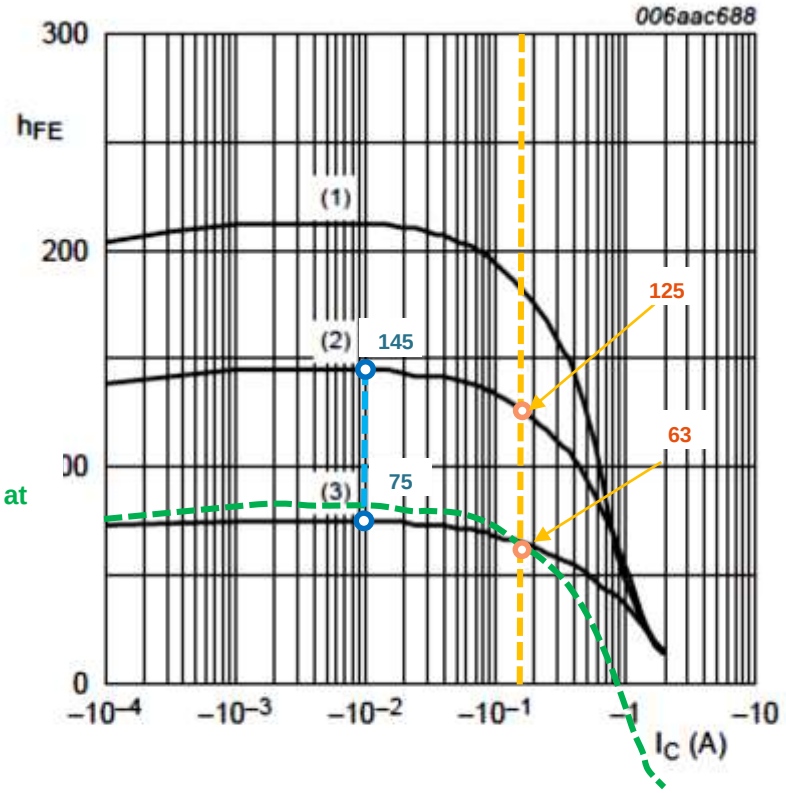
http://www.endmemo.com/convert/thermal%20resistance.php

Power supply pins



- Transistor specifications give the minimum and maximum gain.
- The worst case is usually significantly lower than the nominal figure on the transistor datasheet cover page. Furthermore, the datasheet values are usually given at room temperature (+25 °C).
- The required gain should be calculated at cold temperature, because a PNP/NPN transistor has minimum gain at low temperature.
- The worst case gain at cold temperature can be obtained from the transistor supplier or can be estimated using the graphs given in the transistor datasheet.

Power supply pins



Estimated minimum beta curve at +25°C

V_{CE} = −2 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −55 °C

Quick reference data ...continued

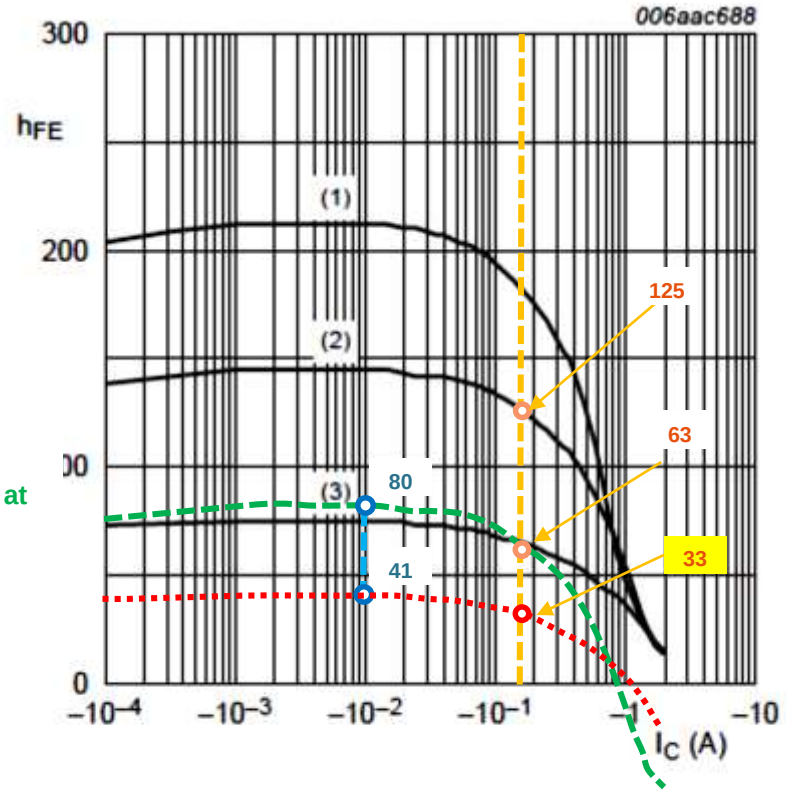
Parameter	Conditions	Min	Typ	Max	Unit
DC current gain	V_{CE} = −2 V; I_C = −150 mA	63	-	250	
h_{FE} selection -10	V_{CE} = −2 V; I_C = −150 mA	63	-	160	
h_{FE} selection -16	V_{CE} = −2 V; I_C = −150 mA	100	-	250	

Step1:
Estimate the minimum beta curve at 150mA +25C
Minimum beta is 63 at 150mA, 25C

Step 2:
Determine temperature coefficient of beta at 10mA from data sheet.

$$= \frac{100\% \times \frac{(145-75)}{145}}{+25°C-(-55°C)} = \frac{48.275}{80} = 0.60\,\%/°C$$

Power supply pins



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h_{FE} selection -16	V_{CE} = −2 V; I_C = −150 mA	100	-	250	

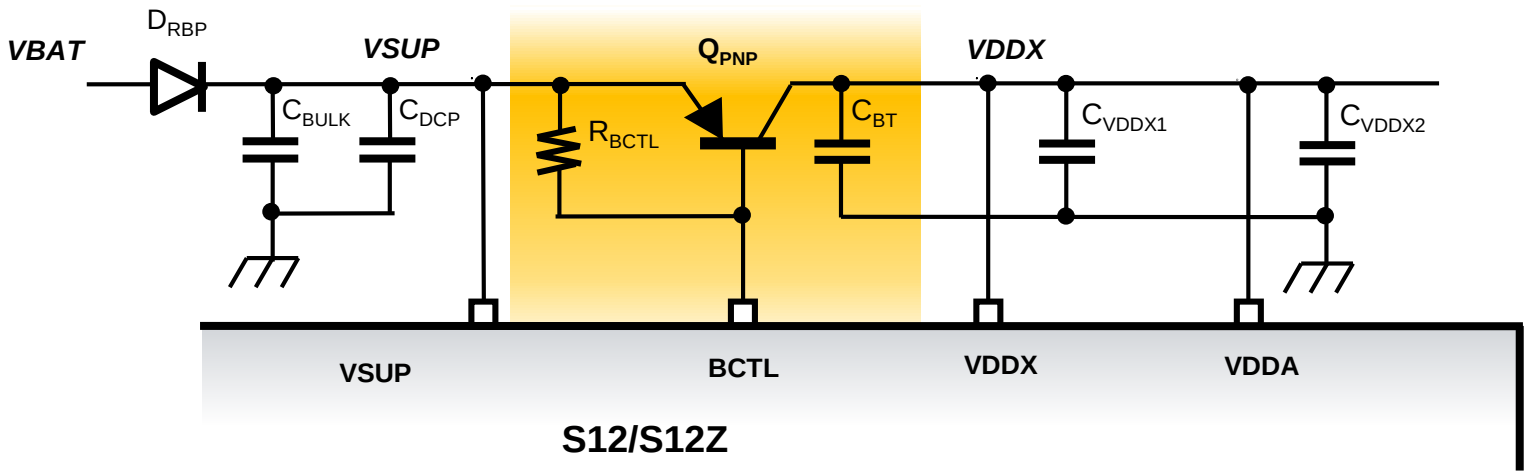
Minimum Beta at -40°C @ 10mA

$$= 80 - (0.60\,\%/{}^{\circ}C * (+25°C - (-40°C)))$$

$$= 80 - (0.60\,\%/{}^{\circ}C * (+60°C) = 33$$

Then we can estimate the minimum beta @150mA, **~33**

Power supply pins

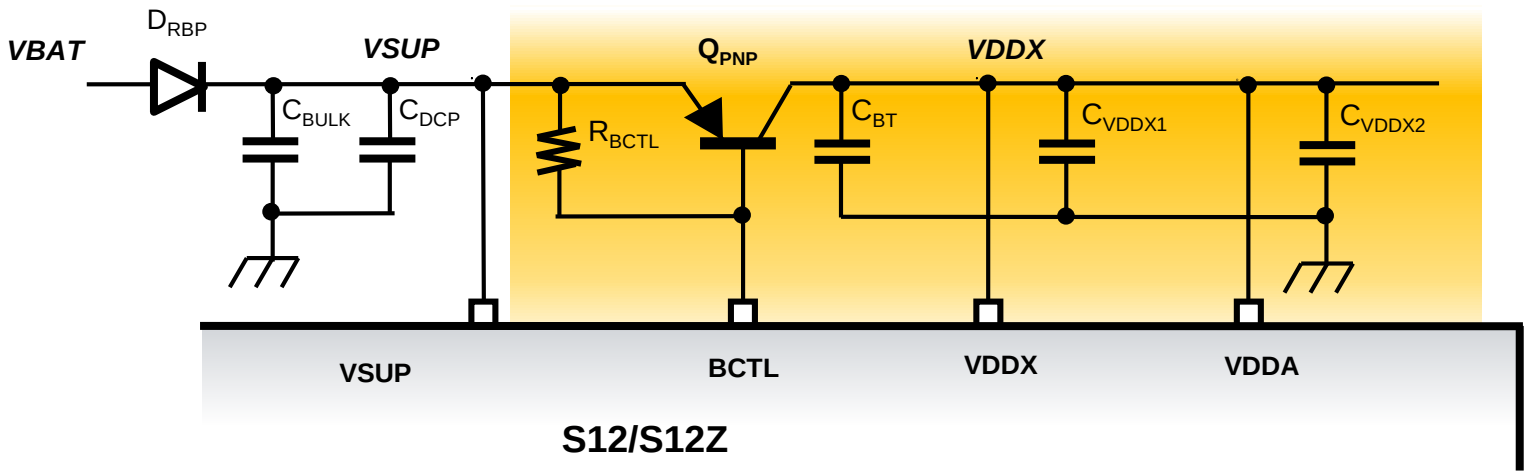


S12/S12Z

Part Number	Package Type	Manufacturer
BCP53	SOT- 223	ONSEMI
		NXP
		FAIRCHILD
2SB1260 / 2SB1181	SOT-89	ROHM
	DPAK	
2SA1952	DPAK	ROHM
2SB1181 TBV	SOT-89	ROHM
	DPAK	

- Develop a Static Thermal Analysis, and select the appropriate package.
- VCEO parameter acording to the customer requirments.
- Avoid transistors with super betas or >500.
- Make sure worst case hFE at low temperature remains above 30 to avoid the quasi-saturation or saturation condition.

Power supply pins

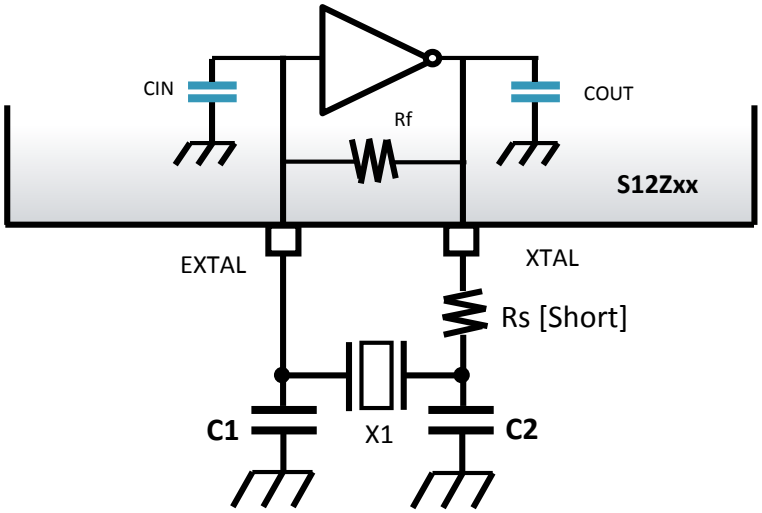


Symbol	Characteristic	Value
R_{BCTL}	Metal Film resistor	1 kΩ
C_{BCTL}	X7R Ceramic or Tantalum	10 uF
C_{VDDX1}	X7R Ceramic	220 nF
C_{VDDX2}	X7R Ceramic	220 nF

External and Internal RC Oscillator

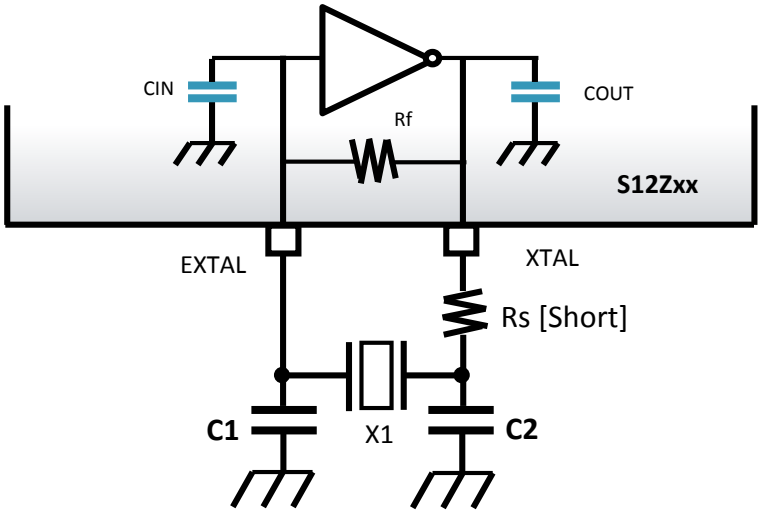
External and Internal RC Oscillator

- The S12Z devices have an internal 1 MHz internal RC oscillator with +/- 1.3% accuracy over rated temperature range.
- There is an alternative to add an external resonator or crystal, for higher and tighter tolerance frequencies.
- Oscillator pins shared with GPIO functionality
- The oscillation mode is selectable by software.



External and Internal RC Oscillator

- The effective load capacitance, CLOAD, appears to the crystal circuit as the series combination of C1 and C2. Correct CLOAD is important for proper operating frequency. Crystals are available with a variety of CLOAD values.
- It is recommended to select a fundamental mode parallel resonant type crystal having a C_{LOAD} of around 12 pF and ESR of 30 to 60 Ω.
- The actual discrete values required for C1 and C2 are generally up to 12 pf below the calculated load capacitance due to PCB traces and the input pin's stray capacitances; the board layout is quite important.



External and Internal RC Oscillator

The following formula may be used to calculate a parallel resonant crystal's external load capacitors:

$C_{LOAD} = ((C_1 \times C_2) / (C_1 + C_2)) + C_{STRAY}$

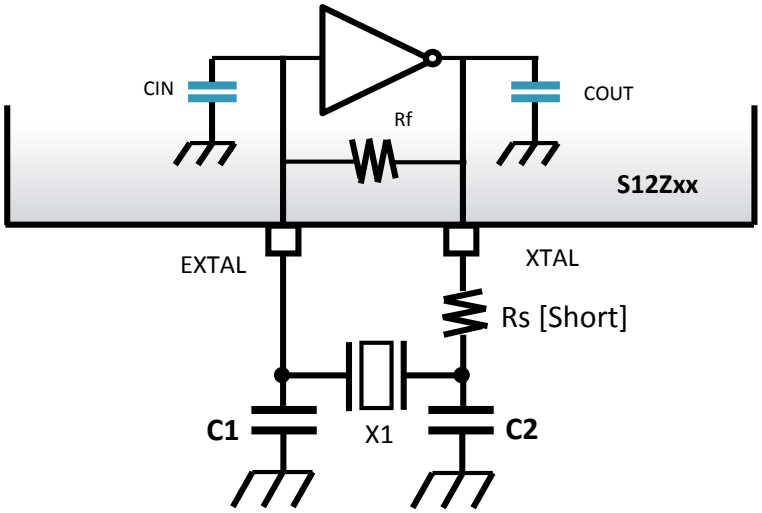
Where:
CL = the crystal load capacitance
Cstray = the stray capacitance in the oscillator circuit,

Which will normally be in the 2pF to 5pF range. Assuming that $C_1 = C_2$ then the equation becomes:

$C_{LOAD} = ((C_1 \times C_1) / (2 \times C_1)) + C_{STRAY}$
$C_{LOAD} = (C_1 / 2) + C_{STRAY}$

Rearranging the equation, we can find the external load capacitor value:

$C_{1,2} = 2(C_{LOAD} - Cstray)$

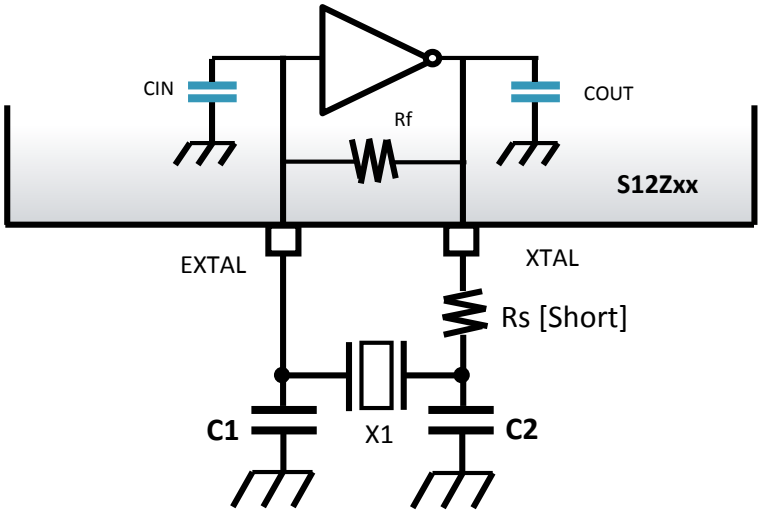


External and Internal RC Oscillator

For example, if the crystal load capacitance is 8pF, and assuming Cstray=3pF, then:

C1 = C2 = 2(8pF - 3pF) = 10pF

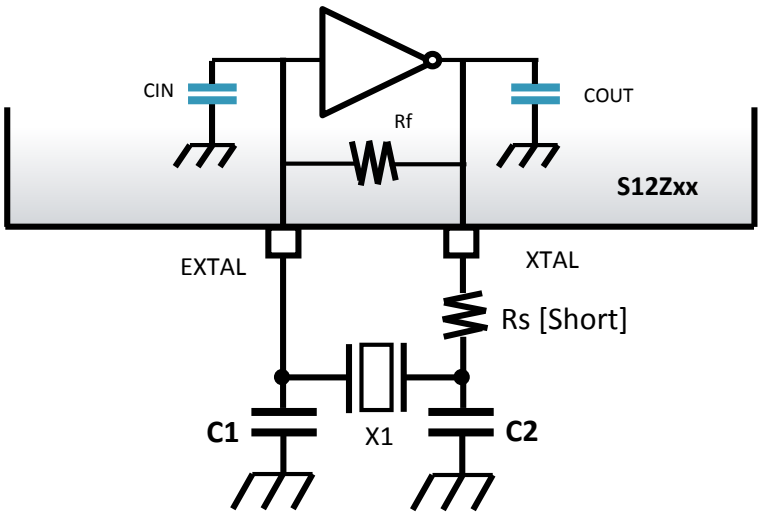
It is difficult to know exactly what the stray capacitance is, but if you find the oscillation frequency is too high, the load capacitor values can be increased. If the frequency is too low, the load capacitors can be decreased.



External and Internal RC Oscillator

- Resistance **Rs** is necessary for the prevention of abnormal oscillation.
- Install Resistance **Rs** on to the output side after checking the IC terminal function.
- Use the shortest distance for lines connecting parts, including ground lines, in order to prevent the inclusion of unnecessary stray capacitance.
- Do not allow any part of the oscillation circuit to cross over a signal line of any other circuit on the same circuit board.
- Normally, C1 and C2 should be **C0G / NP0** type ceramic capacitors for the best tolerance and temperature stability.

- NOTE: All quartz crystal oscillator and ceramic resonator circuits should be characterized by the supplier to make sure the oscillator/resonator is optimized to the particular IC, and that the required accuracy is achieved.



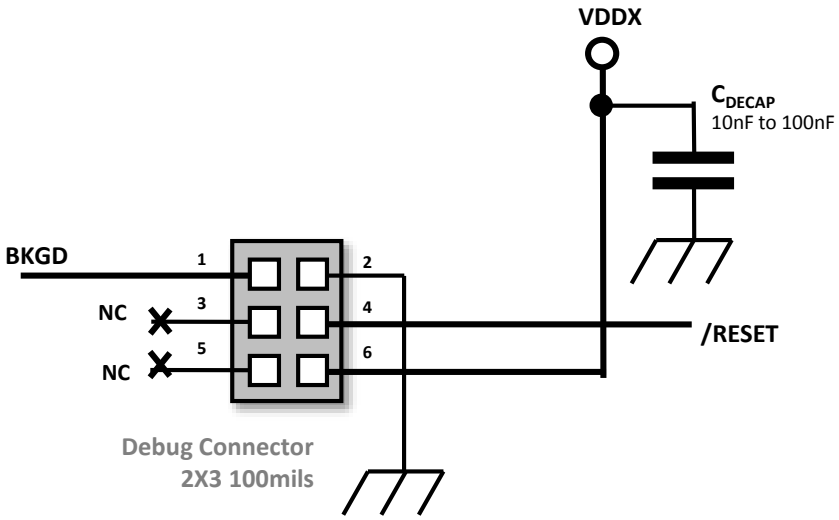
Programming Interface

BKGD pin

Reset pin

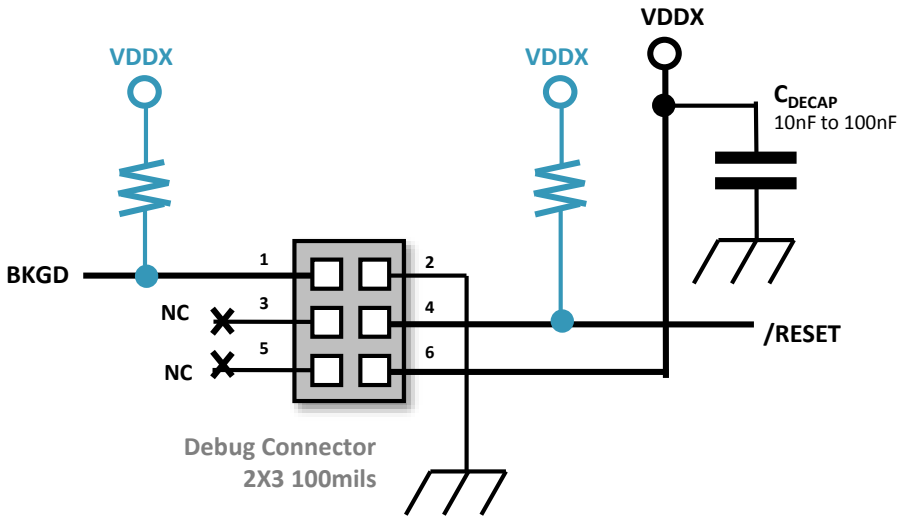
Programming Circuit

- The S12/S12Z family is programmed via the BDM protocol.
- The BDM protocol is a serial communication that is transmitted through the BKGD line.
- The standard BDM connector is a 2 by 3 pin header with 100 mil pitch.
- The BDM connector requires connection to the
  - **BKGD pin**
  - **RESET pin**
  - **VDDX Voltage**
  - **GND.**



Programming Circuit

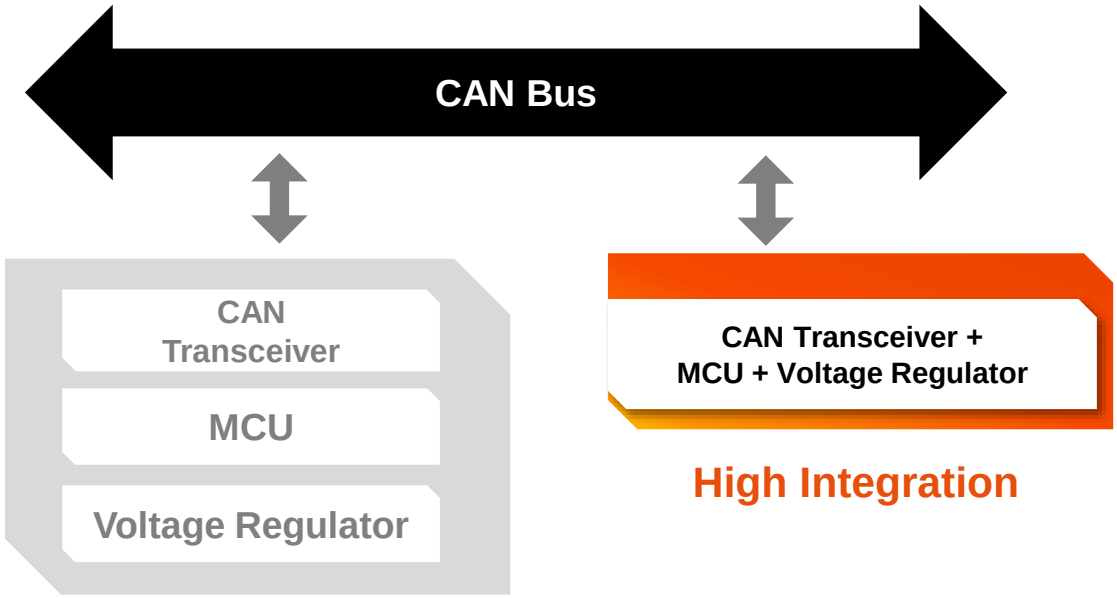
- It is recommended to add a ceramic capacitor to VDDX near the connector to reduce noise that could be injected by the programming circuitry to the power supply.
- The BKGD signal is used as a pseudo-open-drain signal for the background debug communication. **The BKGD pin has an internal pull-up device.**
- The RESET signal is an active low bidirectional control signal. It acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset. **The RESET pin has an internal pull-up device.**



CAN Interface

Hardware Design Guidelines for MagniV Mixed-Signal MCUs

CAN Physical Layer

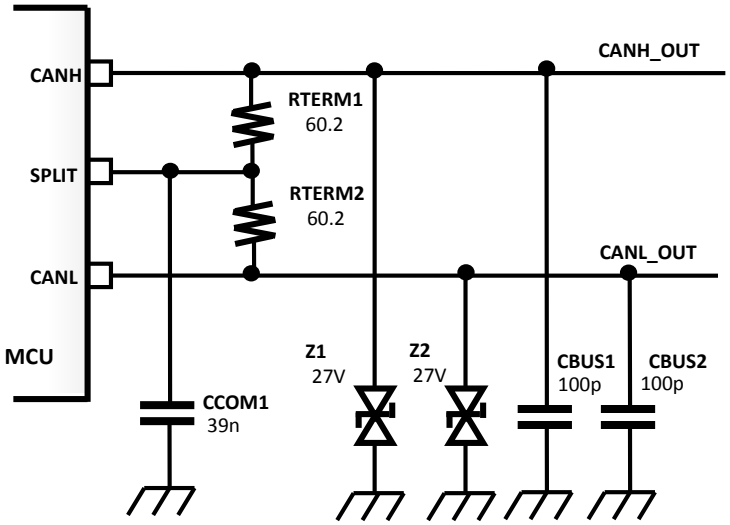


- Freescale offers a complete line of products to meet the needs of high-performance CAN embedded applications.

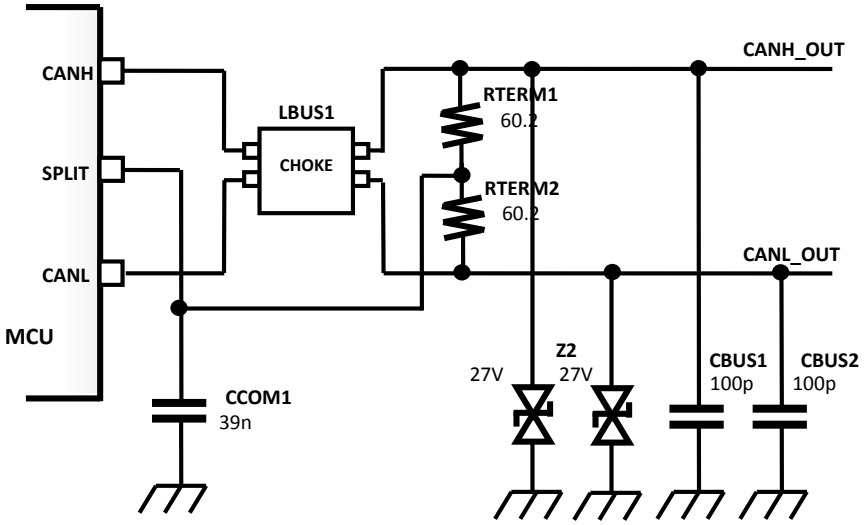
- MagniV MCUs as **S12ZVC** has an **on-chip** CAN physical transceiver and a dedicated power supply using an external ballast transistor for its. Having these modules on-chip helps reduce the total amount of components required to implement CAN communication.

CAN Physical Layer

- As any other CAN physical transceiver, the CANH, CANL and SPLIT pins are available for the designer to terminate bus depending on the application the next Figure 13 1 - CAN Physical transceiver circuit. and Figure 13 2 - CAN Physical transceiver circuit with common mode choke. show an example of a CAN node termination.

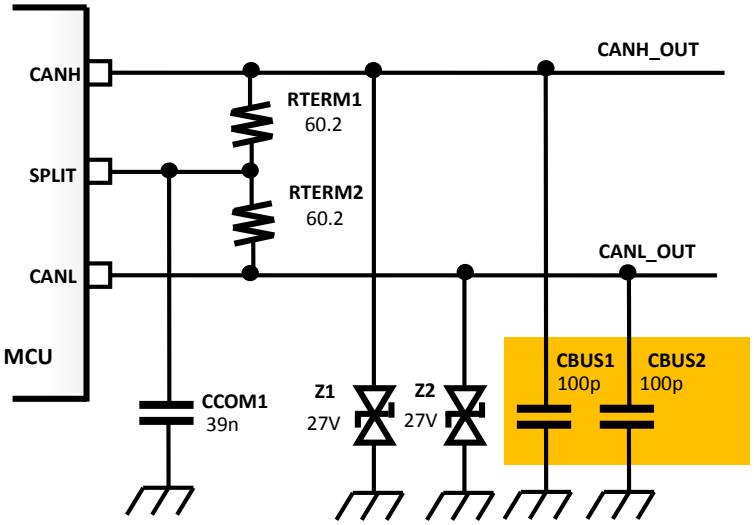


CAN Physical transceiver circuit.



CAN Physical transceiver circuit with common mode choke.

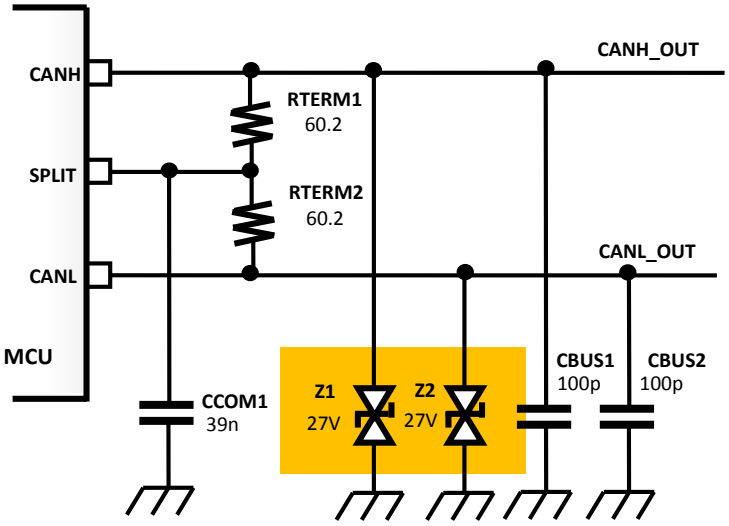
CAN Physical Layer



CAN Physical transceiver circuit.

Reference	Description
CBUS1 and CBUS2	The Capacitors CBUS1 and CBUS2 are not specifically required. They may be added for EMC reasons, in which case the maximum capacitance from either bus wire to ground must not exceed 300pF total. If zener stacks are also needed, the parasitic capacitance of the zener stacks must also be included in the total capacitance budget.
Z1 and Z2	The zener stacks Z1 and Z2 could be required to satisfy Automotive EMC requirements (ESD in particular). These devices should be placed close to the connector.

CAN Physical Layer



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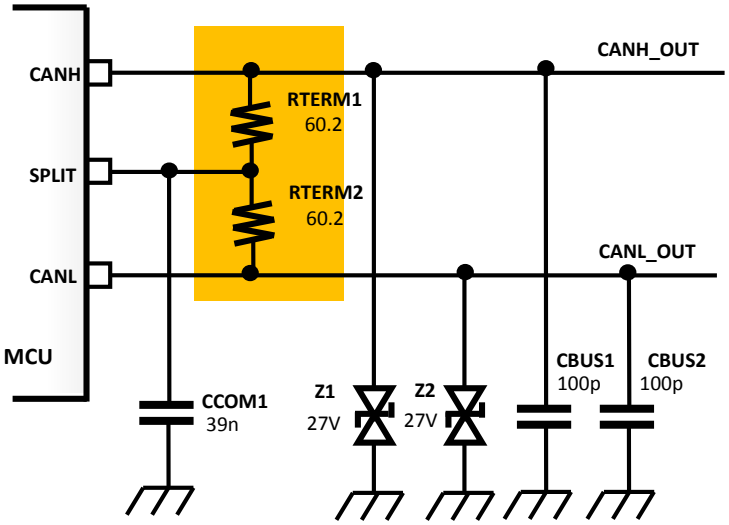
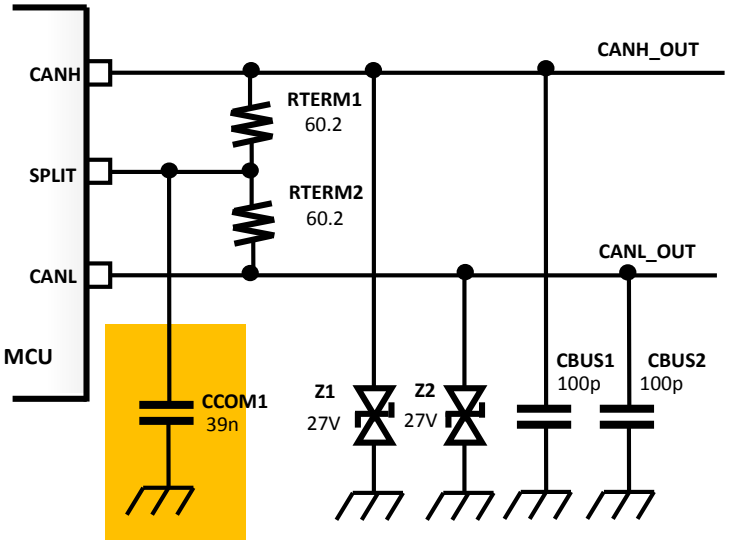


CAN Physical transceiver circuit.

Reference	Description
RTERM1 and RTERM2	Depending on the position of the node within the CAN network it might need a specific termination. $R_{TERM1,}$ R_{TERM2} and C_{COM1} must be that they assist in having an overall cable impedance. On a bus implementation of a CAN network only the two nodes on the two ends of the bus have terminator resistors. The nodes not placed on the end of the CAN bus do not have termination. A thorough analysis is required to maintain this requirement of the CAN networks.
CCOM1	The SPLIT pin on the transceiver is optional and the designer might choose not to use it. This pin helps stabilize the recessive state of the CAN bus and can be enabled or disabled by software when required.

CAN Physical Layer



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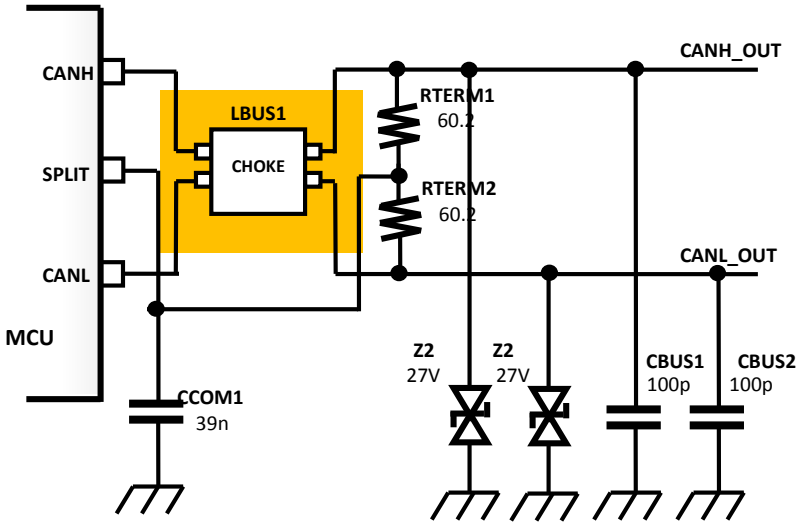
Reference	Description
RTERM1 and RTERM2	Depending on the position of the node within the CAN network it might need a specific termination. R_{TERM1}, R_{TERM2} and C_{COM1} must be that they assist in having an overall cable impedance. On a bus implementation of a CAN network only the two nodes on the two ends of the bus have terminator resistors. The nodes not placed on the end of the CAN bus do not have termination. A thorough analysis is required to maintain this requirement of the CAN networks.
CCOM1	The SPLIT pin on the transceiver is optional and the designer might choose not to use it. This pin helps stabilize the recessive state of the CAN bus and can be enabled or disabled by software when required.

CAN Physical Layer



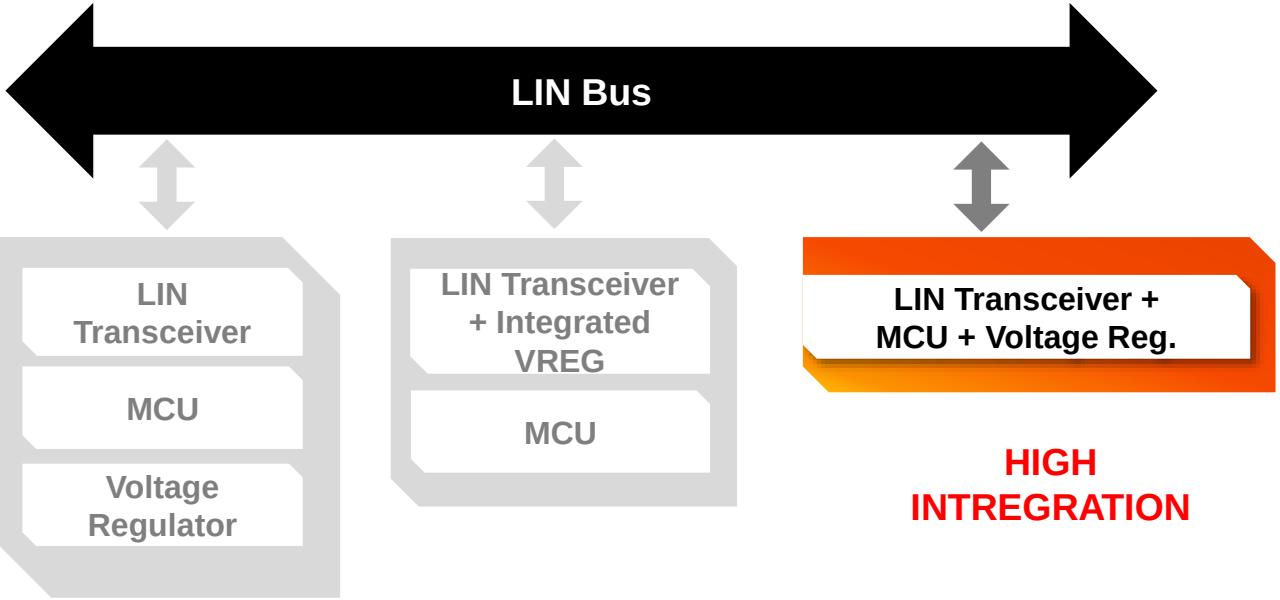
CAN Physical transceiver circuit with common mode choke.

Reference	Description
LBUS1 Common mode choke	A common node choke on the CANH and CANL lines can help reduce coupled electromagnetic interference and needed to satisfy Automotive EMC requirements. This choke, together with transient suppressors on the transceiver pins can greatly reduce coupled electromagnetic noise, and high-frequency transients.

LIN Interface

Hardware Design Guidelines for MagniV Mixed-Signal MCUs

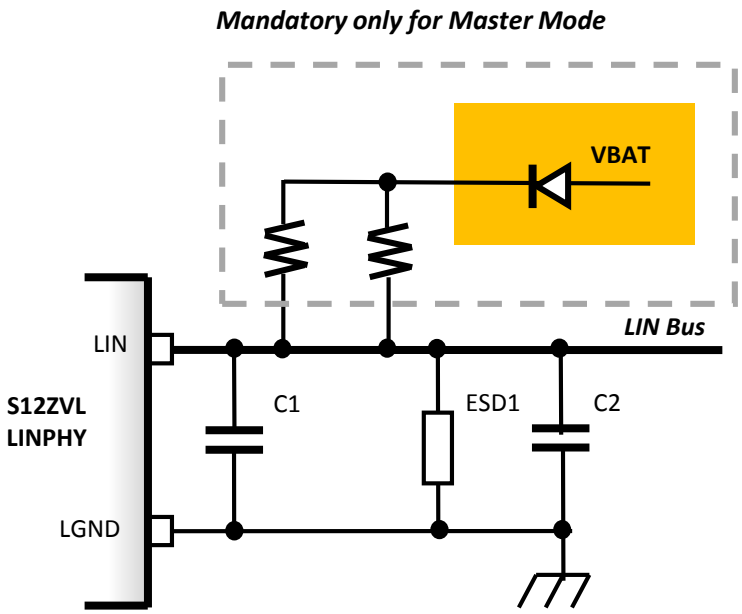
LIN Physical Layer



- Freescale offers a complete line of products to meet the needs of high-performance CAN embedded applications.

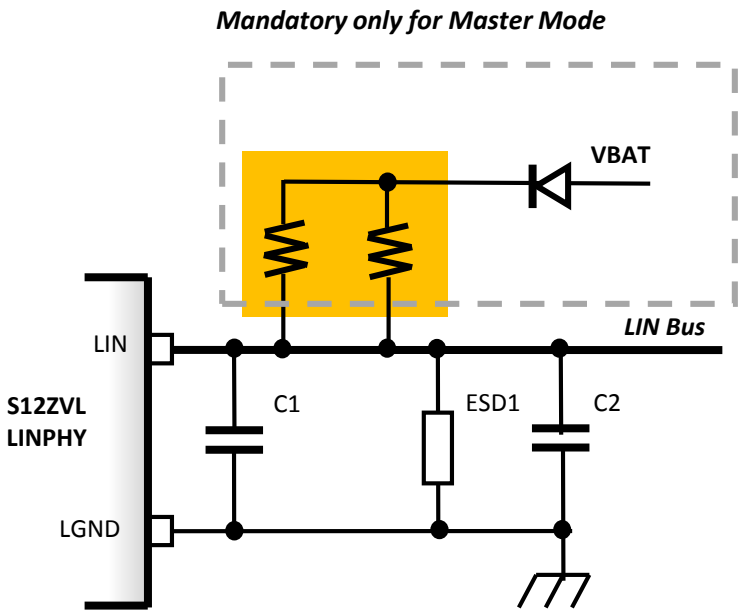
- MagniV MCUs as **S12ZVC** has an **on-chip** LIN physical transceiver and a dedicated power supply using an external ballast transistor for its. Having these modules on-chip helps reduce the total amount of components required to implement LIN communication.

LIN Interface



Reference	Part	Mounting	Remark
DMLIN	Diode	Mandatory only for master ECU	Reverse Polarity protection from LIN to VSUP.
RMLIN1 and RMLIN2	Resistor: 2kΩ Power Loss: 250mW Tolerance: 1% Package Size: 1206 Requirement: Min Power loss of the complete master termination has to be ≥ 500mW	Mandatory only for Master ECU	For Master ECU If more than 2 resistors are used in parallel, the values have to be chosen in a way that the overall resistance RM of 1kΩ and the minimum power loss of the complete master termination has to be fulfilled. For Slave ECU RMLIN1 and RMLIN2 are not needed on the PCB layout

LIN Interface



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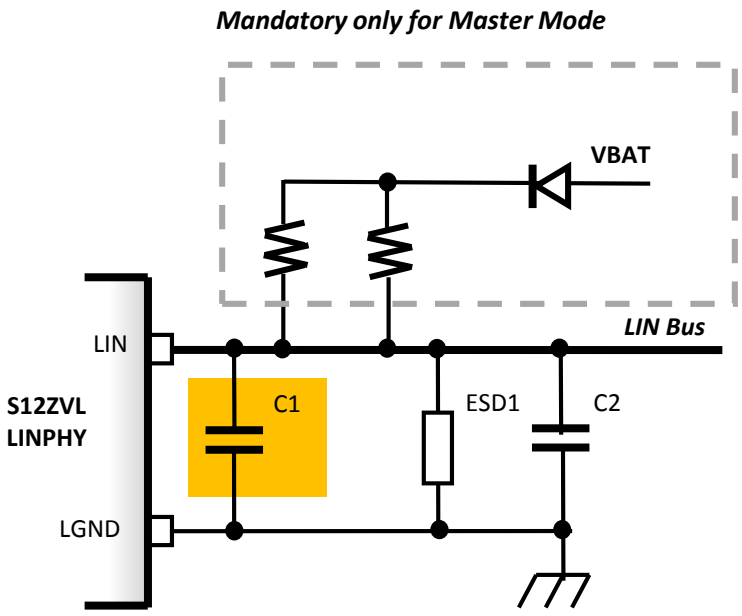
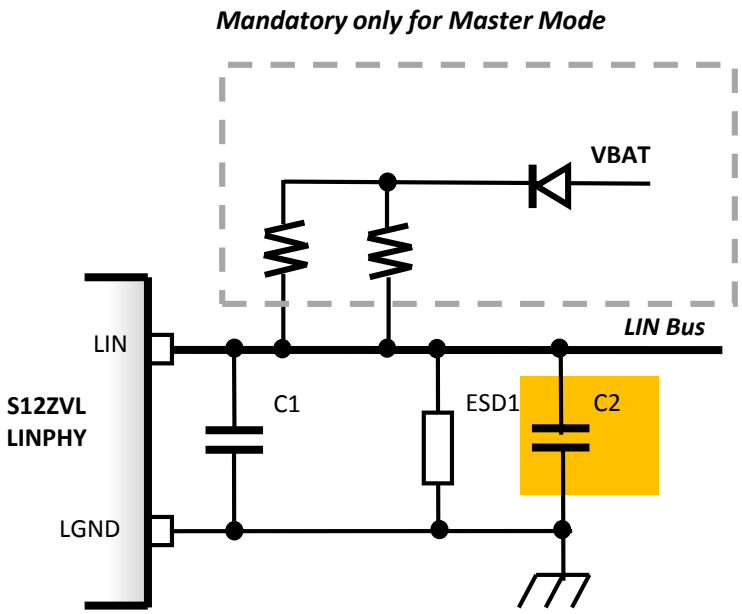
LIN Interface



Reference	Part	Mounting	Remark
C1	Capacitor: Master ECU: ≥560pF Slave ECU: 220pF Tolerance: 10% Package Size: 0805 Voltage: ≥50V	Mandatory	The value of the master node has to be chosen in a way that the LIN specification is fulfilled.
C2	Capacitor: Package Size: 0805	Optional	Mounting of the optional part only allowed if there is an explicit written permission of the respective OEM available. Placed close to the connector.

LIN Interface



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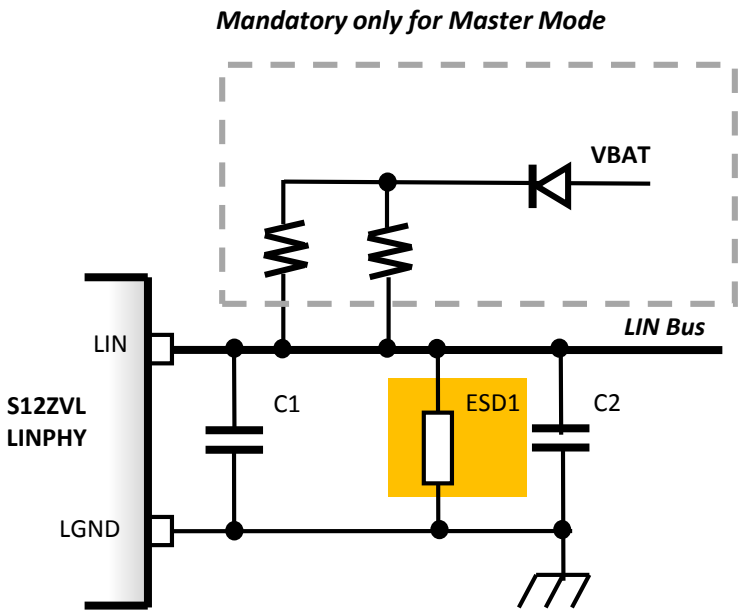
LIN Interface

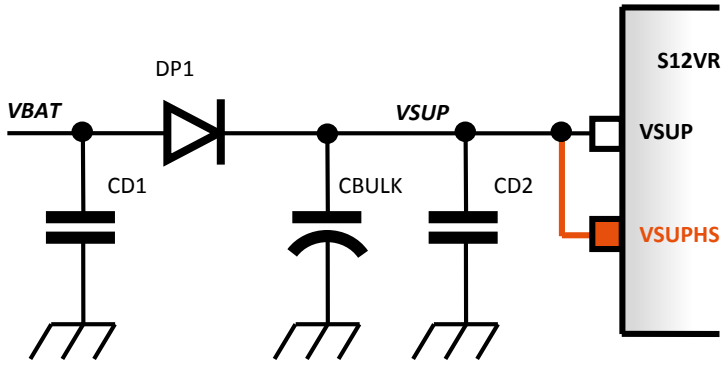


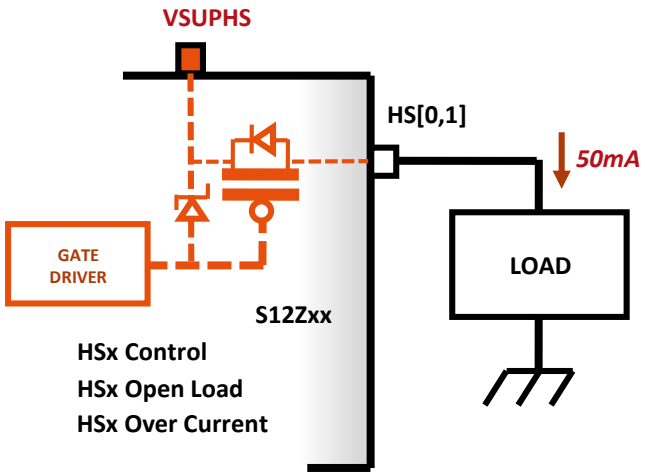
Reference	Part	Mounting	Remark
ESD	ESD Protection • Zener • MOV • TVS	Optional	Layout pad for an additional ESD protection part. Mounting of the optional part only allowed if there is an explicit written permission of the respective OEM available. Place close to the connector.

High Current / High Voltage Pins

High Side Drivers - HSDRV

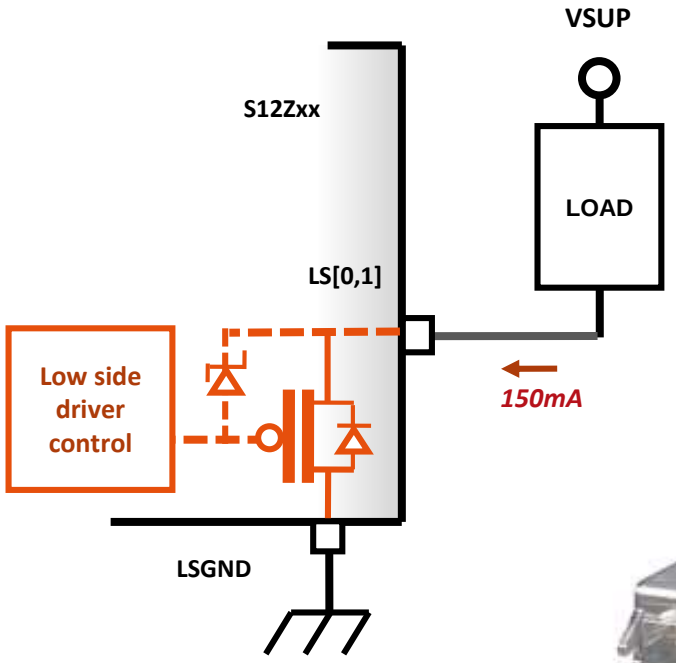
- The **HSDRV** module provides two high-side drivers. The nominal current for continuous operation to **50mA**. This value is valid for each HS-driver output.
- Both high-side drivers have a common high power supply **VSUPHS**. VSUPHS can support up to 18V.
- Selectable gate control of high-side switches:
  - HSDR[1:0] register bits,
  - PWM channel.
  - Timer channel.
- High-load resistance open-load detection when driver enabled and turned off.
- Over-current protection for the drivers, while they are enabled, including:
  - Interrupt flag generation.
  - Driver shutdown.

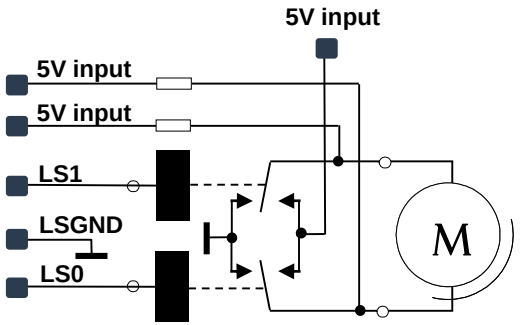




Low Side Drivers - LSDRV

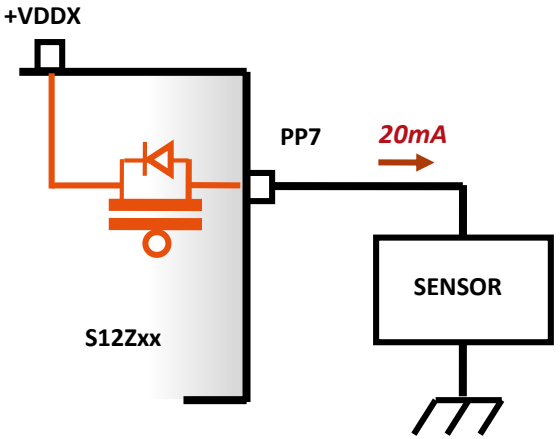
- The **LSDRV** module provides two low-side drivers typically used to drive inductive loads (relays).
- The **LSDRV** module includes two independent low side drivers with common current sink.
- Selectable gate control of low-side switches:
  - LSDRx register bits,
  - PWM channel
  - Timer channel.
- Open-load detection while enabled
  - While driver off:
  - selectable high-load resistance
  - open-load detection
- **Over-current protection** with shutdown and interrupt while enabled.
- **Active clamp to protect the device against over-voltage** when the power transistor that is driving an inductive load (relay) is turned off.



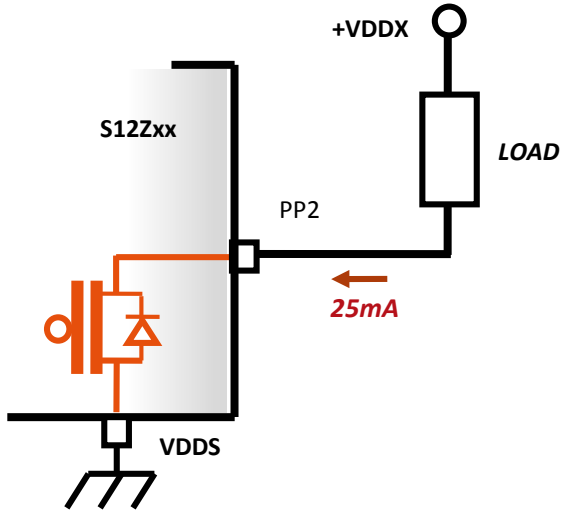


High Currents GPIOs

High-current capable high-side output with over-current interrupt



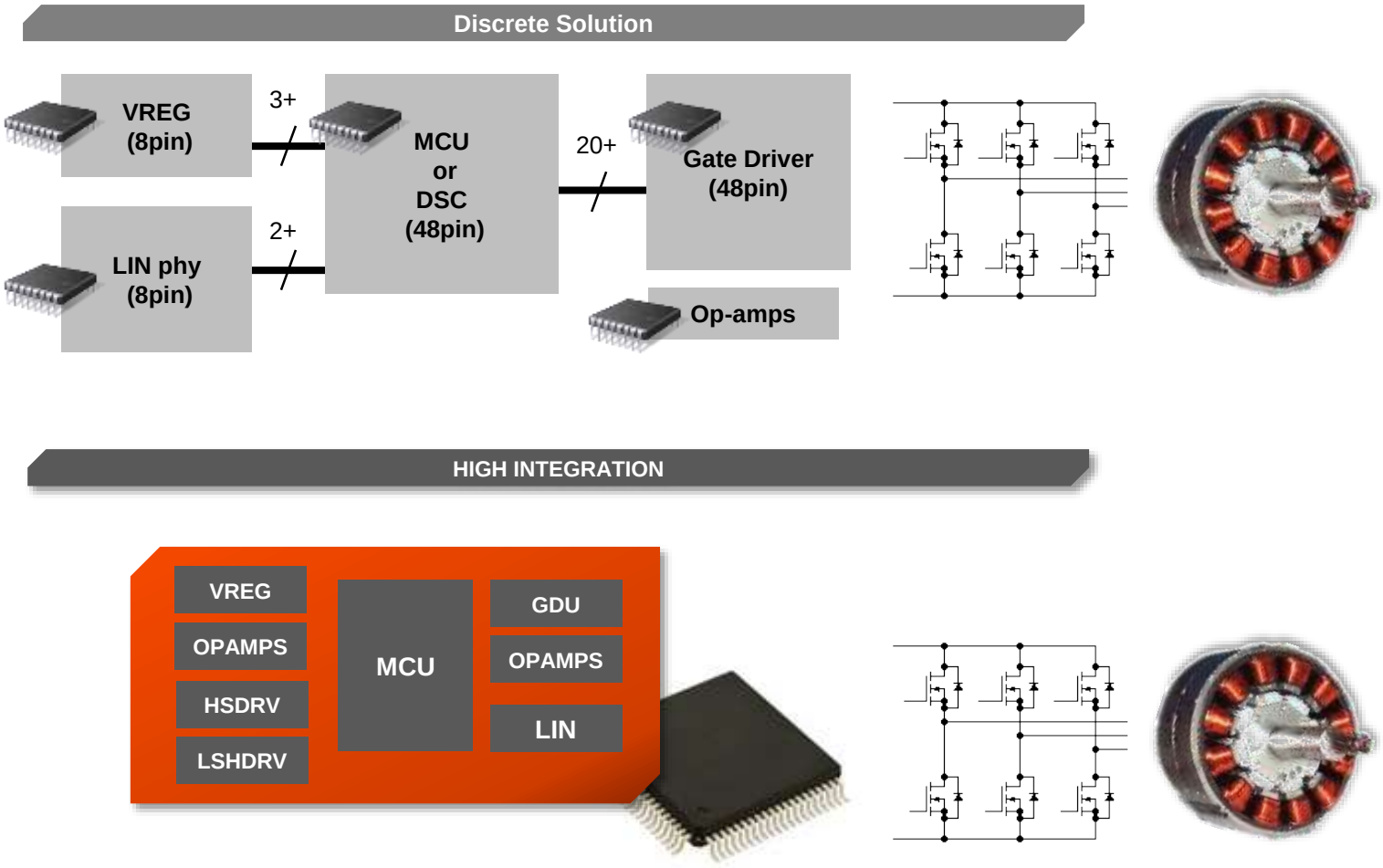
High-current capable low-side output with over-current interrupt



Motor Control Interface

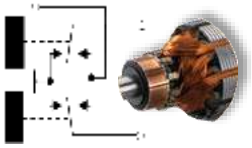
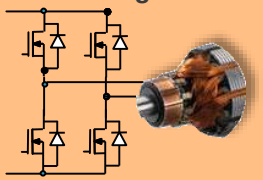
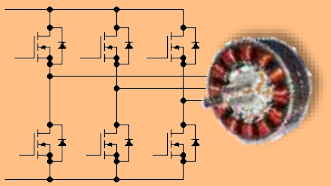
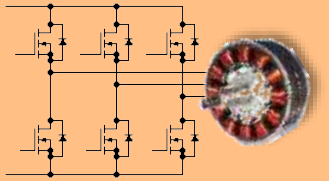
Power Mosfet’s
Gate driver unit
Bootstrap Capacitors
External charge pump
Active Reverse Polarity Protection
Current sensing

S12ZVM for BLC Motor Control

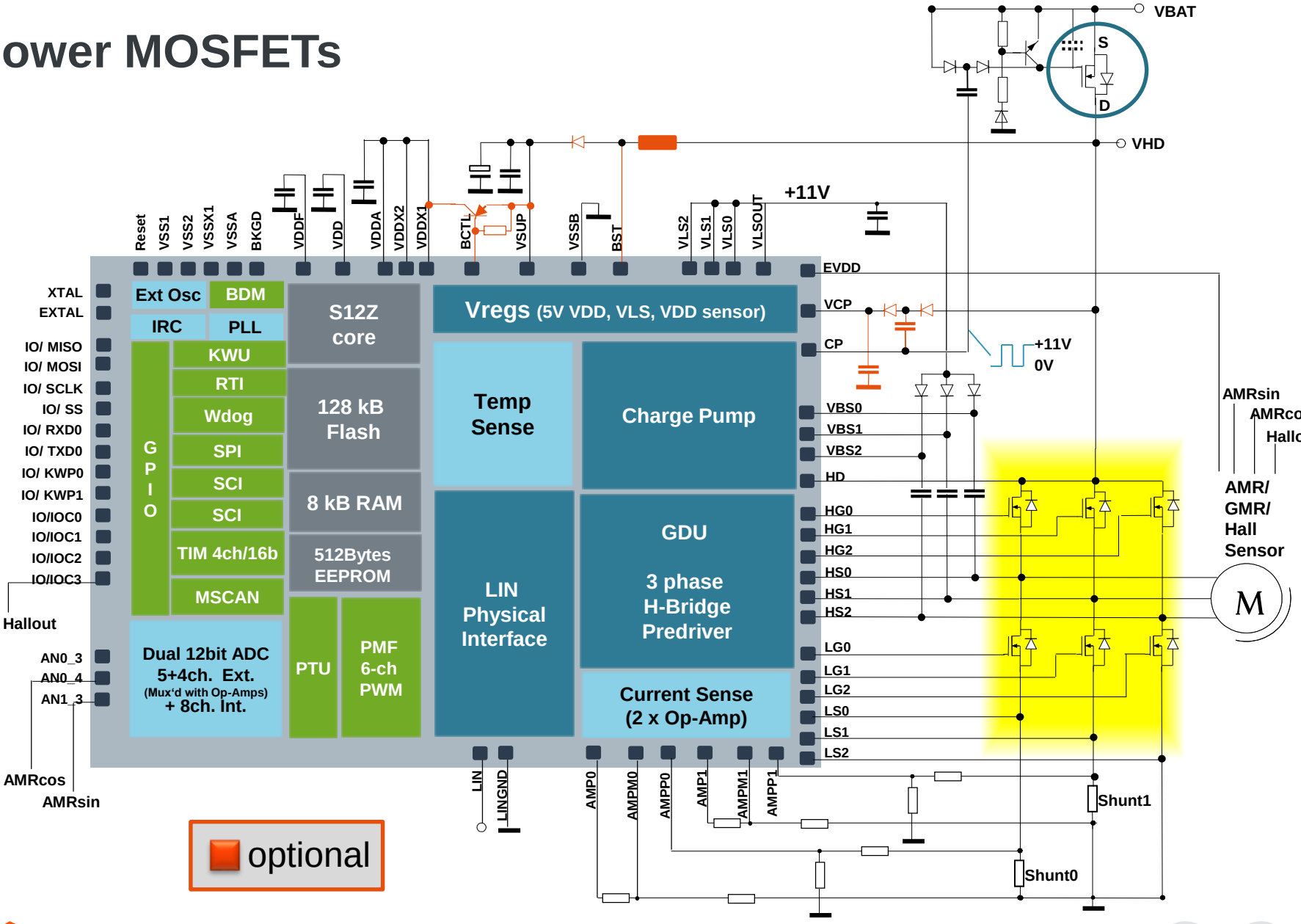


Motor categories

S12ZVM-target area

	Relay-driven DC-motors	*H-Bridge driven DC-motors*	*Brushless DC Motors (BLDC)*	*Permanent Magnet synchronous Motors (PMSM)*
Power Stage	**Relay** 	**H-Bridge** 	**3-phase** 	**3-phase** 
Mechanical construction	Permanent magnets placed on stator  Magnetic poles in rotor generated by current cunducted coil		Permanent magnets Placed on rotor  Current conducted coils in stator generate changing magnetic flux vector	
Commutation & Control Technique	Mechanical Commutation By brushes in the rotor		Electronic Commutation takes place in the stator 6-step / Block Commutation To produce trapezoidal Phase voltage	Sinusoidal / Vector control To produce Sinusoidal Phase voltage
Topology Advantage	Lowest cost	no mechanical component (reliability, electrification) No Relay noise PWM speed regulation	High Efficiency Power to weight ratio Reliability Noise	Best noise behavior High speed & precision Highest efficiency&torque Power to weight ratio

Power MOSFETs



optional

Drive strength versus Total Gate Charge

MOSFET‘s switching performance

Total Gate Charge Qg = minimum charge required to switch the device on.

$Qg = I * t$

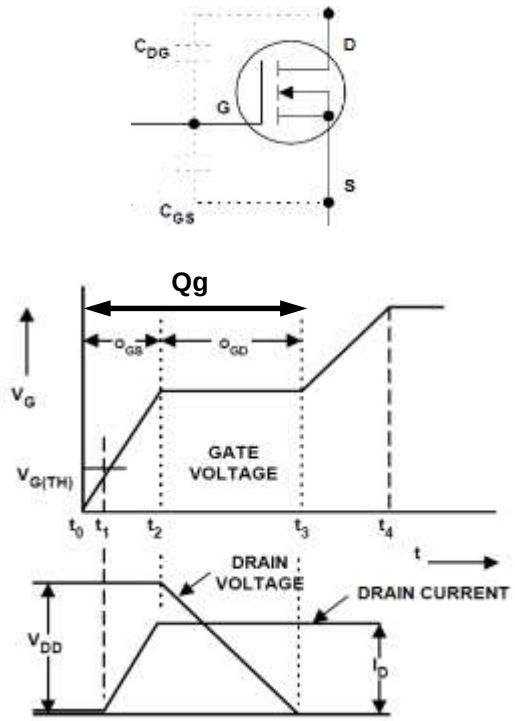
With I= gate current
t= time until internal caps charged

→ 100nC can be turned on in 100nsec if 1A is supplied to the gate or it can turn on in 100msec if the gate current is decreased to 1mA.

Gate Drive Strength

$I = f * Qg * Nx$

Depends on
F = switching frequency
Qg = total gate charge
Nx = number of MOSFETs



Qg = total gate charge
Qgs = gate charge

Qg/Qgs = 3 .. 7 (depending on supplier)

GDU drive strength capability

S12ZVM Gate Drive Strength limit

I = f * Qg * Nx = 70mA

→ absolute max value of LDO

→ limiting factor will be **power dissipation** rather than current limit

Recommended Parameters

- Vgs ~ 11V
- f: 20kHz PWM cycle
- Qg max = **100nC** (**total** gate charge)
- Nx: 6 switch events per PWM cycle

→ I = f * Qg * Nx = 20k * 100n * 6 = **12mA**

→ all parameters can be varied as long as the max supply current and power dissipation is within limits

- Qg max = 150nC (@f=20kHz, Nx = 4)
- Qg max = 66nC (@f=30kHz, Nx = 6)
- Qg max = 100nC (@f=30kHz, Nx = 4)

IFX MOSFET examples

Pin		Qg (typ)	total gate charge max	Vds	Vgs	rdson [mOhm]	Ptot	Avalanche energy [mJ]	IDmax @20degC	IDmax @100degC
IPB80N04S3-06 IPP80N04S3-06 IPI80N04S3-06		15.0	47.0	40.0	2 .. 4	5.4	100.0	125.0	80.0	71.0
IPB80N06S4-05 IPP80N06S4-05 IPI80N06S4-05		28.0	81.0	60.0	2 .. 4	5.4	107.0	152.0	80.0	75.0
IPB80N06S4-07 IPP80N06S4-07 IPI80N06S4-07		21.0	56.0	60.0	2 .. 4	7.1	79.0	71.0	80.0	58.0
IPD90N06S4-07		21.0	56.0	60.0	2 .. 4	6.9	79.0	67.0	90.0	63.0
IPD90N06S4-05		28.0	81.0	60.0	2 .. 4	5.1	107.0	135.0	90.0	77.0
IPD90N06S4-04		44.0	128.0	60.0	2 .. 4	3.8	150.0	331.0	90.0	90.0
IPB90N06S4-04 IPP90N06S4-04 IPI90N06S4-04		44.0	128.0	60.0	2 .. 4	3.7	150.0	331.0	90.0	90.0
IPB120N06S4-02 IPP120N06S4-02 IPI120N06S4-02		63.0	195.0	60.0	2 .. 4	2.4	188.0	560.0	120.0	120.0
IPB180N06S4-H1		84	270		2 .. 4	1.7		700	180	180

Carcassonne supported FET‘s are marked green

IR MOSFET examples

Pin	Module	Qg (typ)	total gate charge max	Vds	Vgs	rdson [mOhm]	Ptot	Avalanche energy [mJ]	IDmax @20degC	IDmax @100degC
AUIRF1018E AUIRF1018ES	2_IRF	10.0	69.0	60.0	2 .. 4	8.4	110.0	88.0	79	56
AUIRF1010EZ AUIRF1010EZS	2_IRF	19.0	86.0	60.0	2 .. 4	8.5	140.0	99.0	84	60
AUIRF2805S	2_IRF	38.0	230.0	55.0	2 .. 4	4.7	100.0	380.0	135	96
AUIRF2804S	2_IRF	63.0	260.0	40.0	2 .. 4	1.6	330.0	630.0	320	230
AUIRF3006-7	2_IRF	37.0	300.0	60.0	2 .. 4	2.1	375.0	303.0	293	207
AUIRFB3206	2_IRF	29.0	170.0	60.0	2 .. 4	3.0	300.0	170.0	210	150
AUIRF3805S	2_IRF	52.0	290.0	55.0	2 .. 4	3.3	300.0	650.0	210	150
AUIRF4104S	2_IRF	21.0	100.0	40.0	2 .. 4	5.5	140.0	120.0	120	84
IRF7739	2_IRF	46.0	330.0	40.0	2 .. 4	1.0	125.0	270.0	375	190

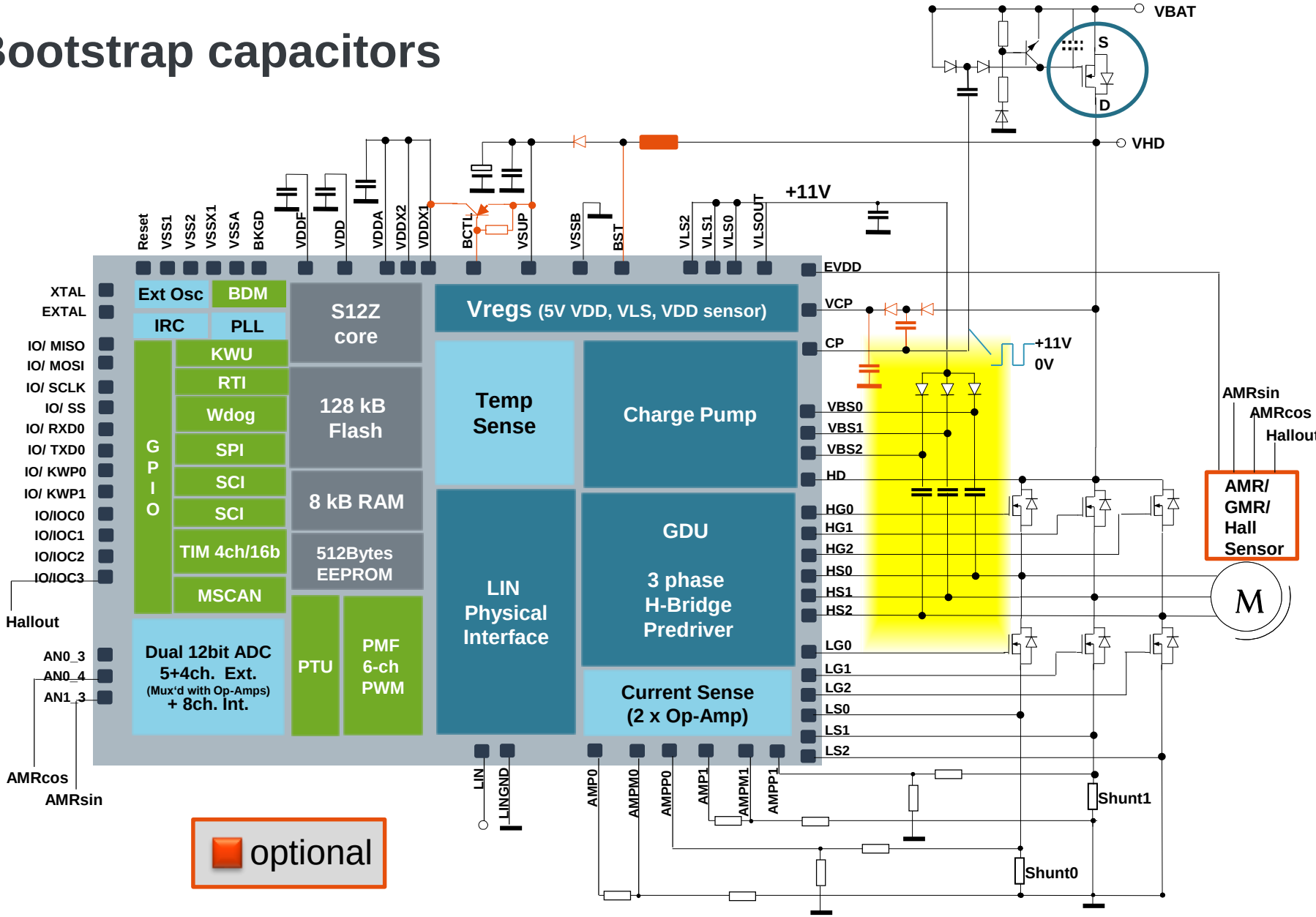
Carcassonne supported FET‘s are marked green

ST MOSFET examples

Pin	Module	Qg (typ)	total gate charge max	Vds	Vgs	rdson [mOhm]	Ptot	Avalanche energy [mJ]	IDmax @20degC	IDmax @100degC
STB141NF55 STP141NF55	2_STM	142 (typ)	na	55	2 .. 4	8.0	300	1300	80	80
STB150NF55 STP150NF55	2_STM		190	55	2 .. 4	6.0	300	850	120	106
STB185N55F3 STP185N55F3	2_STM	100 (typ)	na	55	2 .. 4	3.8	330	1000	120	120
STB60NF06	2_STM		66	60	2 .. 4	16.0	110	360	60	42
STB80NF55-06	2_STM		190	55	2 .. 4	6.5	300	1300	80	80
STB80NF55-08T4	2_STM		155	55	2 .. 4	8.0	300	100	80	80
STB85NF55 STP85NF55	2_STM		150	55	2 .. 4	8	300	980	80	80
STP80NF55-08	2_STM		155	55	2 .. 4	8.0	300	1000	80	80
STV250N55F3	2_STM	100 (typ)	na	55	2 .. 4	2.2	300	1000	250	175

Carcassonne supported FET‘s are marked green

Bootstrap capacitors



Dimensioning of the Bootstrap Capacitor

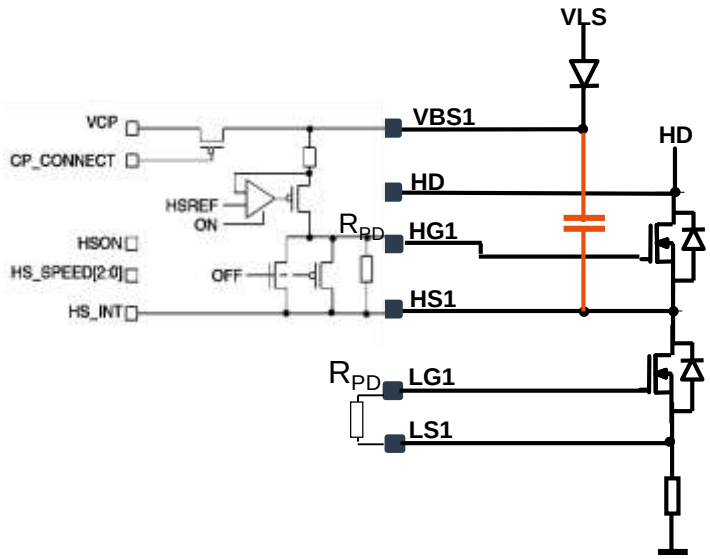
- Bootstrap Capacitor size CBS selection depends on:
  - total gate charge Qg of MOSFET
  - acceptable voltage drop at Bootstrap cap on VBS pin
  - Current used by the GDU during the max. duty cycle (incl. integrated Gate Source resitor of 75kOhm in S12ZVM)

$$Q = C * V$$

$$C_{boot} \geq \frac{Q_G + D_{max} * T_{SW}\left(\frac{V_{LS} - V_f}{R_{PD}} + I_{drv}\right)}{\Delta V}$$

Simplified as I_{GDU}

Q_G = Total gate Charge of MOSFET
D_{max} = maximum Duty cycle
R_{PD} = integrated Gate Source resistor
T_{SW} = PWM Period
I_{drv} = current consumption of HS driver
V_{LS} = Gate drive supply
V_f = forward Voltage
ΔV = voltage drop accepted on Cboot at end of ON time



Dimensioning of the Bootstrap Capacitor

Example EVB board:

With

Q_G of IPD80N04S3-06 = 47nC

T_{SW} = 1/20 kHz = 50µs

D_{max} = 90% = 0.9

ΔV = 0.5V

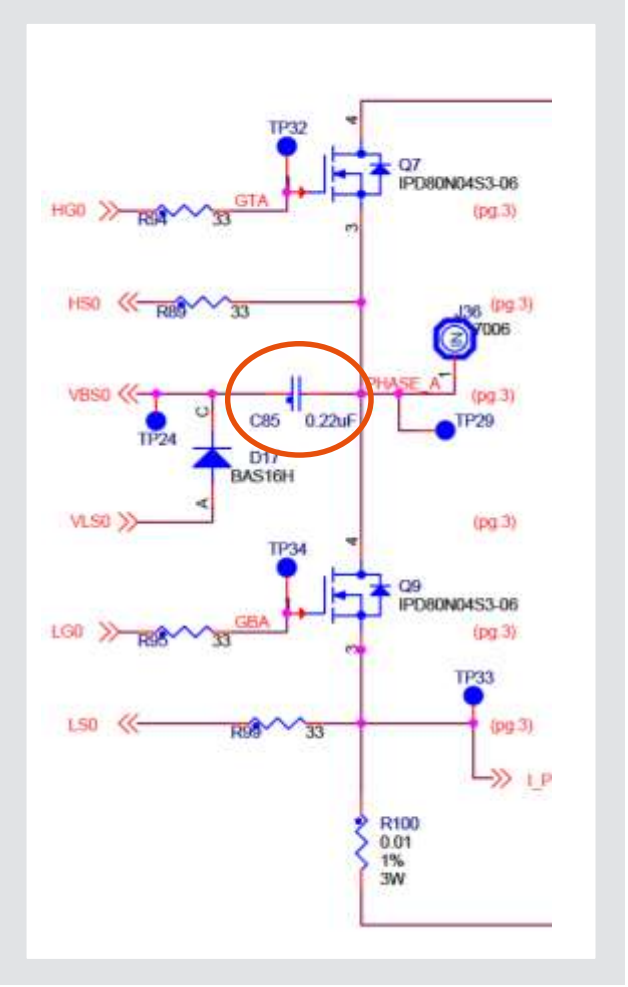
I_{GDU} <=600µA

$$C_{boot} \geq \frac{47nC + 0.9 * 50\mu s * 600\mu A}{0.5V}$$

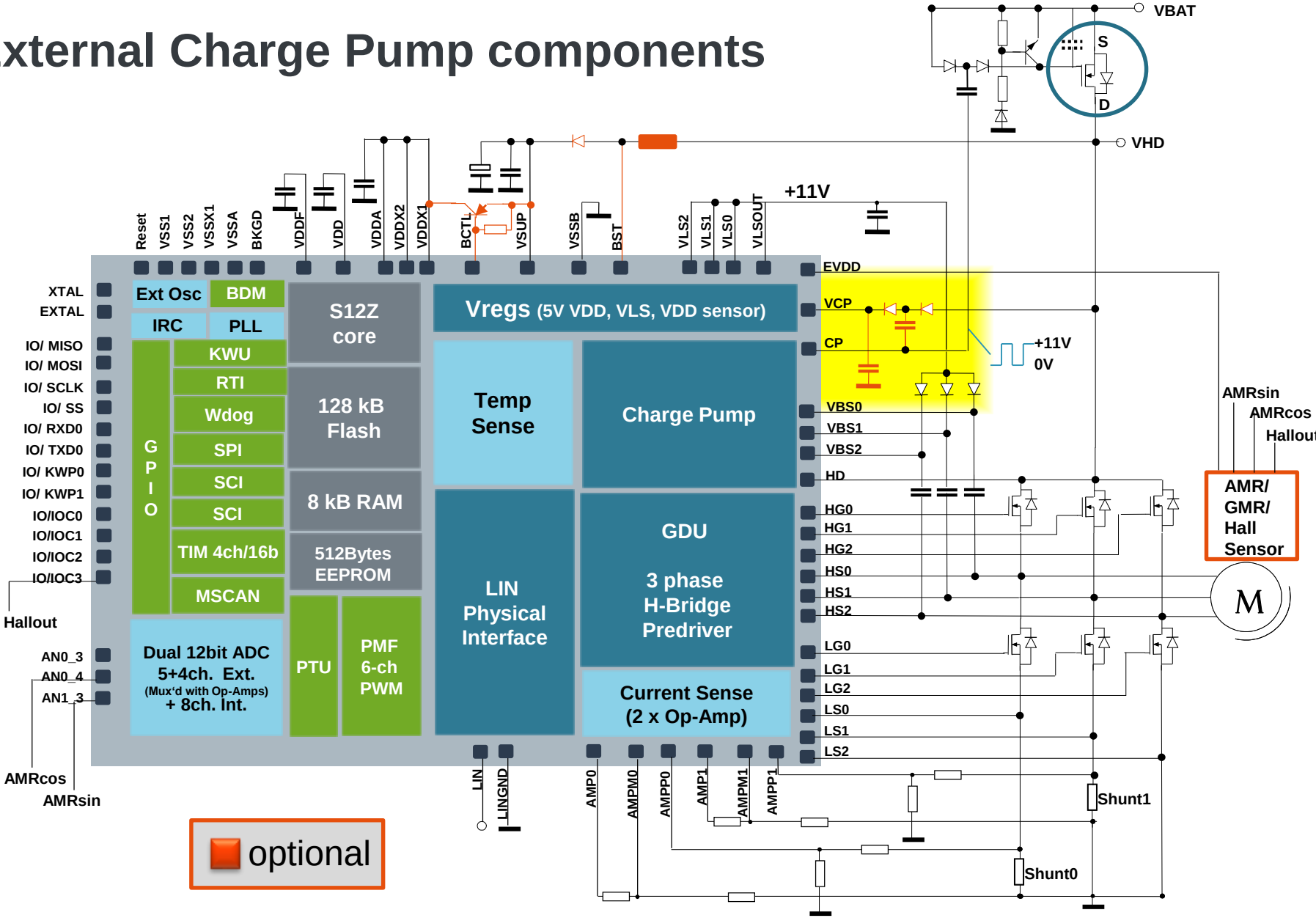
$C_{boot} \geq$ 148nF

Considering lifetime tolerances

C_{boot} = 220nF selected



External Charge Pump components



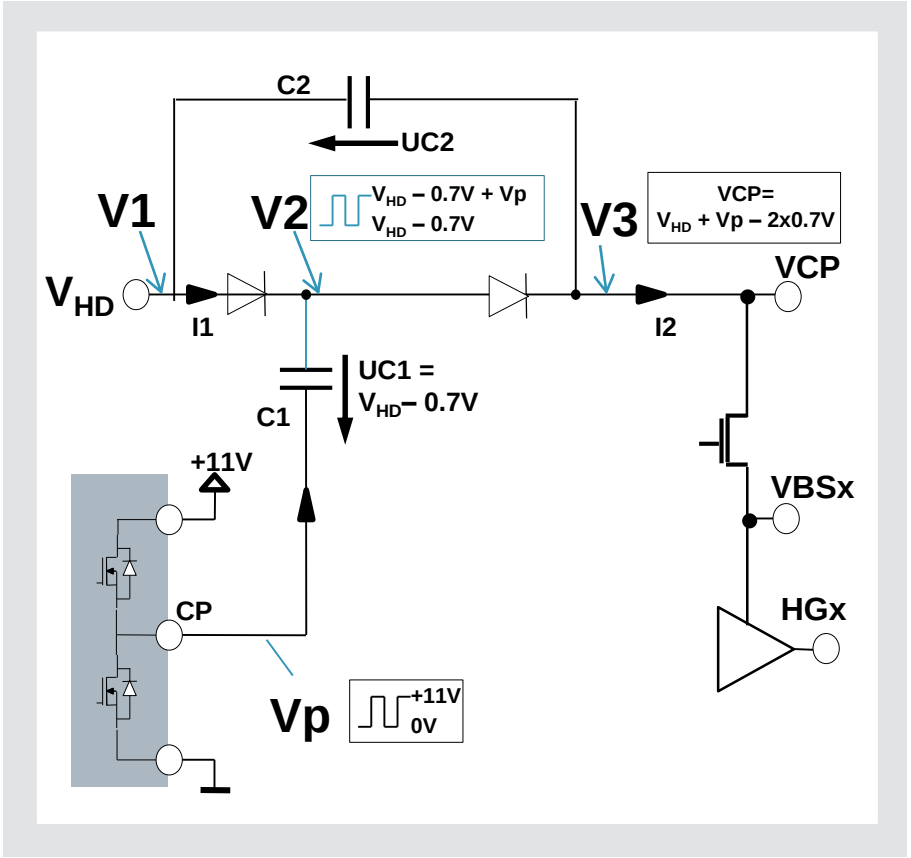
Charge pump basic characteristic

Charge pump states:

- Vp = 0
  - Load C1 to V_{HD} – 0.7V
- Vp = +11V
  - Load C2 with charge of C1
  - dUC2 = UC1 * C1/C2
  - UC2 = VHD– 2x0.7V

Characteristic Summary:

- Charge pump adds fixed voltage on top of V1
  - Independent of the relation of V1 and Vp
  - If V1 = Vp it serves as a voltage doubler
- I1 = 2 x I2
- V3 ripple is minimum for C2 >> C1
  - reduces the feedthrough of V1 ripple on V3
    - Lower plate of C2 should be connected to V_{HD}



V3 = V1 + Vp – 2 x 0.7V

Charge Pump Dimensioning

- **Component selection depends on**
  - selected charge pump frequency
  - acceptable voltage ripple
  - GDU current for the static HS Switch drive
  - acceptable power dissipation (on charge pump diodes)

$$f >= \frac{I_{GDU}}{C_{pump} * V_{ripple}}$$

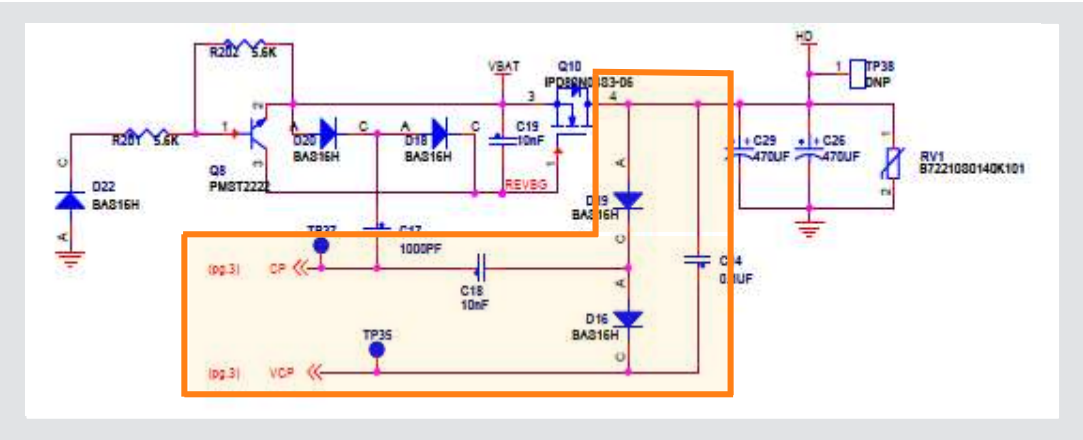
Example EVB board setup:

C1 = 10nF

C2 = 100nF
(connected to V_{HD})

f = 500kHz

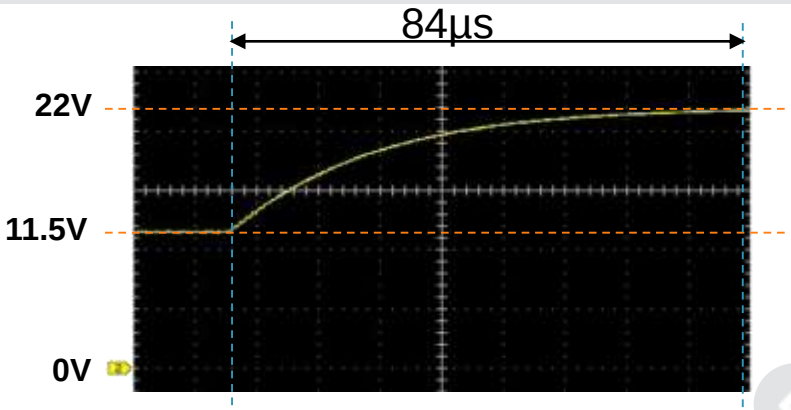
I_{GDU} = 2mA
(assuming worst case of 3 HS to be switched at same time)



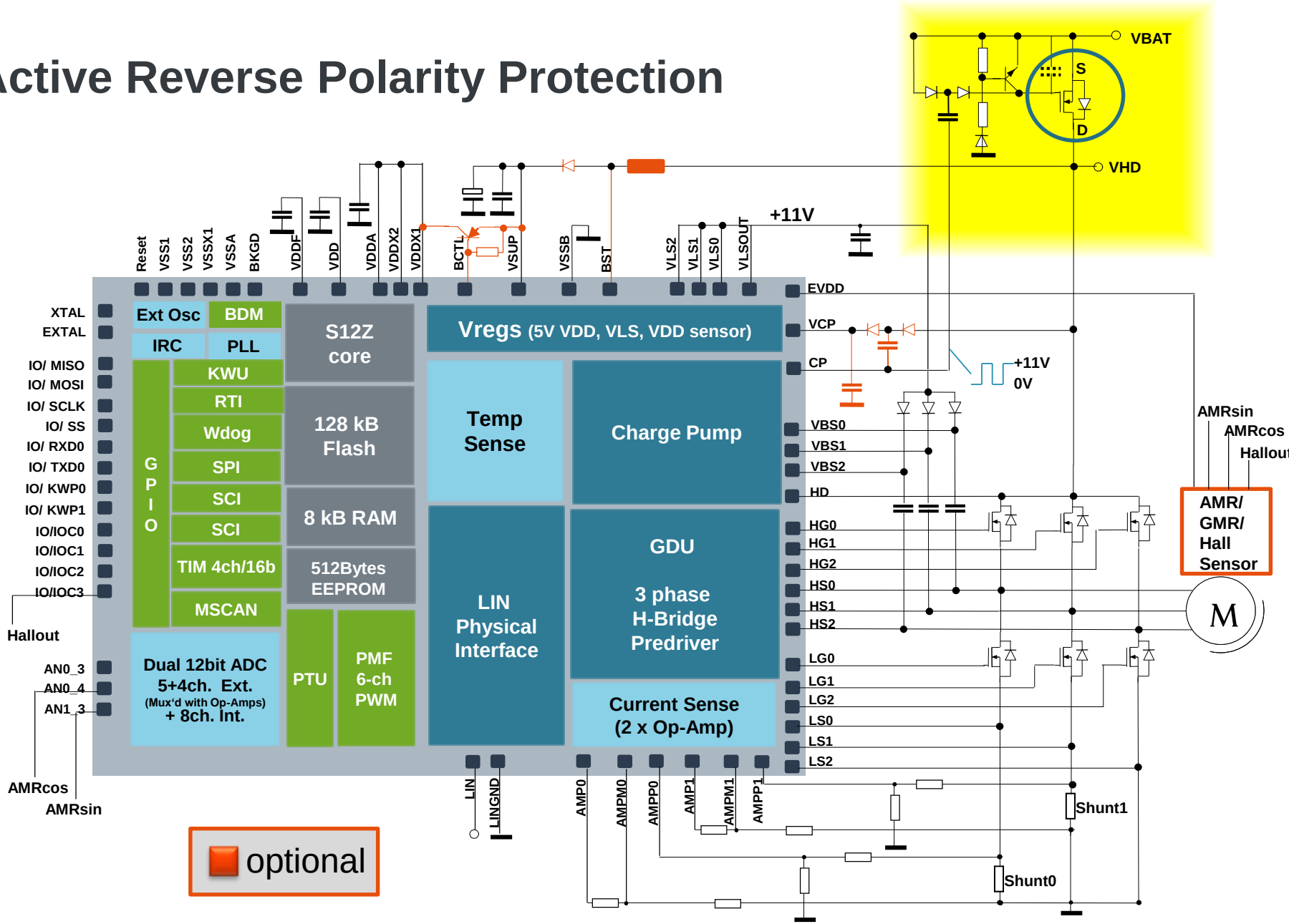
$$\rightarrow V_{ripple} = \frac{2mA}{10nF * 500kHz} = 40mV$$

Charge Pump startup:

Measured smooth charge pump startup on VCP @ 1.56MHz

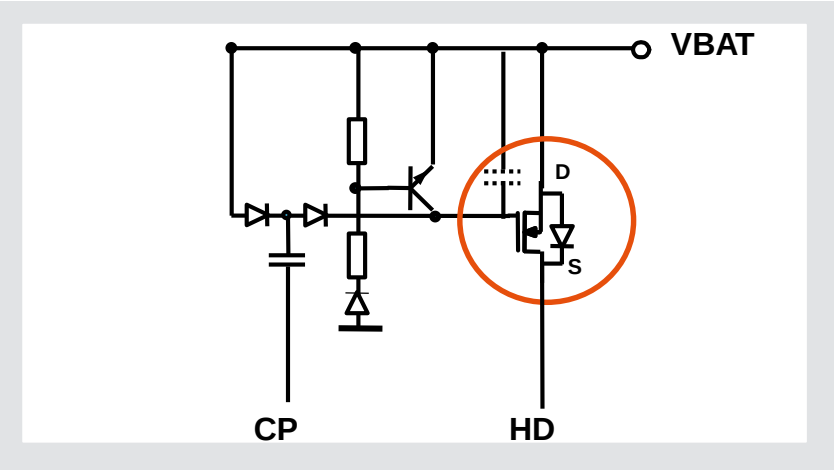


Active Reverse Polarity Protection



Active reverse protection Circuitry

Charge Pump can be used to drive gate of the reverse protection MOSFET



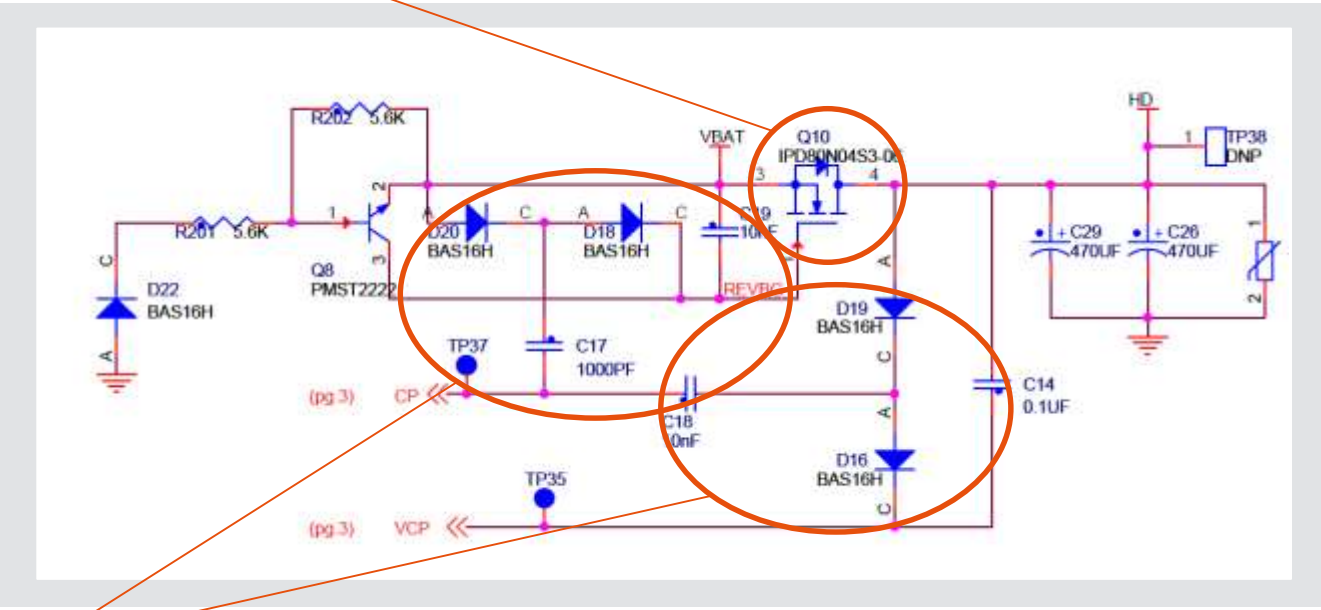
- Secondary charge pump cap & diodes recommended to decouple Gate Charge Pump from Active reverse protection circuitry

- Additional transistor recommended to switch off MOSFET fastly in case of reverse voltage supply

Example active reverse protection Circuitry

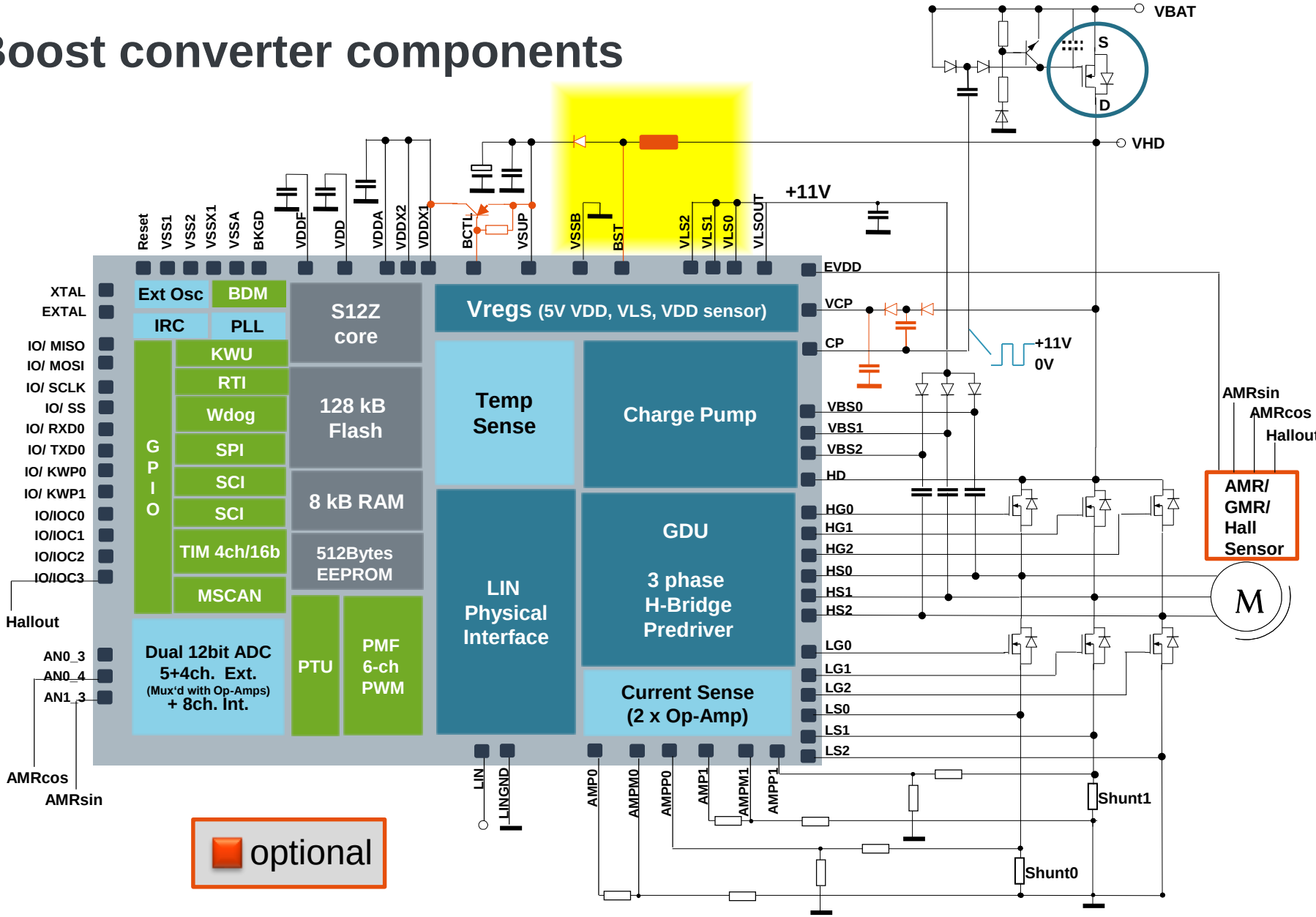
Example EVB board setup:

• same MOSFET as for Bridge
IFX
IPD80N04S3-06



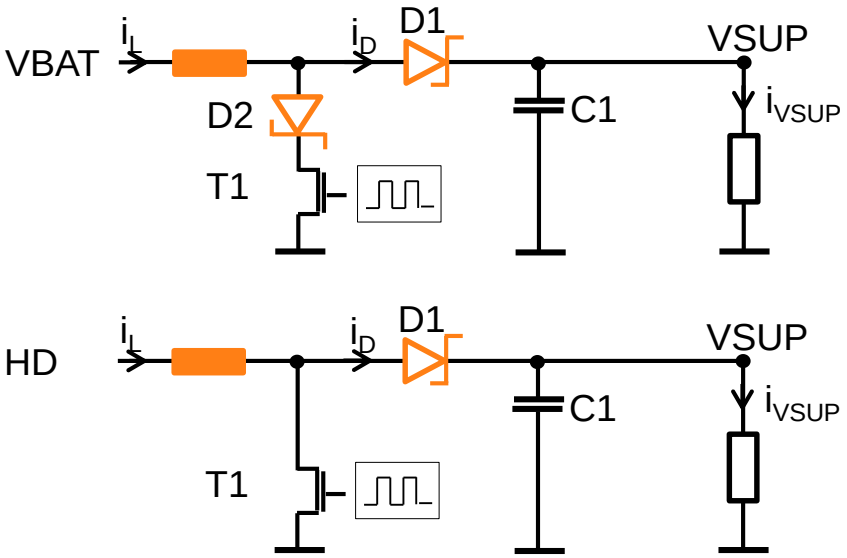
• two independant charge pump circuitries

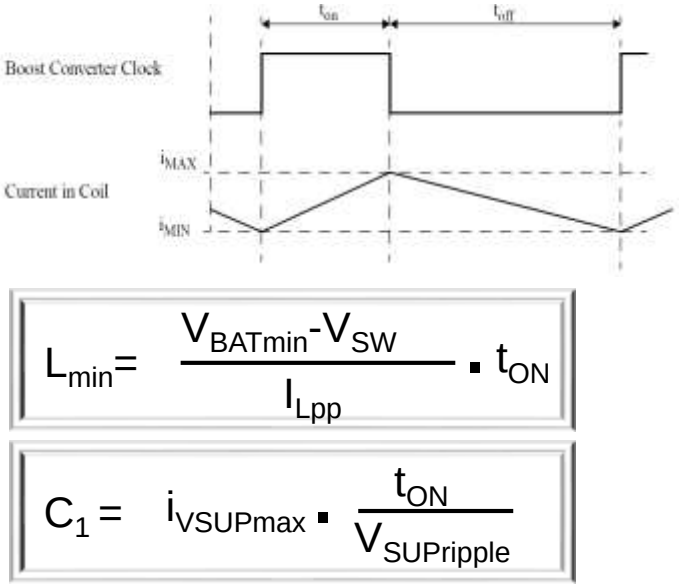
Boost converter components



Boost converter component selection

- Gated oscillator (Pulse Burst Modulation) Converter technique used
- Optional Boost Mode circuitry, two possible setups:





- Component selection depends on:
- Boost frequency
  - selectable from 62kHz to MHz range (High speed frequency option added to optimize design for small Ls)
- Selected Boost duty cycle
  - selectable between 25% , 50% or 75%
- Acceptable peak current iL
  - max. current in coil
- Load current (µC & GDU drive current)
  - depends on system setup , for example bus frequency (if µC VDDX connected via bypass transistor),FET gate charge
- Minimum required Vbat Voltage
  - 3.5V minimum
- Acceptable ripple on Vsup

Boost Converter Coil selection

- The coil inductance and boost frequency/duty cycle strongly influence the Coil peak current, which affects Power Dissipation and EMC emission.
- A good compromise has to be made between
  - EMC ($f_{boost,}$, dI/dt),
  - Power Dissipation (Peak current $I_{Lpp)}$),
  - Cost of external components (Coil Inductance L_{min})

$$I_{Lavg} = I_{OUT} \cdot \frac{V_{OUT}}{V_{IN}}$$

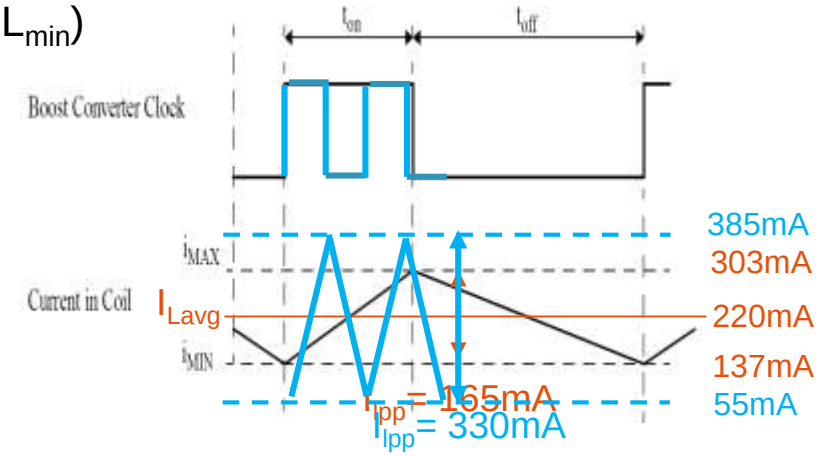
With:
I_{OUT} = 70mA
V_{OUT} = 11V
V_{IN} = 3.5V

$$I_{Lavg} = 70mA \cdot \frac{11}{3.5} = 220mA$$

$$L_{min} = \frac{V_{BATmin} - V_{SW}}{I_{Lpp}} t_{ON}$$

With:
L_{min} = 100µH
V_{BATmin} = 3.5V
V_{SW} = 0.2V
f_{boost} = 100kHz
t_{ON} = 50% = 5µs

$$I_{Lpp} = \frac{3.5V - 0.2V}{100\mu H} \cdot 5\,\mu s = 165mA$$

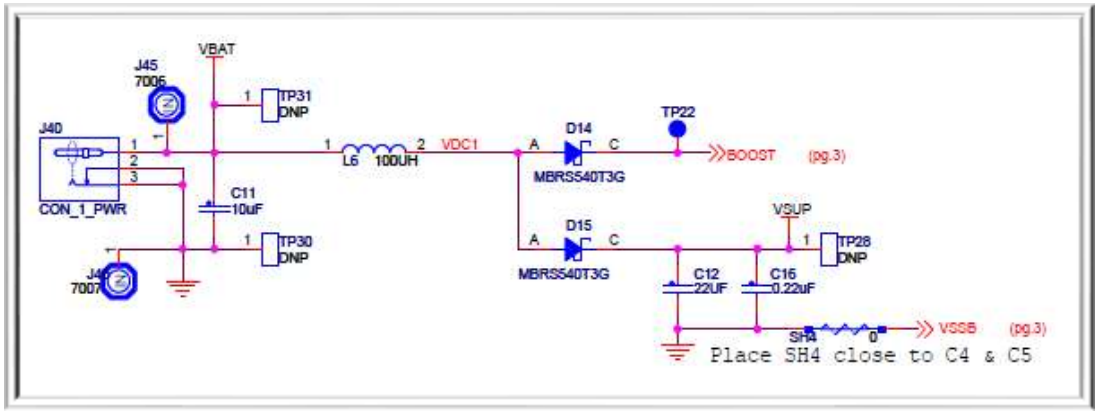


With:
L_{min} = 10µH
V_{BATmin} = 3.5V
V_{SW} = 0.2V
f_{boost} = 500kHz
t_{ON} = 50% = 1µs

$$I_{Lpp} = \frac{3.5V - 0.2V}{10\mu H} \cdot 1\,\mu s = 330mA$$

Boost converter capacitor selection

EVB Board Example:



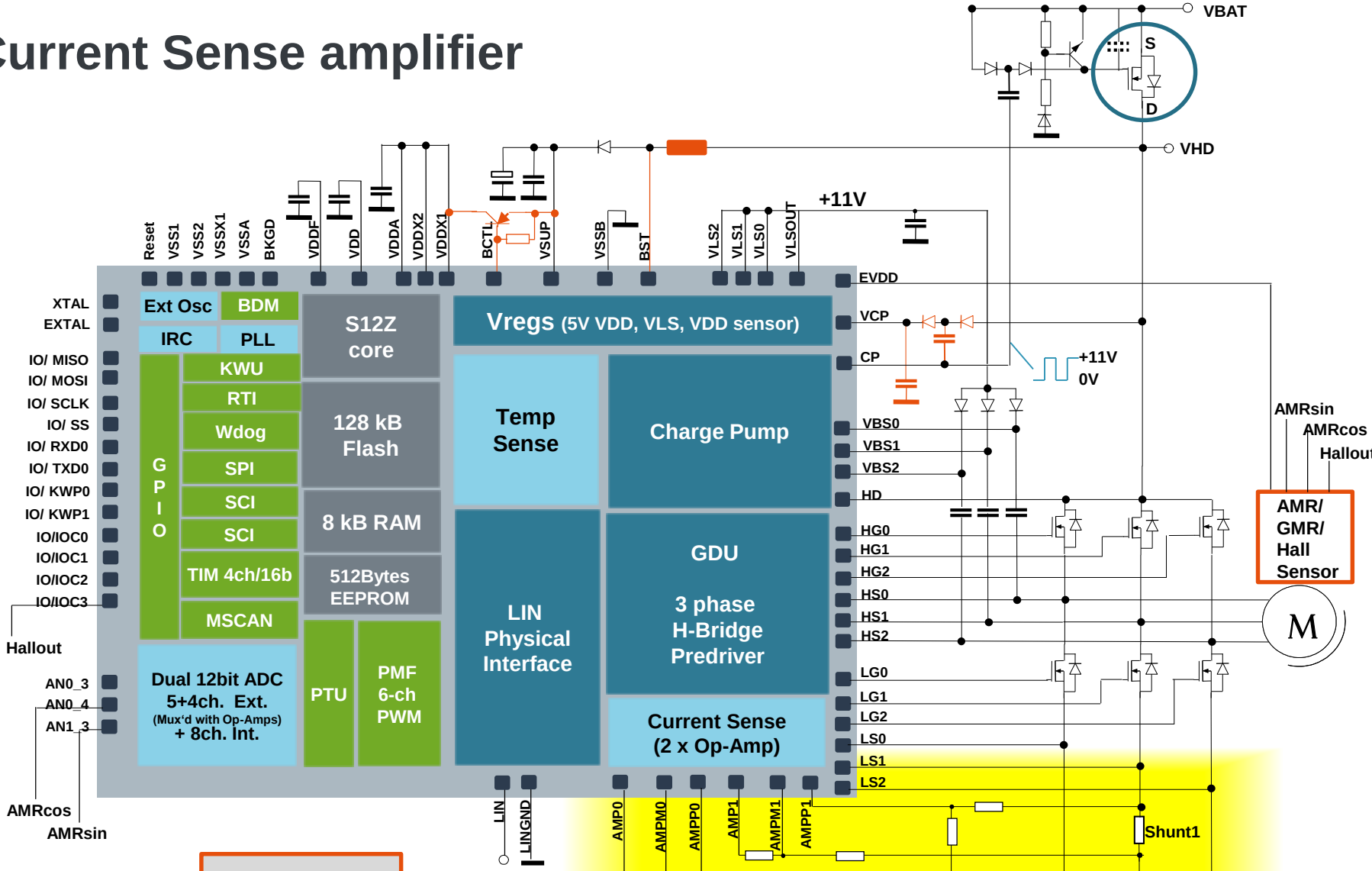
L = 100µH
C1 = 22µF+220nF

With f_{boost}=100kHz , 50% duty cycle and $i_{VSUPmax}$ = 70mA

$$C_1 = i_{VSUPmax} \cdot \frac{t_{ON}}{V_{SUPripple}}$$

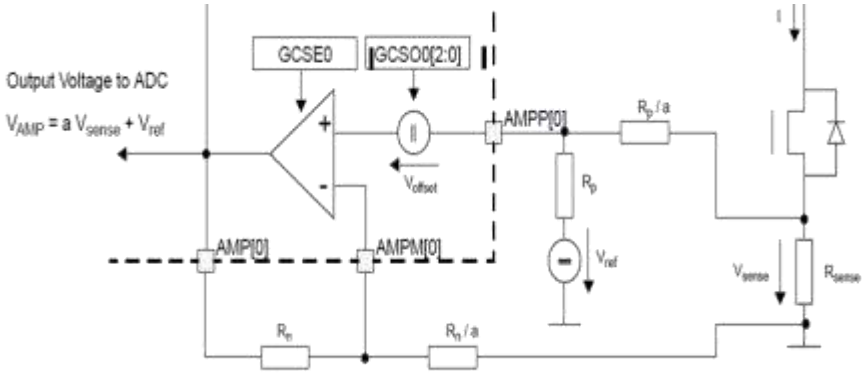
$$V_{SUPripple} = 70m \cdot \frac{5\mu s}{22\mu F +/- 50\%} = 11\ mV \text{ to } 32mV$$

Current Sense amplifier



Current Sense amplifier

- connected as a differential amplifier
- senses the current flowing through the external power FET as a voltage across the shunt
- to measure positive and negative currents an external reference Vref has to be used



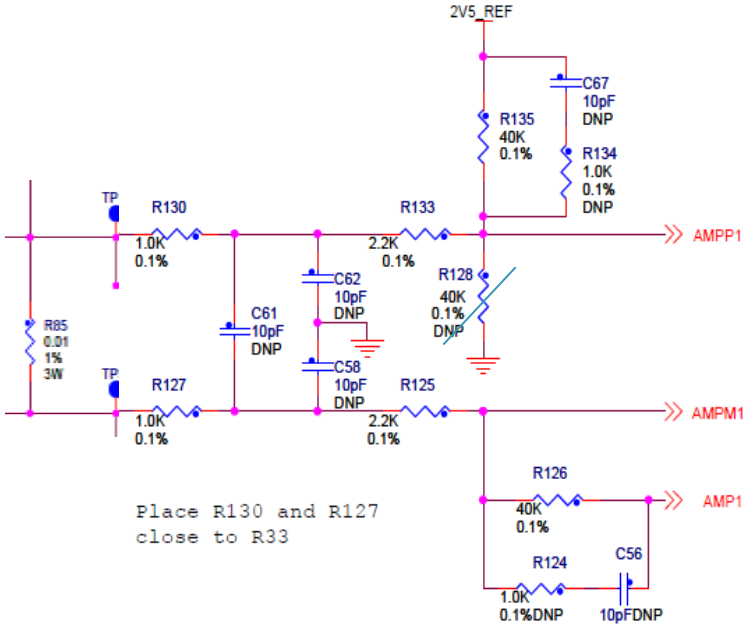
EVB Board Example:

Shunt resistor of 10mΩ sensing current
→ R_{shunt}= 10mΩ = 10mV / A

Selected Gain = 40kΩ / 3.3kΩ = 12.1
→ V_{AMPpp} = 121mV / A * I

Selected V_{ref} = 2.5V

→ @ 20A Phase current : V_{AMP} = 2.4V + 2.5V



MagniV in 24V Applications

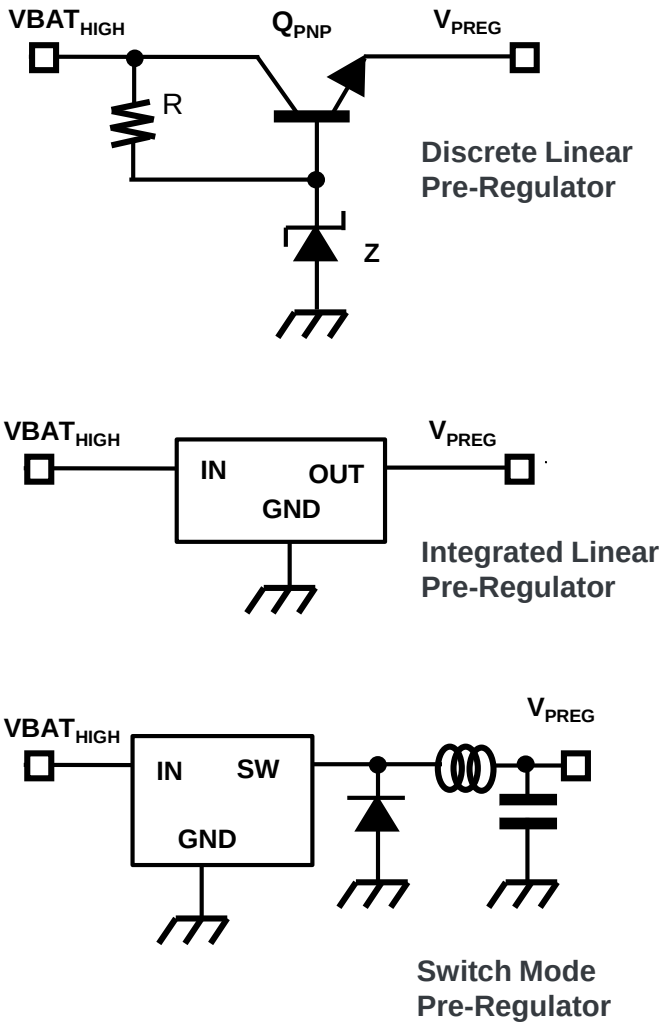
Enabling MagniV for Truck Applications

MagniV in 24V Applications

- This section introduces some considerations on how to enable MagniV family devices for 24V applications.
- In particular cases, the common PCB design can be used for both 12V and 24V applications (e.g. cars and trucks).
- The key approach is to add selected external components that extend the device's operational voltage range.

MagniV in 24V Applications

- The MagniV devices can operate from 5.5V to 18V. **The MagniV devices include a +5V regulator**, so there is no need to regulate the voltage precisely.
- Considering the minimal operating voltage of 10V (ISO16750-2 Norm), and keeping the pre-regulator and MagniV on-chip regulator power dissipation at a reasonable level, **the pre-regulator output voltage is regulated to 8V.**
- The discrete or integrated linear pre-regulator is recommended to use for power supply currents below 50mA. The higher currents are managed by a switching power supply as pre-regulator interface.



Summary

MagniV building blocks

High-Voltage Components

- **VREG for tot. supply:**
  - 70mA w/o ext comp. or
  - 170mA with ext. ballast
- **LIN-PHY**
- **CAN-PHY**
- **V-BAT SENSE**
- **V-SUP SENSE**
- **1-4ch HVI** (12V-input with wake-up and ADC)
- **LS-drivers**
- **HS-drivers**
- **Charge Pump**
- **4-6ch Gate Drive Unit for FET Qg=50-150nC**

Digital Components

- **MSCAN**
- **Sent**
- **SCI**
- **SPI**
- **IIC**
- **GPIO**
- **PGPIO 20mA**
- **NGPIO 25mA**
- **BDM/BDC**
- **Key Wakeups**
- **Win Wdog**
- **RTC**
- **Timer** 16Bit (25-64MHz)
- **PWM** 8/16Bit (25-64MHz)
- **Motorcontrol PWM With Fault protection**
- **Programmable Trigger Unit**
- **Sound Generator**
- **Segment LCD (4x40)**
- **Stepper Motor Driver with SSD**

MCU Core and Memories

- **S12- or S12Z-CPU 25/32/50MHz bus**
- **Flash (ECC) 8kB – 192kB**
- **EEPROM (ECC) 128B – 4kB**
- **RAM (ECC) 512B - 8kB**

5V Analogue Components

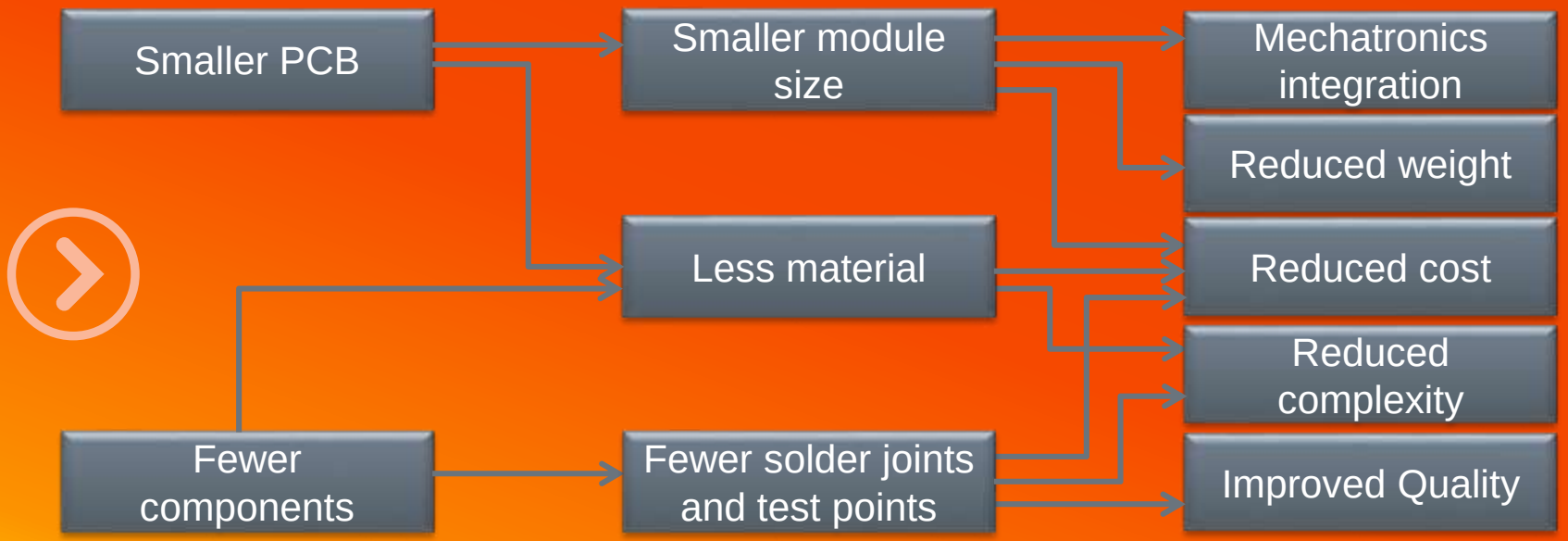
- **List Based ADC** 10-12Bit resolution 1-2 S/H-units Up to 16ch total
- **Temp Sense**
- **Current Sense** (2 x Op-Amp)
- **PGA** Up to 80x
- **2ch ACMP** With 1x6-Bit-DAC
- **Pierce Osc.**
- **32kHz low power Osc**
- **RCosc. +/-1.3%**
- **PLL**

Packaging

- **LQFP:** 32/48/64/100/144-pin
- **LQFP-EP:** 48/64-pin 

- **QFN:** 32-pin (5x5mm)

Manufacturing Efficiency



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