Micron's Support of the Automotive and Embedded Markets

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Review of Freescale / Micron Compatibility Guide and what is new since our last version

Micron® Memory Support for Freescale Platforms

i.MX Processor Memory Support Matrix										
Micron Solutions offered for i.MX Processors		*i.MX 6Quad/i.MX 6Dual/DualLite/Solo*			*i.MX 6SoloLite*		*i.MX 6SoloX*	*i.MX6 Dual/Quad*	*i.MX6 Solo*
		SABRE for Automotive Infotainment	SABRE Platform for Smart Devices	Quick Start Board	Evaluation Kit	WaRP (Wearable Reference design)	SABRE SDB	MX6Q PoP third party reference modules	RIOTBoard.ORG
DRAM	Type	DDR3	DDR3	DDR3	LPDDR2	eMCP (LPDDR2 with eMMC)	DDR3	LPDDR2 PoP	DDR3L
	Density	4Gb	2Gb	2Gb	8Gb	4Gb	4Gb	8Gb	4Gb
	Configuration	256 Meg x 16	128 Meg x 16	128 Meg x 16	256 Meg x 32	256 Meg X 16	256 Meg x 16	128 Meg x 64	256 Meg x 16
	Package	96-ball FGBA	96-ball FGBA	96-ball FGBA	168-ball VFBGA	162-ball VFBGA	96-ball FGBA	216-ball PoP	96-ball VFGBA
	Validated PN	MT41J256M16RE	MT41J128M16HA	MT41J128M16HA	MT42L256M32D2LG	MT29PZZZ4D4BKESK	MT41K256M16HA-125:E	MT42L128M64D2LL-25 AT:A	MT41K256M16HA
	Recommended PN	MT41K family*	MT41K family*	MT41K family*	MT42L family*	MT29P family**	MT41K family*	MT42L family*	MT41K family*
	Qty/Board	4	4	4	1	1	2	1	2
NAND	Type	Raw	e•MMC	e•MMC	e•MMC	eMCP (LPDDR2 with e-MMC)	e•MMC	e•MMC	e•MMC
	Density	64Gb	8GB	8GB	8GB	4GB	8GB	4GB	4GB
	Package	48-pin TSOP	169-ball FBGA	169-ball FBGA	169-ball FBGA	162-ball VFBGA	153-ball TFBGA	153-ball VFBGA	153-ball WFBGA
	Validated PN	MT29F64G08AFAAA				MT29PZZZ4D4BKESK	MTFCBGLCDM	MTFC4GACAAAM-4M IT	MTFC4GMVEA-1M WT
	Recommended PN	MT29F/MTFC families	MTFC family	MTFC family	MTFC family	MT29P family**	MTFC family	MTFC family	MTFC family
NOR	Type	Parallel					Parallel		
	Density	256Mb					1Gb		
	Package	56-pin TSOP					64-ball TBGA		
	Validated PN	M29W256GL7AN6E					MT28GU01GAAA2EGC		
	Recommended PN	M29W family					MT28GU		
SPI NOR	Type	Serial	Serial		Serial		Serial		
	Density	32Mb	32Mb		32Mb		256Mb		
	Package	SO8W	SO8W		SO8W		SO8W		
	Validated PN	M25P32-VMW3TGB	M25P32-VMW6TG		M25P32-VMW6TG		N25Q256A13EF840		
	Recommended PN	N25Q/MT25Q families	N25Q/MT25Q families		N25Q/MT25Q families		N25Q/MT25Q families		

**MT41K family supports both 1.5V and 1.35V power supply and is backward compatible with MT41J family.*
***Micron's MT29PZZZ4D4BKESK is a multichip package which integrates a 4Gb LPDDR2 and a 4GB eMMC v4.5† in a single package.*

Depending on the application needs, choose between Micron's standard lifecycle products and our Product Longevity Program (PLP) products with extended lifecycle support. For more information, visit www.micron.com/lifecycle.

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Micron® Memory Support for Freescale Platforms

i.MX Processor Memory Support Matrix

Micron Solutions offered for i.MX 7 Processors		i.MX 7			
		SABRE for Smart Devices		Validation Platform	
DRAM	Type	DDR3L		LPDDR3	
	Density	4Gb		16Gb	
	Configuration	256 Meg x 16		512 Meg x 32 (2 rank)	
	Package	96-ball VFGBA		168-ball PoP (soldered on board)	
	Validated PN	MT41K256M16HA		EDFA232A2PF-GD-F-D	
	Recommended PN	MT41K family*		EDFA family*	
	Qty/Board	2		2	
NAND	Type	e-MMC	MLC NAND	e-MMC	SLC NAND
	Density	8GB	32Gb	8GB	32Gb
	Package	153-ball WFBGA	48-pin TSOP	153-ball WFBGA	48-pin TSOP
	Validated PN	MTFC8GACAEAM-1M WT	MT29F32G08CBADB	MTFC8GACAEAM-1M WT	MT29F32G08ABCDB14
	Recommended PN	MTFC family	MT29F family	MTFC family	MT29F family
NOR	Type			Parallel	
	Density			1Gb	
	Package			64-ball TBGA	
	Validated PN			MT28GU01GAAA1EG-0SIT	
	Recommended PN			MT28GU family	
SPI NOR	Type	Serial		Serial (Quad SPI)	Serial (Twin Quad)
	Density	256Mb		256Mb	512Mb
	Package	SO8W		SO8W	SO16
	Validated PN	N25Q256A13E1240E		N25Q256A13E1240E	M25TL512HAA1ESF0AAT
	Recommended PN	N25Q/MT25Q families		N25Q/MT25Q families	MT25TL family

*MT41K family supports both 1.5V and 1.35V power supply and is backward compatible with MT41J family.

Kinetis K Family Processors

Micron Solutions			K70	K60	K50	K40	K30	K20	K10	E, L, M, W
DRAM	Type	DDR	✔	✔						
	Density	256Mb–1Gb								
	Configuration	x4, x8, x16								
	Package	TSOP, FBGA								
	Family	MT46V								
NAND	Type	Raw (host ECC required)	✔	✔				✔		
	Density	128Mb–512Gb								
	Package	48-pin TSOP								
	Family	MT29F								
SPI NOR	Type	Serial	✔	✔	✔	✔	✔	✔	✔	✔
	Density	8Mb–1Gb								
	Package	Many								
	Family	N25Q/MT25Q								

✔ *indicates the interface will support the memory device. Actual validation of a particular device has not been completed.*

Vybrid Processors

Micron Solutions				VF6XX	VF5XX	VF3XX
DRAM	Type	DDR3	LPDDR2	✔ DDR3 and LPDDR2	✔ DDR3 and LPDDR2	
	Density	4Gb, 8Gb	4Gb			
	Configuration	x4, x8, x16	x32, x64			
	Package	78-, 96-ball	134-, 253-ball			
	Family	MT41K family*	MT42L			
NAND	Type	Raw NAND		✔	✔	✔
	Density	128–512Gb				
	Package	48-pin TSOP				
	Family	MT29F				
QUAD SPI NOR	Type	Serial (Quad SPI) NOR		✔	✔	✔
	Density	8Mb–1Gb				
	Package	Many				
	Family	N25Q/MT25Q				
NOR	Type	Parallel NOR		✔	✔	✔
	Density	64Mb–2Gb				
	Package	48-, 56-pin TSOP, 64-ball BGA				
	Family	PC28F, JS28F, JR28F, M29W				

✔ *indicates the interface will support the memory device. Actual validation of a particular device has not been completed.*

*MT41K family supports both 1.5V and 1.35V power supply and is backward compatible with MT41J family.

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Micron® Memory Support for Freescale Platforms

QorIQ Processor Memory Support Matrix								
Micron Solutions		Value Tier	Mid-Range Tier			High-Performance Tier		
		P1010/P1014	P2022/P2021E	P2041/P2031	T2080/T2081	P408X	P5020/P5040	T4240
DRAM	Type	DDR3/DDR3L	DDR3	DDR3/DDR3L	DDR3/DDR3L	DDR3	DDR3/DDR3L	DDR3/DDR4L
	Density	4Gb	4Gb	4Gb	4Gb	4Gb	4Gb	4Gb
	Configuration	512 Meg x 8, 256 Meg x 16	512 Meg x 8, 256 Meg x 16	512 Meg x 8, 256 Meg x 16	512 Meg x 8, 256 Meg x 16	512 Meg x 8, 256 Meg x 16	512 Meg x 8, 256 Meg x 16	512 Meg x 8, 256 Meg x 16
	Package	78-ball, 96-ball	78-ball, 96-ball	78-ball, 96-ball	78-ball, 96-ball	78-ball, 96-ball	78-ball, 96-ball	78-ball, 96-ball
	Base PN	MT41J256M	MT41J256M	MT41J256M	MT41J256M	MT41J256M	MT41J256M	MT41J256M
NAND	Type	Raw (host ECC required)	Raw (host ECC required)	Raw (host ECC required)	Raw (host ECC required)		Raw (host ECC required)	Raw (host ECC required)
	Density	128Mb–512Gb	128Mb–512Gb	128Mb–512Gb	128Mb–512Gb		128Mb–512Gb	128Mb–512Gb
	Package	48-pin TSOP	48-pin TSOP	48-pin TSOP	48-pin TSOP		48-pin TSOP	48-pin TSOP
	Family	MT29F	MT29F	MT29F	MT29F		MT29F	MT29F
NOR	Type	Parallel	Parallel	Parallel	Parallel	Parallel	Parallel	Parallel
	Density	64Mb–2Gb	64Mb–2Gb	64Mb–2Gb	64Mb–2Gb	64Mb–2Gb	64Mb–2Gb	64Mb–2Gb
	Package	56-pin TSOP	56-pin TSOP	56-pin TSOP	56-pin TSOP	56-pin TSOP	56-pin TSOP	56-pin TSOP
	Family	M29W	M29W	M29W	M29W	M29W	M29W	M29W
NOR	Type	Serial	Serial	Serial	Serial	Serial	Serial	Serial
	Density	8Mb–1Gb	8Mb–1Gb	8Mb–1Gb	8Mb–1Gb	8Mb–1Gb	8Mb–1Gb	8Mb–1Gb
	Package	Many	Many	Many	Many	Many	Many	Many
	Family	N25Q/MT25Q	N25Q/MT25Q	N25Q/MT25Q	N25Q/MT25Q	N25Q/MT25Q	N25Q/MT25Q	N25Q/MT25Q
e•MMC	Type	Managed (JEDEC STD)	Managed (JEDEC STD)	Managed (JEDEC STD)	Managed (JEDEC STD)	Managed (JEDEC STD)	Managed (JEDEC STD)	Managed (JEDEC STD)
	Density	4GB–64GB	4GB–64GB	4GB–64GB	4GB–64GB	4GB–64GB	4GB–64GB	4GB–64GB
	Package	VFBGA, TFBGA, LFBGA	VFBGA, TFBGA, LFBGA	VFBGA, TFBGA, LFBGA	VFBGA, TFBGA, LFBGA	VFBGA, TFBGA, LFBGA	VFBGA, TFBGA, LFBGA	VFBGA, TFBGA, LFBGA
	Family	MTFC	MTFC	MTFC	MTFC	MTFC	MTFC	MTFC
eUSB	Type	Managed (USB)	Managed (USB)	Managed (USB)	Managed (USB)	Managed (USB)	Managed (USB)	Managed (USB)
	Density	2GB–16GB	2GB–16GB	2GB–16GB	2GB–16GB	2GB–16GB	2GB–16GB	2GB–16GB
	Package	36.9mm x 26.6mm	36.9mm x 26.6mm	36.9mm x 26.6mm	36.9mm x 26.6mm	36.9mm x 26.6mm	36.9mm x 26.6mm	36.9mm x 26.6mm
	Family	MTEDC	MTEDC	MTEDC	MTEDC	MTEDC	MTEDC	MTEDC
SATA SSD	Type	Managed (SATA)		Managed (SATA)	Managed (SATA)		Managed (SATA)	Managed (SATA)
	Density	100GB–960GB		100GB–960GB	100GB–960GB		100GB–960GB	100GB–960GB
	Package	2.5" drive, 7mm height		2.5" drive, 7mm height	2.5" drive, 7mm height		2.5" drive, 7mm height	2.5" drive, 7mm height
	Family	MTFDD		MTFDD	MTFDD		MTFDD	MTFDD

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Micron® Memory Support for Freescale Platforms

QorIQ Processor Memory Support Matrix						
Micron Solutions		Value Tier			Mid-Range Tier	
		LS1020/LS1021/LS1022	T1023/T1024	T1020, T1022, T1040, T1042	LS2085	
DRAM	Type	DDR3L	DDR3L UDIMM	DDR3L UDIMM	DDR4 UDIMM	
	Density	4Gb	4GB (x72, ECC, DR)	4GB (x72, ECC, DR)	8GB (x72, ECC, DR)	
	Configuration	256 Meg x 16	4GB (512 Meg x 72)	4GB (512 Meg x 72)	1 Gig x 72	
	Package	96-ball VFBGA	UDIMM (Dual Rank)	UDIMM (Dual Rank)	UDIMM (Dual Rank)	
	Part Number	MT41K256M16HA-125:E	MT18KSF51272AZ-1G6	MT18KSF51272AZ-1G6	MTA18ASF1G72AZ-2G1A1	
NAND	Type		Raw (host ECC required)	Raw (host ECC required)	Raw (host ECC required)	
	Density		8Gb	8Gb	16Gb	
	Package		48-pin TSOP	48-pin TSOP	48-pin TSOP	
	Family		MT29FBG08ABBCAH4	MT29F8G08ABABAWP-ITX:B	MT29F16G08ABABA	
NOR	Type	Parallel	Parallel	Parallel	Parallel	
	Density	128MB (1Gb) 16-bit NOR	128MB (1Gb) 16-bit NOR	128MB (1Gb) 16-bit NOR	128MB (1Gb) 16-bit NOR	
	Package	56-pin TSOP	56-pin TSOP	56-pin TSOP	56-pin TSOP	
	Part Number	MT28EW01GABA1HJS-0SIT	JS28F00AM29EWHA	JS28F00AM29EWHA	M29EW	
NOR	Type	Serial	Serial	Serial	Serial	
	Density	128Mb	512Mb	512Mb	512Mb	
	Package	24-ball TBGA	SO8, SO16, 24-ball TBGA	SO8, SO16, 24-ball TBGA	SOP2-16/300 mils	
	Part Number	N25Q128A13E1240F	MT25QL512ABA1ESF	N25Q512A13GSF40F	N25Q512A11GSF40F	
e•MMC	Type	Managed (JEDEC STD)		Managed (JEDEC STD)	Managed (JEDEC STD)	
	Density	4GB–64GB		4GB–64GB	4GB–64GB	
	Package	VFBGA, TFBGA, LFBGA		VFBGA, TFBGA, LFBGA	VFBGA, TFBGA, LFBGA	
	Part Number	MTFC		MTFC	MTFC	
eUSB	Type	Managed (USB)	Managed (USB)	Managed (USB)	Managed (USB)	
	Density	2GB–16GB	2GB–16GB	2GB–16GB	2GB–16GB	
	Package	36.9mm x 26.6mm	36.9mm x 26.6mm	36.9mm x 26.6mm	36.9mm x 26.6mm	
	Part Number	MTEDC	MTEDC	MTEDC	MTEDC	
SATA SSD	Type	Managed (SATA)		Managed (SATA)	Managed (SATA)	
	Density	100GB–960GB		100GB–960GB	100GB–960GB	
	Package	2.5" drive, 7mm height		2.5" drive, 7mm height	2.5" drive, 7mm height	
	Part Number	MTFDD		MTFDD	MTFDD	

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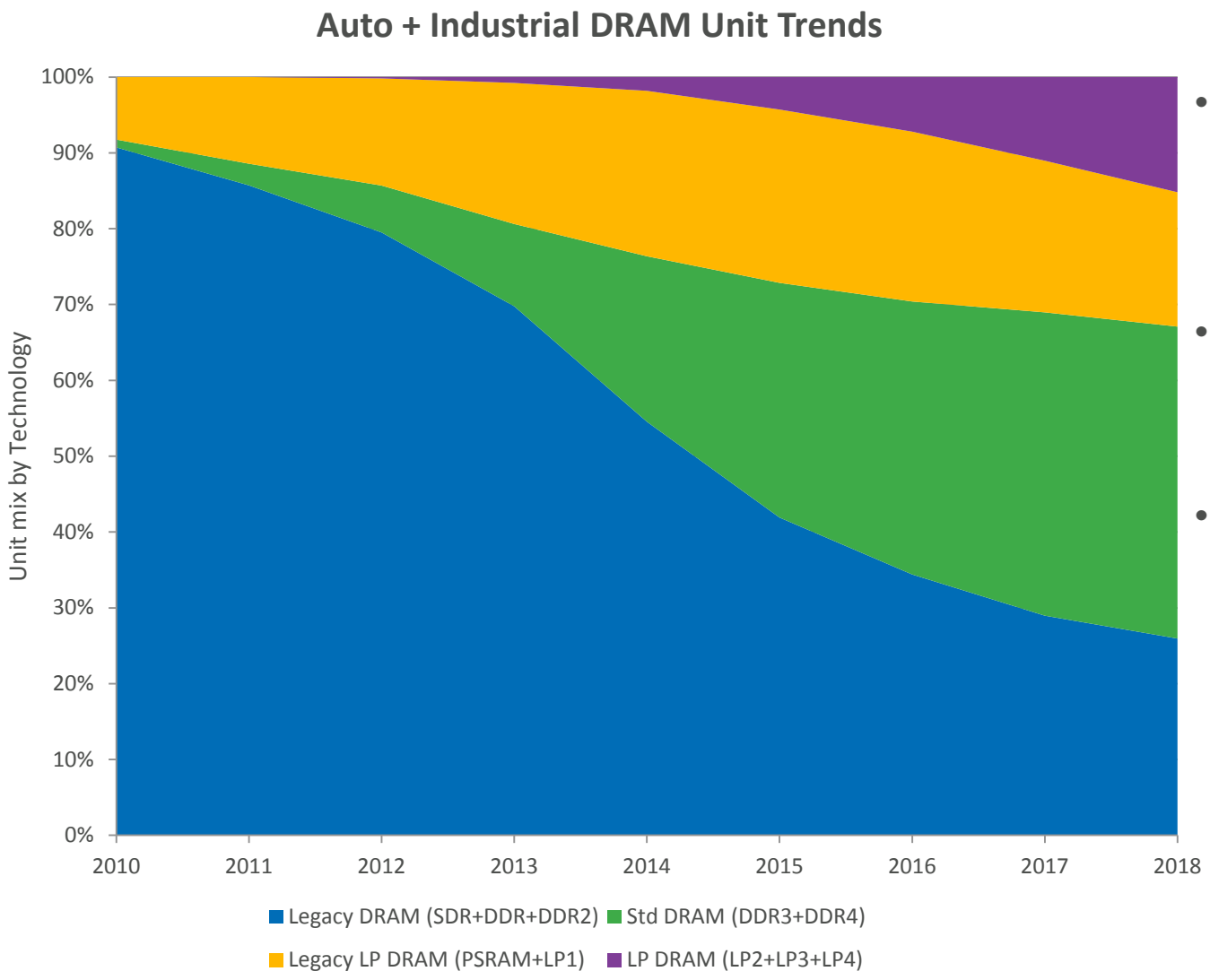
Market and Longevity updates

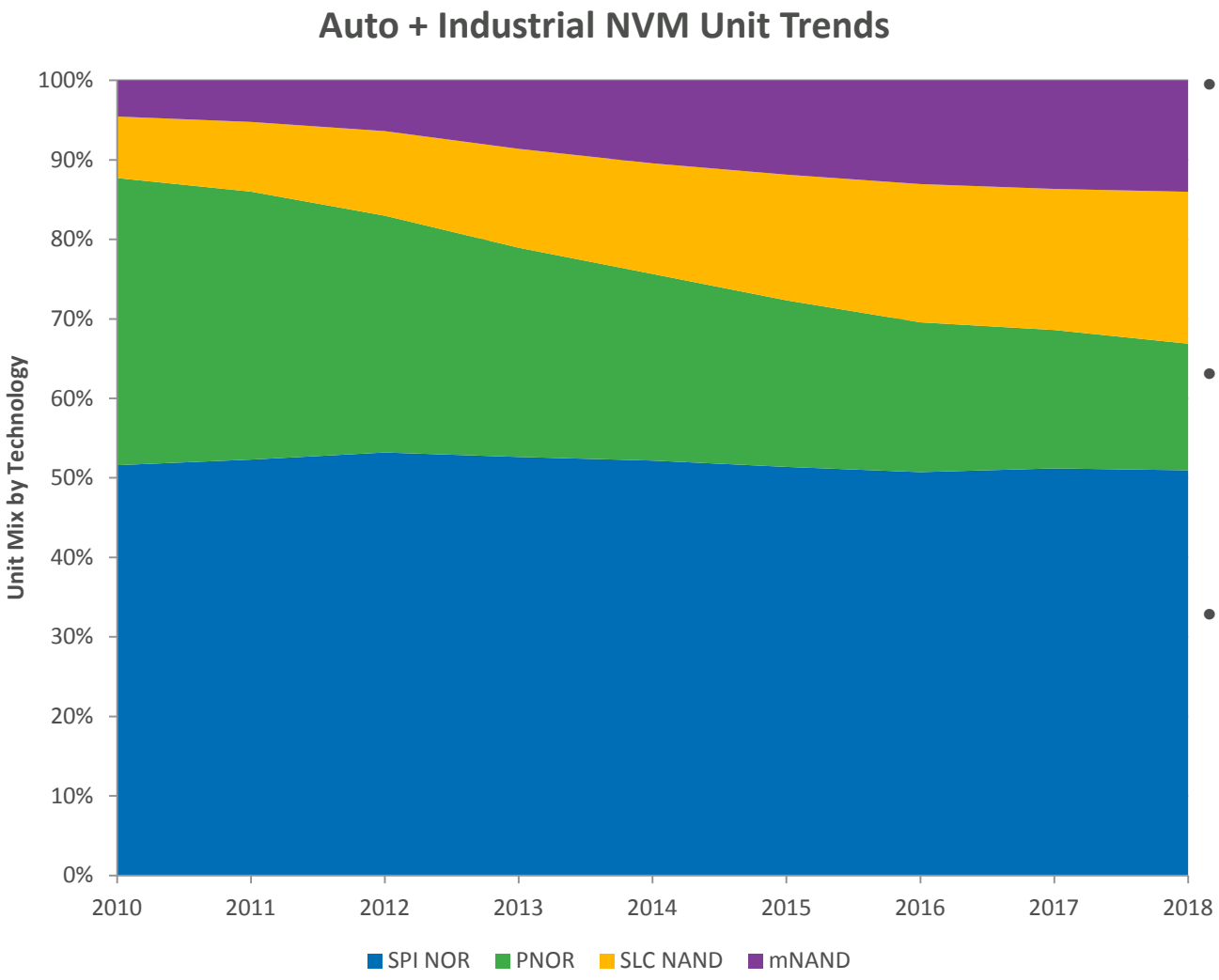
DRAM Market Overview



- Embedded ARM based solutions are driving LP DRAM adoption
- DDR3>DDR4 transition in IPC/SBC will take 3-5 years
- Embedded MCUs require low frequency operations (≤200MHz), anticipate continued long life SDRAM / LP SDRAM roadmap requirements

Source: iSuppli, Gartner, Infonetics, Micron Market Model Jan'14

Non Volatile Market Overview



- High capacity NAND solutions proliferating in embedded [ONFI, SD/uSD, SATA SSD, eMMC, etc.] for GB storage
- PNOR volumes declining on legacy platforms in favor of SPI NOR NAND or Managed NAND (eMMC) alternatives
- Low pin count SPI NOR Flash product lines evolving to address low power, high performance, and security
  - Transition from 3V > 1.8V for lower power
  - I/F expanding: x1, > x4, > x8 for performance

Source: iSuppli, Gartner, Infonetics, Micron Market Model Jan'14

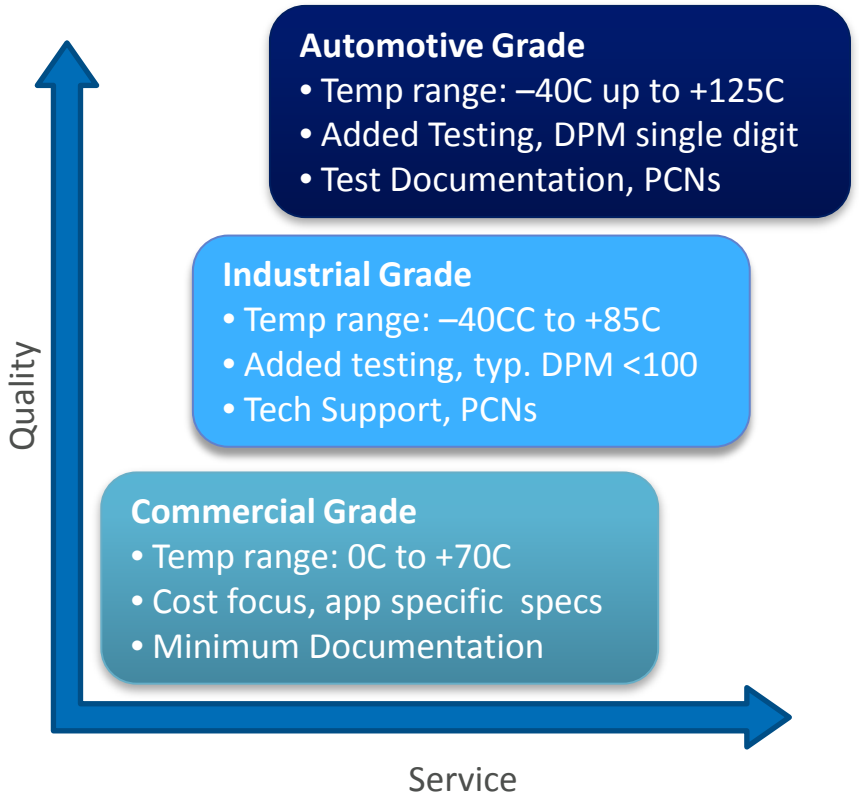
IMM Product Requirements

- **Supply Stability**
  - ✓ Main stream memory architectures
  - ✓ Multiple suppliers where possible
  - ✓ Product longevity & stability

10+ years Form, Fit, Function compatible

Typical Product Life Cycle for Industrial Applications (years)	
Aerospace & Military	10 to 15
Factory Automation	7 to 10
POS Equipment	7 to 10
Energy	7 to 10
Security Equipment	5 to 10
Building & Home Controls	5 to 10
Medical Electronics	3 to 10
Test & Measurement	3 to 7

- **Product Quality**



Source: Micron Sales

Industrial LINE CARD May'15

	Family	Voltage	Bus Width	Performance	Density Range	Temp Range	Package Options
DRAM	MT40 DDR4 SDRAM	1.2V	x8, x16	1067 to 1200 MHz	4-8Gb, 4GB-8GB	CT, IT	BGA, VFBGA, SODIMM, UDIMM, ECC SODIMM, ECC UDIMM
	MT41 DDR3 SDRAM	1.35V	x8, x16	667 to 800 MHz	1-4Gb; 1GB-8GB	CT, IT, AT	BGA, VFBGA, SODIMM, UDIMM, ECC SODIMM, ECC UDIMM
	MT47 DDR2 SDRAM	1.8V	x8, x16	333 to 400 MHz	512Mb-2Gb; 512MB-2GB	CT, IT, AT	BGA, VFBGA, SODIMM, UDIMM
	MT48 SDRAM	3.3V	x8, x16, x32	133 to 167 MHz	64-256Mb; 256-512MB	CT, IT, AT	TSOP, BGA, VFBGA, SODIMM, UDIMM, Wafer
Mobile DRAM	MT53 LP DDR4	1.1V	x32	1600 MHz	8-16Gb	IT, AIT, AAT	BGA
	MT42 LP DDR2	1.2V	x16, x32	333 to 533 MHz	512Mb-8Gb	IT, AT	BGA, PoP, KGD
	MT46 LP DDR1	1.8V	x16, x32	166 to 200 MHz	512Mb-4Gb	IT, AT	VFBGA,PoP, KGD
MCPs	NAND + LP DDR2 MCPs	1.8V	x8 NAND x16, x32 LPDDR2	333-533Mhz 4-bit ECC	1-4Gb 100k SLC NAND Flash 512Mb-2Gb LP DDR2	IT	TFBGA, VFBGA
	NAND + LP DDR1 MCPs	1.8V	x8, x16 NAND x16, x32 LPDDR1	166-200Mhz 4-bit ECC	1-4Gb 100k SLC NAND Flash 512Mb-2Gb LP DDR1	IT	TFBGA, VFBGA
	NOR + PSRAM MCPs	1.8V	x16 NOR x16 PSRAM	66-133MHz no ECC	32-512Mb NOR Flash 16-128Mb PSRAM	IT	TFBGA, VFBGA
mNAND	SSD (MLC NAND Flash)	3.3, 5V		SATA III	60-240 GB	IT	2.5", mSATA
	eMMC (MLC NAND Flash)	3V	x1, x4, x8	MMC4.41, 4.51, 5.0	4-64GB	IT	FBGA, TFBGA
	SPI SLC NAND Flash	1.8, 3V	x1, x2, x4	50MHz on die ECC	1-4Gb 100k SLC NAND 1-4Gb 60k SLC NAND	IT	TSOP, TBGA, DFN, SO16
SLC NAND	MT29F NAND SLC VLP Flash	1.8, 3V	x8	8, 24-bit ECC	4GB-8GB 30k SLC NAND 4Gb-4GB 60k SLC NAND	IT	TSOP, VFBGA, Wafer
	MT29F NAND SLC LP Flash	1.8, 3V	x8, x16	4-bit or on-die (zero) ECC	1-16Gb 100k SLC NAND	IT	TSOP, VFBGA, Wafer
Parallel NOR	G18 NOR Flash	1.8V	x16	133MHz, burst	256Mb-1Gb	IT, AT	ezBGA, KGD
	MT28EW/M29EW NOR Flash	3V	x8, x16	Asynch	64Mb-2Gb	IT	TSOP, FBGA, BGA, KGD
SPI NOR	MT25T Serial Flash	1.8, 3V	x1, x8	80-166MHz	256Mb-1Gb	IT, AT	SO16, TBGA24
	MT25Q/N25Q Serial Flash	1.8, 3V	x1, x2, x4	108-133MHz	8Mb-2Gb	IT, AT	DFN, SOP, TBGA24, CSP, KGD

Added Product Line

Added Product Line

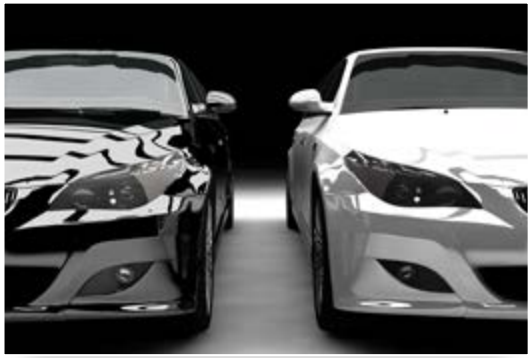
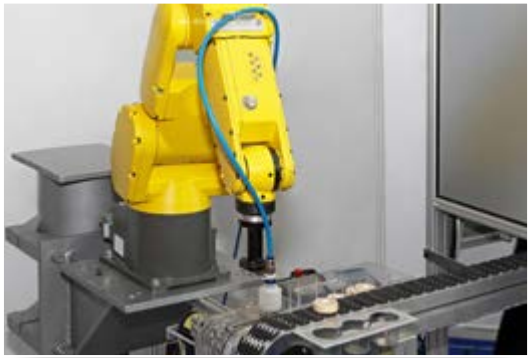
Added Product Line

Temp Range: CT [0 to +95C]; WT [-25 to +85C], IT [-40 to +85 C]; AT [-40 C to 105 C]

Design in products only, legacy product support covered in 5 year confidential roadmaps

Product **Longevity** Program

Product **Longevity** Program

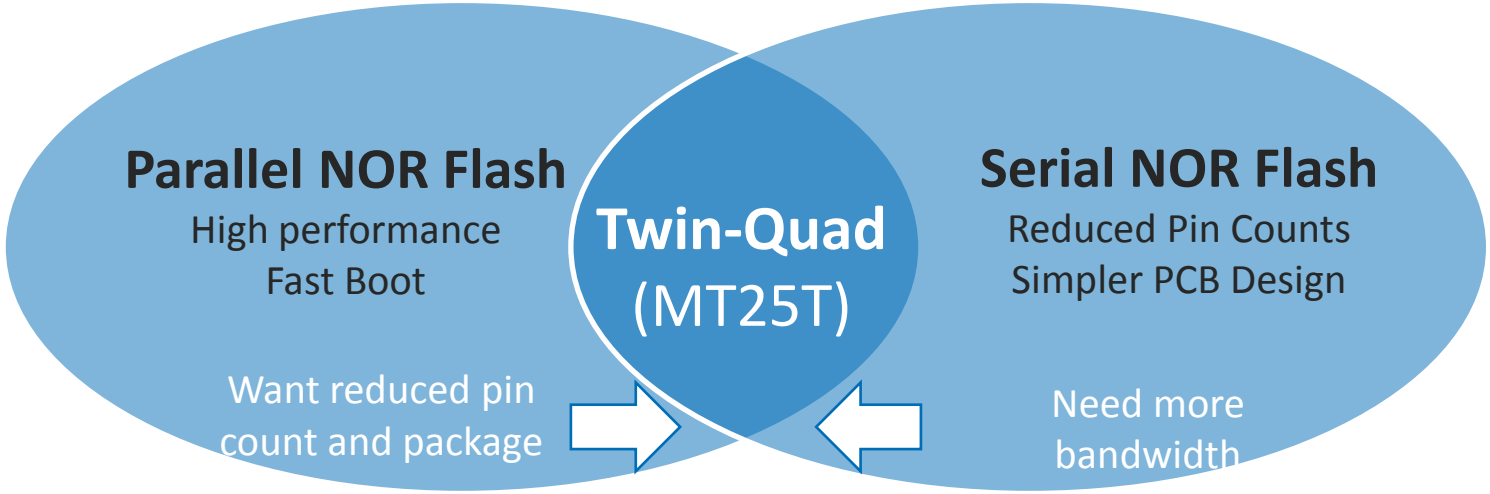

Customer Needs	Micron PLP
Longevity	Minimum **10-years** support after DOI (PLP Date of Introduction) assuring form, fit & function
Stability	**2-years** product change notifications (PCNs) ▪ 1 year to last-time buy (LTB) ▪ 1 year to last-time shipment (LTS) Only in case of ordering MPN changes

Longevity commitment (DOI) remains the same regardless of PCNs, conversions, and/or part number changes

For more details: www.micron.com/PLP

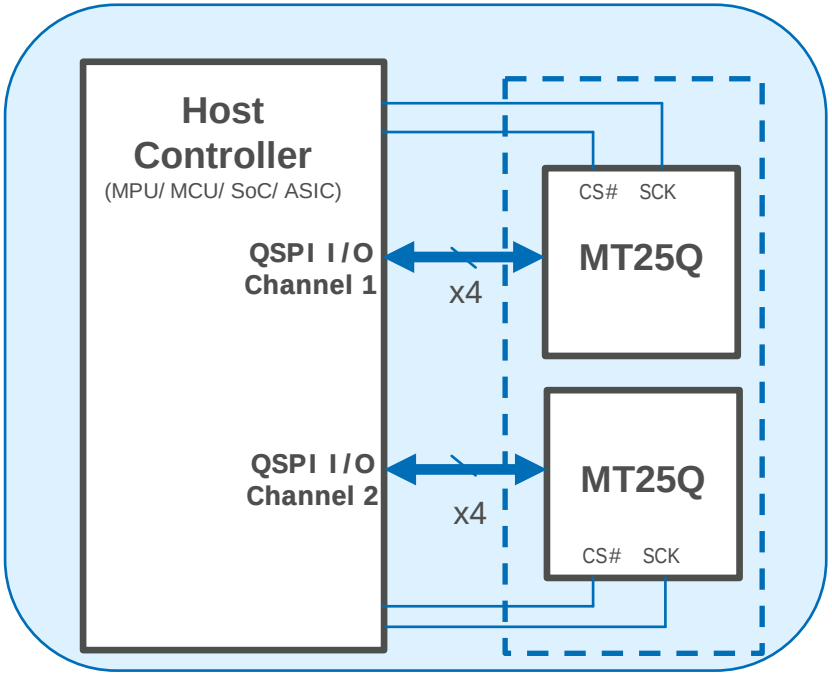
Non Volatile update

Trends and futures of NOR Flash

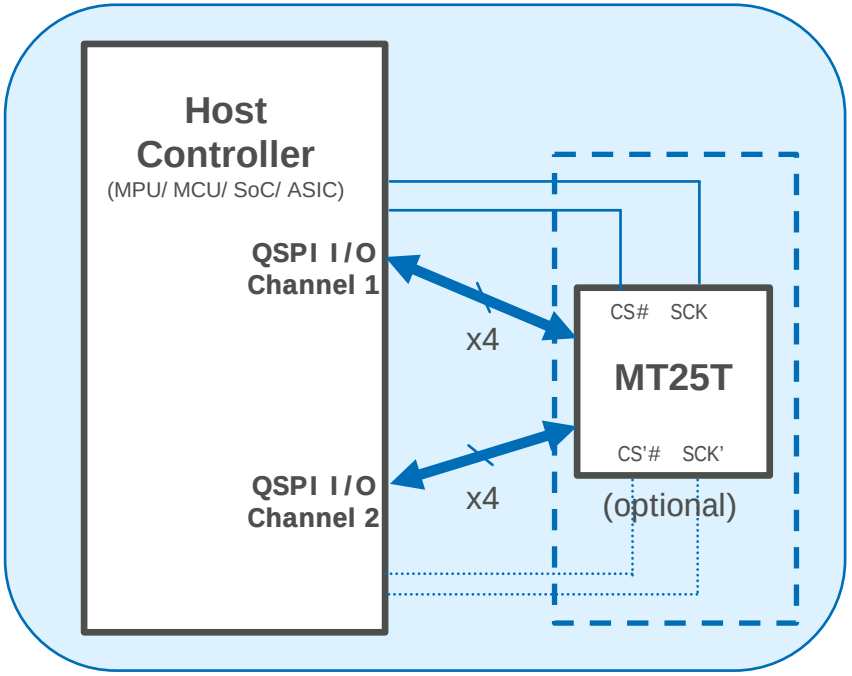


	M28EW Parallel NOR	N25Q, MT25Q Quad SPI	MT25T Twin Quad
Read Bandwidth	83MB/s (page mode)	83MB/s	166MB/s (2x MT25Q)
Access Time	95ns	~ 140ns; 125ns (1.8V)	Same as MT25Q
Package	FBGA-64 (13x11mm) TSOP-56 (14x20mm)	BGA24 (6x8x1.2 mm) SO16W (10.3x10.3x2.65 mm)	BGA24 (6x8x1.2 mm) SO16W (10.3x10.3x2.65 mm)
# of signal pins	48	6	10-12
Densities offered	64Mb – 2Gb	8Mb – 2Gb	256Mb – 1Gb

Twin-Quad Enables Easy Migration from Quad-I/O



Option A



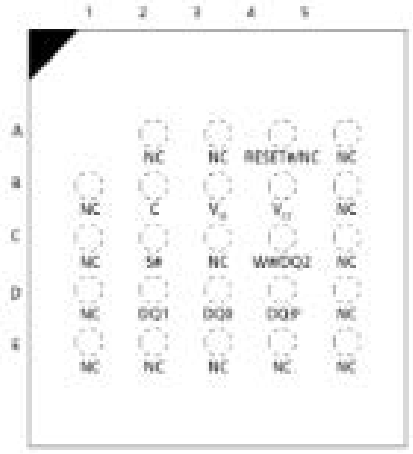
Option B

Host controllers with two quad-I/O channels to interface with separate quad-I/O devices simultaneously can instantly benefit

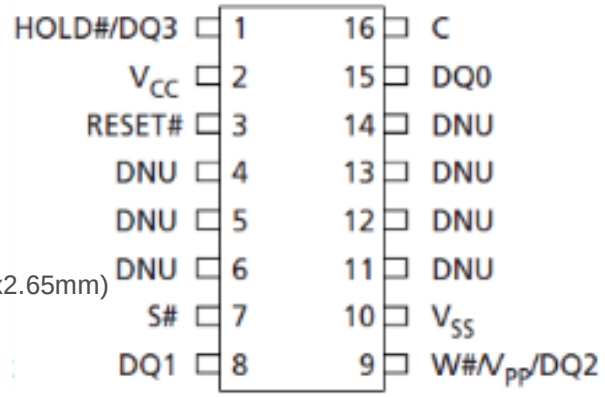
Twin-Quad Backward Compatible with Quad-I/O

MT25Q
Single Quad SPI

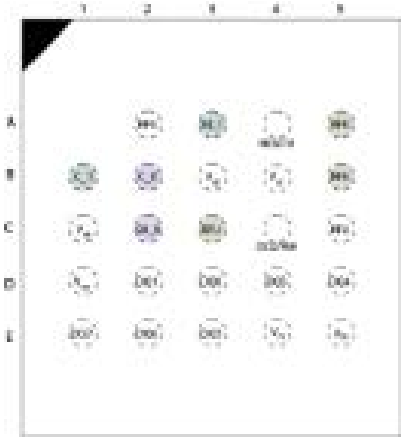
TBGA 24b
(6x8x1.2 mm)

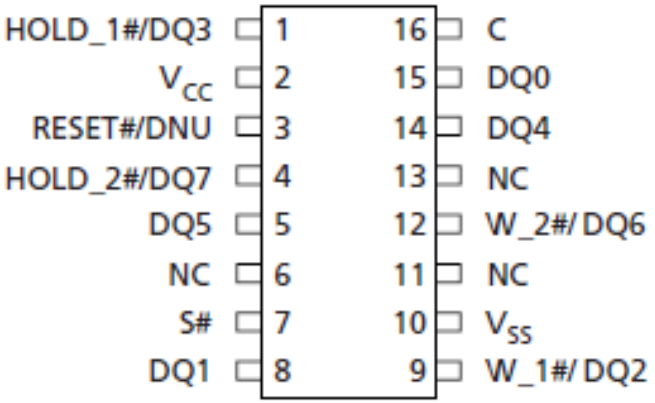


SO16W
(10.3x10.3x2.65mm)



MT25T
Twin-Quad SPI



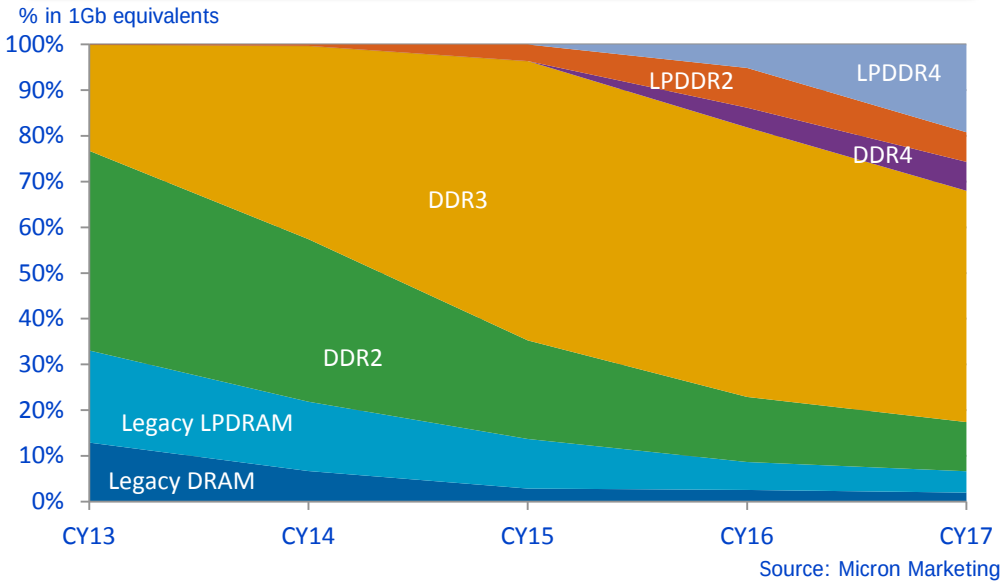


MT25T takes advantage of no connect balls/pins of MT25Q BGA/SOIC to keep the same ball/pin count and footprint

Automotive

Automotive LPDRAM Overview

DRAM Market Adoption by Technology



Source: Micron Marketing

Market Trends

Increasing LPDRAM Usage

- LPDRAM used in multiple applications
  - Instrument Cluster
  - Infotainment
  - ADAS
- Skipping LPDDR3 & moving to LPDDR4
- Increasing MCP adoption in communication modules

LPDRAM Requirements

Zero Defect Target Approach

- Burn in required to lower DPM rate
- Material selection for Auto grade devices

Extended Operating Temperatures

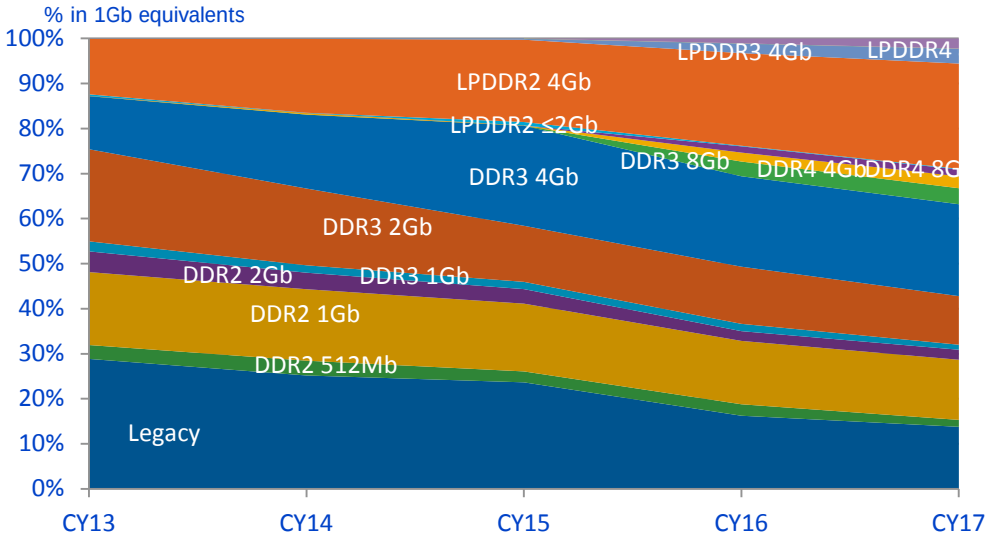
- From -40C up to 125C for next gen devices

Product Longevity

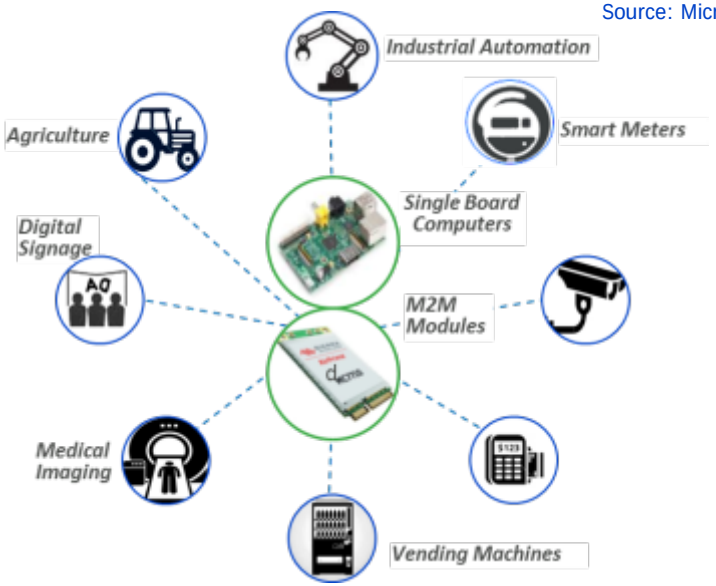
- Formal Product Longevity Program (PLP)
  - Support for 10 years & beyond
- Extended transition times for die shrinks
  - 1 year Last Time Buy + 1 year Last Time Ship

Industrial LPDRAM Overview

DRAM Market Adoption by Technology



Source: Micron Marketing



Market Trends

Wide Mix of DRAM Technology

- Continued need for legacy support

Strong LPDRAM Adoption

- Driven by battery driven applications
- Minimal LPDDR3 adoption projected (follows Auto LPDRAM adoption trends)
  - LP3 adoption driven by mobile CSVs branching into adjacent IMM markets (i.e. Qualcomm)

LPDRAM Requirements

Product Longevity

- Formal Product Longevity Program (PLP)
  - Support for 10 years & beyond
- Proven record of long term support

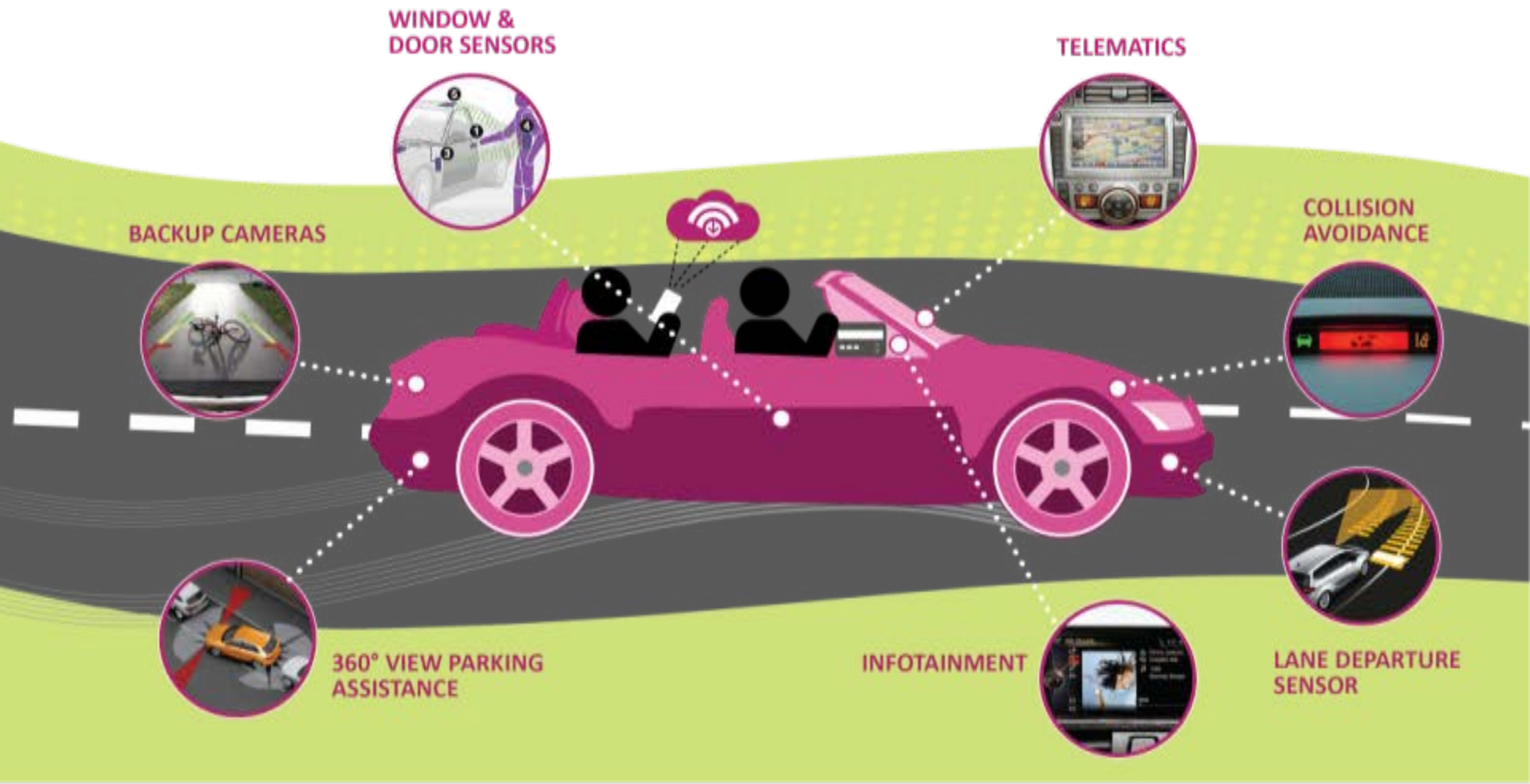
Extended Operating Temperatures

- IT grade components enable systems to operate in harsh environments

Broad portfolio for many applications

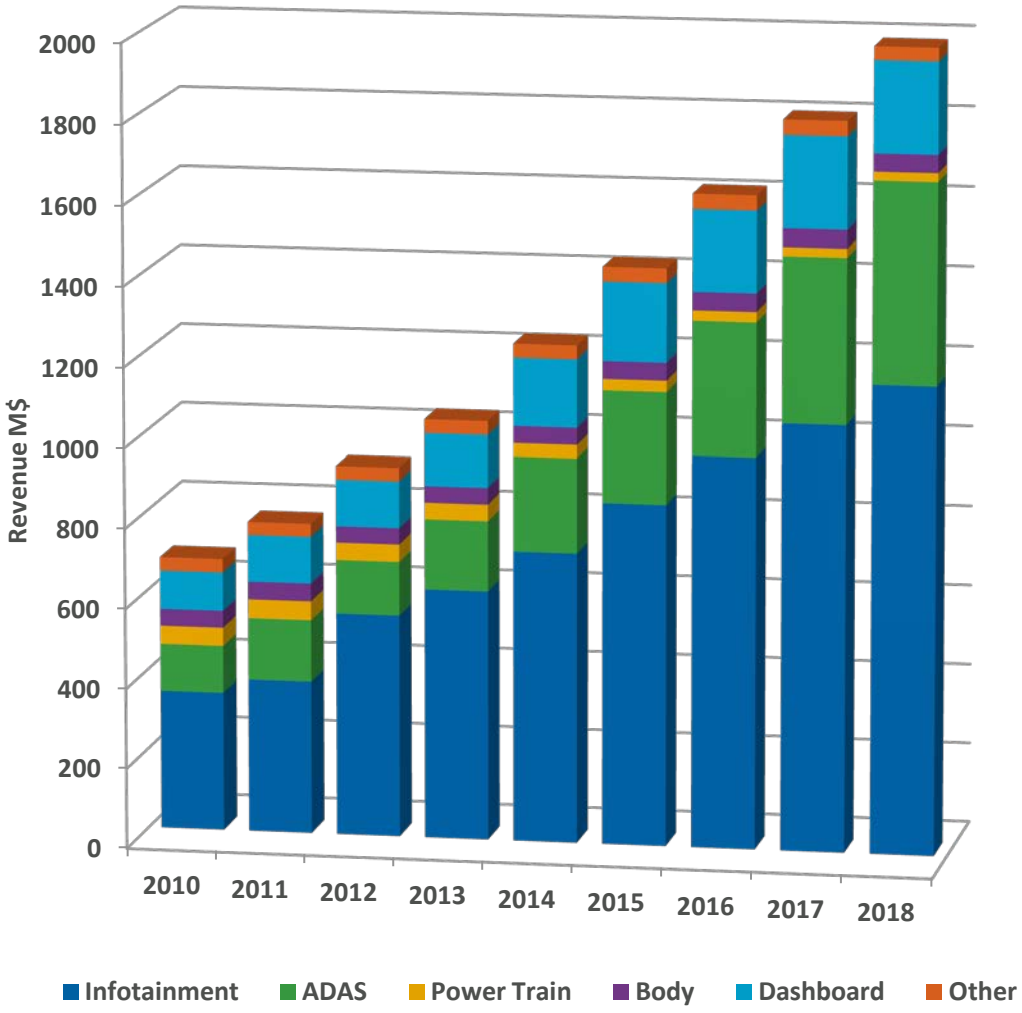
- Lower density offerings (i.e. 4Gb LP3)
- Increasing MCP and PoP adoption

The Connected & Smart Automobile



 |

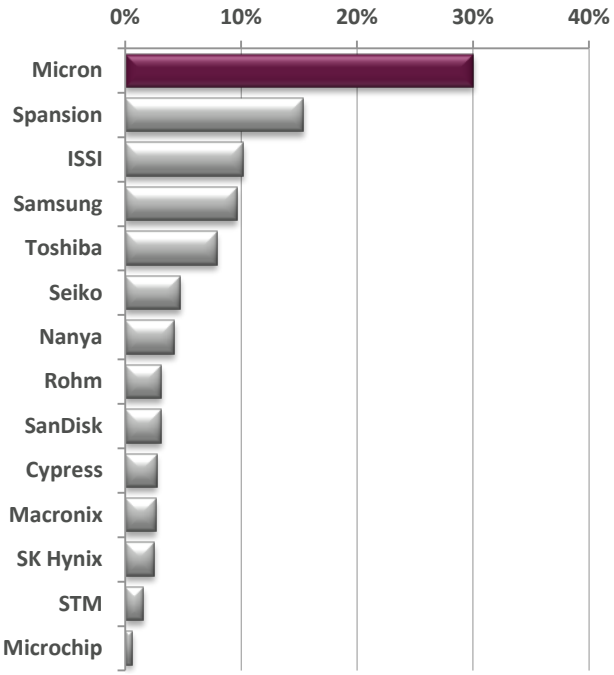
Market and Positioning



Reference: Micron MM rev20

2014 Micron Auto Memory Facts

- WW global car volumes of ~ 83.5Mu
- Statistically each car produced has **2.5 memory parts of Micron** inside
- **13% of new cars** use Micron eMMC, with **about 10GB** in average
- **One component** of Micron's raw flash (NAND/NOR) in each new car
- **1.5Gb of Micron DRAM** per car has hit the road



Gartner report 2014

Infotainment – Then and Now

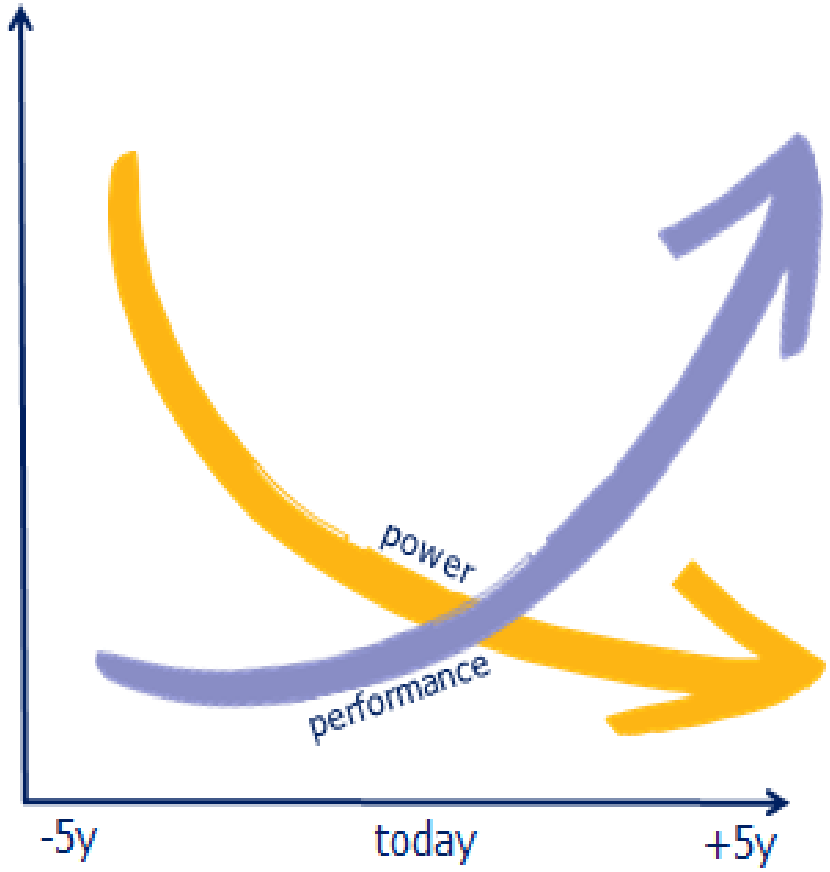
Non-Volatile Memory

-5 years	now	+3 years
• Code: ~256Mb pNOR • Mass storage: 2Gb SLC to 32GB HDD	• Code: 1Gb pNOR or in eMMC • Mass storage: 4GB to 64GB eMMC, up to 240GB HDD	• Code: up to 2Gb NOR or in eMMC • Mass storage: 4GB to 128GB eMMC, up to 480GB SSD
• DRAM: up to 1GB DDR2	• DRAM: up to 4GB DDR3	• DRAM: up to 8GB LPDDR4

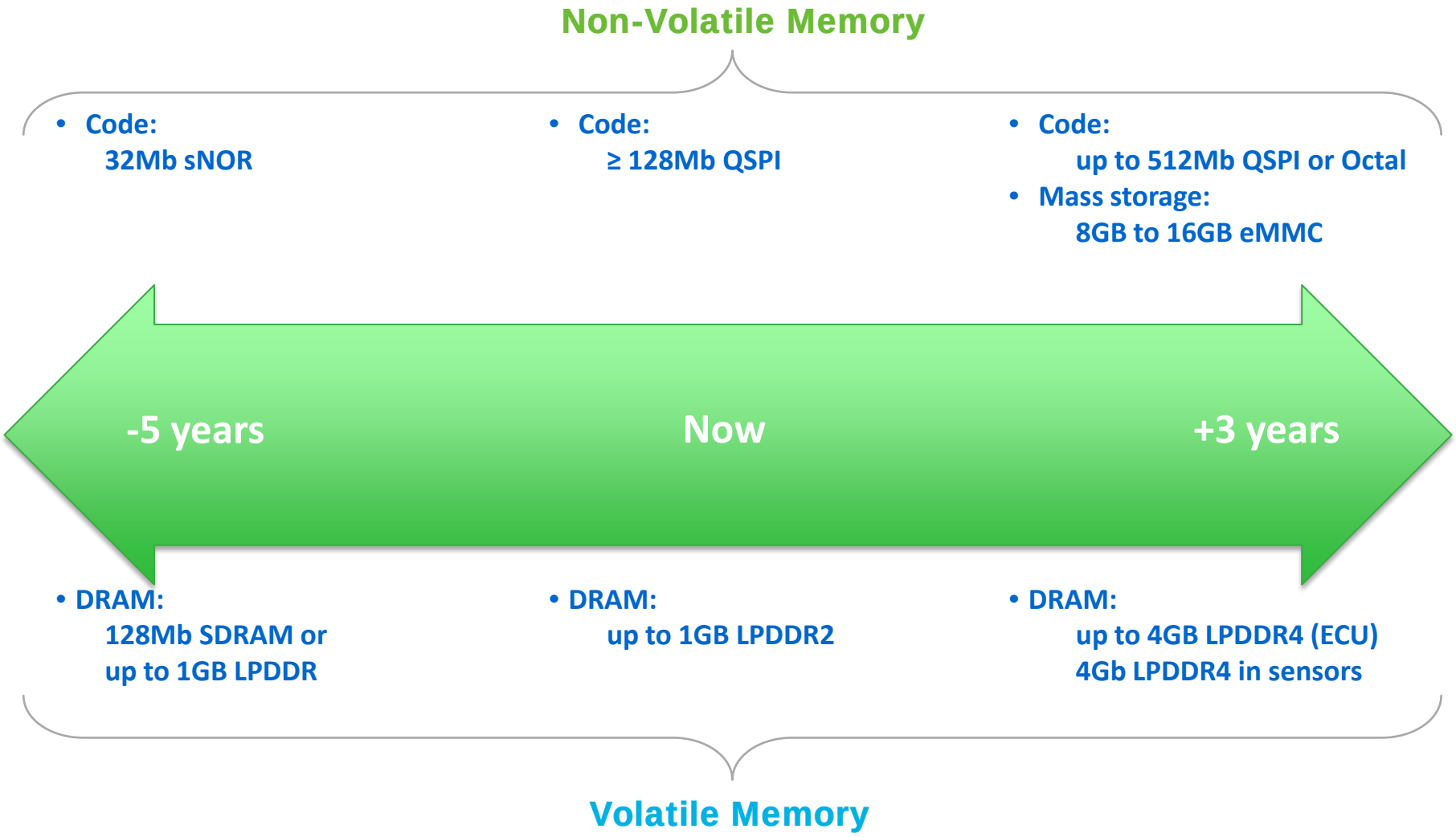
Volatile Memory

Infotainment Care Abouts

- Always-on/Instant-on requirements driving adoption of high speed & low-power solutions
- Increasing Functionality & HD display driving very high speed, high bandwidth DRAM needs
- Storage growth reaches ½ Terabyte in high end
- Leading-edge technology required to meet platform needs



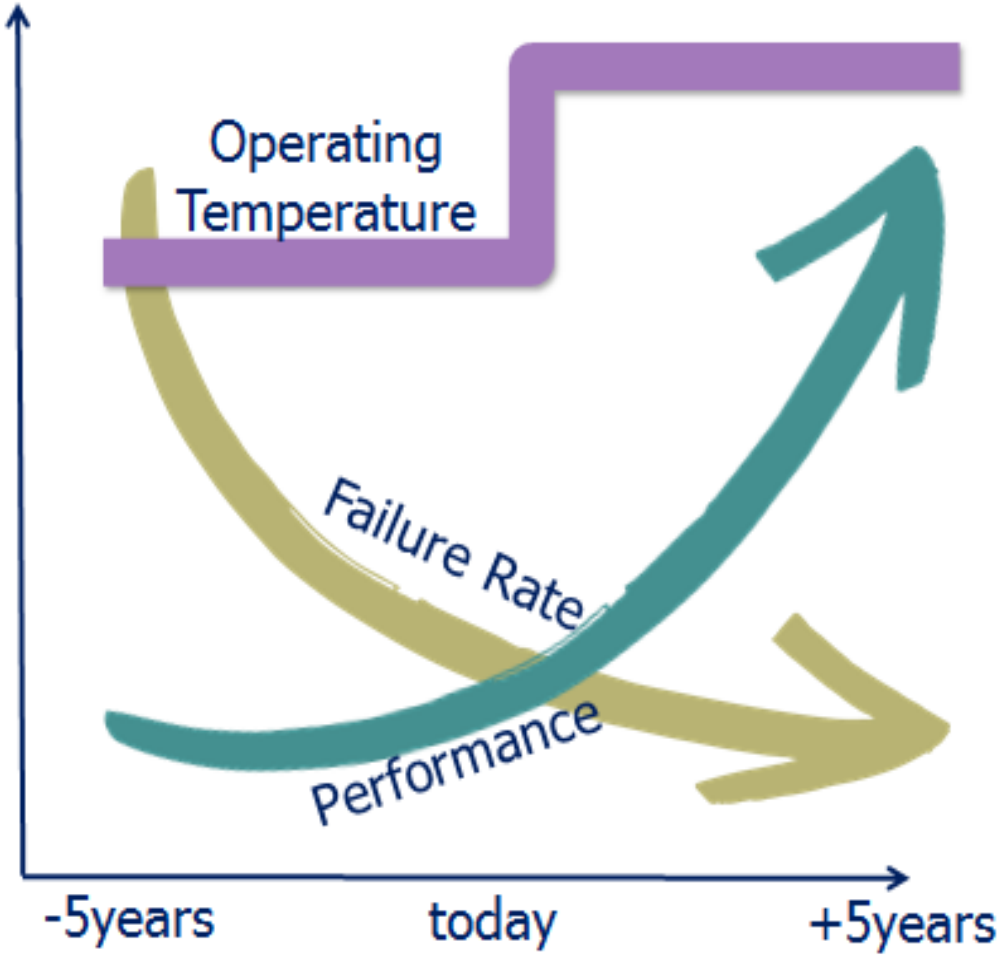
ADAS – Then and Now



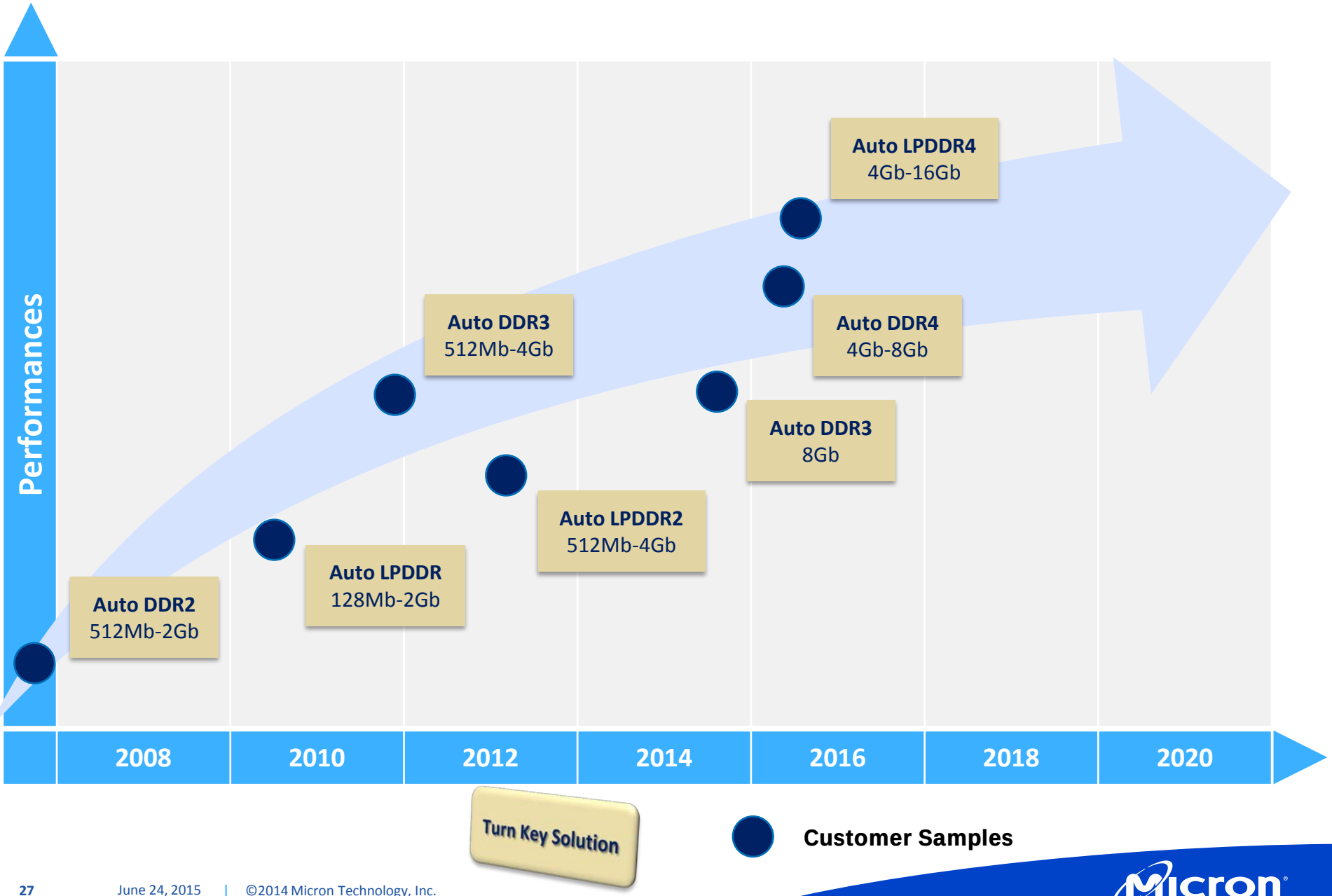
ADAS Care Abouts

Micron UHT targets:
+125C for DRAM and NOR
+105C for NAND and eMMC

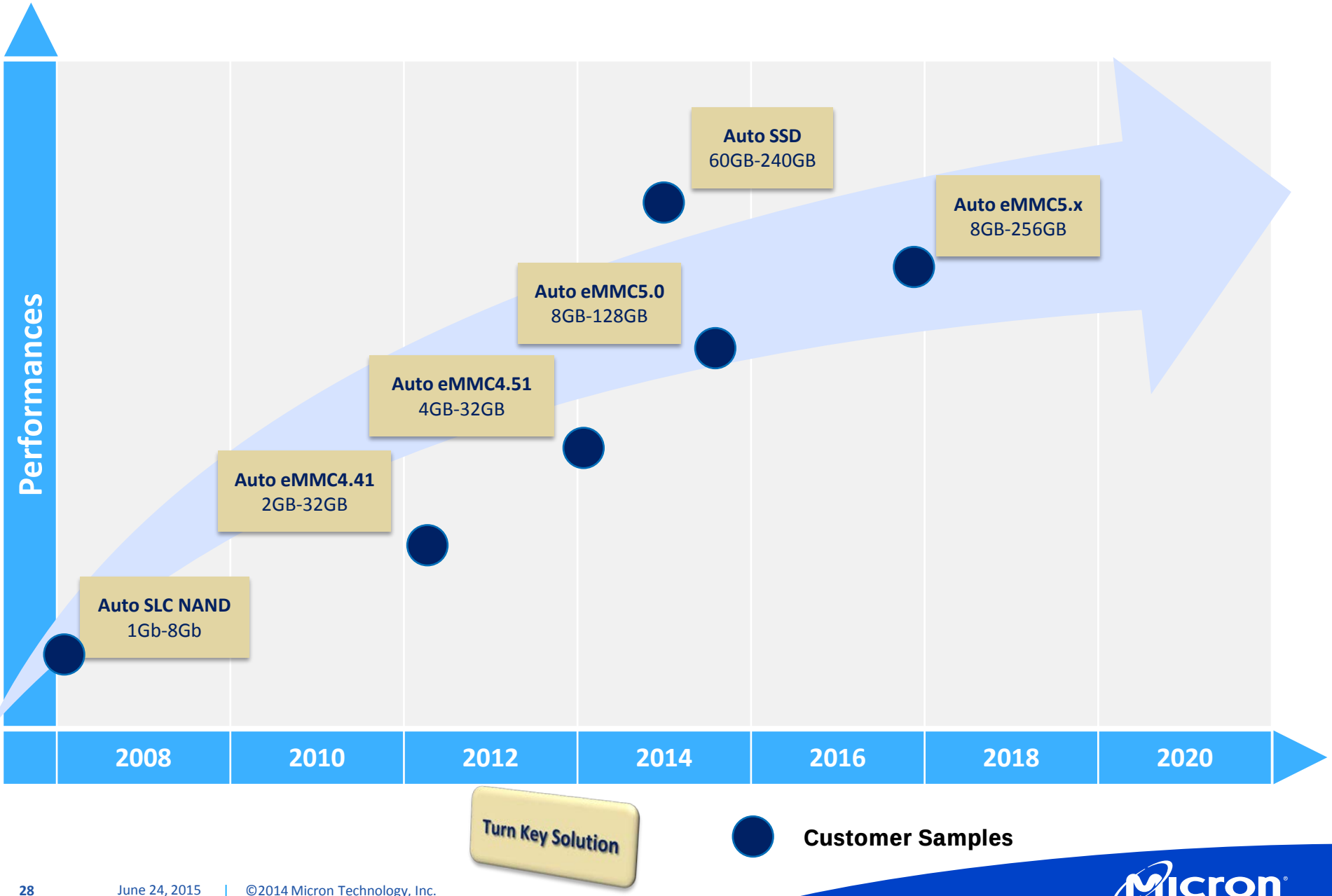
- Always-on/Instant-on requirements driving adoption of high speed & low-power solutions
- Overall system form factor and positioning in the car driving for +125C operating temperature
- System Safety and ASIL requirements driving for ECC
- Small form factor of camera sensors driving for higher integration (MCP)



Market Entry Points: Automotive DRAM Solutions



Market Entry Points: Automotive Mass Storage Solutions



Why LPDRAM?

Performance	• LPDDR4 peak bandwidth 33% faster compared to DDR4
Optimization	• For certain low density applications LPDDR offers BOM savings due to x32 configuration
Power Consumption	• Five times lower power consumption in standby mode compared to standard DRAM
Space, Form Factor & Weight	• Available in Multi Chip Package (MCP)/Package on Package (POP) which saves PCB space

LPDDRx and DDRx SDRAM Feature Comparison

Type	LPDDR2	LPDDR3	LPDDR4	DDR2	DDR3/DDR3L	DDR4
Die Density	Up to 8Gb	Up to 32Gb	Up to 32Gb	Up to 2Gb	Up to 8Gb	Up to 16Gb (128Gb 8H)
Prefetch Size	4n	8n	16n	4n	8n	8n
Core Voltage (Vdd)	1.2V 1.8V WL supply req.	1.2V 1.8V WL supply req.	1.1V/1.0V 1.8V WL supply req.	1.8V 1.55V	1.5V/1.35V	1.2V Separate WL supply 2.5V
I/O Voltage	1.2V	1.2V	1.1V/1.0V	Same as VDD	Same as VDD	Same as VDD
Max Clock Freq. /Data rate	533MHz/DDR1066	800MHz/DDR1600	2133MHz/DDR4267	533MHz/DDR1066	1066MHz/DDR2100	1600MHz+/DDR3200+
Burst Lengths	4, 8, 16	8	16, 32	4, 8	BC4, 8	BC4, 8
Configurations	x16, x32	x16, x32	2Ch x16	x4, x8, x16	x4, x8, x16	x4, x8, x16, x32
Address/ Command Signals	14 pins (Mux'd command address)	14 pins (Mux'd command address)	10 pins per channel (Mux'd command Address)	25 pins	27 pins	29 pins (partial mux'd)
Address/ Command Data Rate	DDR (both rising and falling edges of clock)	DDR (both rising and falling edges of clock)	SDR (rising edge of clock only)	SDR (rising edge of clock only)	SDR (rising edge of clock only)	SDR (rising edge of clock only)
On Die Temperature Sensor	Yes	Yes	Yes	No	Optional/RS	Yes
PASR (Partial-array self refresh)	full, half, quarter-array with individual bank and segment masking for partial-bank modes	individual bank and segment masking for partial-bank modes	individual bank and segment masking for partial-bank modes	optional feature only - full, ¾, half, ¼, 1/8 array, if supported	optional feature only - full, ¾, half, ¼, 1/8 array, if supported	Removed by JEDEC
Drive Strength	34-ohm 40-ohm 48-ohm 60-ohm 80-ohm 120-ohm ZQ calibration for +/- 10% accuracy	34-ohm 40-ohm 48-ohm ZQ calibration for +/-10% accuracy	Low-voltage swing terminated logic (LVSTL) VSSQ terminated	18-ohm (full) 34-ohm (half)	34-ohm 40-ohm ZQ calibration for +/- 10% accuracy	34-ohm 40-ohm TBD-ohm ZQ calibration for +/-10% accuracy
Per Bank Refresh	Yes (8-bank devices only)	Yes	Yes, with directed per-bank refresh	No	No	Fine Granularity Refresh (1x, 2x, 4x)
Output Driver	HSUL_12	HSUL_12	LVSTL_11/LVSTL_10	SSTL_18	"SSTL_15"	POD_12
DPD (Deep power-down mode)	Yes	Yes	No	No	No	No
DLL/ODT	No/No	No/Yes	No/Yes	Yes/Yes	Yes/Yes	Yes/Yes
Package Options	POP, MCP, discrete	POP, MCP, discrete	PoP, MCP, discrete	Discrete	Discrete	Discrete
Product/Temperature Grades	CT,IT,AIT, AT,AAT	CT,IT,AIT, AT,AAT	WT (-25' to 85'C) AT (-40'C to 105'C)	CT,IT,AIT, AT,AAT	CT,IT,AIT, AT,AAT	CT,IT,AIT, AT,AAT

DRAM Temperature Ranges

Temp	Tc	Comments
CT	0°C to +85°C	Commercial Temperature range[1]
IT	-40°C To +95°C	Industrial Temperature range *(+85C for mobile applications)*
A IT	-40°C to +95°C	= IT + package burn in (for automotive product certification)
AT	-40°C to +105°C	Automotive Temperature range
A AT	-40°C to +105°C	=AT + package burn in (for automotive product certification)

1. Auto temperature (AT) is not the same as Auto grade (see Automotive section on www.micron.com for details)
2. Auto grade (AAT/AIT) components follow rigorous AECQ100 standards for quality, reliability, fab/BOM control and PPAP.

Automotive Certification Value Added for DRAM

		- IT	- AIT	- AAT
QUALITY & RELIABILITY	Temperature Range	-40...+85C (+95C for DDR2/DDR3)	-40...+85C (+95C for DDR2/DDR3)	-40...+105C
	AEC-Q 100 qualification	under gap report	under gap report (continuous improvements to reduce gaps)	under gap report (continuous improvements to reduce gaps)
	Burn-In	not for LPDRAM	Yes	Yes
	Material Restriction for better production grading	No	Yes	Yes
	ISO/TS certified Fab and Assembly location	possible	Yes (according to certification roadmap)	Yes (according to certification roadmap)
SUPPORT	Failure analysis (8D report) response	No, Standard Analysis Report	yes, according to 1-2-10 rule	yes, according to 1-2-10 rule
SERVICE	PPAP submission	No	Yes	Yes
	Supply prioritization	No	Yes	Yes
	Buffer stock/ CMI/ VMI	No	Can be negotiated	Can be negotiated
	Documentation support (questionnaires)	Submission of Micron‘s Internal Qualification and Reliability Report under NDA	full questionnaire support	full questionnaire support
	Fab and assembly audit support	ISO 9001 (limited)	ISO/TS 16949 (full)	ISO/TS 16949 (full)

DDR3 SDRAM

MT41J512M4 – 64 Meg x 4 x 8 Banks
MT41J256M8 – 32 Meg x 8 x 8 Banks
MT41J128M16 – 16 Meg x 16 x 8 Banks

Features

- $V_{DD} = V_{DDQ}$ = 1.5V ±0.075V
- 1.5V center-terminated push/pull I/O
- Differential bidirectional data strobe
- 8*n*-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS READ latency (CL)
- Posted CAS additive latency (AL)
- Programmable CAS WRITE latency (CWL) based on ^tCK
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- T_C of 0°C to 95°C
  - 64ms, 8192 cycle refresh at 0°C to 85°C
  - 32ms, 8192 cycle refresh at 85°C to 95°C
- Self refresh temperature (SRT)
- Write leveling
- Multipurpose register
- Output driver calibration

Options[1]

Options[1]	Marking
• Configuration	
– 512 Meg x 4	512M4
– 256 Meg x 8	256M8
– 128 Meg x 16	128M16
• FBGA package (Pb-free) – x4, x8	
– 78-ball (8mm x 10.5mm) Rev. H,M,J,K	DA
– 78-ball (9mm x 11.5mm) Rev. D	HX
• FBGA package (Pb-free) – x16	
– 96-ball (9mm x 14mm) Rev. D	HA
– 96-ball (8mm x 14mm) Rev. K	JT
• Timing – cycle time	
– 938ps @ CL = 14 (DDR3-2133)	-093
– 1.071ns @ CL = 13 (DDR3-1866)	-107
– 1.25ns @ CL = 11 (DDR3-1600)	-125
– 1.5ns @ CL = 9 (DDR3-1333)	-15E
– 1.87ns @ CL = 7 (DDR3-1066)	-187E
• Operating temperature	
– Commercial (0°C ≤ T_C ≤ +95°C)	None
– Industrial (–40°C ≤ T_C ≤ +95°C)	IT
• Revision	:D/:H/:J/:K/:M

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target ^tRCD-^tRP-CL	^tRCD (ns)	^tRP (ns)	CL (ns)
-093[1, 2, 3, 4]	2133	14-14-14	13.09	13.09	13.09
-107[1, 2, 3]	1866	13-13-13	13.91	13.91	13.91
-125[1, 2]	1600	11-11-11	13.75	13.75	13.75
-15E[1]	1333	9-9-9	13.5	13.5	13.5
-187E	1066	7-7-7	13.1	13.1	13.1

Notes: 1. Backward compatible to 1066, CL = 7 (-187E).
2. Backward compatible to 1333, CL = 9 (-15E).
3. Backward compatible to 1600, CL = 11 (-125).
4. Backward compatible to 1866, CL = 13 (-107).

Automotive DDR3 SDRAM

MT41J256M8 – 32 Meg x 8 x 8 Banks
MT41J128M16 – 16 Meg x 16 x 8 Banks

Features

- Industrial and automotive temperature compliant
- $V_{DD} = V_{DDQ}$ = 1.5V ±0.075V
- 1.5V center-terminated push/pull I/O
- Differential bidirectional data strobe
- 8*n*-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS READ latency (CL)
- Posted CAS additive latency (AL)
- Programmable CAS WRITE latency (CWL) based on ^tCK
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- T_C of –40°C to +95°C/+105°C
  - 64ms, 8192 cycle refresh at 0°C to +85°C
  - 32ms, 8192 cycle refresh at +85°C to +95°C/+105°C
- Self refresh temperature (SRT)
- Write leveling
- Multipurpose register
- Output driver calibration
- AEC-Q100
- PPAP submission
- 8D response time

Options[1]

Options[1]	Marking
• Configuration	
– 256 Meg x 8	256M8
– 128 Meg x 16	128M16
• FBGA package (Pb-free) – x8	
– 78-ball (9mm x 11.5mm) Rev. D	HX
• FBGA package (Pb-free) – x16	
– 96-ball (9mm x 14mm) Rev. D	HA
• Timing – cycle time	
– 1.07ns @ CL = 13 (DDR3-1866)	-107
– 1.25ns @ CL = 11 (DDR3-1600)	-125
– 1.5ns @ CL = 9 (DDR3-1333)	-15E
– 1.87ns @ CL = 7 (DDR3-1066)	-187E
• Product certification	
– Automotive	A
• Operating temperature	
– Industrial (–40°C ≤ T_C ≤ +95°C)	IT
– Automotive (–40°C ≤ T_C ≤ +105°C)	AT
• Revision	:D

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target ^tRCD-^tRP-CL	^tRCD (ns)	^tRP (ns)	CL (ns)
-107[1, 2]	1866	13-13-13	13.91	13.91	13.91
-125[1, 2]	1600	11-11-11	13.75	13.75	13.75
-15E[1]	1333	9-9-9	13.5	13.5	13.5
-187E	1066	7-7-7	13.1	13.1	13.1

Notes: 1. Backward compatible to 1066, CL = 7 (-187E).
2. Backward compatible to 1333, CL = 9 (-15E).


Micron®
Focused on Memory | Engineered for your Innovation

Technical Notes

Mike, I think we should add as many TN's as makes sense across all products.

Power calculator (www.micron.com/products/support/power-calc)

TN-41-13 DDR3 point-to-point design support

E0593E20 Technical Note: New function of DDR2 SDRAM – On die termination (ODT)

TN-41-13 DDR3 point to point design support

TN-41-03 Calculating Memory System Power for DDR3

TN-41-08 Design guide for two DDR3-1066 UDIMM systems

TN-41-01 Calculating Memory System power for DDR3

TN-42-01 Calculating Memory System Power for LPDDR2

CSN34 PoP User guide

TN-00-15 Recommended soldering parameters

TN-00-06 Bypass Capacitor Selection

TN-00-08 Thermal Application (junction temp)

Quad-SPI NOR Flash

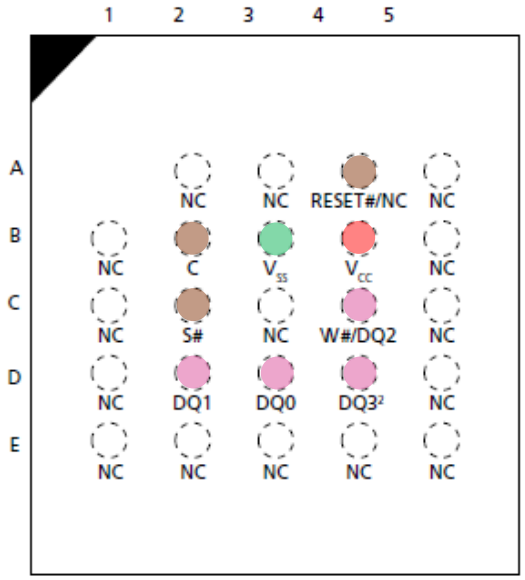
N25Q(65nm)

MT25Q (45nm)

= Data
= Control
= Power
= Ground

24 ball BGA

6 x 8 mm

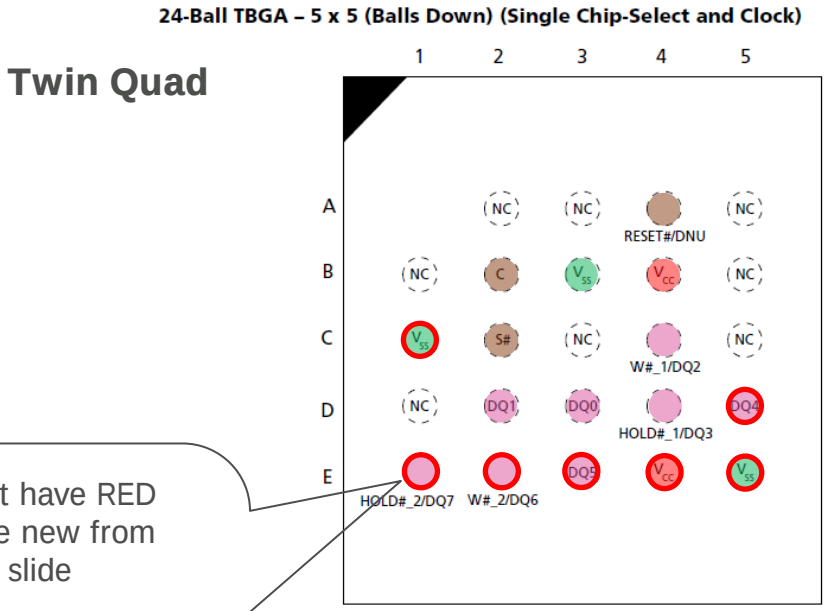


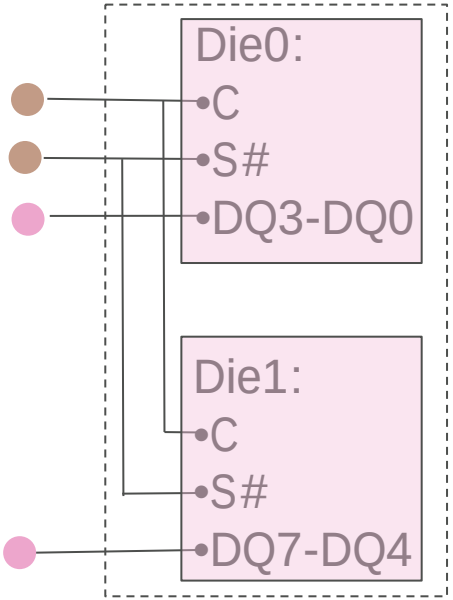
Only 6 signals Required

- C= Clock
- S#= Chip Select (Low)
- DQ= Data (3:0)
- Max clock = 166MHz
- Or **83MB/s**

BGA for Twin-Quad (1C, 1S#)

= Data
= Control
= Power
= Ground





Balls that have RED Circle are new from previous slide

Brings the signal total up to 10, but doubles the max read performance to 166MB/s

Package – BGA for Twin Quad (2C, 2S#)