56F801X/834X/832X/835X Product FIT

SUMMARY

The FIT data represented below comprises qualification activity used to make up generic data for the DSC 0.5µm SGF Product families.

High Temperature Operational Life and Supporting Stress Data

STRESS	READ POINT	Qty of DEVICES	Qty of REJECTS	% REJECTS
56F8013 HTOL @ 125°C	1008hrs	240	0	0.00
56F8013 HTOL @ 125°C	1008hrs	80	0	0.00
56F8013 HTS @ 150°C	1008hrs	240	0	0.00
56F8013 HTS @ 150°C	1008hrs	80	0	0.00
56F8013 125C W/E Cycles (Prior to HTSL and HTOL)	10k Cycles	All HTOL and HTSL above	0 0	0.00 0.00
56F8346 HTOL @ 150°C	2016hrs	482	0	0.00
9S12D64 Generic Data ELFR @ 125C	48hrs	3200	0	0.00
9S12D64 Generic Data (Prior to ELFR)	125C, 1k Flash 10K EE	3200	0	0.00
9S12D64 Generic Data EDR @ 150C	2016	780	0	0.00
9S12D64 Generic Data (Prior to EDR)	-40C, 10k Flash 100K EE	390	0	0.00
9S12D64 Generic Data (Prior to EDR)	125C, 10k Flash 100K EE	390	0	0.00

FIT rates are calculated based only on HTOL results provided above. This data has been documented on DSC product family qualification reports. Current FIT data stands at less than **3.8 FIT at 60% Upper Confidence Limit (9.6 FIT at 90% UCL)** confidence derated to 55°C Tj. Please note these FIT rates are limited by the upper confidence limit bounds due to sample size. There have been no failures. It should be noted that data collection of this family is ongoing at this time and the FIT is expected to decrease further as results are recorded.

DESCRIPTION OF STRESS TESTS

Early Life Fail Rate (ELFR)
125°C, 3.6V, 24 hours

The purpose of this stress is to characterise the early failure rate portion of the bathtub curve. Devices used in this test are sampled directly after the standard production final test flow with no prescreening. A dynamic electrical bias is applied to stimulate the device during the test in much the same way as HTOL below.

High Temperature Operational Life test (HTOL)
125°C, 3.6V, 1008 hours

To determine the constant failure rate of the product at the specified operating temperature (usually 70°C), by accelerating temperature and voltage-activated failure mechanisms to produce device failures.

A dynamic electrical bias is applied to stimulate the device during the life test. Microcontrollers are cycled through software routines, developed to stress the devices to simulate actual use, at elevated temperature and voltage. Reject quantities at the test temperature are modified by the Chi-squared distribution function at 90% confidence levels. The failure rates are then calculated and derated to the required temperature using the Arrhenius equation with a 0.54 eV activation energy assumed as an average for the failure mechanisms. Further details are given in 'Calculation of Failure Rates'.

CALCULATION OF FAILURE RATES

Life test is a technique for determining constant failure rate. To derate from the temperature at which the life test is carried out to the maximum operating temperature an acceleration factor is applied. This calculation uses the Arrhenius equation, with **0.54eV** assumed for the activation energy.

Temperature Acceleration Factor, **Aft = exp (θ/k (1/To - 1/Tt))**

Where: θ is activation energy (eV)
k is Boltzmann's constant (8.617 x 10^{-5} eV/K) (K = -273.16°C)
To = Ta (op) + (Pd x θja)
Tt = Ta (tst) + (Pd x θja)

And: Ta (op) is the ambient user operating temperature (K)
Ta (tst) is the ambient temperature on stress test (K)
Pd is power dissipated by the device (W)
θja is thermal resistance of the package (°C/W)

Rejects obtained in the sample must be modified at a stated confidence level to obtain the rejects which would occur were the entire population tested. This is done using the Chi-square distribution function.

Failure Rate, **Fa = Z / (2 x N x h x Aft)** where: Z is Chi-square ($\chi 2$) reject quantity
N is number of devices on test
h is test duration (hours)

* Fa is multiplied by 10^9 to give the result in FITS (1 FIT = 1 failure in 10^9 device hours).
* Fa is multiplied by 10^5 for % per 1000 hours.

$\chi 2$ value Z, is derived from statistical tables using (2 x Qty. fails + 2) for the Degrees of Freedom:

Qty fails	60% confidence level $\chi 2$ qty	90% confidence level $\chi 2$ qty
0	1.833	4.605
1	4.045	7.779
2	6.211	10.645
3	8.351	13.362
4	10.473	15.987
5	12.584	18.549
6	14.685	21.064
7	16.780	23.542
8	18.868	25.989
9	20.951	28.412

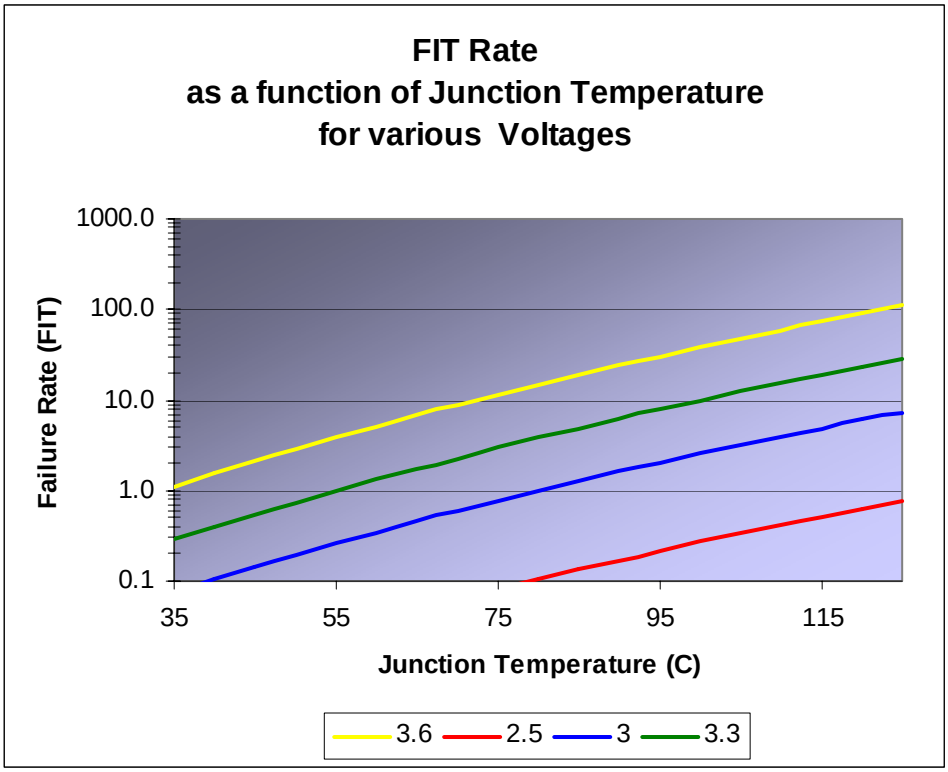
Voltage Acceleration is also taken into account when determining the life of devices. This is calculated by taking the oxide thickness into consideration and derating from the stress test voltage to the life operating voltage.

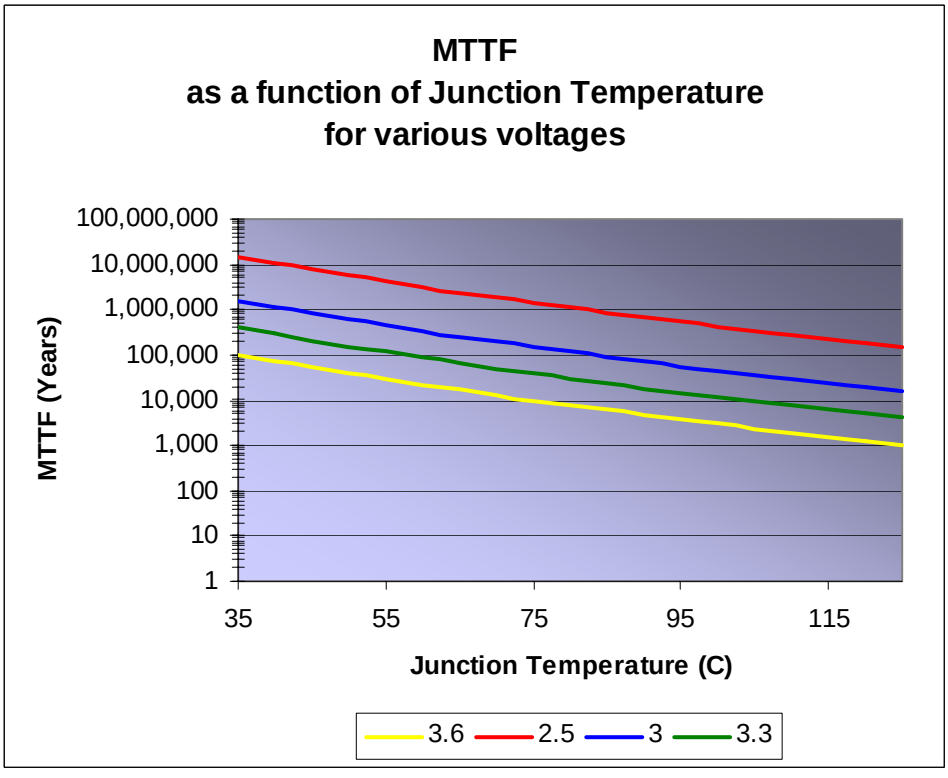
Voltage Acceleration Factor, **Afv = exp $^{\beta[Vt - Vo]}$**

Where:
Vo = Gate voltage under typical operating conditions (in Volts) *
Vt = Gate voltage under accelerated test conditions (in Volts) *
β = Voltage acceleration factor (in 1/Volts) **

** For devices with dual gate oxide, the thin gate oxide voltages are applicable.*
*** Specified by technology in the Reliability Model document 68MWS00084B.*

FIT and MTTF Curves, Based on HTOL Data only, using die size for 56F8013/8014





DESCRIPTION OF SOFT ERROR RATE DATA

Soft error described an event during which an energetic particle enters the Si substrate near a storage node. These atomic interactions result in a tunnel of charge in the wake of the particle. Sufficient charge drifts to the storage node to change its state. The final soft error is the loss of data at the storage node.

JEDEC specifies SER test and analysis procedures in JESD 89.

System-level Tests.

- Data in 1000 devices is monitored for > 1000 hours (2 months).
- Measure number of failures in 10e6 device-hours.
- Used to scale accelerated results to field conditions.

Accelerated Tests

- Data in 2 to 10 devices exposed to an accelerated source is monitored for a few minutes.
- Results are decelerated to operating conditions.
- Tests require little time to collect substantial data (10e8 acceleration).
- JEDEC standards for converting to operating conditions.
- Most SER characterization is performed with accelerated tests.

SUMMARY OF SOFT ERROR RATE DATA

The soft error data representing the DSC product 0.50u SGF technology will be added to this document.