TR1135

Rules and recommendations for in-vehicle CAN networks

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Summary

The intention of this document is to provide necessary information needed for network developers to design in-vehicle networks.

This document deals with items like the maximum number of nodes, the maximum bus line length and topology aspects. Especially the topology appears to have a significant influence on the system performance.

Achieving excellent EMC performance is not only a matter of the transceiver, a careful system implementation (termination, topology, external circuitry and PCB layout) is also very important.

Revision history

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1.0	24-Sep-12	Initial version

1. Introduction

CAN is the standard multi-master asynchronous serial protocol for in-vehicle networks.

Although the protocol is well understood the implementation of its physical layer, especially in larger networks is sometimes challenging. The increasing numbers of electronic control units combined with more individual sub-network stubs require a thorough network design. To assure a good system robustness and quality network simulations with worst case scenarios in an early stage of the developments should be performed.

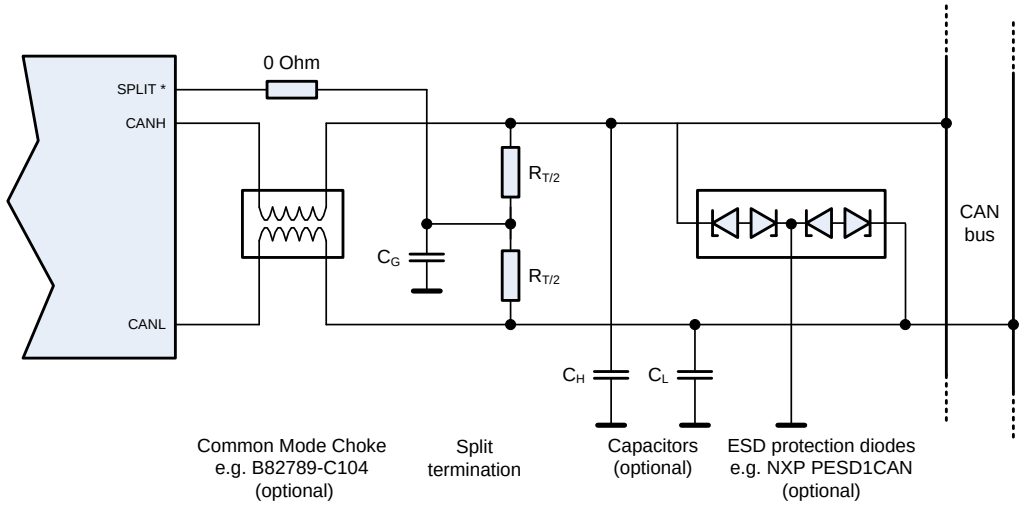
This document can be seen as collection of recommendations and hints on items like the maximum number of nodes, the maximum bus line length and topology aspects. Especially the network topology appears to have a significant influence on the system performance. Achieving excellent EMC performance is not only a matter of the transceiver, a careful system implementation (termination, topology, external circuitry and PCB layout) is also very important.

2. EMC aspects of high speed CAN

Achieving excellent EMC performance is not only a matter of the transceiver, a careful system implementation (termination, topology, external circuitry and PCB layout) is also very important.

The possibilities to improve the EMC performance further include differential and common mode filters, shielded twisted pair cable and ESD protections diodes. Additionally the PCB layout is also critical to maximize the effectiveness of the EMC improvement circuit. All additional circuits could distort the signal waveform and they are also limited by the physical layer specifications.

This chapter presents some application hints (all are referenced to Fig 1) aiming to exploit the outstanding EMC performance of NXP's high speed CAN transceivers.



* TJA1042, TJA1043 only.

General remark: A dedicated application may depend on specific OEM requirements.

Fig 1. Optional circuitry at CANH and CANL

2.1 Common mode choke

A common mode choke provides high impedance for common mode signals and low impedance for differential signals. Due to this, common mode signals produced by RF noise and/or by non-perfect transceiver driver symmetry get effectively attenuated while passing the choke. In fact, a common mode choke helps to reduce emission and to improve immunity against common mode disturbances without adding a large amount of distortion on CAN lines.

Hint: Common-mode chokes pass differential currents (equal but opposite), while blocking common-mode currents. With that, it forces the bus wires towards a symmetrical differential signal behavior for frequencies above about 20MHz. Common mode chokes

are not effective for lower frequencies. Thus, the low frequency signal symmetry is mainly defined by the used CAN transceiver and the overall network symmetry, which cannot be improved with the chokes.

Former transceiver products usually needed a common mode choke to fulfill the stringent emission and immunity requirements of the automotive industry when unshielded twisted-pair cable was used. NXP's entire 3rd generation high speed CAN transceivers have the potential to build in-vehicle bus systems even without chokes. Whether a choke is needed or not finally depends on the specific system implementation like the wiring harness (vehicle specific conditions / wire routing / antenna locations) and the symmetry of the two bus lines (matching tolerances of resistors and capacitors).

Besides the RF noise reduction the stray inductance (non-coupled portion of inductance) may establish a resonant circuit together with pin capacitance. This can result in unwanted oscillations between the bus pins and the choke, both for differential and common mode signals, and in extra emission around the resonant frequency. To avoid such oscillations, it is highly recommended to use only chokes with a lower stray inductance. Bifilar wound chokes typically show a lower stray inductance. Fig 1 shows an application using a common mode choke. As shown the choke shall be placed close to the transceiver bus pins.

2.2 Capacitors

Matching (in pairs) capacitors at CANH and CANL to GND (CH and CL) are frequently used to enhance immunity against electromagnetic interference. Along with the impedance of corresponding noise sources (RF), capacitors at CANH and CANL to GND form an RC low-pass filter. Regarding immunity the capacitor value should be as large as possible to achieve a low corner frequency. The overall capacitive load and impedance of the output stage establish a RC low-pass filter for the data signals. The associated corner frequency must be well above the data transmission frequency. This results in a limit for the capacitor value depending on the number of nodes and the data transmission frequency. Notice that capacitors increase the signal loop delay due to reducing rise and fall times. Due to that, bit timing requirements, especially at 500kbit/s and higher, call for a value of lower than 100pF (see also SAE J2284 and ISO11898). At a bit rate of 125kbit/s the capacitor value should not exceed 470pF per CAN node. Typically, the capacitors are placed between the common mode choke (if applied at all) and the optional ESD clamping diodes as shown in Fig 1.

2.3 ESD protection diodes

NXP's 3rd generation high speed CAN transceivers is designed to withstand ESD pulses of up to

- ±8kV according to the IEC61000-4-2 and
- ±8kV according to the Human Body Model
- ±300V according to the Machine Model
- ±500V according to the Charged Device Model

at bus pins CANH, CANL and pin SPLIT (TJA1042, TJA1043 only) and therefore, typically no further external measures are needed. Nevertheless, if much higher protection is required, external clamping devices can be applied to the CANH and CANL line.

NXP Semiconductors offers a dedicated protection device for the CAN bus, providing high robustness against ESD and automotive transients. The so-called PESD1CAN [5] and PESD2CAN [6] protection devices featuring a very fast diode structure with very low capacitance (typ. 11pF), is compliant to IEC61000-4-2 (level 4), thus allowing air and contact discharge of more than 15kV and 8kV, respectively. Tests at an independent test house have confirmed typically more than 20kV ESD robustness for ECUs equipped with the PESD1CAN and a choke. To be most effective the PESDxCAN diode shall be placed close to the connector of the ECU as shown in Fig 1.

2.4 Power supply buffering

Emission and immunity of transceivers also depend on dynamic behavior of signals. The capacitors placed at voltage supply pins buffer the voltage and provide the sharp rise current needed during the transition from recessive to dominant state.

Consequently it is recommended to make sure, that the VCC supply of a CAN transceiver is sufficiently filtered against noise as well as buffered with respect to load variations caused by sending dominant bits. This is, why it is not recommended to add transistors or other electronic switches within the VCC supply line of transceivers, in case this supply shall be switched on and off due to quiescent current requirements of an ECU. Instead, this VCC supply pin shall be directly driven by a suitable voltage regulator with an accuracy as defined within the data sheet of the used transceiver. Typically such an VCC pin should be equipped with a local buffer capacitor with about 10nF close to the pin. Details for the supply requirements can be found in the product specific application material.

2.5 Split termination concept

The transceiver is connected to the bus via pins CANH and CANL. Nodes connected to the bus end must show a differential termination, which is approximately equal to the characteristic impedance of the bus line in order to suppress signal reflection. Practice has shown that effective reduction of emission can be achieved by a modified bus termination concept called split termination. Instead of a one-resistor termination it is highly recommended using the split termination. In addition this concept contributes to higher immunity of the bus system.

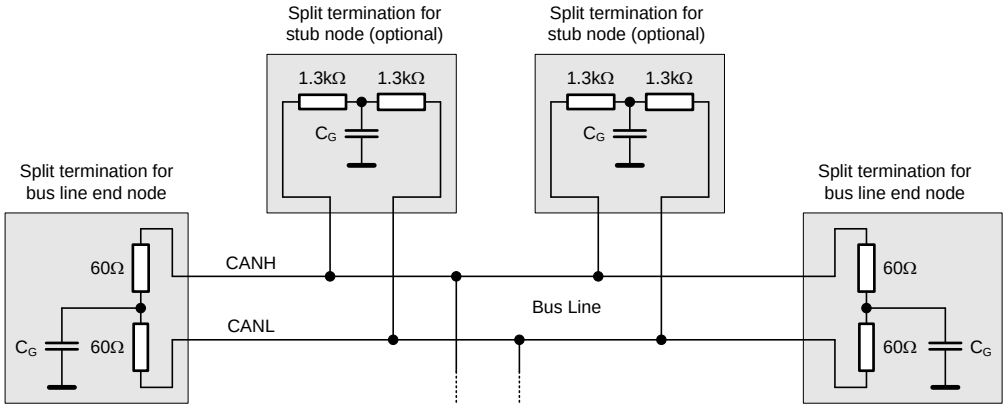


Fig 2. Typical split termination concept

Basically each of the two termination resistors of the bus line end nodes is split into two resistors of equal value, i.e. two resistors of 60Ω instead of one resistor of 120Ω. As an option, stub nodes, which are connected to the bus via stubs, can be equipped with a similar split termination configuration, also called high ohmic termination. The resistor value for these stub nodes has to be chosen in such a way that the bus load of all termination resistors stays within the specified range from 45Ω to 65Ω. As an example for a network with up to 10 nodes (8 stub nodes and 2 bus end nodes) a typical resistor value of the high ohmic termination is 1.3 kΩ. The special characteristic of this split termination approach is that the common mode signal, available at the centre tap of the termination, is terminated to ground via a capacitor. Together with the resistors this termination concept works as a low pass filter. The recommended value for this capacitor is in the range of 4,7nF.

In case of many high-ohmic stub nodes it can be considered to increase the main bus termination of 2 times 60Ω towards 2 times 62Ω or more. Since an automotive bus system is never “ideal” terminated with respect to the “begin” and “end” of the bus line, the overall termination is always a compromise. With that in mind, it might even be considered to have just one central bus termination in the star point of a system using 2 times 31Ω as an example.

As the symmetry of the two CAN bus signal lines is crucial for the emission performance of the system, the matching tolerance of the two termination resistors should be as low as possible (desired: < 2 %).

Generally the termination strategy is prescribed by the individual OEM. Please refer to the corresponding specifications for details.

2.5.1 Open bus wire in split termination networks

The picture below, Fig 3 shows a network in which one wire of the un-terminated stub node 1 is disconnected. Depending on the size of the capacitor in the split termination compared to the bus speed, a transmission of node 1 might still be possible.

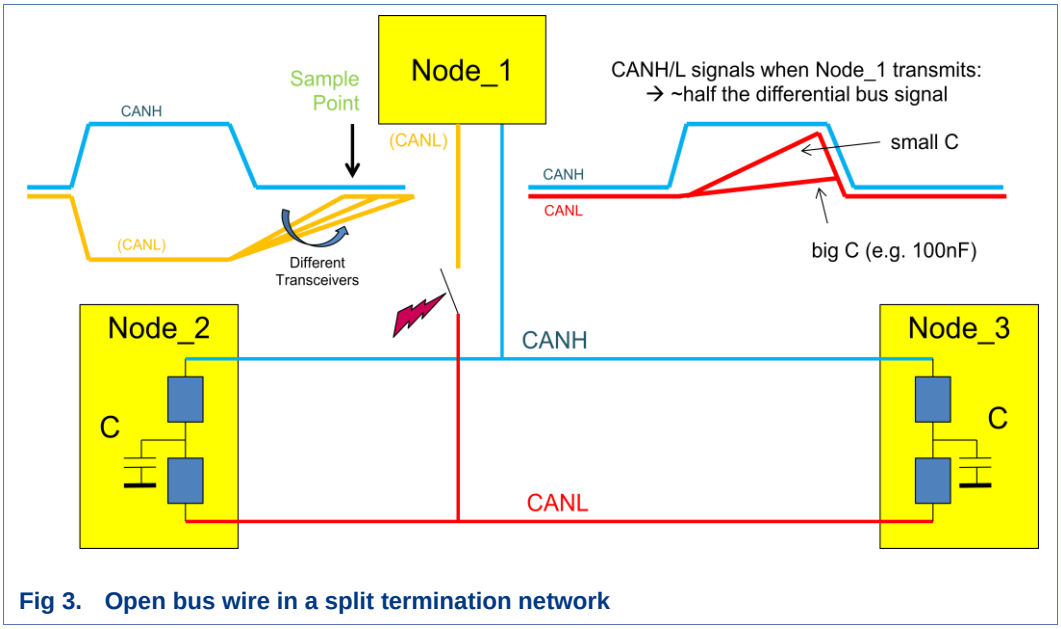


Fig 3. Open bus wire in a split termination network

If node 1 is able to transmit, then depending on the transceiver product, the dominant to recessive edge on of the (CANL) signal, directly at node 1 might not be recessive in time at the sample point and creating bus errors.

The better the EMC performance of a transceiver product, the slower the recessive bit will be on an open un-terminated bus wire and with that, the higher the probability becomes, that the recessive bit is not seen in due time at the node with the open bus wire. It also depends on the bus speed, the detailed bit timing settings, the capacitance of the individual PCB board and the transceiver, whether the recessive bit is seen correctly or not at the sample point.

Why is a big capacitance in the split termination not a good option?

- Communication is not very reliable, bus levels have ½ the amplitude with poor signal quality (when transmitting through an open bus wire spot)
- Dependency on PCB layout and used transceiver having an impact on system performance creating many error frames
- Not very predictable in various vehicle systems

2.5.2 Split termination recommendation

To avoid bus error frames caused by open bus wires in a network (as shown in this example) and to achieve a predictable system behavior, it is recommended to limit the capacitor in the split termination to e.g. 4,7nF (500kBit/s systems).

2.6 Summary of EMC improvements

It is highly recommended to implement the split termination. The system performance can be improved by additional measures like common mode chokes, capacitors and ESD clamping diodes.

However with the optimized EMC performance of NXP's 3rd generation high speed CAN transceivers the split termination can even be used without a choke. As shown in various emission measurements the excellent output stage symmetry of NXP's 3rd generation high speed CAN transceivers allows a choke-less implementation.

2.7 Common mode stabilization via transceiver's SPLIT pin

The SPLIT pin was invented years ago in order to cope with two issues:

- Higher leakage current of "old transceiver generations" when they were unpowered causing an EMC emission issue.
- Common Mode range of "old transceiver generations", if there is injected noise causing an EMC immunity issue.

"Old transceiver generations" means e.g. the 82C250 type of transceiver or other none NXP company devices from the early days of CAN. Modern transceivers of today do not need the SPLIT pin function anymore, because the two above mentioned topics are solved in the transceivers already.

In future there will be no SPLIT pin anymore. The SPLIT pin was a temporary solution to cover old transceiver weaknesses. However the external Split Termination with capacitor to GND is state of the art termination (see also Chapter 2.5).

2.8 Common mode range

Due to disturbances in car network topologies the CAN bus voltages can be reduced or elevated for a certain voltage range. Even though and because of the use of differential input voltage circuits combined with an input resistor divider circuit transceivers are able to receive messages. The common mode range as illustrated in the ISO 11898 is reflecting this requirement (see Figures below).

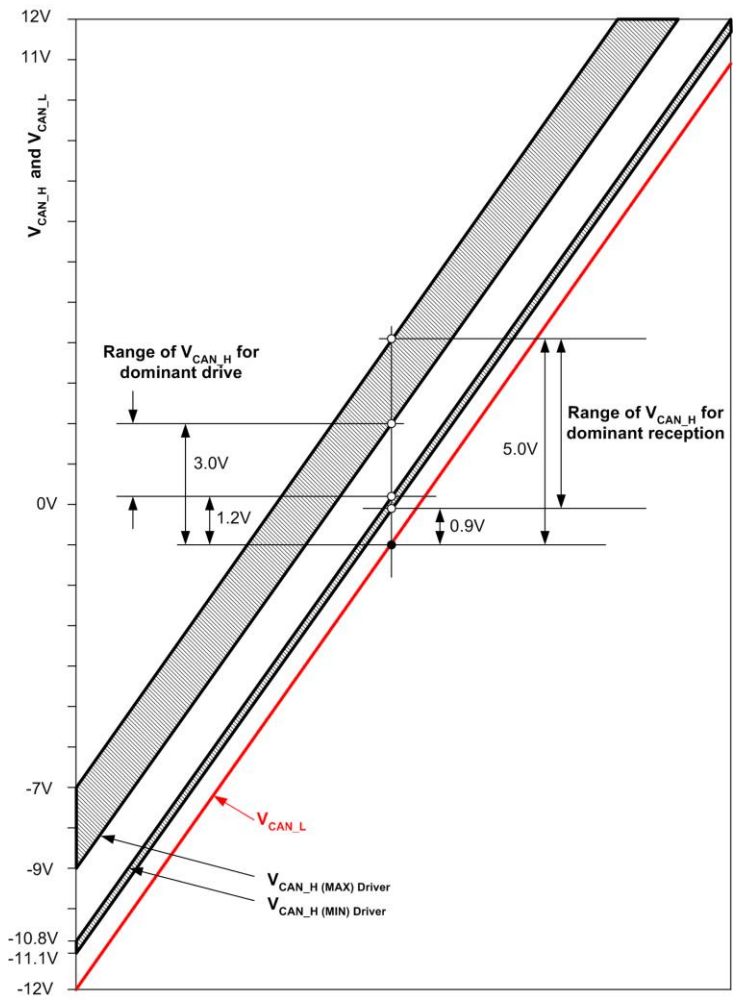


Fig 4. Valid voltage range of VCAN_H for monitoring dominant bus state if VCAN_L varies from min. to max. common mode range of bus according to ISO11898

A valid common mode voltage range of CANH/L from -12V to +12V is defined in the ISO 11898. That means, although the common mode CAN bus voltage might swing up or down the transceiver's input circuit needs to be immune again these symmetrical common mode disturbances. The higher the range of the allowable common mode voltage range is, the better the immunity against interferences.

The figure below shows a typical input circuit of a NXP CAN transceiver. The incoming bus signals are connected to the input threshold detector via a voltage divider. A high ratio of the voltage divider is guaranteeing a high immunity against common mode disturbances.

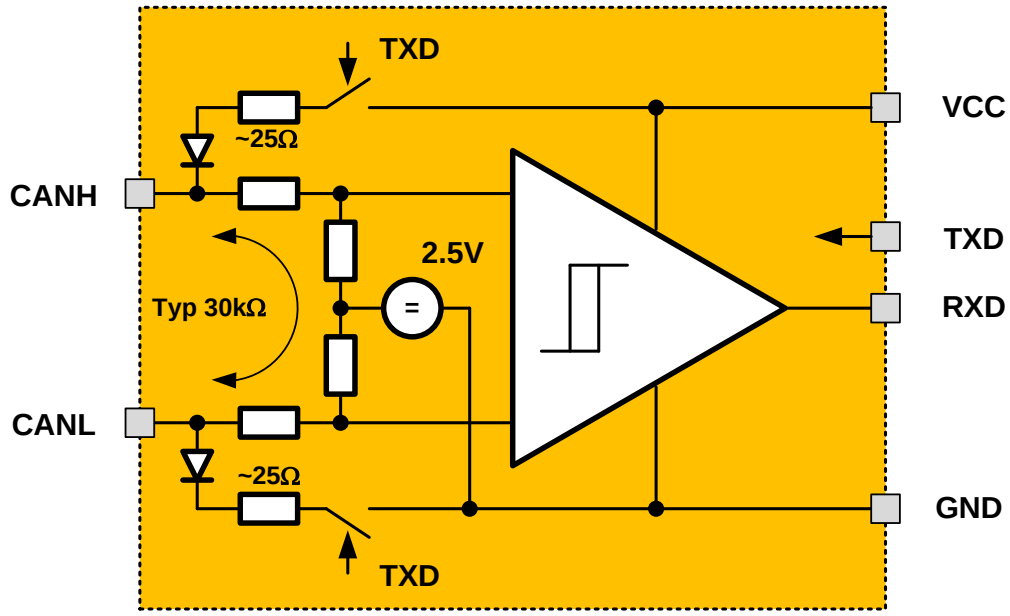


Fig 5. Typical and simplified NXP transceiver circuit

2.9 PCB layout rules (check list)

Following guidelines should be considered for the PCB layout.

- When a common mode choke is used, it should be placed close to the transceiver bus pins CANH and CANL.
- The PCB tracks for the bus signals CANH and CANL should be routed close together in a symmetrical way. Its length should not exceed ~10cm.
- Avoid routing other “off-board” signal lines parallel to the CANH/CANL lines on the PCB due to potential “single ended” noise injection into CAN wires.
- The ESD protection should be connected close to the ECU connector bus terminals.
- For decoupling place a V_{CC} and V_{IO} capacitor to ground close to transceiver supply pins.
  However for all 3rd generation transceiver products (TJA1051/3, TJA1042/3, TJA1043, TJA1048) decouple the VIO pin by a capacitor to VCC (instead to ground and close to the transceiver supply pin). This achieves a high-frequent short of the supplies and improves the electromagnetic immunity.
- The track length between communication controller / µC and transceiver should be as short as possible
- The ground impedance between communication controller (µC) and transceiver should be as low as possible.
- Avoid applying filter elements into the GND signal of the µC or the Transceiver. GND has to be the same for Transceiver and µC.

3. Bus network aspects of high speed CAN

This chapter deals with items like the maximum number of nodes, the maximum bus line length and topology aspects. Especially the topology appears to have a significant influence on the system performance.

3.1 Maximum number of nodes

The number of nodes, which can be connected to a bus, depends on the minimum load resistance a transceiver can drive. NXPs 3rd generation high speed CAN transceivers provide an output drive capability down to a minimum load of $R_{L,min}$ = 45Ohm for V_{CC} > 4,5 V (4,75V for the TJA1048). The overall busload is defined by the termination resistance R_T, the bus line resistance R_W and the transceiver's differential input resistance Ri(dif). The DC circuit model of a bus system is shown in Fig 6. For worst case consideration the bus line resistance RW is considered to be zero. This leads to the following relations for calculating the maximum number of nodes:

$$\frac{R_{T,\min} * R_{i(dif),\min}}{n_{\max} * R_{T,\min} + 2R_{i(dif),\min}} \geq R_{L,\min}$$

Rearranged to n_{max}:

$$n_{\max} \leq R_{i(dif),\min} * \left(\frac{1}{R_{L,\min}} - \frac{2}{R_{T,\min}} \right)$$

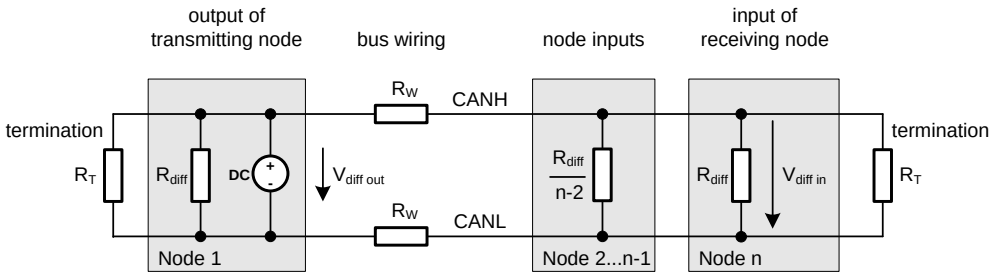


Fig 6. DC circuit model for a bus system according to ISO11898

Table 1 below gives the maximum number of nodes for two different termination resistances. Notice that connecting a large number of nodes requires relatively large termination resistances.

Table 1. Maximum number of nodes (see data sheets for $R_{dif,min}$ and $R_{L,min}$)

Transceiver	$R_{i(dif),min}$(kOhm)	$R_{L,min}$(Ohm)	Nodes (maximum) ($R_{T,min}$=118Ohm)	Nodes (maximum) ($R_{T,min}$=130Ohm)
TJA1051, TJA1042 TJA1048, TJA1043	19	45	100	129

3.2 Maximum bus line length

The maximum achievable bus line length in a CAN network is determined essentially by the following physical effects:

1. Loop delays of the connected bus nodes (CAN controller, transceiver etc.) and the delay of the bus line.
2. Relative oscillator tolerance between nodes.
3. Signal amplitude drop due to the series resistance of the bus cable and the input resistance of bus nodes (for a detailed description refer to [4]).

Effects 1 and 2 result in a value for the maximum bus line length with respect to the CAN bit timing [4]. Effect 3, on the other hand, results in a value with respect to the output signal drop along the bus line. The minimum of the two values has to be taken as the actual maximum allowable bus line length. As the signal drop is only significant for very long lengths, effect 3 can often be neglected for high data rates.

Table 2. Maximum bus line length for some standards

Specification	Data rate		
	125 kBit/s (BT tol. = +/- 1,25%)	250 kBit/s (BT tol. = +/- 0,75%)	500 kBit/s (BT tol. = +/- 0,5%)
SAE J2284	50 m	50 m	33 m
TJA1051, TJA1042 TJA1048, TJA1043	80 m	80 m	40 m

(BT tol. = Bit Time Tolerance)

Table 2 gives the maximum bus line length for the bit rates 125 kbit/s, 250 kbit/s and 500 kbit/s, along with values specified in the SAE J2284 [3] standard associated to CAN. The calculation is based on effects 1 and 2 assuming a minimum propagation delay between any two nodes of 200 ns and a maximum bus signal delay of 8 ns/m. Notice that the stated values apply only for a well-terminated, linear topology. Bad signal quality because of inadequate termination can lower the maximum allowable bus line length.

3.3 Topology

The topology describes the wiring harness structure. Typical structures are linear, star- or multistar-like topologies. In automotive, shielded or unshielded twisted pair cable usually functions as a transmission line. Transmission lines are generally characterized by the length-related resistance R_{Length}, the specific line delay t_{delay} and the characteristic line impedance Z. Table 3 shows the physical media parameters specified in the ISO11898 and SAE J2284 standard. Notice that SAE J2284 specifies the twist rate r_{twist} in addition.

Table 3. Physical media parameters of a pair of wires (shielded or unshielded)

Parameter	Notation	Unit	ISO11898			SAE J2284		
			Min.	Typ.	Max.	Min.	Typ.	Max.
Impedance	Z	Ohm	95	120	140	108	120	132
Length-related resistance	R_{Length}	mOhm/m	-	70	-	-	70	-
Specific line delay	t_{delay}	ns/m	-	5	-	-	5,5	-
Twist rate	r_{twist}	twist/m	-	-	-	33	-	50

Ringing due to signal reflections

Transmission lines must be terminated with the characteristic line impedance, otherwise signal reflections will occur on the bus causing significant ringing. The topology has to be chosen such that reflections will be minimized. Often the topology is a trade-off between reflections and wiring constraints.

CAN is well prepared to deal with reflection ringing due to some useful protocol features:

- Only recessive to dominant transitions are used for resynchronization.
- Resynchronization is allowed only once between the sample points of two bits and only, if the previous bit was sampled and processed with recessive value.
- The sample point is programmable to be close to the end of the bit time.

Linear topology

The high speed CAN standard ISO11898 defines a single line structure as network topology. The bus line is terminated at both ends with a single termination resistor. The nodes are connected via not terminated drop cables or stubs to the bus. To keep the ringing duration short compared to the bit time, the stub length should be as short as possible. For example the ISO11898 standard limits the stub length to 0.3 m at 1 Mbit/s. The corresponding SAE standard, J2284-500, recommends keeping the stub length below 1 m. To minimize standing waves, ECUs should not be placed equally spaced on the network and cable tail lengths should not all be the same [3] . Table 4 along with Fig 7 illustrates the topology requirements of the SAE J2284-500 standard. At lower bit rates

the maximum distance between any two ECUs as well as the ECU cable stub lengths may become longer.

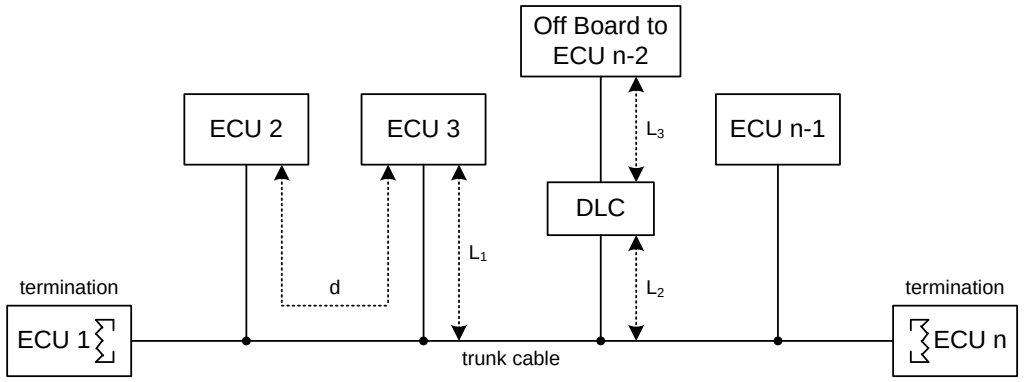


Fig 7. Topology requirements of SAE J2284

In practice some deviation from that stringent topology proposals might be necessary, because longer stub lengths are needed. Essentially the maximum allowable stub length depends on the bit timing parameters, the trunk cable length and the accumulated drop cable length.

The star topology is neither covered by ISO11898 nor by SAE J2284. However, it is used in automotive applications to overcome wiring constraints within the car. Generally, the signal integrity suffers from a star topology compared to a linear topology.

Table 4. ECU topology requirements of SAE J2284-500

Parameter	Symbol	Unit	Min.	Nom.	Max.
ECU cable stub length	L1	m	0	-	1
In-vehicle DLC cable stub length	L2	m	0	-	1
Off board DLC cable stub length	L3	m	0	-	5
Distance between any two ECUs	D	m	0,1	-	33

Note: It is recommended to prove the feasibility of a specific topology in each case by simulations or measurements on a system setup.

4. System Network Pin FMEA

This chapter provides an FMEA (Failure Mode and Effect Analysis) from a system point of view for typical failure situations, when dedicated pins of a HS-CAN transceiver in a network are shorted to supply voltages e.g. V_{BAT}, V_{CC}, GND or to adjacent pins or simply left open. The individual failures are classified, due to their corresponding effects on the transceiver and bus communication in Table 5.

Table 5. Classification of failure effects

Class	Effects
A	- Damage to transceiver - Bus may be affected
B	- No damage to transceiver - No bus communication possible
C	- No damage to transceiver - Bus communication possible - Corrupted node excluded from communication
D	- No damage to transceiver - Bus communication possible - Reduced functionality of transceiver

Table 6. FMEA matrix for pin short-circuits to VBAT and VCC

Pin	Short to V_{BAT} (12V … 40 V)		Short to V_{CC} (5V)	
	Class	Remark	Class	Remark
CANL	B	No bus communication	B	No bus communication
CANH	D	Decline of EMC; Bit timing violation possible	D	Decline of EMC; Bit timing violation possible
SPLIT	D	Bus charged to V_{BAT} level; Bit timing violation possible	D	Bus charged to V_{CC} level; Bit timing violation possible

Table 7. FMEA matrix for pin short-circuits to GND and open

Pin	Short to GND		Open, not connected	
	Class	Remark	Class	Remark
CANL	C	Decline of EMC; Bit timing violation possible	B/C	Bus communication between ECUs on the same side of an interruption may be possible. Bus communication between ECUs on opposite sides of an interruption is disturbed. See also Chapter 2.5.1
CANH	B	No bus communication		
SPLIT	D	Bus discharged to ground level; bit timing violation possible	D	No DC common mode stabilization

Table 8. FMEA matrix for pin short-circuits to adjacent pins

Pin	Short to adjacent pin	
	Class	Remark
CANL to CANH	B	No bus communication

5. Abbreviations

Table 9. Abbreviations

Acronym	Description
CAN	Controller Area Network
Clamp-15	ECU architecture, Battery supply line after the ignition key, module is temporarily supplied by the battery only (when ignition key is on)
Clamp-30	ECU architecture, direct battery supply line before the ignition key, module is permanently supplied by the battery
DLC	Data Link Control
ECU	Electronic Control Unit
EMC	Electromagnetic Compatibility
EME	Electromagnetic Emission
EMI	Electromagnetic Immunity
ESD	Electrostatic Discharge
FMEA	Failure Mode and Effects Analysis
LIN	Local Interconnect Network
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board
SBC	System Basis Chip
SPI	Serial Peripheral Interface

6. References

[1] Road Vehicles – Controller Area Network (CAN) – Part 2: High-speed medium access unit, ISO 11898-2, International Standardization Organization, 2003

[2] Road Vehicles – Controller Area Network (CAN) – Part 5: High-speed medium access unit with low power mode, ISO 11898-5, International Standardization Organization, 2007

[3] High Speed CAN (HSC) for Vehicle Applications at 500kbps - SAE J2284, 2009

[4] Application Note AN97046, Determination of Bit Timing Parameters for the CAN Controller SJA1000 – Philips Semiconductors, 1996

[5] Product data sheet PESD1CAN, CAN bus ESD protection diode – NXP Semiconductors, Rev. 04, 2008 Feb 15

[6] Product data sheet PESD2CAN, CAN bus ESD protection diode – NXP Semiconductors, Rev. 01, 2006 Dec 22

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