

QorIQ T2080 Reference Design Board (T2080RDB-PC) Quick Start

Contents

1 Introduction

The T2080 reference design board (T2080RDB-PC) system is a hardware board, supporting the Freescale QorIQ T2080 Power Architecture® processor with four dual-threaded e6500 cores and speed up to 1.8 GHz.

For the T2080 RDB system, the prototype part number is T2080RDB and the production part number is T2080RDB-PC.

2 Related documentation

Some of the documents listed in the table below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer or sales representative.

Table 1. Useful references

| Document name | Description |
|---|--|
| QorIQ T2080 Reference Design Board (T2080RDB-PC) User Guide | This document explains the procedure to build, configure, and use different components for the Freescale T2080RDB board. |

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Table 1. Useful references (continued)

| Document name | Description |
|--|---|
| T2080 QorIQ Integrated Multicore Communication Processor Family Reference Manual | This document provides a detailed description on T2080 QorIQ multicore processor, and on some of its features, such as memory map, serial interfaces, power supply, chip features, and clock information. |
| T2080 Product Brief | This document provides an overview of the Freescale T2080 features, and usage examples of T2080. |
| T2080 QorIQ Advanced Multicore Processor Data Sheet | This document contains T2080 information on pin assignments, electrical characteristics, hardware design, considerations, package information, and ordering information. |

3 Preparing board

This board has two working modes, the Standalone mode and PCIe Endpoint mode. By default, the system is in the Standalone working mode with 1U chassis. For the PCIe Endpoint mode operation, take the board out from the 1U chassis and install PCIe bracket on the board. Now, the board can be plugged into a PCIe x4 slot in X86 server, and it can work as a PCIe card. [Figure 1](#) shows the I/O of the front panel of the 1U chassis, and [Figure 2](#) shows the PCIe card.



Figure 1. T2080RDB-PC front panel

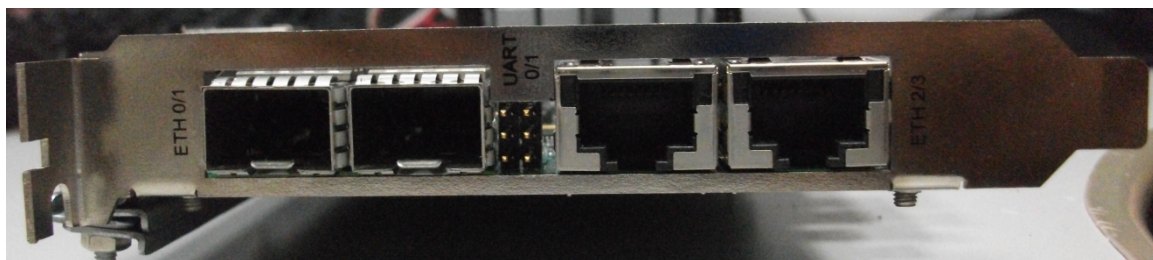


Figure 2. T2080RDB-PC PCIe card

To prepare the T2080RDB-PC for use, default configuration should be:

- CPU: 1.8 GHz
- DDR: 1600 MT/s or 1866 MT/s

The steps to prepare a T2080RDB board are:

1. Attach a RS-232 cable between the T2080RDB UART0 port (Rx-GND-Tx 3 pins) and host computer.
2. Open a serial connection on the host computer to communicate with the T2080RDB board.
3. Configure the host computer's serial port with the following settings:
 - Data rate: 115200 bps
 - Number of data bits: 8
 - Parity: None
 - Number of stop bits: 1
 - Flow control: Hardware/None
4. Push the power button on the front side of the chassis. The board boots up and shows the following U-Boot console messages:

```

U-Boot 2014.01QorIQ-SDK-V1.6+gfe1d4f5 (Jun 10 2014 - 11:45:39)

CPU0: T2080E, Version: 1.1, (0x85380011)
Core: e6500, Version: 2.0, (0x80400120)
Clock Configuration:
CPU0:1799.820 MHz, CPU1:1799.820 MHz, CPU2:1799.820 MHz, CPU3:1799.820 MHz,
CCB:599.940 MHz,
DDR:933.310 MHz (1866.620 MT/s data rate) (Asynchronous), IFC:149.985 MHz
FMAN1: 699.930 MHz
QMAN: 299.970 MHz
PME: 599.940 MHz
L1: D-cache 32 KiB enabled
I-cache 32 KiB enabled
Reset Configuration Word (RCW):
00000000: 1207001b 15000000 00000000 00000000
00000010: 66150002 00000000 ec027000 c1000000
00000020: 00800000 00000000 00000000 000307fc
00000030: 00000000 00000000 00000000 00000004

Board: T2080RDB, Board rev: 0x01 CPLD ver: 0x03, boot from NOR vBank4
SERDES Reference Clocks:
SD1_CLK1=156.25MHZ, SD1_CLK2=100.00MHZ
SD2_CLK1=100.00MHZ, SD2_CLK2=100.00MHZ
I2C: ready
SPI: ready
DRAM: Initializing...using SPD
Detected UDIMM 18KSF51272HZ-1G6K2
2 GiB left unmapped
4 GiB (DDR3, 64-bit, CL=11, ECC on)
DDR Chip-Select
Interleaving Mode: CS0+CS1
Flash: 128 MiB
L2: 2 MiB enabled
Corenet Platform Cache: 512 KiB enabled
Using SERDES1 Protocol: 102 (0x66)
Using SERDES2 Protocol: 22 (0x16)
NAND: 512 MiB
MMC: FSL_SDHC: 0
EEPROM: NXID v1
PCIe1: Root Complex, no link, regs @ 0xfe240000
PCIe1: Bus 00 - 00
PCIe2: Root Complex, x2 gen2, regs @ 0xfe250000
02:00.0 - 1957:0808 - Processor
PCIe2: Bus 01 - 02
PCIe3: disabled
PCIe4: Endpoint, no link, regs @ 0xfe270000
PCIe4: Bus 03 - 03
In: serial
Out: serial
Err: serial
Net: Fman1: Uploading microcode
version 106.4.14
PHY reset timed out
PHY reset timed out

```

System board interface

```
FM1@DTSEC3 [PRIME], FM1@DTSEC4, FM1@TGEC1, FM1@TGEC2, FM1@TGEC3,  
FM1@TGEC4  
Hit any key to stop autoboot: 0  
=>
```

The Linux system auto boots and shows the following messages on the login screen:

```
t208rdb  
login: root  
root@t2080rdb:~#
```

4 System board interface

Figure 3 shows the top view of the T2080RDB-PC system board interface.

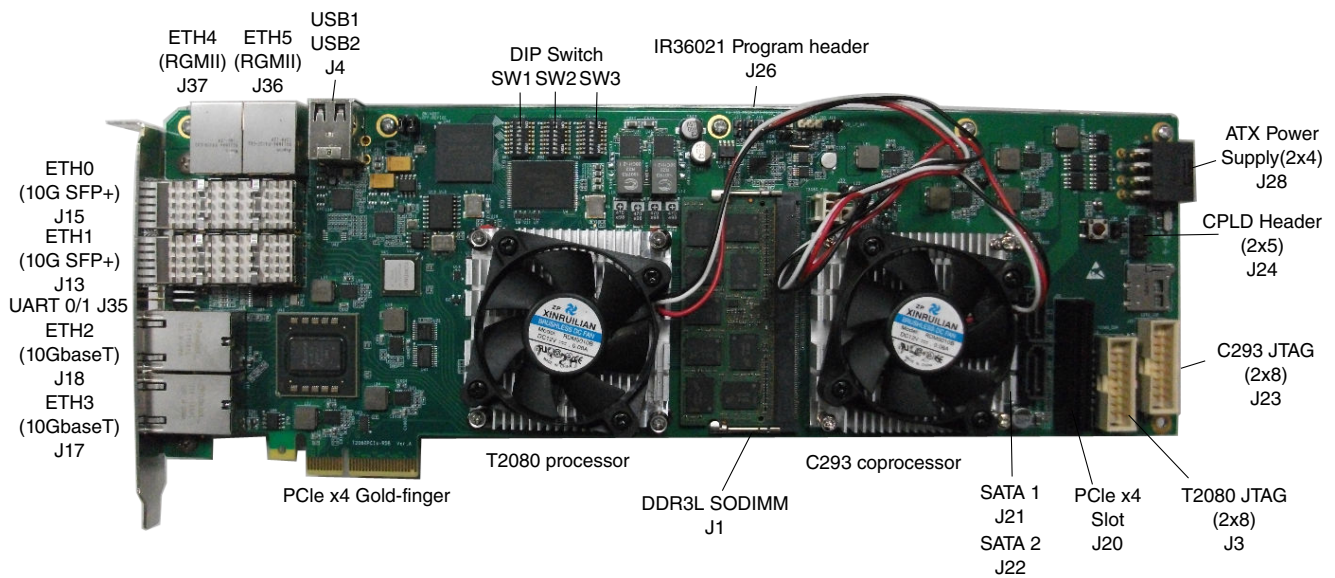


Figure 3. T2080RDB-PC system board interface

4.1 Block diagram

Figure 4 shows the high-level block diagram of the T2080RDB-PC.

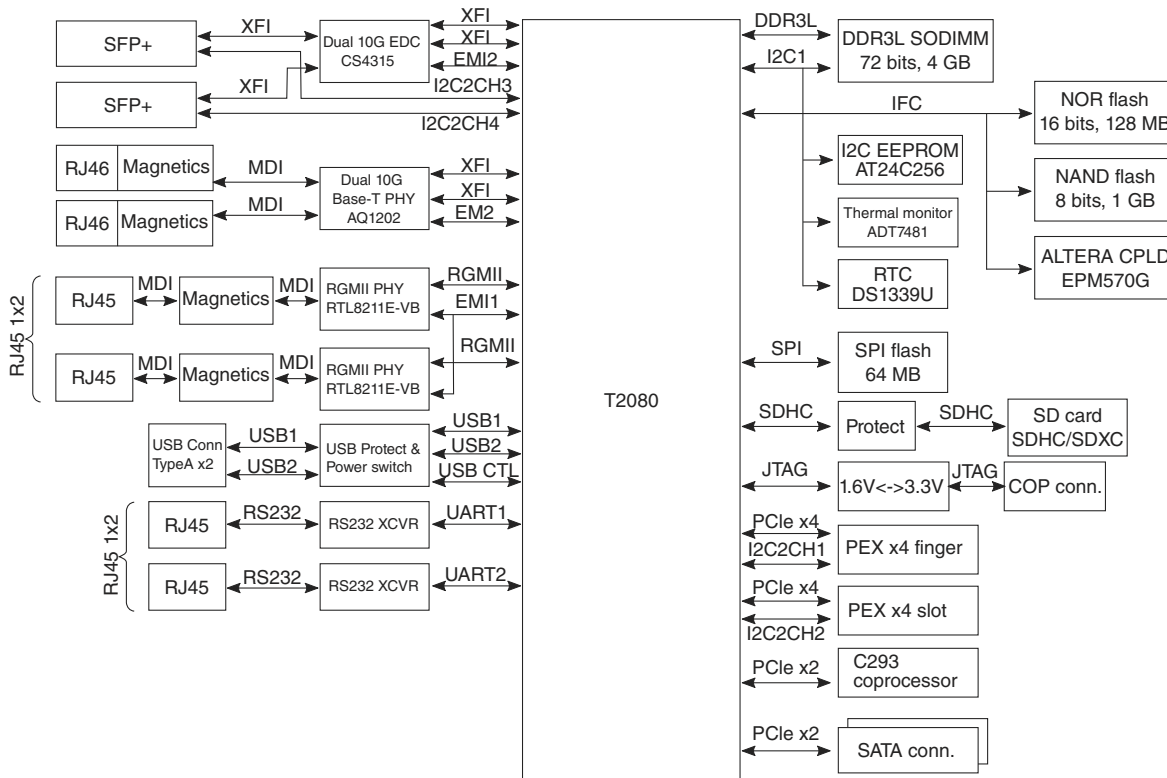


Figure 4. T2080RDB-PC block diagram

4.2 Features

Some key features of the T2080RDB-PC are:

- Freescale QorIQ processing platform
 - QorIQ T2080 SoC integrating four dual-threaded e6500 cores and speed up to 1.8 GHz
- Memory subsystem
 - DDR3 SDRAM
 - Single SODIMM, 72-bit DDR3L at or 1866 MT/s, based on actual DDR3L UDIMM
 - NOR flash
 - 128 MB 16-bit NOR flash, MICRON: JS28F00AM29EWHA
 - NAND flash
 - 1 GB SLC NAND flash, MICRON: MT29F8G08ABABAWP-ITX:B
 - One microSD/TF connector interface
 - Two SATA interfaces
- Ethernet
 - ETH 0 - ETH 1: XFI 10G SFP+, connected to Cortina CS4315 PHY
 - ETH 2 - ETH 3: XFI 10GBase-T copper twisted pair cable, connected to AQ1202 PHY
 - ETH 4 - ETH 5: 10 Mbit/s, 100 Mbit/s, or 1 Gbit/s RGMII, connected to RTL8211E PHY
- PCIe
 - One PCIe-x4 gold-finger
 - One PCIe-x4 connector
 - One crypto coprocessor C293 PCIe Endpoint device
- USB 2.0
 - One dual-USB slot, connected to USB PHY
- UART

Flash image layout

- Supports two UARTs, up to 115200 bit/s for console display; uses dual RJ45 slot for the two UART ports
- Real-time clock (RTC)
 - Supports one DS1339U RTC

4.3 Port map

Table 2 shows how the Ethernet ports can be mapped to Linux and U-Boot.

Table 2. Ethernet port mapping

| Label on front panel | Port in U-Boot | Port in Linux | FMAN address | Comments |
|----------------------|----------------|---------------|--------------|-------------------------------|
| ETH0 | FM1@GTEC1 | fm1-mac9 | 0xfe4f0000 | 10GBase-T SFP+ (Cortina 4315) |
| ETH1 | FM1@GTEC2 | fm1-mac10 | 0xfe4f2000 | 10GBase-T SFP+ (Cortina 4315) |
| ETH2 | FM1@GTEC3 | fm1-mac1 | 0xfe4e0000 | 10GBase-T (AQ1202) |
| ETH3 | FM1@GTEC4 | fm1-mac2 | 0xfe4e2000 | 10GBase-T (AQ1202) |
| ETH4 | FM1@DTSEC3 | fm1-mac3 | 0xfe4e4000 | 1G RGMII (RTL8211E) |
| ETH5 | FM1@DTSEC4 | fm1-mac4 | 0xfe4e6000 | 1G RGMII (RTL8211E) |

5 Flash image layout

Table 3 shows the flash image layout.

Table 3. Flash image layout

| Start address | End address | Image | Maximum size |
|---------------|--------------|---------------------------------------|---------------|
| 0xEFF40000 | 0xEFFFFFFF | U-Boot (current bank) | 768 KB |
| 0xEFF20000 | 0xEFF3FFFF | U-Boot environment (current bank) | 128 KB |
| 0xEFF00000 | 0xEFF1FFFF | FMan microcode (current bank) | 128 KB |
| 0xEFE00000 | 0xEFE3FFFF | PHY CS4315 firmware | 256 KB |
| 0xED300000 | 0xEFEFFFFFFF | rootfs (alternate bank) | 44 MB |
| 0xEC800000 | 0xEC8FFFFFFF | Hardware device tree (alternate bank) | 1 MB |
| 0xEC020000 | 0xEC7FFFFFFF | Linux.ulmage (alternate bank) | 7 MB + 875 KB |
| 0xEC000000 | 0xEC01FFFF | RCW (alternate bank) | 128 KB |
| 0xEBF40000 | 0xEBFFFFFFF | U-Boot (alternate bank) | 768 KB |
| 0xEBF20000 | 0xEBF3FFFF | U-Boot environment (alternate bank) | 128 KB |
| 0xEBF00000 | 0xEBF1FFFF | FMan microcode (alternate bank) | 128 KB |
| 0xEBE00000 | 0xEBE3FFFF | PHY CS4315 firmware (alternate bank) | 256 KB |
| 0xE9300000 | 0xEBEFFFFFFF | rootfs (current bank) | 44 MB |
| 0xE8800000 | 0xE88FFFFFFF | Hardware device tree (current bank) | 1 MB |
| 0xE8020000 | 0xE87FFFFFFF | Linux.ulmage (current bank) | 7 MB + 875 KB |
| 0xE8000000 | 0xE801FFFF | RCW (current bank) | 128 KB |

6 Default RCW setting

Table 4 shows the default reset configuration word (RCW) settings.

Table 4. Default RCW settings

| No | RCW words | Description |
|----|------------|--|
| 1 | 0x120c0017 | 120c: System PLL rate is 1:9 (SYSCLK is 66.66 MHz) and DDR PLL rate is 1:12 (DDRCLK is 133.33 MHz) 0017: Cluster 1 core PLL rate is 1:23 (SYSCLK is 66.66 MHz) |
| 2 | 0x15000000 | 1500: Cluster 2 core PLL rate is 1:21 (SYSCLK is 66.66 MHz) 0000: Reserved |
| 3 | 0x00000000 | Reserved |
| 4 | 0x00000000 | Default setting |
| 5 | 0x66160002 | 0x66: SerDes1 protocol is 0x66 (choose four XFI and PCIe x4 on SerDes 1) 0x16: SerDes1 protocol is 0x16 (choose one PCIe x4, one PCIe x2, and two SATA on SerDes2) 0x02: FMan runs 1x frequency of MAC |
| 6 | 0x00000000 | SerDes clock choice |
| 7 | 0xec027000 | Boot location choice |
| 8 | 0xc1000000 | PME frequency and DDR latency choice |
| 9 | 0x00800000 | PCIe1 in agent mode, others in host mode |
| 10 | 0x00000000 | Default setting, GPIO information |
| 11 | 0x00000000 | Default setting, TDM option |
| 12 | 0x000307fc | 0003: UART option 07fc: ASLEEP, RTC, SDHC_BASE, IRQ_OUT, IRQ_BASE, SPI_BASE option |
| 13 | 0x00000000 | Default setting, IFC option |
| 14 | 0x00000000 | 0000: 1588, SDHC, RGMII, I2C, TDM option 0000: LVDD, L1VDD, CVDD, EVDD, HDLC, DMA option |
| 15 | 0x00000000 | Reserved |
| 16 | 0x00000004 | Reserved |

7 Switch settings

The dual inline package (DIP) switch is used to configure the boot source and to power on or reset some bits. It can choose a NOR flash vbank as a boot vbank.

7.1 Switch default settings (NOR flash boot)

NOR flash boot is the default boot mode. To boot from the NOR flash, the DIP switches should be configured, as shown in the table below.

| DIP switch | Switch binary value | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|------------|---------------------|-----|-----|-----|-----|-----|-----|-----|-----|
| SW1 | 0001 0011 | ON | ON | ON | OFF | ON | ON | OFF | OFF |
| SW2 | 1011 1111 | OFF | ON | OFF | OFF | OFF | OFF | OFF | OFF |
| SW3 | 1110 0001 | OFF | OFF | OFF | ON | ON | ON | ON | OFF |

7.2 Other boot source settings

To boot from the NAND flash, the DIP switches should be configured, as shown in the table below.

| DIP switch | Switch binary value | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|------------|---------------------|-----|-----|-----|-----|-----|-----|-----|-----|
| SW1 | 1000 0010 | OFF | ON | ON | ON | ON | ON | OFF | ON |
| SW2 | 1011 1111 | OFF | ON | OFF | OFF | OFF | OFF | OFF | OFF |
| SW3 | 1111 0001 | OFF | OFF | OFF | OFF | ON | ON | ON | OFF |

To boot from the SPI flash, the DIP switches should be configured, as shown in the table below.

| DIP switch | Switch binary value | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|------------|---------------------|-----|-----|-----|-----|-----|-----|-----|-----|
| SW1 | 0010 0010 | ON | ON | OFF | ON | ON | ON | OFF | ON |
| SW2 | 1011 1111 | OFF | ON | OFF | OFF | OFF | OFF | OFF | OFF |
| SW3 | 1110 0001 | OFF | OFF | OFF | ON | ON | ON | ON | OFF |

To boot from the SD card, the DIP switches should be configured, as shown in the table below.

| DIP switch | Switch binary value | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|------------|---------------------|-----|-----|-----|-----|-----|-----|-----|-----|
| SW1 | 0010 0000 | ON | ON | OFF | ON | ON | ON | ON | ON |
| SW2 | 0011 1111 | ON | ON | OFF | OFF | OFF | OFF | OFF | OFF |
| SW3 | 1110 0001 | OFF | OFF | OFF | ON | ON | ON | ON | OFF |

7.3 Switch detailed description

Table 5 shows the detailed switch description.

Table 5. Switch description

| Switch | POR configure | Signal name | Signal meaning | Setting |
|--------|----------------------|----------------|------------------|---|
| SW1[1] | cfg_rcw_src0 | IFC_AD8 | RCW source | 010011011: Hard-coded RCW for JTAG debug 000100111: NOR flash boot mode 100000101: NAND boot mode 001000101: SPI boot mode |
| SW1[2] | cfg_rcw_src1 | IFC_AD9 | | |
| SW1[3] | cfg_rcw_src2 | IFC_AD10 | | |
| SW1[4] | cfg_rcw_src3 | IFC_AD11 | | |
| SW1[5] | cfg_rcw_src4 | IFC_AD12 | | |
| SW1[6] | cfg_rcw_src5 | IFC_AD13 | | |
| SW1[7] | cfg_rcw_src6 | IFC_AD14 | | |
| SW1[8] | cfg_rcw_src7 | IFC_AD15 | | |
| SW2[1] | cfg_rcw_src8 | IFC_CLE | | |
| SW2[2] | cfg_ifc_te | IFC_TE | | OFF(1): IFC drives logic 0 for TE assertion |
| SW2[3] | cfg_pll_config_sel_b | IFC_A18 | | |
| SW2[4] | cfg_por_ainit | IFC_A19 | | |
| SW2[5] | cfg_svr0 | IFC_A16 | | |
| SW2[6] | cfg_svr1 | IFC_A17 | | |
| SW2[7] | cfg_dram_type | IFC_A21 | | |
| SW2[8] | cfg_rsp_dis | IFC_AVD | | |
| SW3[1] | cfg_eng_use0 | IFC_WE_N | | OFF(1): SYSCLK clock source ON (0): Single-clock source using diff_sys_clk |
| SW3[2] | cfg_eng_use1 | IFC_OE_N | | |
| SW3[3] | cfg_eng_use2 | IFC_WP_N | | |
| SW3[4] | | BOOT_FLASH_SEL | | ON(0): Select NOR flash on CS0 ON(1): Select NAND flash on CS0 |
| SW3[5] | | CFG_VBANK0 | Alter flash bank | 000: NOR flash vbank 0 select 100: NOR flash vbank 4 select |
| SW3[6] | | CFG_VBANK1 | | |
| SW3[7] | | CFG_VBANK2 | | |
| SW3[8] | | TEST_SEL_N | | |

8 How to program flash for the first time (without U-Boot)

To program flash for the first time, without U-Boot, perform the following steps:

- Set DIP switches as:
 - SW1: 0100 1110 (ON is 0 and OFF is 1)
 - SW2: 1011 1111
 - SW3: 1100 0001
- Run `T2080RDB_RCW_override.cfg` in CodeWarrior connection server (CCS) to override RCW.
- Download SPI U-Boot at `0xffff40000`, and set PC reg to `0xfffffff`.
- Run with the CodeWarrior IDE, and enter U-Boot at the console.
- Exit the CodeWarrior IDE.
- Download the following images:

Revision history

- u-boot.bin at 0x100000
- fman_ucode at 0x200000
- t2080.rcw at 0x300000
- cs4315-ucode.txt at 0x400000

7. In U-Boot, run the following commands:

```
protect off all; erase all;
cp.b 100000 eff40000 c0000 (U-Boot)
cp.b 200000 eff00000 10000 (FMan ucode)
cp.b 300000 e8000000 100 (RCW)
cp.b 400000 efe00000 30000 (CS4315 PHY ucode)
```

8. Power down, set DIP switches as:

- SW1: 0001 0011
- SW2: 1011 1111
- SW3: 1100 0001

9. Turn power on, and the system will enter the U-Boot environment.

9 Revision history

This table summarizes revisions to this document.

Table 6. Revision history

| Revision | Date | Topic cross-reference | Description |
|----------|---------|-----------------------|-------------------------|
| Rev. 0 | 02/2015 | - | Initial public release. |

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