

The Analysis Report USB-TAP cannot workable problem

Issue date: 2010/10/13

Report date: 2010/12/13

Problem description: There is a few USB-TAP cannot workable in COP RDB

Fail rate: < 1%

Effect boards: MPC8377E-RDB REV 2.1, MPC8315E-RDB REV A3

Root cause: It's a timing margin issue.

The EMI decoupling capacitor C118 (0.1uF) is too large to slowdown the falling time of TCK (JTAG signal). It makes the setup and hold time over IEEE1149.1 specification.

Analysis:

1. The Timing Specification

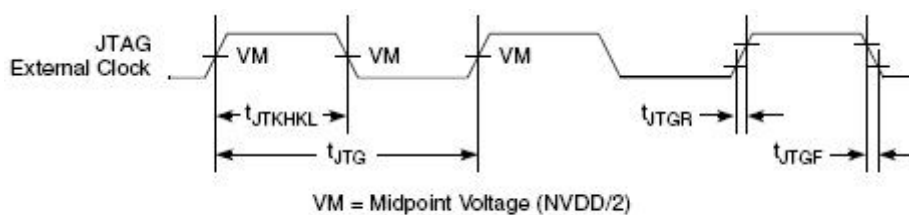


Figure JTAG Clock Input Timing Diagram

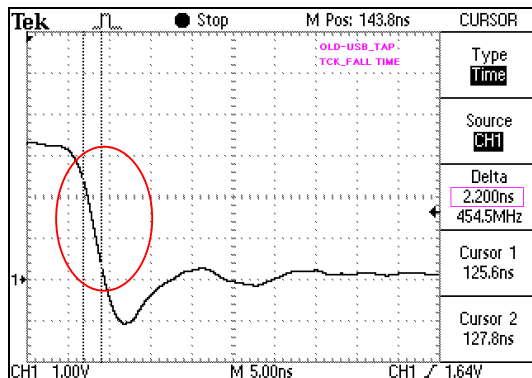
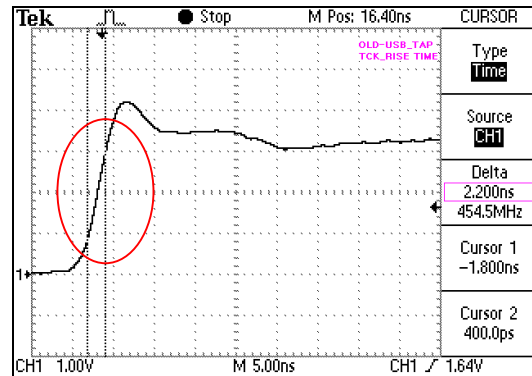
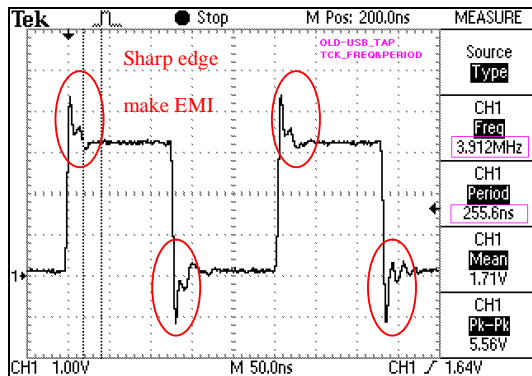
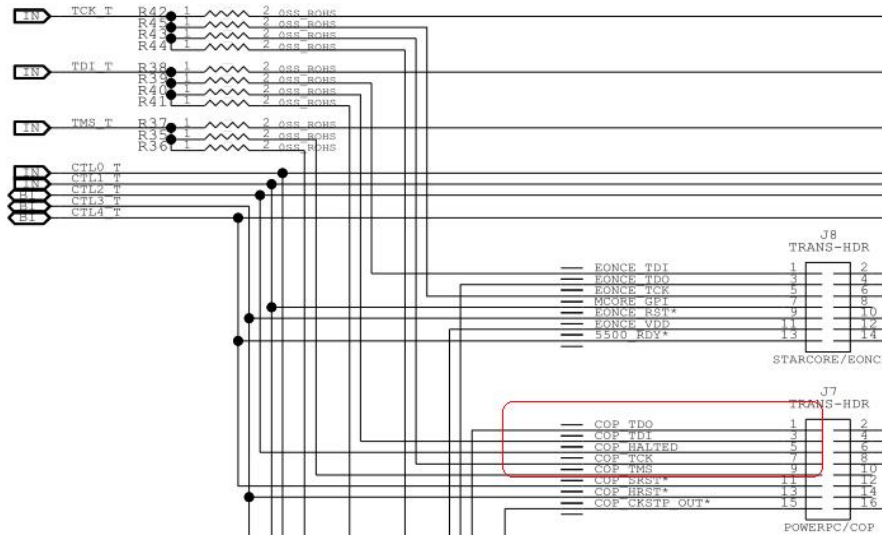
Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JGR}, t_{JGF}	0	2	ns	—

2. Original USB-TAP (Rev.C), no stuff 0.1uF in C118

JTAG timing: $t_{JTG\ R}=2.2\text{ns}$, $t_{JTG\ F}=2.2\text{ns}$ meet spec 2ns (note: probe Tek 116526 has lag)

JTAG Functionality: PASS

EMI in CE/FCC: FAIL



3. NEW USB-TAP (REV.D), C118 stuff 0.1uF

JTAG timing: $t_{JTAGR}=6ns$, $t_{JTAGF}=11ns$ over spec $2ns$ (note: probe Tek 116526 has lag)

JTAG Functionality: Some models are fail

EMI in CE/FCC: PASS

