PCB LAYOUT TIPS AND TRICKS – A JOURNEY TO ROBUSTNESS

LAT-DES-T2445

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SECURE CONNECTIONS FOR A SMARTER WORLD

AGENDA

- Foundation of Electronics
- Electromagnetic Field Behavior
- What’s in the Waves
- How to Use this Wonderful Information
- Power Distribution
- Designing Good Transmission Lines
- Test Results
- New Rules of Thumb
- Design tips
- Closing Remarks and Reference Materials

FOUNDATION OF ELECTRONICS

Myths We Depended On

- Fields are invisible
- Fields are well behaved
- Fields follow the trace
- Fields avoid open spaces
- Fields are someone else’s problem
- Fields are only important in RF and power supply designs
- Fields are only for farmers

What is Electricity?

Is it *volts* and *amperes* …

or *electric* and *magnetic* fields?

(Slide compliments of Ralph Morrison, Consultant)

What is Electricity?

- Fields are basic to all circuit operation

- Volts and amperes make things practical
  - We easily can measure volts and amperes
  - More difficult to measure “E” and “H” fields

- In high clock rate (and rise time) circuits, once the "quasi static” approximation does not hold true anymore, field control plays a critical role

- This must be a carefully considered part of any design

(Slide compliments of Ralph Morrison, Consultant)

ELECTROMAGNETIC FIELD BEHAVIOR

A Loose Field is *Not* a Friendly Field

unHappy field in a sphere with an opening

- Sneaks out and has a party

unHappy field in a poor coaxial cable

- Runs back along the outside of the cable and causes trouble

unHappy field in a widely spaced transmission line pair

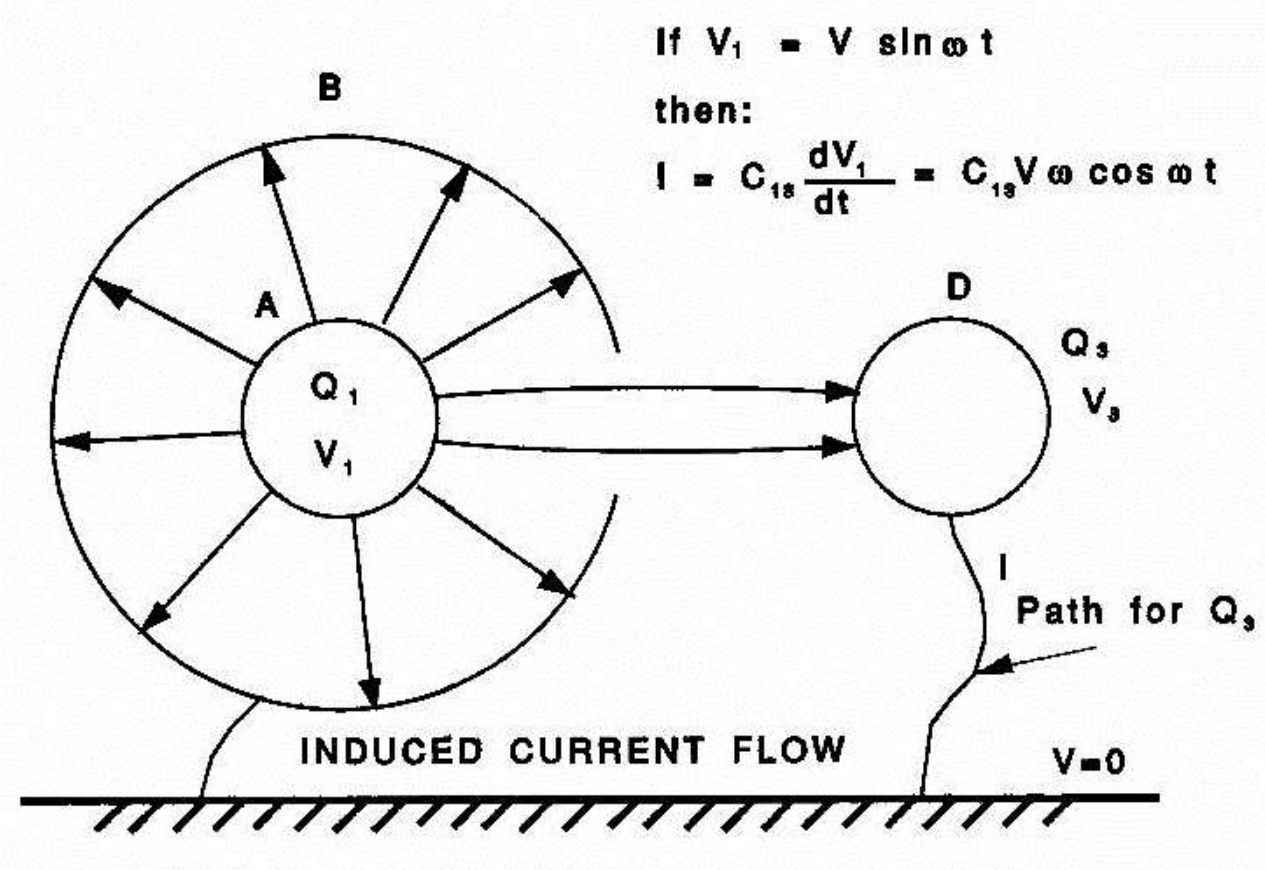
- Reaches out as far as it can, looking for other paths to follow

unHappy field between two widely spaced PCB planes

- Low field density, has very little energy

A Loose Field is *Not* a Friendly Field

A shielded enclosure with an opening



Field is not contained and looks for trouble

(Slide compliments of Ralph Morrison, Consultant)

Energy Management

A capacitor is:

A conductor geometry that concentrates the storage of electric field energy

In a capacitor

Field energy is stored in the space between the plates

An inductor is:

A conductor geometry that concentrates the storage of magnetic field energy

In an inductor

Field energy is stored in the space around wires and in gaps

(Slide compliments of Ralph Morrison, Consultant)

Energy Management

Why does field energy follow conductors?

- Why does water ***flow*** in a stream?
  - Same reason
- Nature follows the path that stores the least energy
- It is easier for fields to follow traces than to go out across space

The Impedance of free space is 377 ohms

- Between conductor pairs it will be lower, so they follow the path of lowest *impedance*

(Slide compliments of Ralph Morrison, Consultant)

Energy Management

Transmission lines are convenient paths for energy flow:

- Every conductor pair is a transmission line
- Trace-to-trace or trace-to-conducting plane
- The fields, and thus the energy flow, will concentrate
  - between traces or between a trace and a conducting plane
- Draw the fields to locate the current

(Slide compliments of Ralph Morrison, Consultant)

Transmission Line Properties

- They direct energy flow
- They can store field energy
- Their position in a circuit is critical
- They cross couple energy only at wave fronts
- They deliver energy at terminations
- They are bi-directional
- They can transport any number of waves at one time
- They can radiate

(Slide compliments of Ralph Morrison, Consultant)

Transmission Line Properties

We use transmission lines to transport energy and to carry logic signals:

- *A transmission line can carry any number of signals in either direction at the same time*
- Below 1 MHz, the geometry of these lines is not too critical
- With today's clock rates and rise times, the geometry of these lines is key to performance

In a good design:

- Fields associated with different signals do not share the same physical space
- If they do share the same space, there is crosstalk

(Slide compliments of Ralph Morrison, Consultant)

Transmission Line Properties

In a good design:

- Energy is available whenever there is a demand
- The voltage source must be reasonably constant
- Energy must be replaced after it is used or there will be logic (signal integrity) problems
- This is called energy management

Local sources of energy:

- Decoupling capacitors
- There is also energy available from ground/power plane capacitance

New problem:

- It takes *time* to move this energy from storage to a load

(Slide compliments of Ralph Morrison, Consultant)

WHAT'S IN THE WAVES

How Long Does It Take?

Wave velocity

- For traces on a circuit board v = c / € $^{1/2}$
- Where c is the velocity of light and € is the relative dielectric constant
  - **v = 150 mm / ns or 6” / ns**

All energy is moved by wave action!

- A *drop in voltage* sends a wave to get more energy
- Waves reflect at discontinuities
- A source of voltage is a discontinuity
- Each reflected wave can carry a limited amount of energy

(Slide compliments of Ralph Morrison, Consultant)

GETTING 1 AMPERE TO FLOW

What does this mean in my circuit board?

- Initial power level in a 50 Ohm line
  - 5 Ohm load and 5 V source
  - I = 0.1 amperes or ½ watt

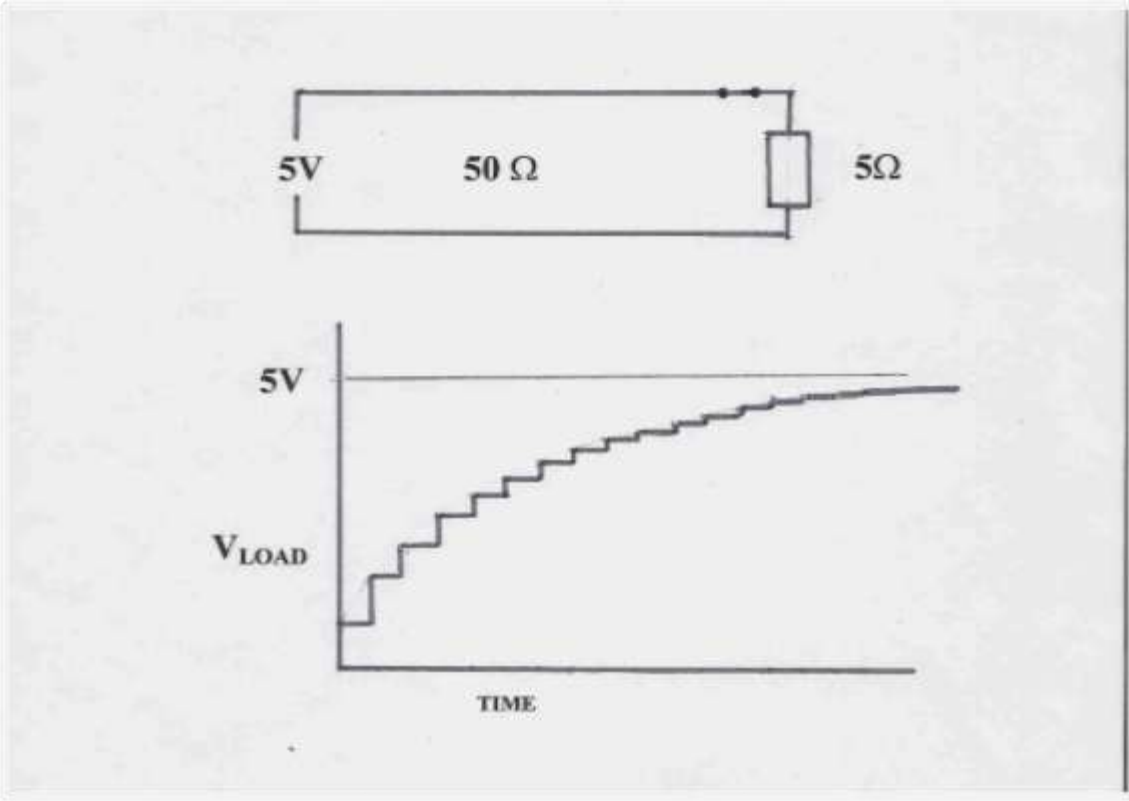
Now, how do I get 1 ampere?

- Even if the line is only 1/16 inch (1.58mm) long:
  - It takes 10 ps for a wave to go 1/16 (1.58mm) inch in fr4
  - It takes 20 ps for a wave to make one round trip
  - It takes 30 round trips on that line to bring current level up to near one amp
  - That is 600 ps, assuming zero rise time

(Slide compliments of Ralph Morrison, Consultant)

GETTING 1 AMPERE TO FLOW

- Note: This is not a curve, but a series of step functions. The amplitude of the step is determined by the impedance of the transmission line and the width of the step is determined by the length of the transmission line and a two way transition for the wave.



(Slide compliments of Ralph Morrison, Consultant)

Typical 1/16 (1.58mm) Inch Connections

- Traces to capacitors
- Connections to IC dies
  - Lead frames and wire bonds
  - BGA interposers
- Traces to vias
- Vias to ground/power planes

(Slide compliments of Ralph Morrison, Consultant)

Transmission Lines

Capacitors are short transmission lines:

- Wave action is required to move energy in and out of a capacitor
- *Don’t forget the connections to the capacitor!*
- Self inductance does not properly tell the story of why it takes time to supply energy
- Circuit theory does not consider time delays

See the previous diagram!

(Slide compliments of Ralph Morrison, Consultant)

Energy Management

All energy is moved by wave action!

When a switching element closes, this results in a drop in the voltage on the power supply. The *resulting* field energy request wave travels until this request is filled or it radiates.

The only way to reduce noise in a system is to reduce this distance and provide adequate sources of electromagnetic field energy.

Energy source hierarchy

- On-chip capacitance
- Space between the wirebonds
- Between layers of Substrate (BGA) or leadframe (QFP)
- Power planes if present
- Local bypass capacitors
- Field energy stored across the PCB structure
- Bulk storage capacitors
- Finally the power supply

We have to keep the field happy and contained as far up the food chain as we can, to reduce system noise.

(Slide compliments of Ralph Morrison, Consultant)

Antenna Size vs. Frequency

- ¼ wavelength is accepted as a good antenna size
- In the Analog Domain, this is 90 degrees

Frequency	¼ wave length
10 MHz HMOS Rise time equivalent, 100 nanoseconds rise time distance, 30,48 m	7,49 m Across the room
100 MHz (TTL Logic) UDR HCMOS Rise time equivalent, 10 nanoseconds rise time distance, 3,04 m	74,98 cm
1 GHz (BiCMOS Logic) IDR HCMOS Rise time equivalent, 1 nanosecond rise time distance, 0,30 m	7,49 cm Less than your finger
10 GHz (GaAs Logic) 65 nm HCMOS Rise time equivalent, 100 picoseconds rise time distance, 3,04 mm	7,49 mm Less than the diameter of a pencil
100 GHz 32 nm HCMOS Rise time equivalent, 10 picoseconds rise time distance, 0,30 mm	0,74mm Half the thickness of a standard FR4 PCB

Antenna Size vs. Frequency

From the previous table, a few things become apparent:

- We got away with ignoring basic physics because IC switching speeds were slow and efficient antennas had to be *huge*.
- At a switching speed of 1 nanosecond, it only takes a PCB feature (trace or slot) of 76,2 mm to be an efficient antenna (1/4 wave length).
- Once you cross that magic boundary of 1 nanosecond, most PCB designs are capable of providing a wonderful source of antennas.
- At 10 picosecond speeds, every structure in the system can be an good antenna.

Since TTL days:

Four order magnitude change in switching speeds

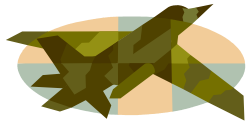
Almost no changes in PCB or system design philosophy

Four Order Magnitude Change

1st order: Vehicles go 10 km an hour

2nd order: Vehicles go 100 km an hour

3rd order: Vehicles go 1.000 km an hour



4th order: Vehicles go 10.000 km an hour

5th order: Vehicles go 100.000 km an hour

Only in our industry we try to make the buggy to go fast!

Rise Time Distance

- Now, what does this really mean?

- Rise time distance is how far the wave travels by the time it reaches full amplitude.
- Determined by the switching speed of the output driver
- In digital circuits, this is really ½ wavelength, or 180 degrees!

- Let's look at this from a *switching speed* vs. lumped distance perspective.
- Remember, lumped distances are basically the size of a discontinuity which remains invisible to the energy flow.

- To prevent problems on uncontrolled impedance transmission lines, the load must be less than 1/6 of the wavelength (67% amplitude reflection)
- The voltage developed is less than ½ of the output voltage, so the reflection is less than the output voltage
- One reflection and the transmission line is stable

- How far is that for a given switching speed?

Switching Frequency vs. Power Source

Frequency	1/20 wave length
5 MHz HMOS Rise time equivalent, 100 nanoseconds Rise time distance, 30m	1,5 m Somewhere in the room
50 MHz (TTL Logic) UDR HCMOS Rise time equivalent, 10 nanoseconds Rise time distance, 3 m	15 cm Somewhere on the board, should be routed as co-planar pairs
500 MHz (BiCMOS Logic) IDR HCMOS Rise time equivalent, 1 nanosecond Rise time distance, 30 cm	1,5 cm Width of your finger, time to look at small geometry capacitors and power islands
5 GHz (GaAs Logic) 65 nm HCMOS Rise time equivalent, 100 picoseconds Rise time distance, 3 cm	1,5 mm (1498.6 µm) In the package
50 GHz 32 nm HCMOS Rise time equivalent, 10 picoseconds Rise time distance, 3 mm	0,15 mm (149.86 µm) On the die

Switching Frequency vs. Power Source

- If the energy source is **not** inside the 1/20 wavelength distance, there will be radiated energy caused by the switching event.
- The job of the PCB designer is to minimize the amount of energy by managing the power delivery system for each type of switching event.
- As the geometry of the ICs we use continues to shrink, so does the area of effective power delivery.
- Well-defined power delivery transmission lines and small geometry, low impedance field storage devices are essential.
- Even if they are outside of the "**zone**," they can minimize the amount of radiated energy.

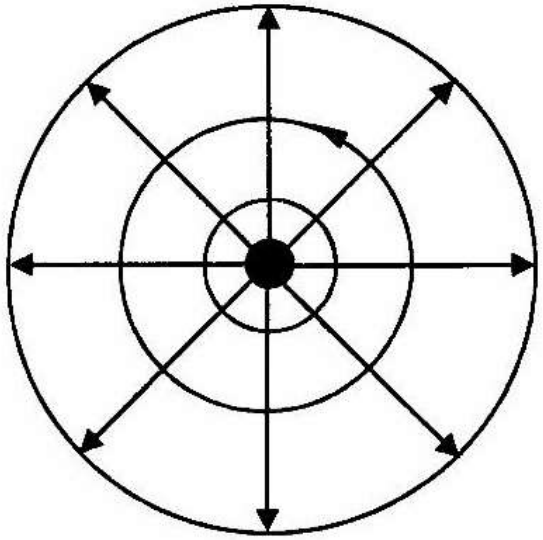
Fields are Friendly!

A contained field is a friendly field:

- Happy field in a sphere
- Happy field in a good coaxial cable
- Happy field in a closely spaced transmission line pair
- Happy field between two closely spaced PCB planes

Fields are Friendly!

Coaxial Transmission



No radiation

E and H fields are contained

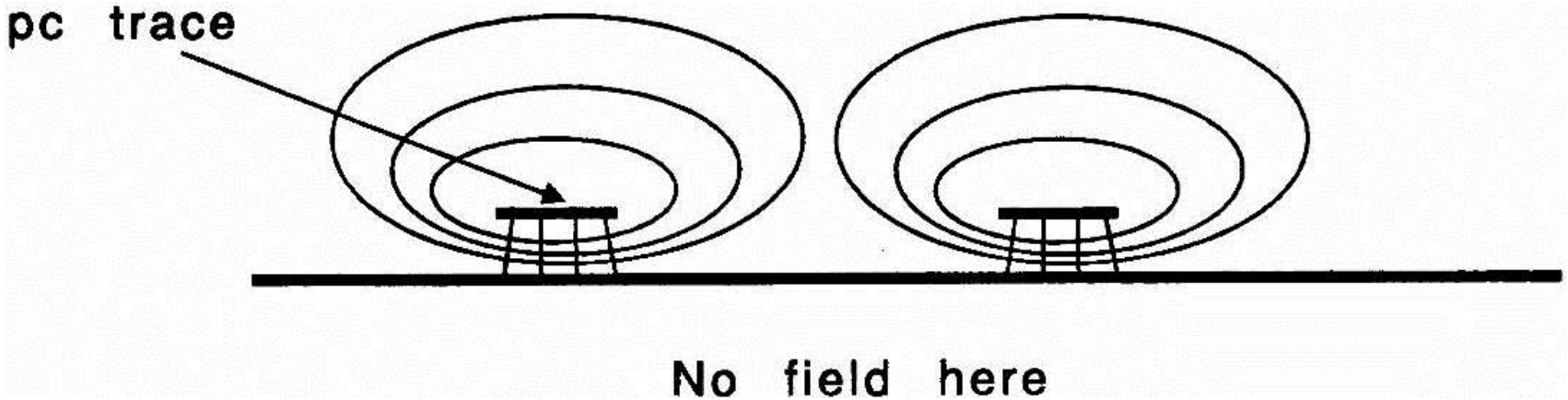
Current return path must be on sheath.

Quiet at home, no reason to roam

(Slide compliments of Ralph Morrison, Consultant)

Fields are Friendly!

Fields concentrate under the traces and there is little crosstalk.



Fields do not penetrate the plane.

Quiet at home, no reason to roam

(Slide compliments of Ralph Morrison, Consultant)

Fields are Friendly!

Fields need to be carefully managed:

- Every connection must be treated as part of a transmission line pair
- Field volumes (read *transmission line impedance*) must be carefully managed
- Each discontinuity (read *change in transmission line GEOMETRY*) results in reflections
- Each segment of this geometry must have enough field energy delivered to match the field density (read *voltage*) from the driver

- **This all takes TIME**

- Yes, this is now **a four-dimensional geometric** design problem

Well-Defined Transmission Lines

- Signal traces *must* be one dielectric away from the return!
  - Adjacent to planar copper
  - Adjacent to ground trace
    - Any deviation from this *must* be an engineered compromise, *not* an accident of signal routing
  - Any deviation from this *will* increase radiated emissions, degrade signal integrity and decrease immunity

- Unless a transmission line is required to be controlled impedance (*read receiver is more than 1/6th wavelength away*), the goal should be the lowest possible (practical) impedance.

This is a very serious problem and a big change from normal board design philosophy

Well-Defined Transmission Lines

- Good news is that any discontinuity that is less than 1/6th wavelength is virtually invisible to the signal
  - Routing schemes need to be driven by the transistor geometry

- Any failure to insure that both signal and ground copper are contiguous (and adjacent) results in large discontinuities that will cause signal integrity and EMC issues
  - Vertical transitions can not be not excluded
    - This is the most common mistake made in otherwise good designs

HOW TO USE THIS WONDERFUL INFORMATION

Where Do We Start?

- Board outline / usually pre-determined
  - Defined by previous product
  - Customer requirements
- Placement

1. Pre-defined components / usually connectors
2. Filter components / high priority, must be as close to the pins as allowed by manufacturing
3. Power control / as close to connector involved as possible

   Voltage regulators

   Power switching devices

   See number 2 above

Schematics Must Be Evaluated During Layout

Arbitrary connections can be redefined to improve layout

- Unscrambling nets can result in:
  - Reduced complexity
  - Reduced trace length
  - Improved EMC performance

- Signals that are not defined to specific pins
  - GPIO on MCUs
  - A/D pins on MCUs
  - Address and data lines to memories
    - No, the memory does not care what you call each pin.
    - They are just address and data, not Addr14 or Data12

Schematics Must Be Evaluated During Layout

Pin assignment to connector signals

- Most connectors do not have adequate signal returns defined
- Unfortunately, these are often either legacy or defined by the wiring harness
- When possible, this can result in significant improvement in EMC behavior
- Can have significant impact on layout complexity

Pin Assignment to Connector Signals

Ideal connector pin assignment:

PGSGSGSGSGP

GSGSGSGSGSG

Not exactly economical or practical

More practical and fewer ground pins:

SSSGSSSGSSP

SGSSSGSSSGP

Each signal is only 1 pin spacing from ground

Pin Assignment to Connector Signals

Signals can be evaluated to route most critical signals adjacent to ground pins

- Highest priority, adjacent to ground labeled **A**,
- Lower priority, diagonally adjacent to ground labeled **B**,
- Next lower priority, one pin position away from ground labeled **C**

BAAGAAAGAAP

AGAAAGAAAGP

This can be applied when you are not allowed sufficient returns, but will improve EMC

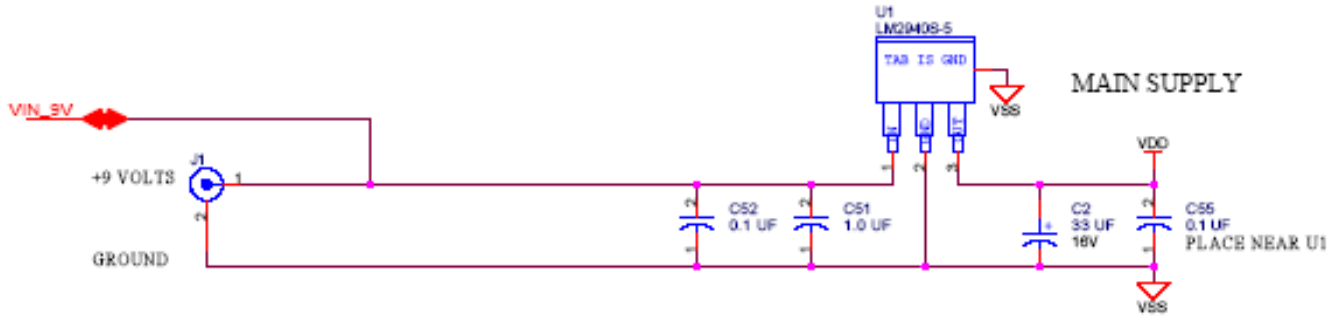
DCAGACDCBAP

DCBABCDCAGP

Pin Assignment to Connector Signals

- **Schematic is often lacking in order definition**

- **Capacitors must be placed in the daisy chain in the correct order**



Uncontrolled Component Placement

You get to decide!

- Placement not specified by customer or company requirements

- Evaluate component domain
  - Power
  - Sensor
  - Digital IC

- Place to limit signal mixing
  - Route power only in power realm
  - Route sensor lines only where needed
  - Digital IC connections only in digital realm

Uncontrolled Component Placement

- Power realm devices must be placed near connectors
  - Shorter traces
  - Cleaner returns
  - Reduced field volumes (Yes, this is a three-dimensional consideration)
- Don’t forget their supporting cast
  - Bypass capacitors, Inductors, resistors
  - Use the largest value capacitor in the smallest package allowed by manufacturing and reliability
- Digital realm devices
  - Technology (geometry) of each device
  - Function
  - Devices placed within lumped distance do not need terminating resistors
  - 1/6 wavelength of the IC switching frequency, not clock frequency (determined by IC geometry) Yes, this is important to know … sometimes controlled by variable drive strength
  - For 1 ns switching speeds (500 MHz) this is about 50mm!

[3] Comment compliments of Dr. Todd Hubing, Clemson University

Uncontrolled Component Placement

- Remember, if you do not route signals where they don’t need to be, there will *not* be any crosstalk or interference.
- This is easier if you do *not* mix the parts together.
- If the traces are not near each other, there is no magic that will cause them to interfere with each other.
- Can I say this any other ways? Is this important, **YES**!
- Let’s move on to actually routing the board…

POWER DISTRIBUTION

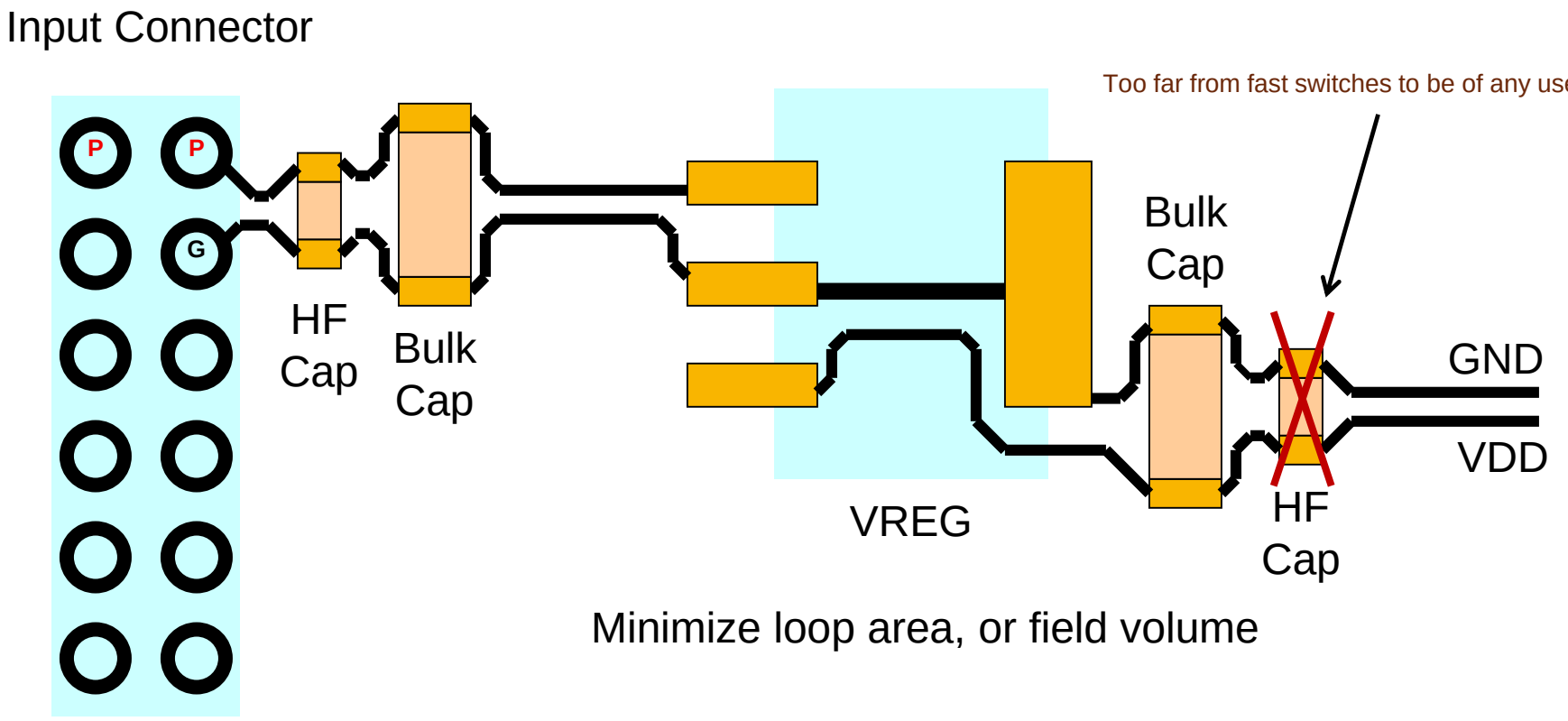
PCB ~~signal~~ Transmission Line Routing

- The first and most important job is to route the power distribution network – it is the source of all of the electromagnetic energy you will be managing on the PCB.

- On low layer count boards, with no dedicated ground plane, the power lines must be routed in pairs
  - Power and ground
  - Side by side
    - Trace width determined by current requirements
    - Spaced as close as manufacturing will allow them
  - Daisy chain from source to destination, connecting to each component, then finally to target devices

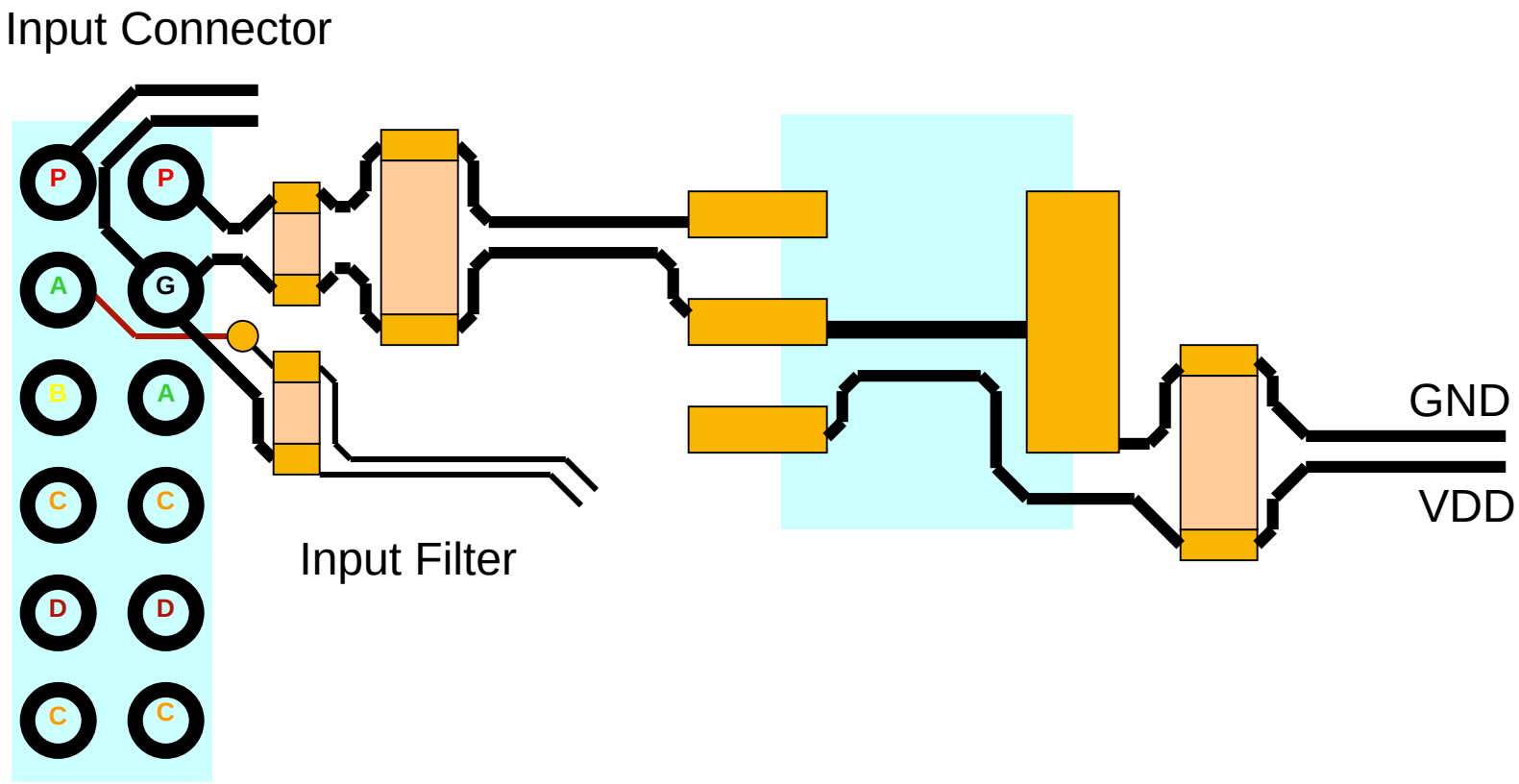
- Minimize the *volume* of the *power transmission* network

PCB ~~signal~~ Transmission Line Routing



DESIGNING GOOD TRANSMISSION LINES

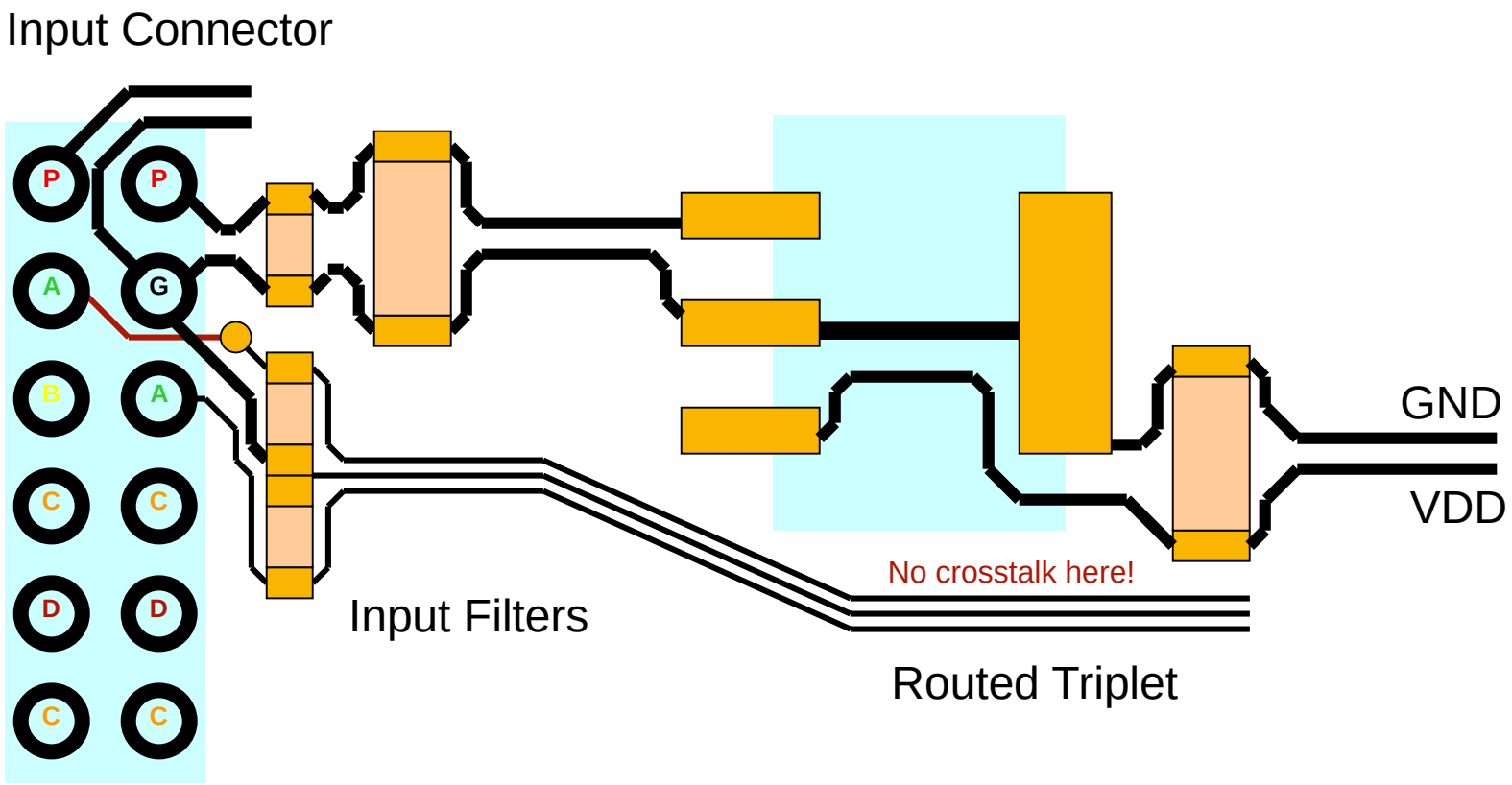
PCB ~~signal~~ Transmission Line Routing



PCB signal Transmission Line Routing

- Input filters must be placed as close as allowable to connectors
- Connections must be directly to the connector ground pins
- Route traces with well defined return path
- Minimize the volume of the signal transmission network

PCB ~~signal~~ Transmission Line Routing

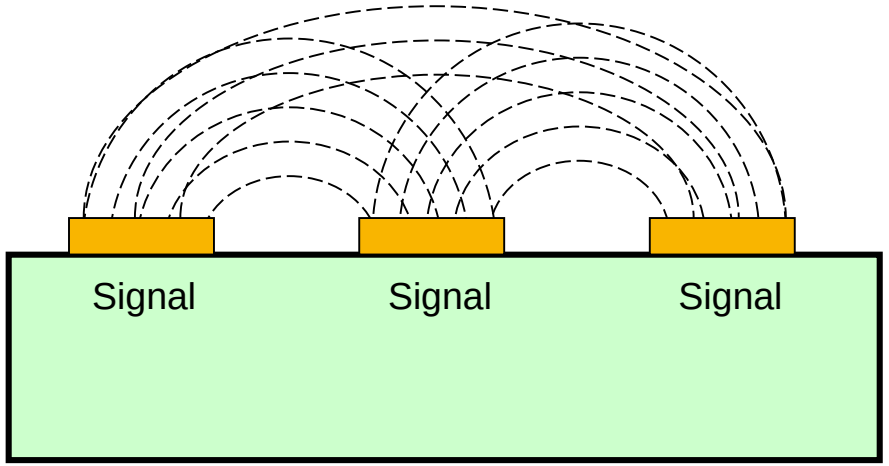


PCB ~~signal~~ Transmission Line Routing

- Routing in “triplets” (**S**-**G**-**S**) provide good signal coupling with relatively low impact on routing density
- Ground trace needs to be connected to the ground pins on the source and destination devices for the signal traces
- Spacing should be as close as manufacturing will allow
- Minimize the volume of the signal transmission network

PCB ~~signal~~ Transmission Line Routing

You really want to make sure that the field energy is coupling to the conductor you choose!



Note: All field lines actually terminate at 90 degree angles

PCB ~~signal~~ Transmission line routing

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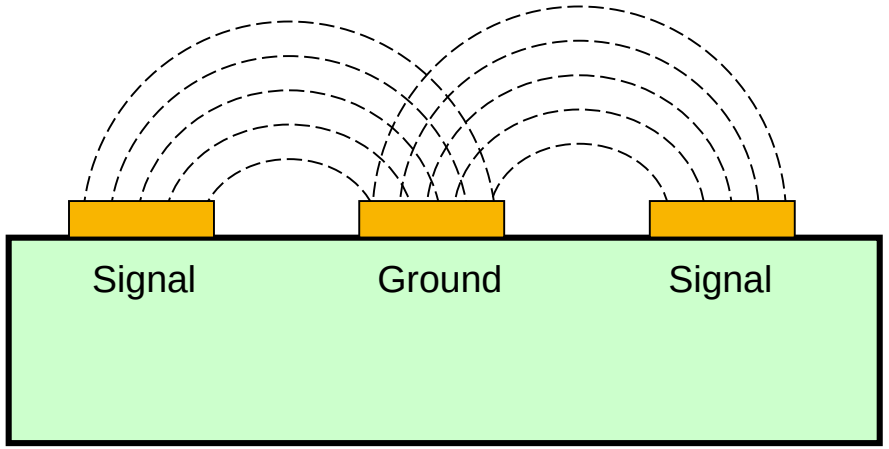
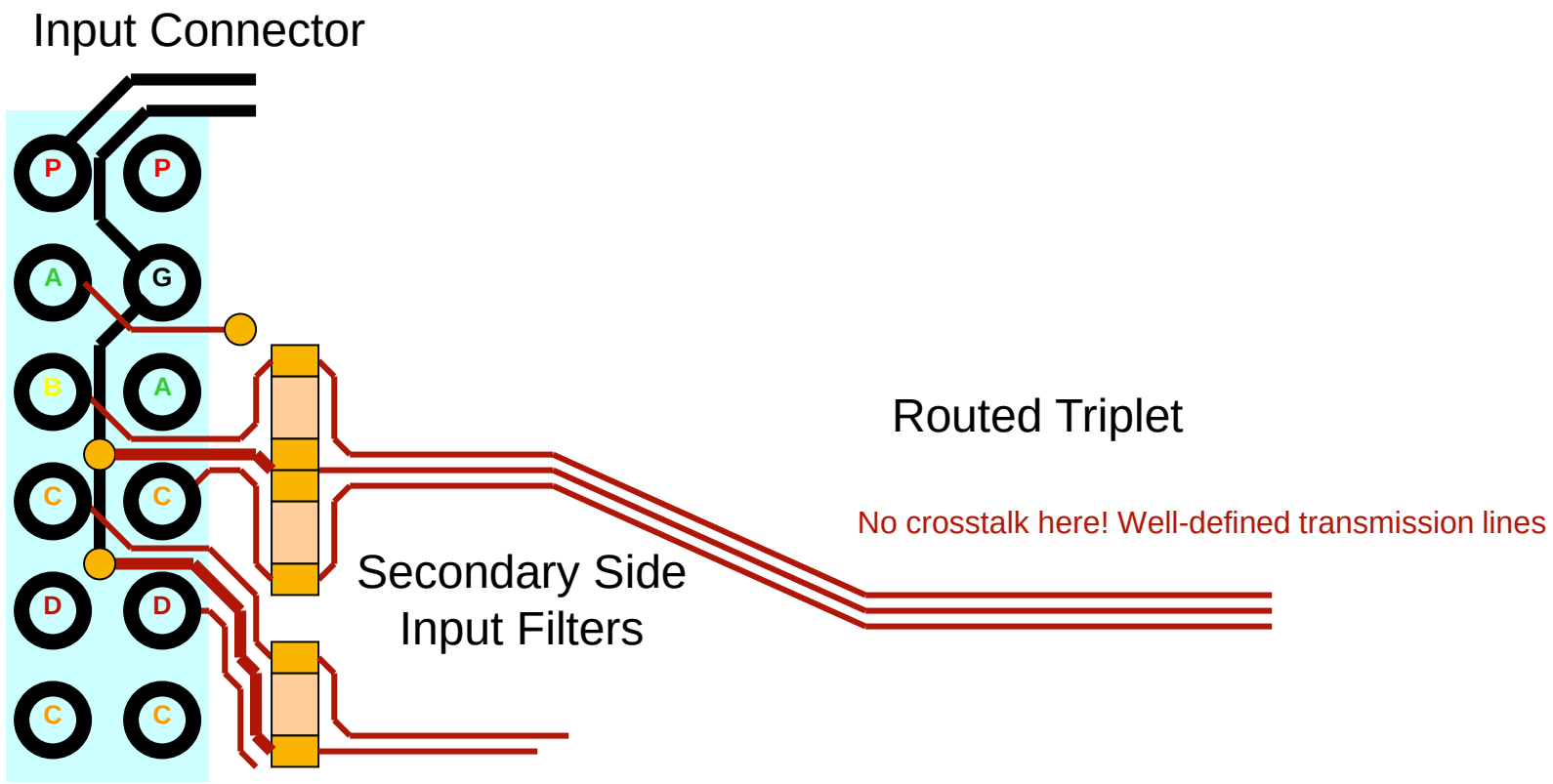


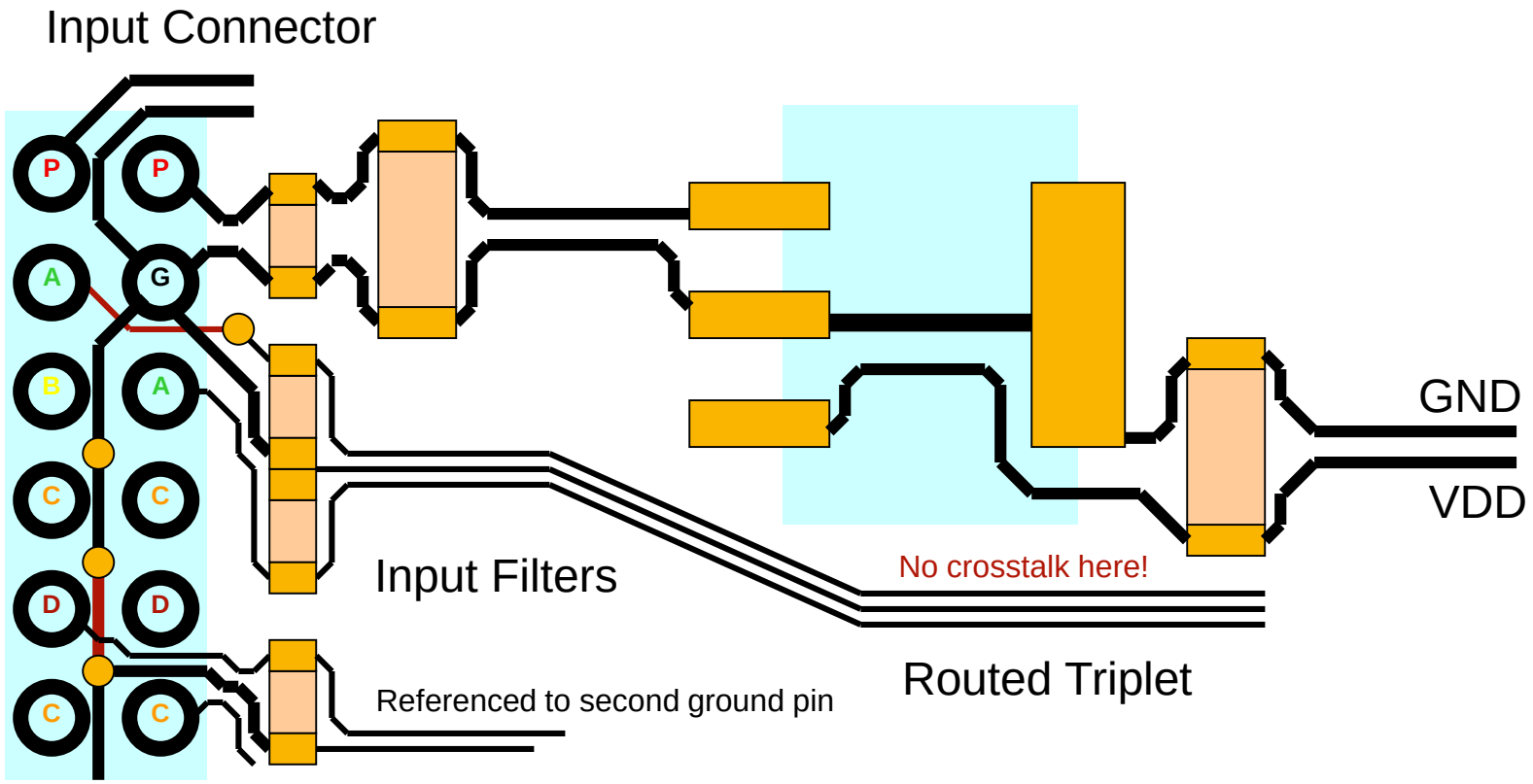
Note: All field lines actually terminate at 90 degree angles

Maybe a “triplet” makes sense?

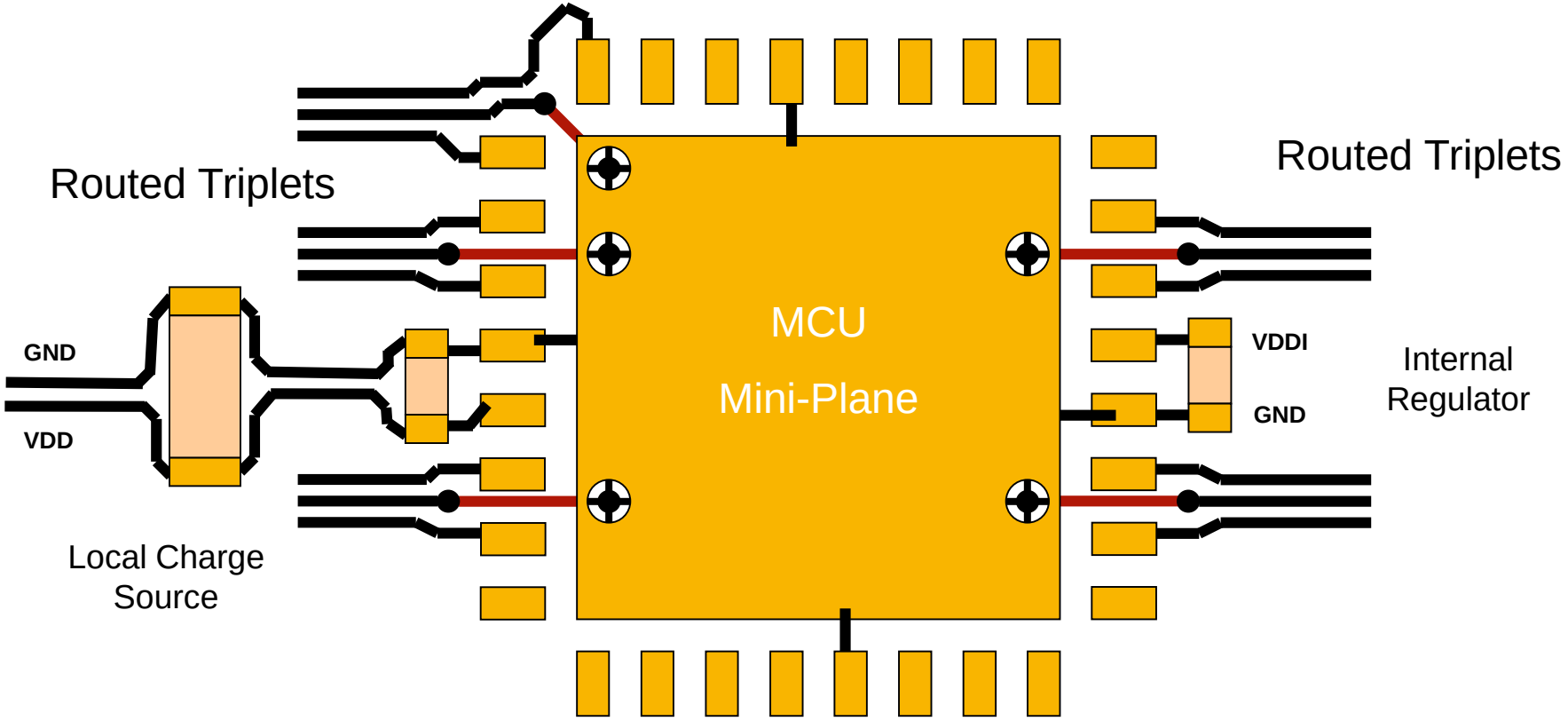
PCB ~~signal~~ Transmission line routing



PCB ~~signal~~ Transmission line routing



PCB ~~signal~~ Transmission line routing



PCB ~~signal~~ Transmission Line Routing

- Lead frame and wire bonds are parts of transmission lines, too

- Mini-plane under the QFP provides improved EMC
- Triplet ground traces can be easily coupled to the mini-plane on secondary side

- In high density applications, even routing with “quints” (**S**-**S**-**G**-**S**-**S**) will provide some improvement

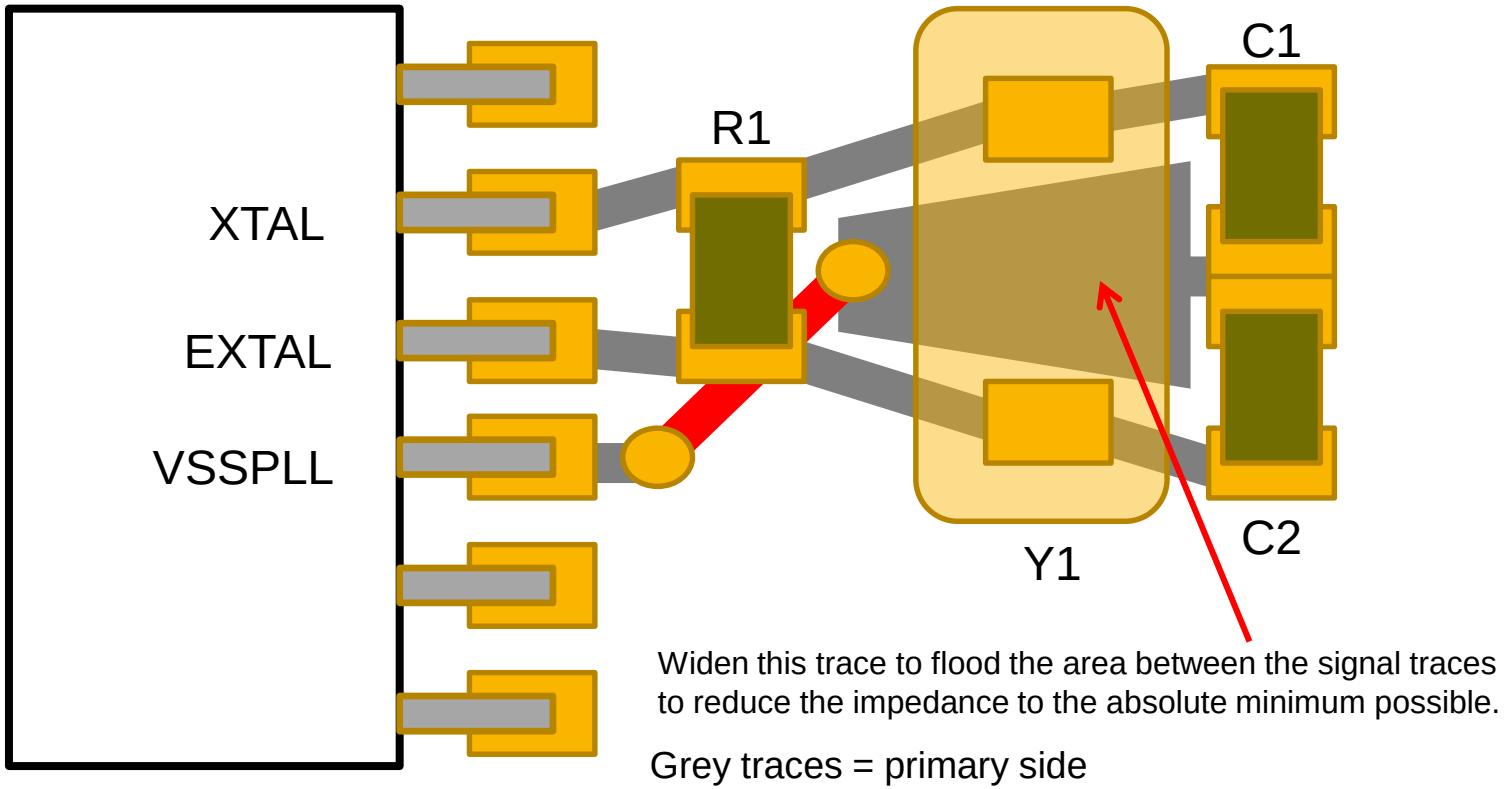
- You know where most of the field energy is going!

- Last but not least, flood everything with ground copper!
- Must be able to tie each “island” with at least two via to adjacent layer ground

- Minimize the volume of the signal transmission network

PCB ~~signal~~ Transmission Line Routing

- Oscillator ground must be routed to MCU pin, not tied to System Ground
- Connect System Ground on the opposite side of the MCU pin



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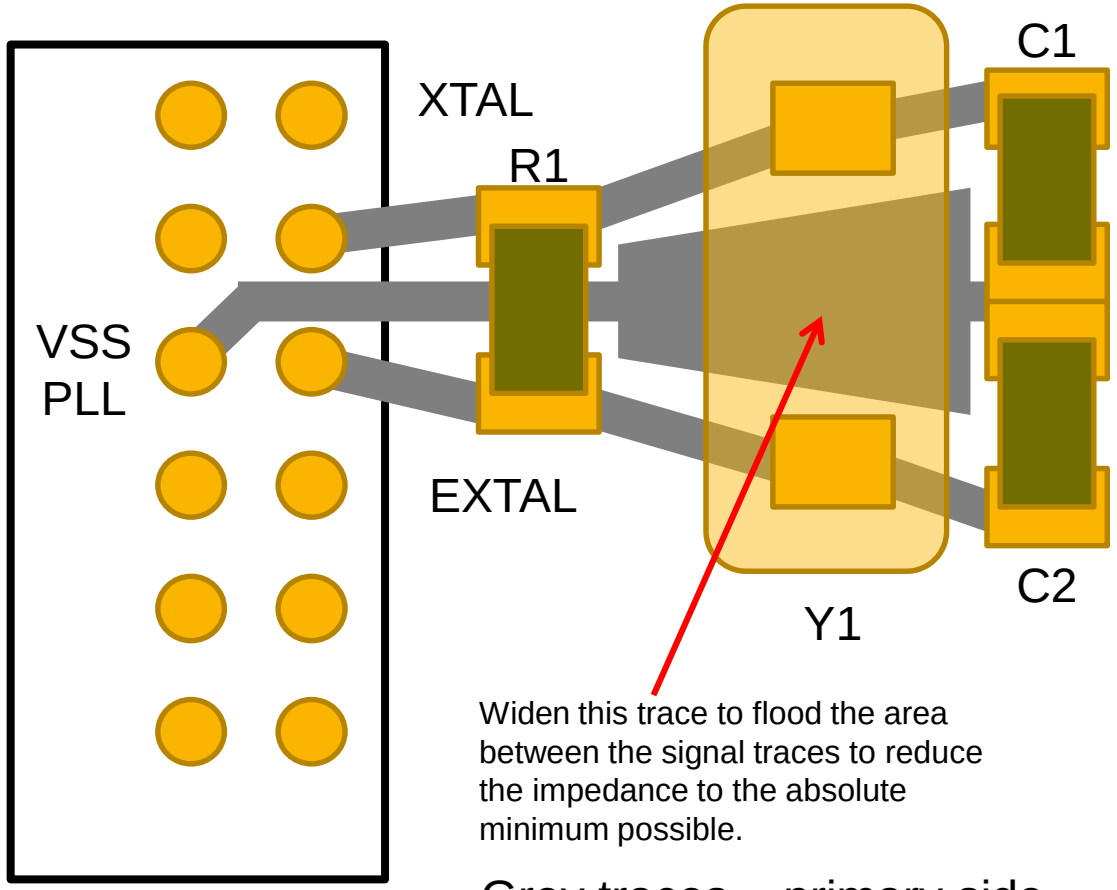
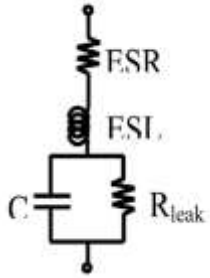


Why This Works

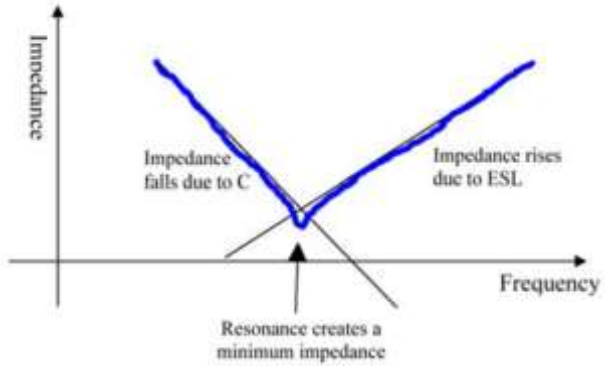
- Crystal output from MCU is the POWER source
  - Energy flows out, between the MCU output signal trace and MCU oscillator ground trace to the crystal or resonator
- Crystal becomes POWER source
  - Energy flows back, between the crystal output signal trace and the oscillator ground trace to the MCU input pin
- This is a closed loop system, and SYSTEM ground is not required
  - Lower impedance for the connecting transmission lines
  - Smaller loop area
  - Significantly improved robustness
- It is always about “Where does the energy come from?”
- This rule should be applied to the entire design
  - Ground for any signal is determined by the power source return
- Another important fact is that this is a low amplitude, low frequency, analog circuit. It is not required to be placed as close as possible to the MCU, just that it must be connected with transmission lines as described above. Moving these components can allow for placement and routing of more critical components in the area near the MCU.

Filtering a higher bandwidth

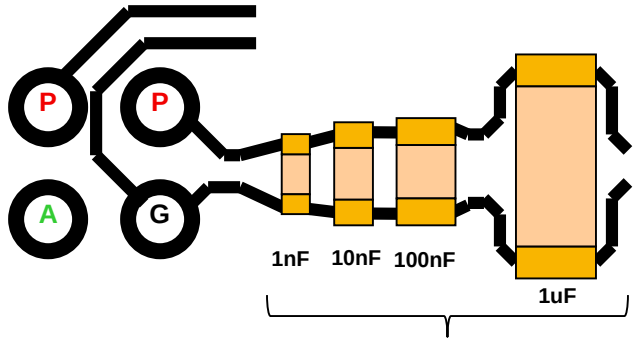
- To filter a higher bandwidth it's recommended to add more capacitors in parallel.
- Each capacitor value/package filter a defined range of frequencies.



Abbrev	Explanation	Source and Details
ESR	Equivalent Series Resistance	• Wire and connections to the plate • Produces Heat
ESL	Equivalent Series Inductance	• Depends on Package Type • Surface mount better • Smaller SMD better
R_{leak}	Leakage Resistance	• Type of dielectric

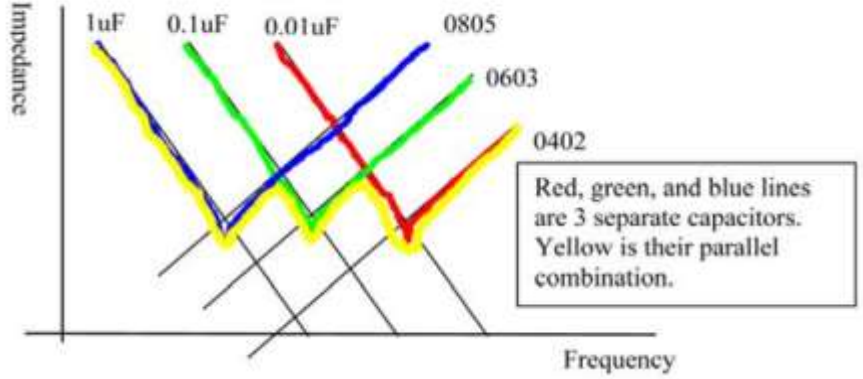


Input Connector



Filtering Capacitors (low ESR)

Close to the noise input path, external connectors



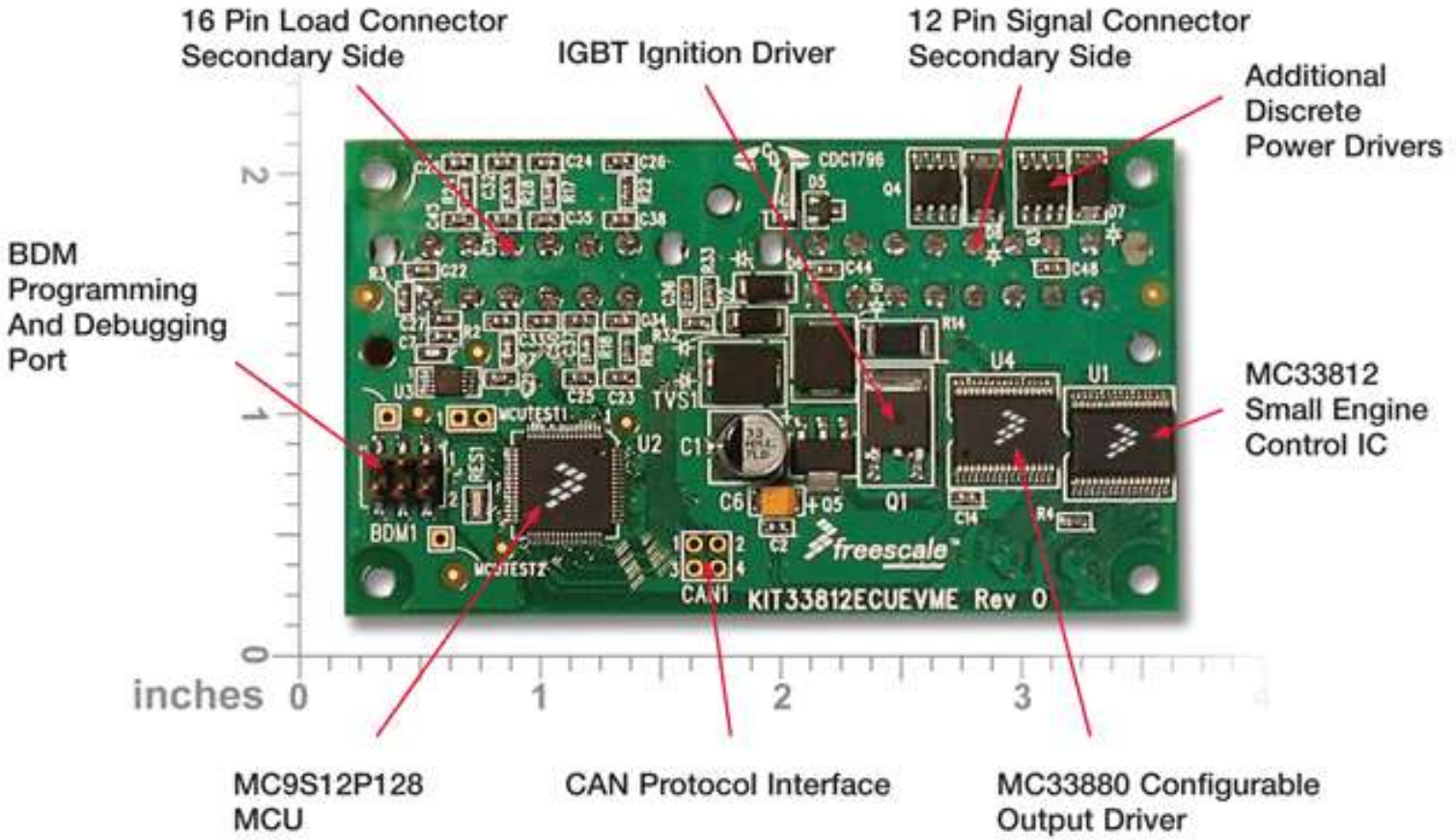
(Slide compliments of Kendall Castor-Perry, Planet Analog)

TEST RESULTS

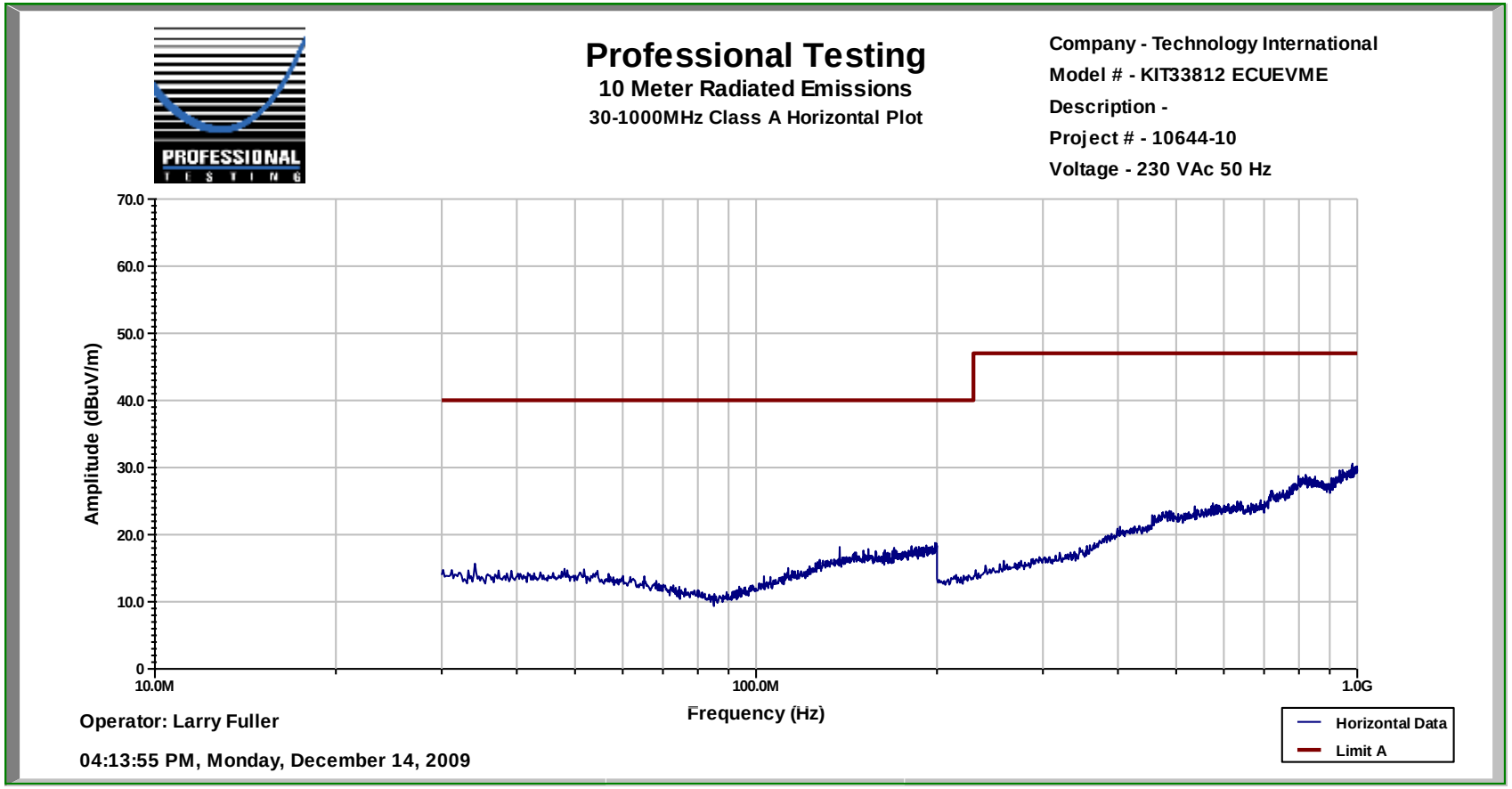
The Proof is in the Testing

- KIT33812ECUEVME Reference Design
  - Intended for motorcycle and other single/dual cylinder small engine control applications
- MC33812 analog power IC
  - Multifunctional ignition and injector driver
- MC9S12XD128 MCU
  - Designed for either the MC9S12P128 or MC9S12XD128
  - Test results are for the older, noisier MCU
- Two-layer PCB
- Business card dimensions
- Implements these design and layout concepts
  - “Smart” connector pinout
  - MCU mini-plane
  - Triplet routing
  - Maximum flooding

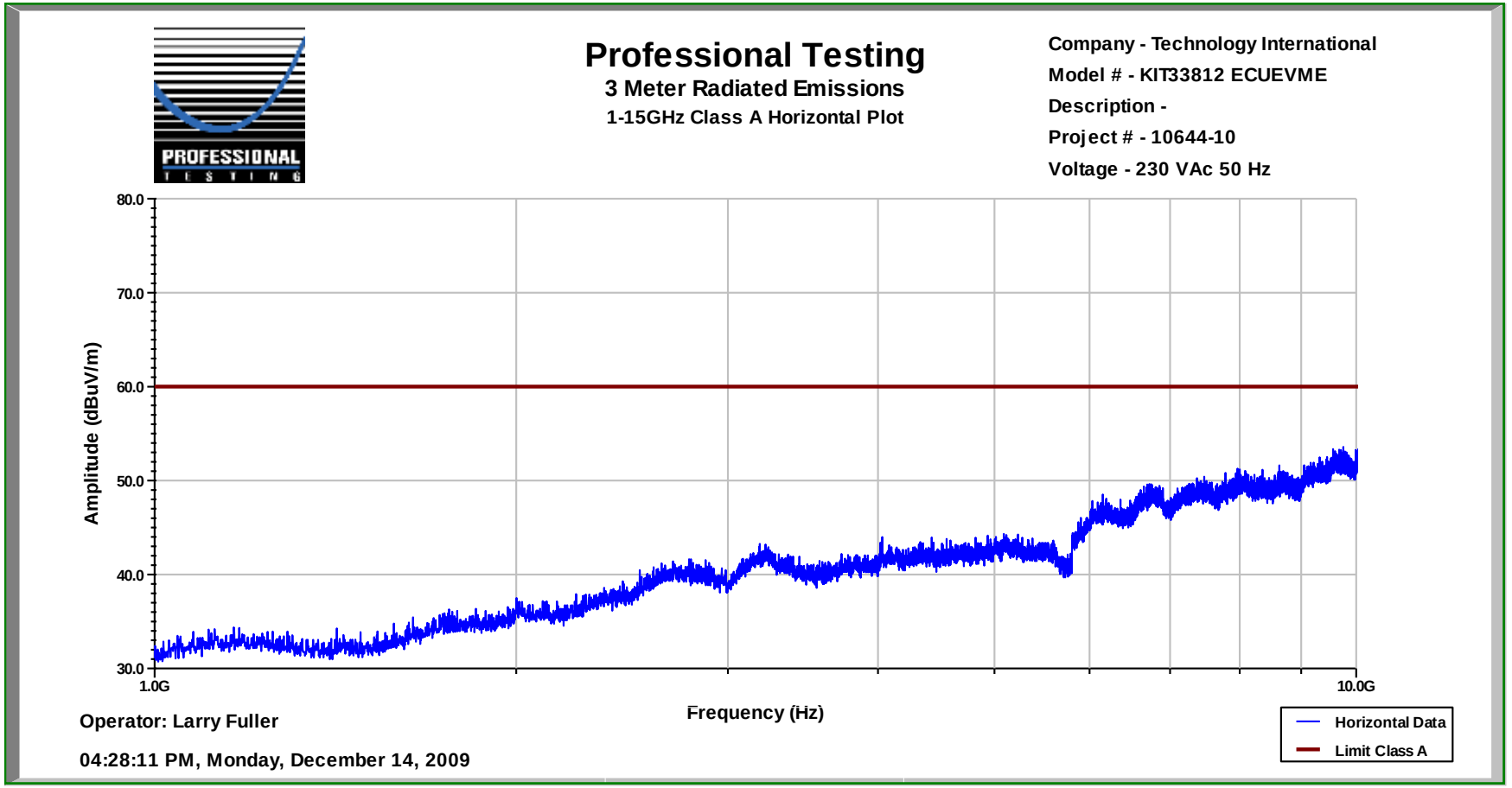
KIT33812ECUEVME Reference Design



KIT33812ECUEVME Reference Design



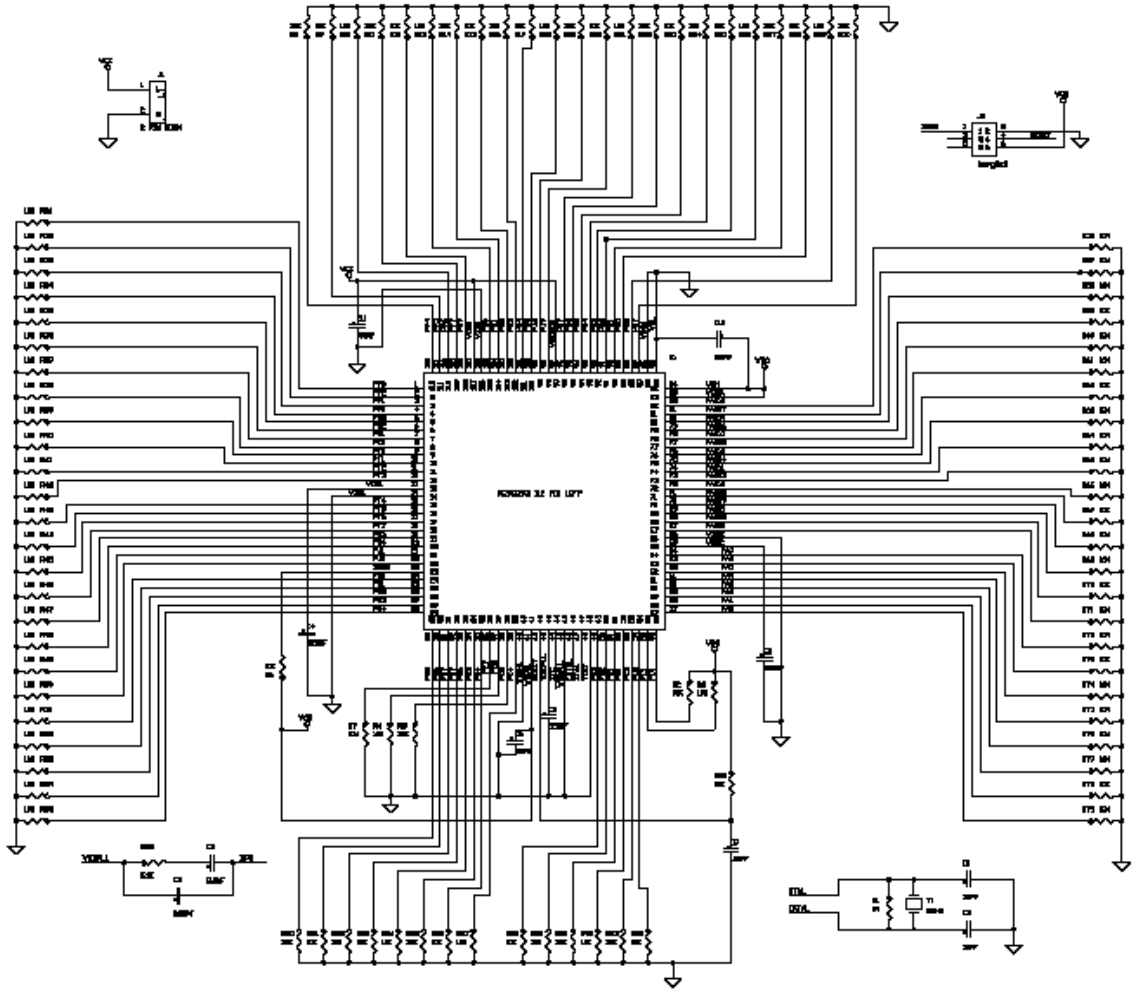
KIT33812ECUEVME Reference Design



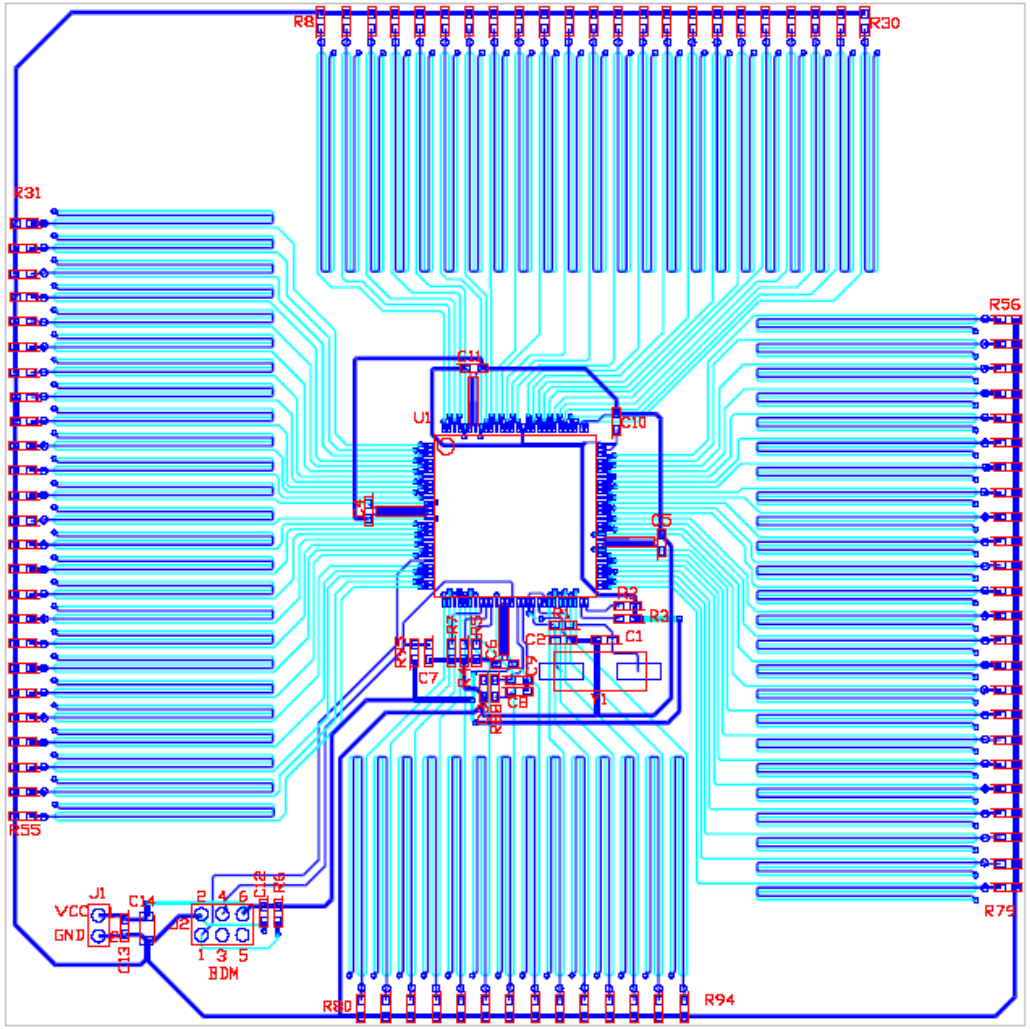
EMC Test Board

- EMC test board with no field control considered
- Two layers
- 112-pin MC9S12XD128 MCU
- All I/O lines routed to 10 K termination resistors using serpentine 6” traces
- All ground connections routed in “convenient” patterns
- Filter components placed “somewhere near”
- Line widths and spacing aimed for low cost FAB
- Software running at 40 MHz, toggling all I/O pins

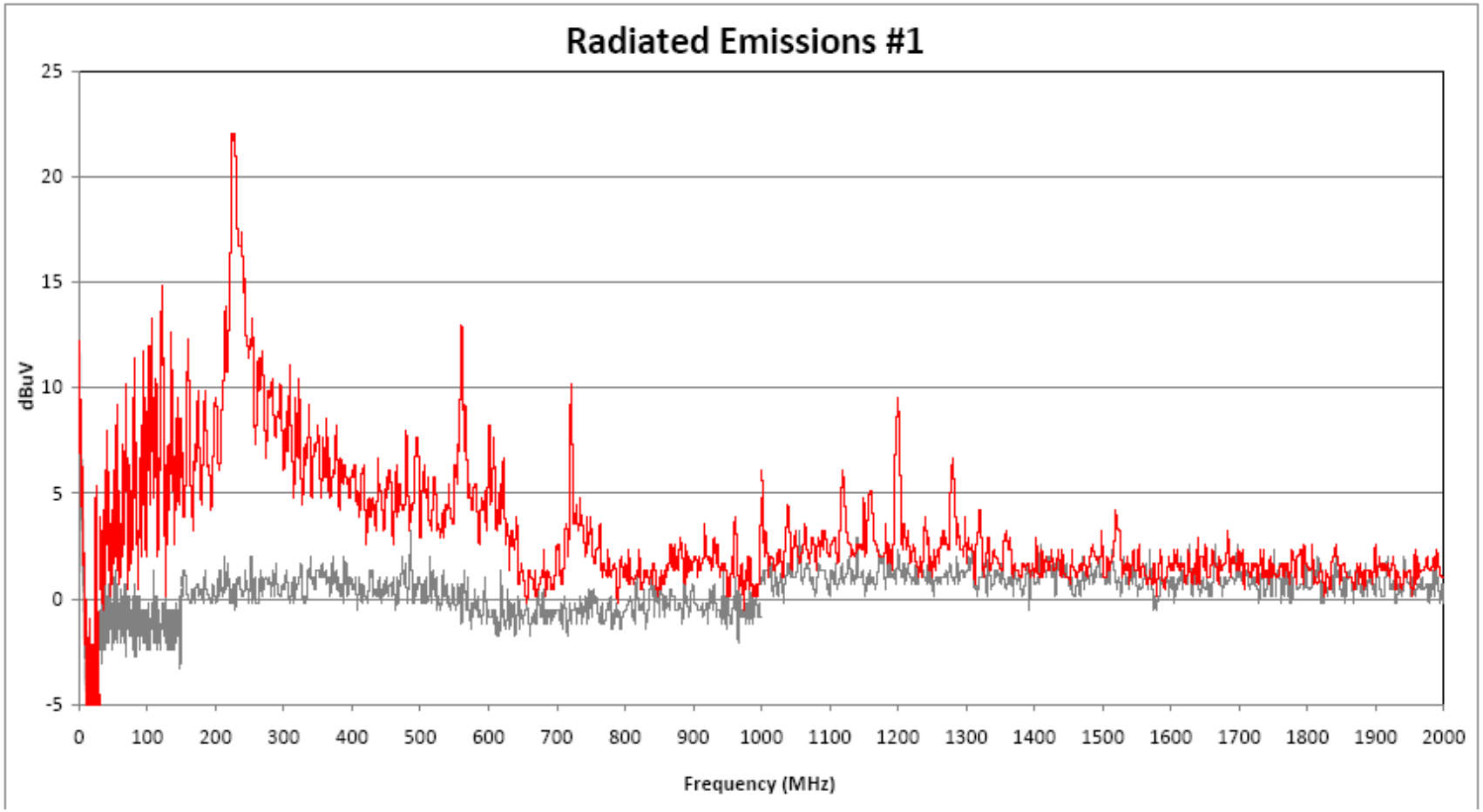
EMC Test Board Schematic



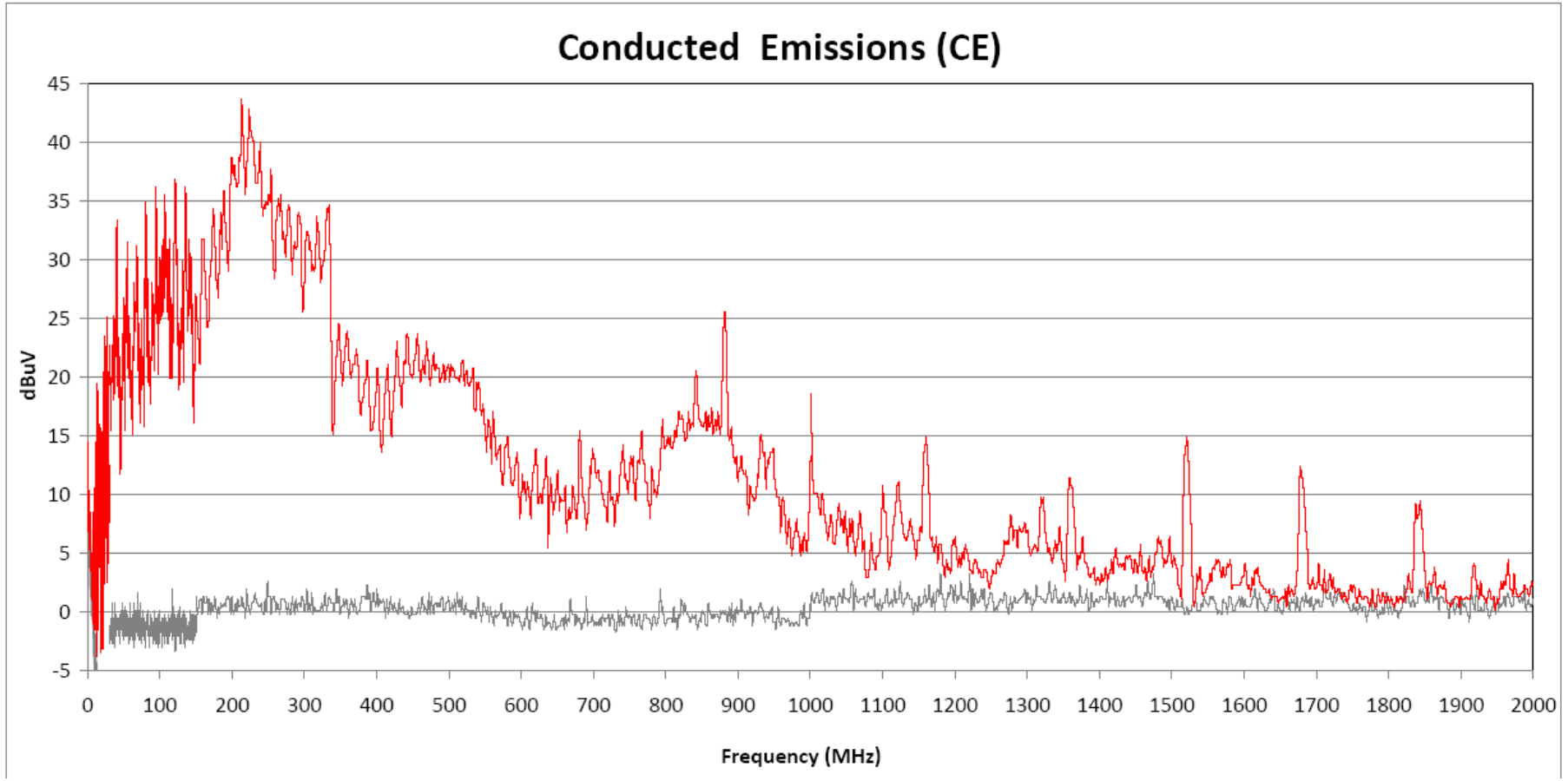
EMC Test Board Layout



Two-layer EMC Test Board Radiated Emissions



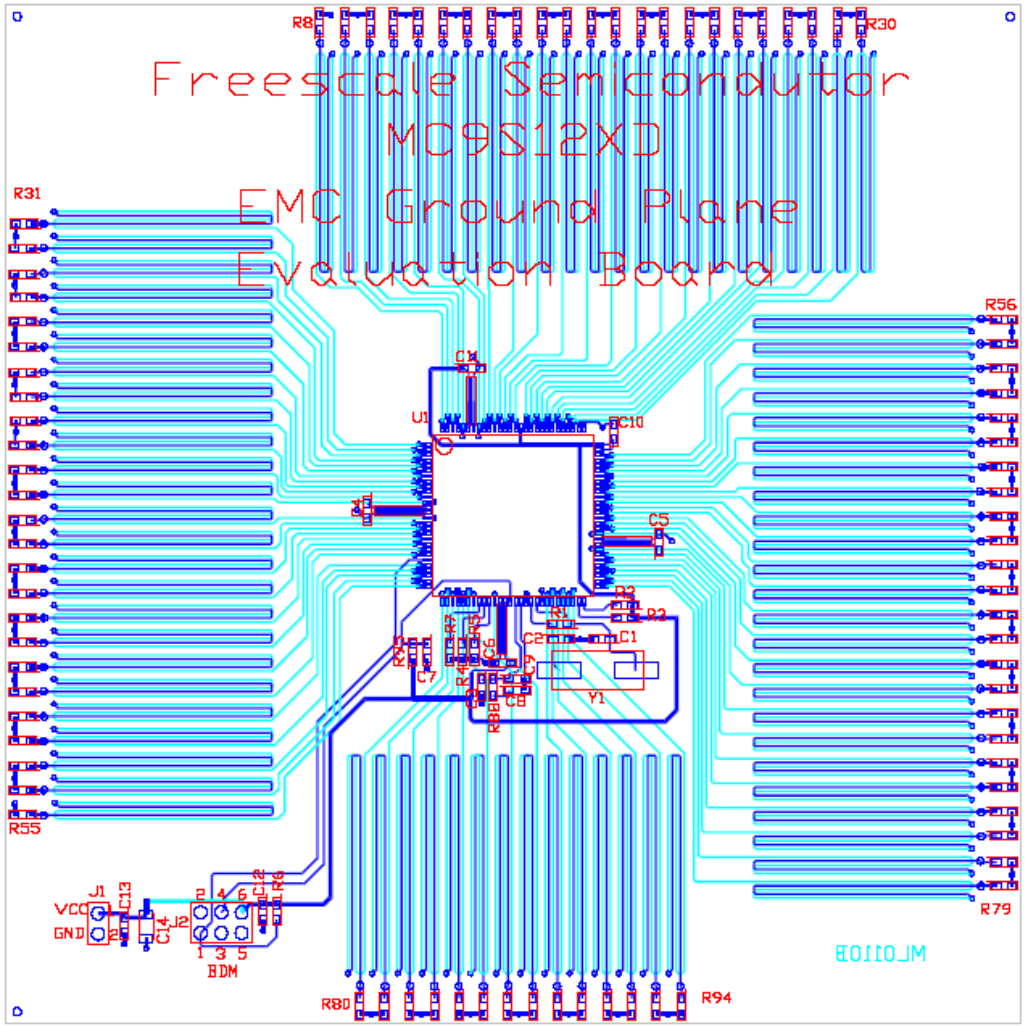
Two-layer EMC Test Board Conducted Emissions



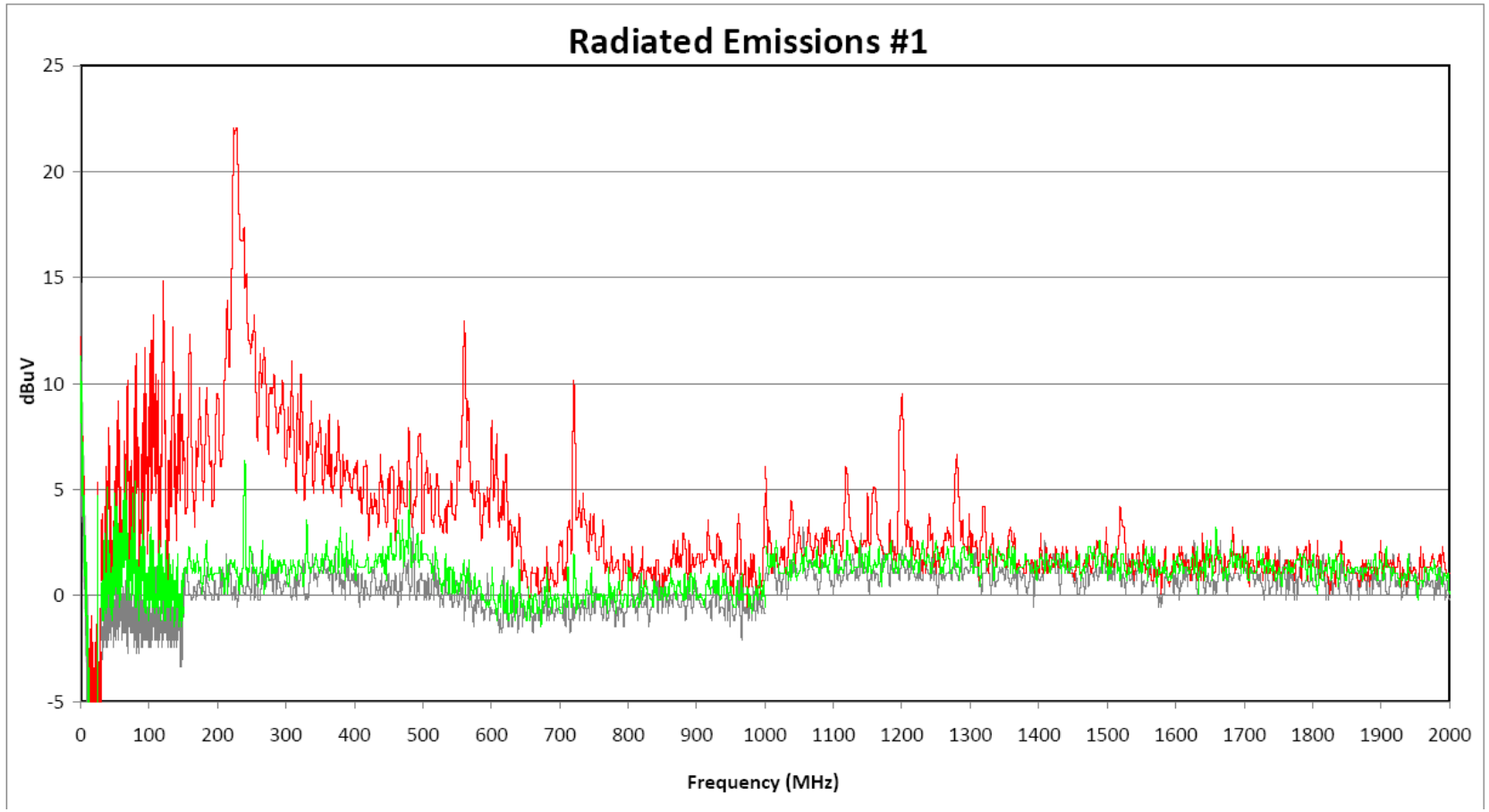
Two-layer EMC Test Board, rev 2

- EMC test board with tight field control considered
- Same schematic
- Four layers
- Core inserted with dedicated ground planes
- Outer layers exactly the same as 2 layer
- All ground connections made with via to ground planes
- Line widths and spacing aimed for low-cost FAB
- Same software

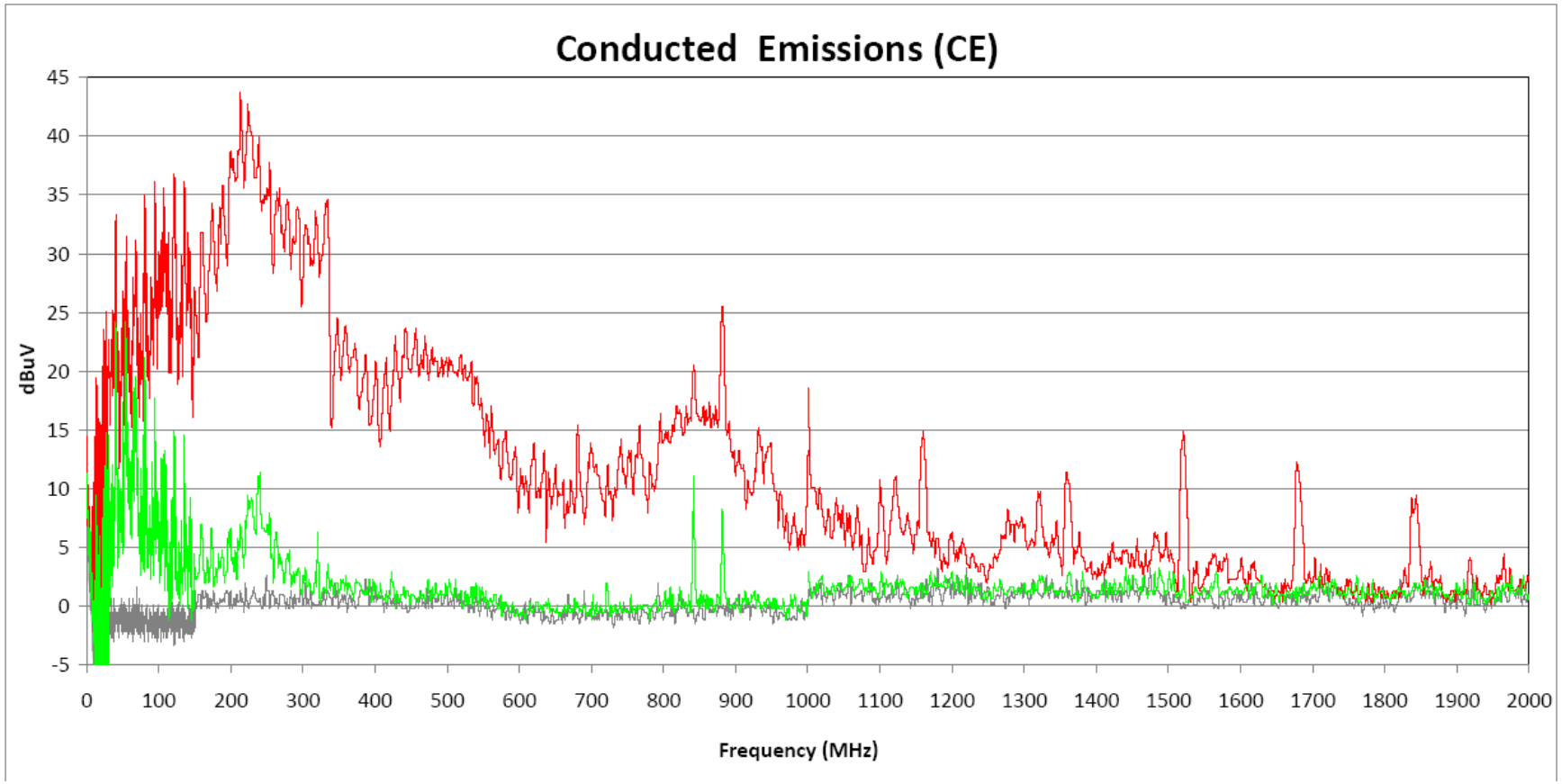
Two-layer EMC Test Board layout, rev 2



2 vs. 4-layer EMC Test Board Radiated Emissions



2 vs. 4-layer EMC Test Board Conducted Emissions



2 vs. 4-layer EMC Test Board Results

WOW!

What would you do for 30 db?

Using EMC Test Results

- EMC test results can be used to identify area of concern
- LFBDMPGMR FCC/CE test result first pass:
  - Radiated immunity
  - “The EUT failed with all LEDs turning off. Manual restart worked. The frequencies that caused this fault were 110 MHz, 112 MHz, 134 MHz and 136 MHz up to 149 MHz. After 149 MHz, the EUT worked properly.”
- Not what you want to see in your e-mail.
- This is a four-layer board, the best I know how to design.
- I know, check the chart to see what the ¼ wave length would be.
- About 1 meter, what? My board is only 4 inches square.
- Aha, the USB cable! I forgot to put a filter on the USB power supply. Add a cap quick.
- Send new board for retest.

Using EMC Test Results

Antenna Size vs. Frequency

Frequency	¼ wave length
1 Hertz Rise time equivalent, who cares	74.980 km Almost 6 times the diameter of the Earth
10 Hertz Rise time equivalent, still who cares	7498 km
100 Hertz Rise time equivalent, .01 seconds	749 km
1 KHz Rise time equivalent, 1 millisecond	75 km
10 KHz Rise time equivalent, 100 microseconds	7,5 km
100 KHz Rise time equivalent, 10 microseconds	749 m
1 MHz Rise time equivalent, 1 microsecond	74,9 m
10 MHz Rise time equivalent, 100 nanoseconds rise time distance, 30,48 m	7,49 m
100 MHz (TTL Logic) **Rise time equivalent, 10 nanoseconds rise time distance, 3,04 m**	**74,9 cm**
1 GHz (BiCMOS Logic) Rise time equivalent, 1 nanosecond rise time distance, 30,4 cm	7,49 cm
10 GHz (GaAs Logic) Rise time equivalent, 100 picoseconds rise time distance, 3,04 cm	0,74 cm
100 GHz (nanometer geometry HCMOS) Rise time equivalent, 10 picoseconds rise time distance, 3,04 mm	0,74 mm

NEW RULES OF THUMB

More PC Board Considerations

Flooding unused spaces on the PCB:

- Properly implemented, will improve EMC performance
- Reduce cost by increasing PCB manufacturing yield
  - Less etch required
  - Balanced copper improves plating
  - Balanced copper improves final assembly
    - Reduced board warping
- Remember to stitch the ground islands and planes together
- Trying to make a pseudo-Faraday cage!

More PC Board Considerations

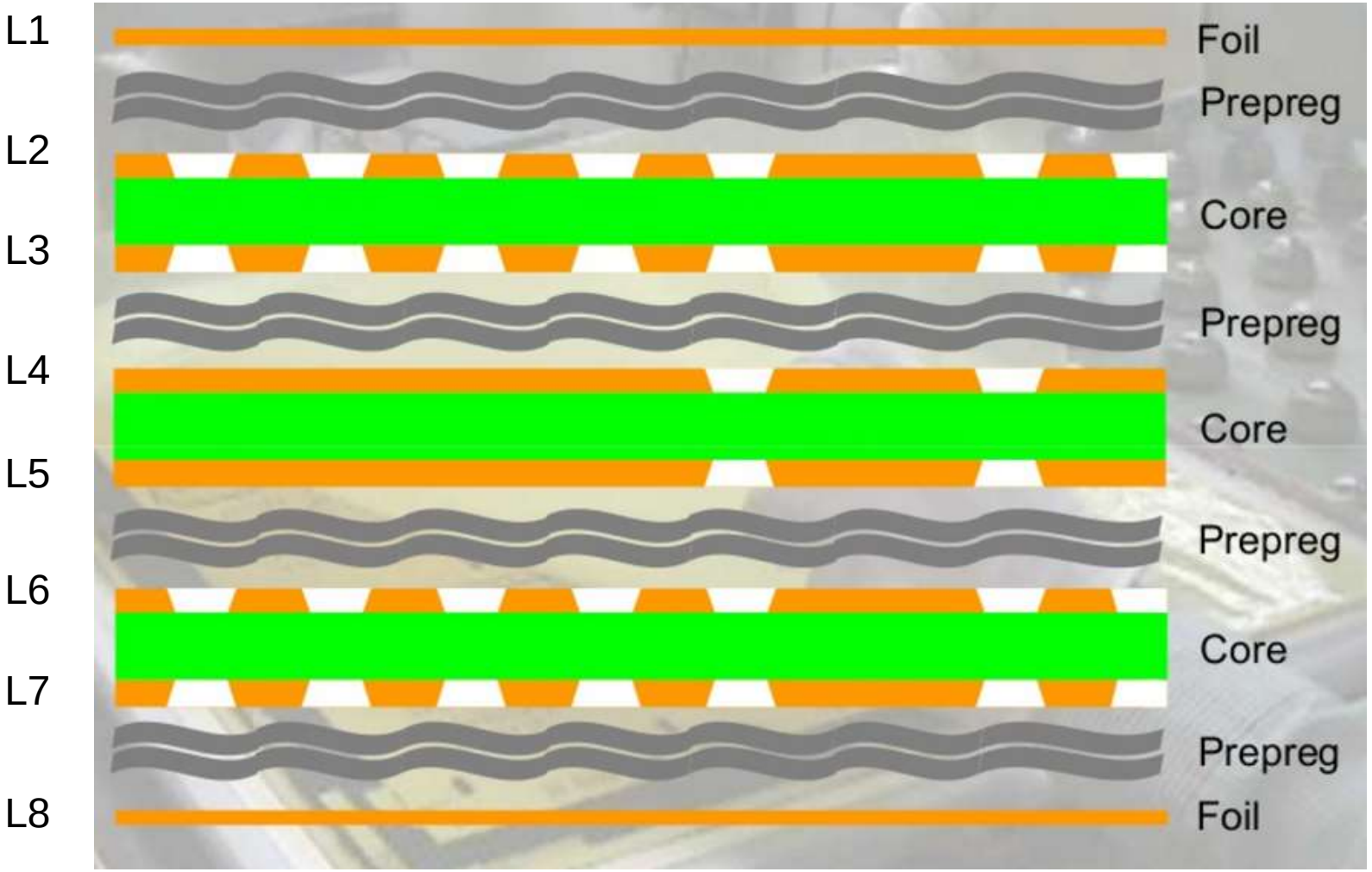
- Use minimum trace widths and spacing for signal transmission lines

- Refer to PCB fabricator’s capabilities without a cost adder
- Same thing goes for drill sizes and pad rings
- May be defined by either customer or internal requirements
- Wider traces for power supply transmission line pairs
- Provides maximum trace density

- Make room for all of those ground traces!

More PC Board Considerations

Most PC boards are “foil laminated”



Eight-Layer Boards

- Made from three 2-layer cores, L2 and L3, L4 and L5, L6 and L7
- L1 and L8 made by adding pre-preg layers and copper foil
- Use the “fattest” core and “thinnest” pre-preg possible without a cost adder from fabricator
  - You will have to find this out
  - Your company or customer may have some min-max specs for these materials
- **Maximum coupling is from L1 to L2 and from L7 to L8**

Four-Layer Boards

- Most effective stackup has one ground layer
- L2 ground means that L1 and L3 are one dielectric from ground
- L4 must be routed as a single layer board, with following ground traces (triplets?)
- Ground transition vias are required when signals go from layer 4 to any other layer to insure the transmission line is continuous

Six-Layer Boards

- Most effective stackup has two ground layers
- L2 as ground means that L1 and L3 are one dielectric from ground
- L5 as ground means that L4 and L6 are one dielectric from ground
- Ground transition vias are required when signals go from one ground reference group (L1-L2-L3 or L4-L5-L6) to any other layer in the other group) to insure the transmission line is continuous

Layer Count Determinations

- Technology of the devices used
- Trace density
- EMC certification level
  - Consumer/commercial
  - Automotive
  - Aviation
  - Military

- All must be considered, not just trace density!

Layer Count Determinations

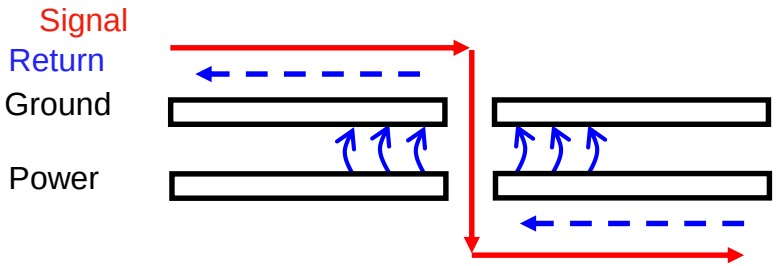
- Must be a conscious decision based on proper electromagnetic field control
- Not just because you ran out of routing paths
- Smaller IC geometries will require more layers and most likely power and ground planes
- It will not be possible to provide a good power distribution network or good signal integrity without adding planes
- System cost is *not* reduced by reducing IC geometries!

Using Planes

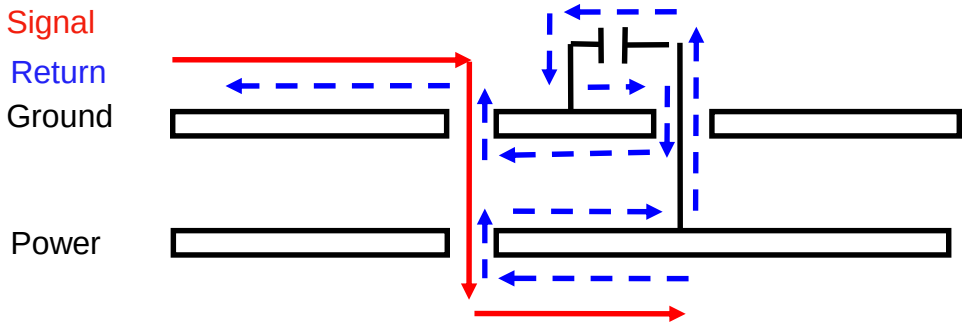
- Both power and ground can be used as signal references
- Transition from one reference plane to another requires close proximity to a bypass capacitor
- That is the only way the field can move!
- *Only* if they are well coupled to each other
- Using Capacitors
  - Impedance is less than 0.1 ohm
- Planes adjacent to each other
  - Dielectric thickness less than 10 mils

Using Planes

When routing signals with returns between power and ground planes, return energy will transfer as follows:



Tightly coupled planes

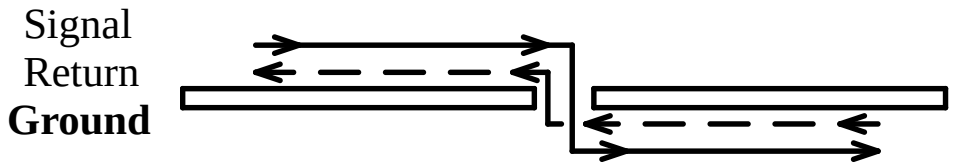


Loosely coupled planes with cap

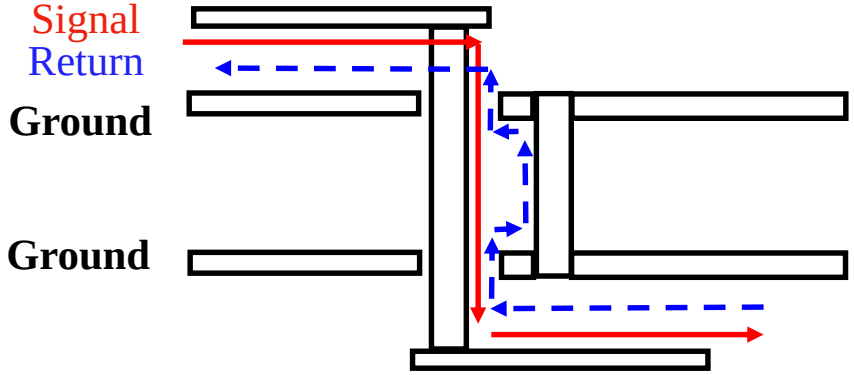
(Slide compliments of Rick Hartley, Consultant)

Using Planes

- When moving signals *between layers*, route on either side of the same plane, as much as possible!



- When moving signals *between two different planes*, use a transfer or “ground transition” via very near the signal via.



(Slide compliments of Rick Hartley, Consultant)

Using Planes

- **Remember, field energy moves in the space between or around the conductors and cannot go through them**
  - That means through the holes in the planes – not inside or on the vias, around them!

- **You must provide the path you want, or the field will find its own path**
  - It will most likely be the one that causes the most problems!

[1] **Statement compliments of Ralph Morrison, Consultant**

Splitting Ground planes

Splitting ground planes is almost never a good idea

- Only when required by customer or internal specifications
- Question those requirements!

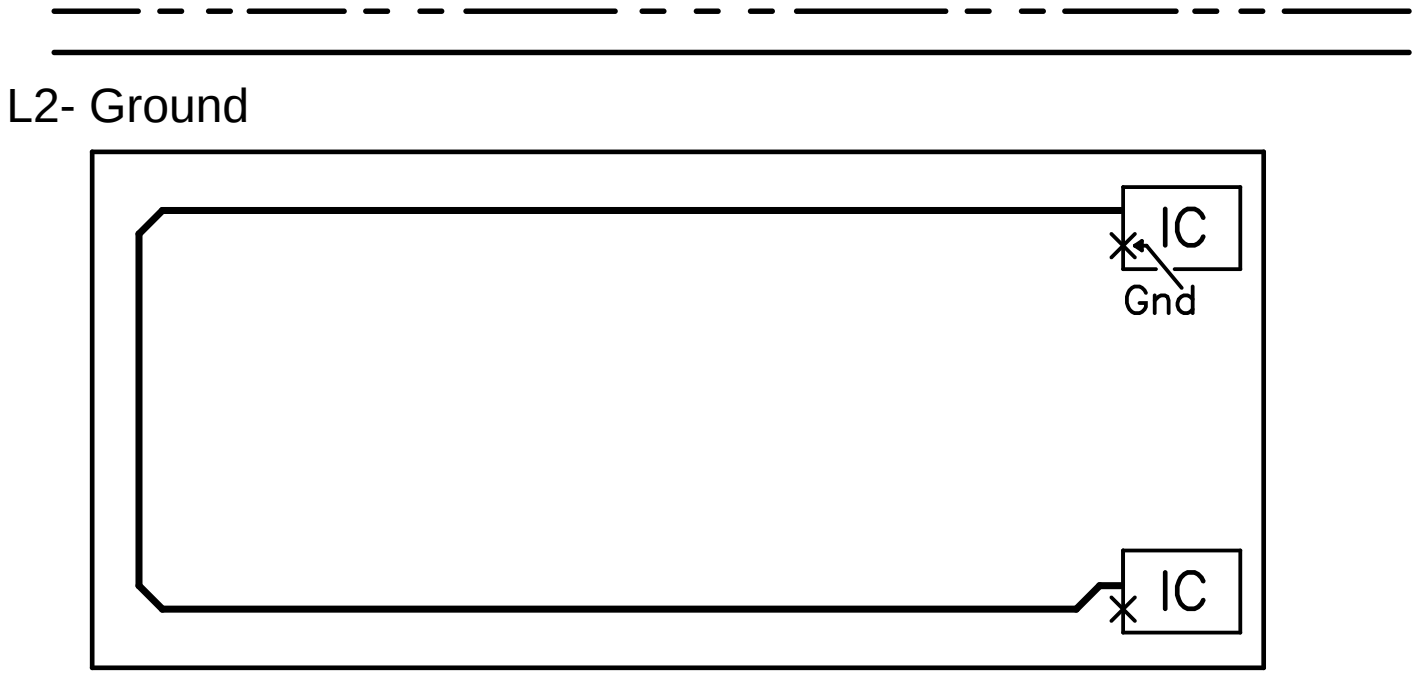
If you have to split a plane, do *not* route traces across the split!

- If you must, then you absolutely have to route a following ground trace across the split next to the signal trace

Splits in planes are very efficient slot antennas!

Signal Return Path

Two-layer Microwave Style PC Board



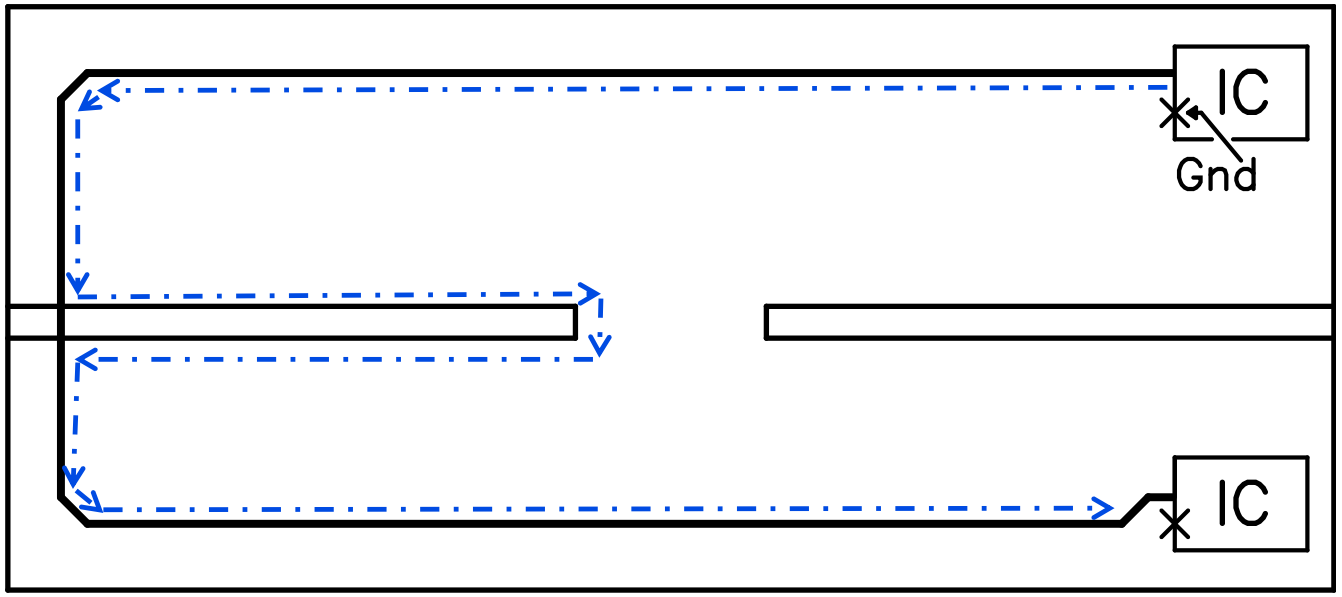
Where does signal's return current flow?

(Slide compliments of Rick Hartley, Consultant)

Signal Return Path

What happens if return plane is split?

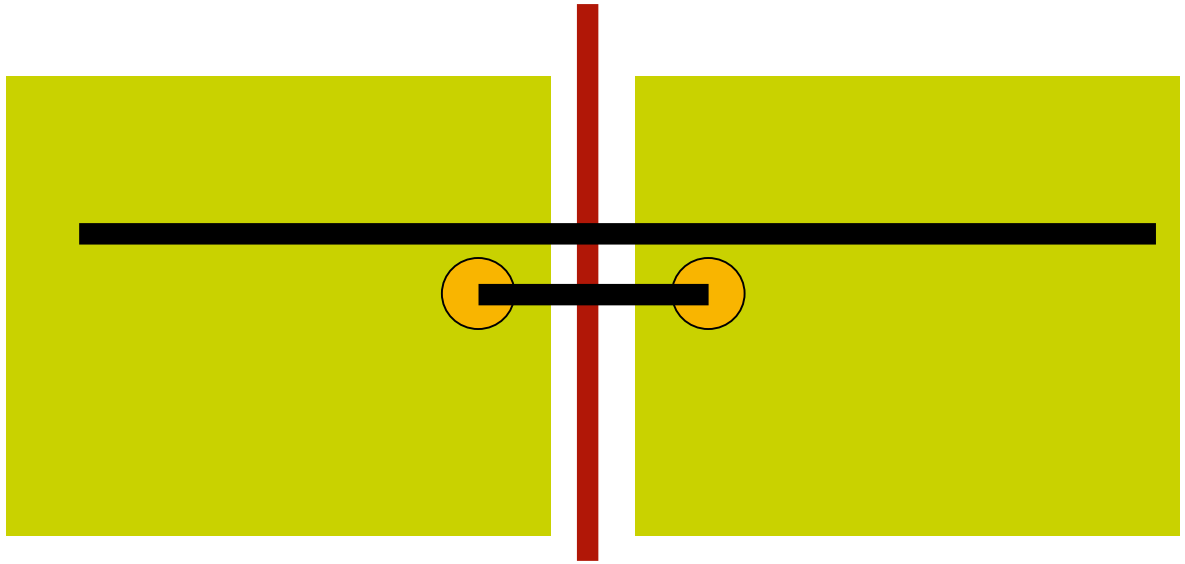
Now where does return current flow?



(Slide compliments of Rick Hartley, Consultant)

Splitting Ground Planes

- Routing over split planes, same potential
- Just use a bridge tied to each plane
- Better to just not split it, but sometimes you have to route a trace in the split



Routing Differential Signals

- Myth: They are coupled to each other

- Differential signals are referenced to each other only when twisted pair wiring is used, NOT on PCBs

- Fact: They are coupled to ground
- Each driver power source is coupled to ground, hence the outputs must be coupled to ground

- They do not have to be routed together
- They do need to be about the same length
- They do need to be treated as transmission lines
  - (You knew I was going to say that, didn't you?)
- They would benefit from being routed as a "triplet"
- Designed to reject common mode noise

- Not possible on PCBs, since there is no way to subject both signals to the same interference by twisting)

DESIGN TIPS

Design tips

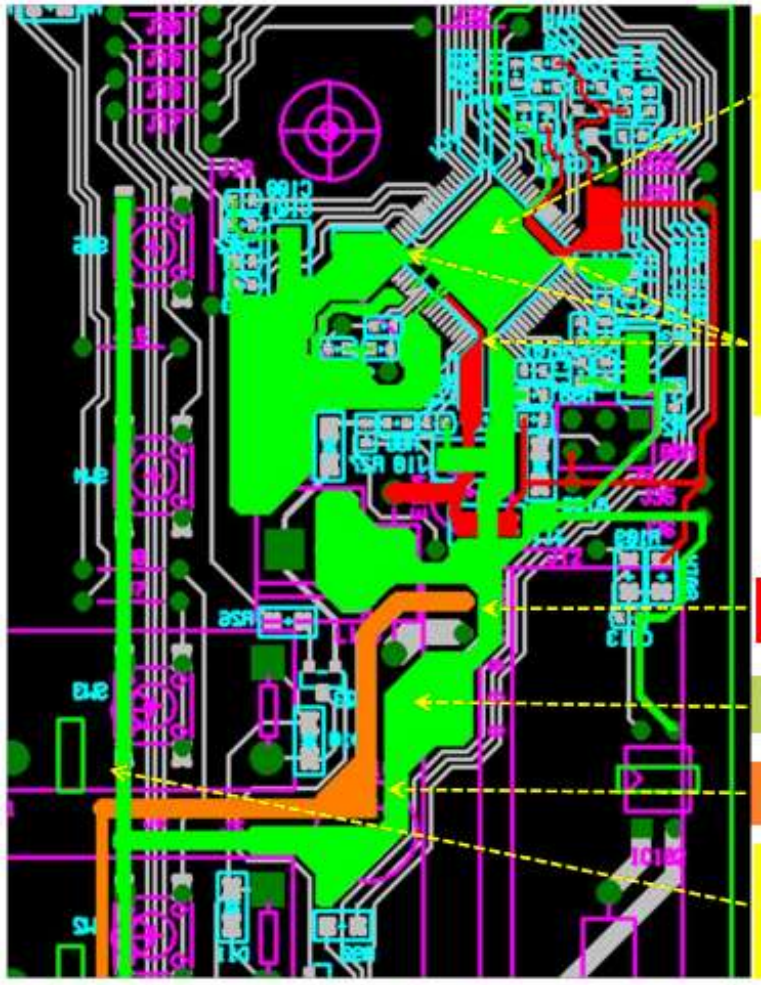
Compelling reasons for considering these design tips:

- Design requirements are more critical
  - Microcontrollers today are more powerful at the trade of operating at higher clocks.
  - Highly integrated companion chips are able to drive more loads in less board area
- Size and shape of the PCB are usually limited by the mechanical form factors
- PCB technology is usually defined in function of size and robustness requirements.
  - For cost consideration, a single-layer with double-side loading PCB is a good choice for most home appliance applications, but it is more challenging to design this kind of PCB with a high pin-count device
  - Multilayer PCB provides more flexibility on component placement, signal trace routing, power supply decoupling, and reference grounding. However are more expensive.
- No matter if single, dual or multilayer, signal integrity should be taken into consideration in any PCB layout.
  - The traces on the layout act as coupling paths, and the geometry factors of the traces (length, width, shape, and position) affect the coupling effectiveness significantly. .

The following subsections describe techniques recommended for a robust hardware design.

Design tips – General recommendations

- Power supply and ground routing



Fill up a ground plane underneath the MCU and connect all VSS pins together with the same potential level

Minimize the ground loops by use of the corner points for peripheral components around the MCU

5V GND

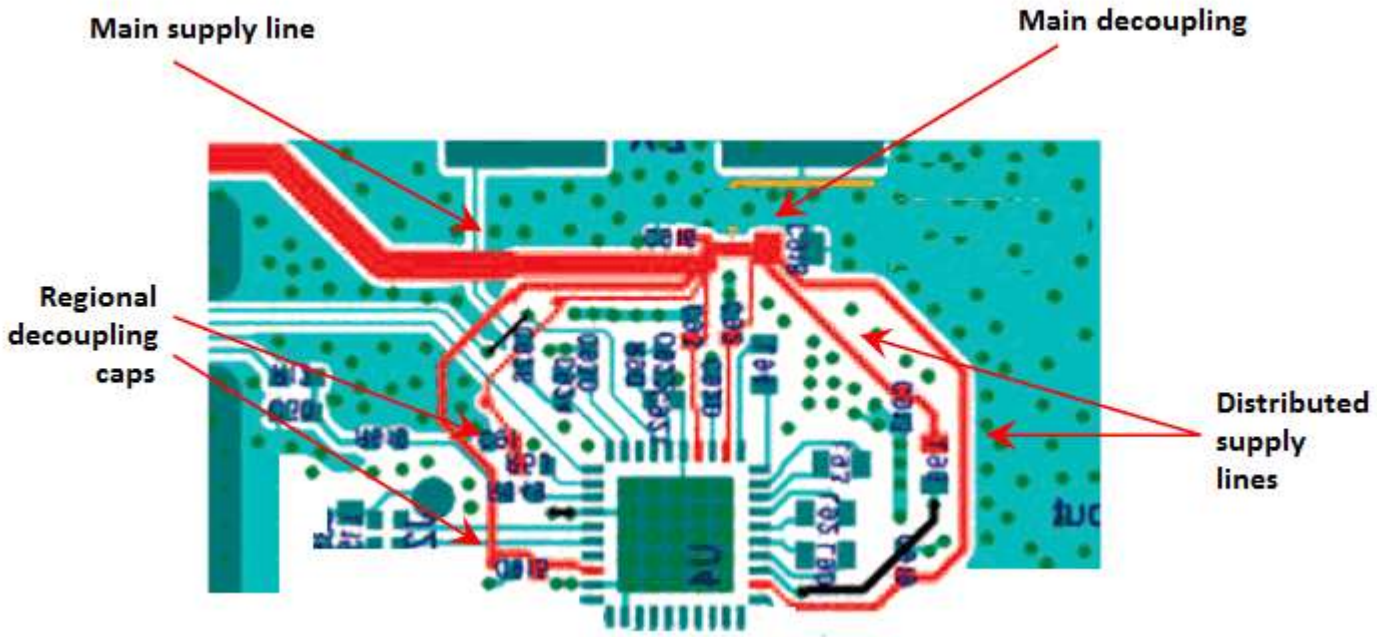
Power supply GND

12V GND

Avoid the ESD discharge energy injects into the 5V GND directly

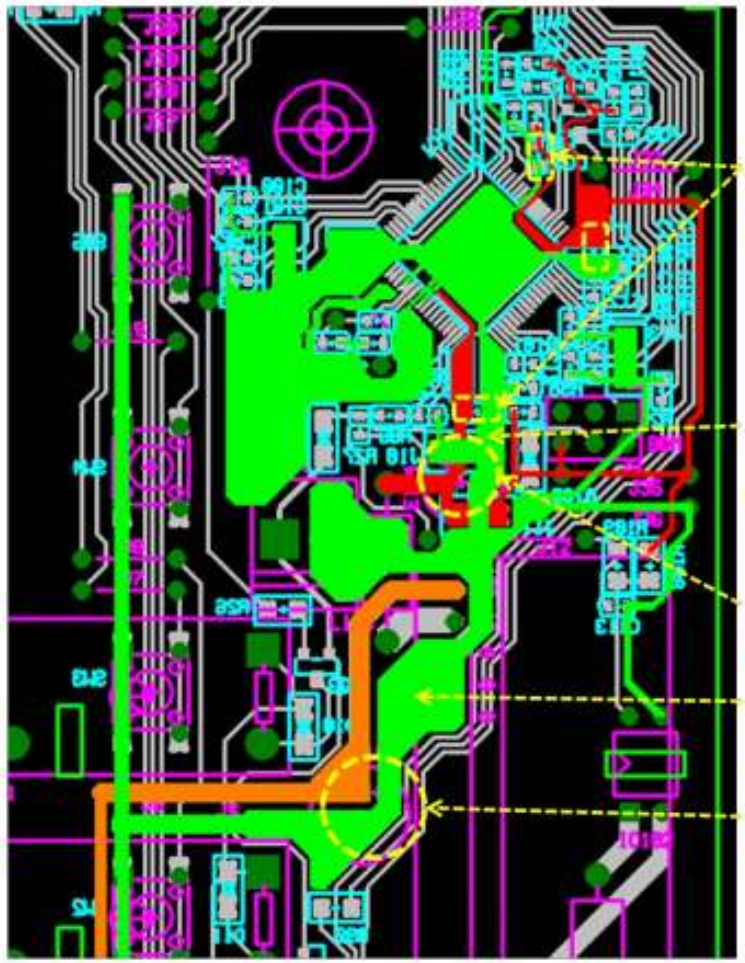
Design tips – General recommendations

- Power supply and ground routing
  - Distributed supply lines



Design tips – General recommendations

- Decoupling and bypassing



Place bypass capacitors as close as possible to the VDD and VSS pairs

Connect VDD and VSS traces to the decoupling capacitor first and then to the bypass capacitor before going to MCU's VDD and VSS pins

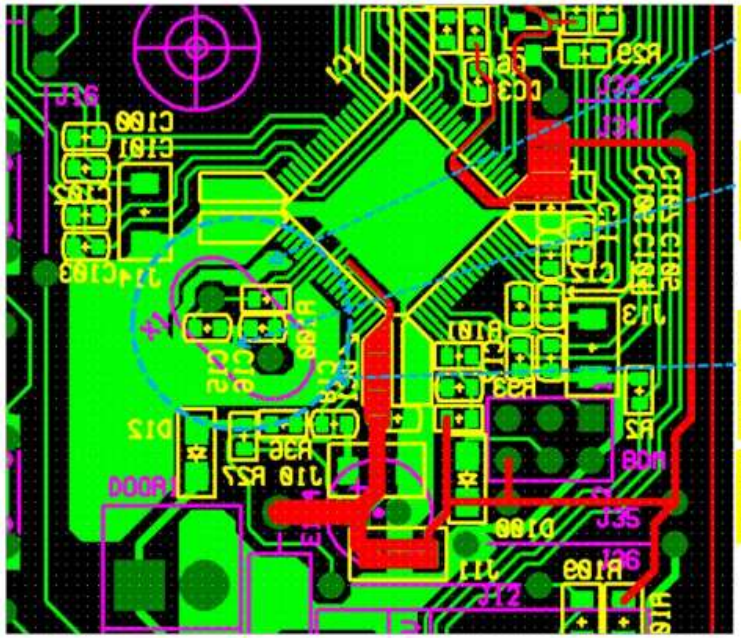
5V decoupling capacitor

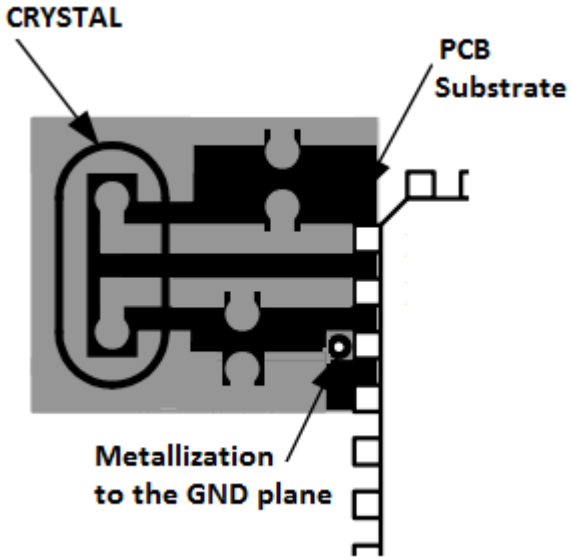
Power supply GND

12V decoupling capacitor

Design tips – General recommendations

- Crystal Oscillator Circuit

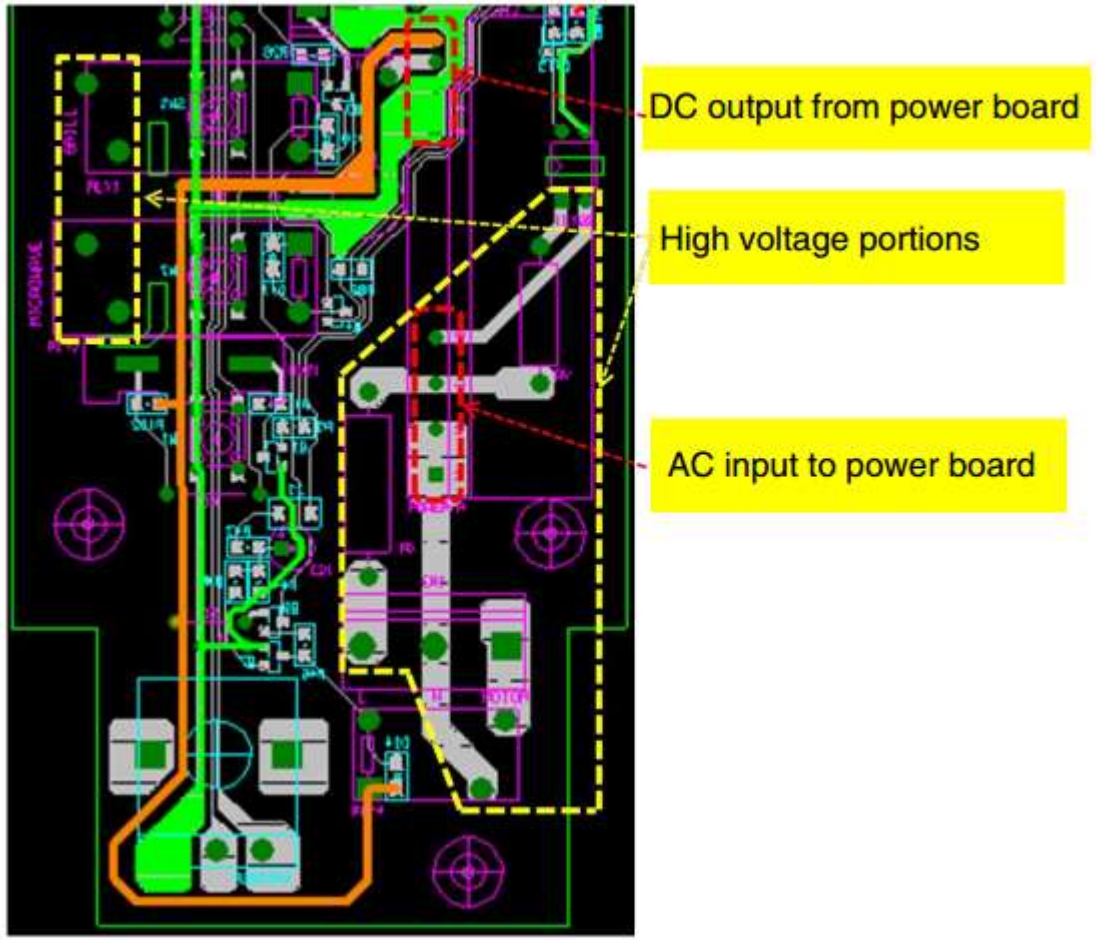




- In order to increase the robustness of high frequency/high impedance blocks against external disturbances, the design of the PCB layout has to be done very carefully.
  - Example: Crystal oscillators
- GND connection for the crystal and load capacitors must be short and avoid the return currents from Power and peripherals (USB, COM).
- Load capacitors must be low leakage and stable across temperature (NPO). Must be placed close to each other. Special care with the capacitor connected to Xin (observing that Xout is usually an low impedance path). Take special care with the parasitic capacitance between Xin and Xout

Design tips – General recommendations

- Spacing and Isolation



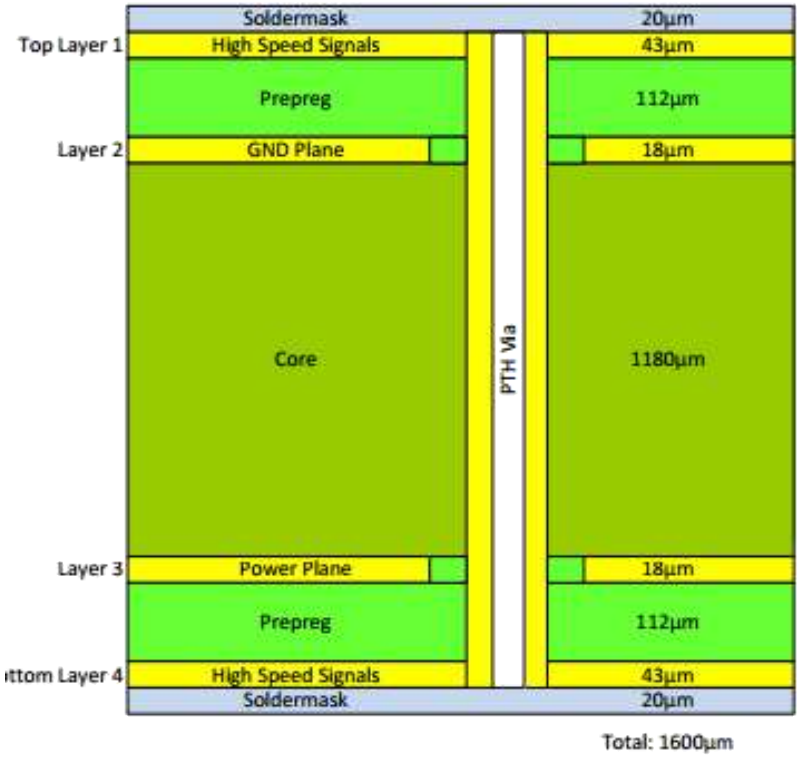
- The isolation for different circuit blocks is important when an AC high-power circuit is involved side by side to a low-power circuit on the same board as shown in this figure.
- In some cases, you may need to add a physical slot for better isolation if the board size is limited. Similarly, apply enough isolation space between the PCB trace and mounting screw holes or board edge for ESD consideration.

Design tips – General recommendations

- Software design
  - A good software design with EMC considerations improves overall system performance and operating stability in noisy environments.
  - In general, the software design cannot change the physical media which couples noise into the system, or reduce the absolute magnitude of noise generated from external sources. However, the software provides an intelligent method to select corrective actions in fault conditions and implement precautionary features for system protection.
  - These software techniques are recommended for a good defensive software design:
    - Enable WatchDog function to avoid code runaway.
    - Refresh data direction setting registers periodically.
    - Fill unused memory to avoid code runaway.
    - Define all interrupt vectors, even those that are not used.
    - Select Frequency-Locked Loop (FLL) engaged mode.
    - Always reconfirm edge triggered event.
    - Enable digital filter on input port.

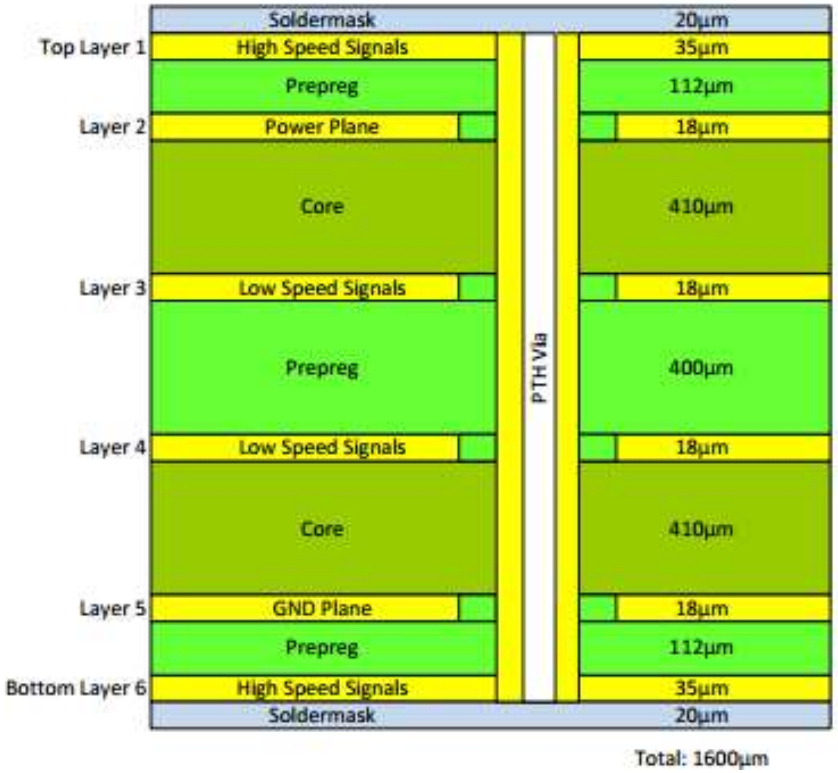
Design tips

- Multilayer stack-up.
- 4 layer usual implementation with external layers exposed.
  - High speed signals on the top layer are referenced to the ground plane on layer 2. Since the references for the high-speed signals on the bottom layer are the power planes on Layer 3, it is necessary to decouple power planes to ground.
  - It is recommended to route high speed signals on the top layer as opposed to the bottom layer so that the signals have a direct reference to the ground layer.
  - In some cases it may be desirable to have the bottom layer as primary high speed routing layer. In this case, the power and ground usage on Layer 2 and 3 could be swapped.



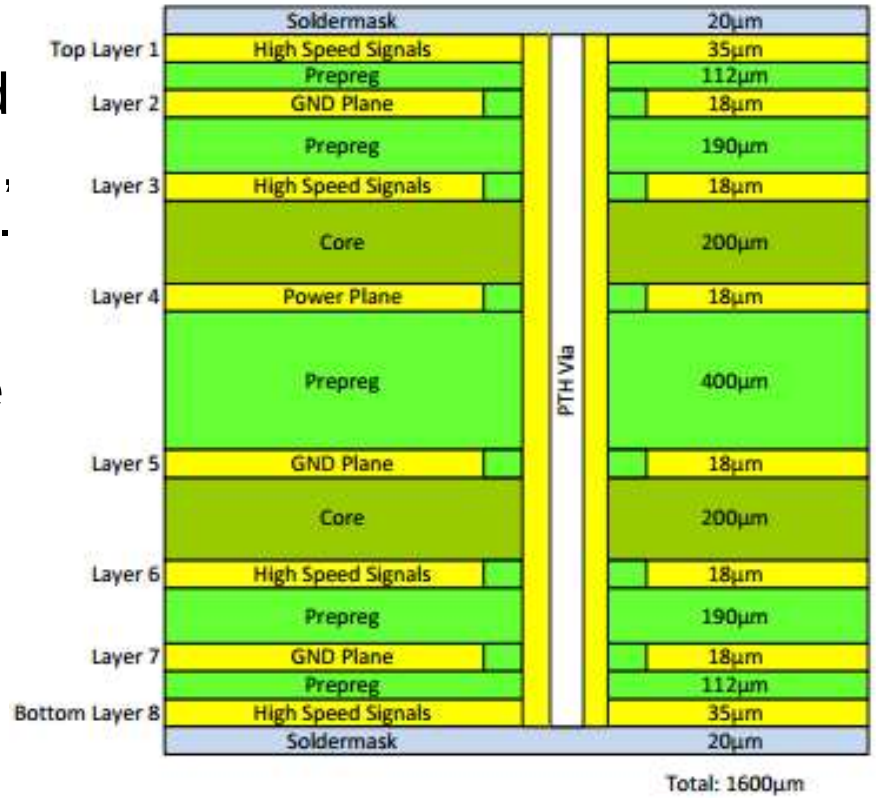
Design tips

- Multilayer stack-up.
- 6 layer usual implementation with external layers exposed.
  - Reference planes for the high-speed signals on the top layer are the power planes on layer 2.
  - Power and ground layers could be swapped if it is desirable to have the primary high-speed routing layer on the top layer.
  - Reference planes for signals on Layer 3 are located on Layer 2 and 5. The same reference planes are used by signals routed on Layer 4. As the reference planes are on layers which have a relatively large distance from Signal Layers 3 and 4 the traces would need to be very wide in order to achieve a common impedance of 50Ω. Therefore, these layers are not suitable for routing high-speed signals. In this stack-up approach, Layers 3 and 4 can only be used for routing low-speed signals where impedance matching is not required.



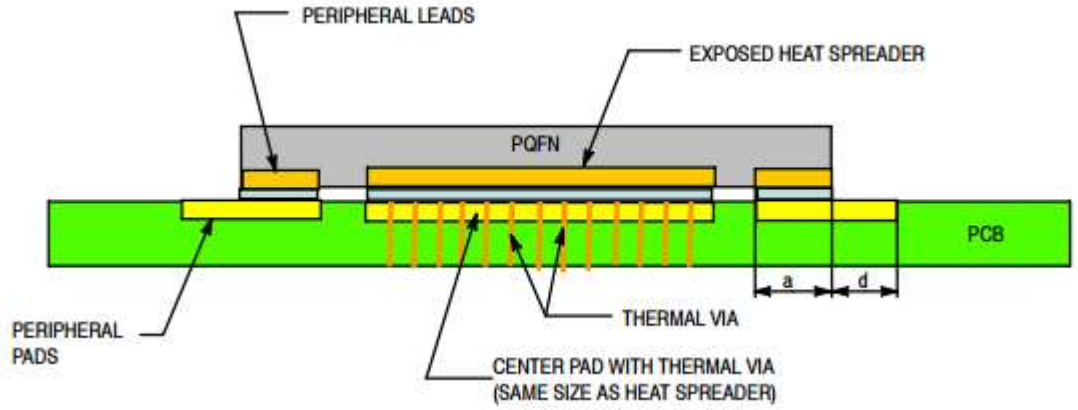
Design tips

- Multilayer stack-up.
- 8 layer usual implementation with external layers exposed
  - Signals on the top layer are referenced to the plane in Layer 2, while the signals on the bottom layer are referenced to layer 7. The reference planes for Signal Layer 3 are the ground plane on Layer 2 and the power planes on Layer 4.
  - Power planes on Layer 5 and 7 are used as references for the high-speed signals routed on Layer 6. The inner layer 6 with the two adjacent ground planes is the best choice for routing high-speed signals which have the most critical impedance control requirements. The inner layers cause less EMC problems as they are capsulated by the adjacent ground planes.
  - As Layer 3 is referenced to a power plane, outer layer 1 and 8 are preferable for high-speed routing if Layer 6 is already occupied.



Design tips

- Temperature
- Small packages such as Quad Flat (PQFN/QFN) are cost effective, great for board area savings and offer great performance for high frequency (RF). High frequency applications typically generate heat that must be conducted away from the device.
  - The heat source is on the die and to dissipate this heat through the PCB, the exposed heat spreader is attached to a center pad with via holes.



Design tips - Conclusion

- The guidelines illustrated in this presentation are intended to help customers apply robustness considerations in the early design phase using NXP Microcontrollers and Microprocessors in general.
  - Detailed descriptions on hardware and software techniques are listed as a quick reference for customer to adapt a NXP solution more effectively.

- Looking for additional information? See the additional references provided at the end of this presentation.

CLOSING REMARKS AND REFERENCE MATERIALS

PCB DESIGN IS NOT A BLACK ART!

Fundamentals to Remember

- Electromagnetic fields travel in the space between the conductors, not in the conductors
- The switching speed of the transistors determines the frequency of operation, not the clock rate
- Signal and power connections need to be one dielectric from ground for their entire length (including layer transitions)
  - Adjacent plane
  - Co-planar trace
- In a 4-layer design, if one layer is a ground plane, the two adjacent layers are one dielectric from ground.
- The 4th layer must be routed as if it were a single layer board.
- **There is no such thing as a noisy ground, just poor transmission line design**
- To quote Dr. Todd Hubing, “Thou shalt not split ground.”
- Any compromises to these rules will increase system noise and must be done as carefully considered engineering decisions.

High Speed Design Reading List

- *Right the First Time: A Practical Handbook on High Speed PCB and System Design* Volumes I & II, Lee W. Ritchey. Speeding Edge, ISBN 0-9741936-0-7
- *High Speed Digital System Design: A Handbook of Interconnect Theory and Practice*, Hall, Hall and McCall. Wiley Interscience 2000, ISBN 0-36090-2
- *High Speed Digital Design: A Handbook of Black Magic*, Howard W. Johnson & Martin Graham. Prentice Hall, ISBN 0-13-395724-1
- *High Speed Signal Propagation: Advanced Black Magic*, Howard W. Johnson & Martin Graham. Prentice Hall, ISBN 0-13-084408-X
- *Signal Integrity Simplified*, Eric Bogatin. Prentice Hall, ISBN 0-13-066946-6
- *Signal Integrity Issues and Printed Circuit Design*, Doug Brooks. Prentice Hall, ISBN 0-13-141884-X
- *Toradex Layout Guide* - http://docs.toradex.com/102492-layout-design-guide.pdf

(Slide compliments of Rick Hartley, Consultant)

EMI Reading List

- PCB Design for Real-World EMI Control, Bruce R. Archambeault. Kluwer Academic Publishers Group, ISBN 1-4020-7130-2
- Digital Design for Interference Specifications: A Practical Handbook for EMI Suppression, David L. Terrell & R. Kenneth Keenan. Newnes Publishing, ISBN 0-7506-7282-X
- Noise Reduction Techniques in Electronic Systems, 2nd Edition, Henry Ott. John Wiley and Sons, ISBN 0-471-85068-3
- Introduction to Electromagnetic Compatibility, Clayton R. Paul. John Wiley and Sons, ISBN 0-471-54927-4
- EMC for Product Engineers, Tim Williams. Newnes Publishing. ISBN 0-7506-2466-3
- Grounding & Shielding Techniques, 5th Edition, Ralph Morrison. John Wiley & Sons, ISBN 0-471-24518-6
- EMC Design Tips for Kinetis E Family - http://cache.nxp.com/files/microcontrollers/doc/app_note/AN4779.pdf

(Slide compliments of Rick Hartley, Consultant)

Additional References

- Ralph Morrison's New Book: Digital Circuit Boards: Mach 1 GHz. Available from Wiley and Amazon
- The Best PCB design conference website: http://pcbwest.com/
- Doug Smith's website: http://www.emcesd.com/ (He is the best at finding what is wrong! Lots of useful app notes.)
- IEEE EMC Society website: http://www.emcs.org/
- Clemson's Automotive Electronics website: http://www.cvel.clemson.edu/auto
- Clemson's EMC website: http://www.cvel.clemson.edu/emc
- Missouri University of Science and Technology website: http://www.mst.edu/about/
- IPC — Association Connecting Electronics Industries website: http://www.ipc.org/default.aspx

Summary and Q&A

- Well-defined transmission lines result in significantly improved EMC performance
- Careful routing of transmission lines can result in behavior similar to that gained by adding extra PCB ground layers
- Evaluating test results can lead you to solutions
- The *black magic* is tamed!
- Q&A

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