

# DEMYSTIFYING DESIGN WITH I.MX PROCESSORS: AN OVERVIEW OF THE AVAILABLE DOCUMENTATION AND TOOLS TO ENABLE YOUR MPU DESIGN

LAT-DES-T2441

BRUNO CASTELUCCI  
MPU/SECURITY FAE  
NOVEMBER 2016



PUBLIC



SECURE CONNECTIONS  
FOR A SMARTER WORLD

- **Introduction**

- Evaluation
- Boards
- Binaries
- Product

- **Hardware**

- Reference Boards Files
- Power Consumption
- Data Sheet
- IOMUX
- Hardware Dev Guide
- DDR Programming Aid
- DDR Stress Test
- MFGTools
- PMICs

- **Secure boot**

- Code Signing Tool
- High Assurance Boot
- Security RM

- **Software**

- Reference BSP Source
- BSP Document Bundle
- Linux RM
- BSP Release Notes
- BSP User Guide
- Yocto UG
- Multimedia UG
- Chip Errata
- Device Reference Manual
- Application Notes

- Other Security SW

- **Support**

- Community
- Official Online Support

- **Partners**

- SoM Partners
- Software Partners
- Training Partners



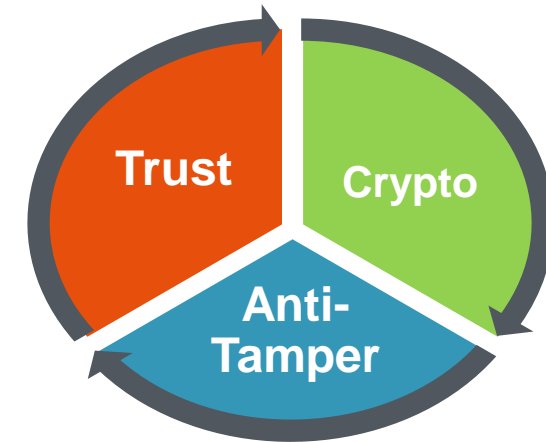
# INTRODUCTION



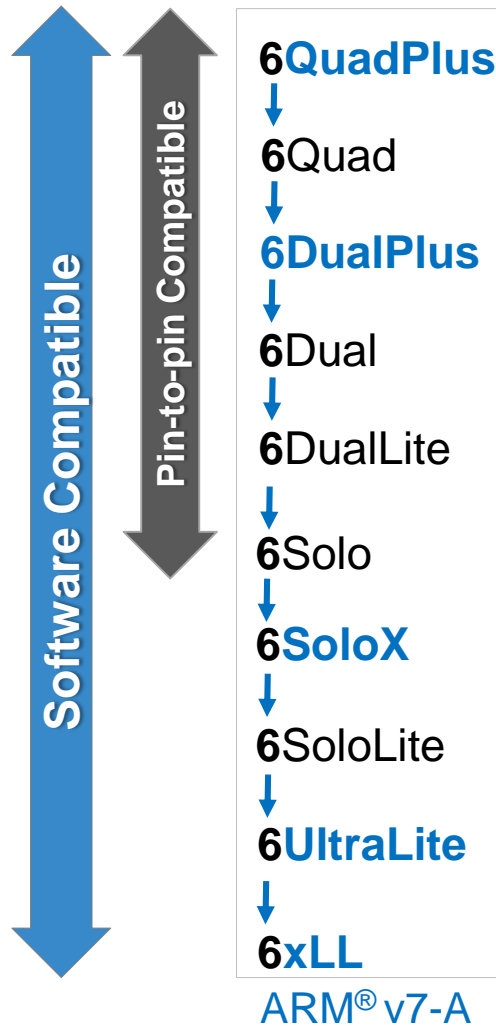
# i.MX Applications Processor Values

- **Scalability**
  - CPU (single/dual/quad, asymmetric), GPU, IO
  - Software: Linux, Android, Windows-embedded, RTOS
  - Pin compatibility and software portability
- **Trust**
  - Longevity: minimum of 10-15 years in all markets
  - Quality, robustness, zero-defect methodology
  - Security and Safety
  - Qualifications: AEC-Q100, JEDEC Industrial and Consumer
- **Ease of Use**
  - Industry-leading ecosystem, partnerships and support
  - Design collateral, distribution, communities
  - System solutions: SoC, sensors, memory, PMIC, connectivity

## Product **Longevity**



# i.MX 8 Series: 3 families of parts with targeted features



## i.MX 8 family

Advanced Graphics and Performance

ARM® v8-A  
(32-bit/ 64-bit)

## i.MX 8M family

Advanced Audio and Video

ARM® v8-A  
(32-bit/ 64-bit)

## i.MX 8X family

Safety Critical & Efficient Performance

ARM® v8-A  
(32-bit/ 64-bit)

## i.MX 7

Power Efficiency & BOM Cost Optimizations

ARM® v7-A  
(32-bit)



# EVALUATION

# Enablement through Reference Designs

## SABRE Platform for Smart Devices

- Builds on SABRE Board design with additional features including 10.1" capacitive multi-touch display, 2x MIPI camera sensors, SPI Nor Flash, GPS, ambient light sensor and digital microphones

Supported	Description
i.MX 6Quad i.MX 6Dual (emulated)	Quad-core 1-1.2 GHz ARM Cortex-A9 Dual-core 1-1.2 GHz ARM Cortex-A9
i.MX 6DualLite i.MX 6Solo (emulated)	Dual-core 1GHz ARM Cortex-A9 Single-core 1GHz ARM Cortex-A9

## SABRE for Auto Infotainment

- Support for terrestrial and satellite radio tuners, Wi-Fi, Bluetooth, GPS, cellular modem, iAP authentication modules, MOST vehicle networking, cameras and displays

Supported	Description
i.MX 6Quad i.MX 6Dual (emulated)	Quad-core 800MHz-1GHz ARM Cortex-A9 Dual-core 800MHz-1GHz ARM Cortex-A9
i.MX 6DualLite i.MX 6Solo (emulated)	Dual-core 800MHz ARM Cortex-A9 Single-core 800MHz ARM Cortex-A9
i.MX 6SoloX (Q3'15)	800MHz ARM Cortex-A9 200MHz ARM Cortex-M4

## SABRE Board for Smart Devices

- Multiple connectivity options: Wi-Fi®, Bluetooth®, GPS, Ethernet, SD, parallel/serial interfaces, SATA (i.MX 6Quad only), and PCIe

Supported	Description
i.MX 6Quad i.MX 6Dual (emulated)	Quad-core 1-1.2 GHz ARM Cortex-A9 Dual-core 1-1.2 GHz ARM Cortex-A9
i.MX 6SoloX	1GHz ARM Cortex-A9 200MHz ARM Cortex-M4

## i.MX 6SoloLite Evaluation Kit

- Enables EPD and/or LCD or HDMI display, touch control and audio playback, and the ability to add WLAN, a 3G modem or Bluetooth technology
- E-Ink display available separately

Supported	Description
i.MX 6SoloLite	Single-core 1GHz ARM Cortex-A9

# IMX6\_SW: i.MX 6 Series Software and Development Tool Resources

[Link](#)

**Overview**

Building your designs and getting to market quickly is easier with five market-focused development tools based on the i.MX 6 series processor—the Smart Application Blueprint for Rapid Engineering (SABRE) platform for smart devices, SABRE board for smart devices (i.MX 6QuadPlus, i.MX 6Quad, i.MX 6SoloX), SABRE for automotive infotainment, the i.MX 6SoloLite Evaluation Kit and the i.MX 6UltraLite Evaluation Kit.

Complete with reference software, an optimized OS and a system-validated board support package (BSP), NXP® provides you with the tools to test and maximize the performance of the applications you develop.

**Application Notes**

**i.MX 6 BSP Updates and Releases**

- Android
  - Android 6.0.1 Marshmallow (M6.0.1\_2.1.0, 4.1 kernel) [Current Release]
    - Supports i.MX 6QuadPlus, i.MX 6Quad, i.MX 6DualPlus, i.MX 6Dual, i.MX 6DualLite, i.MX 6Solo, i.MX 6SoloX, i.MX 6SoloLite
    - Source Code
    - Demo Images - SABRE for Automotive Infotainment based on i.MX 6QuadPlus, i.MX 6Quad and i.MX 6DualLite
    - Demo Images - SABRE Platform and SABRE Board based on i.MX 6QuadPlus, i.MX 6Quad and i.MX 6DualLite
    - Demo Images - i.MX 6SoloLite Evaluation Kit
    - Demo Images - SABRE Board based on i.MX 6SoloX
    - Demo Images - SABRE for Automotive Infotainment based i.MX 6SoloX

**Documentation**

- Android
  - Android M6.0.1\_2.1.0 BSP Documentation
  - Android 4.4.3 Patch Documentation
  - Android L5.0.0\_1.0.1 Patch Documentation
- Archived
- Linux
  - Linux 4.1.15\_2.0.0 BSP & Multimedia Codecs Documentation
  - Linux 4.1.15\_1.2.0 BSP & Multimedia Codecs Documentation
  - Linux 4.1.15\_1.1.0 BSP & Multimedia Codecs Documentation
  - Linux 4.1.15\_1.0.0 BSP & Multimedia Codecs Documentation
  - Linux 3.14.52 BSP & Multimedia Codecs Documentation
  - Linux L3.14.38 6ul Documentation

- Binaries
- Source
- Software Docs
- Tools
- Board page links
- Device page links





# Board web page – [link](#) (iMX6ULEVK)

MCIMX6UL-EVK: i.MX6UltraLite Evaluation Kit ☆

Overview Documentation Downloads Buy / Specifications Training & Support

**Jump To**


- Overview
- Features
- Supported Devices
- Kit Contains
- Jump Start Your Design
- Related Products
- Community Discussions

**Overview**

NXP® delivers a highly flexible, market-focused development tools with an evaluation kit (EVK) based on the i.MX 6UltraLite applications processor. The i.MX 6UltraLite processor is the first device in the i.MX product line to have a single ARM® Cortex®-A7 core operating at speeds of up to 696 MHz. This EVK enables an LCD display and audio playback as well as many connectivity options. It is designed to showcase the most commonly used features of the processor in a small, low cost package and to facilitate software development with the ultimate goal of faster time to market through the support of the Linux® operating system.

[Buy](#)

**i.MX 6UltraLite Evaluation Kit**



The image shows a green printed circuit board (PCB) for the i.MX 6UltraLite Evaluation Kit. It features a central processor, various connectors, a USB port, and a small LCD display. The board is populated with numerous components, including capacitors, resistors, and integrated circuits. The board is shown from a top-down perspective, highlighting its compact size and the density of components.

- Description
- User Guide
- Design Files
  - Schematics
  - Layout
  - BOM
- Buy Direct



# Device Page – [link](#) (iMX6UL)

i.MX6UL: i.MX 6UltraLite Processor - Low-power, secure, ARM® Cortex®-A7 Core ☆

Overview Documentation Software & Tools Buy / Parametrics Package / Quality Training & Support

**Jump To**  
Overview  
Features  
Target Applications  
Related Products  
Community Discussions

### Overview

Expanding the i.MX 6 series, the i.MX 6UltraLite is a high performance, ultra-efficient processor family featuring an advanced implementation of a single ARM® Cortex®-A7 core, which operates at speeds up to 696 MHz. The i.MX 6UltraLite applications processor includes an integrated power management module that reduces the complexity of external power supply and simplifies power sequencing. Each processor in this family provides various memory interfaces, including 16-bit LPDDR2, DDR3, DDR3L, raw and managed NAND flash, NOR flash, eMMC, Quad SPI and a wide range of other interfaces for connecting peripherals such as WLAN, Bluetooth™, GPS, displays and camera sensors.

[Data Sheet](#) [Application Notes](#) [Buy](#)

### i.MX 6UltraLite Applications Processor Block Diagram

The block diagram illustrates the architecture of the i.MX 6UltraLite Applications Processor, organized into several functional blocks:

- System Control:** Secure JTAG, PLL, OSC, RTC and Reset, Smart DMA, IOMUX, Timer x 4, PWM x 6, Watch Dog x 3.
- Power Management:** LDO, Temp Monitor.
- ADC:** ADC x 2 (10-ch.) w/ touch ctrl.
- Internal Memory:** 96 KB ROM, 128 KB ROM.
- External Memory:** Parallel NOR FLASH, Dual-Channel Quad SPI x 1, 16-bit LP-DDR2/DDR3/DDR3L.
- CPU Platform:** ARM® Cortex®-A7, 32 KB I-Cache, 32 KB D-Cache, NEON™, PTM, 128 KB L2-Cache.
- Multimedia:** CSC, Combine, Rotate, Programmable Proc. Engine, 24-bit Parallel CSI, 24-bit Parallel LCD.
- Connectivity:** eMMC 4.5 / SD 3.0 x 2, NAND Ctrl (BCH40), UART x 8, SIM V2/ EMV/SIM x 2, PC x 4, SPI x 4, GPIO, 8 x 8 Keypad, FS/SAI x 3, S/PDIF Tx/Rx, ASRC, FlexCAN x 2, 10/100 ENET x 2 with IEEE 1588, USB2 OTG w/ PHY x 2.
- Security:** Clones, OTF DRAM Encryption, RNG, 10 Tamper Pins, eFuse, RSA4096 DPA Protection, Secure RTC, 32 KB Secure Storage.

Optional

- Documents
  - DS
  - RM
  - SRM
  - Errata
- App Notes
- Samples
- Other



# HARDWARE DESIGN



# Board Reference Design Files - [link](#) (iMX6ULEVK)

## Schematics (1)



Design files, including hardware schematics, Gerbers, and OrCAD files.

(REV 0)

Design files, including hardware schematics, Gerbers, and OrCAD files..

ZIP (9.9 MB) MCIMX6UL-EVK\_DESIGNFILES

9/24/2015

Download

- MCIMX6UL-EVK\_DESIGNFILES
  - MCIMX6UL\_BB\_DESIGNFILES
    - BOM
    - Layout
      - GERBER Files
      - Schematics
  - MCIMX6UL\_CM\_DESIGNFILES
    - BOM
    - Layout
      - GERBER Files
      - Schematics

# Datasheet – Device Page – [link](#) (iMX6UL)

- ⊕ 1 i.MX 6UltraLite Introduction
- ⊕ 2 Architectural Overview
- ⊕ 3 Modules List
- ⊖ 4 Electrical Characteristics
  - ⊕ 4.1 Chip-Level Conditions
  - ⊕ 4.2 Power Supplies Requirements and Restrictions
  - ⊕ 4.3 Integrated LDO Voltage Regulator Parameters
  - ⊕ 4.4 PLL's Electrical Characteristics
  - ⊕ 4.5 On-Chip Oscillators
  - ⊕ 4.6 I/O DC Parameters
  - ⊕ 4.7 I/O AC Parameters
  - ⊕ 4.8 Output Buffer Impedance Parameters
  - ⊕ 4.9 System Modules Timing
  - ⊕ 4.10 General-Purpose Media Interface (GPMI) Timing
  - ⊕ 4.11 External Peripheral Interface Parameters
  - ⊕ 4.12 A/D Converter
- ⊕ 5 Boot Mode Configuration
- ⊕ 6 Package Information and Contact Assignments

- ⊖ 5 Boot Mode Configuration
  - ⊖ 5.1 Boot Mode Configuration Pins
  - ⊖ 5.2 Boot Device Interface Allocation
- ⊖ 6 Package Information and Contact Assignments
  - ⊖ 6.1 14x14 mm Package Information
    - ⊖ 6.1.1 14x14 mm, 0.8 mm Pitch, Ball Matrix
    - ⊖ 6.1.2 14x14 mm Supplies Contact Assignments and Functional Contact Assignments
    - ⊖ 6.1.3 14x14 mm, 0.8 mm Pitch, Ball Map
  - ⊖ 6.2 9x9 mm Package Information
    - ⊖ 6.2.1 9x9 mm, 0.5 mm Pitch, Ball Matrix
    - ⊖ 6.2.2 9x9 mm Supplies Contact Assignments and Functional Contact Assignments
    - ⊖ 6.2.3 9x9 mm, 0.5 mm Pitch, Ball Map
  - ⊖ 6.3 GPIO Reset Behaviors during Reset

# IOMUX – Tools Page – [link](#) (iMX6)

The screenshot shows the iMX6 Pin Manager interface. On the left, a table lists pins and their configurations:

Pin	Pin name	Label	Identifier	GPIO
A1	VSS0			
B1	SD1_DATA2	SD1_DATA2/..		gpio2_IC
C1	SD1_CLK	SD1_CLK/P8..		gpio2_IC
D1	CSI_DATA07	CSI_DATA7/..		gpio4_IC
E1	CSI_DATA03	CSI_DATA3/..		gpio4_IC
F1	DRAM_ODT1	DRAM_ODT1		
G1	DRAM_ADD..	DRAM_ADD..		
H1	DRAM_SDBA1	DRAM_SDBA1		
J1	DRAM_SDW..	DRAM_SDW..		
K1	DRAM_ADD..	DRAM_ADD..		
L1	DRAM_ADD..	DRAM_ADD..		
M1	DRAM_SDBA0	DRAM_SDBA0		
N1	DRAM_ODT0	DRAM_ODT0		
P1	DRAM_SDCL..	DRAM_SDCL..		
R1	DRAM_DAT..	DRAM_DAT..		
T1	DRAM_SDQS..	DRAM_SDQS..		
U1	VSS1			
A2	SD1_DATA3	SD1_DATA3/..		gpio2_IC
B2	SD1_DATA1	SD1_DATA1/..		gpio2_IC
C2	SD1_CMD	SD1_CMD/P..		gpio2_IC
D2	CSI_DATA06	CSI_DATA6/..		gpio4_IC
E2	CSI_DATA02	CSI_DATA2/..		gpio4_IC
F2	CSI_VSYNC	CSI_VSYNC		gpio4_IC
G2	DRAM_ADD..	DRAM_ADD..		
H2	DRAM_ADD..	DRAM_ADD..		
J2	DRAM_CAS_B	DRAM_CAS_B		
K2	DRAM_SDBA2	DRAM_SDBA2		
L2	DRAM_ADD..	DRAM_ADD..		
M2	DRAM_ADD..	DRAM_ADD..		
N2	DRAM_CS0_B	DRAM_CS0_B		
P2	DRAM_SDCL..	DRAM_SDCL..		
R2	DRAM_DAT..	DRAM_DAT..		
T2	DRAM_SDQS..	DRAM_SDQS..		
U2	DRAM_DAT..	DRAM_DATA8		

The central grid shows the physical pin layout for the MCMX6G3CVM05AA - MAPEGA 289 package. The bottom window shows the 'Routed Pins' table:

#	Peripheral	Signal	Route to	Label	Identifier	Power group
U9	CCM	ccm_pmic_stby_req	CCM_PMIC_STBY_REQ	PMIC_STBY_REQ/P801A[3]	n/a	VDD_SNVS_IN (0V)

```

imx6ul-board.dtsi | iomux_config.c | iomux_config.h

#include "skeleton.dtsi"
#include "imx6ul-pinfunc.h"

/ {
    model = "Freescale i.MX 6UltraLite User Board";
    compatible = "fsl,imx6ul-board", "fsl,imx6ul";

    soc {
        #address-cells = <1>;
        #size-cells = <1>;

        iomuxc: iomuxc@020e0000 {
            compatible = "fsl,imx6ul-iomuxc";
            reg = <0x020e0000 0x4000>;
        };
    };

    &iomuxc {
        pinctrl-names = "default";
        pinctrl-0 = <&init_ccm_pins>;

        imx6ul-board {

            init_ccm_pins: init_ccm_pinsgrp {
                /*
                 * TEXT BELOW IS USED AS SETTING FOR THE PINS TOOL *****
                init_ccm_pins:
                - options: {coreID: singlecore}
                - pin_list:
                  - {pin_num: U9, peripheral: CCM, signal: ccm_pmic_stby_req, pin_signal: CCM_P
                  * BE CAREFUL MODIFYING THIS COMMENT - IT IS YAML SETTINGS FOR THE PINS TOOL **
                */
                fsl,pins = <
                    >;

            init_csi_pins: init_csi_pinsgrp {
                /*
                 * TEXT BELOW IS USED AS SETTING FOR THE PINS TOOL *****
                init_csi_pins:
                - options: {coreID: singlecore}

```

## i.MX 6UltraLite Power Consumption Measurement

### 1. Introduction

This application note helps to design power management systems. Through several use cases this application note illustrates the current drain measurements of the i.MX 6UltraLite Applications Processors taken on the MX6UL EVK Evaluate Kit Platform. You will be enabled to choose the appropriate power supply domains for the i.MX 6UltraLite chips and become familiar with the expected chip power in various scenarios.

Because the data presented in this application note is based on empirical measurements taken on a small sample size, the presented results are not guaranteed.

### Contents

1.	Introduction.....	1
2.	Overview of i.MX 6UltraLite Voltage Supplies .....	2
3.	Internal Power Measurement of the i.MX 6UltraLite Processor .....	3
3.1.	VDD_HIGH_CAP power .....	3
3.2.	DDR I/O power.....	4
3.3.	Voltage levels and DVFS usage in measurement process .....	5
3.4.	Temperature measurements .....	6
3.5.	Hardware and tool used .....	6
3.6.	Board setup used for power measurements .....	6
3.7.	Measuring points on the MX6UL EVK platform .....	6
4.	Use Cases and Measurement Results .....	7
4.1.	Low-power mode use cases .....	7
4.2.	Dhrystone benchmark .....	9
4.3.	Heavy loading use case: 480P video playback.....	10
4.4.	SNVS .....	11
5.	Reducing Power Consumption .....	12
5.1.	Steps to be performed before entering Suspend (Deep-Sleep mode): .....	13
5.2.	Steps to be performed after exiting Suspend: .....	14
6.	Use Case Configuration and Usage Guidelines .....	14
6.1.	Deep-Sleep mode .....	14
6.2.	System Idle mode.....	15

# Hardware Development Guide for the i.MX 6UltraLite Applications Processor

Hardware Development Guide for the i.MX 6UltraLite Applications Processor (REV 1)

 PDF (1.2 MB) IMX6ULHDG [English]

## 1 About This Book

### 1.1 Overview

This document's purpose is to help hardware engineers design and test their i.MX 6UltraLite processor-based designs. It provides information on board layout recommendations, and design checklists to ensure first-pass success and avoidance of board bring-up problems. It also provides information on board-level testing and simulation such as using BSDL for board-level testing, using the IBIS model for electrical integrity simulation and more.

#### Contents

1. About This Book	1
2. i.MX 6UL Design Checklist	6
3. i.MX 6 Series Layout Recommendations	16
4. Avoiding Board Bring-up Problems	32
5. Understanding the IBIS Model	36
6. Using the Manufacturing Tool	46
7. Using BSDL for Board-level Testing	51
8. Revision History	53
A. Development Platforms	54



# Slide 2 - Hardware Design Guide - Device Page – [link](#) (iMX6UL)

- 2 i.MX 6UltraLite design checklist
  - 2.1 Design checklist tables
    - Table 4. DDR recommendations
    - Table 5. LCD recommendations for developer's boot modes
    - Table 6. Boot mode input recommendations
    - Table 7. I2C recommendations
    - Table 8. JTAG recommendations
    - Table 9. Power supply decoupling recommendations
    - Table 10. Power and decoupling recommendations
    - Table 11. Oscillator and clock recommendations
    - Table 12. Reset and ON OFF recommendations
    - Table 13. USB recommendations
    - Table 14. Miscellaneous recommendations
  - 2.2 DDR reference circuit
  - 2.3 JTAG signal termination
  - 2.4 Oscillator tolerance
  - 2.5 Unused analog interfaces
  - 2.6 Migrating from i.MX 6UltraLite TO1.0 to TO1.1

- 3 i.MX 6UltraLite Layout Recommendations
  - 3.1 Introduction
  - 3.2 Basic design recommendations
  - 3.3 Stackup recommendations
  - 3.4 DDR connection information
  - 3.5 Routing considerations
  - 3.6 DDR power recommendations
  - 3.7 USB recommendations
  - 3.8 Impedance signal recommendations
  - 3.9 ESD and radiated emissions recommendations
  - 3.10 Component placement recommendations
  - 3.11 Reducing skew and phase problems in differential pairs traces

- 4 Avoiding Board Bring-up Problems
  - 4.1 Introduction
  - 4.2 Using a current monitor to avoid power pitfalls
  - 4.3 Using a voltage report to avoid power pitfalls
  - 4.4 Checking for clock pitfalls
  - 4.5 Avoiding reset pitfalls
- 5 Understanding the IBIS Model
- 6 Using the Manufacturing Tool
- 7 Using BSDL for Board-level Testing

# Board Bring-Up and Debug Checklist

Checklist Item
The following items need to be completed serially
Visual Inspection
Verify all SoC voltage rails
Verify power up sequence
Measure/probe input clocks (32kHz, 24MHz, others)
JTAG connectivity (DS-5, RV-ICE, Lauterbach, Macraigor, etc)
Access internal RAM
<b>Run basic DDR initialization and test memory</b>
<b>Run DDR Stress test</b>
The following items may be worked on in parallel with other bring up tasks
Verify CLK0 outputs (measure and verify default clock frequencies for desired clock output options); this assumes that the board design supports probing of the CLK0 pin.
Measure boot mode frequencies (set the boot mode switch for each boot mode and measure the following, depending on what is available in the system): - NAND (probe CE to verify boot, measure RE frequency) - SPI-NOR (probe slave select and measure clock freq) - MMC/SD (measure clock freq)
Run other unit tests



# Recommended Flow and Tools for Optimal DDR Initialization

**Create initial DDR initialization script**

- Use the **DDR Register Programming Aid**
- Input values from Memory vendor datasheet

**Perform calibration to optimize script**

- Use the **DDR Stress Test : Calibration Routine**
- Generates optimal calibration values

**Validate DDR interface with optimized script**

- Use **DDR Stress Test : Memory Sub routines**
- Using updated calibration values

More details? Look for **FTF-DES-N1936** FTF Americas Presentation on the community.

# DDR Programming Aid – community – [link](#) (iMX6)

i.MX6UL

- [i.MX6UL DDR3 DRAM Register Programming Aid](#)
- [i.MX6UL LPDDR2 DRAM Register Programming Aid](#)

How to use the DRAM register programming aid outline

Step 1. Obtain the desired DRAM data sheet from the DRAM vendor

The following are to be completed in the Register Configuration Worksheet tab.

How To Use **Register Configuration** DStream .ds file

Step 2. Update the Device Information table to include the DRAM information and system usage

Device Information	
Memory type:	DDR3
Manufacturer:	Micron
Memory part number:	MT41J128M16HA-15E
Density of each DDR3 device (Gb):	2
Number of DRAM devices per chip select	4
Density per chip select (Gb) <sup>1</sup> :	8
Number of Chip Selects used <sup>2</sup> :	2
Number of ROW Addresses <sup>2</sup> :	14
Number of COLUMN Addresses <sup>2</sup> :	10
Number of BANKS <sup>2</sup> :	8
Bus Width (input 16, 32, or 64 bits) <sup>2</sup> :	64
Clock Cycle Freq (MHz) <sup>3</sup> :	533
Clock Cycle Time (ns):	1.876

Step 3. Go through the various shaded cells in the spread sheet to update with data from the DRAM sheet (t

### i.MX6UL MMDC DDR3 Configuration Spreadsheet Based on EVK board

**Introduction**

This spreadsheet is used to configure the MMDC registers for DDR3 memory. It is based on the EVK board. The spreadsheet is divided into several tabs: Introduction, Legend, Device Information, Memory Bank, and Register Configuration. The Register Configuration tab is the main configuration area and contains a large table of registers. The other tabs provide additional information and guidance.

**Legend**

Yellow	Default Value
Green	Value to be updated
Orange	Value to be updated (Warning)

**Device Information**

Field	Value
Memory type	DDR3
Manufacturer	Micron
Memory part number	MT41J128M16HA-15E
Density of each DDR3 device (Gb)	2
Number of DRAM devices per chip select	4
Density per chip select (Gb) <sup>1</sup>	8
Number of Chip Selects used <sup>2</sup>	2
Number of ROW Addresses <sup>2</sup>	14
Number of COLUMN Addresses <sup>2</sup>	10
Number of BANKS <sup>2</sup>	8
Bus Width (input 16, 32, or 64 bits) <sup>2</sup>	64
Clock Cycle Freq (MHz) <sup>3</sup>	533
Clock Cycle Time (ns)	1.876

**Memory Bank**

Bank	Bank Select	Bank Size (Mb)	Bank Type
0	0	128	DDR3
1	1	128	DDR3
2	2	128	DDR3
3	3	128	DDR3

**Register Configuration**

Register	Value	Bank	Bank Select	Bank Size (Mb)	Bank Type
0x00000000	0x00000000	0	0	128	DDR3
0x00000004	0x00000004	0	0	128	DDR3
0x00000008	0x00000008	0	0	128	DDR3
0x0000000C	0x0000000C	0	0	128	DDR3
0x00000010	0x00000010	0	0	128	DDR3
0x00000014	0x00000014	0	0	128	DDR3
0x00000018	0x00000018	0	0	128	DDR3
0x0000001C	0x0000001C	0	0	128	DDR3
0x00000020	0x00000020	0	0	128	DDR3
0x00000024	0x00000024	0	0	128	DDR3
0x00000028	0x00000028	0	0	128	DDR3
0x0000002C	0x0000002C	0	0	128	DDR3
0x00000030	0x00000030	0	0	128	DDR3
0x00000034	0x00000034	0	0	128	DDR3
0x00000038	0x00000038	0	0	128	DDR3
0x0000003C	0x0000003C	0	0	128	DDR3
0x00000040	0x00000040	0	0	128	DDR3
0x00000044	0x00000044	0	0	128	DDR3
0x00000048	0x00000048	0	0	128	DDR3
0x0000004C	0x0000004C	0	0	128	DDR3
0x00000050	0x00000050	0	0	128	DDR3
0x00000054	0x00000054	0	0	128	DDR3
0x00000058	0x00000058	0	0	128	DDR3
0x0000005C	0x0000005C	0	0	128	DDR3
0x00000060	0x00000060	0	0	128	DDR3
0x00000064	0x00000064	0	0	128	DDR3
0x00000068	0x00000068	0	0	128	DDR3
0x0000006C	0x0000006C	0	0	128	DDR3
0x00000070	0x00000070	0	0	128	DDR3
0x00000074	0x00000074	0	0	128	DDR3
0x00000078	0x00000078	0	0	128	DDR3
0x0000007C	0x0000007C	0	0	128	DDR3
0x00000080	0x00000080	0	0	128	DDR3
0x00000084	0x00000084	0	0	128	DDR3
0x00000088	0x00000088	0	0	128	DDR3
0x0000008C	0x0000008C	0	0	128	DDR3
0x00000090	0x00000090	0	0	128	DDR3
0x00000094	0x00000094	0	0	128	DDR3
0x00000098	0x00000098	0	0	128	DDR3
0x0000009C	0x0000009C	0	0	128	DDR3
0x000000A0	0x000000A0	0	0	128	DDR3
0x000000A4	0x000000A4	0	0	128	DDR3
0x000000A8	0x000000A8	0	0	128	DDR3
0x000000AC	0x000000AC	0	0	128	DDR3
0x000000B0	0x000000B0	0	0	128	DDR3
0x000000B4	0x000000B4	0	0	128	DDR3
0x000000B8	0x000000B8	0	0	128	DDR3
0x000000BC	0x000000BC	0	0	128	DDR3
0x000000C0	0x000000C0	0	0	128	DDR3
0x000000C4	0x000000C4	0	0	128	DDR3
0x000000C8	0x000000C8	0	0	128	DDR3
0x000000CC	0x000000CC	0	0	128	DDR3
0x000000D0	0x000000D0	0	0	128	DDR3
0x000000D4	0x000000D4	0	0	128	DDR3
0x000000D8	0x000000D8	0	0	128	DDR3
0x000000DC	0x000000DC	0	0	128	DDR3
0x000000E0	0x000000E0	0	0	128	DDR3
0x000000E4	0x000000E4	0	0	128	DDR3
0x000000E8	0x000000E8	0	0	128	DDR3
0x000000EC	0x000000EC	0	0	128	DDR3
0x000000F0	0x000000F0	0	0	128	DDR3
0x000000F4	0x000000F4	0	0	128	DDR3
0x000000F8	0x000000F8	0	0	128	DDR3
0x000000FC	0x000000FC	0	0	128	DDR3



# DDR Stress Test – community – [link](#) - (iMX6)

## Option 1 GUI based:

Run the GUI executable and connect your board to the host PC via USB

- Archive file: *ddr\_stress\_tester\_vX.xx.zip*
- The tool will first need to run a DDR initialization script for the specific i.MX6 development boards can be found in this zip file under

## Option 2 DDR Stress Tester: JTAG Interface

A hardware debugger connected to the board via the JTAG

Results are shown on the UART serial port (115200-8-n-1).

- Archive file: *ddr\_stress\_tester\_jtag\_vX.xx.zip*
- As with the GUI tool, the JTAG/debugger option will first location of the example scripts (which are found in the

Freescle DDR Test Tool

Load Init Script

TARGET MX6DQ ARM Speed Default  Verify DCD Address

DDR Density Default DDR 0 DDR channel 0

VDD\_ARM\_CAP Auto - auto + VDD\_SOC\_CAP Auto - auto + Set Voltage

DDR Calibration

MR1 Value(HEX) 0000

DDR Freq(MHz) 0

Calibration Save Result

DDR Stress Test

Over Night Test

Start Freq(MHz) 0

End Freq(MHz) 0

Stress Test Save Result

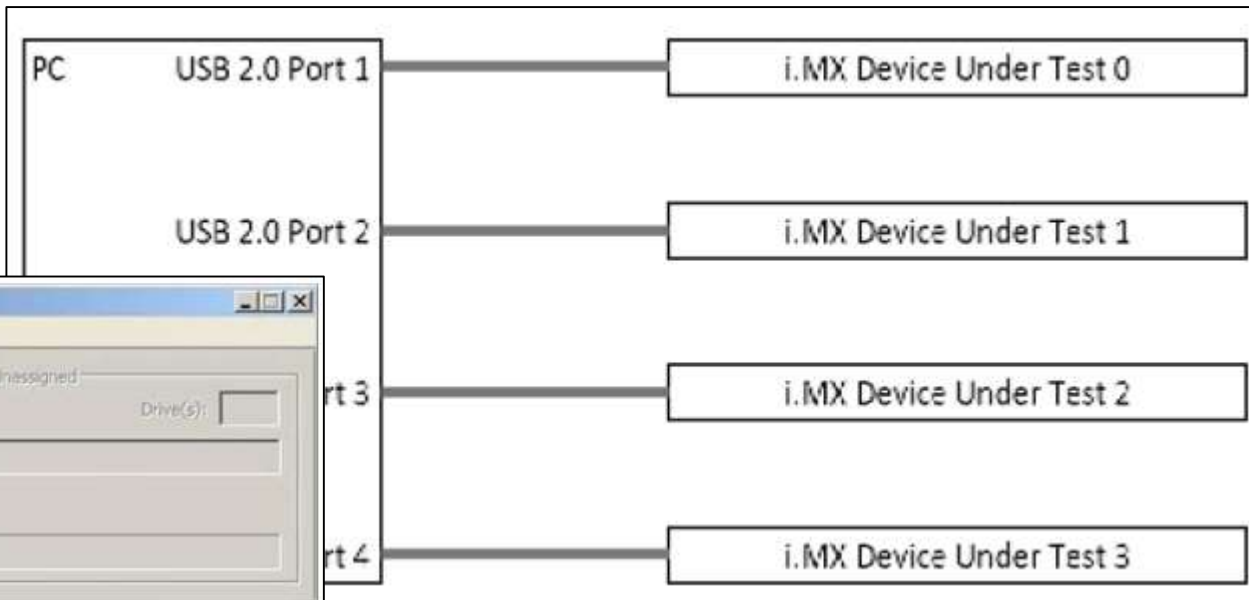
32bit Memory Read/Write

ADDR(HEX)

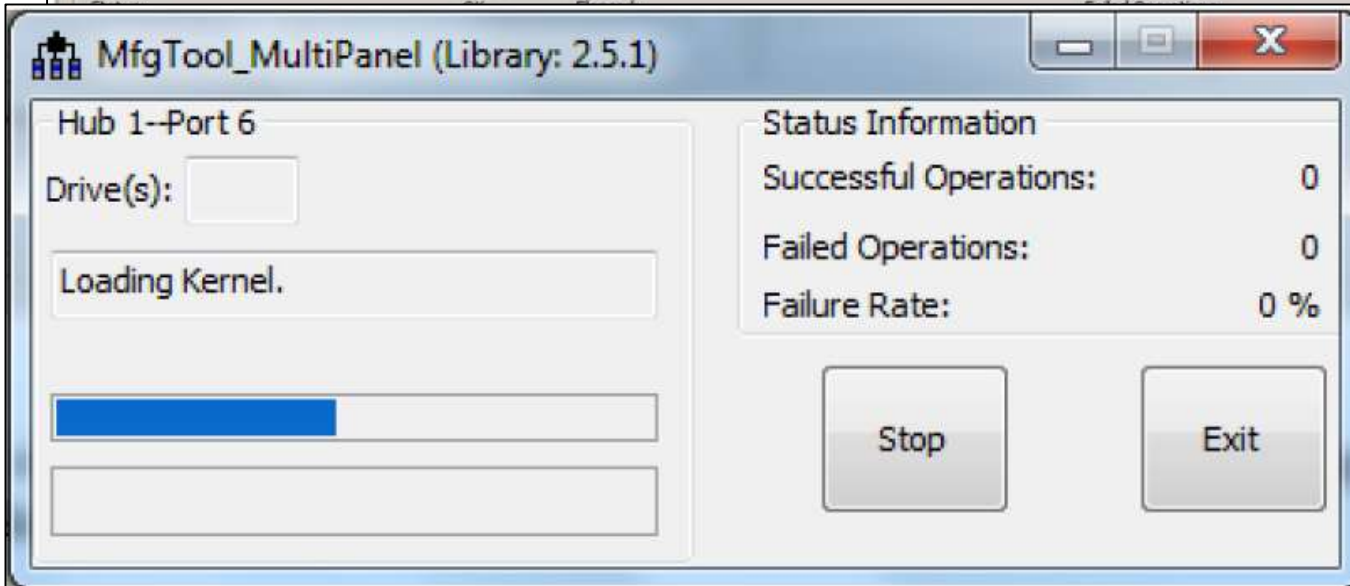
SIZE 1 WORD Read

DATA(HEX) Write

# MFGTools - Tools Page – [link](#) (i.MX6)



- Configurable through xml input files.
- Flexible to program NAND, eMMC, QSPI, SDCard, etc.
- Can burn fuses and other internal registers.
- Can work with multiple boards at the same time.



# Power Management – Device Page – [link](#) – (PF3000)

- Documentation
  - App Notes
  - Data Sheets
- Dev Boards

NXP > Power Management > PMICs > PMICs for i.MX Processors

## PF3000: 12-Channel Configurable PMIC UPDATED ☆

[Overview](#) | [Documentation](#) | [Software & Tools](#) | [Buy / Parametrics](#) | [Package / Quality](#) | [Training & Support](#)

**Jump To**  
[Overview](#)  
[Features](#)  
[Related Products](#)

### Overview

The PF3000 power management integrated circuit (PMIC) features a configurable architecture that supports numerous outputs with various current ratings as well as programmable voltage and sequencing. This enables the PF3000 to power the core processor, external memory and peripherals to provide a single-chip system power solution.

The PF3000 is ideally suited to Cortex™ A7 based [i.MX 7Solo](#) and [i.MX 7Dual](#) application processors to meet low power application requirements. The PF3000 is a perfect companion for the very low power Cortex™ A9 core product family including the [i.MX 6DualLite](#) and [all single-core Cortex A9 i.MX processors](#).

Compatibility with i.MX applications processors is shown in multiple reference designs and facilitates software controlled, dynamic voltage scaling.

[Data Sheet](#) | [Application Notes](#) | [Buy](#) | [Sample](#)

### PF3000 Functional Internal Block Diagram

PF3000 Functional Internal Block Diagram

OTP Startup Configuration		Power Generation	
OTP Prototyping (Try before burn)	Voltage	Switching Regulators	Linear Regulators
Sequence and Timing	Phasing and Frequency Selection	SW1A (0.70 V to 3.3 V, 1.0 A)	VCC_SD (1.80 V or 1.85 V, 100 mA) or (2.85V or 3.3V, 100 mA)
Bias & References		SW1B	V33 (2.85 V to 3.30 V, 350 mA)
Indicator/Internal Core Voltage Reference			



## Other Tips

1. Copy the DDR, eMMC and PMIC Design.
2. NAND, eMMC or QSPI Flash?
3. Leave the boot selection for protothype.
4. Leave the Ethernet for development.
5. No production rootfs on SDCard.  
    But leave an SDCard for bring-up.
6. Leave the OTG USB connector for factory programming.
7. Follow the design check list.
8. Submit your schematics for review.
9. Thermal on higher performance devices.



# SECURE BOOT



# High Assurance Boot – AN4581 – [link](#) – (HABv4)

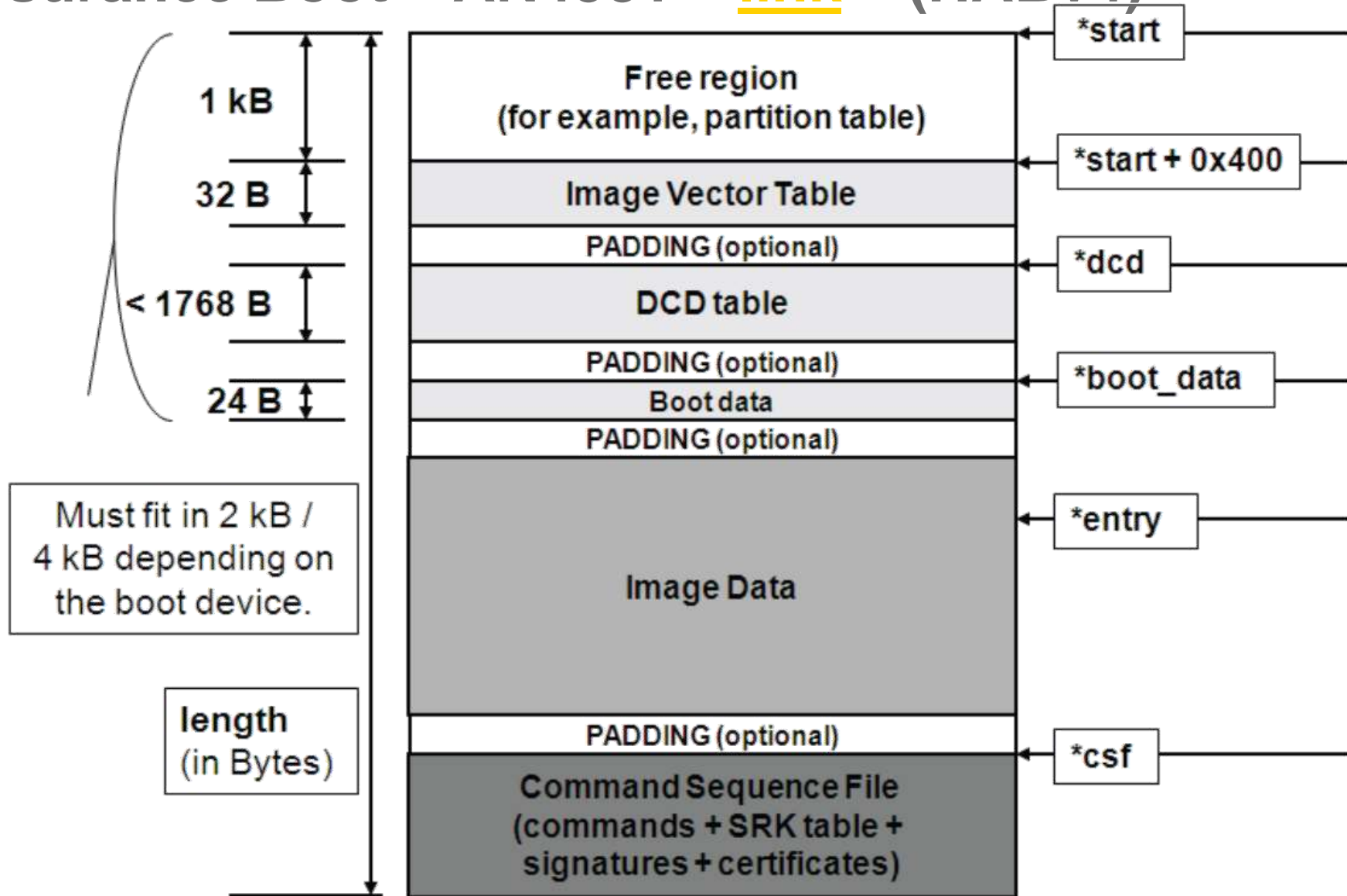


Figure 1. Typical memory layout of a signed image



# Code Signing Tool - Tools Page – [link](#) (iMX6)

## Generating Keys

```
bruno@bruno:~/cst-2.3.2/keys$ ./hab4_pki_tree.sh
```

## Generating Key Table

```
bruno@bruno:~/cst-2.3.2/keys$ ../linux64/srktool -help
```

## Extracting fuse values

```
bruno@bruno:~/cst-2.3.2/keys$ hexdump -e '/4 "0x"' -e '/4 "%X""\n"' SRK_1_2_3_4_fuse.bin
```

## Programming fuses

```
Uboot: fuse prog <bank> <word> <value>
```

## Create a boot command file on xml-like format

```
bruno@bruno:~/cst-2.3.2/keys$ gedit csf-uboot
```

## Generate the signature binary from the cs

```
bruno@bruno:~/cst-2.3.2/keys$ ./cst --o csf-uboot.bin < csf-uboot
```

## Concatenate the signature to u-boot

```
bruno@bruno:~/cst-2.3.2/keys$ cat u-boot.imx csf-uboot.bin > u-boot-signed.imx
```

## On u-boot, check boot status

```
Uboot: hab_status
```

## Burn last fuses



# SOFTWARE DESIGN



# NXP Public GIT – git repository – [link](#) (all NXP products)

Name	Description	
<i>auto</i>		
buildroot.git	Automotive Buildroot Tree	18593
freertos.git	Automotive FreeRTOS Tree	7485
linux.git	Automotive Linux Tree	1033
u-boot.git	Automotive U-Boot Tree	1795
<i>crypto</i>		
cryptodev.git	Freescale SEC upstream Linux driver tree	3861
<i>embedded-software</i>		
usbdm-eclipse.git	Unnamed repository; edit this file 'description'	3937
<i>graphics</i>		
svg_tool.git	Tool for converting an SVG image file to a	1734
<i>imx</i>		
fsl-arm-yocto-bsp.git	i.MX Linux BSP Release Yocto Project m	4968
imx-firmware.git	i.MX Firmware	873
linux-2.6-imx.git	Freescale i.MX Linux Tree	508
<u>linux-imx.git</u>	i.MX Linux Kernel	506
meta-fsl-bsp-release.git	i.MX BSP Yocto Project Release Layer	4071
meta-nxp-agl.git	NXP AGL Yocto Project Demo Layer	7656
meta-nxp-genivi.git	NXP Genivi Yocto Project Demo Layer	3748
meta-nxp-imx-scm.git	NXP SCM i.MX Yocto Project Layer	2033
meta-nxp-iotg.git	NXP IOTG Yocto Project Demo Layer	509
meta-nxp-xbmc.git	NXP XBMC Yocto Project Demo Layer	3974
uboot-imx.git	Freescale i.MX u-boot Tree	

README	18593
REPORTING-BUGS	7485
arch	1033
block	1795
crypto	3861
drivers	3937
firmware	1734
fs	4968
include	873
init	508
ipc	506
kernel	4071
lib	7656
mm	3748
net	2033
samples	509
scripts	3974



# Document Bundle - Tools Page – [link](#) (iMX6)

## Documentation

### [-] Android

- Android M6.0.1\_2.1.0 BSP Documentation
- Android 4.4.3 Patch Documentation
- Android L5.0.0\_1.0.1 Patch Documentation

### [+] Archived

### [-] Linux

- Linux 4.1.15\_2.0.0 BSP & Multimedia Codecs Documentation
- Linux 4.1.15\_1.2.0 BSP & Multimedia Codecs Documentation
- Linux 4.1.15\_1.1.0 BSP & Multimedia Codecs Documentation
- Linux 4.1.15\_1.0.0 BSP & Multimedia Codecs Documentation
- Linux 3.14.52 BSP & Multimedia Codecs Documentation
- Linux L3.14.38 6ul Documentation

### [+] Archived

### [-] Others

- PCI Express® Certification Guide for the i.MX 6SoloX
- i.MX Series Manufacturing Toolkit for Linux 4.1.15 Release

- ▲ fsl-yocto-L4.1.15\_1.2.0-ga
- ▲ fsl-yocto-L4.1.15\_1.2.0-ga
  - doc

- doc
- Freescle\_Yocto\_Project\_User's\_Guide.pdf
- README

- i.MX\_6\_Graphics\_User's\_Guide.pdf
- i.MX\_BSP\_Porting\_Guide.pdf
- i.MX\_Linux\_Reference\_Manual.pdf
- i.MX\_Linux\_Release\_Notes.pdf
- i.MX\_Linux\_User's\_Guide.pdf
- i.MX\_VPU\_Application\_Programming\_Interface\_Linux\_Reference\_Manual.pdf

# BSP User Guide – Docs Bundle – [link](#) (iMX6)

- Introduction
- Basic Terminal Setup
- Booting Linux OS
  - Enabling Solo Emulation
- Power Management
- Multimedia
- Graphics
- Security
- Connectivity

- Booting Linux OS
  - Software overview
  - Manufacturing Tool
  - Preparing an SD/MMC card to boot
  - Downloading images
  - How to boot the i.MX boards
  - Flash memory maps
  - Running Linux OS on the target
  - Enabling Solo Emulation

- Power Management
  - Suspend and resume
  - CPU frequency scaling
  - Bus frequency scaling

- Multimedia
  - Freescale multimedia packages
  - Building limited access packages
  - Multimedia use cases
    - Playback use cases
    - Audio encoding
    - Video encoding
    - Transcoding
    - Audio recording
    - Video recording
    - Audio/Video recording
    - Camera preview
    - Recording the TV-in source
    - Web camera
    - HTTP streaming
    - Real Time Streaming Protocol (RTSP) playback
    - RTP/UDP MPEGTS streaming
    - RTSP streaming server
    - Video conversion
    - Video composition
  - Pulseaudio input/output settings
  - Overlaysink usage
  - Installing gstreamer1.0-libav into rootfs

- Graphics
  - fsl-gpu-sdk
  - G2D-fsl-samples
  - viv\_samples
  - Qt 5



# BSP Release Notes - Tools Page – [link](#) (iMX6)

## 1 Release Contents

This document contains important information about the package contents, supported features, known issues and limitations in this release.

This release contains the latest updates for the last GA release. For more information on changes, see the manifest Readme at [index: fsl-arm-yocto-bsp.git](#) and the Change Log at [index: fsl-arm-yocto-bsp.git](#).

### Supported hardware SoC/board

- i.MX 6QuadPlus SABRE-SD Board and Platform
- i.MX 6QuadPlus SABRE-AI Board
- i.MX 6Quad SABRE-SD Board and Platform
- i.MX 6DualLite SABRE-SD Board
- i.MX 6Quad SABRE-AI Board
- i.MX 6DualLite SABRE-AI Board
- i.MX 6SoloLite EVK Board
- i.MX 6SoloX SABRE-SD Board
- i.MX 6SoloX SABRE-AI Board
- i.MX 7Dual SABRE-SD Board
- i.MX 6UltraLite EVK Board

- 📖 BSP Supported Features
- 📖 Kernel Boot Parameters
- 📖 Known Issues/Limitations
- 📖 Multimedia
  - 📖 Freescale GStreamer plugins
  - 📖 Freescale playback engine API
  - 📖 Freescale recording engine API
  - 📖 Freescale Qt Applications
  - 📖 Multimedia feature matrix
  - 📖 Known issues and limitations for multimedia

Feature	Supported board	Comment
		i.MX 6SoloLite EVK supports LPDDR2 400 MHz @ 32 bit and boot using L2Cache as OCRAM
		i.MX 7Dual SABRE-SD supports DDR3 533 MHz @ 32 bit and boot using L2Cache as OCRAM
		i.MX 6UltraLite EVK supports DDR3 400 Mhz @ 16 bit
<b>Machine-specific layer</b>		
ARM® Core	All i.MX	6SABRE-SD, 6SABRE-AI, 6SoloLite, 6SoloX-SD, and 6SoloX-AI support the ARM Cortex-A9 processor. 7D-SABRE-SD supports the ARM Cortex-A7 processor. 6UltraLite EVK supports the ARM Cortex-A7 processor. Supports reboot and power-off.
Memory	All i.MX	The user/kernel space is split 2G/2G.
Interrupt	All i.MX	GIC.
Lock	All i.MX	Controls the system frequency and clock tree distribution.
Timer (GPT)	All i.MX	System timer tick support.
PIO/EDIO	All i.MX	GPIO is initialized in earlier phase according to hardware design.
IOMUX	All i.MX	Provides the interfaces for I/O configuration. IOMUX-V3 version is used.
<b>DMA engine</b>		
DMA	All i.MX	Conforms to the DMA engine framework.
PBH-Bridge-DMA	6SABRE-AI	Conforms to the DMA engine framework. This feature requires a NAND U-Boot.
<b>Character device drivers</b>		
MXC UART	All i.MX	i.MX 6 SABRE-SD, and SoloLite EVK support console through internal Debug UART1. i.MX 6SoloX SABRE-SD and SABRE-AI support Cortex-A9 processor through UART1 and Cortex-M4 processor through UART2. i.MX 7Dual SABRE-SD Cortex-A7 processor through UART1 and Cortex-M4 processor through UART2. i.MX 6UltraLite EVK Cortex-A7 processor through UART1. i.MX 6 SABRE-AI supports console through internal Debug UART 4.
<b>Power Management Drivers</b>		
All i.MX		Supports Anapod regulator management.
All i.MX		Supports standby mode and dormant (mem) mode.
All i.MX		2 levels CPUIdle supported; purely WFI and WFI with wait mode enabled.
All i.MX		CPUFreq can be used for CPU frequency adjustment. The Interactive governor is added and enabled by default.
All i.MX		Supports the system bus clock frequency scaling.
All i.MX		-
<b>Networking drivers</b>		
All i.MX		i.MX 6Quad/SoloX board supports AR8031 PHY, i.MX 6UltraLite EVK board supports KSZ8081 PHY, and i.MX 7Dual SABRE-SD board supports BCM54220 PHY. i.MX 6SoloX SABRE-SD, SABRE-AI, and i.MX 7Dual SABRE-SD support AVB Features.

Kernel parameter	Description	Typical value	Used when
video on 6SoloLite	Tells the ELCDIF FB driver which LCD panel is in use and which bpp should be used for the Frame Buffer.	video=mx_c_elcdif_fb:SEIKO-WVGA,bpp=16	Used when enabling LCDIF to select the correct panel parameters to use. bpp=16 selects RGB565 FB pix format Note: if only use EPDC FB, then turn off ELCDIF FB by "video=mx_c_elcdif_fb:off"
video on 7D SABRE-SD	Tells the ELCDIF FB driver which LCD panel is in use and which bpp should be used for the Frame Buffer.	video=mx_cfb0:dev=mipi_dsi,TRULY-WVGA,il=RGB24	Used when primary displaying on the TRULY-WVGA MIPI DSI LCD panel.
dmfc	Tells the kernel/driver how to set the IPU DMFC segment size.	None Or dmfc=3	"dmfc=1" means DMFC_HIGH_RESOLUTION_DC. "dmfc=2" means DMFC_HIGH_RESOLUTION_DP. "dmfc=3" means DMFC_HIGH_RESOLUTION_ONLY_DP. DMFC_HIGH_RESOLUTION_ONLY_DP can only be set by the command line. It is recommended to set this when no IPU connects the two panels. When it is set, each IPU can only connect one panel.
mtddparts on 6SABRE-AI	Tells the kernel mtd partition information.	mtddparts=gpmi-nand:16m(boot), 16m(kernel), 1024m(rootfs), -(user)	When to enable NAND. The partition: 16m (boot), 16m (kernel), 1024m (rootfs) is an example, you can change it according to your needs.





# Yocto User Guide - Tools Page – [link](#) (iMX6)

## 1 Overview

This document describes how to build an image for an i.MX Freescale board by using a Yocto Project build environment. It describes the Freescale release layer and Freescale-specific usage.

- Features
- Host Setup
  - Host packages
  - Setting up the repo utility
- Yocto Project Setup
- Image Build
- Image Deployment
  - Creating a Custom DISTRO
  - Creating a Custom Board Configuration
- Appendix A: Frequently Asked Questions
- Appendix B: References

- Image Deployment
  - Flashing an SD card image
  - Manufacturing Tool, MFGTool

- Image Build
  - Build configurations
  - Choosing a Freescale Yocto project image
  - Building an image
  - Bitbake options
  - U-Boot configuration
  - Build scenarios
    - X-11 image on i.MX 6Quad SABRE-SD
    - Frame Buffer image on i.MX 6QuadPlus SABRE-AI
    - Xwayland image on i.MX 6SoloX SABRE-SD
    - Wayland image on i.MX 6SoloX SABRE-SD
    - Restarting a build environment
    - Chromium Browser on X11, XWayland and Wayland
    - Qt 5 and QtWebEngine browsers

- imx6qpsabreauto
- imx6qpsabresd
- imx6ulevk
- imx6dlsabreauto
- imx6dlsabresd
- imx6qsabreauto
- imx6qsabresd
- imx6slevk
- imx6solosabreauto
- imx6solosabresd
- imx6sxsabresd
- imx6sxsabreauto
- imx7dsabresd

**Table 1. Freescale Yocto project images (continued)**

Image name	Target	Provided by layer
fsl-image-machine-test	An FSL Community i.MX core image with console environment - no GUI interface	meta-fsl-demos
fsl-image-gui	Builds a Freescale image with a GUI without any Qt content.	meta-fsl-bsp-release/imx/meta-sdk
fsl-image-qt5	Builds an opensource Qt 5 image. These images are only supported for i.MX SoC with hardware graphics. They are not supported on the i.MX 6UltraLite and i.MX 7Dual.	meta-fsl-bsp-release/imx/meta-sdk



# Linux Reference Manual - Tools Page – [link](#) (iMX6)

- Chapter 3: Machine-Specific Layer (MSL)
- Chapter 4: Smart Direct Memory Access (SDMA) API
- Chapter 5: AHB-to-APBH Bridge with DMA (APBH-Bridge-DMA)
- Chapter 6: Image Processing Unit (IPU) Drivers
- Chapter 7: MIPI DSI Driver
- Chapter 8: LVDS Display Bridge(LDB) Driver
- Chapter 9: Video for Linux Two (V4L2) Driver
- Chapter 10: Electrophoretic Display Controller (EPDC) Frame Buffer Driver
- Chapter 11: Pixel Pipeline (PxP) DMA-ENGINE Driver
- Chapter 12: ELCDIF Frame Buffer Driver
- Chapter 13: Graphics Processing Unit (GPU)
- Chapter 14: Wayland
- Chapter 15: On-Chip High Definition Multimedia Interface (HDMI) Driver
- Chapter 16: External High-Definition Multimedia Interface (HDMI) for i.MX 6SoloLite
- Chapter 17: X Windows Acceleration
- Chapter 18: Video Processing Unit (VPU) Driver
- Chapter 19: OmniVision Camera Driver
- Chapter 20: MIPI CSI2 Driver
- Chapter 21: Low-level Power Management (PM) Driver
- Chapter 22: PF100 Regulator Driver
- Chapter 23: CPU Frequency Scaling (CPUFREQ) Driver
- Chapter 24: Dynamic Bus Frequency Driver
- Chapter 25: Thermal Driver
- Chapter 26: Anapop Regulator Driver
- Chapter 27: SNVS Real Time Clock (SRTC) Driver
- Chapter 28: Advanced Linux Sound Architecture (ALSA) System on a Chip (ASoC) Sound Driver
- Chapter 29: Asynchronous Sample Rate Converter (ASRC) Driver
- Chapter 30: The Sony/Philips Digital Interface (S/PDIF) Driver
- Chapter 31: SPI NOR Flash Memory Technology Device (MTD) Driver
- Chapter 32: MMC/SD/SDIO Host Driver
- Chapter 33: NAND GPMI Flash Driver
- Chapter 34: SATA Driver
- Chapter 35: Inter-IC (I2C) Driver
- Chapter 36: Enhanced Configurable Serial Peripheral Interface (ECSPI) Driver
- Chapter 37: FlexCAN
- Chapter 38: Media Lo
- Chapter 39: CHIPIDEA USB Driver
- Chapter 40: PCI Express Root Complex Driver
- Chapter 41: EIM NOR Driver
- Chapter 42: Quad Serial Peripheral Interface (QuadSPI) Driver
- Chapter 43: Fast Ethernet Controller (FEC) Driver
- Chapter 44: ENET IEEE-1588 Driver
- Chapter 45: Universal Asynchronous Receiver/Transmitter (UART) Driver
- Chapter 46: Wi-Fi BCM4339 Driver
- Chapter 47: Pulse-Width Modulator (PWM) Driver
- Chapter 48: Watchdog (WDOG) Driver
- Chapter 49: OProfile
- Chapter 50: CAAM (Cryptographic Acceleration and Assurance Module)
- Chapter 51: Remote Processor Messaging (RPMsg)
- Chapter 52: Display Content Integrity Checker (DCIC)
- Chapter 53: ADC Driver
- Chapter 54: Video Analog-to-Digital Converter (VADC)
- Chapter 55: Bluetooth® BCM4339 Driver
- Chapter 42: Quad Serial Peripheral Interface (QuadSPI) Driver
  - Introduction
  - Hardware Operation
  - Software Operation
  - Driver Features
  - Source Code Structure
  - Menu Configuration Options
- Samsung MIPI DSI Driver
- Subscriber Identification Module (SIM) Driver



# Graphics User Guide - Tools Page – [link](#) (iMX6)

- ⊕ Chapter 2 i.MX 6 G2D API
- ⊕ Chapter 3 i.MX 6 EGL and OGL Extension Support
- ⊕ Chapter 4 i.MX 6 Framebuffer API
- ⊕ Chapter 5 OpenCL
- ⊕ Chapter 6 XServer Video Driver
- ⊕ Chapter 7 Vivante Software Tool Kit
- ⊕ Chapter 8 GPU Tools
- ⊕ Chapter 9 GPU Memory Introduction
- ⊕ Chapter 10 Application Programming Recommendations
- ⊕ Chapter 11 Demo Framework
- ⊕ Chapter 12 Environment Variables Summary

- ⊖ Chapter 10 Application Programming Recommendations
  - 10.1 Understand the system configuration and target application
  - 10.2 Optimize off chip data transfer such as accessing off-chip DDR memory/mobile DDR memory
  - 10.3 Avoid random cache or memory accesses
  - 10.4 Optimize your use of system memory
  - 10.5 Target a fixed frame rate that is visibly smooth
  - 10.6 Minimize GL state changes
  - 10.7 Batch primitives to minimize the number of draw calls
  - 10.8 Perform calculations per vertex instead of per fragment/pixel
  - 10.9 Enable early-Z, hierarchical-Z and back face culling
  - 10.10 Use branching carefully
  - 10.11 Do not use static or stack data as vertex data - use VBOs instead
  - 10.12 Use dynamic VBO if data is changing frame by frame
  - 10.13 Tessellate your data so that Hierarchical Z (HZ) can do its job

- ⊖ Chapter 4 i.MX 6 Framebuffer API
  - 4.1 Overview
  - ⊕ 4.2 API data types and environment variables
    - 4.3 API description and syntax
- ⊖ Chapter 5 OpenCL
  - ⊕ 5.1 Overview
  - ⊕ 5.2 Vivante OpenCL Implementation
  - ⊕ 5.3 Optimization for OpenCL Embedded Profile
  - ⊕ 5.4 OpenCL Debug Messages
- ⊖ Chapter 6 XServer Video Driver
  - ⊕ 6.1 EXA driver
  - ⊕ 6.2 XRandR
- ⊕ Chapter 7 Vivante Software Tool Kit
- ⊖ Chapter 8 GPU Tools
  - ⊕ 8.1 gputool
  - 8.2 gmem\_info tool
  - ⊕ 8.3 Aptrace user guide
- ⊖ Chapter 9 GPU Memory Introduction
  - 9.1 GPU memory overview
  - 9.2 GPU memory pools
  - 9.3 GPU memory allocators
  - 9.4 GPU reserved memory
  - 9.5 GPU memory base address



















# Device Reference Manual - Device Page – [link](#) (iMX6UL) - about 4000 pages

- Chapter 2: Memory Maps
- Chapter 3: Interrupts and DMA Events
- Chapter 4: External Signals and Pin Multiplexing
- Chapter 5: Fusemap
- Chapter 6: External Memory Controllers
- Chapter 7: System Debug
- Chapter 8: System Boot
- Chapter 9: Multimedia
- Chapter 10: Clock and Power Management
- Chapter 11: System Security
- Chapter 12: ARM Cortex A7 Platform (CA7)
- Chapter 13: Analog-to-Digital Converter (ADC)
- Chapter 14: AHB to IP Bridge (AIPSTZ)
- Chapter 15: AHB-to-APBH Bridge with DMA (APBH-Bridge-DMA)
- Chapter 16: Asynchronous Sample Rate Converter (ASRC)
- Chapter 17: 40-BIT Correcting ECC Accelerator (BCH)
- Chapter 18: Clock Controller Module (CCM)
- Chapter 19: CMOS Sensor Interface (CSI)
- Chapter 20: Enhanced Configurable SPI (ECSPI)

- Chapter 21: External Interface Module (EIM)
- Chapter 22: 10/100-Mbps Ethernet MAC (ENET)
- Chapter 23: Enhanced Periodic Interrupt Timer (EPIT)
- Chapter 24: Flexible Controller Area Network (FLEXCAN)
- Chapter 25: General Power Controller (GPC)
- Chapter 26: General Purpose Input/Output (GPIO)
- Chapter 27: General Purpose Media Interface (GPMI)
- Chapter 28: General Purpose Timer (GPT)
- Chapter 29: I2C Controller (I2C)
- Chapter 30: IOMUX Controller (IOMUXC)
- Chapter 31: Keypad Port (KPP)
- Chapter 32: Enhanced LCD Interface (eLCDIF)
- Chapter 33: Multi Mode DDR Controller (MMDC)
- Chapter 34: Medium Quality Sound (MQS)
- Chapter 35: On-Chip OTP Controller (OCOTP\_CTRL)
- Chapter 36: On-Chip RAM Memory Controller (OCRAM)
- Chapter 37: Power Management Unit (PMU)
- Chapter 38: Pulse Width Modulation (PWM)
- Chapter 39: Pixel Pipeline (PXP)
- Chapter 40: Quad Serial Peripheral Interface (QuadSPI)

- Chapter 41: ROM Controller with Patch (ROMC)
- Chapter 42: Synchronous Audio Interface (SAI)
- Chapter 43: Smart Direct Memory Access Controller (SDMA)
- Chapter 44: Subscriber Identification Module (SIM)
- Chapter 45: System JTAG Controller (SJC)
- Chapter 46: Secure Non-Volatile Storage (SNVS)
- Chapter 47: Shared Peripheral Bus Arbiter (SPBA)
- Chapter 48: Sony/Philips Digital Interface (SPDIF)
- Chapter 49: System Reset Controller (SRC)
- Chapter 50: Temperature Monitor (TEMPMON)
- Chapter 51: Touch Screen Controller (TSC)
- Chapter 52: TrustZone Address Space Controller (TZASC)
- Chapter 53: Universal Asynchronous Receiver/Transmitter (UART)
- Chapter 54: Universal Serial Bus Controller (USB)
- Chapter 55: Universal Serial Bus 2.0 Integrated PHY (USB-PHY)
- Chapter 56: Ultra Secured Digital Host Controller (uSDHC)
- Chapter 57: Watchdog Timer (WDOG)
- Chapter 58: Crystal Oscillator (XTALOSC)

# Chip Errata - Device Page – [link](#) (iMX6UL)

 Table 1. Document Revision History
 Table 2. Summary of Silicon Errata
 ERR008958
 ERR008959
 ERR008960
 ERR008961
 ERR007265
 ERR009455
 ERR009606
 ERR009535
 ERR004446
 ERR005829
 ERR007805
 ERR005778
 ERR009596
 ERR009541
 ERR009454
 ERR006281

Errata	Name	Solution	Page
<b>ARM® – Cortex A7</b>			
<a href="#">ERR008958</a>	ARM/MP: 814220—B-Cache maintenance by set/way operations can execute out of order	No fix scheduled	5
<a href="#">ERR008959</a>	ARM/MP: 809719—C PMU events 0x07, 0x0C, and 0x0E do not increment correctly	No fix scheduled	7
<a href="#">ERR008960</a>	ARM/MP: 805420—C PMU event counter 0x14 does not increment correctly	No fix scheduled	9
<a href="#">ERR008961</a>	ARM/MP: 804069—C Exception mask bits are cleared when an exception is taken in Hyp Mode	No fix scheduled	10
<b>CCM</b>			
<a href="#">ERR007265</a>	CCM: When improper low-power sequence is used, the SoC enters low power mode before the ARM core executes WFI	No fix scheduled	11
<b>Clock</b>			
<a href="#">ERR009455</a>	Clock: 24 MHz Oscillator does not start up	Fixed in silicon revision 1.1	12
<b>eCSPI</b>			
<a href="#">ERR009606</a>	eCSPI: In master mode, burst lengths of 32n + 1 will transmit incorrect data	No fix scheduled	13
<a href="#">ERR009535</a>	eCSPI: Burst completion by SS signal in slave mode is not functional	No fix scheduled	14
<b>EIM</b>			
<a href="#">ERR004446</a>	EIM: AUS mode is nonfunctional for devices larger than 32 MB	No fix scheduled	15
<b>FlexCAN</b>			
<a href="#">ERR005829</a>	FlexCAN: FlexCAN does not transmit a message that is enabled to be transmitted in a specific moment during the arbitration process	No fix scheduled	16
<b>I2C</b>			
<a href="#">ERR007805</a>	I2C: When the I2C clock speed is configured for 400 kHz, the SCL low period violates the I2C specification	No fix scheduled	18
<b>MMDC</b>			
<a href="#">ERR005778</a>	MMDC: DDR Controller's measure unit may return an incorrect value when operating below 100 MHz	No fix scheduled	19
<a href="#">ERR009596</a>	MMDC: ARCR_GUARD bits of MMDC Core AXI Re-ordering Control register (MMDC_MAARCR) does not behave as expected	No fix scheduled	20



# Application Notes - Device Page – [link](#) (iMX6Q)

Application Notes (17)	
Name/Description	
i.MX 6Quad/6Dual Personality Fuses (REV 0)	<a href="#">PDF</a> (53.6 kB) AN5323 [English]
MIPI-CSI2 Peripheral on i.MX6 MPUs (REV 0)	<a href="#">PDF</a> (862.5 kB) AN5305 [English]
i.MX 6 Temperature Sensor Module - Application Note (REV 0)	<a href="#">PDF</a> (507.2 kB) AN5215 [English]
Secure Boot on i.MX50, i.MX53, and i.MX 6 Series using HABv4 (REV 1)	<a href="#">PDF</a> (867.8 kB) AN4581 [English]
<b>Common Hardware Design for i.MX 6Dual/6Quad and i.MX 6Solo/6DualLite (REV 2)</b>	<a href="#">PDF</a> (322.8 kB) AN4397 [English]
Configuring Secure JTAG for the i.MX 6 Series Family of Applications Processors (REV 1)	<a href="#">PDF</a> (560.1 kB) AN4686 [English]
Fast Image Processing with i.MX 6 Series (REV 1)	<a href="#">PDF</a> (1.2 MB) AN4629 [English]
<b>i.MX 6 Series DDR Calibration (REV 2)</b>	<a href="#">PDF</a> (426.3 kB) AN4467 [English]
Configuring USB on i.MX 6 Series Processors (REV 1)	<a href="#">PDF</a> (175.2 kB) AN4589 [English, 中文]

<b>Influence of Pin Setting on System Function and Performance (REV 0)</b>	09 Feb 2015
<a href="#">PDF</a> (687.7 kB) AN5078 [English]	
<b>AN4724, i.MX 6Dual/6Quad/6DualPlus/6QuadPlus Product Usage Lifetime Estimates - Application Note (REV 2)</b>	06 Aug 2014
<a href="#">PDF</a> (264.1 kB) AN4724 [English]	
<b>i.MX 6 Audio Clock Configuration Options (REV 0)</b>	26 Jun 2014
<a href="#">PDF</a> (1.3 MB) AN4952 [English]	
<b>AN4784: PCIe Certification Guide for i.MX 6Dual/6Quad and i.MX 6Solo/6DualLite - Application Note (REV 0)</b>	14 Oct 2013
<a href="#">PDF</a> (271.7 kB) AN4784 [English]	
<b>AN4671, i.MX 6 Series HDMI Test Method for Eye Pattern and Electrical Characteristics - Application Notes (REV 0)</b>	22 Apr 2013
<a href="#">PDF</a> (432.4 kB) AN4671 [English]	
<b>i.MX 6 Series Thermal Management Guidelines (REV 0)</b>	10 Dec 2012
<a href="#">PDF</a> (3.7 MB) AN4579 [English]	
<b>i.MX 6Dual/6Quad Power Consumption Measurement (REV 0)</b>	24 Oct 2012
<a href="#">PDF</a> (476.0 kB) AN4509 [English]	
<b>Using Open Source Debugging Tools for Linux on i.MX Processors (REV 0)</b>	19 Jul 2012
<a href="#">PDF</a> (251.5 kB) AN4553 [English]	

# SUPPORT RESOURCES



# i.MX Community – community page – [link](#) – (all i.MX)

All Content (325) 📄 Documents (262) 📺 Videos (60)

Type to filter by text Filter by tag Sort by latest activity: newest first ▼

Title	Author	Date
Boundary Devices - FreeRTOS BSP v1.0.1 for Nitrogen7 & Nit6_SoloX	Gary Bisson	August 3, 2016 4:13:06 PM
imx7 ethernet not working with BCM54220 phy <small>Shared by sudeep kumar c from i.MX Community</small>	sudeep kumar c	August 3, 2016 4:13:06 PM
need A7001 security micro pin mapping details	shridhar hl	August 3, 2016 4:13:06 PM
SINLINX SIN-IMX6UL SDK BOARD	alex lee	August 3, 2016 4:13:06 PM
SGTL5000 audio quality debug	foxmaze	July 12, 2016 7:29:20 PM
imx6sl Eink屏幕uboot显示问题	kangzhikuan	July 10, 2016 8:05:56 PM
i.mx257 usb 擦除 NANDFLASH	haifeng xi	July 9, 2016 6:44:08 PM
ARM Webinar in #Россия (Russia) about i.MX - Процессорные платы на базе iMX6 (ARM)	Florian Wohlrab	June 28, 2016 6:05:10 PM
PMIC PF3000/3001 + i.MX 6UL Resources	Zhi Liu	June 20, 2016 2:50:01 AM
Unable to open connection to supplicant on "/data/system/wpa_supplicant/wlan0" <small>Shared by Raj kamsani from i.MX Community</small>	Raj kamsani	August 24, 2016 12:36:00 AM
RloTboard	Last modified by Martha Diana Torres Ramirez	May 16, 2016 10:04:28 AM
Boundary Devices - Crank Storyboard demo on i.MX7 Nitrogen7	Gary Bisson	May 3, 2016 9:33:45 AM
NXP Technology Form #NXPFTF 2016, we will join! - TechNexion	Florian Wohlrab	April 28, 2016 7:53:09 PM

Community
Home
News
Content
People
Places

## i.MX Solutions

in i.MX Community ▼

Overview
Content
People
Subspaces

### WELCOME TO THE NEW NXP COMMUNITY

NXP and Freescale combine to bring complete solutions to your design challenges in RF, Security, Connectivity, Automotive, Analog, Sensors and Networking.

Using NXP Community

Demo Lab

NXP IoT Solutions Center

FTF 2016 Presentations

Smarter World Tour

University Programs



# Support Center – Cases- support page – [link](#) (all NXP products)

**NXP** Bruno English Cart

ALL Search...

PRODUCTS APPLICATIONS **SUPPORT** ABOUT

NXP Community  
Online Academy  
Classroom Training & Events  
Video Vault  
University Programs  
**Sales and Support**  
B2B Integration  
Browser Compatibility  
Professional Support and Service Resources  
Order Samples  
Buy Direct  
Distributor Network  
Pricing and Availability  
Buy Obsolete Products  
Tracking and Tracing Shipment  
NXP Professional Services  
Documentation

NXP > Sales and Support

## Sales and Support

### ASK FOR HELP

**NXP<sup>®</sup> Supported Communities**  
Interact with our support team and industry colleagues.

Ask technical questions, share your issue and research thousands of answers.

- CodeWarrior<sup>®</sup> Development Tools
- i.MX Community (SoCs and PMIC Support)
- Kinetis<sup>®</sup> Microcontrollers
- LPC
- NFC
- PowerQUICC
- QorIQ<sup>®</sup> Processors
- S12 / MagniV<sup>®</sup> Microcontrollers
- Wireless Connectivity

[View All >](#)

**NXP Support Tickets**  
Reach the support team through private tickets if you cannot share details publicly. *We may direct tickets to the community that do not contain private information.* Tickets receive the same priority and are answered by the same team as community posts.

	Submit new tickets	View existing tickets
nxp.com sign in	<ul style="list-style-type: none"><li>Web or Access issues</li><li>Contact eCommerce Support</li><li>Training</li></ul>	<ul style="list-style-type: none"><li>Ticket (Service Request) begins with 1-... or 2-...</li></ul>
Uses separate sign in	<ul style="list-style-type: none"><li>Hardware &amp; Software</li><li>All Other Issues</li></ul>	<ul style="list-style-type: none"><li>All Other Tickets (Cases)</li></ul>

**Non-Technical Issues**

Live Chat: Offline

实时中文聊天 离线

Phone Support



# Enter a CASE to get Online Technical Support from NXP

- Use this link: <http://nxpcommunity.force.com/community/CommunityContactSupport>
- Use your NXP TechSupport credentials (NOT the same like the [www.nxp.com](http://www.nxp.com) login !) or Request Password if you forget yours or Register as new user
- Make sure you have and select a support “context folder” for this project. If not, create it first.
- Enter your support CASE within this folder

Login with the details you registered on this page:

User Name

Password

[Forgot Your Password?](#)  
[New user for the support ticket system? Please register here](#)  
[Sign In as Internal User](#)

Login

If no verification email received, please check the spam folder. Verification is sent from [engineers.corner@nxp.com](mailto:engineers.corner@nxp.com)

**1** To create project folder: Press here to continue  
(If you did this last time already, just select the project folder and add another case)

**2** Within folder, press “Add a new case” and fill the form. Some fields are mandatory.

**3** On main page, select project folder.  
(You may invite your colleagues, NXP FAE, DFAE, customers, etc.)

eBike Converter Re-design

+ Add a new case + Invite people



# PARTNERS



# Hardware SoM Partners

- Hardware & Software complexity.
- Time to market
- Support



# Software Partners

- Time to market
- Yocto BSP
- Hardware + Software



yocto .  
PROJECT

# Training Partners

- Linux
  - Embedded Linux
  - Device Drivers
  - Programação
  - Debugging
- Yocto
- Android
- FreeRTOS

Embedded Labworks

[Início](#) [Empresa](#) [Treinamentos](#) [Consultoria](#) [Clientes](#) [Contato](#) [Blog](#)

## TREINAMENTOS E CONSULTORIA EM SISTEMAS EMBARCADOS

A Embedded Labworks é uma empresa especializada em projetos de software para sistemas embarcados, provendo serviços de treinamento, consultoria e desenvolvimento, com foco em Linux embarcado, Android embarcado e sistemas operacionais de tempo real (RTOS).

[Conheça nossos treinamentos](#)



SECURE CONNECTIONS  
FOR A SMARTER WORLD