LPC800 MCU TECHNICAL OVERVIEW

NXP'S FASTEST GROWING PORTFOLIO FOR THE BROAD, 8-BIT ALTERNATIVE MARKET

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SECURE CONNECTIONS
FOR A SMARTER WORLD

AGENDA

- LPC Microcontroller Portfolio
- Cortex-M0+ Introduction
- LPC84x Technical Overview
- LPC84x Software, Tools and Support
- Summary
- Questions

NXP LPC

Consumer and Industrial Microcontrollers for the Broad Market

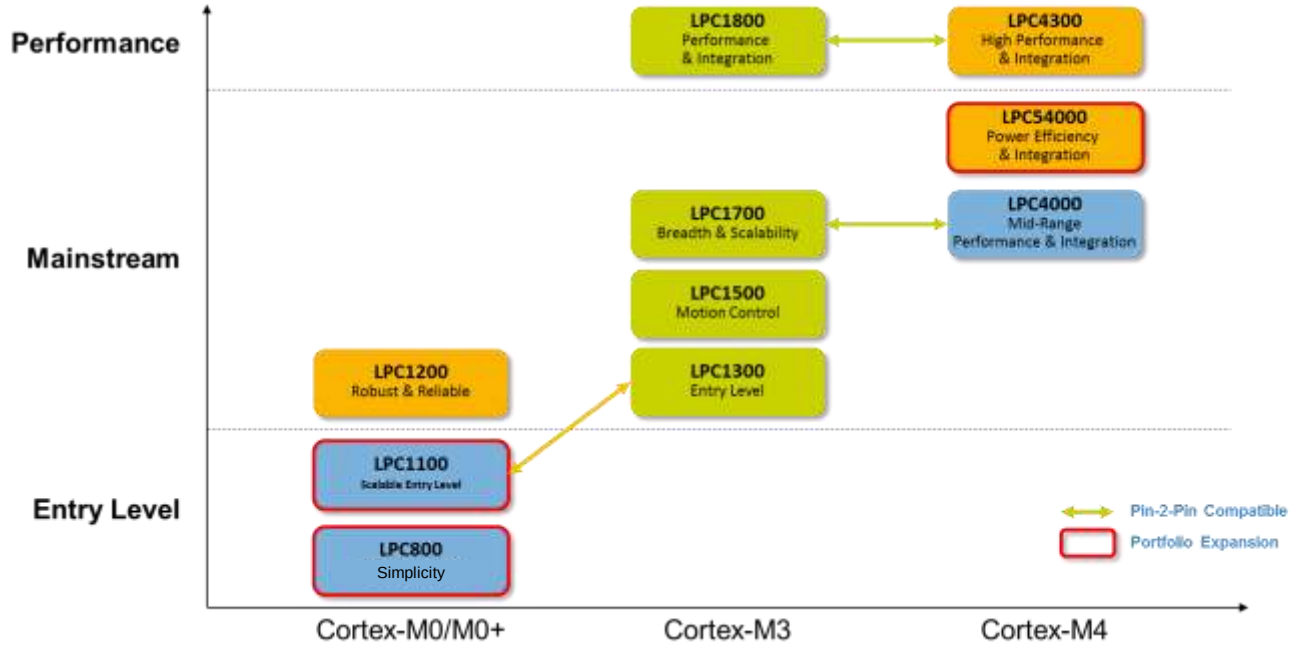
LPC 32-bit Microcontrollers for the Mass Market

Over 1B units shipped	>400 part numbers	Thriving ecosystem	Complementary professional development suite (HW/SW)

Open Development Environment

- **MCUXpresso IDE with Easy to Use Software Code Bundles**
- **Development, Debug & Expansion Boards**
- **Developer Community**

Complete Portfolio of Cortex-M MCUs



Easy Development **Scalable Expansion**

LPC Focus on Consumer & Industrial Markets

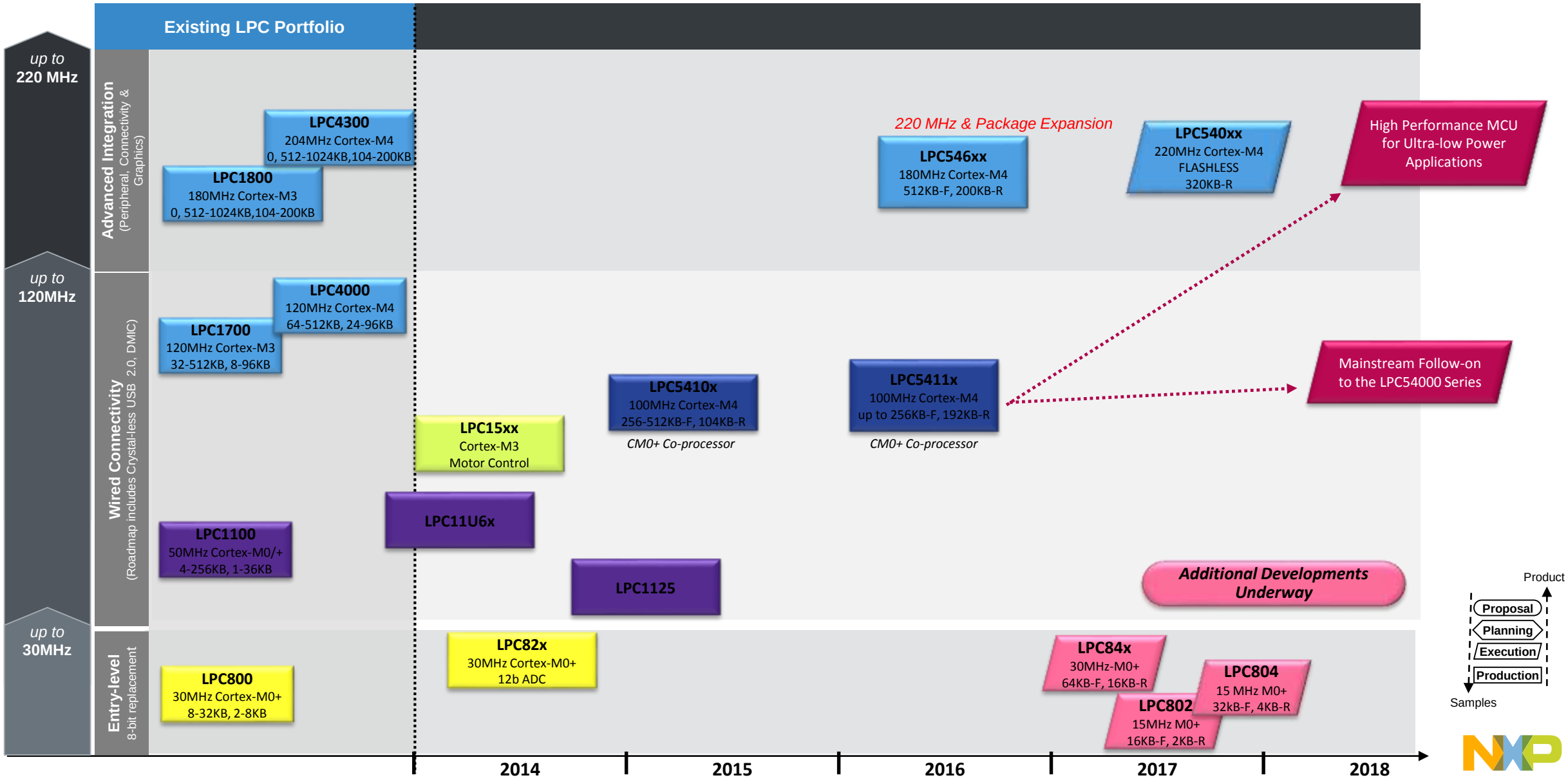
1. **Product Innovation.**
2. **Ecosystem & Partners.**
3. **Supply, Longevity, & Quality.**
4. **Local Support.**
5. **Extensive Software & Tools.**

» Accelerating Transition from 8-bit to **Entry-level Cortex-M0+ based MCUs**

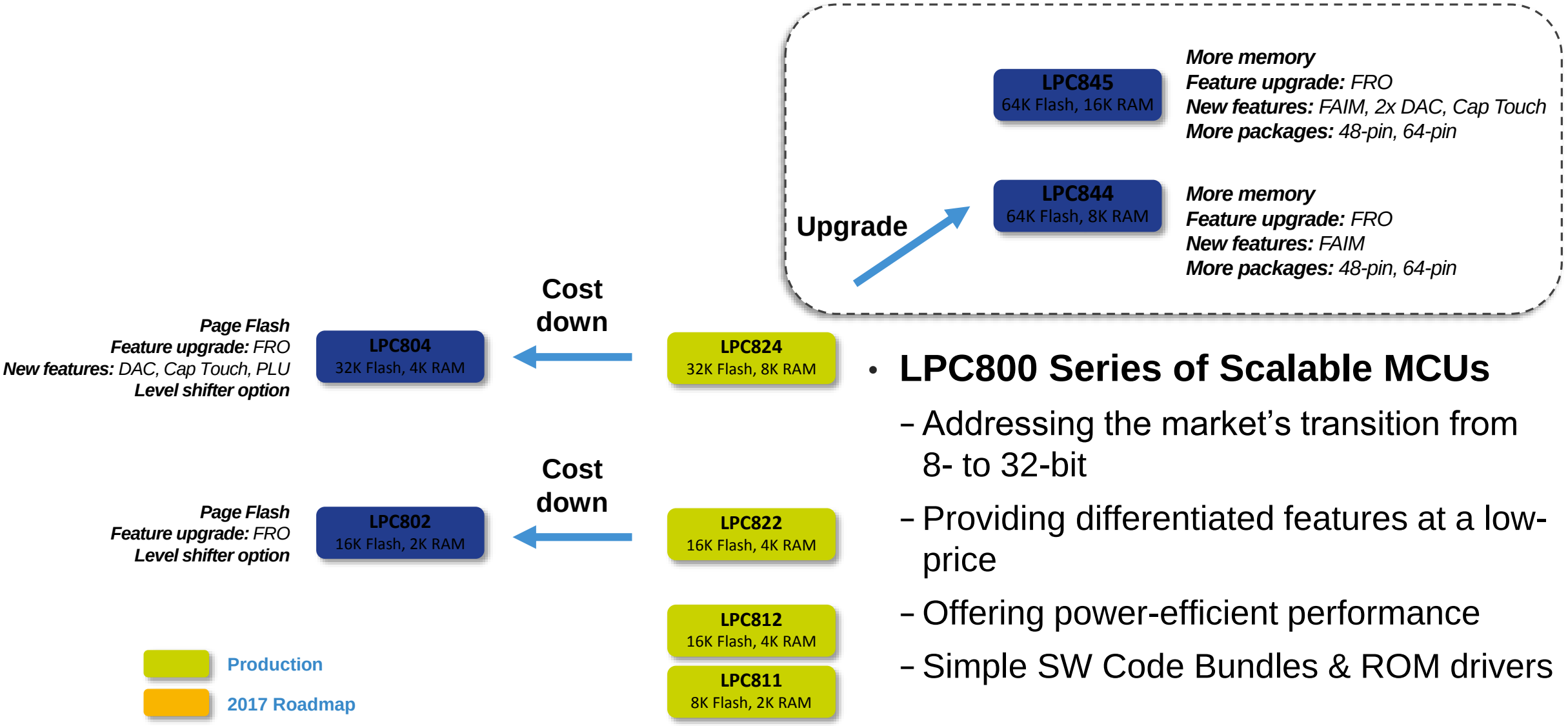
» **Low Power, High Performance MCUs** for Energy Conscious Application

Low Power MCU Roadmap

(not a complete portfolio summary)



LPC84x Part of NXP's Rapid Expansion of the LPC800 Series



- **LPC800 Series of Scalable MCUs**
  - Addressing the market's transition from 8- to 32-bit
  - Providing differentiated features at a low-price
  - Offering power-efficient performance
  - Simple SW Code Bundles & ROM drivers

Leaving behind proprietary 8-bit MCUs for **LPC800**

a diverse range of applications













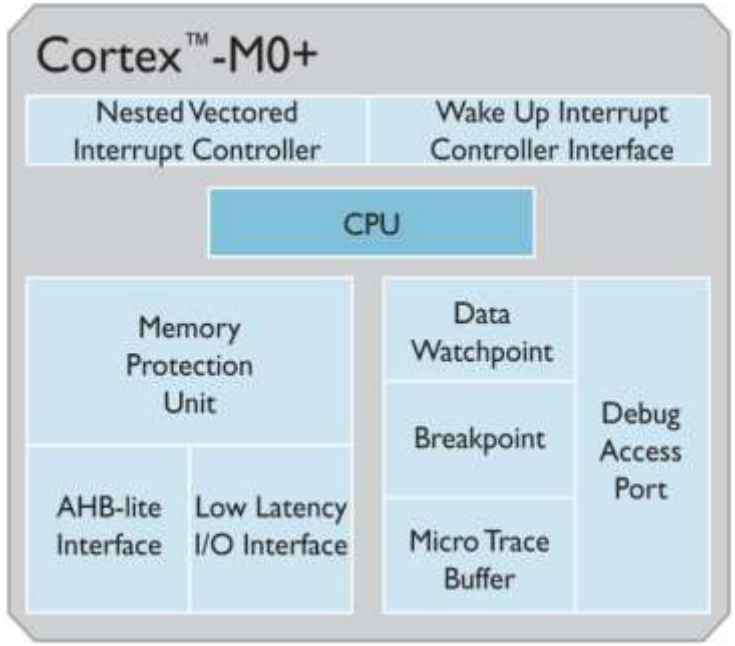



01.

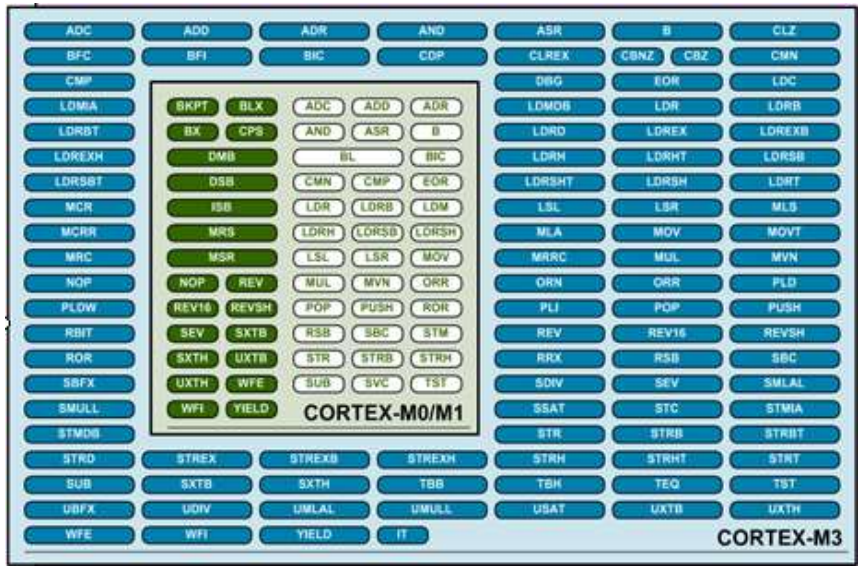
CORTEX-M0+ OVERVIEW

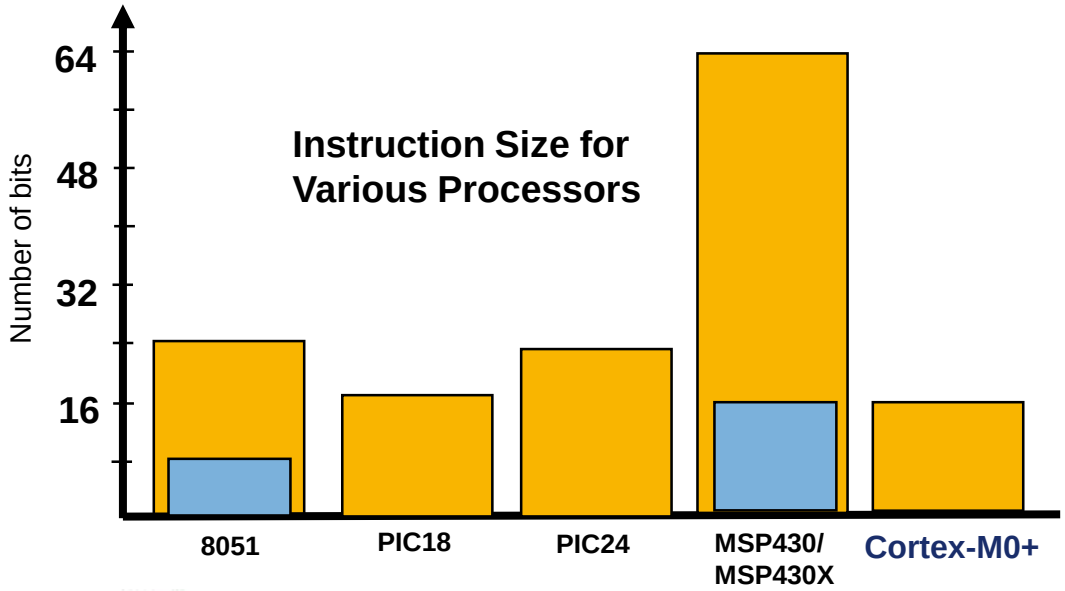
Cortex-M0+ Overview

- High performance 32-bit CPU
- 2 stage pipeline
- Performance efficiency
  - 1.77 CoreMark/MHz - 0.93 DMIPS/MHz
- Deterministic operation
- Single cycle IO
- Built-in Nested Vectored Interrupt Controller (NVIC) with Wake-up Interrupt Controller (WIC)
- Debug using 2 pins with up to 4 breakpoints and 2 watchpoints
- Micro Trace Buffer (MTB)
- Vector Table relocation
- Thumb2 instructions (56 instructions)

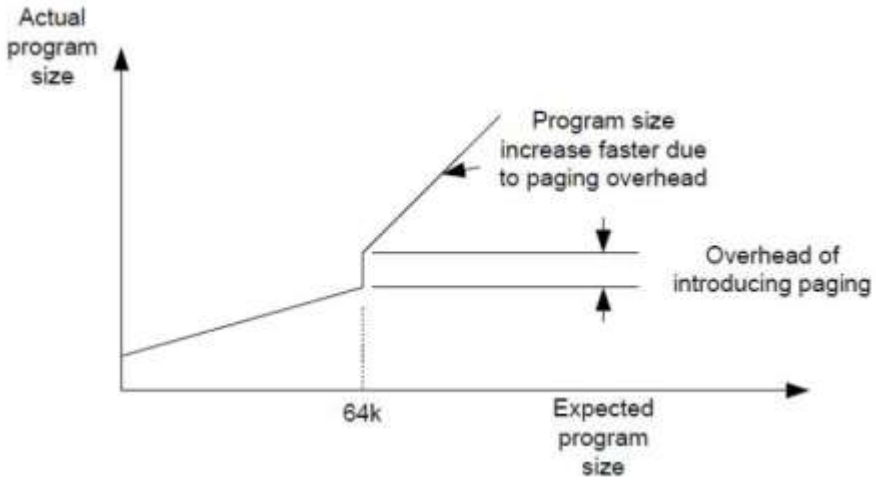


Superior Code Density





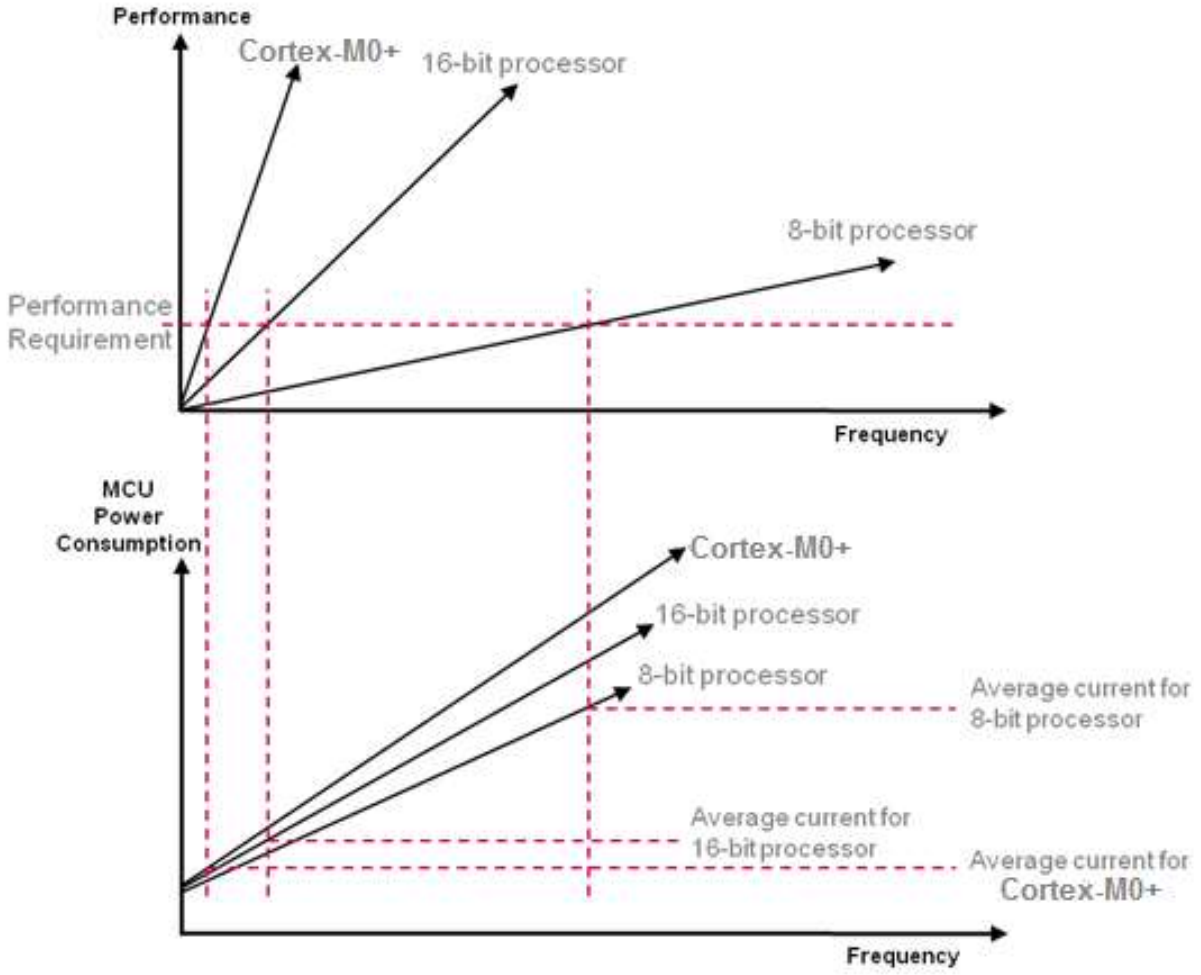
- Leading to superior code density:
  - In Cortex-M0/M0+ all instructions (except BL) are **16 bits wide** instructions
  - **Over 64kB of address space,** 8- and 16- processors have to introdu paging, leading to extra overhead in code



Cortex-M0+ Has Lower Power Consumption

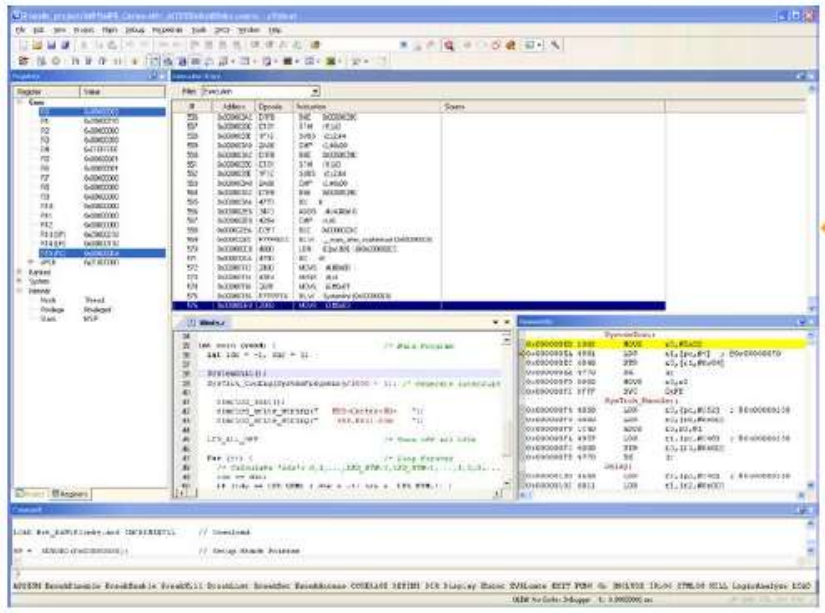
- Cortex-M0+ runs at a much slower clock frequency for the same required performance

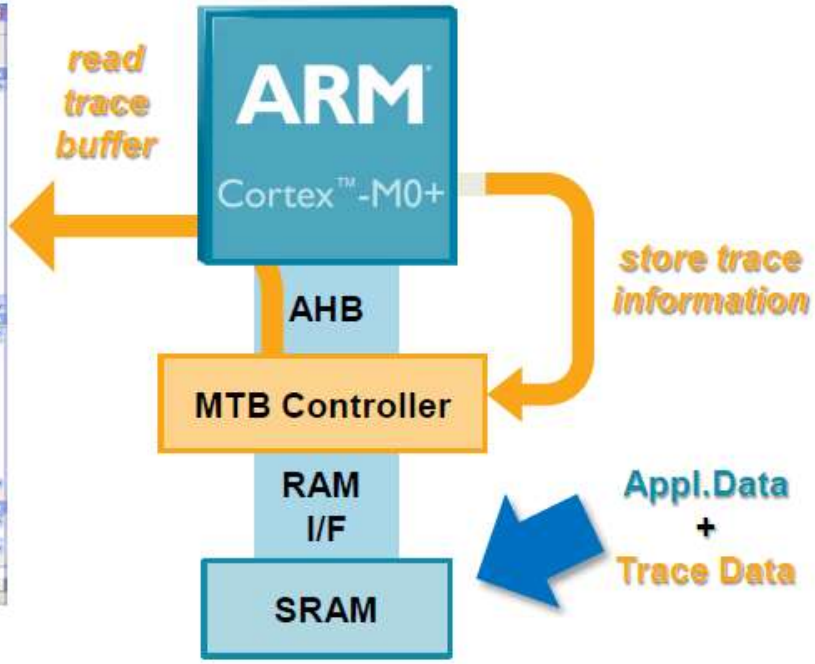
- Cortex-M0+ can sleep most of the time, or it can handle additional tasks



Cortex-M0+ Micro-Trace Buffer (MTB)

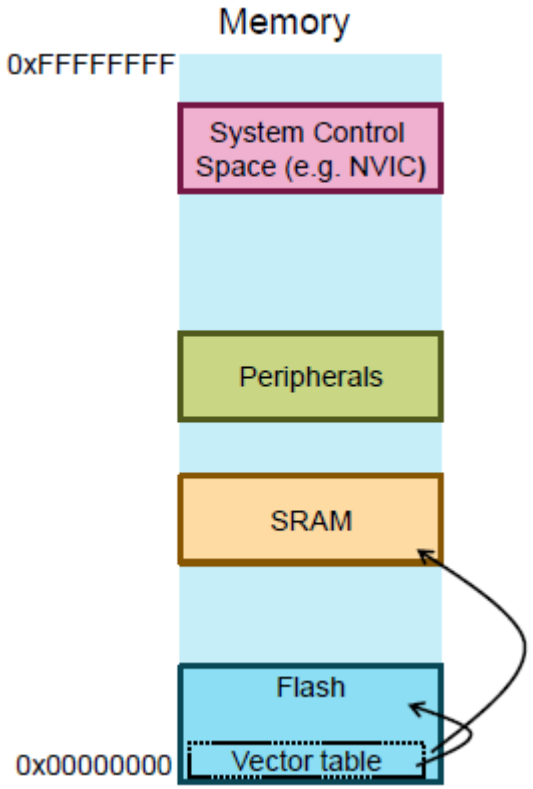
- Trace store in RAM (non-instusive)
- Read over Serial Wire / JTAG (CPU stopped)





Cortex-M0+ Vector Table Relocation

- Relocate vector table in other locations in flash or SRAM
- Exception vector reconfiguration at runtime

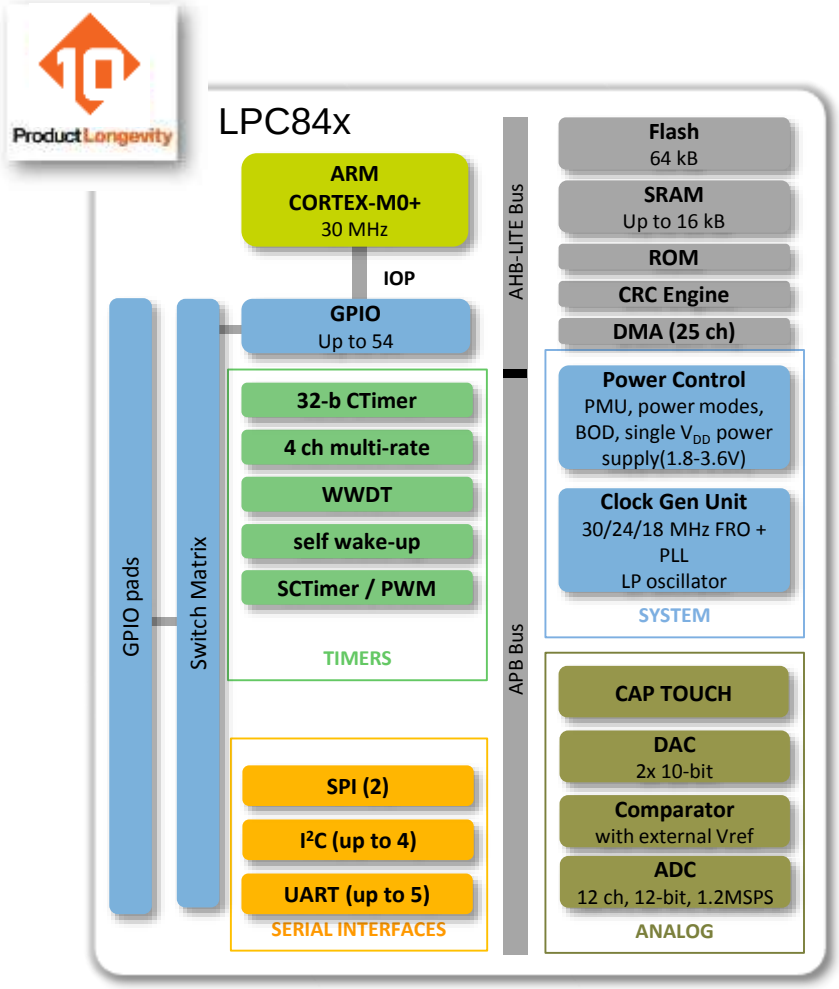


02.

LPC84x Block DIAGRAM

LPC84x Overview

Expansion from LPC824 with Added Flexibility & Features



System

- **30-MHz** Cortex-M0+ ARM core
- 64 kB Flash, with 64 B page size
- Up to 16 kB RAM
- **Separate 256b user programmable memory (FAIM) for device configuration at Reset**
- 25-channel DMA

Exceptional power efficiency

- Four Low power modes
- Low Power Boot at 1.5 MHz using FAIM

Serial connectivity and GPIOs

- Up to 4 I2C (1 Fm+, 3 Fm), 2 SPI, Up to 5 UART
- Up to 54 GPIOs
- **Pattern Matching**
- **Switch matrix** for flexible I/O pin assignment

Analog

- 12-bit, 1.2MSPS ADC, 12ch
- **Analog Comparator**: 4 input pins
- **2x 10-bit DAC**
- **Capacitive Touch Interface**

Timers

- **SCTimer**/PWM, 1x 32-bit CTimer
- 4-ch Multi-Rate Timer (MRT)
- Wakeup Timer, Watchdog Timer

Single **power supply**: **1.8 to 3.6V**

Temperature range: **-40 to +105 ° C** (ambient)

Packages: HVQFN33, HVQFN48, LQFP48, LQFP64

03.

LPC84x MEMORY

Memory Block

- Flash: 1kB sectors with 64-byte page program/erase
  - Organization: 64 sectors x 16 pages/sector x 64 bytes/page
- 64 Byte page erase and write
- Erase/Program Time (100ms/1ms)
- Endurance
  - Sector erase – 10,000 cycles
  - Page erase – 1,000 cycles

Sector number	Sector size [kB]	Page number	Address range	4 kB	8 kB	16 kB
0	1	0 -15	0x0000 0000 - 0x0000 03FF	yes	yes	yes
1	1	16 - 31	0x0000 0400 - 0x0000 07FF	yes	yes	yes
2	1	32 - 47	0x0000 0800 - 0x0000 0BFF	-	yes	yes
3	1	48 - 63	0x0000 0C00 - 0x0000 0FFF	-	yes	yes
4	1	64 - 79	0x0000 1000 - 0x0000 13FF	-	yes	yes
5	1	80 - 95	0x0000 1400 - 0x0000 17FF	-	yes	yes
6	1	96 - 111	0x0000 1800 - 0x0000 1BFF	-	yes	yes
7	1	112 - 127	0x0000 1C00 - 0x0000 1FFF	-	yes	yes
8	1	128 - 143	0x0000 2000 - 0x0000 23FF	-	yes	yes
9	1	144 - 159	0x0000 2400 - 0x0000 27FF	yes	yes	yes
10	1	160 - 175	0x0000 2800 - 0x0000 2BFF	yes	yes	yes
11	1	176 - 191	0x0000 2C00 - 0x0000 2FFF	yes	yes	yes
12	1	192 - 207	0x0000 3000 - 0x0000 33FF	yes	yes	yes
13	1	208 - 223	0x0000 3400 - 0x0000 37FF	yes	yes	yes
14	1	224 - 239	0x0000 3800 - 0x0000 3BFF	yes	yes	yes
15	1	240 - 255	0x0000 3C00 - 0x0000 3FFF	yes	yes	yes

FAIM Features

- Fast Initialization Memory (FAIM) is a 256-bit memory or 8 words
- FAIM is multiple time programmable (MTP), limited to 200 program cycle
- MCU initial configuration after reset
  - FRO clock frequency
  - Pin configuration with pull-ups, pull-downs, and tri-state
  - SWD
  - ISP interface for programming and ISP pins
- One reset cycle to take effect
- FAIM programming voltage range is 3.0 V ≤ Vdd ≤ 3.6 V

Code Read Protection Levels

- Four levels of the Code Read Protection
- This feature allows user to enable different levels of security in the system so that access to the on-chip flash and use of the SWD and ISP can be restricted
- When needed, CRP is invoked by programming a specific pattern into a dedicated flash location
- Program CRP pattern at location @2FC

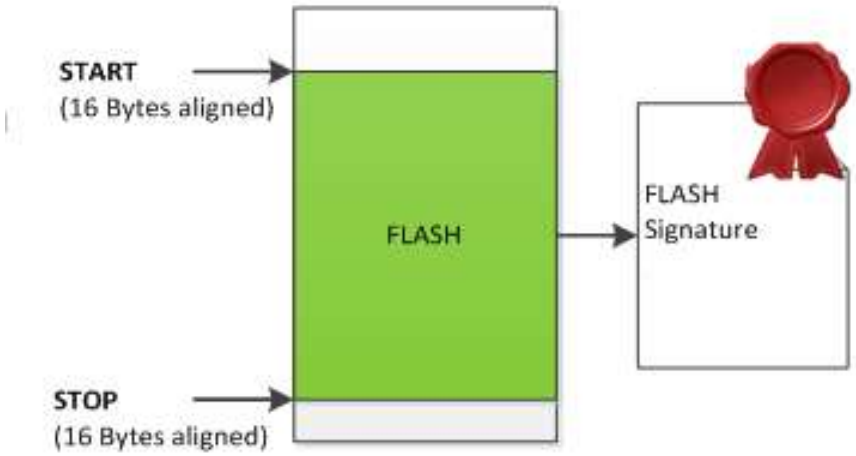
	Read Code	Full Chip Erase	Erase Sectors	Program Sectors	SWD Access
NO CRP	**Enabled**	**Enabled**	**Enabled**	**Enabled**	**Enabled**
CRP 1	Disabled	**Enabled**	**Enabled**	**Enabled**	Disabled
CRP 2	Disabled	**Enabled**	Disabled	**Enabled**	Disabled
CRP 3	Disabled	Disabled	Disabled	Disabled	Disabled
NO_ISP	No Protection (SWD can read)	Disabled	Disabled	Disabled	**Enabled**

FLASH Accelerator and FLASH Controller

- FLASH Controller is for FLASH WRITE
- FLASH Accelerator is for FLASH READ
- AHB Matrix, accessing by M0+ core, DMA
- FLASH buffer for buffering and prefetching, 8 x 32 bits
- Buffer is for both data and instruction fetch, configurable
- FLASH TIM $FLASHAccessTime = (FLASHTIM + 1) \times SystemClock$

FLASH Signature Generator

- Controls hardware flash signature generation (32-bits)
- Procedures
  - Set 16-Bytes aligned start address
  - Set 16-Bytes aligned stop address, start calculation
  - Wait calculation done by checking status register
  - Retrieve 32-bit FLASH signature



$$Duration = int\left(\frac{60}{AHB\ Period} + 3\right) * (FMSTOP - FMSSTART\ +\ 1)$$

04.

LPC84x CLOCK GENERATION UNIT

LPC84x Clock Generation Unit

Clock Sources	Characteristics
FRO Oscillator	System clock by default Stable. Quick power up and power down 30/24/18 MHz (±1% over 0 C to 70 C)
Watchdog Oscillator	Low power operation Low frequency oscillator 9.3 kHz – 2.3 MHz (+/- 40%)
MAIN Oscillator	1 MHz – 25 MHz
CLKIN	1 MHz – 25 MHz
SYS PLL	Multiplies the clock source (FRO, Main Osc, CLKIN) Up to 100 MHz and divide down to 30 MHz or less
Low Power Oscillator	Low power operation Low frequency oscillator 10 kHz (+/- 40%)

Free Running Oscillator (FRO)

- Low power internal Free-Running Oscillator (~100 uA, replaces former “IRC”)
- Provides selectable outputs: 30 MHz, 24 MHz or 18 MHz which can be divided
- Factory Trimmed for 30 MHz/24 MHz/18 MHz

  +/- 1% accuracy over 0 C to 70 C
- Some peripherals allow asynchronous operation from FRO while CPU operates from main clock
- FRO can be used as Main clock or PLL clock source
- Reduces dependency on System PLL
  - Benefit: fast restart after halting the CPU by sleep modes
  - Benefit: low power!
- Main Clock selects the 12 MHz FRO as the clock source on power-up or after reset

05.

LPC84x ROM

BOOT ROM

- 16 KB on-chip ROM
- Bootloader
  - In-System Programming (ISP) API calls
  - Update FLASH via USART, I2C or SPI
- ROM API
  - In-Application Programming (IAP) of flash memory
  - Integer divide routines
  - FAIM APIs
  - FRO API

FLASH programming (in ROM)

- In-System Programming (ISP)

  Programming or re-programming the on-chip flash memory, using the boot loader software through the USART, I2C, SPI. This can be done when the part resides in the end-user board

- In Application Programming (IAP)

  Performing erase and write operation on the on-chip flash memory, as directed by the end-user application code

ISP Entry from bootloader (via Pins)

- ISP Entry and mode is configurable in FAIM
- FAIM Content Invalid → Use Default Configuration + Auto Detection
- FAIM Content valid

ISP interface select WORD 0 (bit 31:30)	
00	USART0
01	I2C0
10	SPI0
11	Reserved

ISP PIN select WORD 1 (bit 31:30)	
4:0	ISP Rx pin select (USART0 Rx, SPI MOSI)
7:5	ISP Rx port select (USART0 Rx, SPI MOSI)
12:8	ISP Tx pin select (USART0 Tx, SPI MISO)
15:13	ISP Tx port select (USART0 Tx, SPI MISO)
20:16	ISP clock pin select (SPI SCK)
23:21	ISP clock port select (SPI SCK)
28:24	ISP SPI0 SSELN0 pin select
31:29	ISP SPI0 SSELN0 port select

06.

LPC84x GPIO

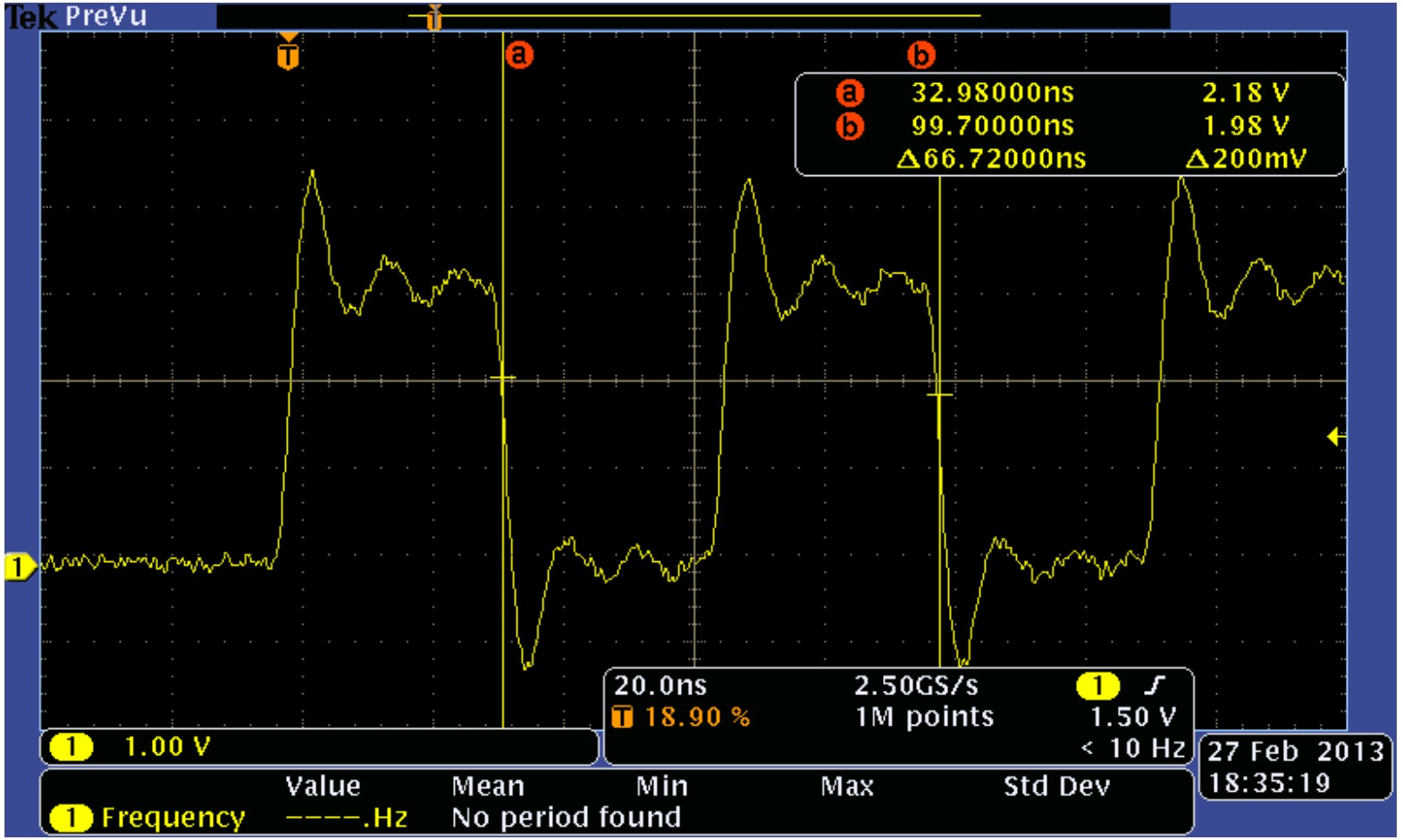
LPC84x: Flexible I/O Port

- I/O Port
  - Up to 54 GPIOs
  - **Single cycle** access to all port pins
  - **Support high frequency I/O toggling** – As fast as CPU_Clock/2 = 15 MHz!
  - **Enhanced GPIO Pin Manipulation** – Capable of simultaneously reading Bit/Byte/Word or toggling up to 54 I/Os per two instructions
  - Up to 8 pins can be selected from all GPIO pins as edge- or level-sensitive **interrupt** requests
  - **Programmable** Internal pull-up/pull-down resistor, open-drain function, input inverter, and repeater mode
  - All GPIO pins are equipped with a **programmable digital glitch filter**. The filter rejects input pulses with a selectable duration of shorter than one, two, or three cycles of a filter clock
  - High-current source output driver (20 mA) on four pins
  - High-current sink driver (20 mA) on two true open-drain pins

Enhanced GPIO Pin Manipulation

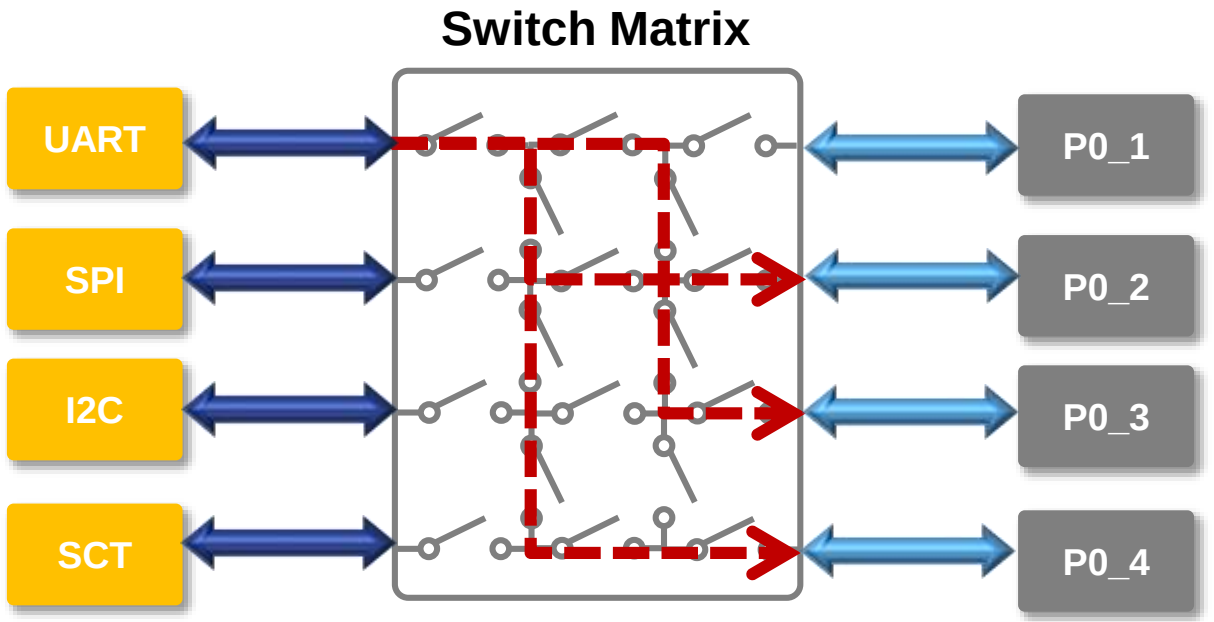
- **Support high frequency I/O toggling** – as fast as CPU_Clock/2= 15MHz!

- This scope trace shows the single cycle IO port access allowing 15 MHz with a core clock of 30 MHz



Switch Matrix

- **Movable functions**
  - Can be assigned to any external pin that is not power or ground
  - UART, SPI, I²C, SCT, comparator output, CLKOUT, pattern match output, and Ctimer
- **Fixed pin functions**
  - Oscillator pins, comparator input, GPIOs
  - Can be replaced by movable functions



07.

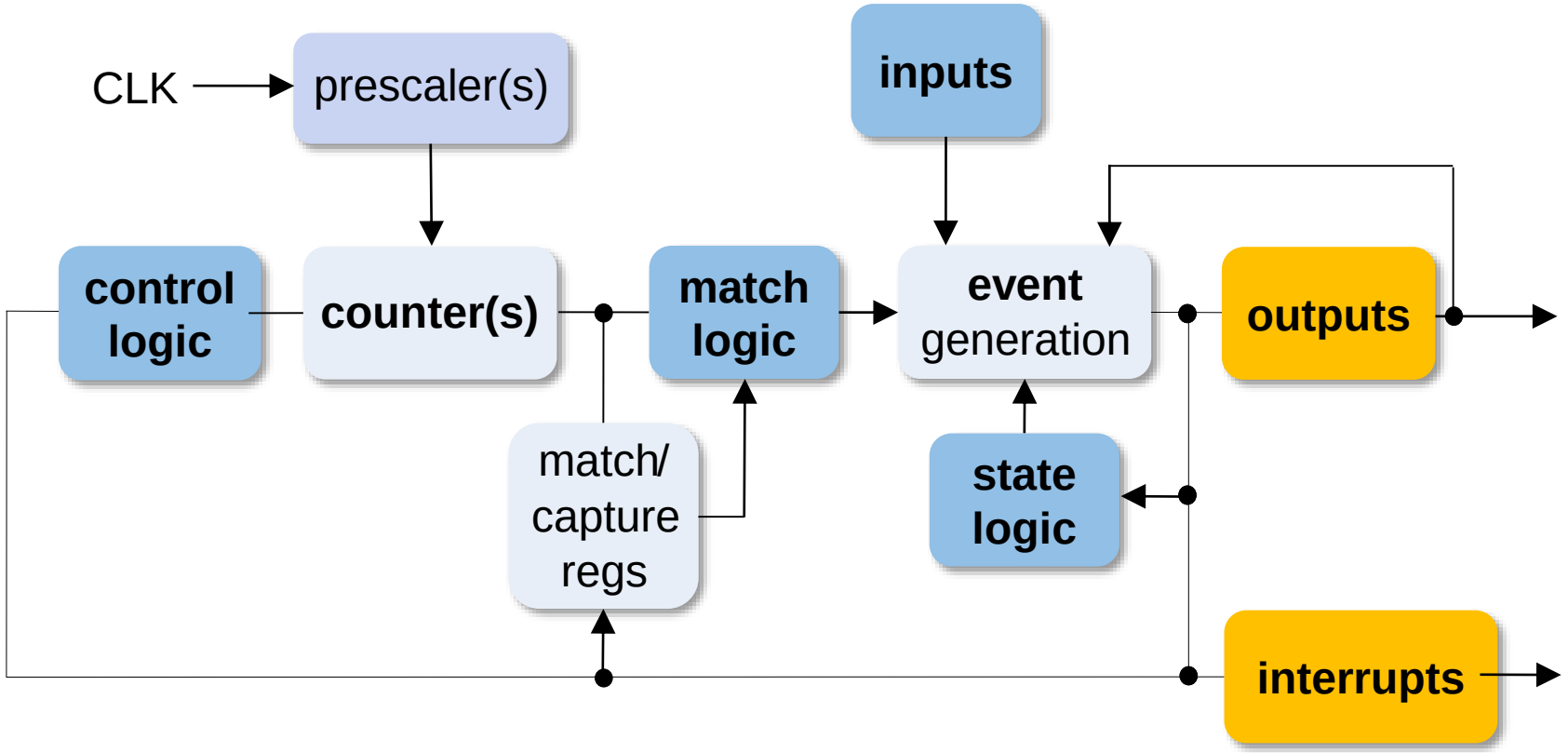
LPC84x PERIPHERALS

Timers

- Standard 32-bit Timer
- Multi-Rate timer (MRT)
  - Timer with four independent channels
  - Each channel can generate interrupts
    - Repeat interrupt mode
    - One-shot interrupt mode
- Self wake-up timer (WKT)
  - A non-zero value in this 32-bit timer initiates a countdown sequence. Wake-up source from low-power modes
- Windowed watchdog timer (24-bit timer)
- Systick Timer (24-bit timer)

State Configurable Timer/PWM (SCTimer/PWM)

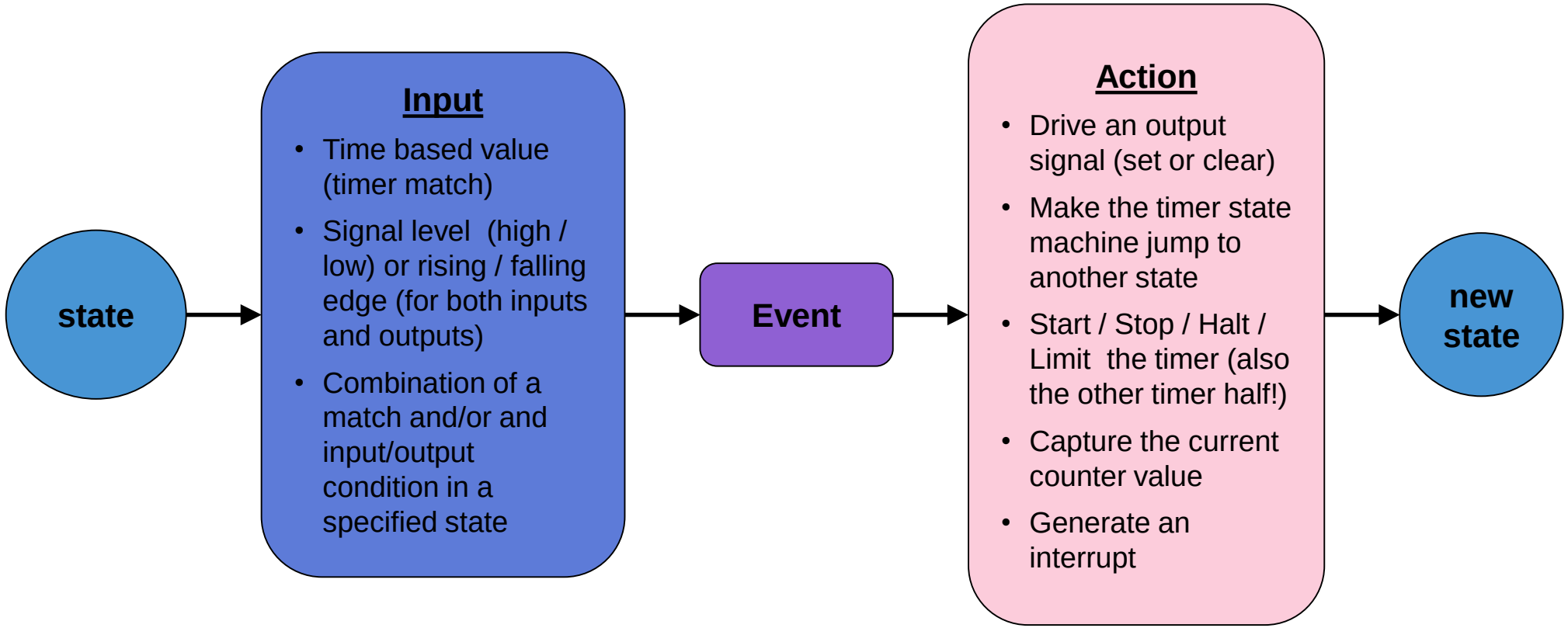
- State Configurable Timer/PWM (SCTimer/PWM) is a timer/capture unit coupled with a highly flexible event driven state machine block.
- Can be configured as 32-bit counter or two 16-bit counters with a configurable state machine



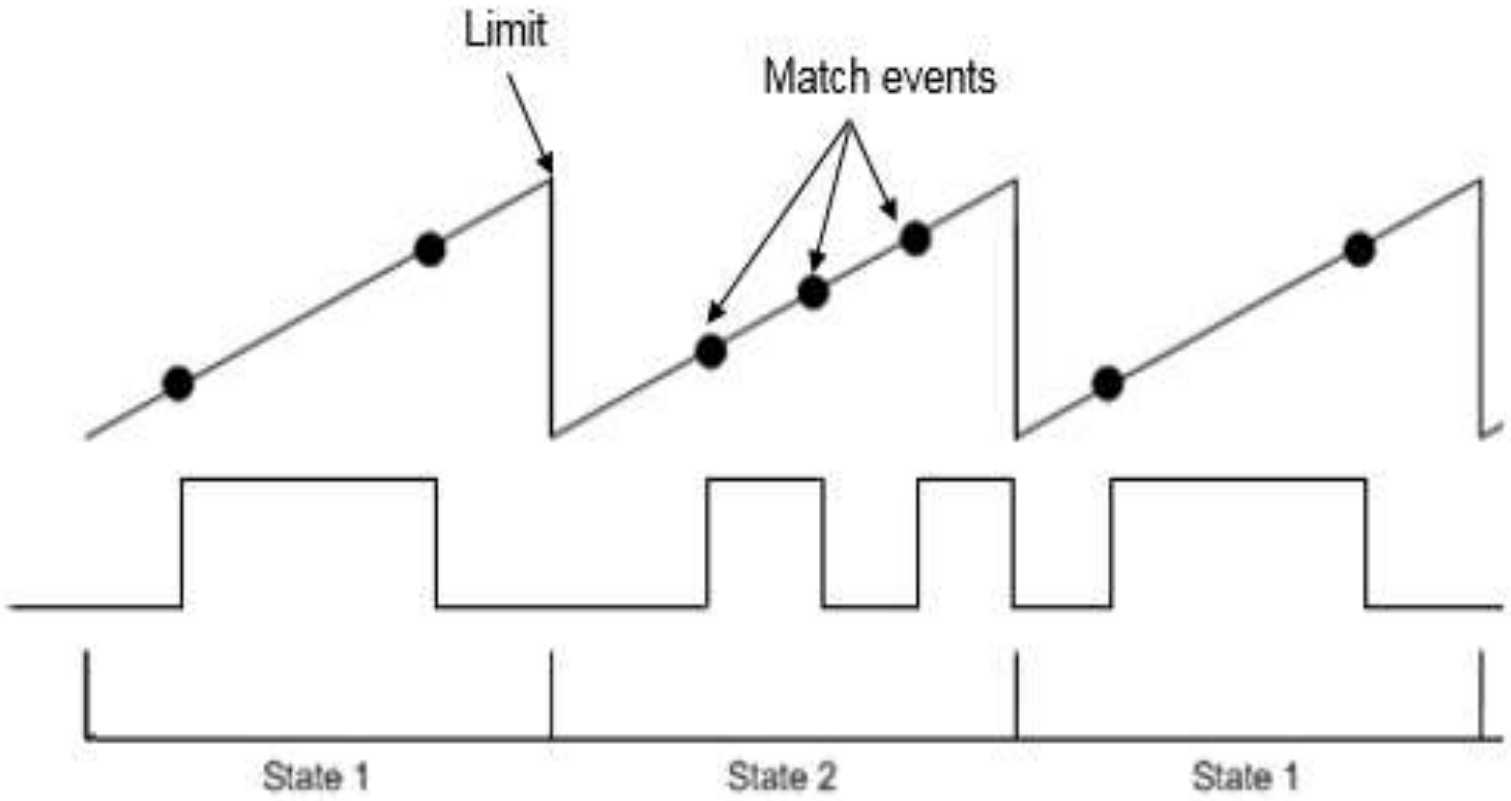
State Configurable Timer/PWM (SCTimer/PWM)

- Allows a wide variety of timing, counting, output modulation, and input capture operations
- Key Features:
  - 4 inputs
  - 4 outputs
  - 5 match/capture registers
  - 6 events with state machine support
  - 2 states

How Does the SCT Work?



SCTimer/PWM – Examples



2-channel PWM with Dead-time Control Using SCT

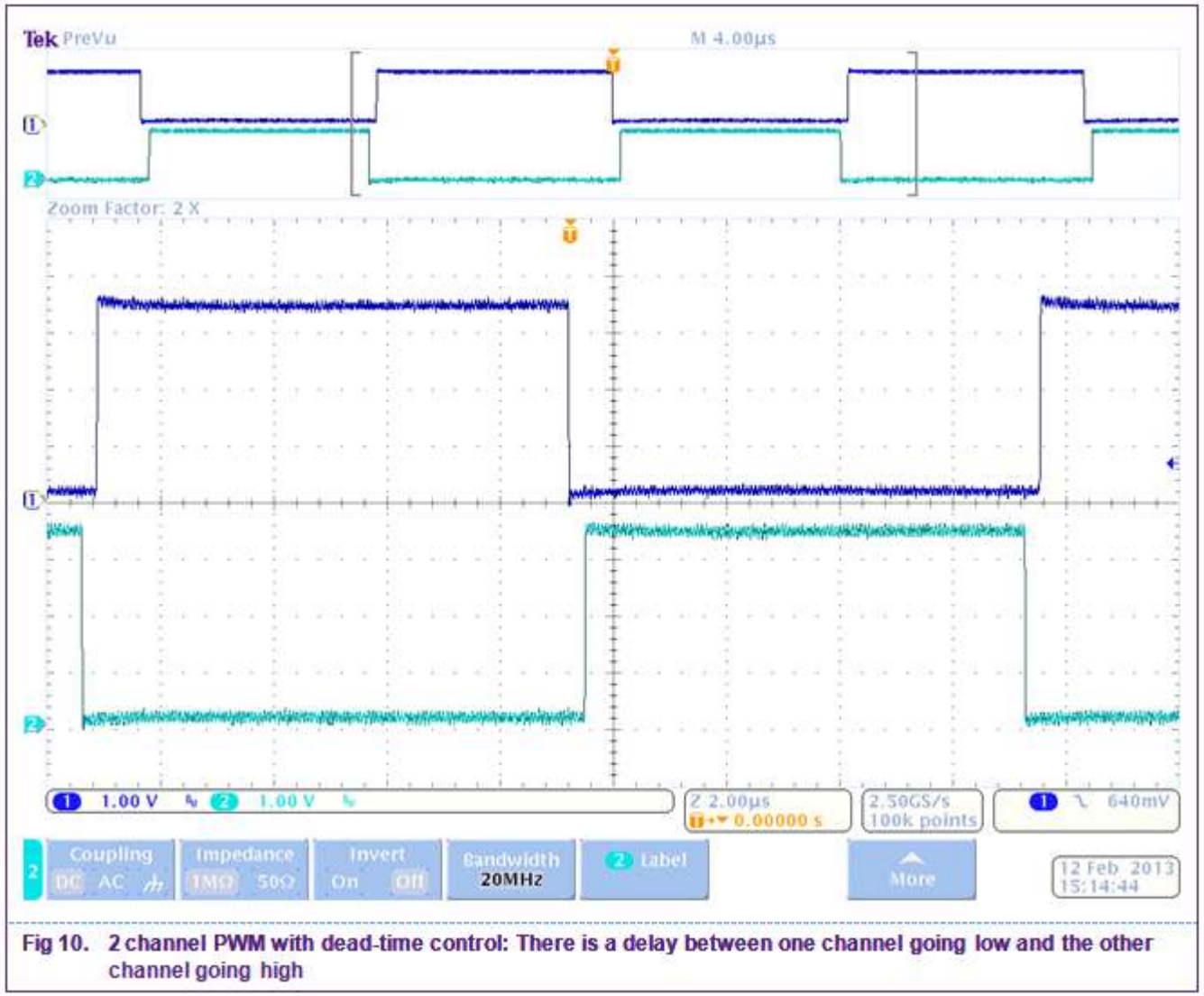


Fig 10. 2 channel PWM with dead-time control: There is a delay between one channel going low and the other channel going high

State Configurable Timer/PWM (SCTimer/PWM)

- Implements virtually any timing or PWM function found on popular 8-bit MCUs without loading the CPU
  - Wide variety of counting, output, input, and control operations
  - Dead time insertion
  - High resolution PWMs

Motor Control PWM
Generating PWM outputs with programmable dead-time

Lighting
Modulated PWM outputs, reaction to lamp sensor

Custom sampling of input signals for:
- Frequency detection
- Pulse width detection
- Phase detection

Custom control signals in hardware:
- Clock or signal gating
- Complex modulation of outputs
- Pulse sequences

SCTimer/PWM Cookbook

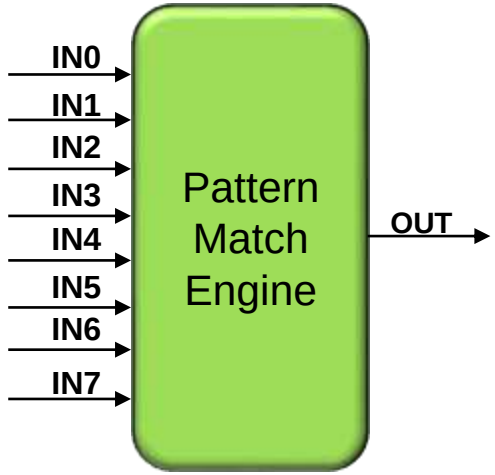
- Collection of code examples (both LPCXpresso and Keil)
- Each code example summarized in Cookbook document
- Available so far (and more to follow):
  - SCT_blinky_irq : generate 10 msec timer tick
  - SCT_blinky_match : toggle output every 10 msec
  - SCT_match_toggle : same using conflict resolution
  - SCT_pwm : generate PWM output
  - SCT_pwm_um : PWM with two different duty cycles
  - SCT_pwm_deadtime : PWM and dead time generation (for HB control)
  - SCT_pwm_4ch : 4 channel PWM + abort input
  - SCT_pwm_decode : pulse width measurement
  - SCT_rc5_send : modulate RC5 code at 36 kHz carrier
  - SCT_rc5_receive : decode RC5 frame (Manchester coding)

Pattern Match Engine (PME)

- Pin Interrupt generator
  - Up to 8 pins can be selected to generate interrupts to the core
- Pattern match feature
  - The same 8 pins (above) can be selected from all GPIO pins to contribute to a Boolean expression
- Example:

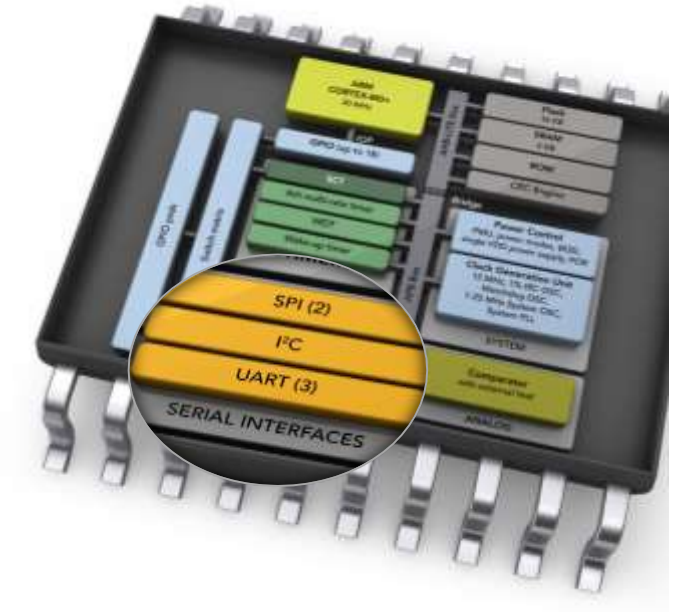
```
(IN0)~(IN1)(IN3)^+(IN4)(IN5)+(IN0)~(IN3)~(IN4)

  where: ~=low; ^=rising edge; +=OR
```

  - The PME keeps polling these pins and generates an interrupt to the core when one or more of the bit slices match
- Both the pin interrupt and pattern match blocks are mutually exclusive



USART/I²C/SPI

- USART
  - Synchronous operations on all 5 UARTs
  - Maximum bit rates of 1.875 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous mode for USART functions
  - Fractional rate divider is shared among all USARTs
  - Built-in baud rate generator
- I²C
  - 4 I²C
  - Fast-mode Plus (up to 1Mbit/s) capability on the open-drain pins
- SPI
  - 2 SPI
  - Maximum data rate of 30 Mbit/s in master and 25 Mbit/s in slave
- Wake from sleep, deep-sleep, or power-down mode

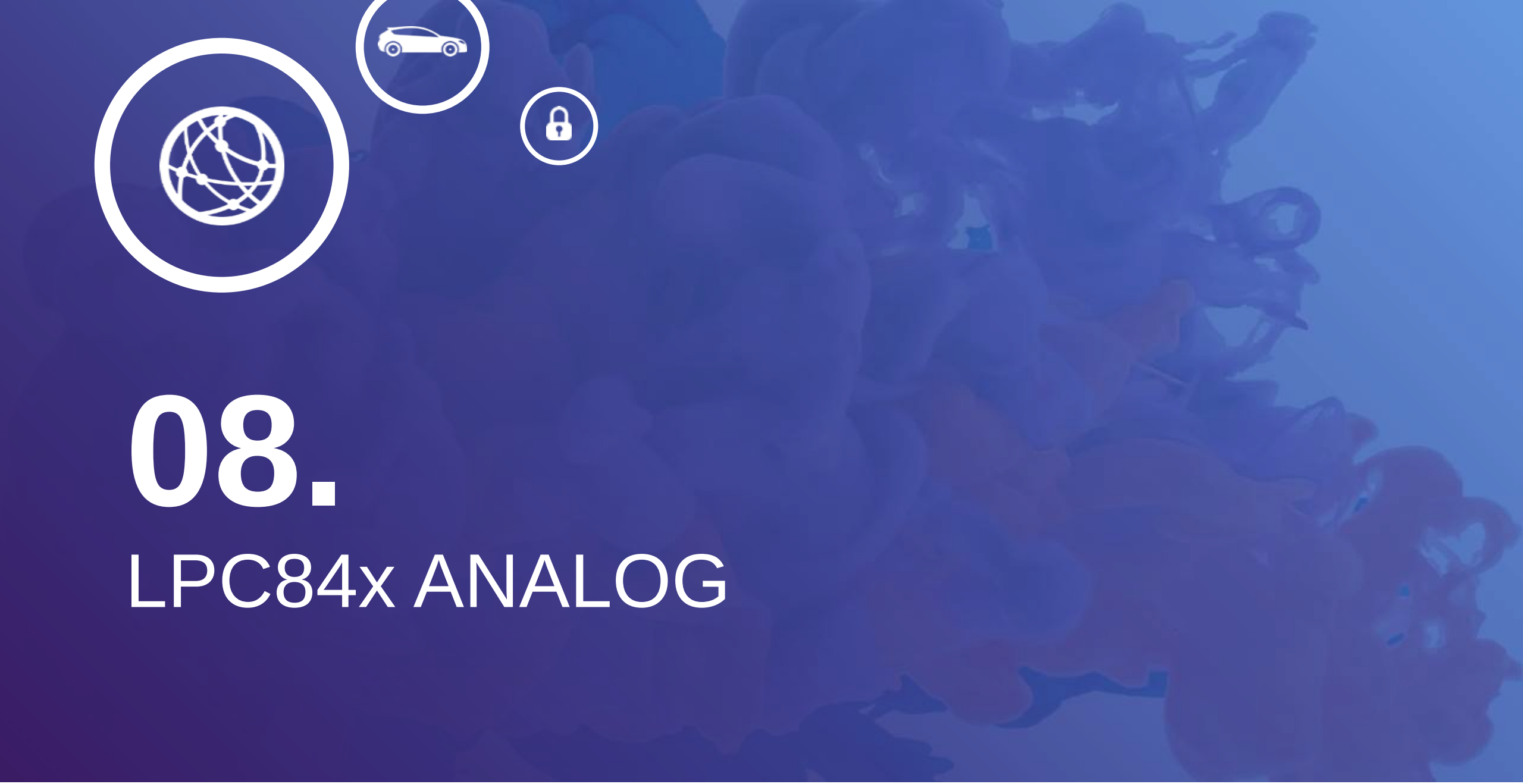


DMA

- 25 channel DMA: all connected to peripheral request inputs and outputs
  - 25 sources from USART, SPI, I2C, and DAC peripherals
  - SCT request 0&1, ADC sequence A&B, ACMP, pin interrupt 0&1, CTimer32 match
- Supports single transfers up to 1024 words
- Operates in sleep mode
- Priority is user selectable for each channel
- Continuous priority arbitration
- Address cache with four entries
- Address increment options allow packing and/or unpacking data

Cyclic Redundancy Check (CRC) Engine

- Supports three common polynomials CRC-CCITT, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Accept any size of data width per write: 8-, 16- or 32-bit
  - 8-bit write: 1-cycle operation
  - 16-bit write: 2-cycle operation (8-bit x 2-cycle)
  - 32-bit write: 4-cycle operation (8-bit x 4-cycle)

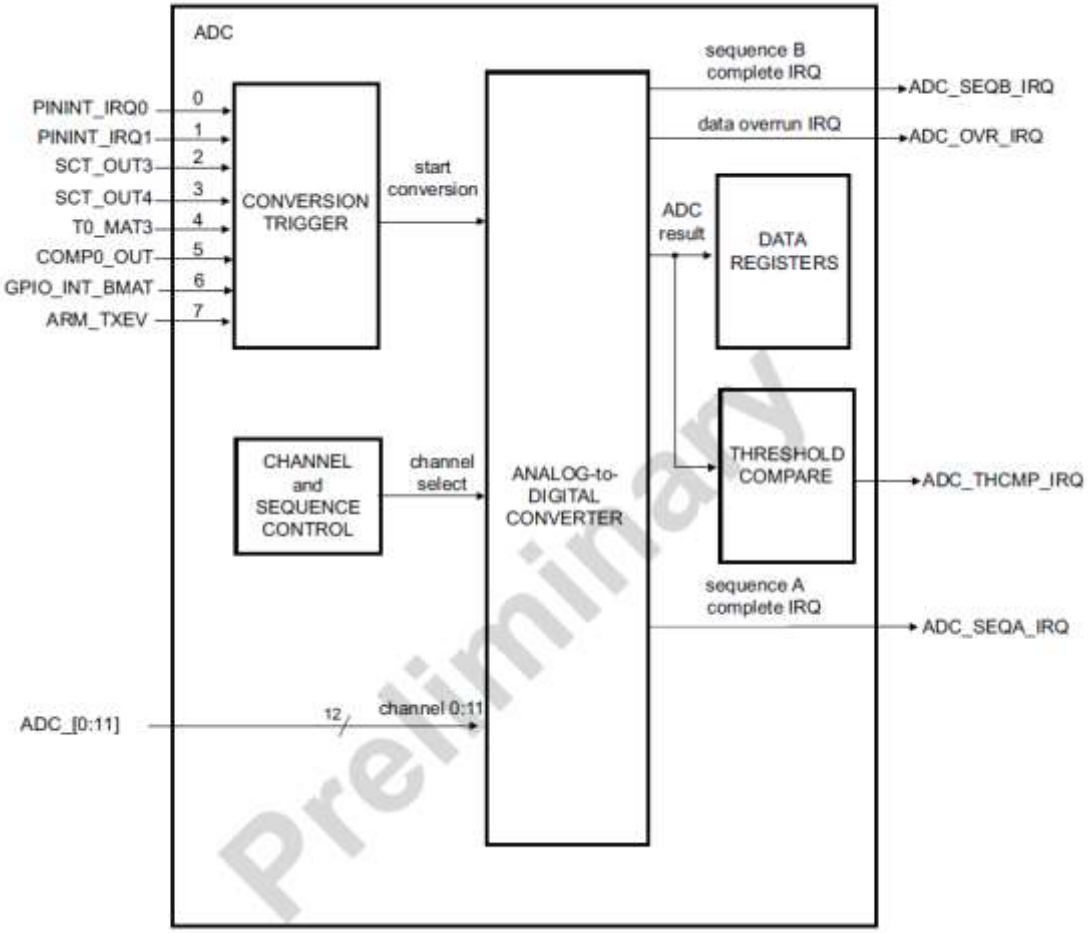


08.

LPC84x ANALOG

Analog to Digital Converter

- 12-bit successive approximation
- Input multiplexing among 12 pins
- 12-bit conversion rate up to 1.2 Msps
- Two configurable conversion sequences with independent triggers
- Optional automatic high/low threshold comparison and “zero crossing” detection
- Power down mode and low-power operating mode
- Burst conversion mode for single and multiple inputs
- DMA support

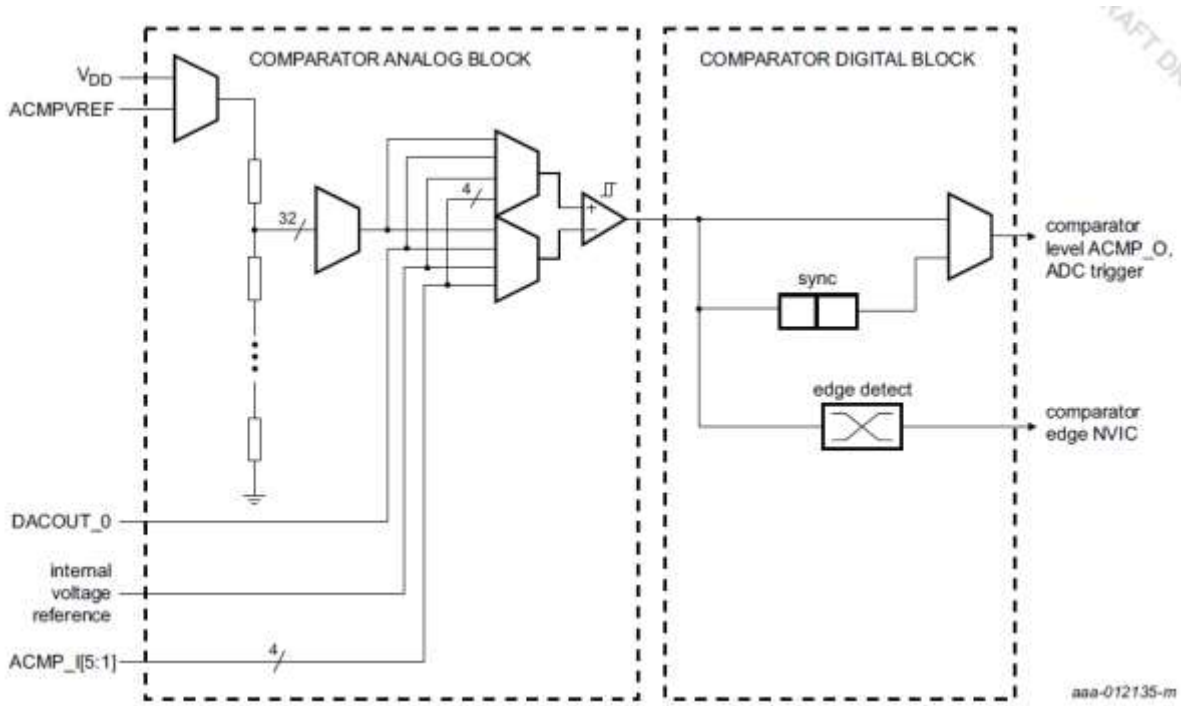


DAC Feature

- 2 10-bit digital to analog converters
- Resistor string architecture
- Buffered output
- Power-down mode
- Selectable speed vs. power
- Maximum update rate of 1 MHz
- Support DMA

Analog Comparator

- Compares voltage levels on external pins and internal voltages
- 5 inputs are multiplexed separately to the positive voltage input and negative inputs
- The Internal voltage reference (0.9 V bandgap reference) and DACOUT can be used as either the positive or negative input of the comparator
- Voltage ladder source selectable between the supply pin VDD or ACMPVREF pin
- 32 levels of Comparator reference voltage for fine grain comparison
- Edge and level Comparator output signals connected to State Configurable Timer (SCT) using the Switch matrix, allows for the recording of event comparison – “timestamps”



09.

LPC84x LOW POWER MODES

LPC84x Low Power Modes

Low Power Mode	Impact	Wake-Up Sources	Current Consumption
Sleep	System Clock to Cortex-M0+ is stopped. Peripherals and memories are active. Processor state and registers, peripheral registers, and internal SRAM are maintained, and the logic levels of the pins remain static	Any peripherals interrupts (SCT, MRT, USART, SPI, I2C, CMP, Capacitive Touch) Pin interrupts & Pattern Match Engine BOD interrupt and reset WWDT interrupt and reset External Reset Self Wake-up Timer	1.3 mA
Deep Sleep	Peripherals receive no internal clocks. Flash is in stand-by mode. Peripherals and memories are active. Processor state/registers, peripheral registers, and internal SRAM contents are maintained, and the logic levels of the pins remain static	Interrupts from USART, SPI, I2C Interrupt from Capacitive Touch Pin interrupts BOD interrupt and reset WWDT interrupt and reset External Reset Self Wake-up Timer	240 µA
Power-Down	Peripherals receive no internal clocks. The flash memory is powered down. Processor state/registers, peripheral registers, and internal SRAM contents are maintained, and the logic levels of the pins remain static	Interrupts from USART, SPI, I2C) Pin interrupts BOD interrupt and reset WWDT interrupt and reset External Reset Self Wake-up Timer	1.5 µA
Deep Power-Down	The entire system is shut down except for four 32-bit general purpose registers in the PMU and the self wake-up timer. Register states and internal SRAM contents are lost	Wake up on a pulse on the WAKEUP pin, RESET pin, or when the self wake-up timer times out. On wake-up, the part reboots.	400 nA

10.
LPC800 DEBUG MODULE

Emulation and Debugging

- Debug and trace functions are integrated into the ARM Cortex-M0+
- Serial wire debug (SWD: 2 pins)
- Supports up to four breakpoints and two watchpoints
- Micro Trace Buffer (MTB) supported
- Standard JTAG pins (5 pins) supports ONLY boundary scan testing

11. LPC84x SOFTWARE, TOOLS AND SUPPORT

Software for the LPC8xx

- LPCOpen API software platform available for LPC81x/LPC82x. and LPC83x
  - LPCOpen provides the ease of use without diving into details of each peripheral registers, and it is easy to migrate from LPC8xx to LPC11xx family.
- Example Code Bundles (register level) available for entire LPC800 family
  - Fastest, and simplest way for user to learn how to program each peripheral before progressing to more advance features of the peripheral.
  - New users of LPC800 can step through the Example Code like a tutorial.
  - Concise and accurate explanations in Readme files and comments in source files help the user to start/debug quickly.
  - Work right out of the box for the LPC800 LPCXpresso-MAX boards and easy to read how the peripherals registers are setup /access without going through many levels of APIs.
  - Register level peripheral access, and direct correspondence between software and memory maps in the chip User Manuals.
  - Example Code Project and source code directory structures are kept simple, flat, and consistent (as much as possible) between LPCXpresso/MCUXpresso IDE, Keil, and IAR tools.
- System base on Example Code is smaller in code size, with much simpler code vs LPCOpen for a similar task
  - >25% code size reduction for a simple Blinky. This can be crucial in applications where the code size is close to the device flash limit.
- No SDK support for the LPC800

LPCXpresso845MAX Board (OM13097)

- LPC845 in LQFP64 package
- On-board CMSIS-DAP debug interface
  - Supported by MCUXpresso IDE and popular 3rd party IDEs
  - Includes VCOM support (UART bridged via USB to host)
- Expansion options
  - Arduino UNO R3-compatible connectors
  - LPCXpresso and Pmod® options
  - Prototyping area
- User application test features
  - Red, Green and Blue user LEDs for test & debug
  - On board speaker with driver
  - User button
  - Easily configured for LPC845 power measurement
- USB powered
- UART, SPI, I2C ISP boot-capable

Orderable Part Number: ***OM13097UL***
http://www.nxp.com/demoboard/OM13097

✓ **NXP Software Code Bundle**

✓ **Free MCUXpresso IDE & 3rd Party Options**

NXP IDE · IAR SYSTEMS · KEIL Tools by ARM · ARM mbed *Coming soon

Support

- NXP Community Site

https://community.nxp.com/community/lpc

- Training and Events

http://www.nxp.com/support/training-events:TRAINING-EVENTS

12.

LPC84x SUMMARY

LPC84x Summary

- Simplicity
- High performance at a low price point
- 2-10x higher performance than 8-/16-bit MCUs
- 2-3x power saving compared to 8-/16-bit MCUs
- 40-50% smaller code size than 8-/16-bit MCUs
- Single cycle IO access
- Easy to use and flexible peripherals: SCTimer/PWM, Multi Rate Timer, Switch Matrix, USART, I2C, SPI, Cap Touch
- FAIM
- Code bundle software examples

Software, Professional Support & Services

Complimentary Software & Tools

- Kinetis Design Studio, Software Development Kit, Pin Config, Power Estimator/Analyzer
- THREAD, BLE, ZigBee, Bootloader, RTOS
- Linux & Android BSP…

Professional Services

- Managing Skills Gaps & Engineering Capacity
- Global Staffing Capability
- Vested Interest in Mutual Success
- Graphic, Security, Linux/Android, Cloud, Connectivity

Complimentary Support

- NXP Boards
- Communities
- Technical Information Center
- Customer Application & Technical Support
- Distributor technical support

Hardware Services

- 1st Time Boot
- Schematics & Layout Review

Software Products / Technology

- AVB, Miracast, HDCP2.x, TRLE, TEE, Home Kit, CarPlay, Android Auto, MICROEJ, Sensor Fusion, AUTOSAR, Connected Audio Solution, Graphic Tools, VisionECG, GPU Driver, AGL, Genivi, XBMC, HAB

Professional Support

- Risk Reduction
- Fast Answers
- Hot Fixes

SECURE CONNECTIONS
FOR A SMARTER WORLD