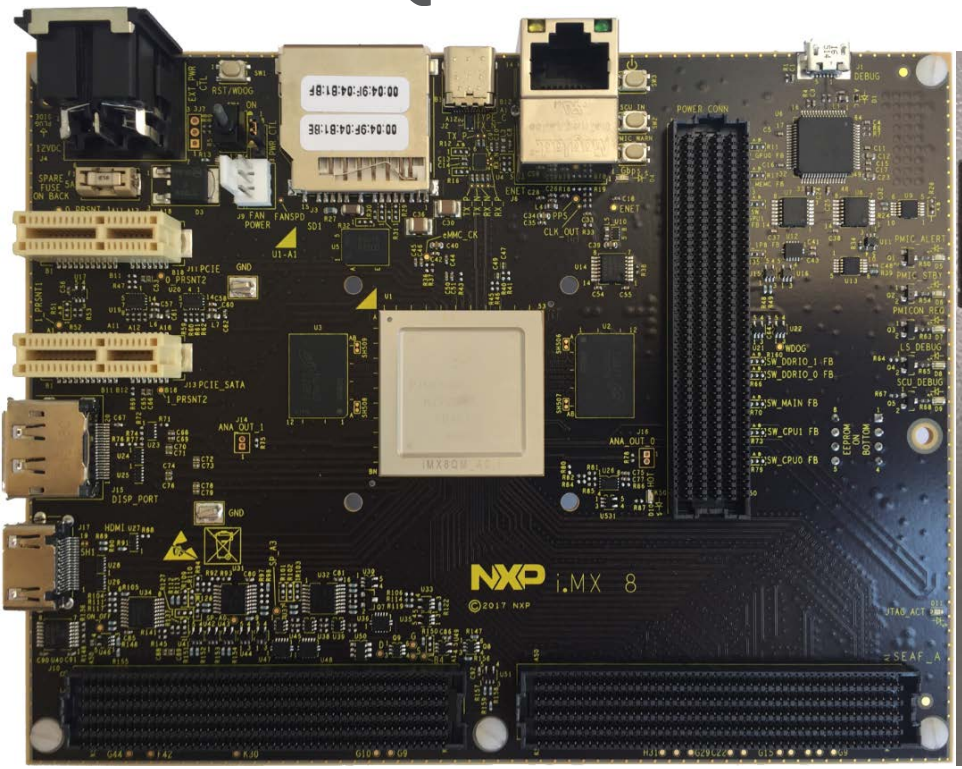
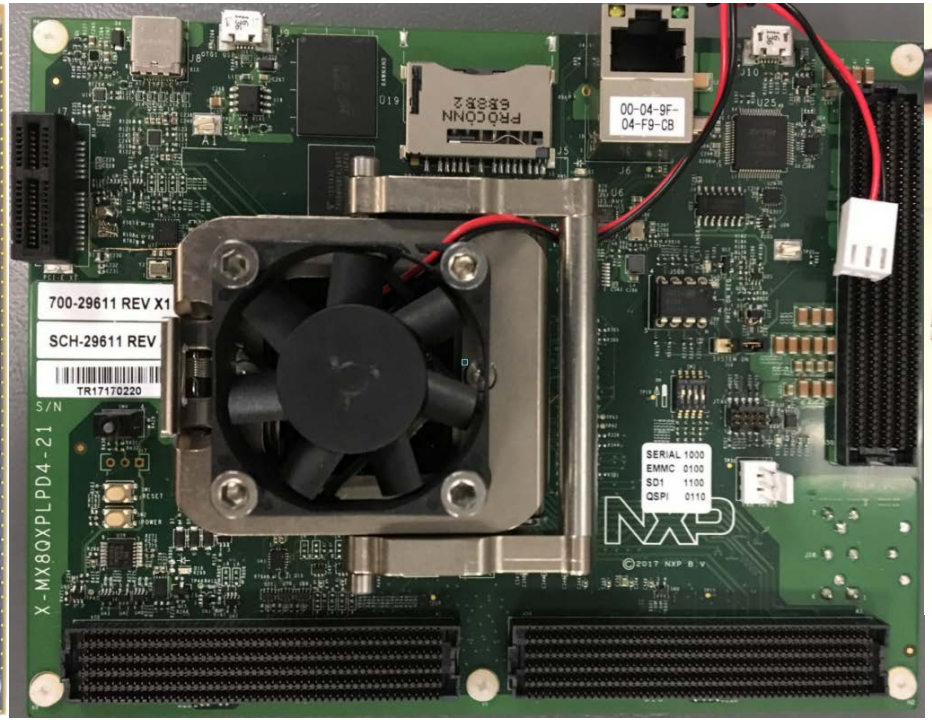
New Memory Choices for the New i.MX8 Processors

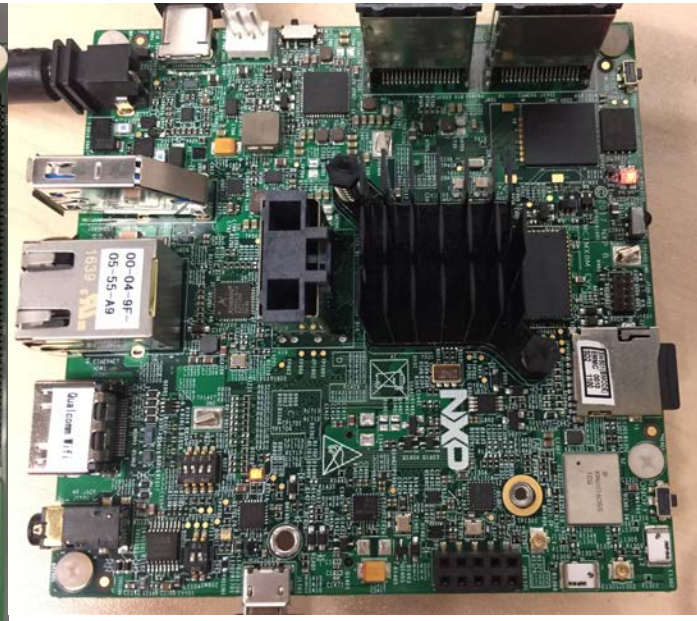
i.MX8 Quad Max



i.MX8 Quad X Plus



i.MX8 M



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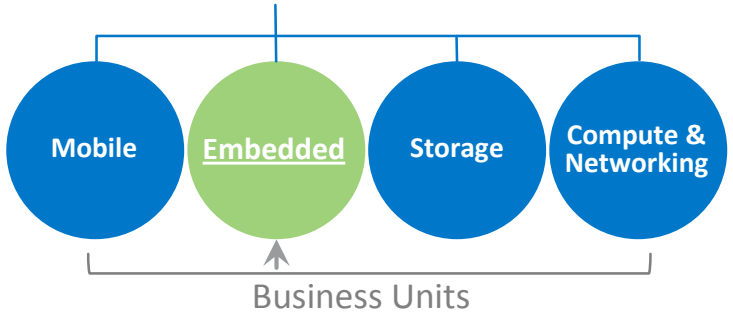
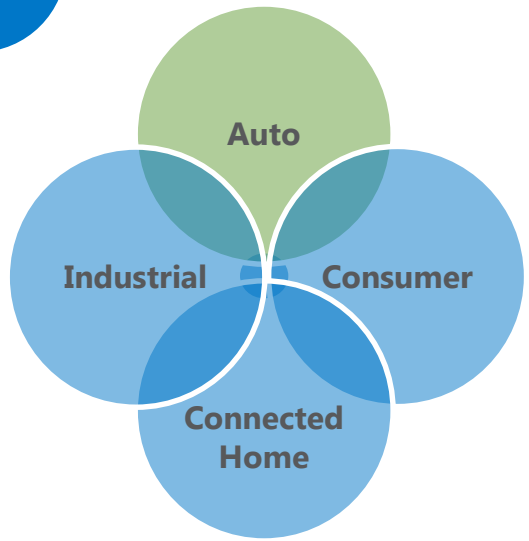
Abstract:

- We will discuss the new memories supported on the latest i.MX8 processors.
- NXP's latest and most powerful Microprocessor requires the latest and fastest memories to keep it running efficiently. As a system designer, your memory choices can impact the performance, size, cost, power reliability and longevity of your end product.
- During this session, we will discuss the new memories supported on the new i.MX8 processor family. For DRAM, this will include DDR4 and Low Power DDR4 (LPDDR4). For non-volatile memory this will include Octal SPI NOR (Xccela™ Flash) which offers up to 400MB/s as well as the latest eMMC 5.X devices that also support high speeds. These devices are offered with Commercial, Industrial or Automotive temperature and quality ratings.
- This year, we will provide additional information on LPDDR4X (X=lower power I/O) as well as eMMC 5.1 high performance features including command queueing, and several new Cache operations.
- This session will provide designers with the tools necessary to create state-of-the-art i.MX8 systems.

Micron's Segment / Product Focus



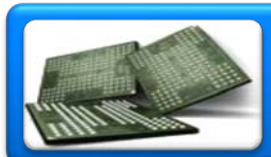


NOR Flash:

- Parallel NOR
- Serial (Q-SPI, Twin Quad, **Xccela™ Octal SPI**)

DRAM:

- SDR/DDR (DDR2, 3, 4)
- LPSDR/LPDDR (LPDDR2, **LPDDR4**)

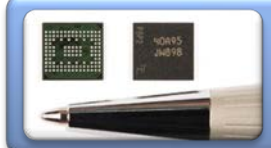


NAND Flash:

- SLC NAND / MLC NAND

eMMC™: 4.5, 5.0, 5.1

SSD: SATA, PCIe/NVMe



MCP

Compatibility Guides

https://www.micron.com/solutions/micron-valued-partner-program/chipset-partner/nxp

Compatibility Guides (Pages 1 & 2 of 8)

Micron® Memory Support for NXP® i.MX8 Platforms

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Micron Memory		i.MX Processor Memory		
		i.MX 8 Quad Max, i.MX8 Quad Plus, i.MX8 Quad	i.MX8 Quad X Plus, i.MX8 Dual X Plus, i.MX8 Dual X	i.MX8 M Quad / Quad Lite i.MX8 M Dual / Dual Lite
DRAM	Type	LPDDR4	LPDDR4	LPDDR4
	Family	MT53B	MT53B	MT53D
	Density	24Gb	24Gb	24Gb
	Configuration	384 Meg x 32	384 Meg x 32	384 Meg x 32
	Package	200-ball FBGA	200-ball FBGA	200-ball FBGA
	Validated PN	MT53D1024M32D4NQ-046 AAT:D	MT53D1024M32D4NQ-046 AAT:D	MT53D1024M32D4NQ-046 AAT:D
	Qty/Board	2	1	1
NAND/e.MMC	Type	e.MMC (5.0)	e.MMC (5.0)	e.MMC (5.0)
	Family	MTFC	MTFC	MTFC
	Density	32GB	32GB	16GB
	Package	153-ball VFBGA	153-ball VFBGA	153-ball VFBGA
	Validated PN	MTFC32GAKAEEF-AIT	MTFC32GAKAEEF-AIT	MTFC16GAKAECN-2M WT
NOR	Type	Xccela™ Flash (Octal SPI), Serial (Quad SPI)	Xccela™ Flash (Octal SPI), Serial (Quad SPI)	Quad SPI
	Family	MT35X, MT25T, MT25Q	MT35X, MT25T, MT25Q	MT25Q
	Density	512Mb	512Mb	256Mb
	Package	25-ball BGA (8mm x 6mm)	25-ball BGA (8mm x 6mm)	24-ball BGA (8mm x 6mm)
	Validated PN	MT35XU512ABA1G12-0AAT	MT35XU512ABA1G12-0AAT	MT25Q256ABA1EW9-0SIT

*MT41K family supports both 1.5V and 1.35V power supply and is backward compatible with MT41J family.

Micron® Memory Support for NXP® i.MX6 Platforms

Save yourself time and money—Micron memory comes ***validated*** on NXP Platforms

Micron Memory		i.MX Processor Memory					
		i.MX 6Quad/i.MX 6Dual/DualLite/Solo i.MX 6QuadPlus/i.MX 6DualPlus			i.MX 6SoloLite		i.MX 6SoloX
		SABRE for Automotive Infotainment	SABRE Platform for Smart Devices	Quick Start Board	Evaluation Kit	WaRP (Wearable Reference Design)	SABRE SDB
DRAM	Type	DDR3	DDR3	DDR3	LPDDR2	eMCP (LPDDR2 with e.MMC)	DDR3
	Family	MT41K*	MT41K*	MT41K*	MT42L	MT29P**	MT41K*
	Density	4Gb	2Gb	2Gb	8Gb	4Gb	4Gb
	Configuration	256 Meg x 16	128 Meg x 16	128 Meg x 16	256 Meg x 32	256 Meg X 16	256 Meg x 16
	Package	96-ball FBGA	96-ball FBGA	96-ball FBGA	168-ball VFBGA	162-ball VFBGA	96-ball FBGA
	Validated PN	MT41J256M16RE	MT41J128M16HA	MT41J128M16HA	MT42L256M32D2LG	MT29PZZZ4D4BKESK	MT41K256M16HA-125:E
	Qty/Board	4	4	4	1	1	2
NAND/e.MMC	Type	Raw	e.MMC	e.MMC	e.MMC	eMCP (LPDDR2 with e.MMC)	e.MMC
	Family	MT29F/MTFC	MTFC	MTFC	MTFC	MT29P**	MTFC
	Density	64Gb	8GB	8GB	8GB	4GB	8GB
	Package	48-pin TSOP	169-ball FBGA	169-ball FBGA	169-ball FBGA	162-ball VFBGA	153-ball TFBGA
	Validated PN	MT29F64G08AFAAA				MT29PZZZ4D4BKESK	MTFC8GLCDM
NOR	Type	Serial (Quad SPI)	Serial (Quad SPI)		Serial (Quad SPI)		Serial (Quad SPI)
	Family	MT25Q	MT25Q		MT25Q		MT25Q
	Density	32Mb	32Mb		32Mb		256Mb
	Package	SO8W	SO8W		SO8W		SO8W

*MT41K family supports both 1.5V and 1.35V power supply and is backward-compatible with MT41J family.
**Micron's MT29PZZZ4D4BKESK is a multichip package that integrates a 4Gb LPDDR2 and a 4GB e.MMC v4.51 in a single package.

Compatibility Guides (Pages 3 & 4 of 8)

Micron® Memory Support for NXP® i.MX6 Platforms

Save yourself time and money—Micron memory comes *validated* on NXP Platforms

Micron Memory		i.MX Processor Memory					
		i.MX 6Quad/i.MX 6Dual/DualLite/Solo i.MX 6QuadPlus/i.MX 6DualPlus			i.MX 6SoloLite		i.MX 6SoloX
		SABRE for Automotive Infotainment	SABRE Platform for Smart Devices	Quick Start Board	Evaluation Kit	WaRP (Wearable Reference Design)	SABRE SDB
DRAM	Type	DDR3	DDR3	DDR3	LPDDR2	eMCP (LPDDR2 with e.MMC)	DDR3
	Family	MT41K*	MT41K*	MT41K*	MT42L	MT29P**	MT41K*
	Density	4Gb	2Gb	2Gb	8Gb	4Gb	4Gb
	Configuration	256 Meg x 16	128 Meg x 16	128 Meg x 16	256 Meg x 32	256 Meg X 16	256 Meg x 16
	Package	96-ball FBGA	96-ball FBGA	96-ball FBGA	168-ball VFBGA	162-ball VFBGA	96-ball FBGA
	Validated PN	MT41J256M16RE	MT41J128M16HA	MT41J128M16HA	MT42L256M32D2LG	MT29PZZZ4D4BKESK	MT41K256M16HA-125 E
	Qty/Board	4	4	4	1	1	2
NAND/e.MMC	Type	Raw	e.MMC	e.MMC	e.MMC	eMCP (LPDDR2 with e.MMC)	e.MMC
	Family	MT29F/MTFC	MTFC	MTFC	MTFC	MT29P**	MTFC
	Density	64Gb	8GB	8GB	8GB	4GB	8GB
	Package	48-pin TSOP	169-ball FBGA	169-ball FBGA	169-ball FBGA	162-ball VFBGA	153-ball TFBGA
	Validated PN	MT29F64G08AFAAA				MT29PZZZ4D4BKESK	MTFC8GLCDM
NOR	Type	Serial (Quad SPI)	Serial (Quad SPI)		Serial (Quad SPI)		Serial (Quad SPI)
	Family	MT25Q	MT25Q		MT25Q		MT25Q
	Density	32Mb	32Mb		32Mb		256Mb
	Package	SO8W	SO8W		SO8W		SO8W

*MTFC family supports both 1.8V and 3.3V power supply and is backward compatible with MTAO family.
**Micron's MT29PZZZ4D4BKESK is a multichip package that integrates 4Gb LPDDR2 and a 4Gb e.MMC v4.51 in a single package.

Micron® Memory Support for NXP® i.MX7 Platforms

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Micron Memory		i.MX Processor Memory				
		i.MX 7				i.MX7 ULP
		SABRE for Smart Devices		Validation Platform		
DRAM	Type	DDR3L		LPDDR3		LPDDR3
	Family	MT41K*		EDFA		MT52L
	Density	4Gb		16Gb		16Gb
	Configuration	256 Meg x 16		512 Meg x 32 (2 rank)		512 Meg x 32
	Package	96-ball VFBGA		168-ball PoP (soldered on board)		168-ball PoP (soldered on PCB)
	Validated PN	MT41K256M16HA		EDFA232A2PF-GD-F-D		MT52L512M32D2PU-107 WT:B
	Qty/Board	2		2		1
NAND/e.MMC	Type	e.MMC	MLC NAND	e.MMC	SLC NAND	e.MMC (5.0)
	Family	MTFC	MT29F	MTFC	MT29F	MTFC
	Density	8GB	32Gb	8GB	32Gb	32GB
	Package	153-ball WFBGA	48-pin TSOP	153-ball WFBGA	48-pin TSOP	153-ball VFBGA
	Validated PN	MTFC8GACAEAM-1M WT	MT29F32G08CBADB	MTFC8GACAEAM-1M WT	MT29F32G08ABCDB14	MTFC8GAKAJCN-1M WT
NOR	Type	Serial (Quad SPI)		Serial (Quad SPI)	Serial (Twin Quad)	Xccela™ Flash (Octal SPI), Serial (Quad SPI)
	Family	MT25Q		MT25Q	MT25TL	MT35X, MT25T, MT25Q
	Density	256Mb		256Mb	512Mb	512Mb
	Package	SO8W		SO8W	SO16	25b BGA
	Validated PN				M25TL512HAA1ESF0AAT	MT35XU512ABA1G12-0SITES

*MTFC family supports both 1.8V and 3.3V power supply and is backward compatible with MTAO family.

Compatibility Guides (Pages 5 & 6 of 8)

Micron® Memory Support for NXP® Platforms

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Micron Memory			Kinetis K Family Processors								
			K30	K70	K60	K50	K40	K30	K20	K10	E,L,M,W
DRAM	Type	DDR									
	Family	MT46V									
	Density	256Mb–1Gb		✔	✔						
	Configuration	x4, x8, x16									
	Package	TSOP, FBGA									
NAND	Type	Raw (host ECC required)									
	Family	MT29F									
	Density	128Mb–512Gb		✔	✔				✔		
	Package	48-pin TSOP									
NOR	Type	Serial									
	Family	MT25Q									
	Density	8Mb–1Gb		✔	✔	✔	✔	✔	✔	✔	✔
	Package	Many									
Xccela™ Flash	Type	Octal SPI NOR									
	Family	MT35X									
	Density	256Mb–2Gb	✔								
	Package	24-ball TFBGA									

✔ Indicates the interface is compatible with the memory device.

Micron Memory		i.MX RT Series	
		i.MX RT 10xx	
DRAM	Type	SDR/M	
	Family	MT48LC	
	Density	256Mb	
	Configuration	16M x 16	
	Package	54-ball FBGA	
	Validated PN	MT48LC16M16A2B4-6A IT:G	
	Quantity/board	1	
NAND/ e.MMC	Type	SPI NAND	e.MMC (5.0/4.5 usage)
	Family	MT29F	MTFC
	Density	1GB	8GB
	Package	24-ball TFBGA	153-ball VFBGA 11.5x13x1mm
	Validated PN	MT29F1G01ABAFD12-ITF	MTFC8GAKAJCN-1M WT
Quad-SPI/ Parallel NOR	Type	Quad SPI	Parallel
	Family	MT25Q	MT28EW
	Density	128Mb	128Mb
	Package	W-PDFN-8	64-ball LBGA
	Validated PN	MT25QL128ABA1ESE-0SIT	MT28EW128ABA1LPC-0SIT
Xccela™ Flash	Type	Octal SPI NOR	
	Family	MT35X	
	Density	256Mb-2Gb	
	Package	24-ball TFBGA 6 x 8mm	
	Validated PN	MT35XL512ABA2G SF-0SIT	

Micron Memory		Hybrid Processors			
			VF5XX	VF5XX	VF3XX
DRAM	Type	DDR3 / LPDDR2	✔ DDR3 and LPDDR2	✔ DDR3 and LPDDR2	
	Family	MT41K* / MT42L			
	Density	4Gb, 8Gb / 4Gb			
	Configuration	x4, x8, x16 / x32, x64			
	Package	78-, 96-ball / 134-, 253-ball			
NAND	Type	Raw	✔	✔	✔
	Family	MT29F			
	Density	128–512Gb			
	Package	48-pin TSOP			
NOR	Type	Serial (Quad SPI)	✔	✔	✔
	Family	MT25Q			
	Density	128Mb–2Gb			
	Package	Many			

✔ Indicates the interface is compatible with the memory device.
*MT41K family supports both 1.5V and 1.35V power supply and is backward-compatible with MT41J family.

Micron® Memory Support for NXP® Platforms

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Micron Memory		Automotive Processors	
		ADAS Vision Processor S32V234	Instrument Cluster MAC57D
DRAM	Type	LPDDR2	DDR2
	Family	MT42L	MT47H
	Density	2Gb	1Gb
	Configuration	64M x 32	64M x 16
	Package	134-ball FBGA	84-ball FBGA
	Validated PN	MT42L64M32D1TK-18 AA	MT47H64M16NF-25E
	Quantity/board	2	2
NOR	Type	Serial (Twin Quad SPI)	Serial (Quad SPI)
	Family	MT25TL	MT25Q
	Density	256-1024Mb	128-2048Mb
	Package	SOIC-16, 24-ball TFBGA	SOIC-16
	Validated PN		
Xccela™ Flash	Type	Octal SPI	Octal SPI
	Family	MT35X	MT35X
	Density	512Mb	512Mb
	Package	24-ball TFBGA	24-ball TFBGA
	Validated PN	MT35XL512ABA1G120A-0T	MT35XL512ABA1G120A-0T
NAND/e.MMC	Type	e.MMC	
	Family	MTFC	
	Density	8GB	
	Package	153-ball VFBGA	
	Validated PN	MTFC8GACAAAM-4M IT	

NXP Micron Compatibility Guides (Pages 7 & 8 of 8)

Micron® Memory Support for NXP® Networking Platforms

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Micron Memory		QorIQ Processor Memory						
		Value Tier	Mid-Range Tier			High-Performance Tier		
		P1010/P1014	P2022/P2021E	P2041/P2031	T2080/T2081	P4080X	P5020/P5040	T4240
DRAM	Type	DDR3/DDR3L	DDR3	DDR3/DDR3L	DDR3/DDR3L	DDR3	DDR3/DDR3L	DDR3/DDR4L
	Family	MT41	MT41	MT41	MT41	MT41	MT41	MT41
	Density	4Gb	4Gb	4Gb	4Gb	4Gb	4Gb	4Gb
	Configuration	512 Meg x 8, 256 Meg x 16	512 Meg x 8, 256 Meg x 16	512 Meg x 8, 256 Meg x 16	512 Meg x 8, 256 Meg x 16	512 Meg x 8, 256 Meg x 16	512 Meg x 8, 256 Meg x 16	512 Meg x 8, 256 Meg x 16
	Package	79-ball, 96-ball	79-ball, 96-ball	79-ball, 96-ball	79-ball, 96-ball	79-ball, 96-ball	79-ball, 96-ball	79-ball, 96-ball
	Base PN	MT41J256M	MT41J256M	MT41J256M	MT41J256M	MT41J256M	MT41J256M	MT41J256M
NAND	Type	Raw (host ECC required)	Raw (host ECC required)	Raw (host ECC required)	Raw (host ECC required)		Raw (host ECC required)	Raw (host ECC required)
	Family	MT29F	MT29F	MT29F	MT29F		MT29F	MT29F
	Density	128Mb–512Gb	128Mb–512Gb	128Mb–512Gb	128Mb–512Gb		128Mb–512Gb	128Mb–512Gb
	Package	48-pin TSOP	48-pin TSOP	48-pin TSOP	48-pin TSOP		48-pin TSOP	48-pin TSOP
NOR	Type	Serial	Serial	Serial	Serial	Serial	Serial	Serial
	Family	MT25Q	MT25Q	MT25Q	MT25Q	MT25Q	MT25Q	MT25Q
	Density	128Mb–2Gb	128Mb–2Gb	128Mb–2Gb	128Mb–2Gb	128Mb–2Gb	128Mb–2Gb	128Mb–2Gb
	Package	Many	Many	Many	Many	Many	Many	Many
e.MMC	Type	Managed (JEDEC STD)	Managed (JEDEC STD)	Managed (JEDEC STD)	Managed (JEDEC STD)	Managed (JEDEC STD)	Managed (JEDEC STD)	Managed (JEDEC STD)
	Family	MTFC	MTFC	MTFC	MTFC	MTFC	MTFC	MTFC
	Density	4GB–64GB	4GB–64GB	4GB–64GB	4GB–64GB	4GB–64GB	4GB–64GB	4GB–64GB
	Package	VFBGA, TFBGA, LFBGA	VFBGA, TFBGA, LFBGA	VFBGA, TFBGA, LFBGA	VFBGA, TFBGA, LFBGA	VFBGA, TFBGA, LFBGA	VFBGA, TFBGA, LFBGA	VFBGA, TFBGA, LFBGA
eUSB	Type	Managed (USB)	Managed (USB)	Managed (USB)	Managed (USB)	Managed (USB)	Managed (USB)	Managed (USB)
	Family	MTEDC	MTEDC	MTEDC	MTEDC	MTEDC	MTEDC	MTEDC
	Density	2GB–16GB	2GB–16GB	2GB–16GB	2GB–16GB	2GB–16GB	2GB–16GB	2GB–16GB
	Package	36.9mm x 26.6mm	36.9mm x 26.6mm	36.9mm x 26.6mm	36.9mm x 26.6mm	36.9mm x 26.6mm	36.9mm x 26.6mm	36.9mm x 26.6mm
SATA SSD	Type	Managed (SATA)		Managed (SATA)	Managed (SATA)		Managed (SATA)	Managed (SATA)
	Family	MTFDD		MTFDD	MTFDD		MTFDD	MTFDD
	Density	100GB–960GB		100GB–960GB	100GB–960GB		100GB–960GB	100GB–960GB
	Package	2.5" drive, 7mm height		2.5" drive, 7mm height	2.5" drive, 7mm height		2.5" drive, 7mm height	2.5" drive, 7mm height

Micron® Memory Support for NXP® Networking Platforms

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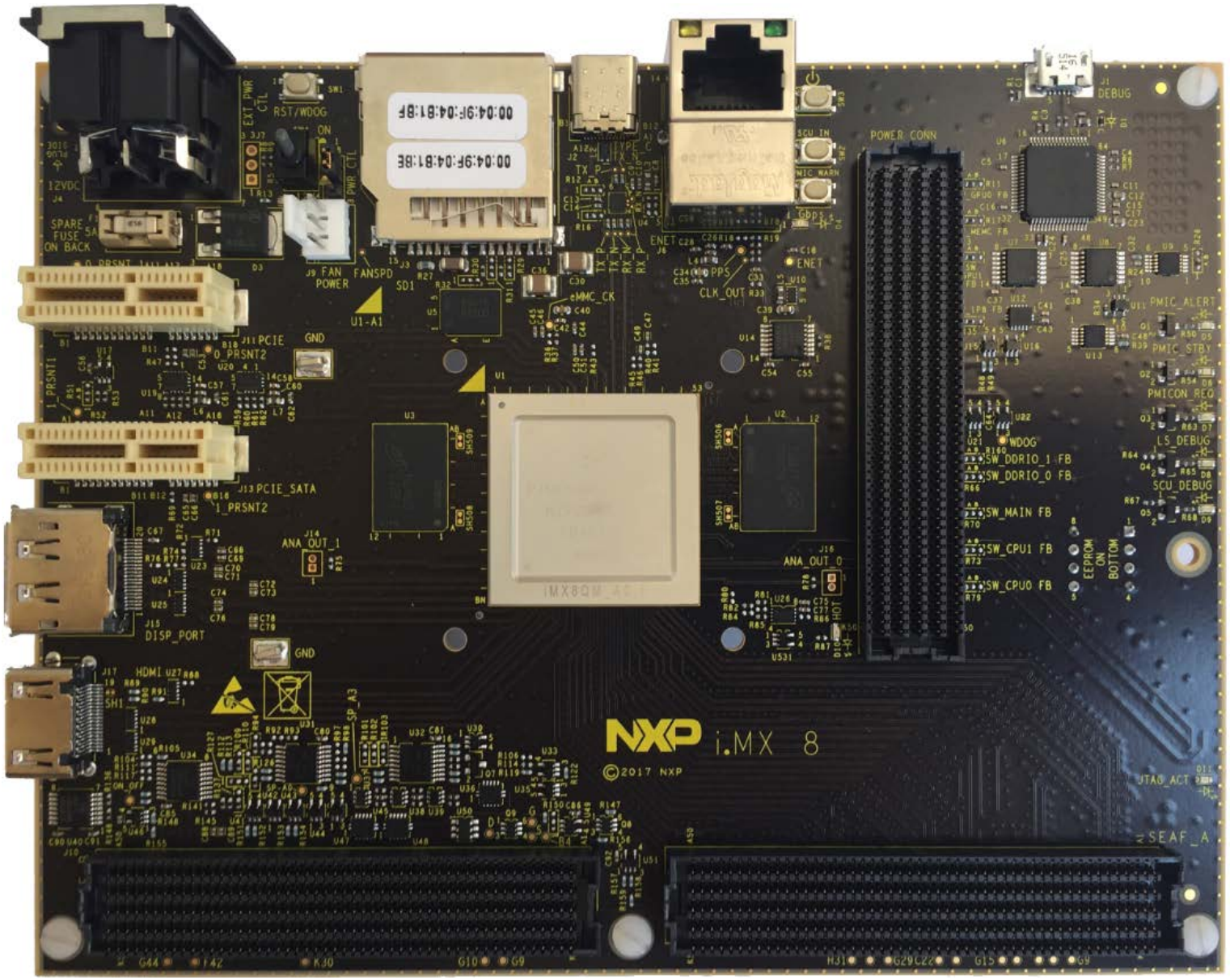
Micron Memory		QorIQ Processor Memory			
		Value Tier			Mid-Range Tier
		LS1020/LS1021/LS1022	T1023/T1024	T1020, T1022, T1040, T1042	LS2085
DRAM	Type	DDR3L	DDR3L UDIMM	DDR3L UDIMM	DDR4 UDIMM
	Density	4Gb	4GB (x72, ECC, DR)	4GB (x72, ECC, DR)	8GB (x72, ECC, DR)
	Configuration	256 Meg x 16	4GB (512 Meg x 72)	4GB (512 Meg x 72)	1 Gig x 72
	Package	96-ball VFBGA	UDIMM (Dual Rank)	UDIMM (Dual Rank)	UDIMM (Dual Rank)
	Part Number	MT41K256M16HA-125:E	MT18KSF512720Z-1G6	MT18KSF512720Z-1G6	MTA18ASF1G72AZ-2G1A1
NAND	Type		Raw (host ECC required)	Raw (host ECC required)	Raw (host ECC required)
	Density		8Gb	8Gb	16Gb
	Package		48-pin TSOP	48-pin TSOP	48-pin TSOP
	Part Number		MT29F8G08ABBCAH4	MT29F8G08ABABAWP-ITX:B	MT29F16G08ABABA
NOR	Type	Serial	Serial	Serial	Serial
	Density	128Mb	512Mb	512Mb	512Mb
	Package	24-ball TBGA	SO8, SO16, 24-ball TBGA	SO8, SO16, 24-ball TBGA	SCP2-16/300 mils
	Part Number		MT25QL512ABA1ESF		
e.MMC	Type	Managed (JEDEC STD)		Managed (JEDEC STD)	Managed (JEDEC STD)
	Density	4GB–64GB		4GB–64GB	4GB–64GB
	Package	VFBGA, TFBGA, LFBGA		VFBGA, TFBGA, LFBGA	VFBGA, TFBGA, LFBGA
	Part Number	MTFC		MTFC	MTFC
eUSB	Type	Managed (USB)	Managed (USB)	Managed (USB)	Managed (USB)
	Density	2GB–16GB	2GB–16GB	2GB–16GB	2GB–16GB
	Package	36.9mm x 26.6mm	36.9mm x 26.6mm	36.9mm x 26.6mm	36.9mm x 26.6mm
	Part Number	MTEDC	MTEDC	MTEDC	MTEDC
SATA SSD	Type	Managed (SATA)		Managed (SATA)	Managed (SATA)
	Density	100GB–960GB		100GB–960GB	100GB–960GB
	Package	2.5" drive, 7mm height		2.5" drive, 7mm height	2.5" drive, 7mm height
	Part Number	MTFDD		MTFDD	MTFDD

Micron

i.MX8 Quad Max

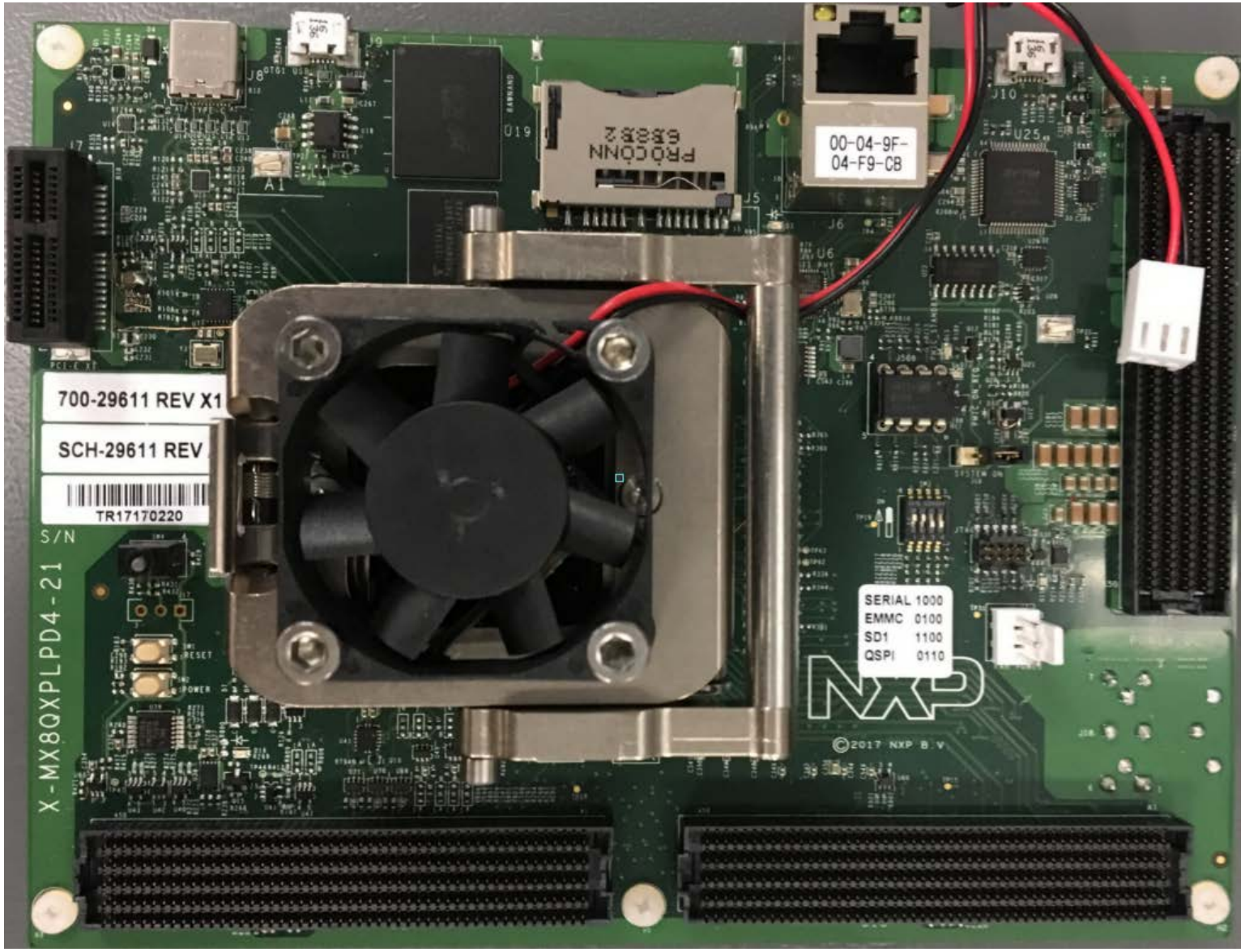


i.MX8 QM Features Micron's:

- **LPDDR4 (up to 8GB)**
- **Xccela™ Octal Flash, Q-SPI**
- **32GB eMMC5.0** (back side)

Board photo of released MX8 Quad Max

i.MX8 Quad X Plus

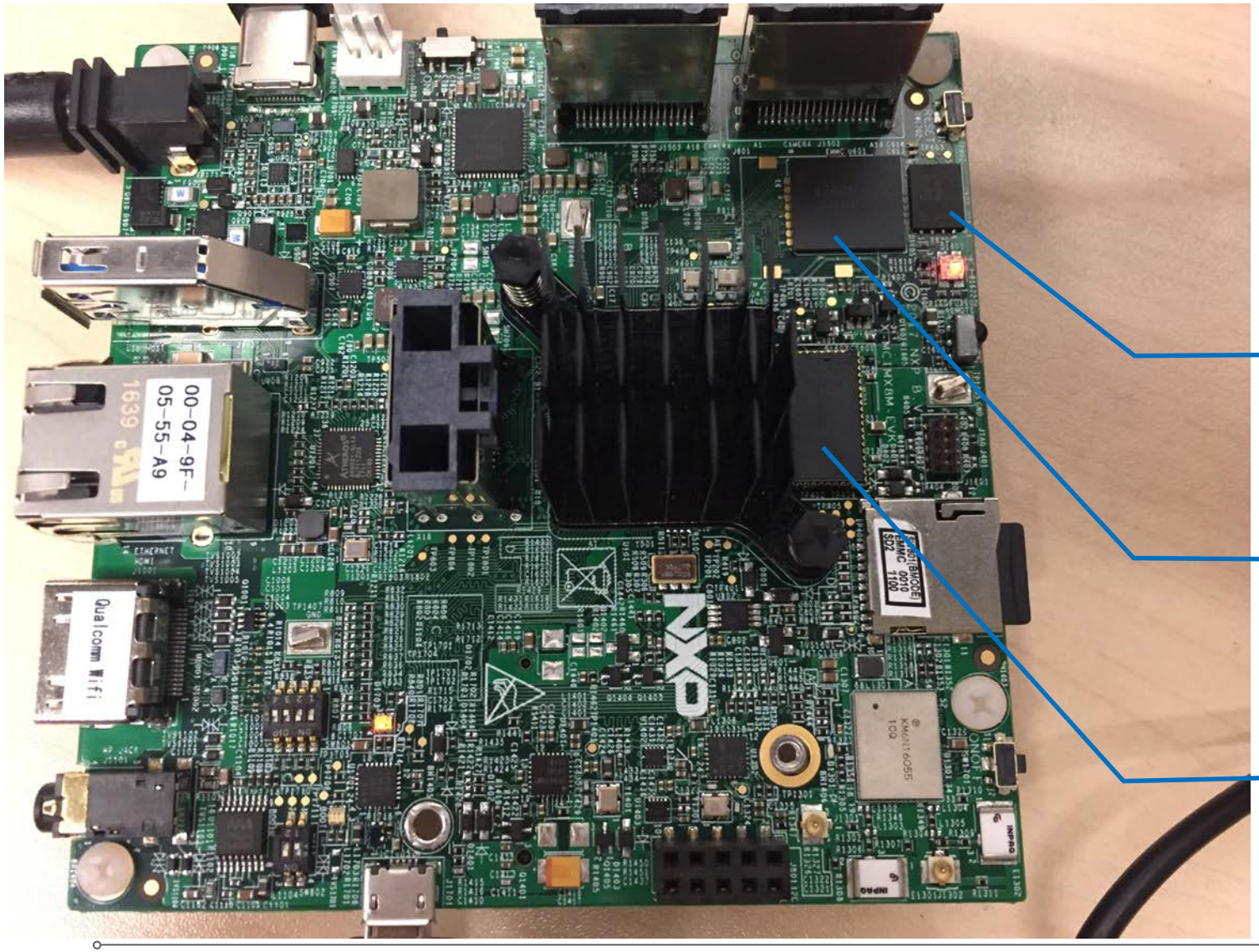


i.MX8 QXP Features Micron's:

- **LPDDR4 (up to 8GB)**
- **Xccela™ Octal Flash, Q-SPI**
- **32GB eMMC5.0** (back side)

Board photo of released MX8 Quad X Plus

i.MX8 M



i.MX8 M has validated Micron's:

- **3GB LPDDR4**
- **256MbQuad SPI**
- **16GB eMMC5.0**

Quad SPI Flash
MT25QL256ABA1EW9-0SIT

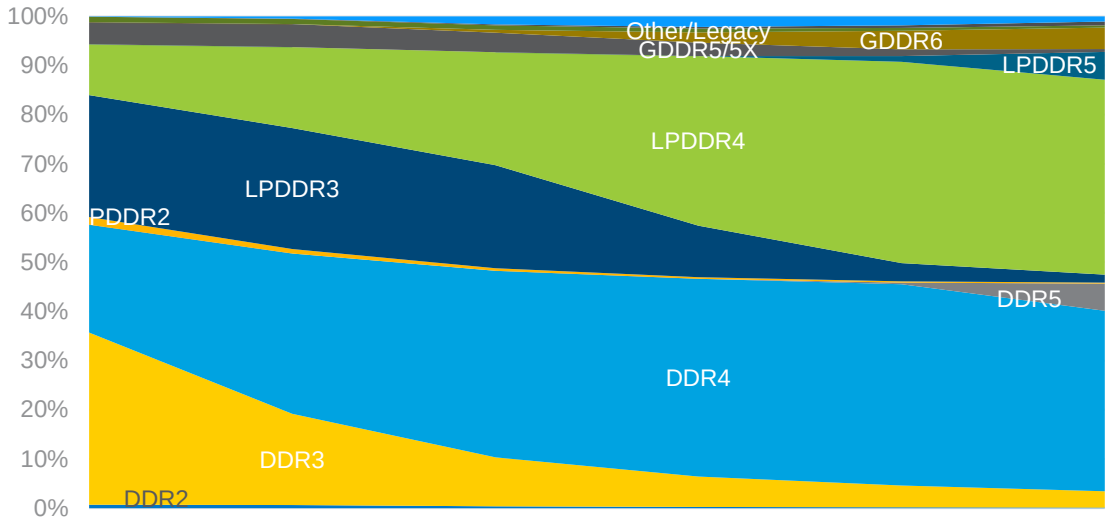
16GB e.MMC
MTFC16GAKAECN-2M WT

3GB LPDDR4
MT53B768M32D4NQ-062 WT:B

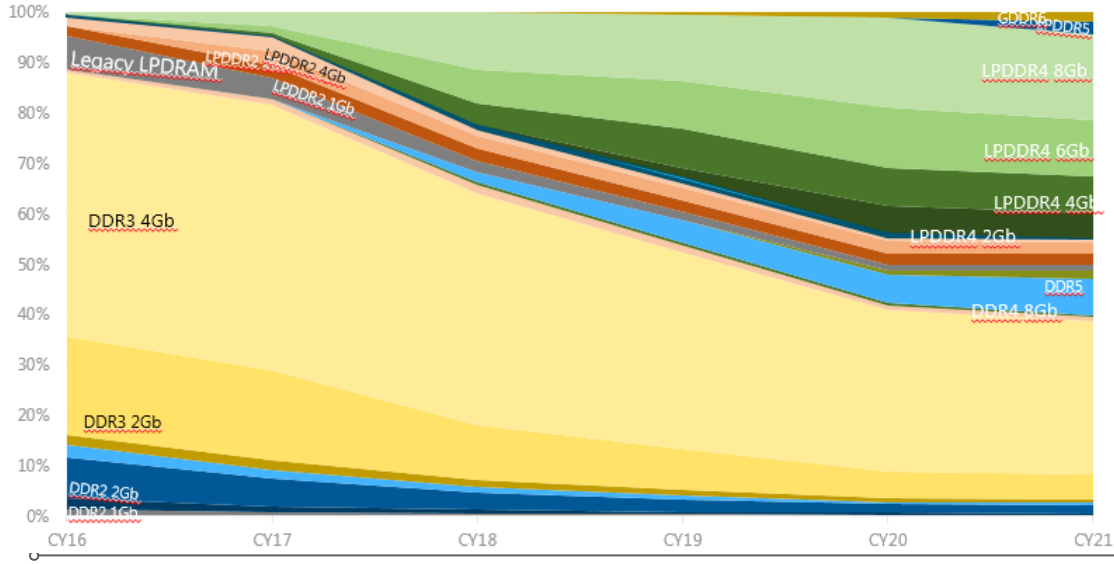
Board photo of released MX8 M

DRAM / Flash Market Section

DRAM Market Trends, General Market vs Automotive Adoption



Automotive

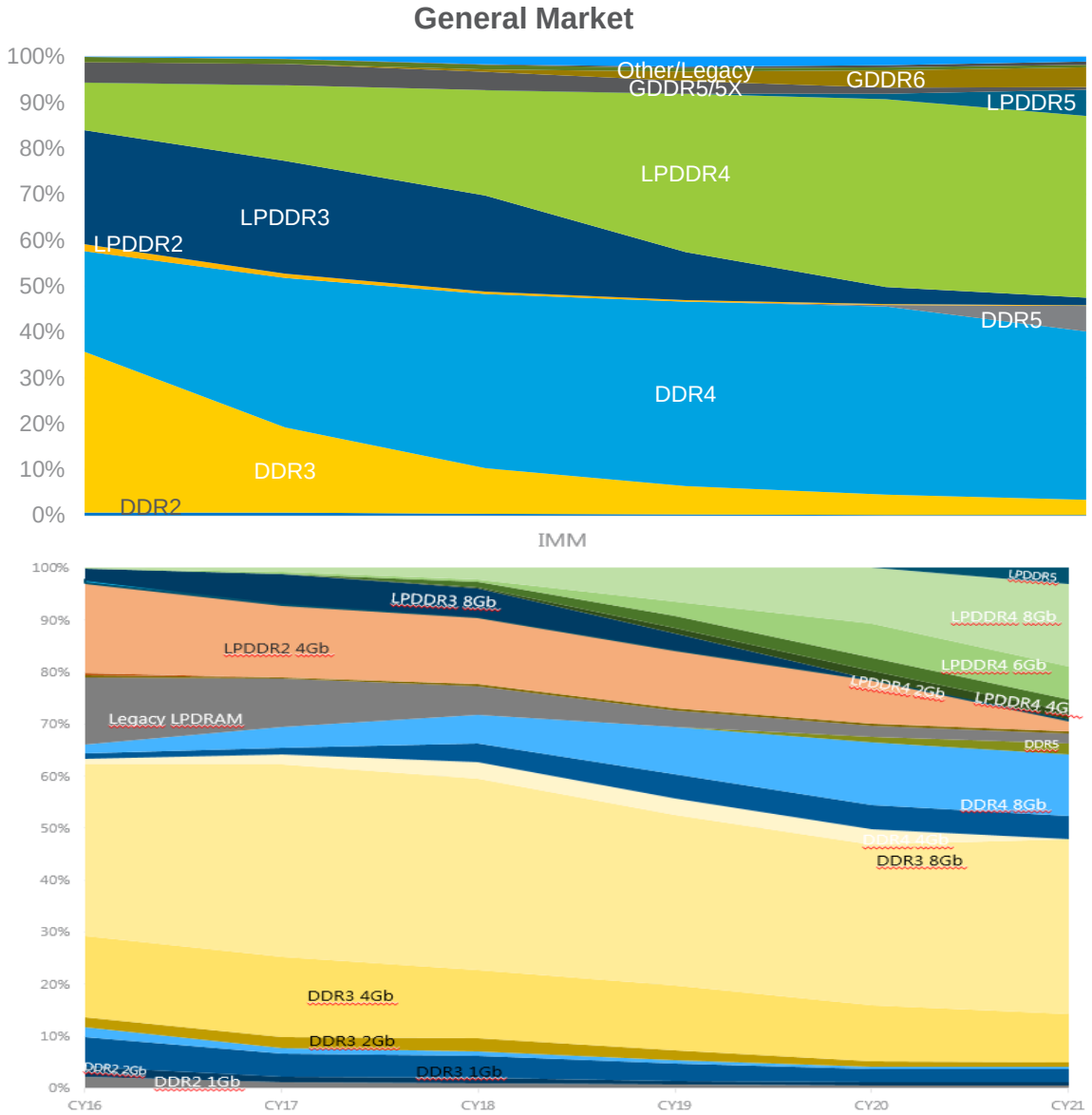


- General Market:
  - DDR is the dominant interface for devices without batteries
  - Increased LPDRAM adoption outside of mobile handsets driven by Tablets & other Client apps
  - DDR5/LPDDR5 adoption projected to start in late CY'19

- Automotive:
  - Continued need for legacy support
  - DDR3 is the primary choice for current gen low cost Infotainment and Cluster applications
  - LPDDR4 will be the primary choice for next gen ADAS and high-end Infotainment applications

Source: Micron Market Models

DRAM Market Trends, General Market vs IMM



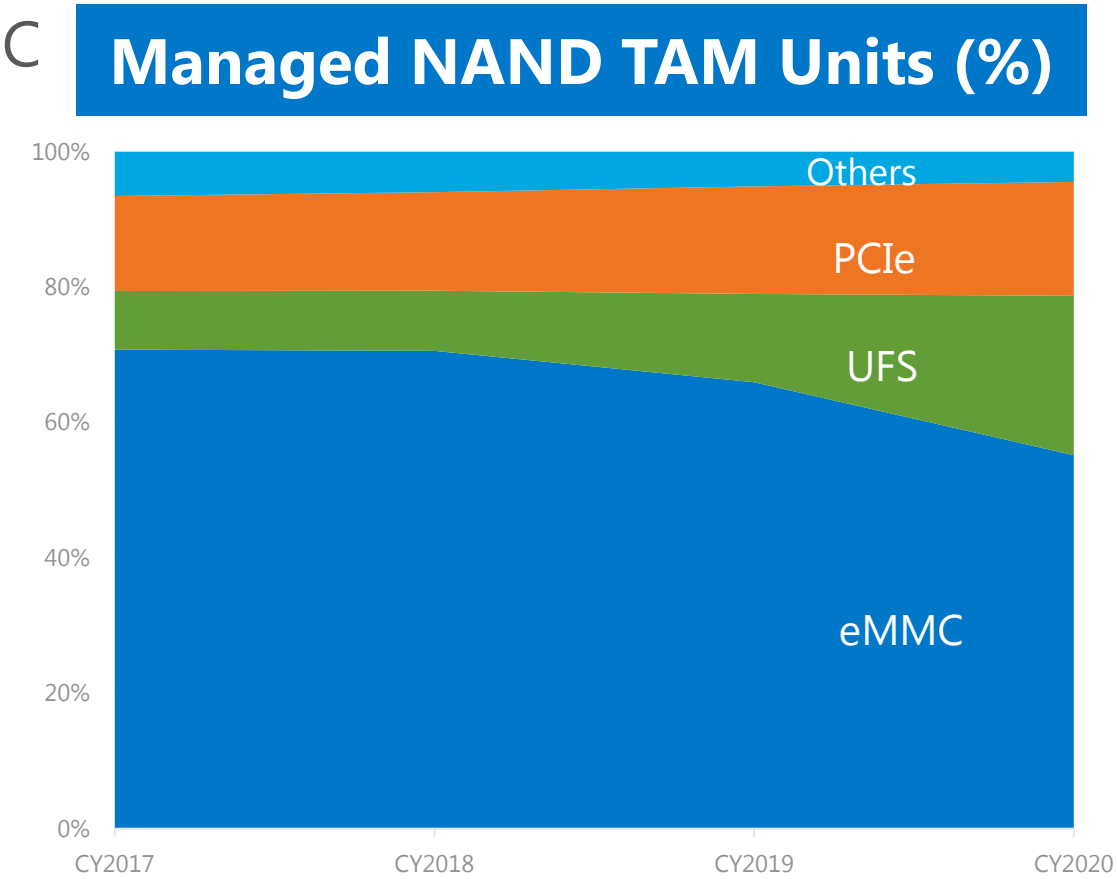
- General Market:
  - DDR is the dominant interface for devices without batteries
  - Increased LPDRAM adoption outside of mobile handsets driven by Tablets & other Client apps
  - DDR5/LPDDR5 adoption projected to start in late CY'19

- Industrial Multi-Market (IMM):
  - Continued need for legacy support in both DRAM and LPDRAM with a wide mix of technologies
  - DRAM modules in Industrial Automation drive bulk of DDR4 adoption
  - Strong LP adoption for battery driven applications
    - LPDDR4 is gaining traction

Source: Micron Market Models

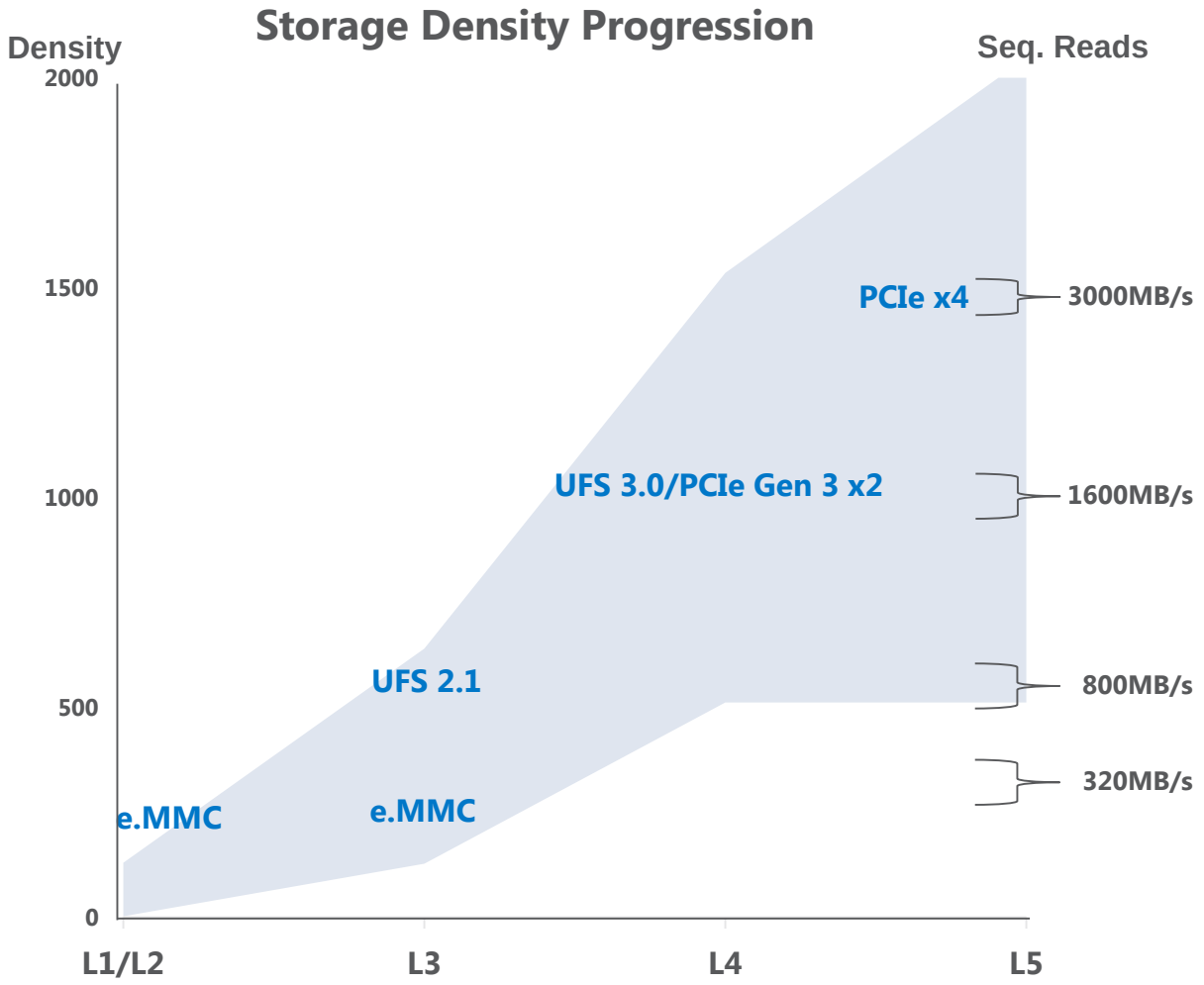
Broad NVM Market Growth Dynamics

- Continued strong deployment of eMMC
  - Broader, embedded markets
- UFS driven by mobile
  - Higher performance / density
- Strong market momentum for PCIe
  - Essential, performance driven applications



Source: Micron market models

Explosive Demand for Memory with Autonomous Driving



L5 expected to need >1TB storage

Includes IVI, Cluster, Central & Boot storage for autonomous, Black Box Recording

Source: Micron Marketing

Technical Details

LPDDRx and DDRx SDRAM Feature Comparison

Type	LPDDR2	LPDDR3	LPDDR4/4X	DDR2	DDR3/DDR3L	DDR4
Die Density	Up to 8Gb	Up to 32Gb	Up to 32Gb	Up to 2Gb	Up to 8Gb	Up to 16Gb (128Gb 8H)
Core Voltage (Vdd)	1.2V 1.8V WL supply req.	1.2V 1.8V WL supply req.	1.1V/1.0V 1.8V WL supply req.	1.8V 1.55V	1.5V/1.35V	1.2V Separate WL supply 2.5V
I/O Voltage	1.2V	1.2V	1.1V (4X = 0.6V)	Same as VDD	Same as VDD	Same as VDD
Max Clock Freq. /Data rate	533MHz/DDR1066	800MHz/DDR1600	2133MHz/DDR4267	533MHz/DDR1066	1066MHz/DDR2100	1600MHz+/DDR3200+
Burst Lengths	4, 8, 16	8	16, 32	4, 8	BC4, 8	BC4, 8
Configurations	x16, x32	x16, x32	2Ch x16	x4, x8, x16	x4, x8, x16	x4, x8, x16
Address/ Command Signals	14 pins (Mux'd command address)	14 pins (Mux'd command address)	10 pins per channel (Mux'd command Address)	25 pins	27 pins	29 pins (partial mux'd)
Address/ Command Data Rate	DDR (both rising and falling edges of clock)	DDR (both rising and falling edges of clock)	SDR (rising edge of clock only)	SDR (rising edge of clock only)	SDR (rising edge of clock only)	SDR (rising edge of clock only)
On Die Temperature Sensor	Yes	Yes	Yes	No	Optional/RS	Yes
DPD (Deep power-down mode)	Yes	Yes	No	No	No	No
Package Options	POP, MCP, discrete	POP, MCP, discrete	PoP, MCP, discrete	Discrete	Discrete	Discrete
Product/Temp. Grades	CT, IT, AIT, AT, AAT	CT, IT, AIT, AT, AAT	WT (-25' to 85'C) AAT (-40C to 105C) AUT (-40'C to 125'C)	CT, IT, AIT, AT, AAT	CT, IT, AIT, AT, AAT, AUT	CT, IT, AIT, AT, AAT, AUT

Standard DRAM & LPDRAM Trade Offs

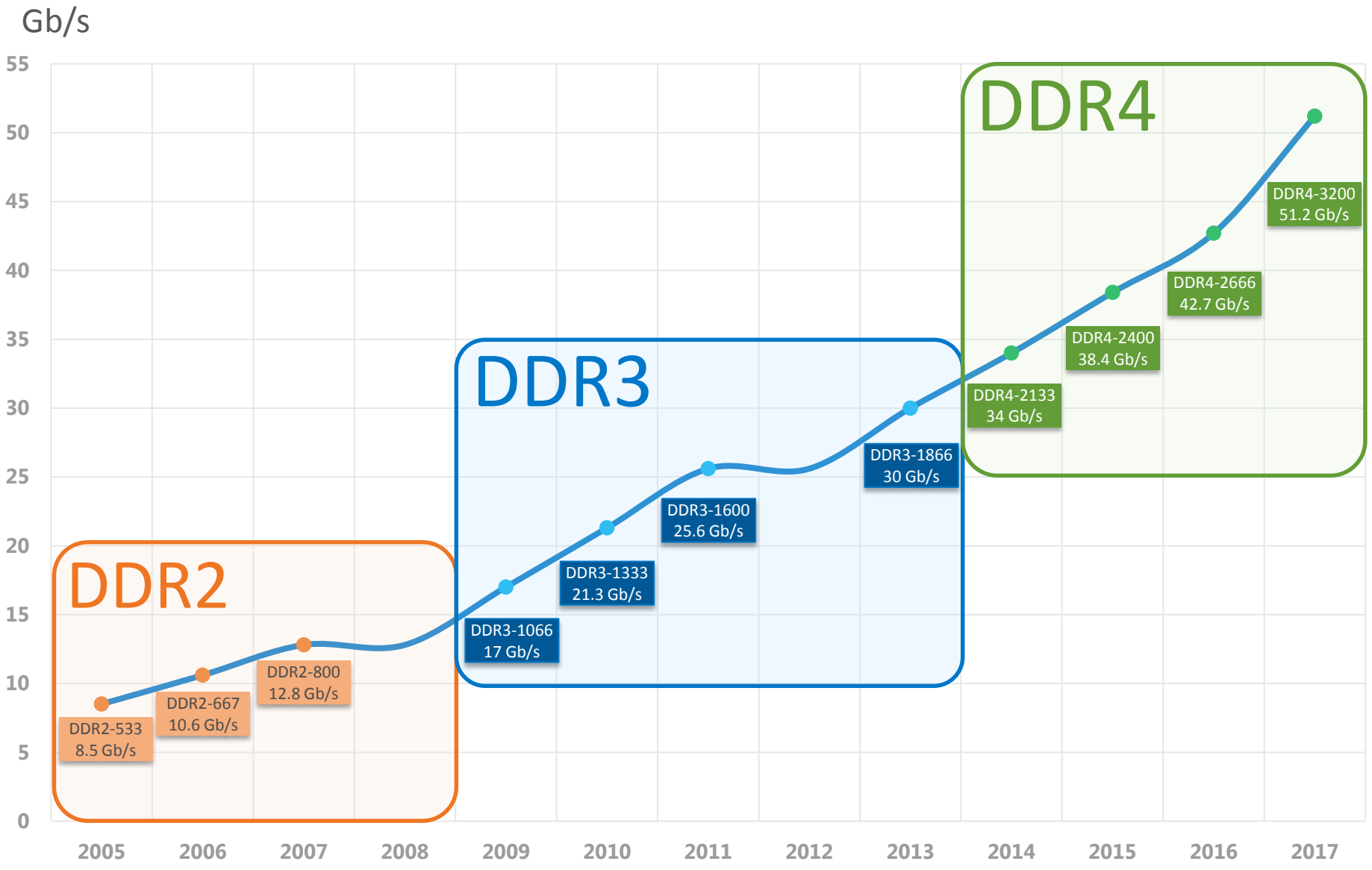
General LP vs. DDR Comparison

LPDDR4 Specific Info

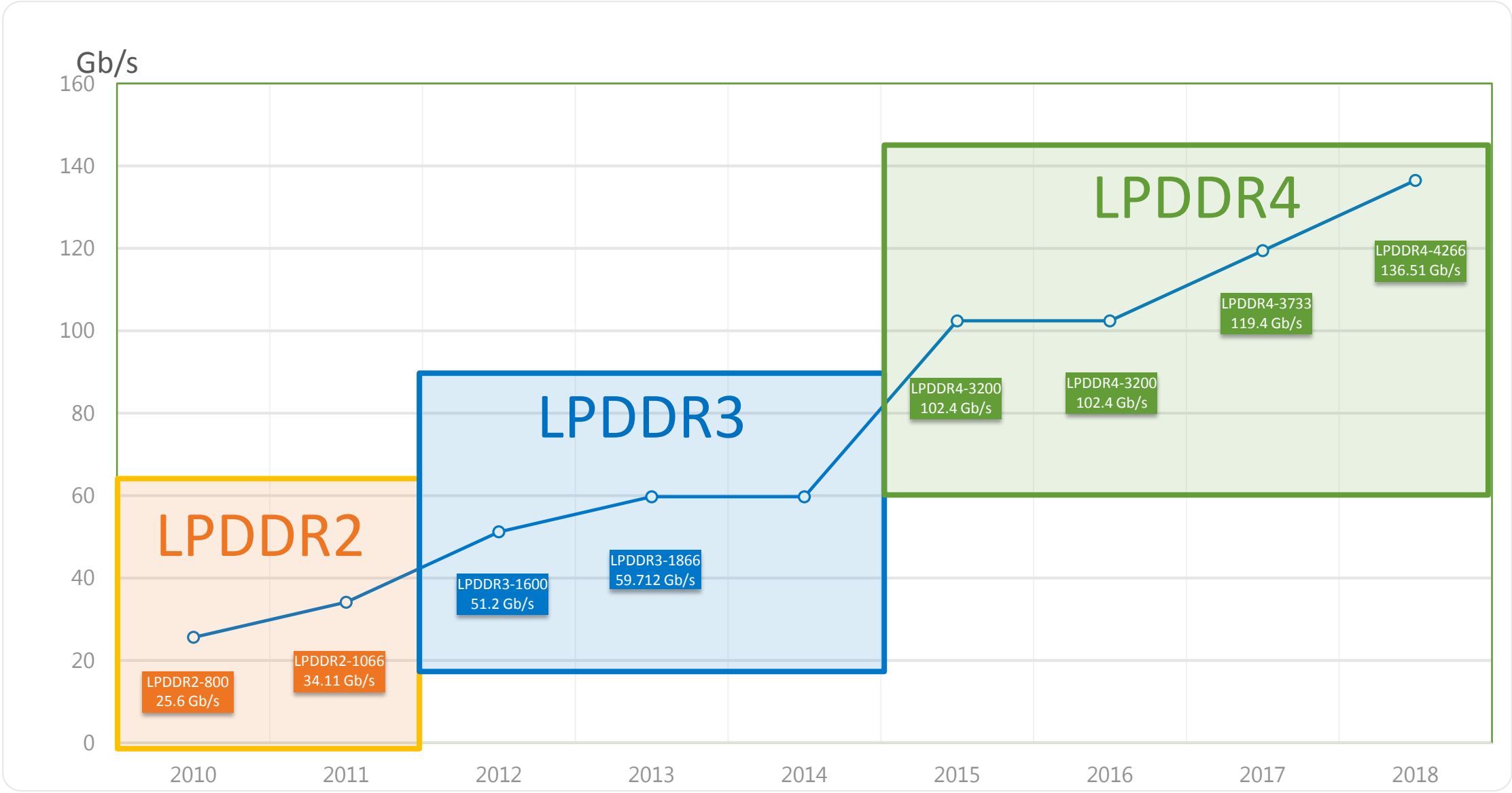
	Standard DRAM	LPDRAM
Form Factor	Center bond pads for highest performance and lowest cost	Edge bond pads allow for stacked die for MCP and PoP packaging, enabling compact form factors
Performance	x4, x8, x16 is lower cost and supports higher density configurations	x32 allows system to support high bandwidth in point-to-point applications
DRAM power	IDD specifications are geared towards moderate stand-by power, providing the highest yields and lowest cost	Ultra low standby power enabled by on-die power management and long refresh rates
System power	Additional Delay Locked Loop (DLL) circuitry required for high performance which inhibits system power savings	Lack of DLL circuitry allows for improved system power management; System can enter/exit power-down modes as well as throttle or stop the clock
Key Takeaway	**Optimized for cost and performance; *cost is primary feature***	**Optimized for battery life and portability; *low power & smallest possible footprint are primary features***

LPDRAM offers additional value over standard DRAM

DRAM Performance Improvements Over Time (IO x16)

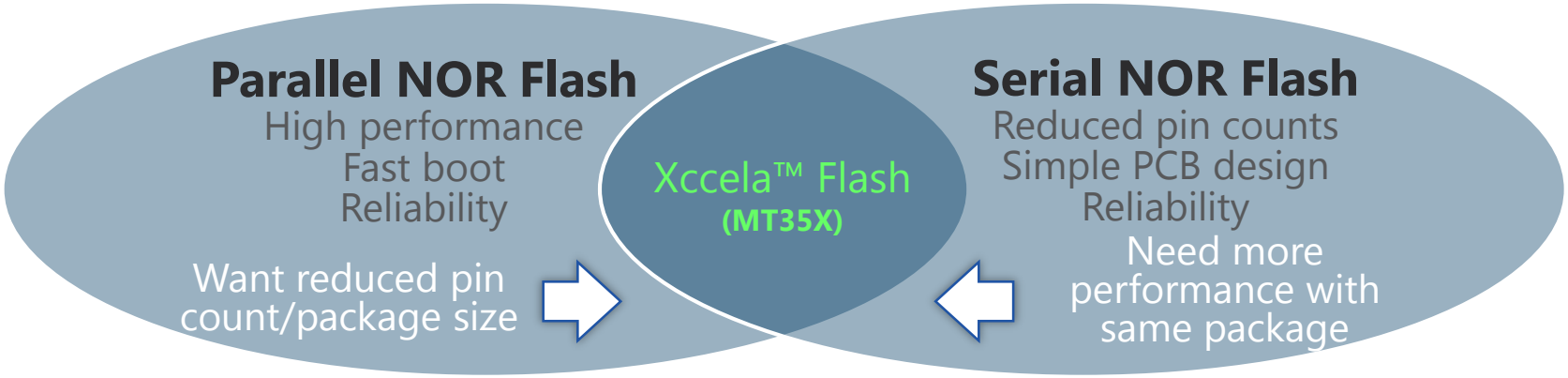


LPDDR Performance Improvements Over Time (IO x32)



Non-Volatile Details

Xccela™ Flash: Best of Parallel and Serial NOR Flash



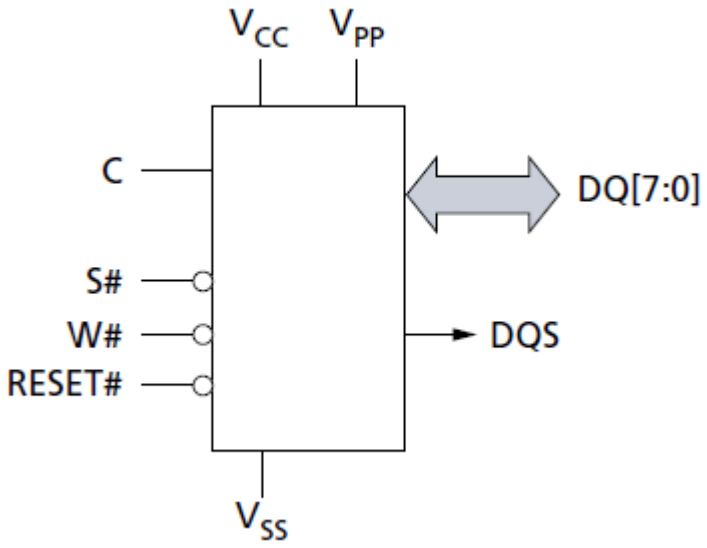
	512Mb Parallel NOR MT28EW	512Mb Quad-SPI MT25Q	512Mb Twin-Quad MT25T	512Mb Xccela Flash MT35X
Bandwidth	80MB/s (Page mode, async, x16)	90MB/s (90MHz, DDR mode)	180MB/s (90MHz, DDR mode)	**400MB/s (200MHz, DDR mode)**
Initial Word Access Time	95ns (x16)	139ns (1.8V, 4-bit) 157ns (1.8V, 16-bits)	139ns (1.8V, 8-bit) 145ns (1.8V, 16-bit)	**85ns (1.8V, 8-bit) 87.5ns (1.8V, 16-bit)**
Subsequent Word Access	20ns (16-bits) (95ns across 32B page)	6ns (4-bits) 24ns (16-bits)	6ns (8-bits) 12ns (16-bits)	**2.5ns (8-bits) 5ns (16-bits)**
Package and Pins	64-TBGA (11x13mm) 50 Active Pins	24-BGA (6x8mm) 6 Active Pins	24-BGA (6x8mm) 11 Active Pins	**24-BGA (6x8mm) 11 Active Pins**
Energy Per Bit	101 pJ/bit	41 pJ/bit	41 pJ/bit	**28 pJ/bit**

5X THE PERFORMANCE, **4X** FEWER PINS, **3X** LESS ENERGY, AND **2X** SMALLER PACKAGE*

Source Micron datasheets

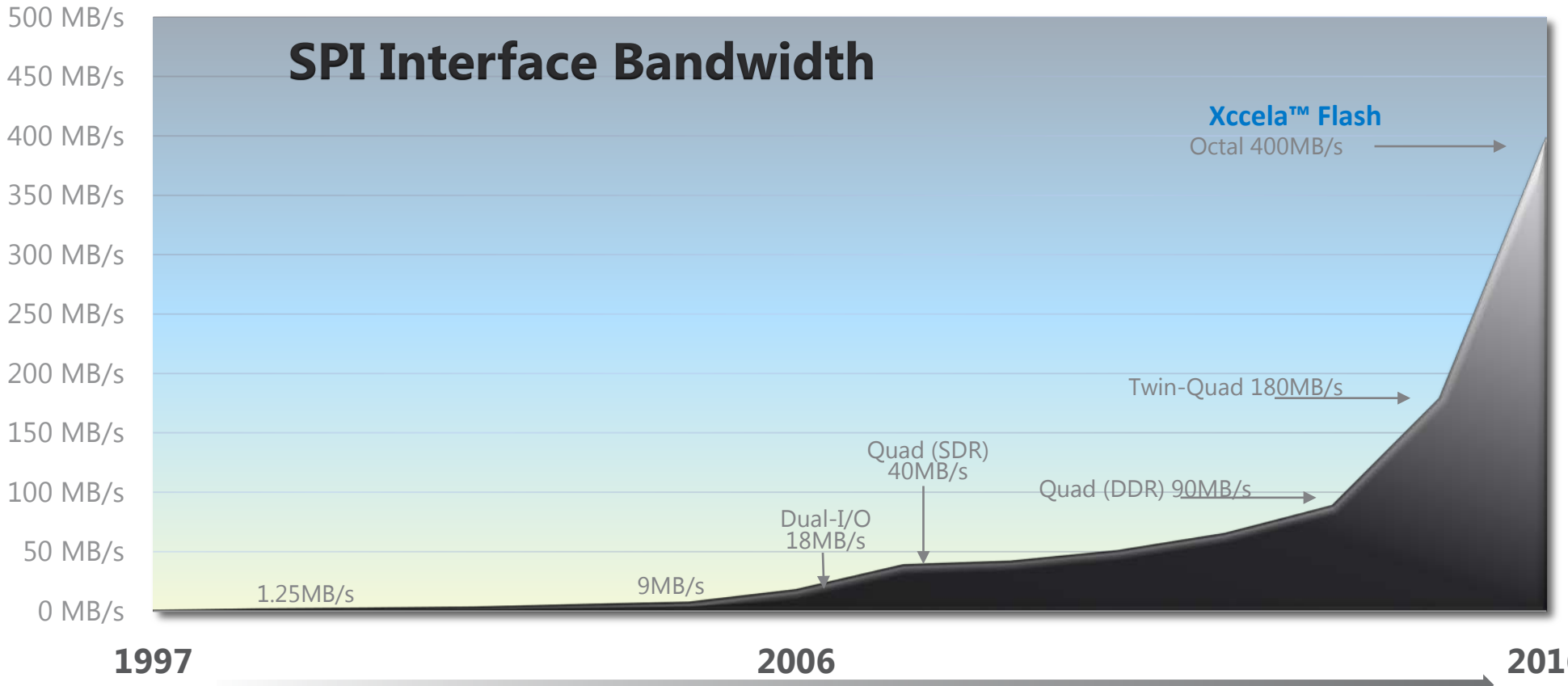
* Compared to Page Mode Parallel NOR

MT35X (Octal) aka
Xccela™ Flash



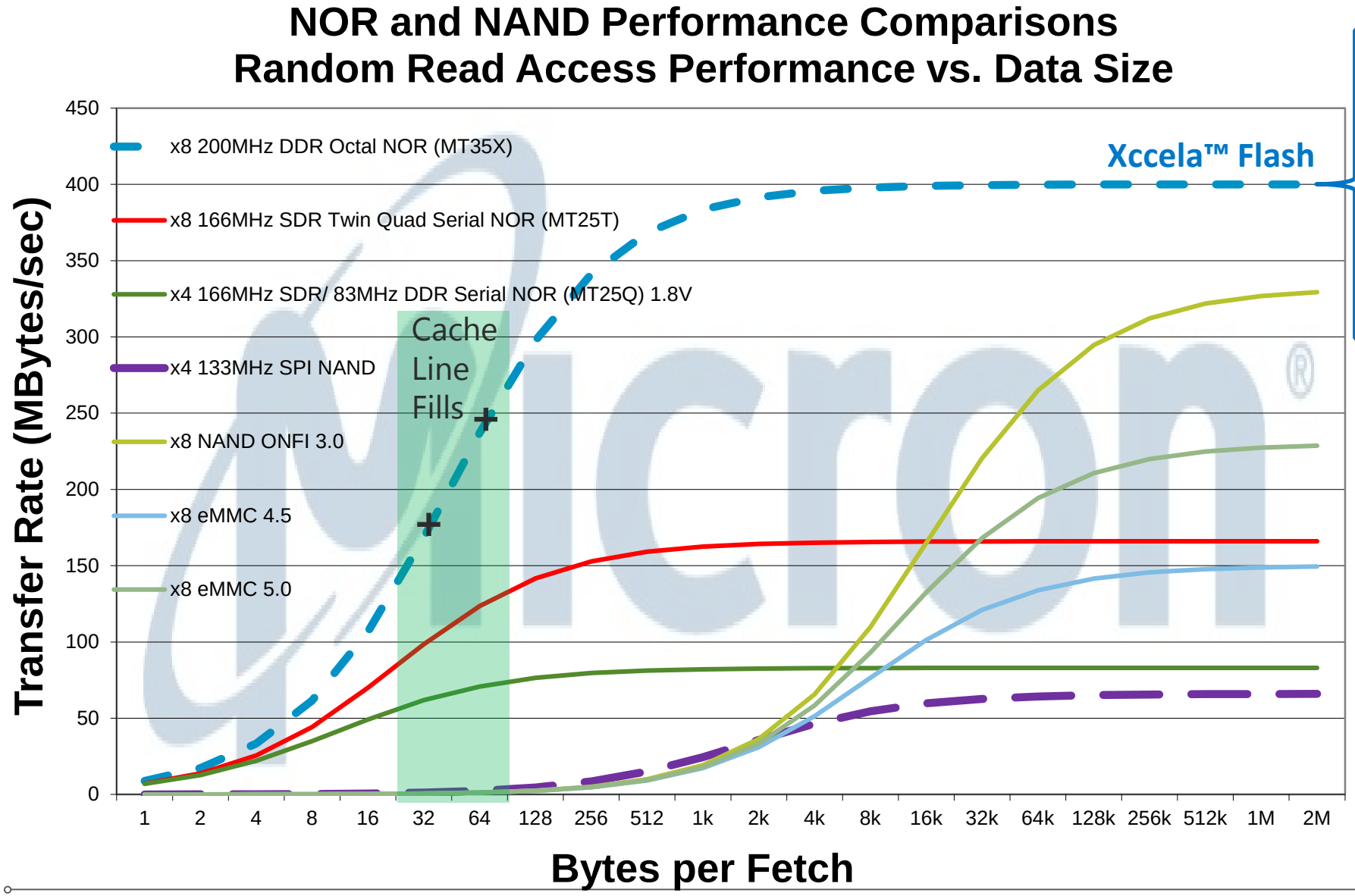
Symbol	Type	Description
C	Input	**Clock:** Provides timing for the serial interface. Command, address, or data inputs are latched on the rising edge of C. Data is shifted out on the falling edge of C.
S#	Input	**Chip select:** When S# is LOW, device is selected and in active power mode. Operations are initiated on the falling edge of S#. When S# is HIGH, device is deselected, DQ pins are tri-stated, and unless an internal WRITE operation is in progress, device enters standby mode.
RESET#	Input	**RESET:** Resets device to its default settings, such as after a volatile configuration register setting which then requires a return to the device default setting. Reset is optional when device settings are fixed by nonvolatile configuration register settings and always synchronized with the host. This pad is internally tied to weak pull-up so the pin can be floated.
W#	Input	**Write protect:** This input signal is used to freeze the status register in conjunction with the enable/disable bit of the status register. When the enable/disable bit of the status register is set to 1 and the W# signal is driven LOW, the status register nonvolatile bits become read-only and the WRITE STATUS REGISTER operation will not execute. During the extended-SPI protocol with OCTAL READ/PROGRAM instructions, and during octal DDR protocol, this pin functions as an input/output (DQ2 functionality). This signal does not have internal pull-ups, it cannot be left floated and must be driven, even if none of W#/DQ2 function is used.
DQ[7:0]	I/O	**Serial I/O:** Bidirectional signals that transfer address, data, and command information. In extended-SPI protocol, DQ0 functions as input and DQ1 as output. DQ[7:2] are not used. In octal protocol, input/output on DQ[7:0] depends on the command. Input can be latched on the rising edge of C (SDR) or on both edges of C (DDR). Data can be shifted out on the falling edge of C (SDR) or on both edges of C (DDR). In octal DDR, DQ[7:0] always function as I/O, input is latched on both edges of C, and output is shifted out on both edges of C. DQ2 is used also as write protection control.
DQS	Output	**Data Strobe:** Indicates output data valid for DDR modes and is required to support high speed data output. Not required in extended-SPI protocol except to achieve high frequency for specific DDR commands.
V_{CC}	Supply	**Supply voltage:** Core and I/O supply.
V_{PP}	Supply	**Supply voltage:** If V_{PP} is in the voltage range of V_{PPH}, the signal acts as an additional power supply for programming operation, as defined in the Operating Conditions table. The V_{PP} pad will be internally pulled up to V_{CC}, so customer can leave V_{PP} pin floated if not used.
V_{SS}	Supply	**Ground:** Core and I/O ground connection. V_{SS} is the reference for the V_{CC} supply voltage.

The Evolution of SPI



	SPI	Dual-SPI	Quad-SPI	Twin Quad	Octal
# of Signals	6	6	6	10-12	11
Clock (max)	75MHz	75MHz	180MHz SDR (90MHz DDR)	180MHz SDR (90MHz DDR)	166MHz SDR (200MHz DDR)
Bandwidth (max)	9MB/s	18MB/s	90MB/s	180MB/s	400MB/s

Micron Read Performance Comparisons



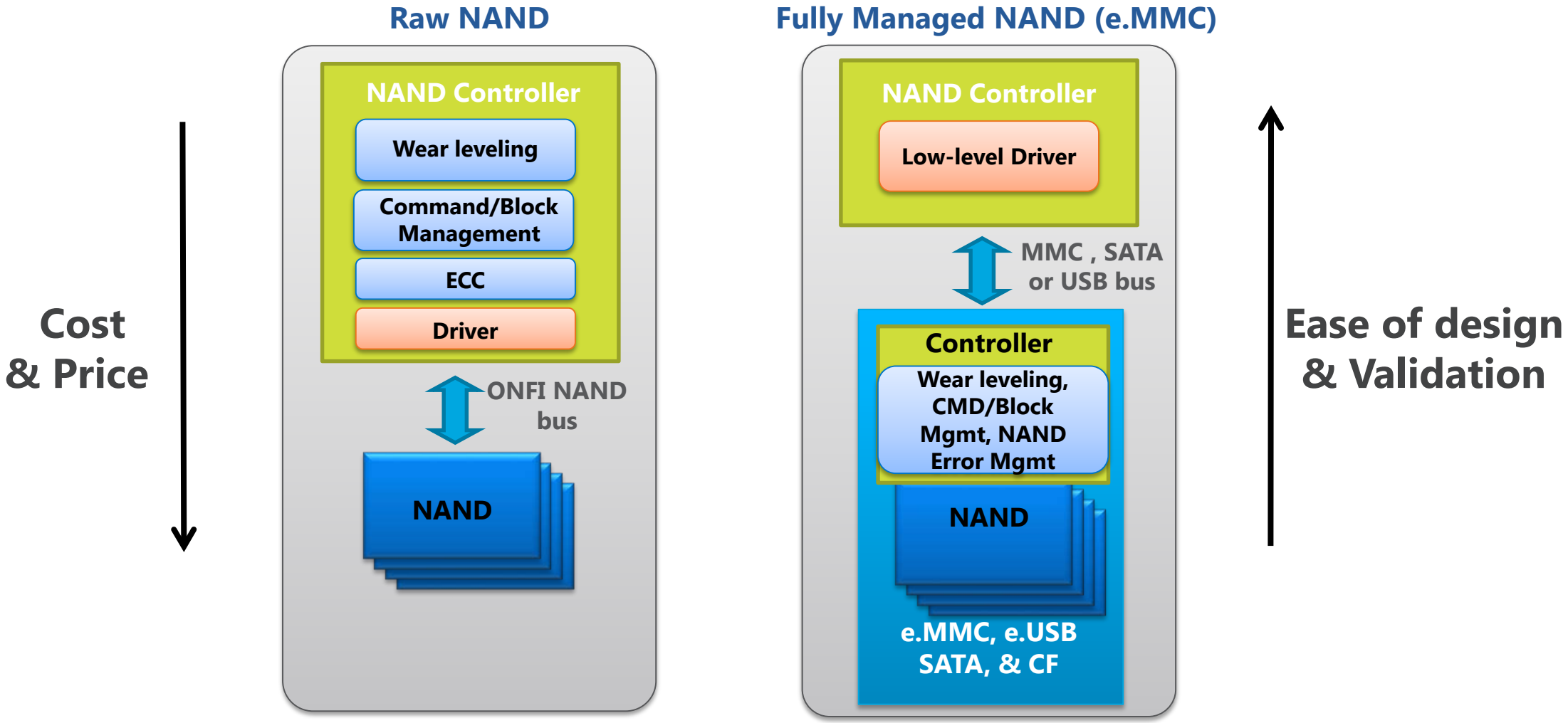
Xccela™ Flash
Highest Performance

BOOT or Read time at 400MB/s			
Bit density	512Mb	1Gb	2Gb
Byte density	64MB	128MB	256MB
Time to read	.16 sec	.32 sec	.64 sec

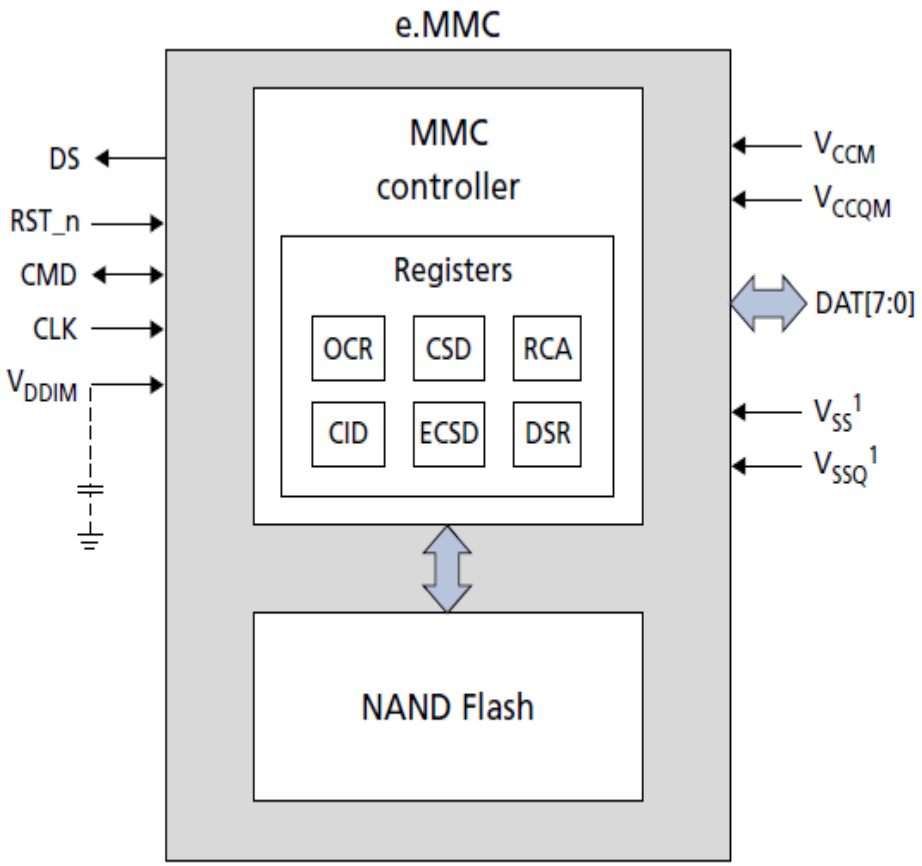
Graphic image read @2Bytes (65K colors)		
Pixel Size	1K x 1K	4K x 4K
Byte density	2MB	34MB
Time to read	5.2ms	88ms

e.MMC Fully Managed NAND

PROVIDES REDUCED DESIGN EFFORT FOR MINIMAL COST



e.MMC



Note: 1. V_{SS} and V_{SSQ} are internally connected.

Symbol	Type	Description
CLK	Input	Clock: Each cycle of the clock directs a transfer on the command line and on the data line(s). The frequency can vary between the minimum and the maximum clock frequency.
RST_n	Input	Reset: The RST_n signal is used by the host for resetting the device, moving the device to the pre-idle state. By default, the RST_n signal is temporarily disabled in the device. The host must set ECSD register byte 162, bits[1:0] to 0x1 to enable this functionality before the host can use it.
CMD	I/O	Command: This signal is a bidirectional command channel used for command and response transfers. The CMD signal has two bus modes: open-drain mode and push-pull mode. Commands are sent from the MMC host to the device, and responses are sent from the device to the host.
DAT[7:0]	I/O	Data I/O: These are bidirectional data signals. The DAT signals operate in push-pull mode. By default, after power-on or assertion of the RST_n signal, only DAT0 is used for data transfer. The MMC controller can configure a wider data bus for data transfer either using DAT[3:0] (4-bit mode) or DAT[7:0] (8-bit mode). The device includes internal pull-up resistors for data lines DAT[7:1]. Immediately after entering the 4-bit mode, the device disconnects the internal pull-up resistors on the DAT[3:1] lines. Upon entering the 8-bit mode, the device disconnects the internal pull-ups on the DAT[7:1] lines.
DS	Output	Data strobe: Generated by the device and used for data output and CRC status response output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output, each cycle of this signal directs two bits transfer (2x) on the data, one bit for the positive edge and the other bit for the negative edge. For CRC status response output, the CRC status is latched on the positive edge only, and is "Don't Care" on the negative edge.
V_{CC}	Supply	V_{CC}: NAND interface (I/F) I/O and NAND Flash power supply.
V_{CCQ}	Supply	V_{CCQ}: e.MMC controller core and e.MMC I/F I/O power supply.
V_{SS}[1]	Supply	V_{SS}: NAND I/F I/O and NAND Flash ground connection.
V_{SSQ}[1]	Supply	V_{SSQ}: e.MMC controller core and e.MMC I/F ground connection.
V_{DDIM}		Internal voltage node. Do not tie to supply voltage or ground.
NC	–	No connect: No internal connection is present.
RFU	–	Reserved for future use: No internal connection is present. Leave it floating externally.

Enjoy Micron Automotive eMMC comprehensive Product Portfolio

Performance + Longevity

4.41 protocol
Density 4GB÷32GB
SR 44MB/s
SW 20MB/s
-40°C to 85°C

4.51 protocol
Density 4GB÷32GB
SR 140 MB/s
SW 37MB/s
-40°C to 85°C
-40°C to 105°C

5.0 protocol
Density 8GB÷128GB
SR 280 MB/s
SW 70MB/s
-40°C to 85°C
-40°C to 105°C

5.1 protocol
Density 8GB÷128BGB
SR 320 MB/s
SW 130MB/s
Target performance
-40°C to 85°C
-40°C to 105°C

PCIe / NVMe
UFS 2.x

2012 2013 2015 2017 2018

Reliability + Package JEDEC
100b, 1.0mm ball pitch
153b-169b, 0.5mm ball pitch

New Features in eMMC 5.1

eMMC 5.1 Feature	Description	Impact	Supported in Micron Automotive 5.1 eMMC?
CMD Queuing	Command Queuing in eMMC	Improved Performance (Random Read)	√
Cache Barrier	Reduce number of cache flush occurrences	Improved Performance	√
Cache Flushing Policy	eMMC device reports to host whether cache data written in order	Improved Performance	√
BKOP Control	Setting to indicate whether host allows BKOP during idle time	Improved Performance (latency)	√
RPBM Throughput Improvement	Improved performance due to increased RPMB chunk size (8KB)	Improved RPMB Performance	√
Enhanced Strobe	Align CMD response to DS	Improved Signal Integrity	√
Secure Write Protection	Authentication-based device write protect configuration using RPMB method for increased security	Increased Security	√

SSD Form Factors

EXISTING AND FUTURE DIRECTIONS

- FORM FACTORS
  - 2.5”
  - mSATA
  - M.2
  - uBGA (Future)
- INTERFACES
  - SATA III
  - PCIe
- YEARLY FIRMWARE UPDATES

Parameter	2.5”	mSATA	M.2
Capacities (GB)	60/120/240	60/120/240	120/240
Specification	EIA-720	MO-300B, variation A	PCIe M.2 Spec. Rev. 1.0
Dimensions	(L) 100.45mm (W) 69.85mm (H) 7mm	(L) 50.80mm (W) 29.85mm (H) 3.75mm	(L) 60 mm (W) 22 mm (H) 1.5 mm
Weight	< 70g	< 10g	< 10 g

Packaging

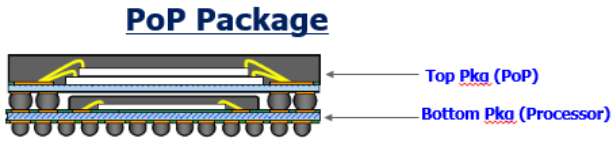
MCP (Multi Chip Package),
PoP (Package on Package)

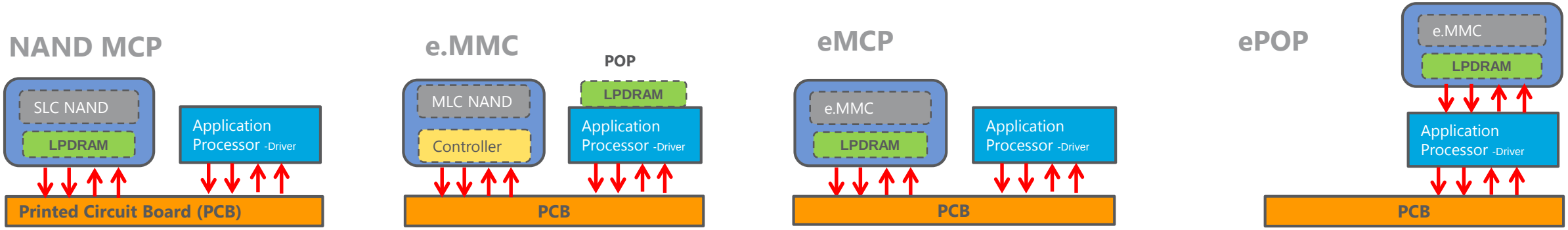
What is an e.MCP/e.PoP?

e.MCP is a Multi Chip Package including e.MMC and LPDDRx

e.PoP is an e.MCP in a PoP (Package on Package) design

- Benefits include…
  - Board space savings through vertical stacking of several memory chips
  - Minimize bill of materials for simplified manufacturing and cost savings
  - High density, low power consumption, shortest interconnections possible
  - Accelerated time to market through rapid integration of modules





Link to Micron's DRAM Power Calculators

https://www.micron.com/support/tools-and-utilities/power-calc

System Power Calculators

Whether it is calculating battery life for a portable application, planning cooling for a desktop, or determining the power supply for a server, an accurate power budget for the memory is essential.

That's why we've created the Micron System-Power Calculator for all of our SDRAM devices. A system designer can use these models to accurately approximate the power requirements of SDRAM in a system environment, as well as experiment with various memory access schemes to determine the impact on power consumption.

These tools provide an easy method for estimating the memory power requirements needed in making important system architecture and design decisions. With an accurate estimation of power consumption, the system designer can quickly handle complex system trade-offs to optimize the system performance.

For more detailed information on system-power calculations, see the following technical notes:

- DDR TN-46-03
- DDR2 TN-47-04
- DDR3 TN-41-01
- RLDRAM II TN-49-04
- Mobile LPDRAM TN-46-12
- Mobile LPDDR2 TN-42-01 (Restricted Access)

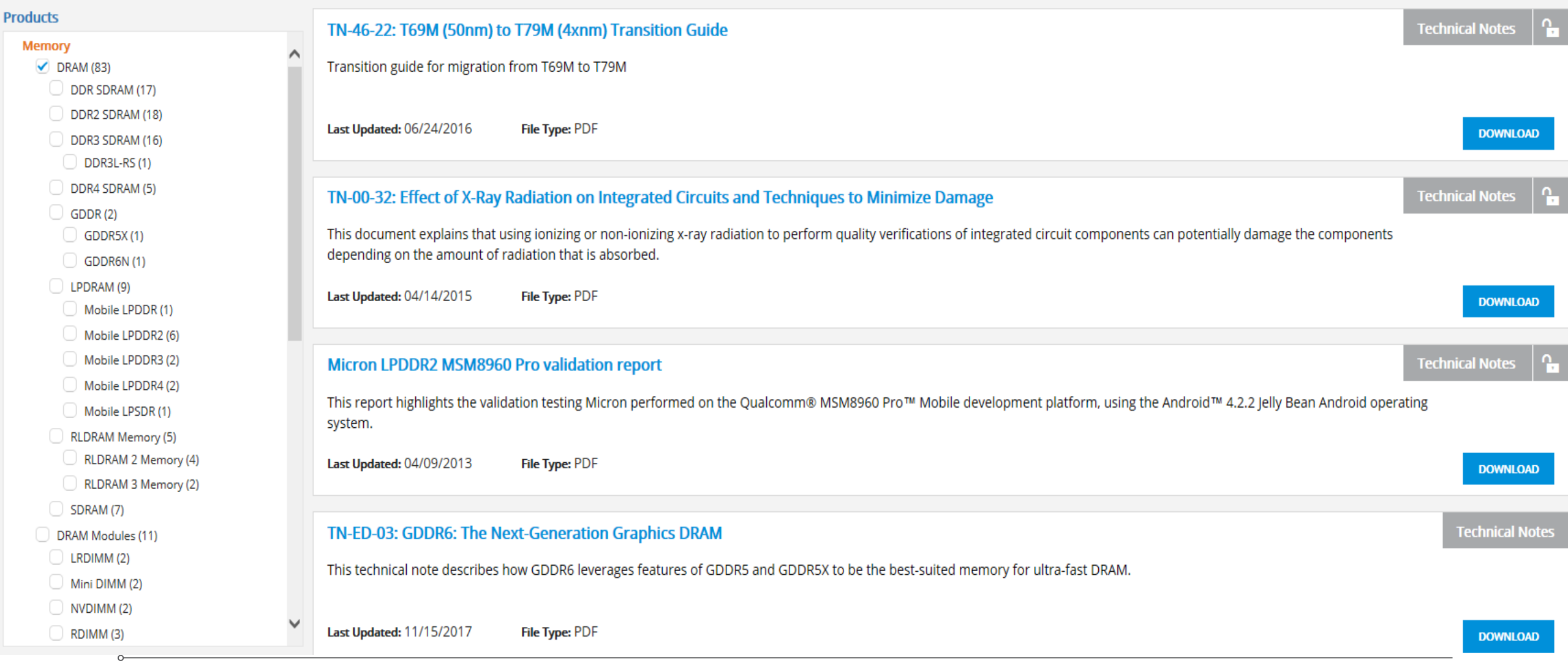
Download Calculator to Excel

- SDRAM System-Power Calculator*
- DDR SDRAM System-Power Calculator*
- DDR2 SDRAM System-Power Calculator*
- DDR3 SDRAM System-Power Calculator*
- DDR4 SDRAM System-Power Calculator*
- RLDRAM II Power Calculator*
- RLDRAM 3 Power Calculator*
- Mobile LPDDR2 System-Power Calculator* (Restricted Access)
- TN-52-01: LPDDR3 System Power Calculator* (Restricted Access)
- TN-53-01: LPDDR4 System Power Calculator* (Restricted Access)
- TN-53-07: LPDDR4X System Power Calculator* (Restricted Access)

*This spreadsheet is for estimating purposes only. Any information provided herein is provided "as is" and without warranties of any kind. Micron warrants only that its products comply with micron's specification sheet for the product at the time of delivery; provided that deviations from specifications which do not materially affect form, fit or function of such product in the system and configuration in or for which it is initially installed or qualified by customer shall not be deemed to constitute failure to comply with such specifications.

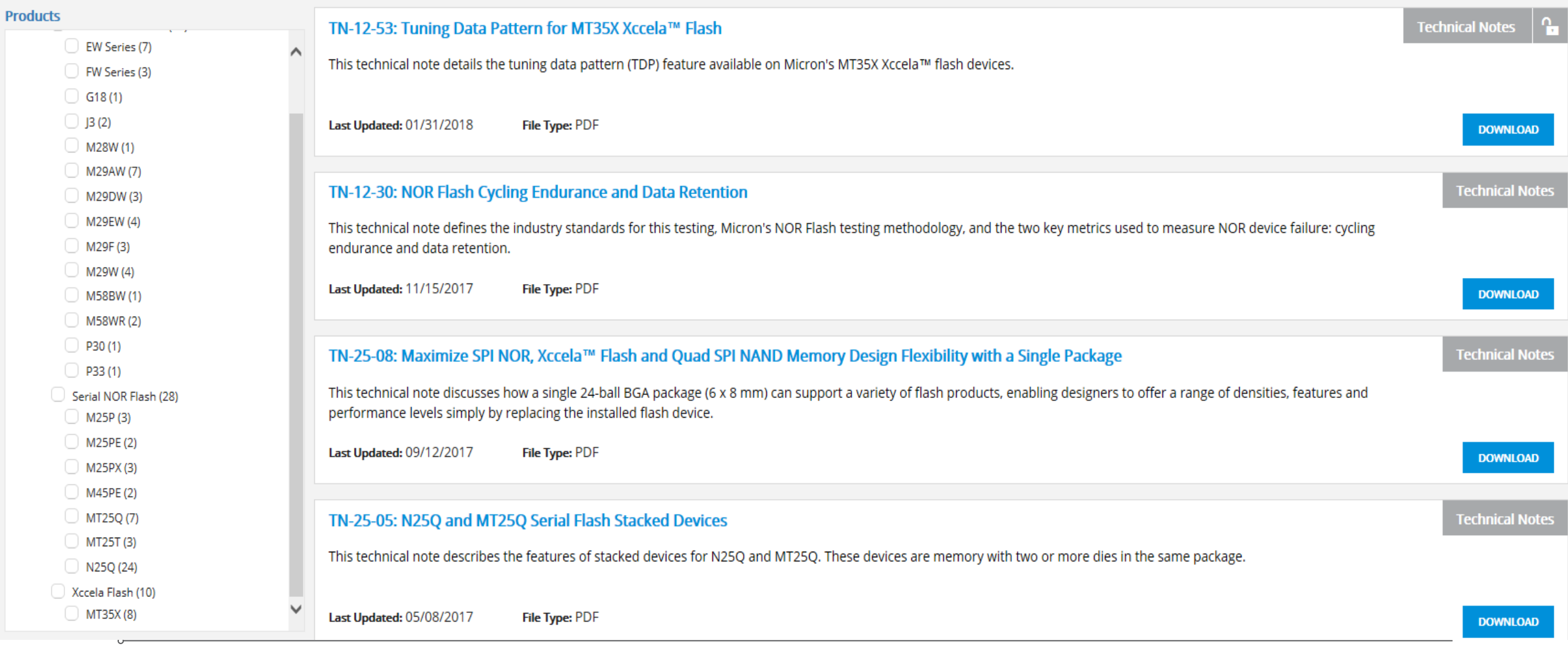
Link to Micron's DRAM Technical Notes:

- https://www.micron.com/advanced search?q=&page=1&site=0&within=productssupport&doc=False&sec=False&incl=False&sort=&show=10&family=2dd96f4ee22e4de7b7027e6dd6a2718c&new_document_type=5538556ed3e64d7195ce3986f06fbf34%7C5538556ed3e64d7195ce3986f06fbf34



Links to Micron's NOR Flash Technical Notes:

https://www.micron.com/advanced-search?q=&page=1&site=0&within=productssupport&doc=False&sec=False&incl=False&sort=date&show=10&family=1f8cfba0d95c4ea9a6c99e3272fd0e39&new_document_type=5538556ed3e64d7195ce3986f06fbf34%7C5538556ed3e64d7195ce3986f06fbf34



Link to Micron's e.MMC Technical Notes:

https://www.micron.com/advanced-search?q=&page=1&site=0&within=productssupport&doc=False&sec=False&incl=False&sort=date&show=10&family=ff04c268087d4d33a126d6a5a59ccebd&technology=9b8d2c45520a422c8f635832d3a2b0ea&new_document_type=5538556ed3e64d7195ce3986f06fbf34%7C5538556ed3e64d7195ce3986f06fbf34

Products

Memory
- [x] Managed NAND (10)
- [x] eMMC (10)

Solutions

By Industry
- [x] Automotive (10)
- [ ] Embedded (2)

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TN-FC-42: e.MMC Device Health Report 5.0 — Technical Notes

This technical note describes the device health report procedure for Micron Automotive 5.0 e.MMC™ Micron firmware.

Last Updated: 01/29/2018 **File Type:** PDF DOWNLOAD

TN-FC-47: e.MMC Data Removal — Technical Notes

This TN explains the commands used to remove data from an e.MMC device. All information applies to an automotive e.MMC with controller 5.0.

Last Updated: 06/29/2017 **File Type:** PDF DOWNLOAD

e.MMC Automotive 5.0 Cache Features — Technical Notes

This technical note introduces an optional cache feature available in the Micron automotive e.MMC 5.0 device.

Last Updated: 05/21/2017 **File Type:** PDF DOWNLOAD

TN-FC-54: Refresh Features for Micron e.MMC Automotive 5.0 Devices — Technical Notes

This technical note describes additional data refresh features available in Micron e.MMC automotive 5.0 devices built with Micron firmware.

Last Updated: 04/07/2017 **File Type:** PDF DOWNLOAD

TN-FC-46: Configure HS200 and HS400 mode in e.MMC memory — Technical Notes

This technical note describes how to configure the high-speed interface timing setting, HS200 and HS400, in e.MMC memory devices.

Last Updated: 03/02/2017 **File Type:** PDF DOWNLOAD

Link to Micron's SSD Technical Notes:

https://www.micron.com/advanced-search?q=&page=1&site=0&within=productssupport&doc=False&sec=False&incl=False&sort=date&show=10&family=59b6cc75486a4bca80f5b1b8a2086740&new_document_type=5538556ed3e64d7195ce3986f06fbf34%7C5538556ed3e64d7195ce3986f06fbf34

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TN-FD-40: 5200 SSD SMART Implementation — Technical Notes

This technical note provides the self-monitoring, analysis and reporting technology (SMART) command (B0h) feature set for the Micron® 5200 SSD.

Last Updated: 01/25/2018 **File Type:** PDF DOWNLOAD

TN-FD-34: 5100 SSD SMART Implementation — Technical Notes

This technical note provides the self-monitoring, analysis, and reporting technology (SMART) command feature set for MIcron 5100 SSD.

Last Updated: 12/05/2016 **File Type:** PDF DOWNLOAD

TN-FD-22: Client SATA SSD SMART Attribute Reference — Technical Notes

This technical note describes the SMART feature set available for Micron's client SATA SSDs.

Last Updated: 09/29/2016 **File Type:** PDF DOWNLOAD

TN-FD-24: M500IT SSD SMART Attributes — Technical Notes

This document describes the self-monitoring, analysis, and reporting technology (SMART) feature set

Last Updated: 06/08/2016 **File Type:** PDF DOWNLOAD

TN-FD-28: Installing Micron SEDs in Windows 8 and 10 — Technical Notes

This technical note describes the proper installation and operation of Windows BitLocker in hardware encryption mode.

Last Updated: 08/18/2015 **File Type:** PDF DOWNLOAD


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