SIMPLIFY YOUR INVERTER THROUGH ADVANCEMENTS IN IGBT GATE DRIVERS

AMF-AUT-T2371

KIM GAUEN

MC33GD3100 IGBT GATE DRIVER

06 OCTOBER, 2016

OUTLINE

IGBT/MOSFET CHARACTERISTICS

FEATURES OF AN IDEAL GATE DRIVE IC

MC33GD3100 OVERVIEW

SELECTING A GATE DRIVE POWER ARCHITECTURE

MINIMIZING SWITCHING LOSSES

PROTECTING THE IGBT

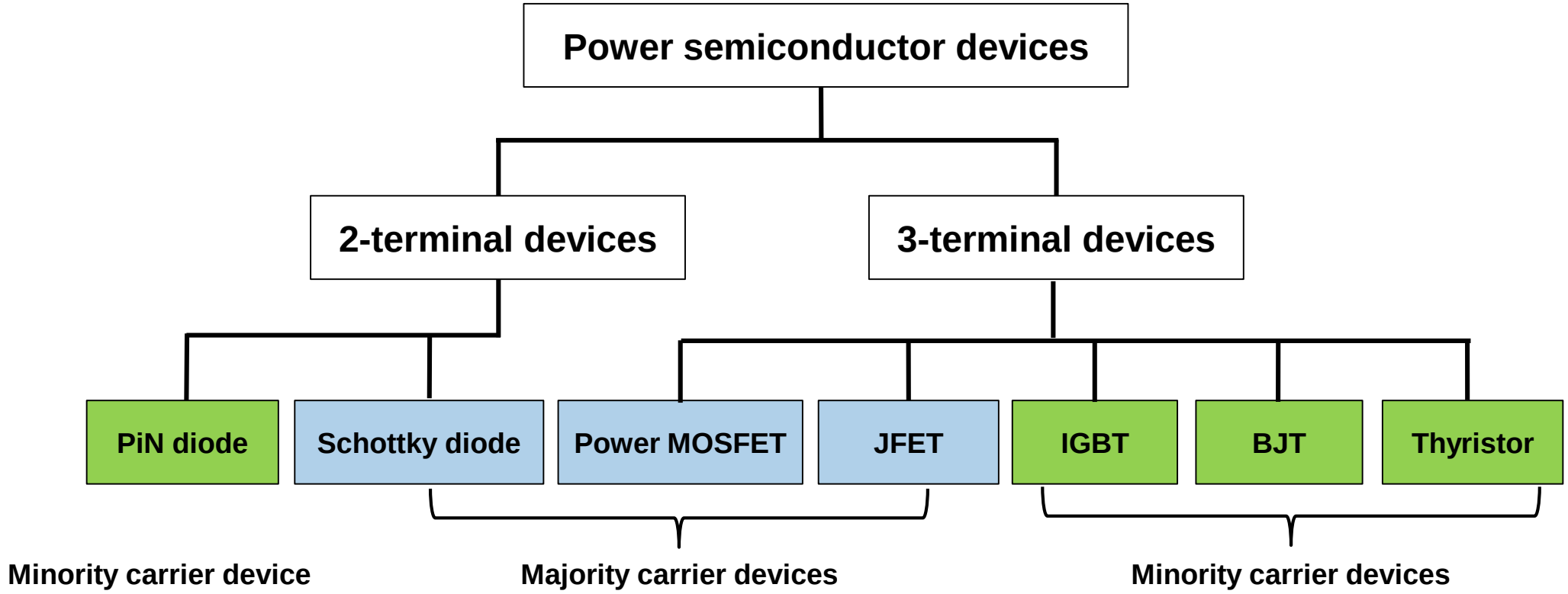
USE OF NEGATIVE GATE SUPPLY

REDUCING SYSTEM COST

ESTIMATING GATE DRIVE LOSSES

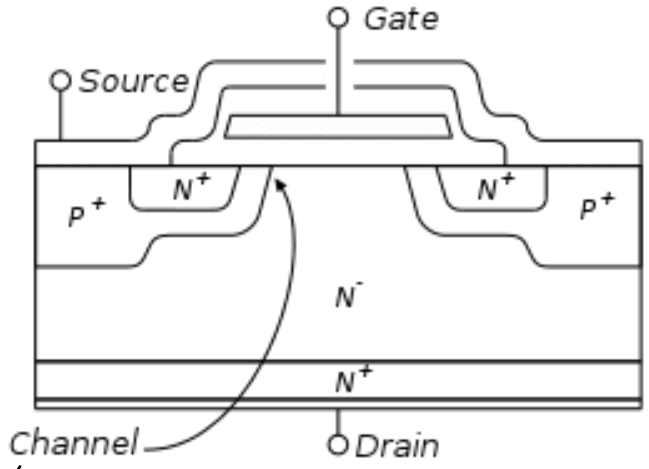
DESIGN SUPPORT

Power Semiconductor Families

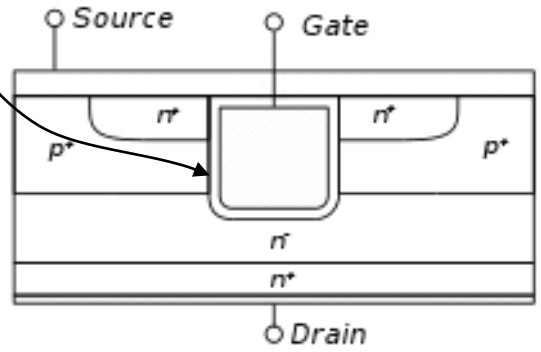


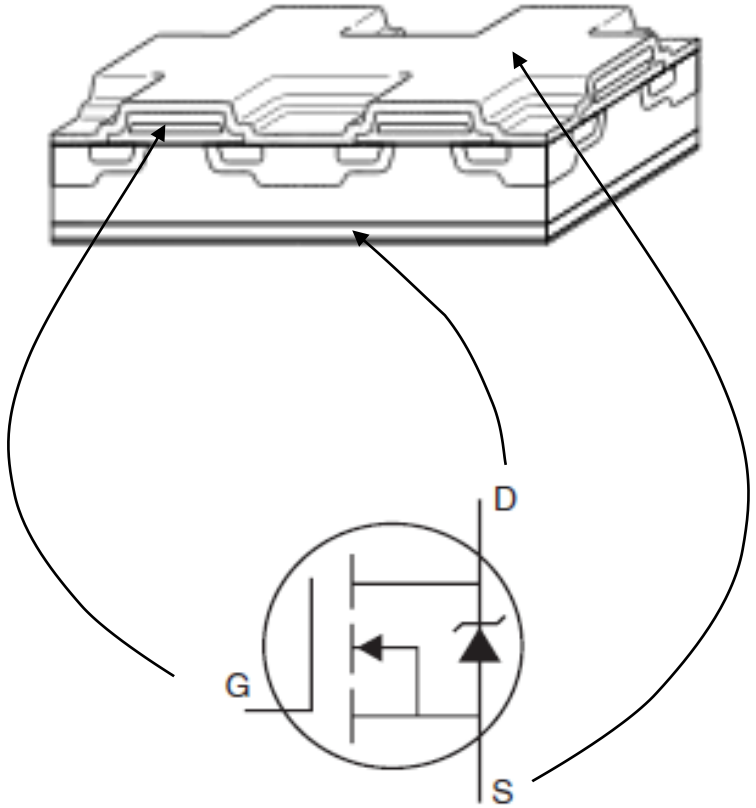
Vertical MOSFET Cross Sections & Symbol

“vertical” power MOSFET

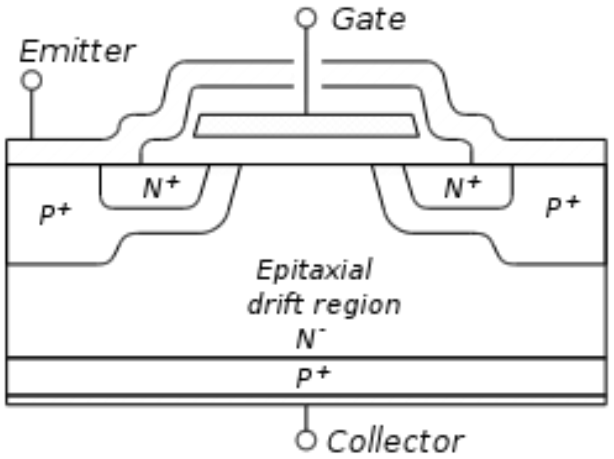


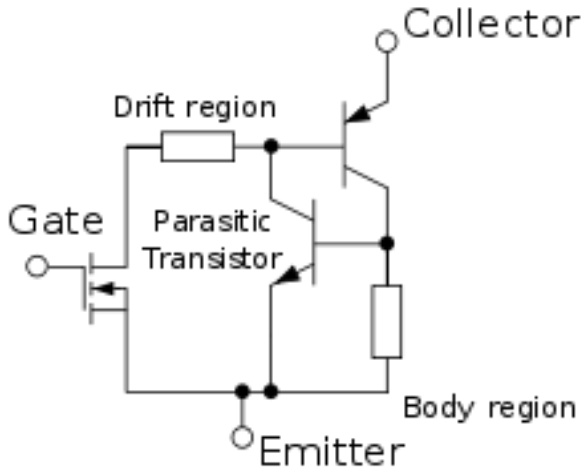
“Trench” power MOSFET

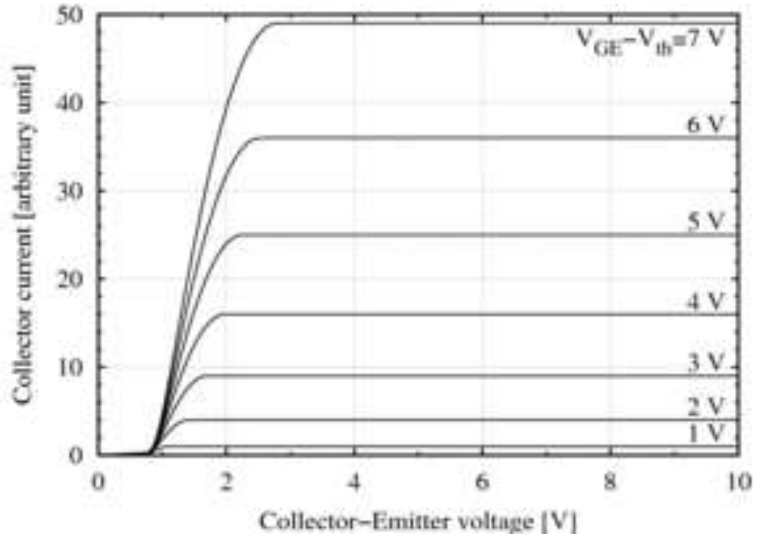




IGBT Cross Section, Equivalent Circuit & Output Characteristics

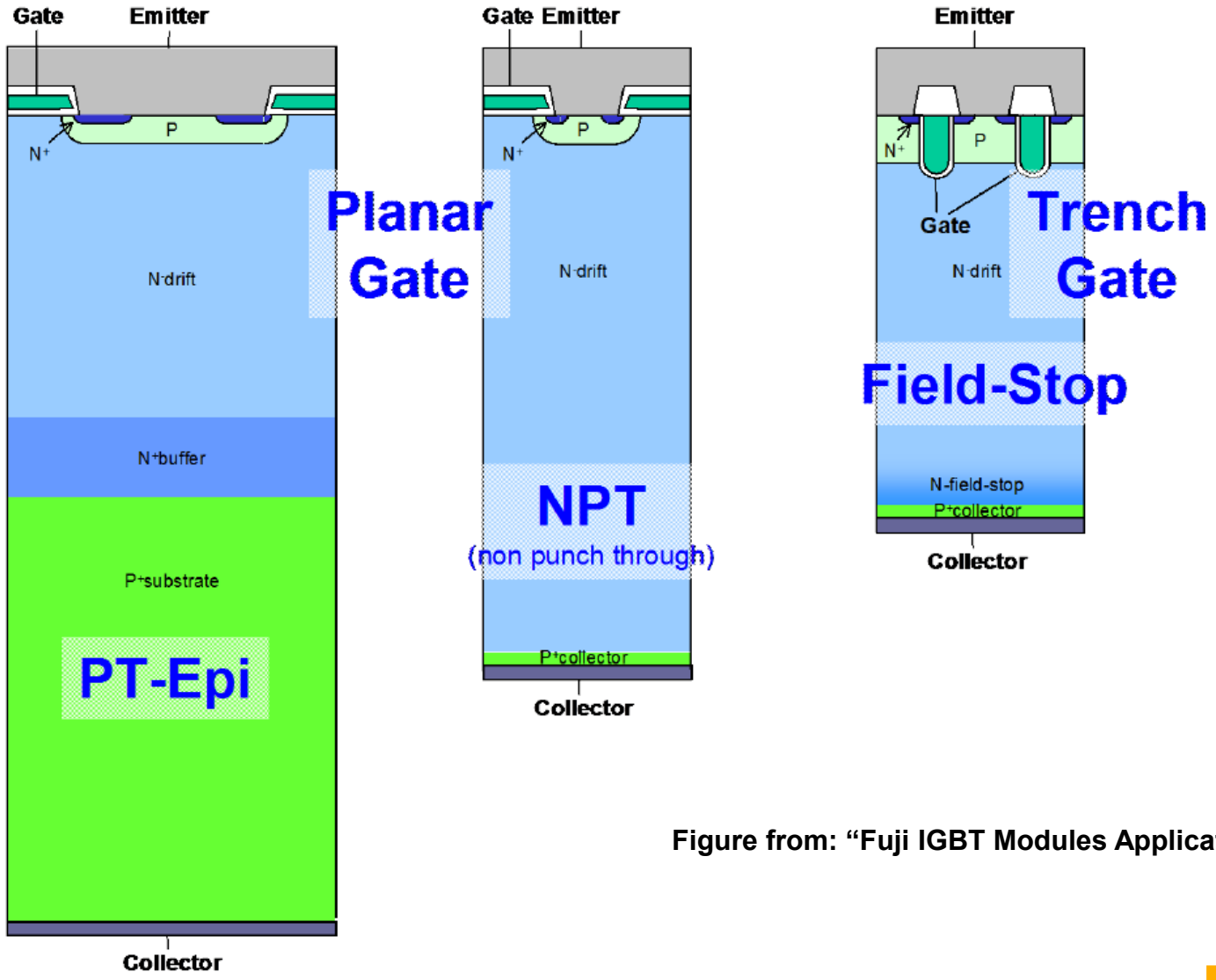






Effect of IGBT Technology Trends

- Inverter costs must be reduced
- IGBT is a prime contributor to inverter cost
- IGBT die size must be reduced to reduce module cost & size
- Reduced IGBT die size increases power density during faults
- Increased power density requires faster protection



(a) Punch Through type (b) Non Punch Through type (c) Field Stop type

Figure from: "Fuji IGBT Modules Application Manual"

IGBT and MOSFET Comparison Summary

- IGBTs and MOSFETs are “isolated gate” controlled and behave similarly.
- IGBT uses minority (vs. majority) carriers to conduct current
- Stored charge creates turn off tail (and losses)
- IGBT switching behavior changes with junction temperature
- Minority carriers improve (increase) current density
- IGBT is more prone to latch-up due to 4 layer structure; may have additional SOA restrictions
- gfs (gain) is higher, increasing short circuit current for a given gate voltage
- Power density is greater during a short circuit fault
- Isolated gate allows predicting gate drive power
- IGBTs lack an integrated body diode – except for new “reverse conduction” IGBTs

Key IGBT Characteristics Curves and Specifications

- Output characteristics
- Transfer (or transconductance) characteristics
- Gate charge characteristics
- Safe Operating Area curves
- Package inductance, especially “common emitter inductance”
- Switching losses vs. gate resistance
- Diode on-voltage and reverse recovery characteristics
- Internal gate resistance

IGBT Output Characteristics Curves

$V_{ce(on)}$ variation with $V_{ge(on)}$

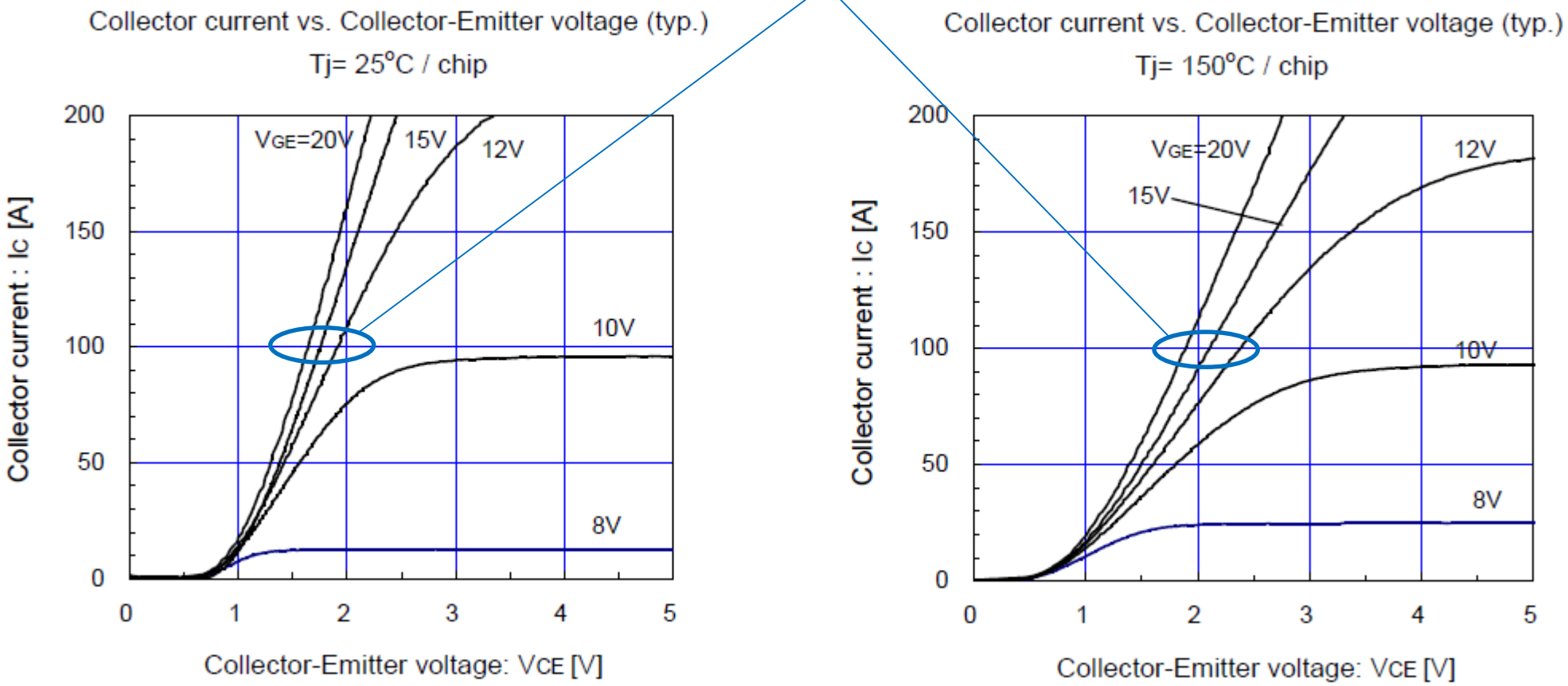
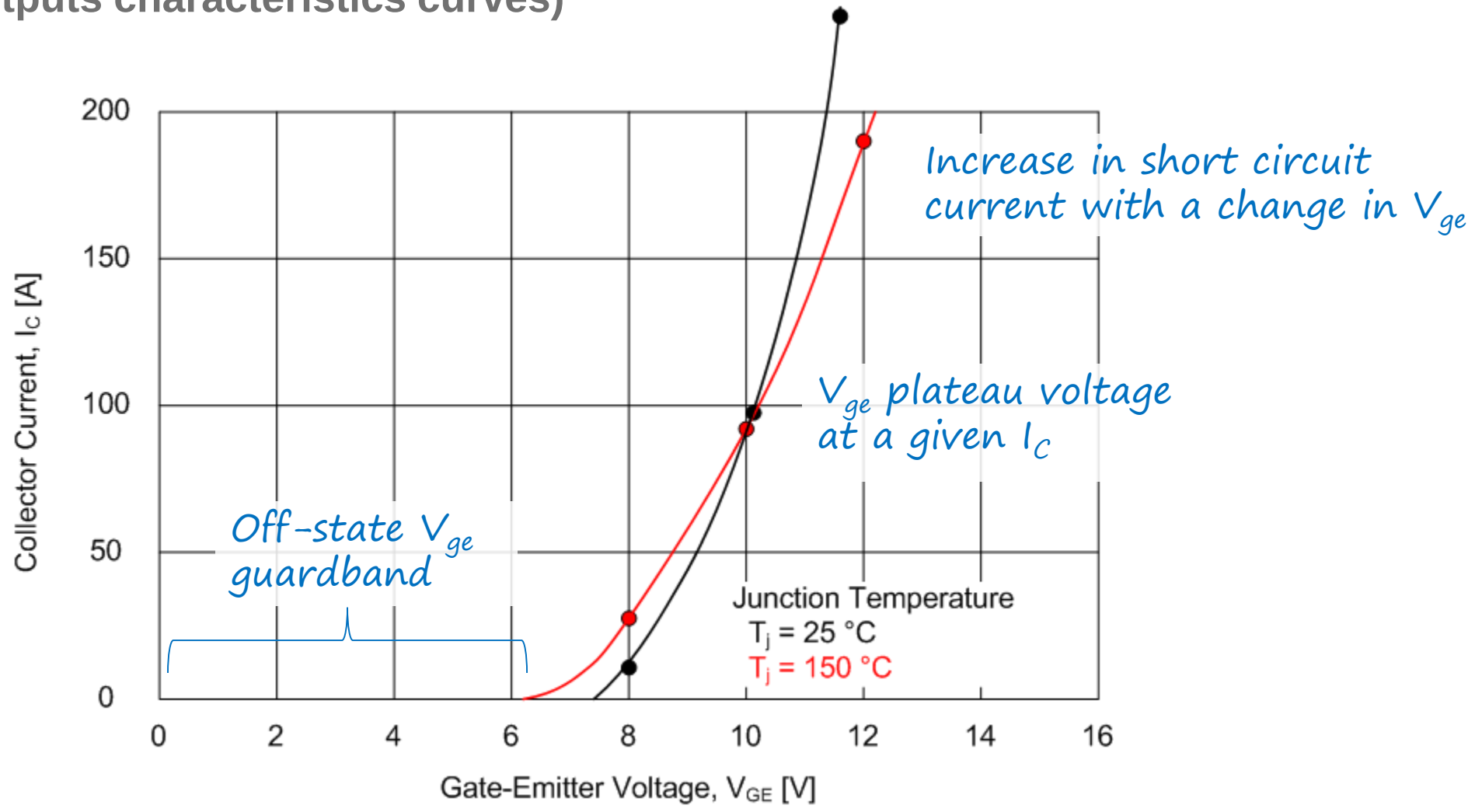


Figure from: "Fuji IGBT Modules Application Manual"

IGBT Transfer Characteristics Curves

(estimated from outputs characteristics curves)



IGBT Gate Charge Curves

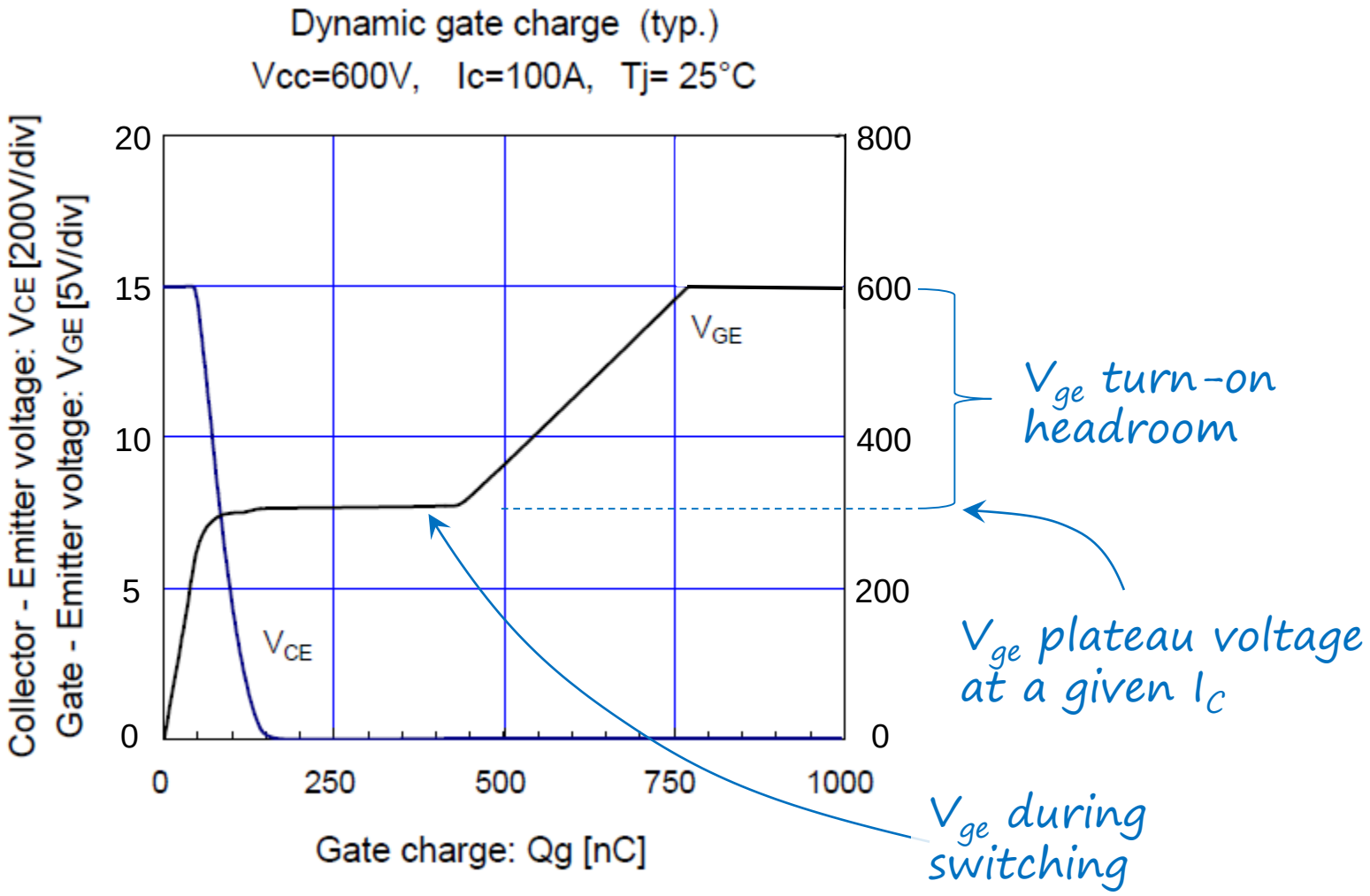


Figure from: "Fuji IGBT Modules Application Manual"

IGBT Gate Charge Curves (cont)

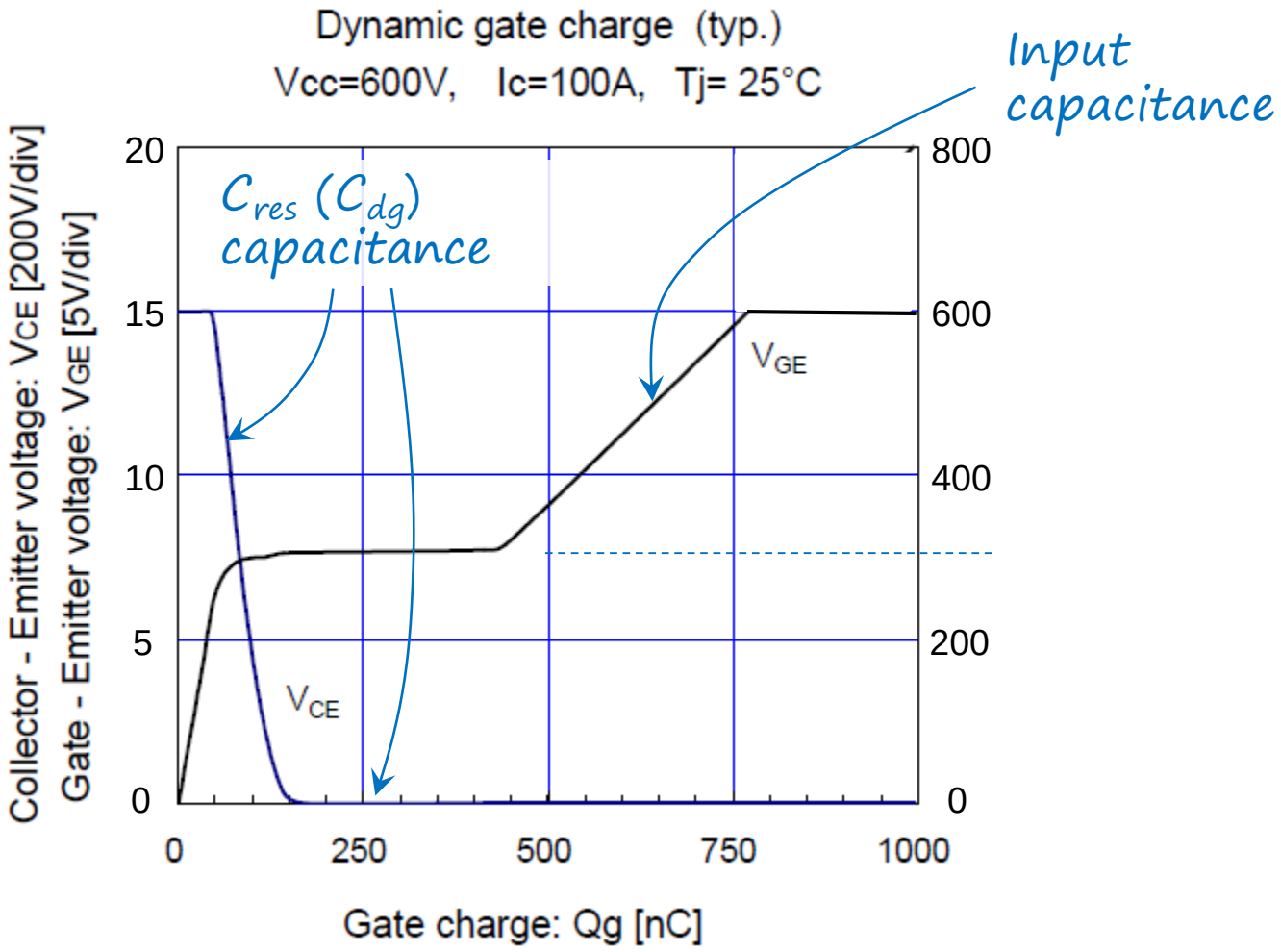
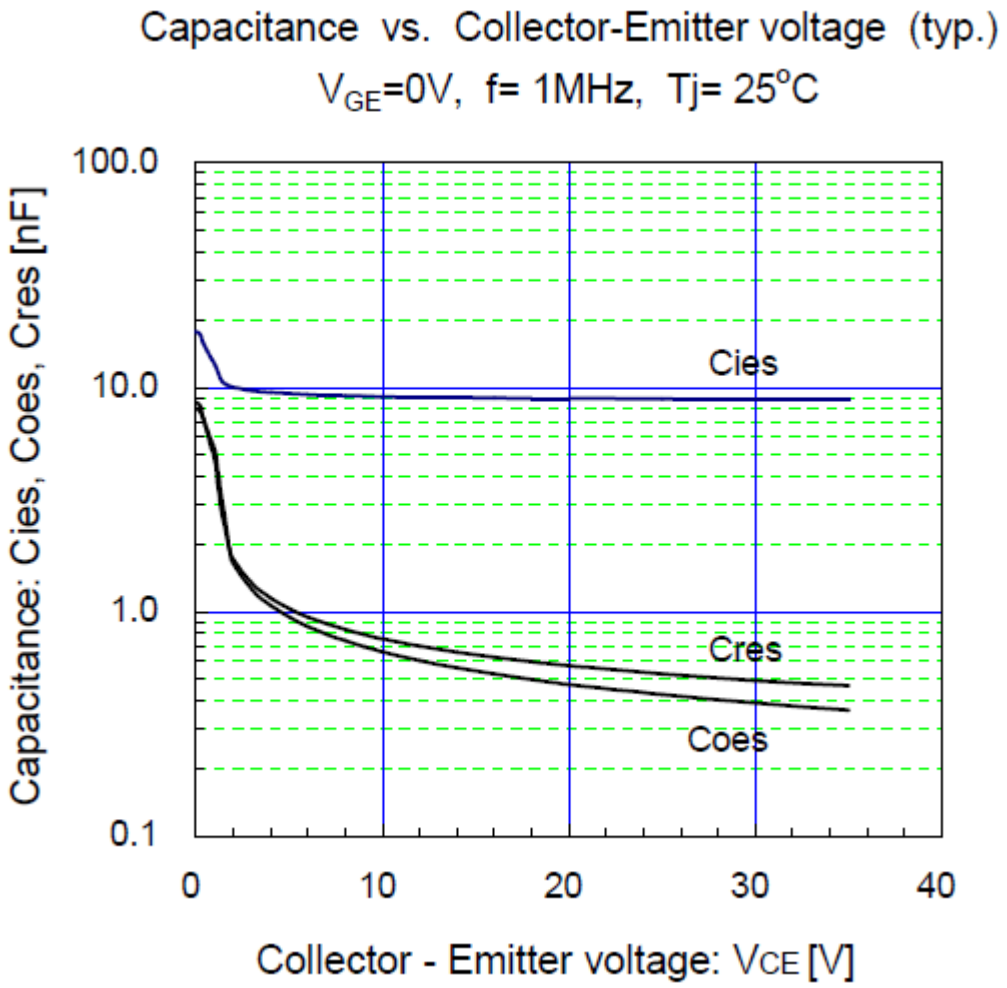
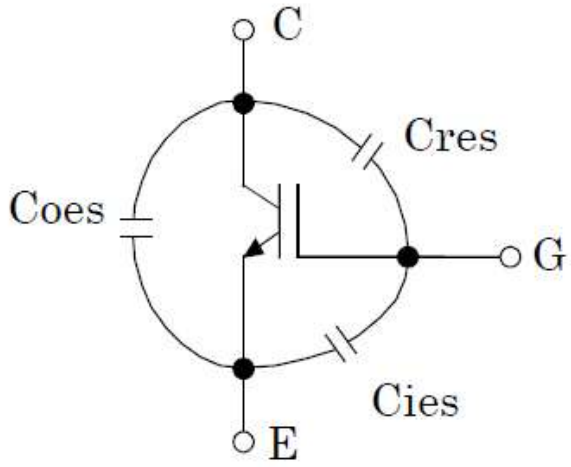


Figure from: "Fuji IGBT Modules Application Manual"

Input and Output Capacitances

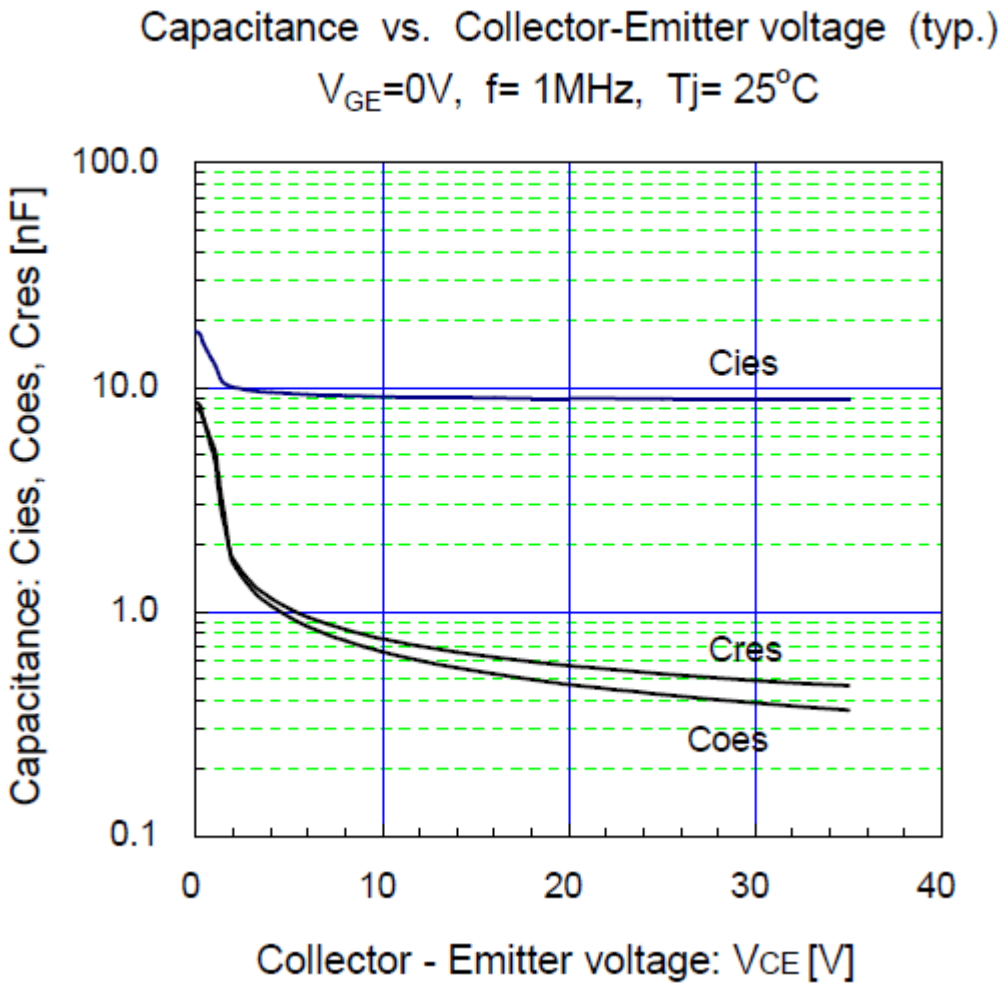




The traditional C-V curves do not show the value of C_{res} (C_{cg}) when the IGBT is on.

Figure from: "Fuji IGBT Modules Application Manual"

Input and Output Capacitances



Expanded MOSFET C-V curve shows behavior when MOSFET is on.

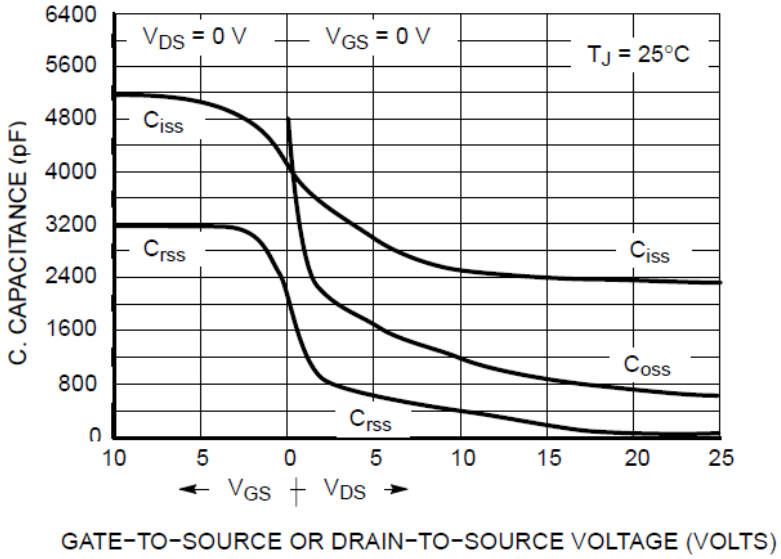
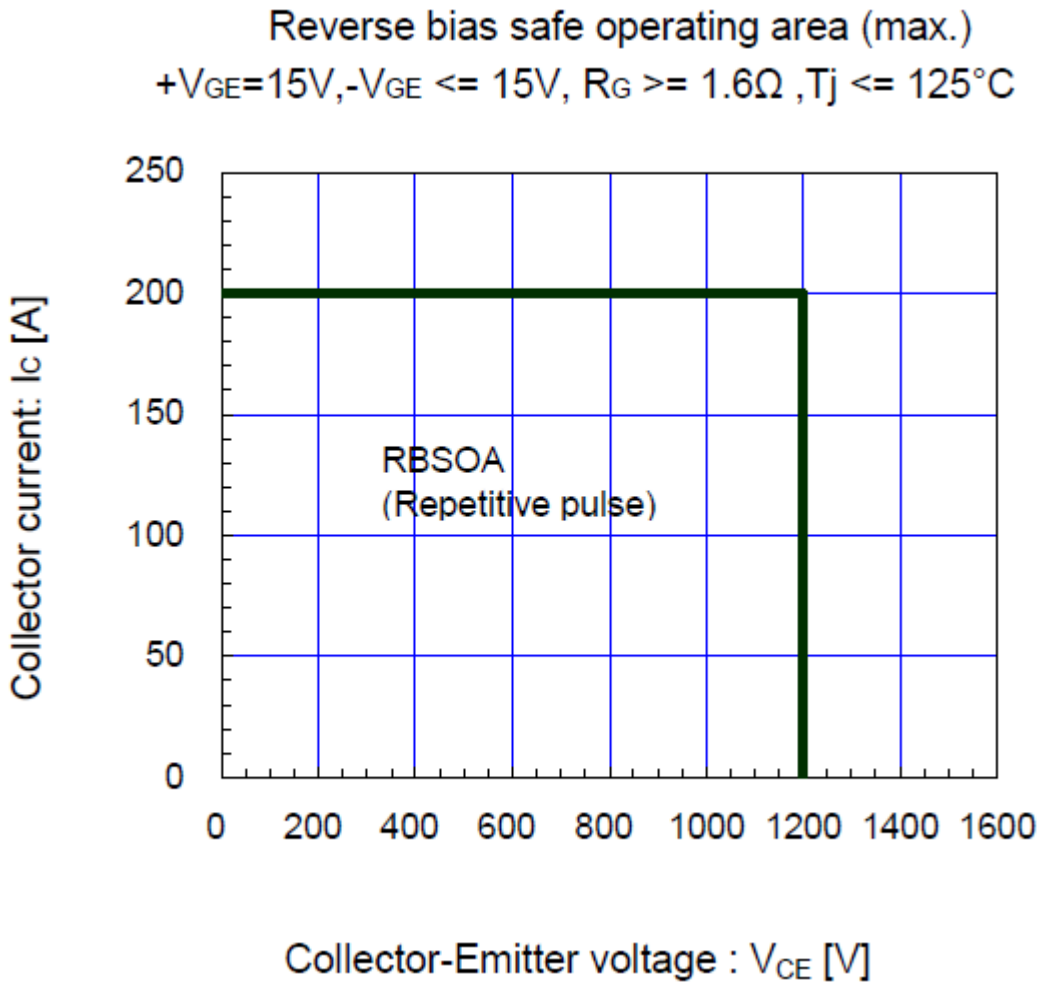


Figure from: "Fuji IGBT Modules Application Manual"

Safe Operating Areas

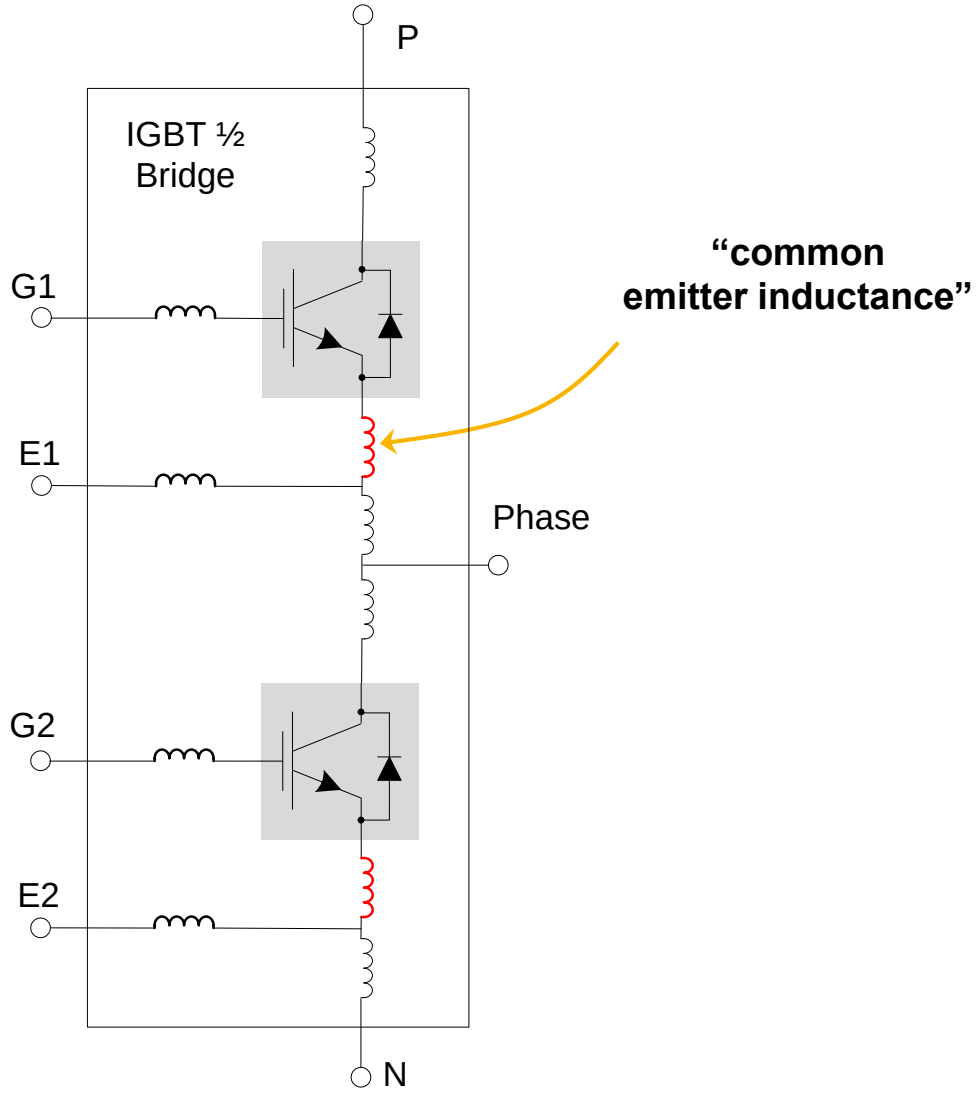


Short Circuit SOA (SCSOA) or a single pulse energy specification may also be provided.
Strict $V_{ce(max)}$ limit is common.

Figure from: "Fuji IGBT Modules Application Manual"

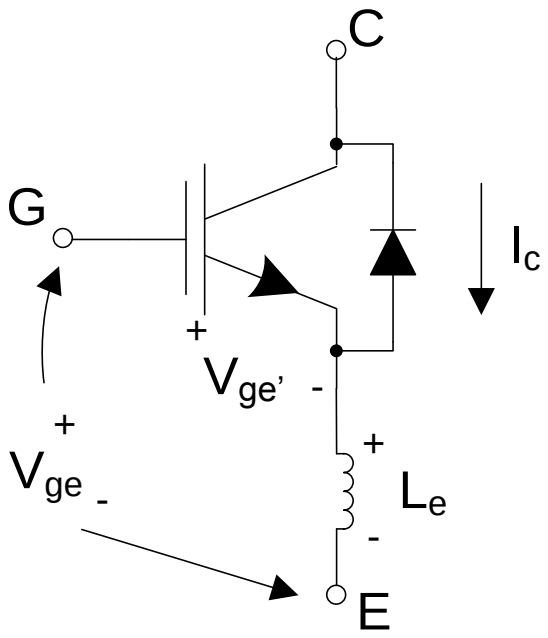
IGBT Module Inductances

- Inductance specifications vary widely
- Emitter & collector inductances greatly affect switching behavior and peak V_{ce} at the terminals and the die.
- “Common emitter inductance” greatly affects switching speed
- Gate inductances create noise and degrade & complicate gate-emitter monitoring and control
- Inductances vary from die-to-die for paralleled die



Effect of “Common Emitter Inductance”

- L_e conducts gate current and collector current
- Induced V_{Le} polarity detracts from the desire change in V_{ge}, slowing turn on and turn off



$V_{Le} = L_e * \Delta I_c / \Delta t$

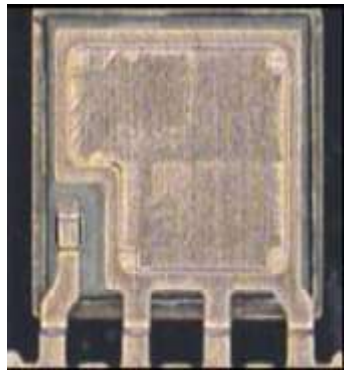
For example: 1 nH * 1 A / ns → 1 V
Target di/dt may be > 5 A / ns

$V_{ge'} = V_{ge} - V_{Le}$

Advances in D2PAK Internal Wirebonding

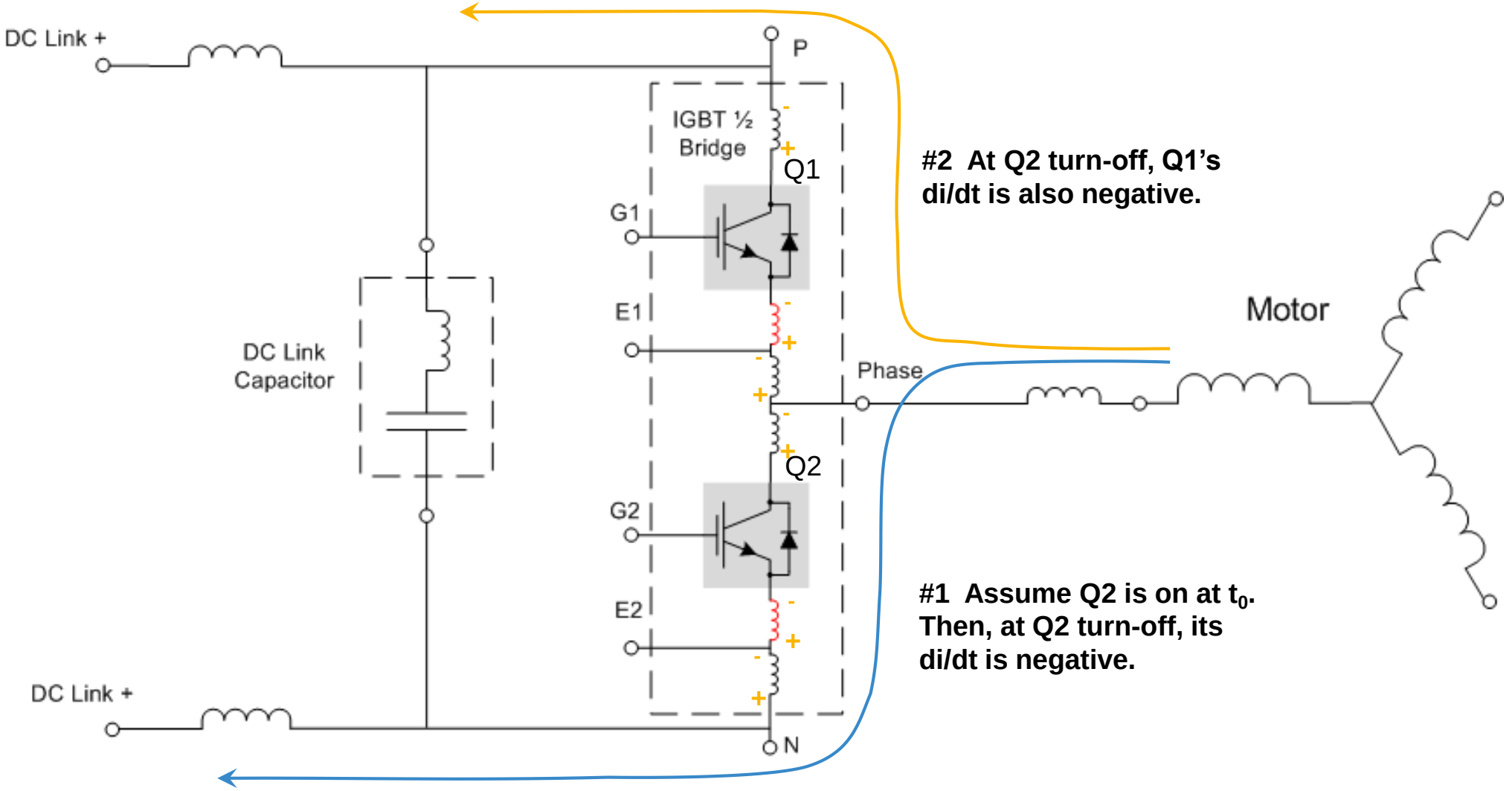
- Efforts to maximize source current capacity also tend to minimize source inductance
- The same practices are applicable to PCB layout, i.e., you should minimize common source/emitter inductance

Multiple source wirebonds

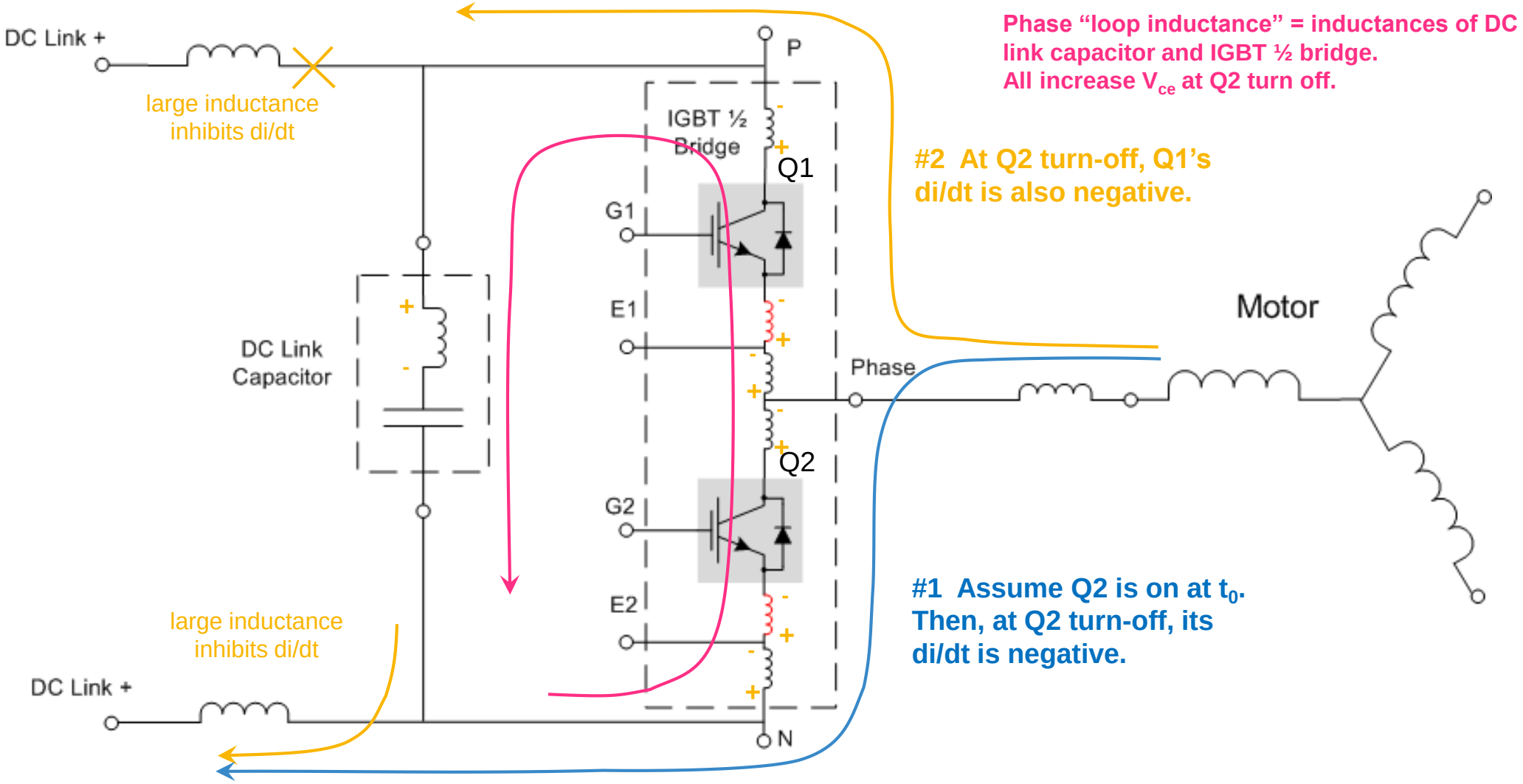


Topside copper clip

Half Bridge Connection to Motor



Half Bridge Connection to Motor (cont)



Phase "loop inductance" = inductances of DC link capacitor and IGBT ½ bridge.
All increase V_{ce} at Q2 turn off.

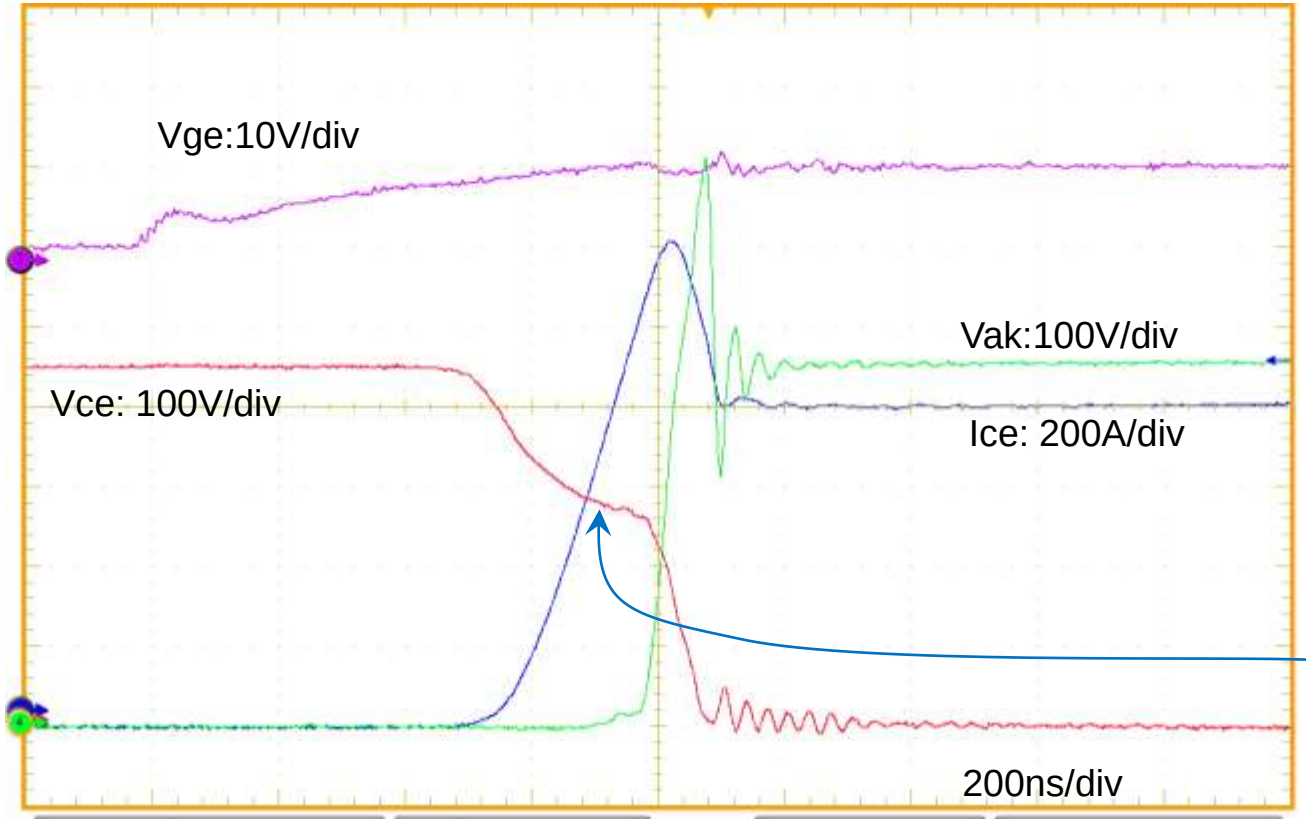
#2 At Q2 turn-off, Q1's di/dt is also negative.

#1 Assume Q2 is on at t_0. Then, at Q2 turn-off, its di/dt is negative.

Turn on at Cold Temperature (Tested at Fuji)

T_{IGBT} = ⁻40°C, 450V/800A

$R_{gon/off}$ = 7.4Ω/1.2 Ω, C_{ge}= 0.015µF, VEE = 0V



Loop inductance causes V_{ce} droop at turn on – and V_{ce} overshoot at turn off

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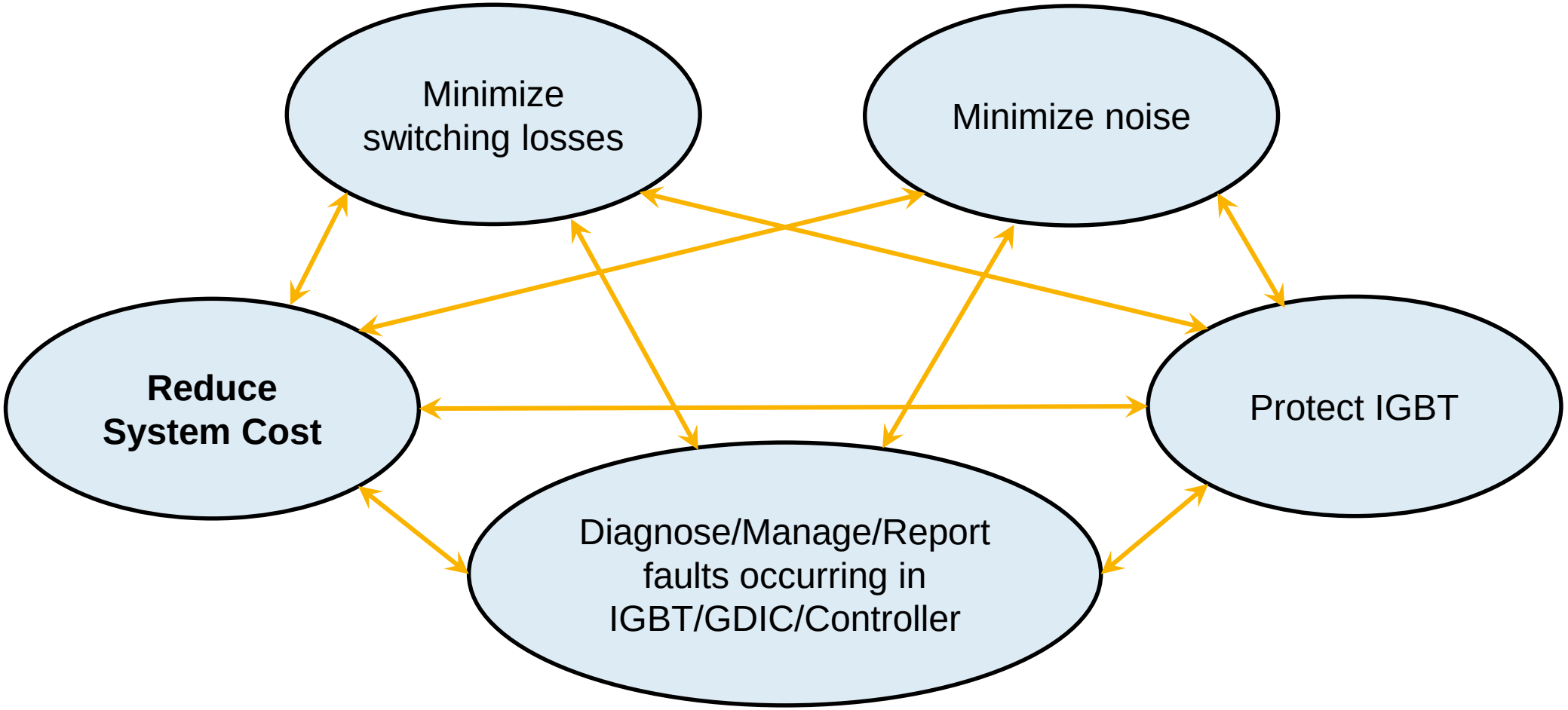
DESIGN SUPPORT

Key Requirements of an Ideal Gate Drive IC

- Most gate drive IC features affect multiple system requirements



Primary Considerations

- **#1 – Minimizing system cost, where possible, but especially IGBT's cost**
- The focus is on reducing cost of the highest cost system components, if at all possible. Since the GD3100 controls the (expensive) IGBT, there are several ways it can reduce the IGBT's cost. Having high speed protection for the emerging generation of IGBTs is especially important. The GD3100 also affects complexity of the required safing circuitry, overall inverter efficiency, gate drive power supply components, PCB area, heat generated in the IGBTs, etc. All these contribute to system cost.

- **#2 – Meet ISO 26262 ASIL-D safety metrics**
- This is an emerging standard that will likely be required by most systems. Compliance enhances the IC even when ISO 26262 is not required.

- **#3 – Minimize required PCB area**
- As the IGBT modules size decreases and the diagnostic and safety requirements increase, the gate drive board area allotted to the drive circuit is reduced.

- **#4 - Minimize power dissipation on the gate drive board PCB**

- **#5 – Design Flexibility and Reuse**
- In order to reduce engineering costs, the GD3100 was designed to be compatible with IGBTs that have (or do not have) a current sense pin, a collector voltage sense pin, on-die temperature sensing, etc. The GD3100 is has extensive programmability of the protection and diagnostics features.

Minimizing System Cost

- To minimize the cost of the IGBT module, the IGBT die size and the IGBT module size must be reduced. Consequently, current density in the IGBT die increases with each new generation. Transconductance of the newer IGBTs is also increasing. This increases fault current magnitude, further increasing SOA stress during a short circuit fault. This mandates that the gate drive's short circuit protection be improved with each new generation to allow the use of the new IGBT die technology. The GD3100 monitors the ISENSE pin of current sense IGBTs to improve the SC response. Two Level Turn Off is used to reduce V_{ge} during a fault and thereby reduce peak fault current. Soft shutdown can be used to gently turn off the gate once the fault is validated.

- Monitoring the IGBT's die temperature provides a more accurate sensing than using a temperature sensor in the coolant or on the IGBT's baseplate. The more accurate temperature reading may allow safely extending the inverter power output during high power or high temperature conditions.

- Integrating the gate driver transistors not only saves component cost and PCB area, it also provides direct and independent control of the charging and discharging paths. Protection delay times are minimized; the gate voltage is more closely monitored. Rail-to-rail control more accurately determines the on-state voltage, and the off state voltage is pulled to the negative supply (and not a diode drop above it).

Minimizing System Cost (cont.)

- VCCREG post regulator minimizes the variation of on-state gate voltage. This also minimizes the peak collector current during a short circuit (for each 1 V increase in the gate voltage, the short circuit fault current can be hundreds of amperes greater).

- Active Miller Clamp feature minimizes system cost in several ways. It improves the IGBT's immunity to dv/dt induced turn on. A dedicated AMC pin (with no external series resistance to the IGBT gate) often allows designers to omit the negative gate drive supply that is otherwise often needed. Omitting the supply saves PCB area and eliminates a few components, but more importantly it saves the gate drive losses associated with a negative supply. The extra gate power is about 30% when a negative supply is used. This increases heat on the gate drive board and requires a larger gate drive power supply.

- The AMUXIN pin, working with the AOUT pin, provides a duty cycle encoded signal representing the IGBT temperature, the gate supply voltage, or the voltage at the AMUXIN pin. These features can eliminate the component cost and board area otherwise need to provide feedback from the HV domain.

- The failsafe pins, FSENB and FSSTATE integrate some of the failsafe control circuitry.

- The PWMALT pin integrates protection circuitry otherwise required for deadtime enforcement and cross conduction protection.

- The CLAMP pin reduces the size and cost of the collector-to-gate zener (if used). It also reduces the variation of the clamp voltage and thereby reduces the peak voltage at the IGBT's collector. Again, this affects an IGBT feature: maximum voltage rating.

ISO 26262 Features

- ISO 26262 is an emerging standard that will likely be required in most systems. Compliance enhances the IC even when ISO 26262 is not required.

- Features included for compliance:
  - FSENB and FSSTATE pins to interface with Safing Logic (Torque Security)
  - HV domain failsafe input
  - Safe SPI Configuration Mode
  - Framing error detection and 8-bit CRC to ensure error free SPI communications
  - Ability to read all programmed SPI registers
  - All key safety functions tested on demand
  - BIST (analog and logic) checks on demand
  - IGBT on/off state validation
  - Integrated deadtime enforcement via the PWMALT pin
  - Continuous monitoring of die to die communications link
  - Continuous monitoring of power supplies
  - Monitoring CRC of programmed registers
  - Uninterrupted gate control during power up/down
  - Rapid short circuit shutdown to minimize IGBT stress
  - Input logic pins tolerant to 18 V
  - Redundant LV & HV grounds and VEE pins
  - Design and documentation process meets ISO26262 requirements

Minimize Required PCB area

Reducing the PCB area needed for the gate drive IC is mandatory due to decreasing IGBT module dimensions.

The GD3100 reduces the required area by:

- Eliminating the requirement for the negative gate drive supply
- Integrating the Galvanic isolation
- Integrating the gate drive transistors
- Integrating the deadtime enforcement, cross conduction protection, and failsafe logic
- Post regulating the gate power supply. This feature allows combining power supply outputs onto fewer transformer cores (the post regulator can reduce the output-to-output voltage variation. This not only reduces PCB area, it reduces the number of components that span the galvanic isolation barrier.
- If the ISENSE pin is available, the need for Vce active clamping is reduced (because the peak fault current can be lower). Eliminating the active clamping zeners and associated diodes saves significant area and cost.

Minimize power dissipation on the gate drive board PCB

The primary source of power dissipation on the gate drive board is associated with charging/discharging the IGBT’s gate and the power supplies providing the power.

- Because the GD3100 can help eliminate/reduce the negative gate drive voltage, the gate drive losses can be reduced. The lower power requirement reduces the size of the gate drive power supplies.

Design Flexibility and Reuse

- The type/generation/size/pinout/features of IGBTs varies widely. Often the response of the gate drive must be tuned to optimize performance of a given IGBT. Having a flexible and configurable gate driver allows optimizing IGBT performance, regardless of the IGBT chosen.
- LV domain can be powered by VBATT or a 5 V supply. The power supply architecture may change with the safing strategy (how or if the GD3100 is powered during a loss of battery, for example.
- Use of the HV domain post regulator is optional
- The GD3100 has the features needed to control IGBTs with or without an ISENSE pin.
- PMW deadtime, operating modes and fault masks, Vce desaturation thresholds and filter times, Ic short circuit and over current thresholds and filter times, VCC under voltage threshold, IGBT over temperature and over temperature warning thresholds, two level turn off voltage, soft shut down current, etc. are programmable.
- The GD3100 is compatible with failsafe management from the LV or HV domain.

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GD3100 Overview

Advanced gate driver for high voltage power IGBTs with integrated high voltage isolator. New current sense features minimize short circuit stress & reduce IGBT die size.

Differentiation:

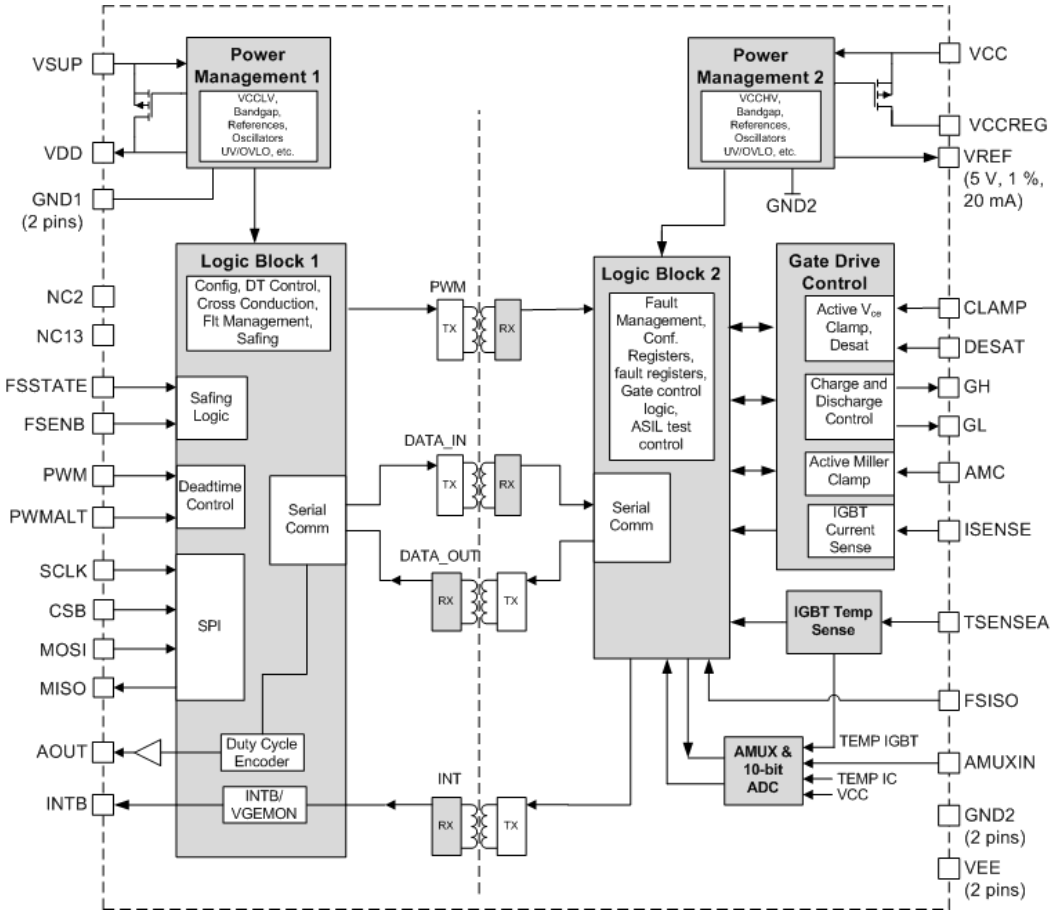
- SPI interface for ASIL D monitor and reporting, device programmability and flexibility
- Fast short circuit protection via direct feedback through i-sense IGBTs
- High speed over current protection with soft shutdown
- Integrated temperature sense for system warning and ultimately soft shutdown for system protection
- Integrated galvanic signal isolation between the low-voltage drive electronics and the high-voltage power electronics in single package to reduce PCB area

Features:

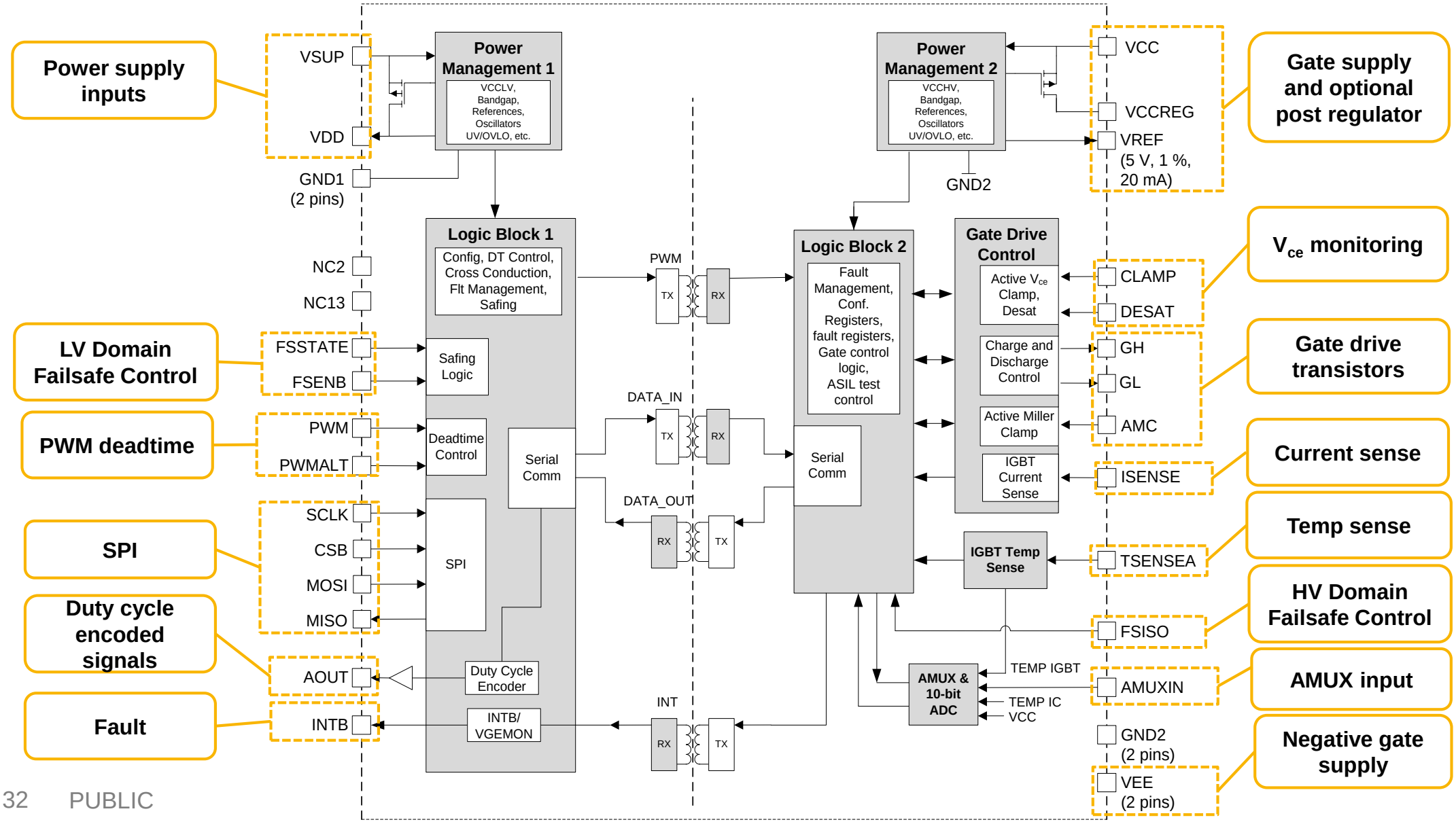
- Integrated high voltage electrical isolation between the low-voltage drive electronics and the high-voltage power electronics in a single package; for bidirectional signal transmission
- Compliant with ASIL D functional safety requirements (ISO 26262).
- SPI for configurability and for providing detailed fault & status data for integrated protection and programmability
- High speed over current protection with soft shutdown
- Isolated AMUX for monitoring key circuit voltages and currents
- Gate-emitter clamp eliminates the need for negative gate supply voltage
- Integrated gate drive power stage capable of 10A source and sink
- Compatible with 200V to 1700V IGBTs, power range >125kW

32-Pin
SOIC-WB

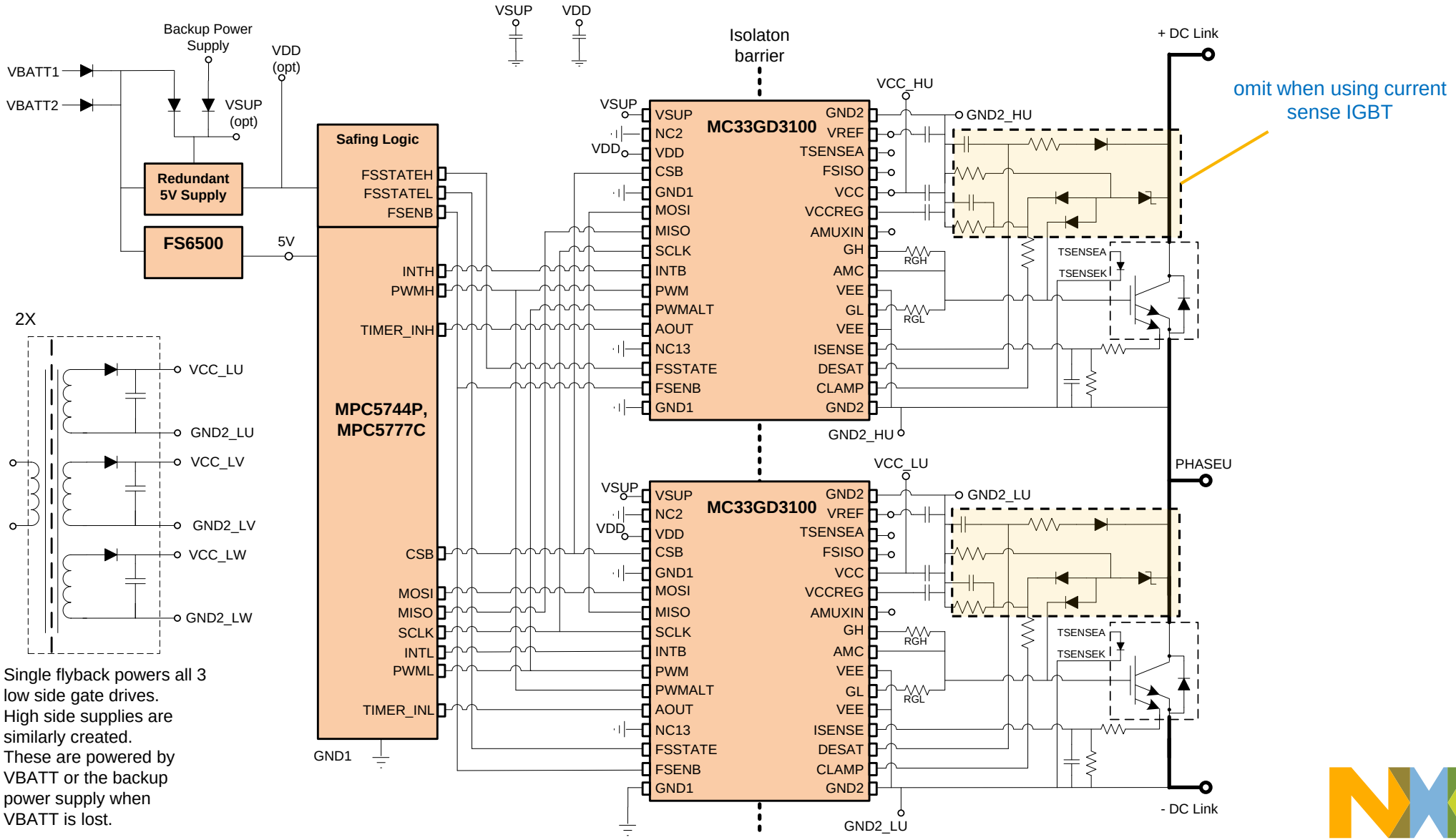
PART #	PKG	SAMPLES	RELEASE
MC33HB3100EK	SOICWB32	NOW (Pass 0.3)	Q1'18



Block diagram and pinout



High Voltage Inverter Schematic



Single flyback powers all 3 low side gate drives.
High side supplies are similarly created.
These are powered by VBATT or the backup power supply when VBATT is lost.

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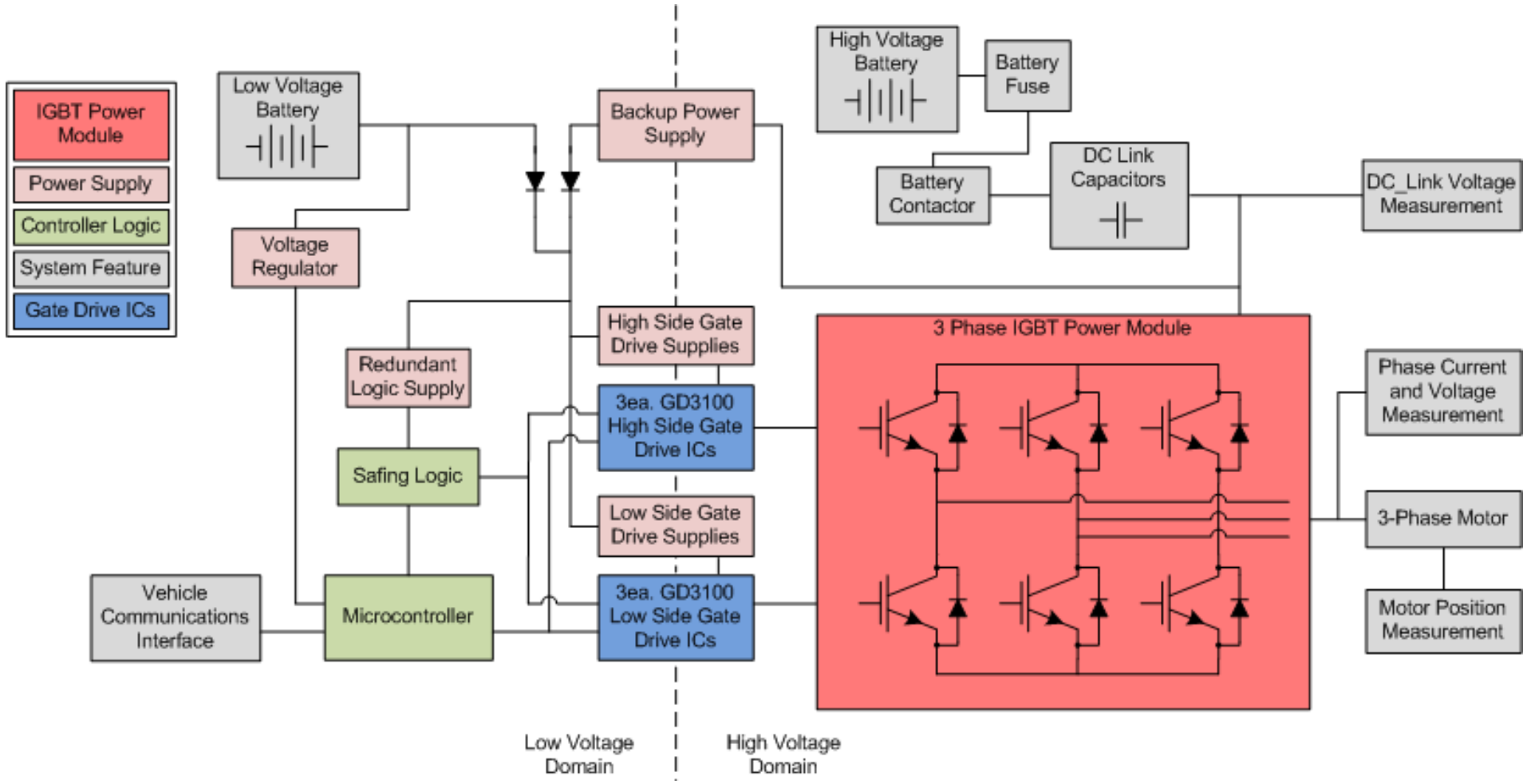
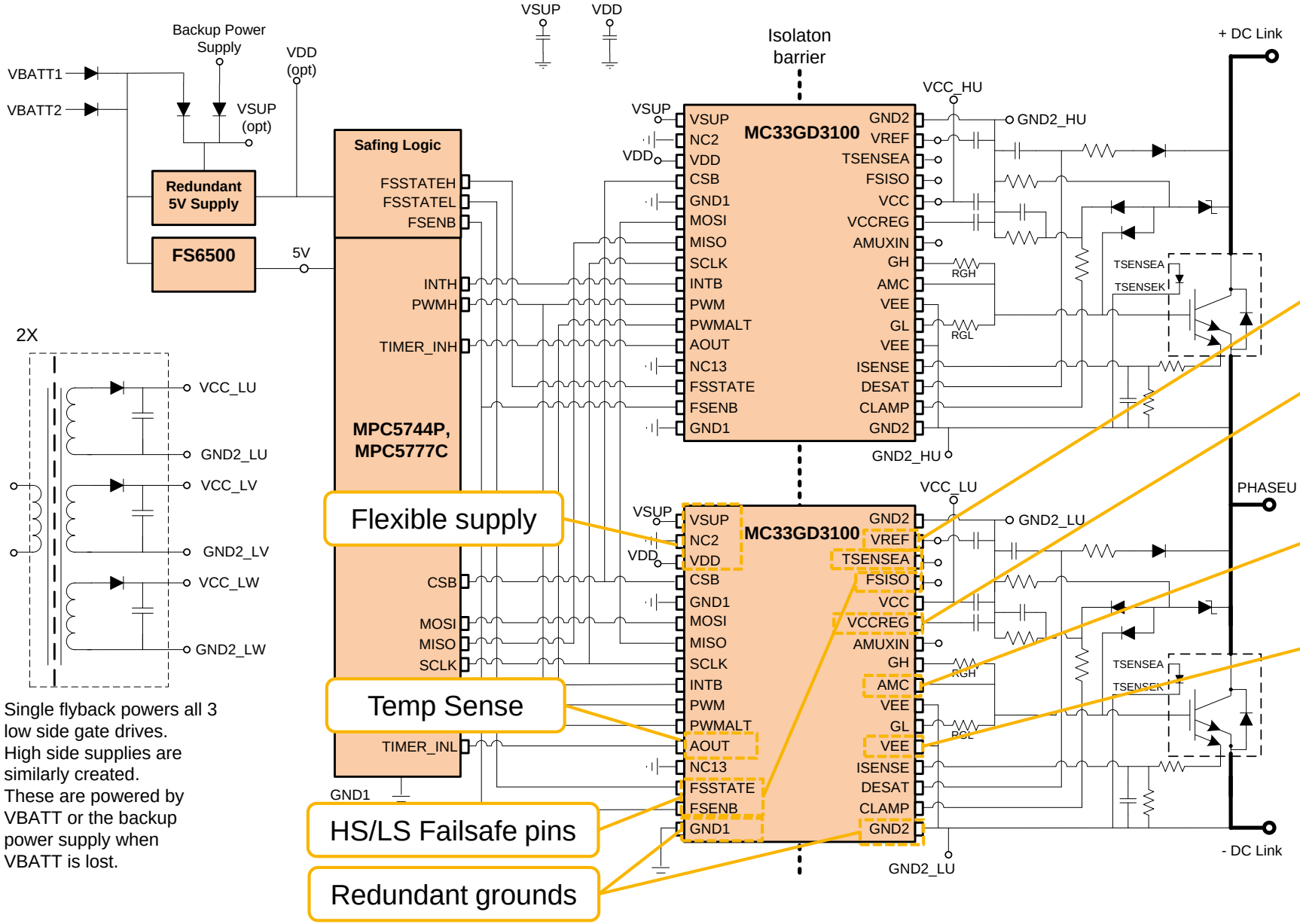
Power Supply Architecture



Features Related to Power Supply Architecture



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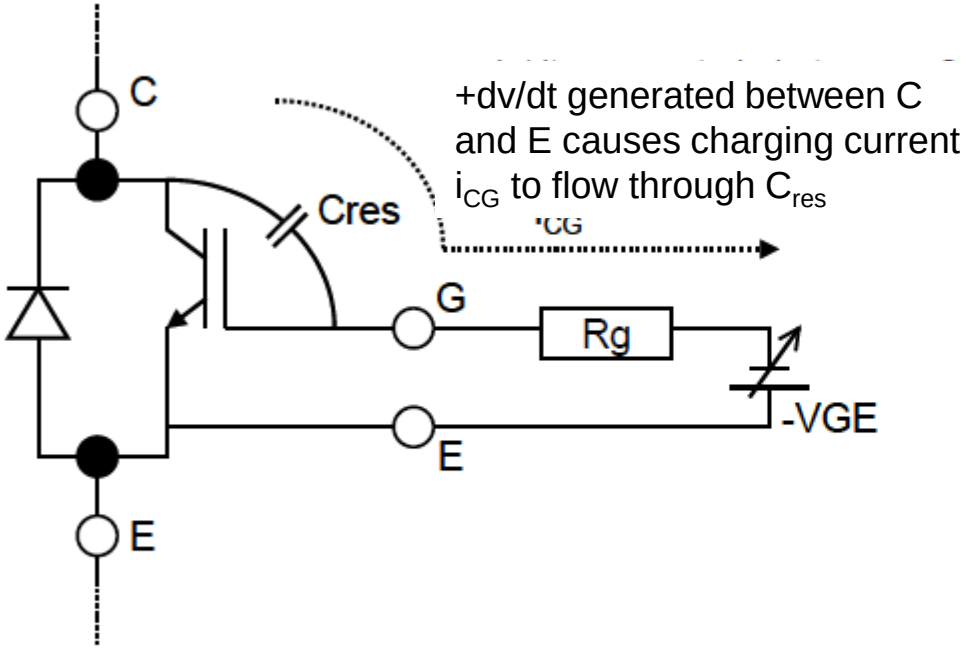
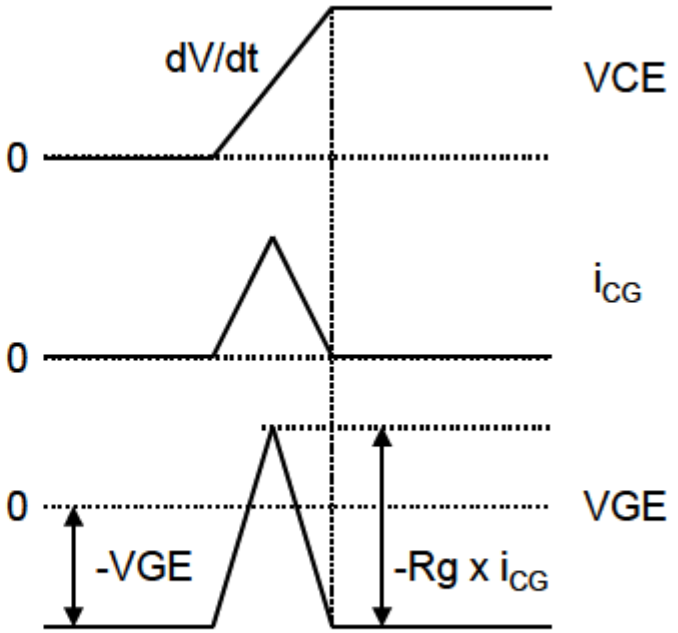
Gate Voltage During Commutation



Principles of dv/dt malfunctioning



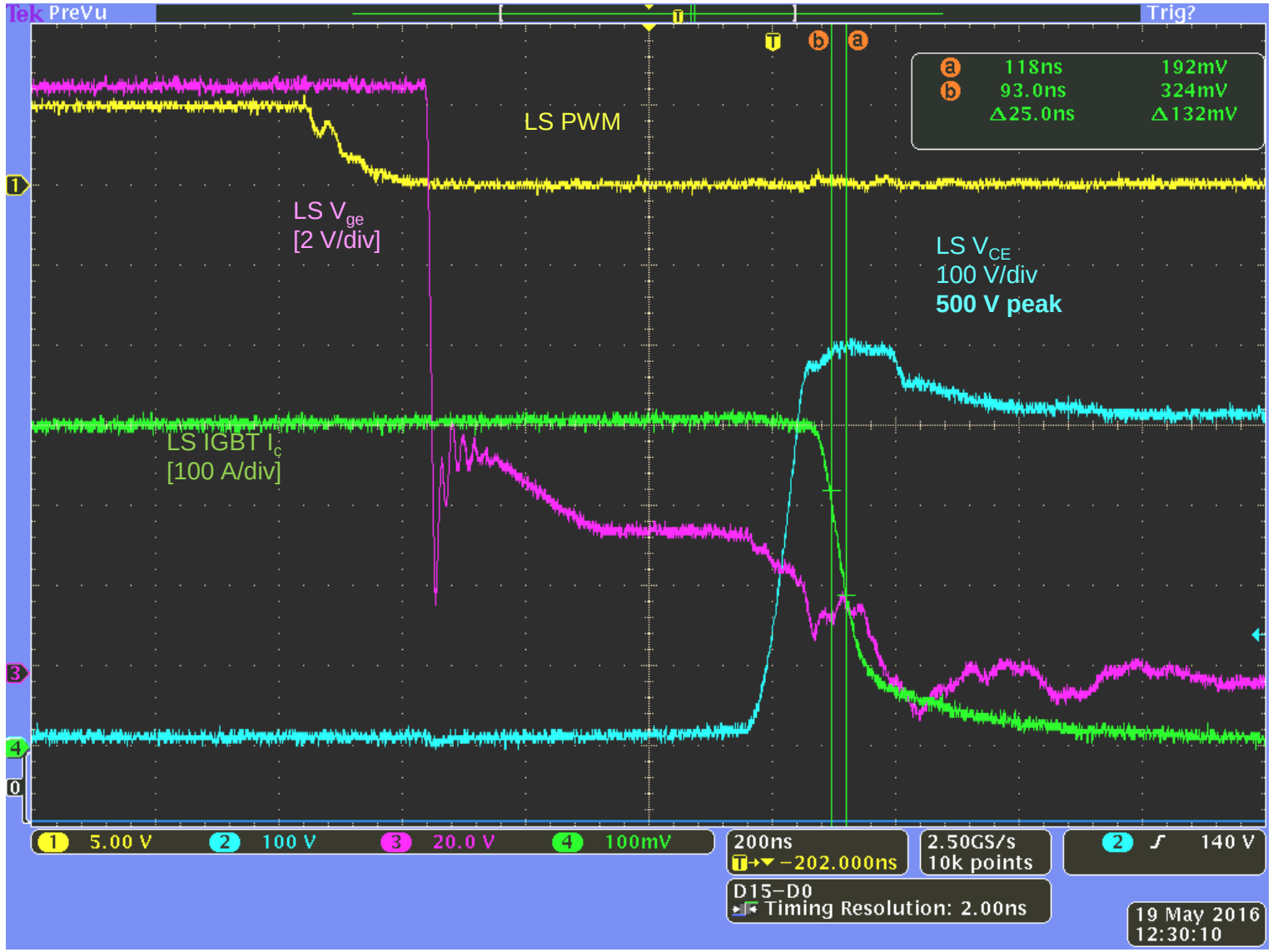
Waveforms during reverse recovery

AMC pin's ability to clamp gate-to-VEE helps reduce E_{on} losses and negative gate supply voltage.

Figure from: "Fuji IGBT Modules Application Manual"

Non-Faulted Turn-off

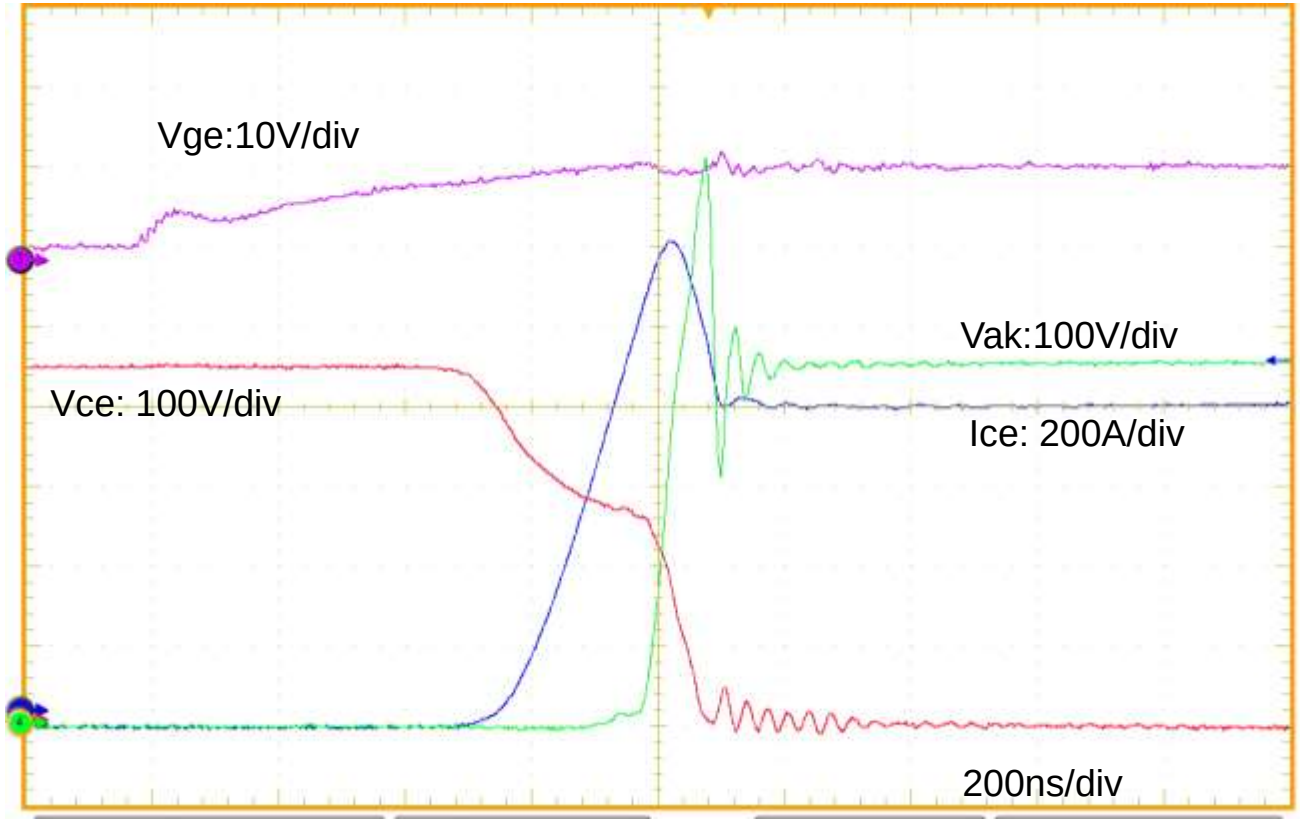
DC Link = 400 V, I_c = 400 A, R_{off} = 0.6 Ω (internal IGBT R_g ~ 0.5 Ω)



Turn on at Cold Temperature (Tested at Fuji)

T_{IGBT} = ⁻40°C, 450V/800A

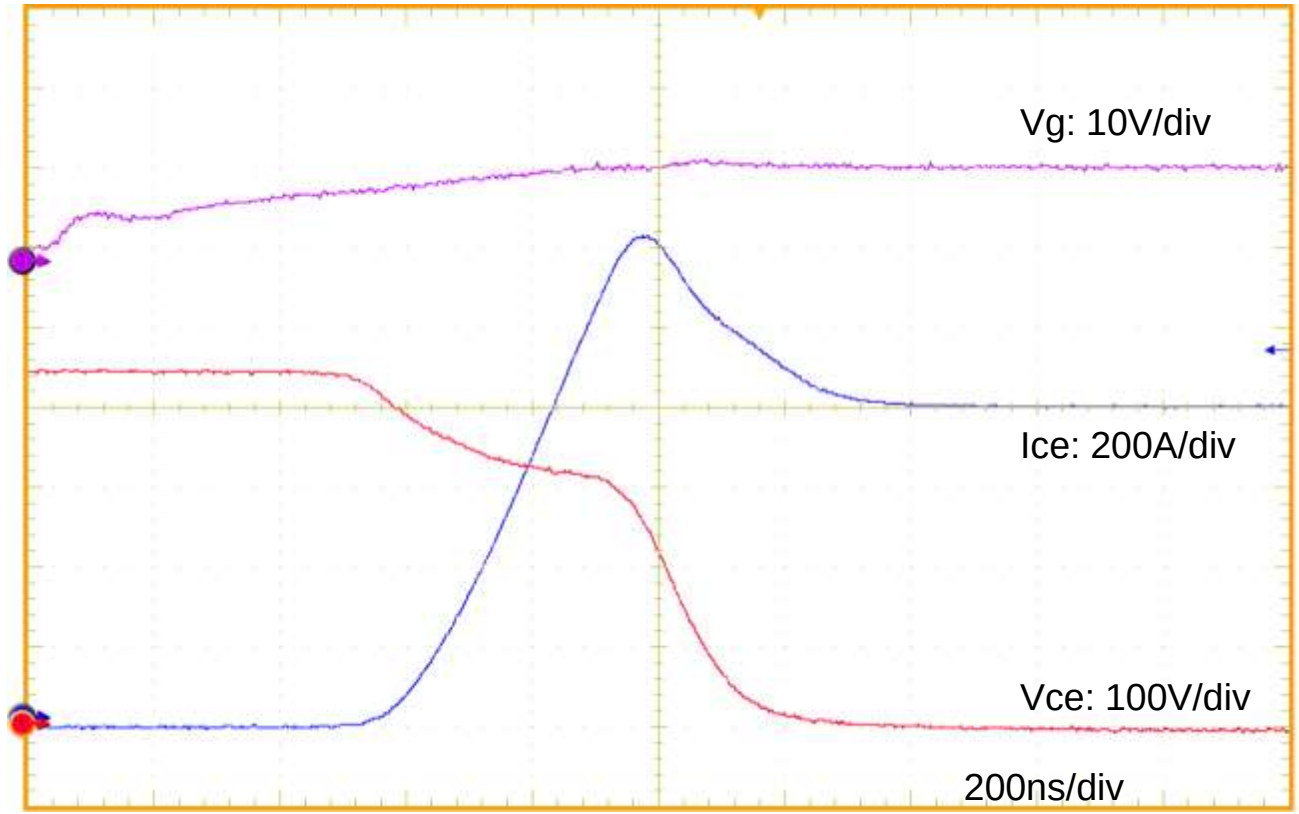
$R_{gon/off}$ = 7.4Ω/1.2 Ω, C_{ge}= 0.015µF, VEE = 0V



Turn on at Hot Temperature (Tested at Fuji)

T_{IGBT} = 175°C, 450V/800A

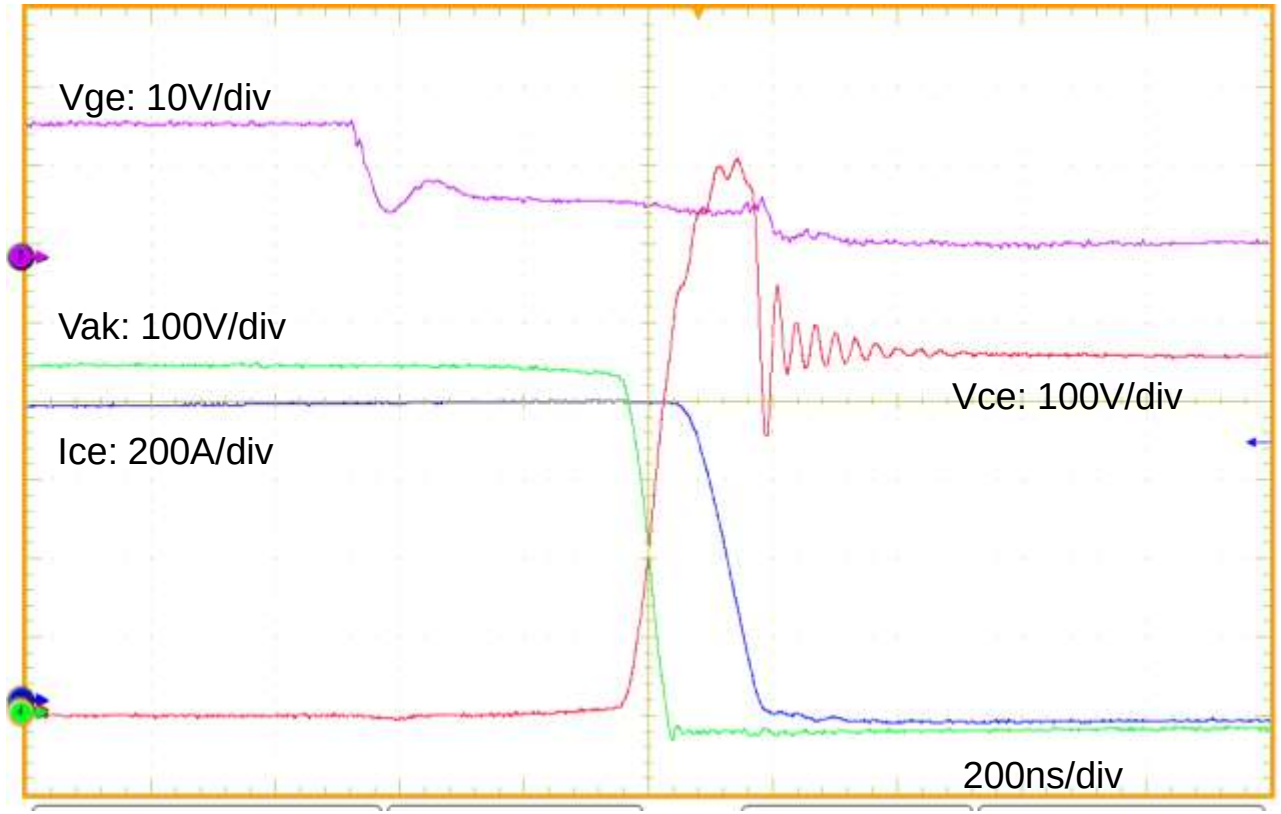
$R_{gon/off}$ = 7.4Ω/1.2 Ω, C_{ge}= 0.015µF, VEE = 0V



Turn off at Cold Temperature (Tested at Fuji)

T_{IGBT} = -40°C, 450V/800A

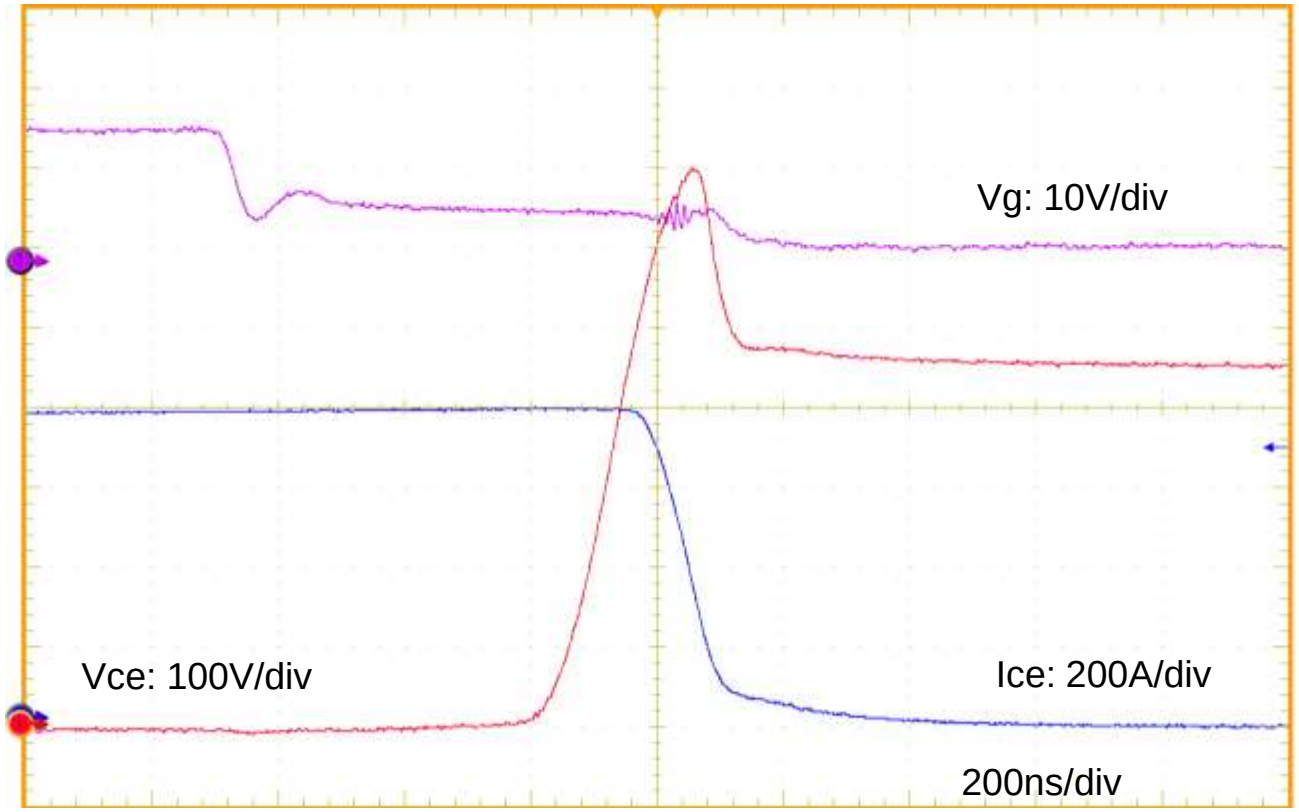
$R_{gon/off}$ = 7.4Ω/1.2 Ω, C_{ge}= 0.015µF, VEE = 0V



Turn off at Hot Temperature (Tested at Fuji)

T_{IGBT} = 175°C, 450V/800A

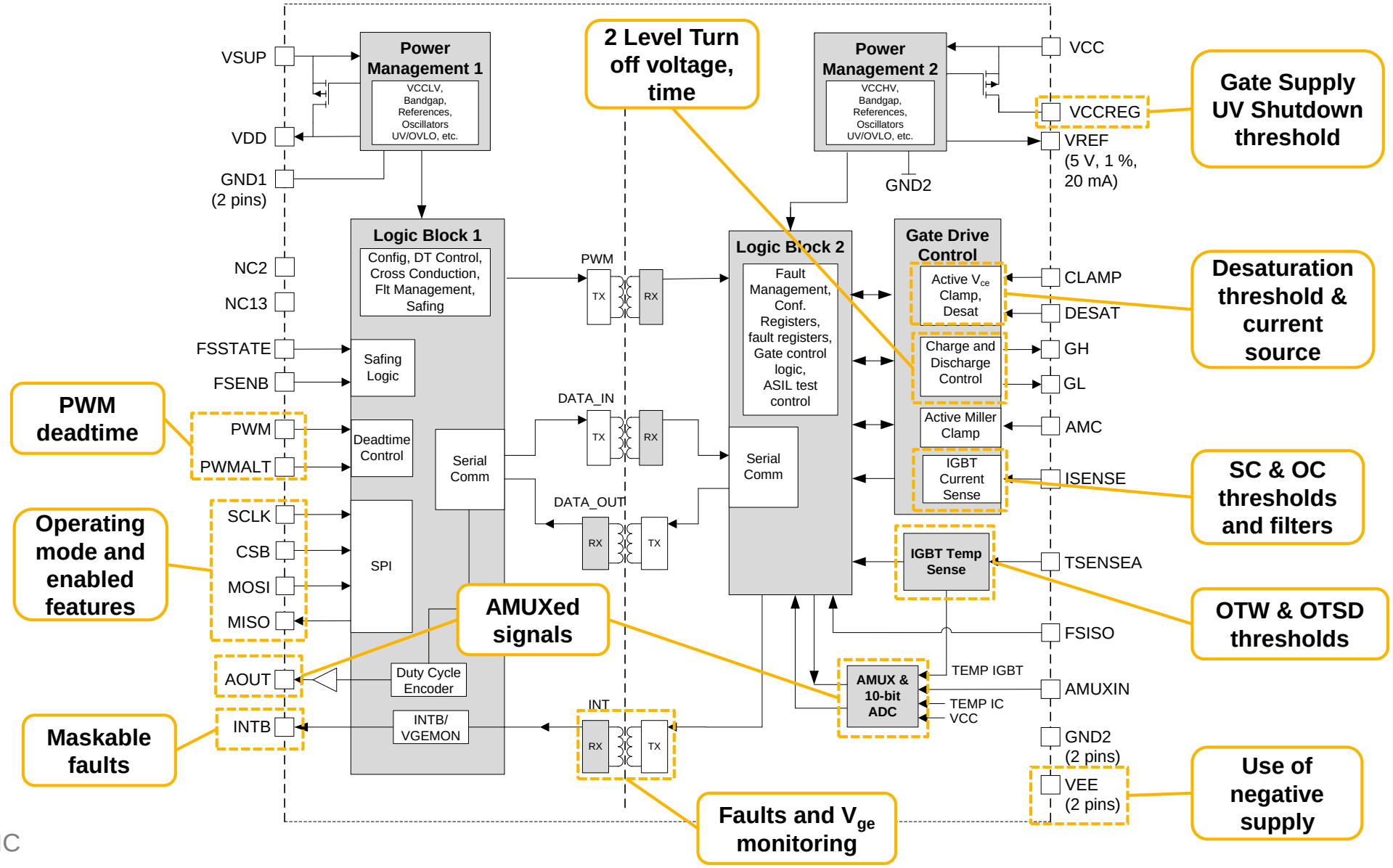
$R_{gon/off}$ = 7.4Ω/1.2 Ω, C_{ge}= 0.015µF, VEE = 0V



OUTLINE

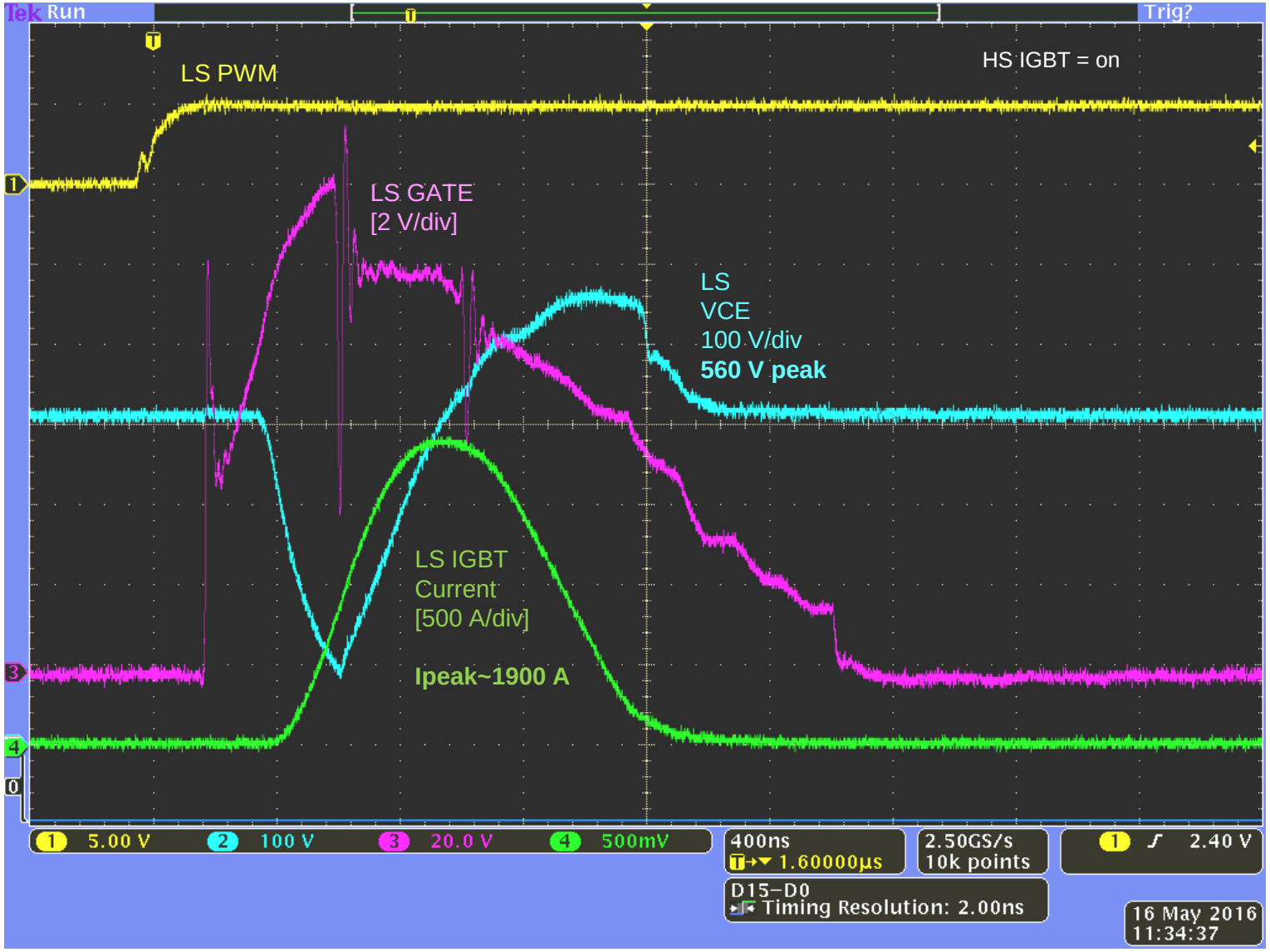
IGBT/MOSFET CHARACTERISTICS
FEATURES OF AN IDEAL GATE DRIVE IC
MC33GD3100 OVERVIEW
SELECTING A GATE DRIVE POWER ARCHITECTURE
MINIMIZING SWITCHING LOSSES
PROTECTING THE IGBT
USE OF NEGATIVE GATE SUPPLY
REDUCING SYSTEM COST
ESTIMATING GATE DRIVE LOSSES
DESIGN SUPPORT

Programmable Protection Features



Short Circuit Response

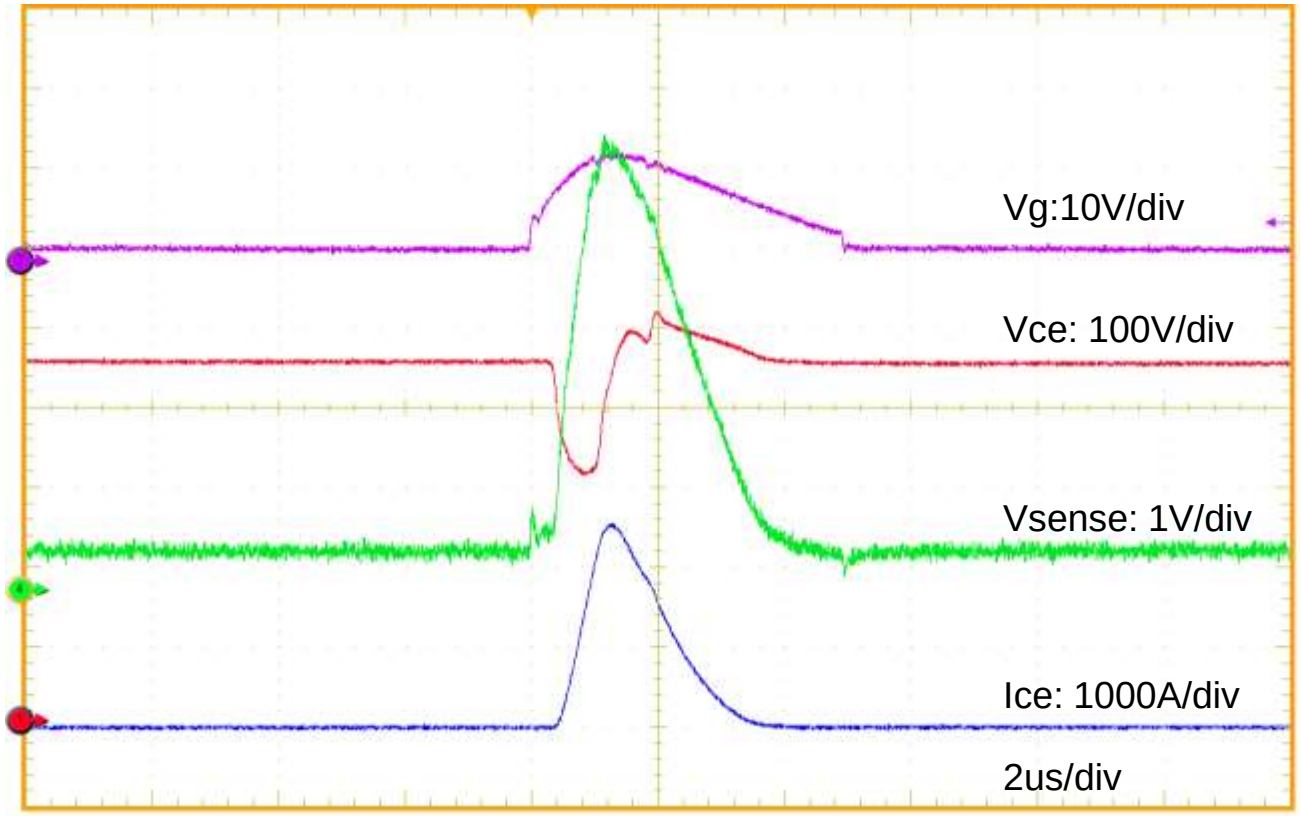
DC Link = 400 V (SCFILT = 400 ns, 2LTOV = 8.8V, I_{SSD} = 400 mA)



GD3100 with M6+ IGBT (Tested at Fuji)

Short Circuit at 175°C, VPN = 450V

HS on; LS turned on



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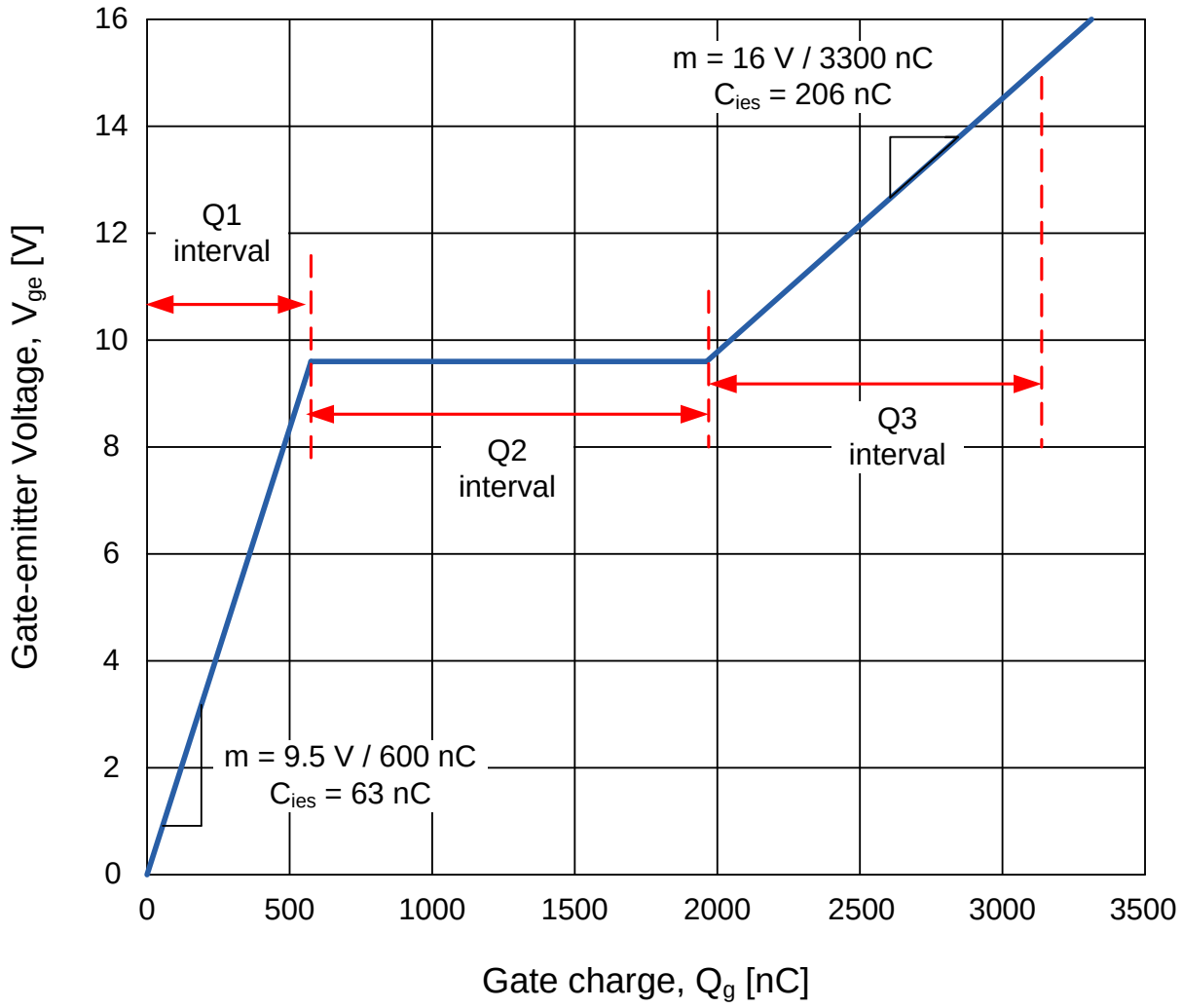
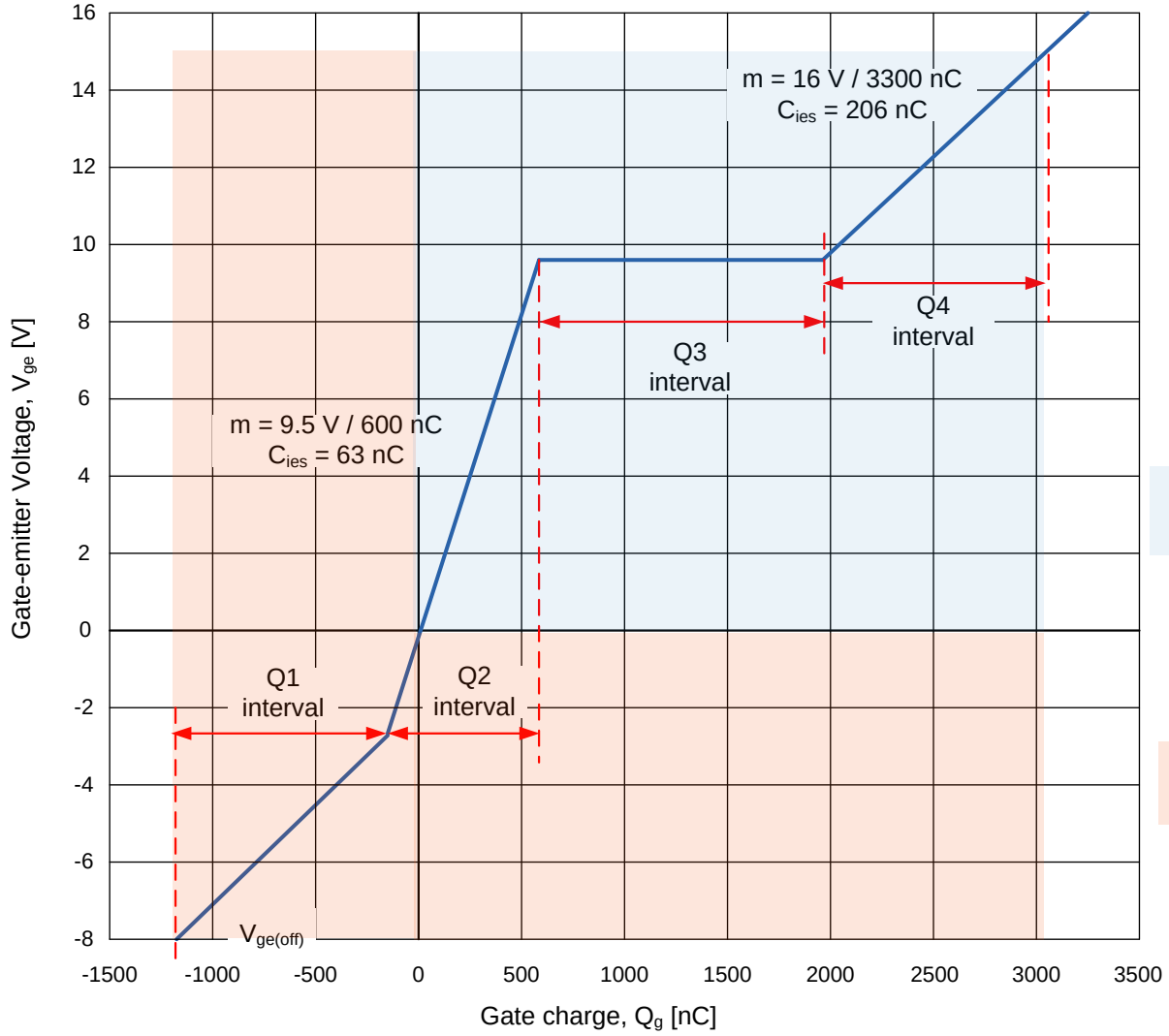
Gate Charge Characterization

- Indicates turn-on and turn off energy dissipated by gate drive resistances
- Indicates total gate drive power
- Indicates input capacitance
- If V_{ce} waveform is shown, C_{cg} can be estimated



Gate Charge Loss Comparison, $V_{ge(off)}$ = 0V vs. -8V

- Losses are 2.1X greater when using a -8V negative gate supply voltage.
- Gate drive supplies must provide the extra power
- Gate drive board must dissipate the extra power



465 mW @ 10 KHz

524 mW @ 10 KHz

(989 mW total)

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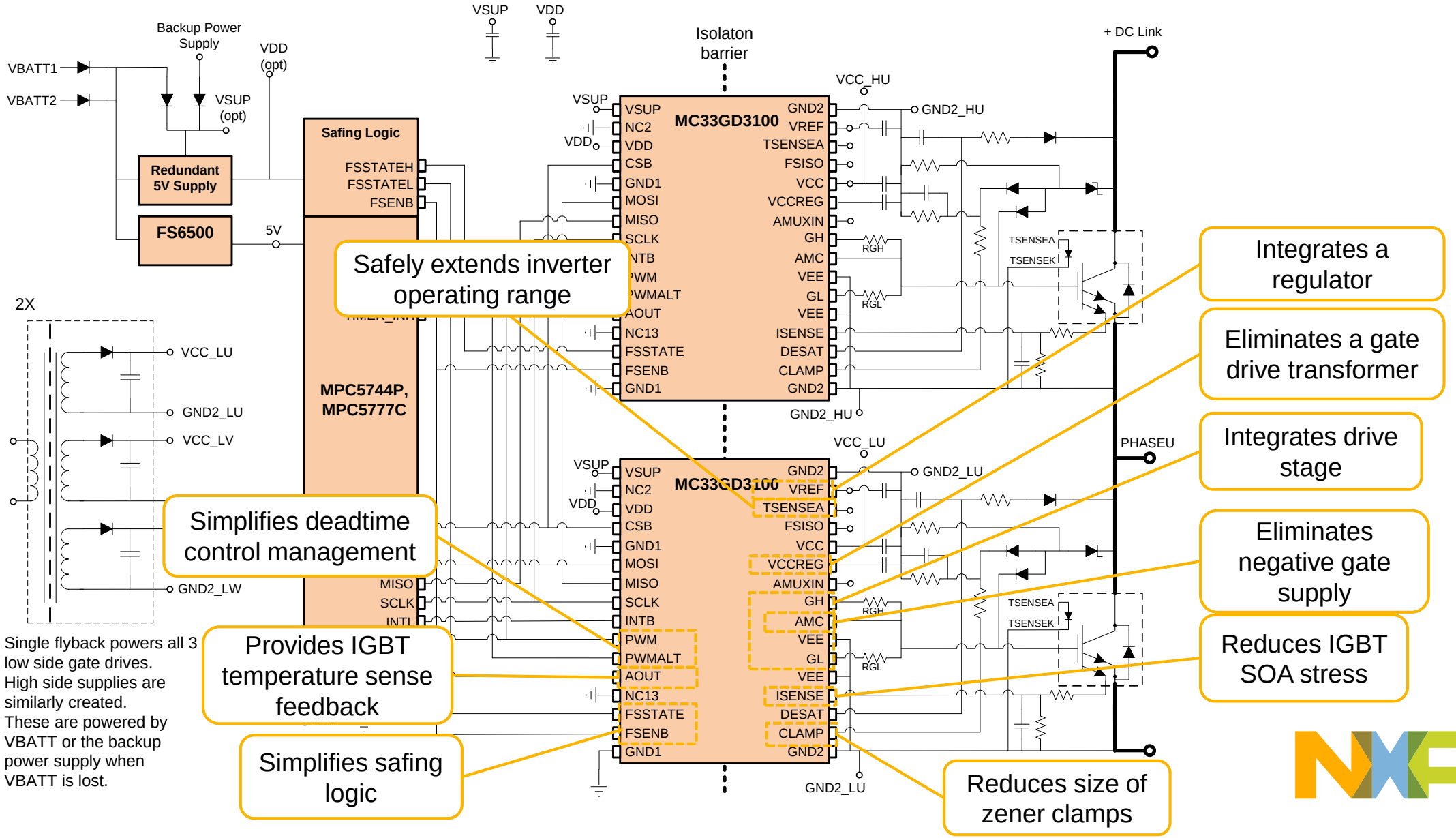
System Simplification & Savings



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Gate Drive Power Dissipation and Junction Temperature Calculator

- The calculator's purpose is to provide a quick means to predict the magnitude of the losses in the gate drive circuit and indicate where the losses appear.
- "User Input" cells are highlighted in yellow. System level values should be entered in the first worksheet.
- Only the losses of the gate drive circuit are estimated, not the IGBT losses.
- The workbook is set up for use with a specific IGBT. If another IGBT is used, its gate charge curve should be used to adjust the gate voltage and gate charge values in the "input" section.
- If the VCCREG post regulator is not used, set VCCREG and VCC to the same value.
- Populate I_{VREF} with its external load current, if any.
- If the temperature sense circuitry is used, set Die 2 Tempsense current = 1 mA.
- Worksheets for $^{-}5$ and $^{-}8$ V provide comparisons with systems using negative gate supplies.
- The estimates are based on gate charging and discharging and are therefore independent of actual switching speeds.
- "AMC Losses in the OFF State" estimates the AMC losses due to the opposing IGBT turning on and off, inducing displacement current in the AMC transistor. The associated losses are based on the required C_{cg} charge and an estimated rise/fall time. The formulae are shown in the final worksheet.
- Junction temperature is estimated based on board temperature or ambient temperature, using R_{thJ-B} or R_{thJ-A}.
- Power dissipation per channel is estimated. This includes power in all gate resistors.

GD3100 Power Budget Calculator

Calculator Inputs:

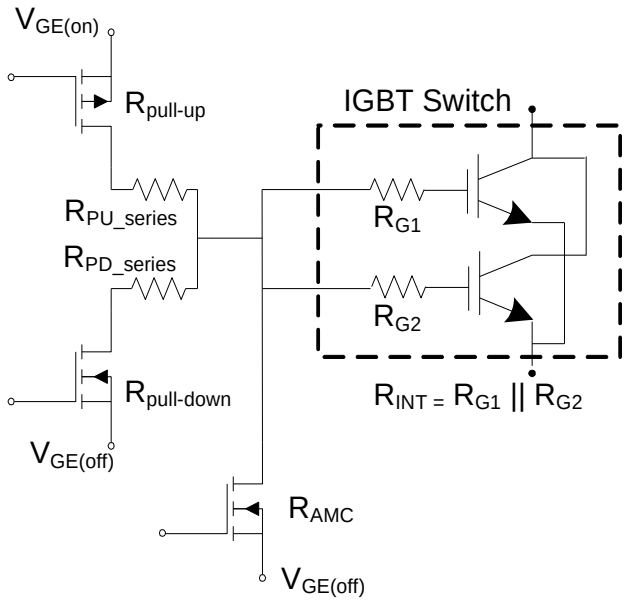
user input	

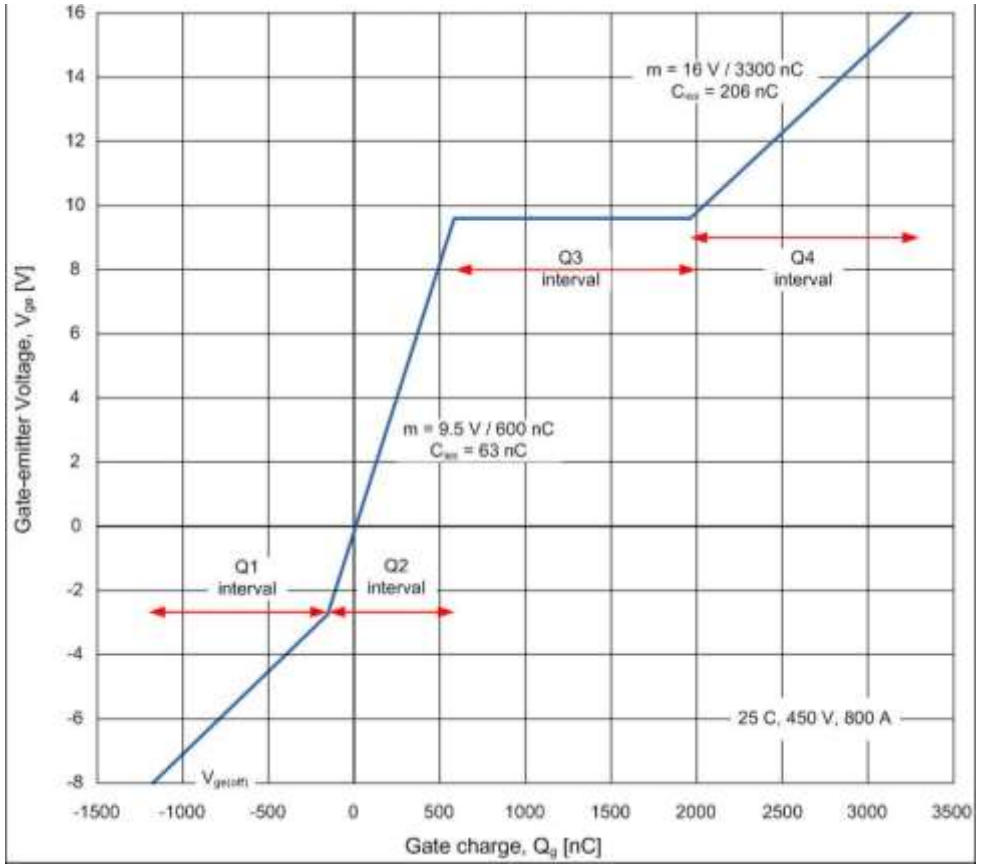
System Assumptions

VSUP	14	V
VCC	17	V
VCCREG	15	V
$V_{GE(off)}$	-8	V
I_{VREF}	0	mA
PWM frequency	10	KHz
$R_{pull-up}$ (internal to IC)	0.5	Ω
R_{PU_series} (external discrete)	3.0	Ω
R_{int_gate} (internal to IGBT)	0.5	Ω
R_{PD_series} (external discrete)	1.0	Ω
$R_{pull-down}$ (internal to IC)	0.5	Ω

IGBT Characteristics

Q1 (negative Vge)	1100	nC
Q2	700	nC
Q3, Plateau Gate Charge	1400	nC
Q4 (to 15V)	1000	nC
Total Gate Charge	4200	nC
Plateau Voltage	9	V
Negative V_{ge} Inflection	-3	V





GD3100 Power Budget Calculator

Regulator and Gate Drive Losses:

Gate Drive IC Q-current & Regulator Losses

Die 1		
Die 1 General I_{VSUP}	9.3	mA
Die 1 Logic Supply Losses	130	mW
Die 2		
Die 2 General $I_{VCC\ current}$	13.2	mA
VCCREG Regulator Losses	112	mW
VREF Losses	0	mW
Die 2 Tempsense current	1	mA
Die 2 Tsense Losses	17	mW
Die2 Logic Supply Losses	224	mW
I_{VEE}	1	mA
I_{VEE} Losses	8	mW

Charging/Discharging Losses

Turn-on (Charging) Losses	Energy		Power		Power per Resistor $R_{pull\text{-}up}$	R_{PU_series}	R_{int_gate}	R_{PD_series}	$R_{pull\text{-}down}$	
Q1 Interval	22550	nJ	225.5	mW	28.2	169.1	28.2	0.0	0.0	mW
Q2 Interval	8400	nJ	84.0	mW	10.5	63.0	10.5	0.0	0.0	mW
Q3 Interval	8400	nJ	84.0	mW	10.5	63.0	10.5	0.0	0.0	mW
Q4 Interval	3000	nJ	30.0	mW	3.8	22.5	3.8	0.0	0.0	mW
Total	42350	nJ	423.5	mW	52.9	317.6	52.9	0.0	0.0	mW

Turn-off (Discharging) Losses	Energy		Power		Power per Resistor $R_{pull\text{-}up}$	R_{PU_series}	R_{int_gate}	R_{PD_series}	$R_{pull\text{-}down}$	
Q1 Interval	2750	nJ	27.5	mW	0.0	0.0	6.9	13.8	6.9	mW
Q2 Interval	7700	nJ	77.0	mW	0.0	0.0	19.3	38.5	19.3	mW
Q3 Interval	23800	nJ	238.0	mW	0.0	0.0	59.5	119.0	59.5	mW
Q4 Interval	20000	nJ	200.0	mW	0.0	0.0	50.0	100.0	50.0	mW
Total	54250	nJ	542.5	mW	0.0	0.0	135.6	271.3	135.6	mW

Total Charging/Discharging Losses										
96600	nJ	**966.0**	mW	52.9	317.6	188.6	271.3	135.6	mW

AMC Losses in OFF State	34.3	mW

GD3100 Power Budget Calculator

Summary of Losses and Junction Temperature Estimate:

Total Losses in the Gate Drive IC

			% of total
Total Charging/Discharging Losses in the Gate Drive IC	**222.9**	**mW**	31%
Die 1 Logic Supply Losses	130	mW	18%
VCCREG Regulator Losses	112	mW	16%
VREF Losses	0	mW	0%
Die 2 Tsense, DESAT Losses	17	mW	2%
Die2 Logic Supply Losses	224	mW	31%
I_{VEE} Losses	8	mW	1%
Total IC Losses	**715**	**mW**	

Total Losses on Gate Drive Board

R_{PU} & R_{DP} losses	589	mW
Die 1 losses	130	mW
Die 2 losses	619	mW
Total channel losses	**1338**	**mW**

Junction Temperature Estimates

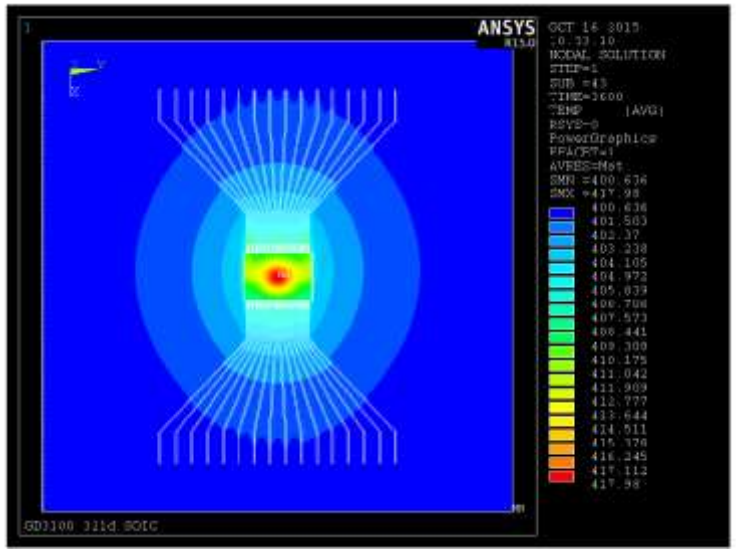
Junction-to-Board estimate

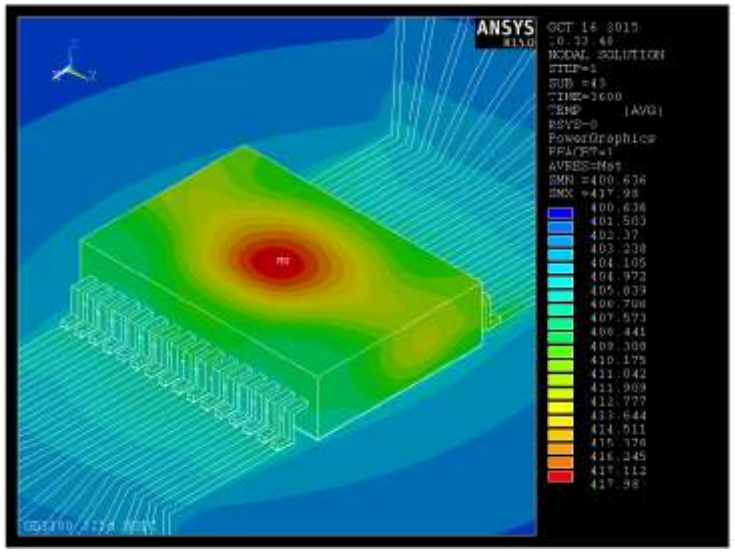
J-Board thermal resistance	43	C/W
Junction temperature rise	30.7	C
Board temperature	120	C
Junction temperature	**151**	**C**

Junction-to-Ambient estimate

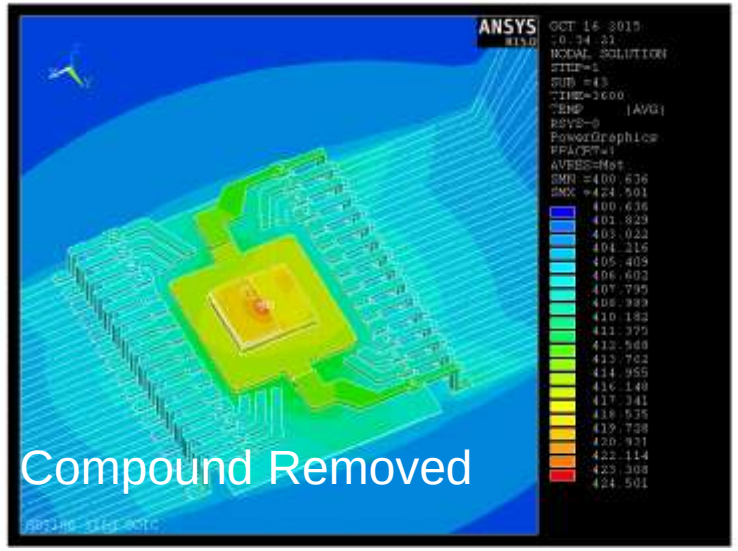
J-Amb thermal resistance	65	C/W
Junction temperature rise	46.5	C
Amb. temperature	100	C
Junction temperature	**146**	**C**

Temperature Distribution – Package Top Surface





Units: Kelvin (K)



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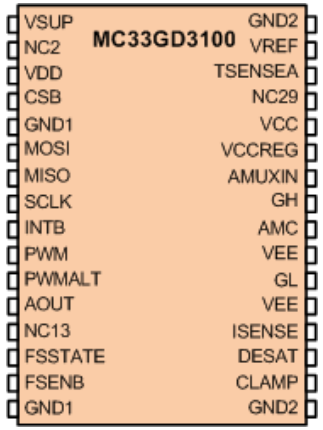
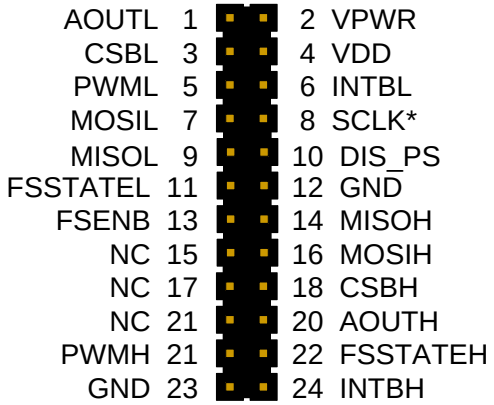
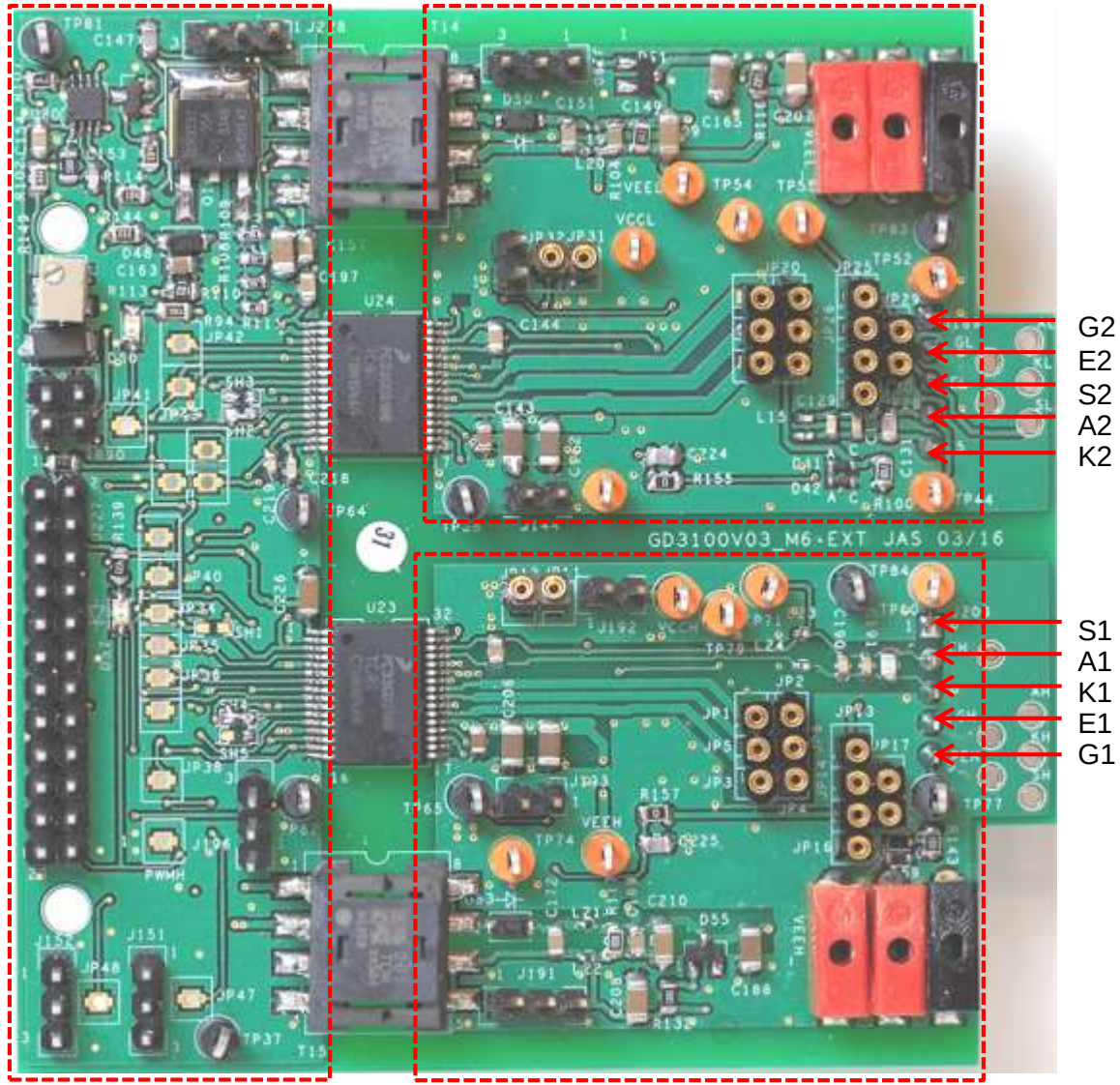
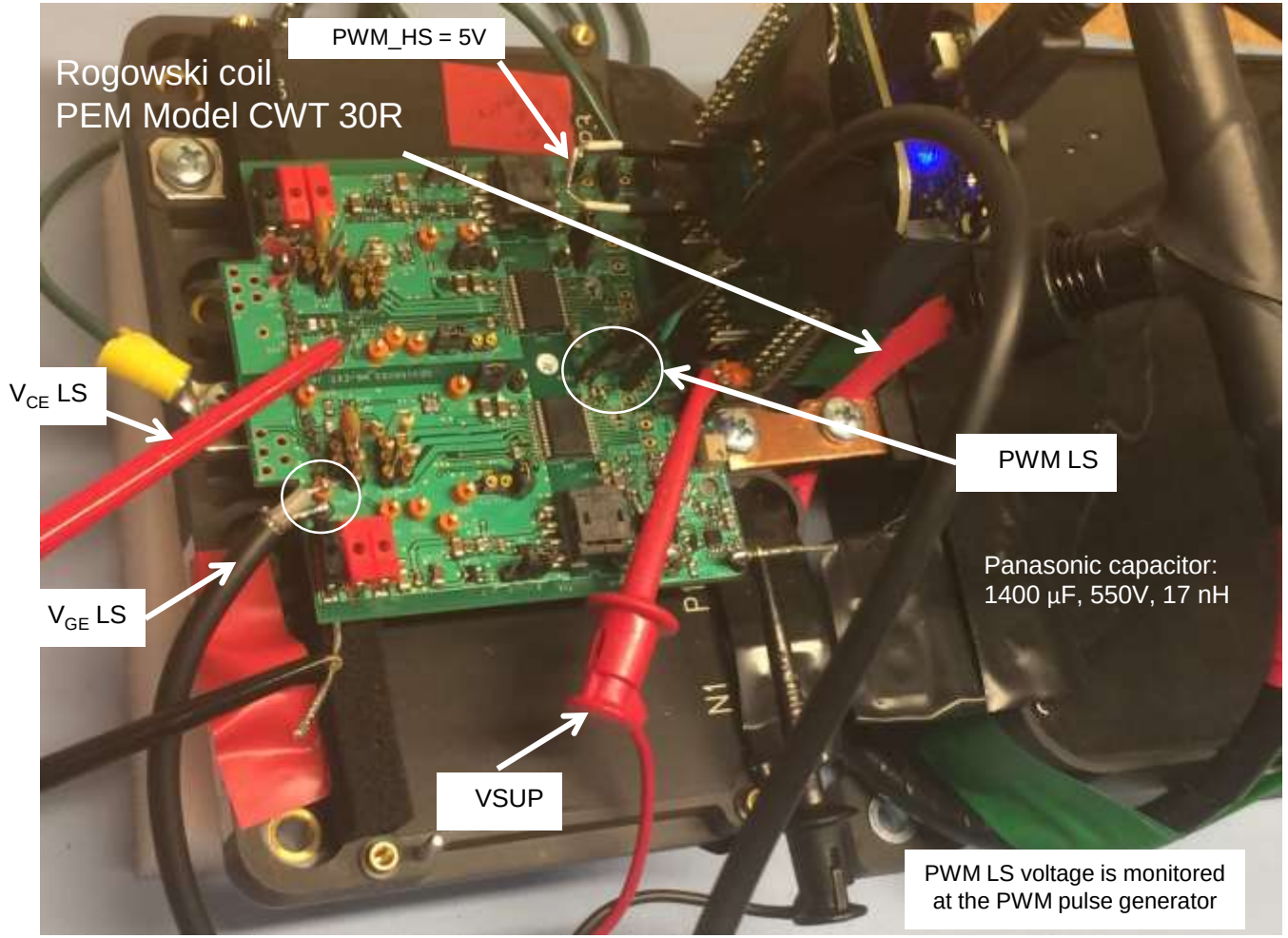
GD3100 ½ Bridge Evaluation Board



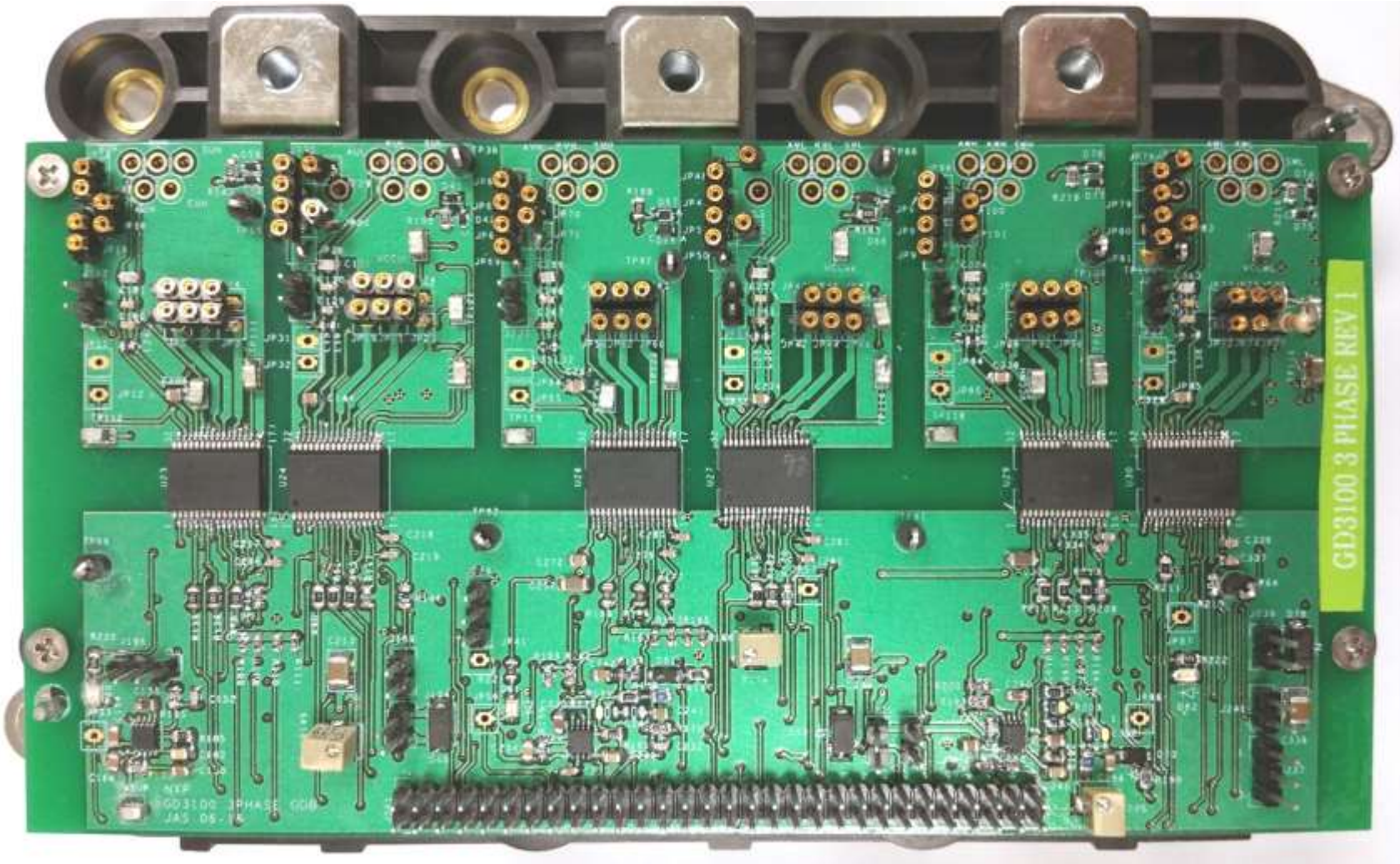




GD3100 Prototype on ½ Bridge Evaluation Board



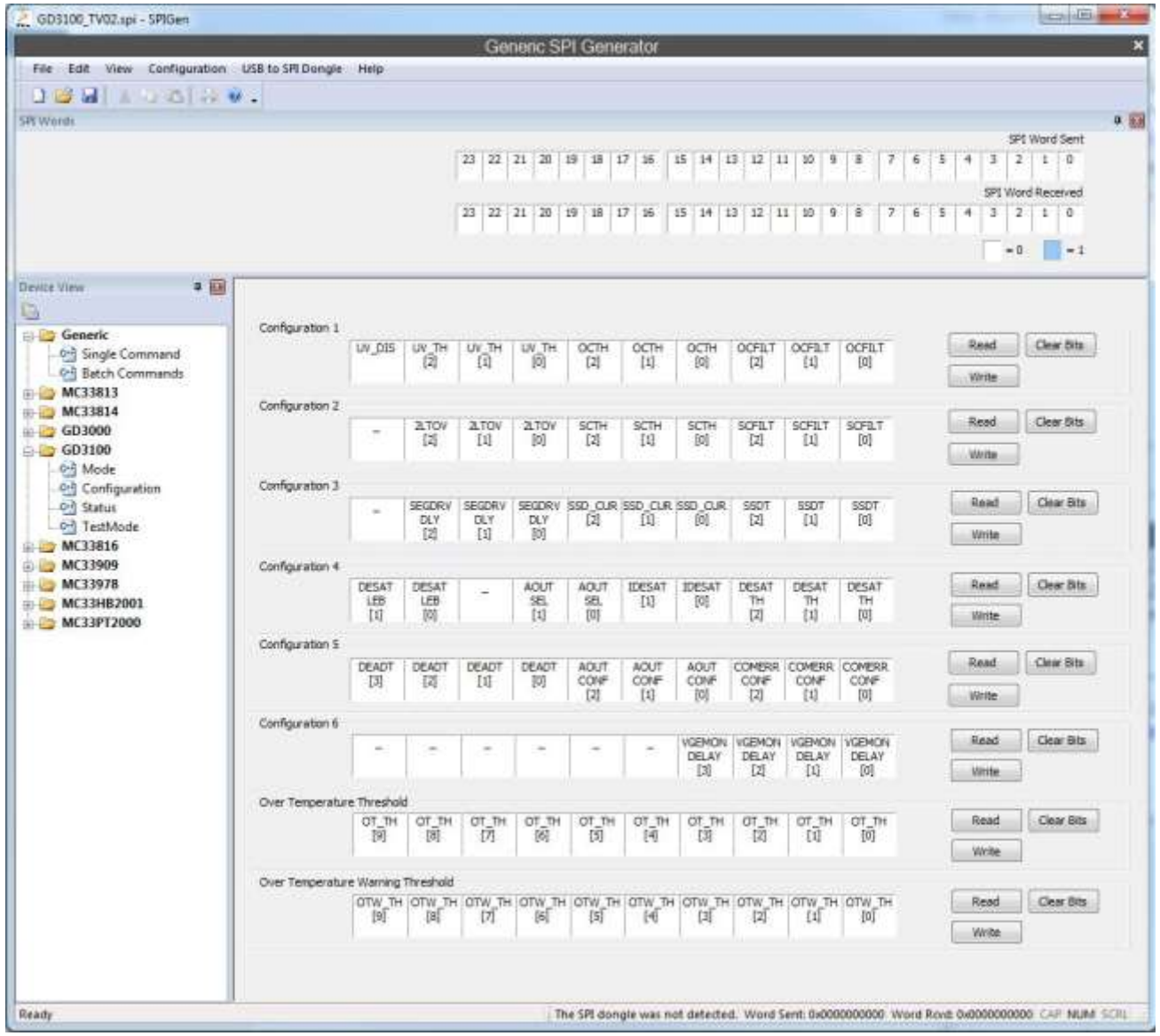
GD3100 Three Phase Evaluation Board



Layout Considerations

- Integrated drivers require high current connections to the GD3100. These include GND, VEE, VCC, VCCREG, GH, GL and AMC.
- VCC, VCCREG and VEE capacitors should be close to the GD3100.
- High current paths to and from the gate should have minimized loop area.
- Gate resistors will dissipate most of the gate drive power.
- Omitting the negative gate drive supply will save significant gate drive power.
- A production version of the NXP ½ bridge evaluation board will have significantly less area allotted for each gate drive circuit.
- Mounting the GD3100 to the board’s topside is probably the best choice thermally.
- Use multiple vias and pins to conduct current from layer to layer.
- Refer to IEC60664 for creepage and clearance requirements.

GD3100 EVB SPIGEN Features/Assessment



REFERENCES

Fuji IGBT Module Application Manual

https://www.fujielectric.com/products/semiconductor/model/igbt/application/box/doc/pdf/REH984c/REH984c.pdf

Available upon request:

MC33GD3100 specification
Training presentation
GD3100 Power Budget Assessment workbook
½ Bridge or 3-Phase Bridge Evaluation Board
SPIGEN software
ISO-26262 Documentation

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