# VEHICLE DYNAMICS COBRA 55

SCOTT O'BRIEN

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SECURE CONNECTIONS FOR A SMARTER WORLD

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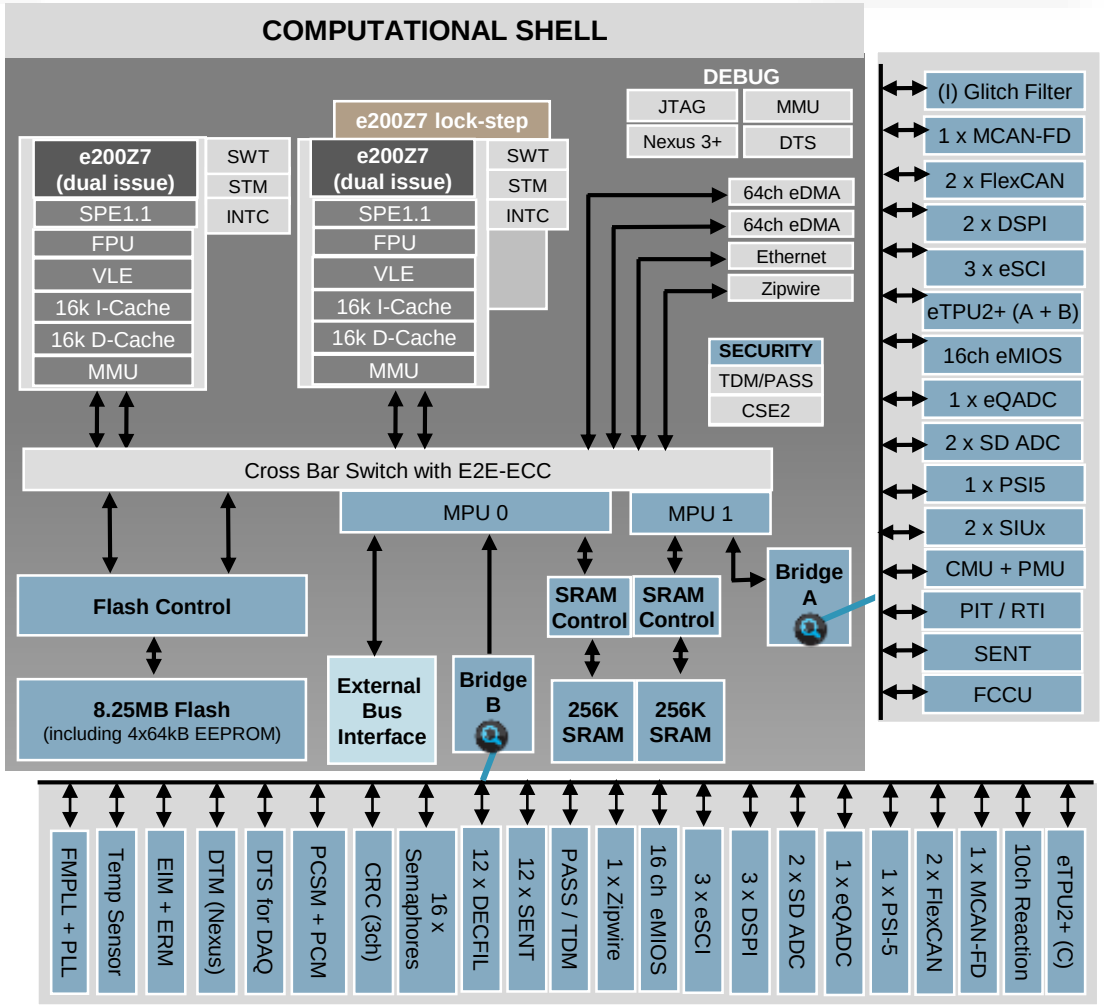
# MPC5777C (Cobra55) Block Diagram

**Cores & Memory**
- Two independent z7 dual issue computational cores @ 264MHz
  - Cores include VLE, SPE1.1, FPU , MMU
  - 16kB i-cache & 16kB data-cache w/ coherency
- Single z7 lockstep core @ 264MHz (for ISO26262 and ASIL-D)
- Up to 8.25MB Flash RWW w/ ECC including 4 x 64kB EEPROM
- On-chip SRAM
  - 512kB on chip static RAM w/ECC (up to 64KB standby)
  - 45kB eTPU RAM , 32kB data cache (w/line locking)
- Security
  - PASS and TDM (Tamper Detection)
  - CSE2 (Crypto Services Engine for Encryption & Secure Boot)

**I/O & System**
- Up to 70ch eQADC from 4 converters w/12bit resolution
  - On-chip temperature sensor and VGA (x1,x2,x4)
  - 12 x Decimation Filters w/ hardware knock integrators
  - Supports triggered burst conversions.
- 20ch ΣΔ ADC (4 converters w/16bit resolution)
- Timers – up to 128 channels (96ch eTPU2+ and 32ch eMIOS)
- 2 x 64ch eDMA support (128ch total)
- 6 x CAN ports (4 x FlexCAN + 2 x MCAN with Flexible Datarate)
- Ethernet
- DSPI – 5 *channels (2 supporting µSec ch.)*
- eSCI – *6 channels (2 supporting uSec ch.)*
- Reaction module – 10 channels for current control
- Up to 12ch SENT, Zipwire, 2ch PSI-5
- 1 x CRC unit – w/ 3 independent channels,
- 4 x protected port outputs, MPU and MMU
- FMPLL + PLL clocks
- Safety Monitors – e2eECC, CLK, Voltage, Fault Collection

**Packaging & Enablement**
- 416 PBGA, 516 PBGA
- Calibration – VertiCALl (using 552CSP)

***Enhanced Target Frequency:***
- *300MHz per core*




***Reflects Standard Device***

SAFE ASSURE™

# Flash & BAM

- In order to communize on all 55nm devices, Flash mapping has been drastically changed.
- The BAM is capable of booting from all 4 SMALL (16K) Flash sectors, along with 1 LARGE (246K) Flash sector.
- The Key message here is that only 1 Large Flash sector is bootable.
- See the Memory Map in the Reference Manual for sector addressing.

| BAM Priority | Flash Address | Size |
|---|---|---|
| 0 | 0x0080_0000 | 256K |
| 1 | 0x0002_0000 | 64K |
| 2 | 0x0003_0000 | 64K |
| 3 | 0x0000_0000 | 64K |
| 4 | 0x0001_0000 | 64K |

# Lockstep Cores

- This device includes an option for a Lockstep Core to be coupled to Core 1.
- If this feature is enabled, then ALL Core 1 Registers must be initialized before being read.
- Accessing uninitialized Core 1 Registers will lead to a Lockstep Error, as Core registers generally are undetermined after Reset
- Contact your local FAE for an example start up file

# SRAM Ports & Mapping

- This device includes 512K of SRAM
- This SRAM is split into 2 contiguous blocks
- There are 2 ports into the SRAM
- The ports are aligned to the Lower & Upper halves of  the memory space
- It may be advantageous to assign each core highest priority to one of the SRAM ports, through the XBAR.  The port may also be “Parked” on this core.
- Core specific variables would then need to be mapped into one particular half of the SRAM
- This scheme would allow each core to freely access SRAM without contention from the other core
- Of course, the operation and requirements of other bus masters must be kept in mind (DMA, Ethernet, etc)
- The priority scheme may be tuned for optimum operation in a particular application

# E2E ECC – Application Effects

- This device includes End To End Error Correction Coding on memory and peripheral bridges.
- This feature extends ECC functionality into the Address field, and is important for ASIL-D operation.
- For this device, the E2E ECC may result in memory accesses requiring an additional clock cycle to complete.
- Due to complex buffering schemes, this additional clock cycle will not show up in bench marks where a full application, or representative simulated application is running.
- The additional clock cycle will show up as a substantial performance degradation form previouses devices, when executing long loops that perform the following:
  - Use Store Multiple Instructions (STMx) into SRAM  (SRAM Initialization)
  - Use Load/Store Instructions to Read/Write to eTPU RAM
  - Use Load/Store Instructions to Read/Write block of peripheral registers

# eTPU RAM

- ECC is now included on all eTPU RAM
- It is essential that ALL eTPU RAM be initialized before being read
- Reading uninitialized eTPU RAM will result in an ECC Machine Check Exception

# CAN Message Buffers

- ECC is now included on all CAN Message Buffers ( RAM )
- It is essential that ALL CAN Message Buffers be initialized before being used
- Reading uninitialized CAN Message Buffers will result in an ECC Machine Check Exception
- Even if the application is not using all Message Buffers, it is important to initialize them, as the CAN Controller may access them

# MCAN-FD

- Cobra90 has 4 x FlexCANs
- Cobra55 has 4 x FlexCANs + 2 x MCAN-FD modules
- The MCAN-FD module implements the CAN FD data link layer protocol which supports higher bit-rates than 1 Mbit/s and allows frame payloads longer than 8 byte.
- CAN FD makes use of the internationally standardized CAN high-speed transceivers (ISO 11898-2). For bus-line topologies, the data-rate can be increased to 8 Mbit/s and theoretically higher data-rates using state-of-the-art transceivers.
- For passive star topologies as used in passenger cars the maximum data-rate is expected to be 2 Mbit/s.
- Issue: There was an error with CRC calculation in the initial CAN-FD Specification.  As of this writing, the new specification has not been released. This device only supports the initial CAN-FD specification.  CAN-FD may still be used with additional SW support to insure proper message reception.

# eDMA TCD RAM

- There is an issue in the eDMA, due to backward compatibility when Minor Looping feature is enabled, possibly even when not.
- The bit fields given in the header do not apply in this case.
- NONE of the TCD RAM should go uninitialized as reset values are totally random.
- Failure to do this WILL result in completely unsuspected behavior of the DMA engine
- Examples of this include the CITER and BITER values, along with NBYTES, etc.

# FCCU Operation

- Fault Collection / Control Unit
- Provides a common location for all on board fault reporting (Clocks, LVDS, BIST, etc)
- The FCCU is more than just a register mapped peripheral, it is a state machine that operates over 2 Clock Domains (Peripheral Clock & 16MHz IRC).
- As a result of this, specific procedures must be followed in order to configure the peripheral and monitor it’s behavior (See RM for details)
- Also, you cannot step through FCCU code with a debugger, or have any FCCU register windows open when executing FCCU code.
- Attempting to debug through code will most likely result in failed FCCU operations, and or unexpected behavior.

# PLL's & Clocking

- The clocking in this device is much more complicated then previous devices
- The device comes out of Reset running on an internal 16MHz IRC
- The External OSC must be enabled in the SIU
- There are 2 PLL's (One PLL and one FMPLL)
- There is a restriction on the input of PLL1.  It must be between 35 and 78MHz. Therefore, it most likely will come from an output (PHI1) of PLL0
- The eTPU is limited to 200MHz
- There are multiple peripheral clocks and dividers, so look closely at the RM
- There are also 9 Clock Monitors which will insure the integrity of all the different clocks, and report their status to the FCCU

# Dual Core Interrupts

- Due to the flexibility of the Interrupt Controller, you may map any external interrupt (IVOR4) to either core, or both cores.
- Please do not map interrupts to both cores!
- If you feel that you MUST do this for some reason, consider the following options for inter processor communications instead:
  - Shared SRAM Variables
  - Hardware Semaphore Block
  - Core 2 Core Interrupts
- It is very easy to get into trouble when attempting to service an interrupt using both cores.  If you see no way around this situation, please contact your local FAE for support on how to properly construct the handlers.

# eMIOS Split

- The 32 channel eMIOS is now split into two instances of 16 channels each
- This is an enhancement for ASIL-D
- The channel mapping is laid out below and also in the Header file.

| | Instance Channels | |
|---|---|---|
| **eMIOS Pads** | **EMIOS_0** | **EMIOS_1** |
| 0-7 | 0-7 | |
| 8-15 | | 0-7 |
| 16-23 | 16-23 | |
| 24-31 | | 16-23 |

# Glitch Filter Block

- A new peripheral has been added to provide programmable filters on specific eTPU and eMIOS pins
- ALL pin filters are DISBALED by default
- To use a pin that has an associated filter, you must enabled the Glitch Filter module, and then enabled the specific pin filter
- Check the RM for Pin details

# CSE Tips

- When working with the CSE, keep in mind that ONLY Physical addresses are recognized, as the CSE does not recognize any MMU addressing from the cores.
- Any Keys to be moved to RAM need to be specified as either Global Variables, or Absolute Addresses.
- Local Variables will not work, as the compiler uses registers for these and the CSE commands require actual addresses.
- Do not access PFLASH Registers During Secure Boot.  This may result in an unexpected Reset.

- Note On Security Flags:
  - If the SFE bit = 0 in the CSE_CR, then all the Security Flags shift left 1, as the VERIFY_ONLY flag is eliminated.
  - This seems to correspond to the SHE specification.

# MPU Info

- There are several errors in the RM (Rev 2) including the example configuration.
- Yes, you really do use Logical Master Addresses.  Everyone asks this because it appears contrary to the descriptor layout.
- Yes, you must use the MPU for which the Slave Port is assigned.  Despite what the RM says, you cannot use any address in the entire memory space.
- No, the MPU does NOT work with Flash.  Why?  We believe it is because all Flash accesses would be delayed in order to compare with MPU descriptors.
- MPU Access Errors will generate a Machine Check
- For Read Errors, you must increment the Return PC to the Next instruction.  This may require decoding the instruction if VLE is used (Contact your FSL FAE for assistance in this, as the ASM code is available)
- For Write Errors, you must return to the instruction which was executing when the error occurred.  In other words, NO Return PC increment.  This is because the Write will actually execute further down the pipe, and may also be delayed further due to Write Buffering.

# VertiCAL Specifics

- There are 6 extra pin on the VertiCAL device that need to be included on the board:
  - 2 TPWR – Tool Power Pins
    - This is a straight pass through and should be battery or ignition (12V)
  - 4 TOOLIO – Tool I/O (Trigger) Pins
    - These should be defined by the application
- JTAG Signal Jumpers keep JTAG signals from the target board
  - These are on the VertiCAL ring and depopulated by default.
  - There is an issue with TCK going to both the VertiCAL ring and the target.
  - If possible, use the Nexus connector on the VertiCAL Debug Adapter Board, as opposed to having it on the application target.
  - This will simplify layout and assure signal integrity.
  - Both Nexus and the EBI require 3.3V to operate.

# Supply Pins & Sequencing

- VDDPWR and VDDPMC MUST be at the same voltage level

- If VDDPWR = VDDPMC = 3.3V
  Then VDDFLA (Previously VDDSYN) MUST also be connected to 3.3V
  Else VDDFLA should have only capacitors (Internally Generated)

- VDDE2 MUST be 3.3V as the NEXUS Trace Supply

- VDDEH1 MUST be 5V I/O

# Supply Pins & Sequencing (2)

- If VDD_EQ (eQADC Supply) does not ramp up before VDDPWR
- Then a Reset may occur due to PMC Temperature Sensor Comparators
- This may be avoided by disabling the Reset through a DCF Record

- eQADC_B Channels 8 to 23 are powered by VDDEH7 not VDDA_EQ
- If VDDEH7 is connected to 3.3V, then ANB8-ANB23 will be limited to 3.3V. ***THIS COULD BE A LARGE GOTCHA!***

# AIPS Registers

- The AIPS PACR and OPACR registers determine Read/Write characteristics for each of the peripherals.  Make sure that these values are set up properly for Read/Write & User/Supervisor access.  Bus errors will result if access is not properly controlled.  The Default values may not be sufficient for your application.

- Similarly, the MPRA registers define Bus Master access characteristics for the Peripheral Bridges. A Bus Master is defined by it's Logical ID.  Again, the Default values may not be sufficient for your application.

# Power Supply Route 5V Main Regulator - LDO

- For main 5V, create a star route from near the place where the power island connects to that trace, and have a large capacitor there.  You  want the field energy to be available reasonably close to the part.  As close to the part as possible, small package capacitors, (0402).  At the output of the pass transistor, a reasonably large capacitor, but 0402s as close to the part as you can.

- The pass transistor and its supporting components (except for the 0402 at the MCU) do not have to be pushed up against the part.  You just need to make sure you use transmission lines for the power in, the gate control, and the power out.  Lumped distance for this circuit is longer than your PCB will be.  A bipolar transistor does not react to changes very quickly, many microseconds, so if it is a couple of inches away it will not matter.  What does matter is again, using transmission lines and close placement of the small capacitors.

- More important, is that the power conductors never, ever, ever are more than one dialectic from ground.  Failing to do so will cause more noise than any power conductor routing scheme.

***From Dan Beeker – Layout Master***

# MIDR Register Settings

- The reference manual (up to and including REV 8) has the incorrect value for the MASKNUM_MINOR field.
- The correct values for this is MASKNUM_MINOR field:

  1N45H = 0001b

  2N45H = 0010b

  3N45H = 0000b

# Flash Values With The Same ECC Value

This can be useful for “Over Programming” or EEPROM Emulation

*(UTEST also contains 2 locations for Single and Multi bit ECC Errors)*

| Double word | ECC all 1s no error |
|---|---|
| 0xFFFF_FFFF_FFFF_FFFF | 0xFF |
| 0xFFFF_FFFF_FFFF_0000 | 0xFF |
| 0xFFFF_FFFF_0000_FFFF | 0xFF |
| 0xFFFF_0000_FFFF_FFFF | 0xFF |
| 0x0000_FFFF_FFFF_FFFF | 0xFF |
| 0xFFFF_FFFF_0000_0000 | 0xFF |
| 0xFFFF_0000_FFFF_0000 | 0xFF |
| 0x0000_FFFF_FFFF_0000 | 0xFF |
| 0xFFFF_0000_0000_FFFF | 0xFF |
| 0x0000_FFFF_0000_FFFF | 0xFF |
| 0x0000_0000_FFFF_FFFF | 0xFF |
| 0xFFFF_0000_0000_0000 | 0xFF |
| 0x0000_FFFF_0000_0000 | 0xFF |
| 0x0000_0000_0000_0000 | 0xFF |

# Lauterbach

If you using the Lauterbach debugger, you may need to add the following command to any scripts that you are using:

SYStem.Option.KEYCODE “256 Bit JTAG Password”

Is used to enter a JTAG Password for the SYStem.Up command

Example:

```
SYStem.Option.KEYCODE 0x01111111 0x02222222 0x03333333 0x04444444 0x05555555 0x06666666 0x07777777 0x08888888
SYStem.Up
```

Another useful command can extend the length of the Reset for the SYStem.Up command:

SYStem.Option.SLOWRESET

# Censorship Tips

- The JTAG Password is functional only after the Life Cycle has been Advanced at least to OEM Production.
- If you are planning on using the PASS module Password feature, program ALL Passwords in UTEST BEFORE advancing the Life Cycle to OEM Production or beyond  You will not be able to add them later.
- If you program PASS module Passwords in UTEST, you should provide default values for PASS_LOCKn the registers by programming DCF records.
- When advancing the Life Cycle, the previous Life Cycle must be Invalidated, and the new one Validated.  This is accomplished by programming the proper locations:
  - Invalidate: 0x400xx8 = 0x55AA50AF 0x55AA50AF
  - Validate: 0x400xx8 = 0x55AA50AF 0x55AA50AF
  - Example Addresses: 0x400218 & 0x400220
- Do not enable censorship on a blank device (erased).  If you do, the BAF will enter Reset Escalation after Power On and the device will be rendered useless!

# Cobra 55 Plus

There is a plan to offer a Cobra 55 Plus Device by Q4 2017

This would be accomplished through a device Sort during Testing

Key Differences From Cobra 55:

- MAX of 300MHz Operating Frequency
- MAX of 240MHz eTPU Frequency
- No Ethernet
- Possible limitations on SDADC clocking
- Overall 9 to 12 percent increase in overall core performance

# The End / Revision History

# Revisions Information

1) Initial document

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FOR A SMARTER WORLD