Open Industrial Linux® (OpenIL): Secure, Robust, Real-Time for Industrial Automation

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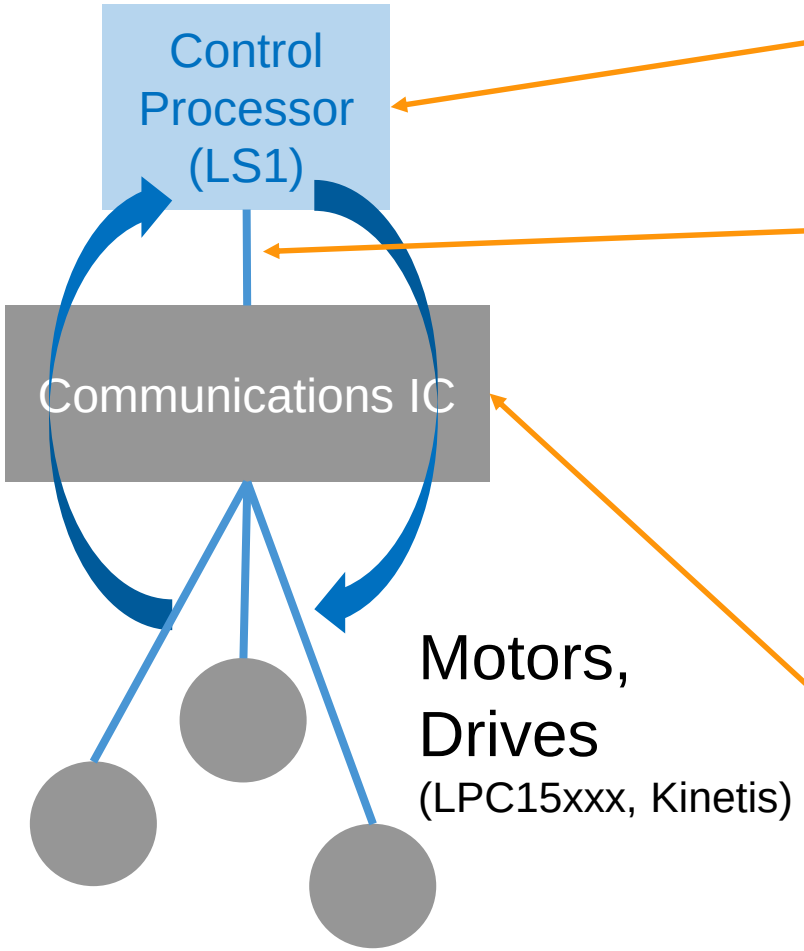
SECURE CONNECTIONS FOR A SMARTER WORLD

Agenda

- Industrial Application Requirements
- Deterministic Computing
- Protecting Industrial Devices
- Time Synchronization
- Deterministic Networking

Manufacturing Automation/Smart Grid Requirements



Processor Requires Real-Time Performance

Traditionally supported via RTOS

PCIe or 16 bit parallel bus

Depends on data sizes and system architecture

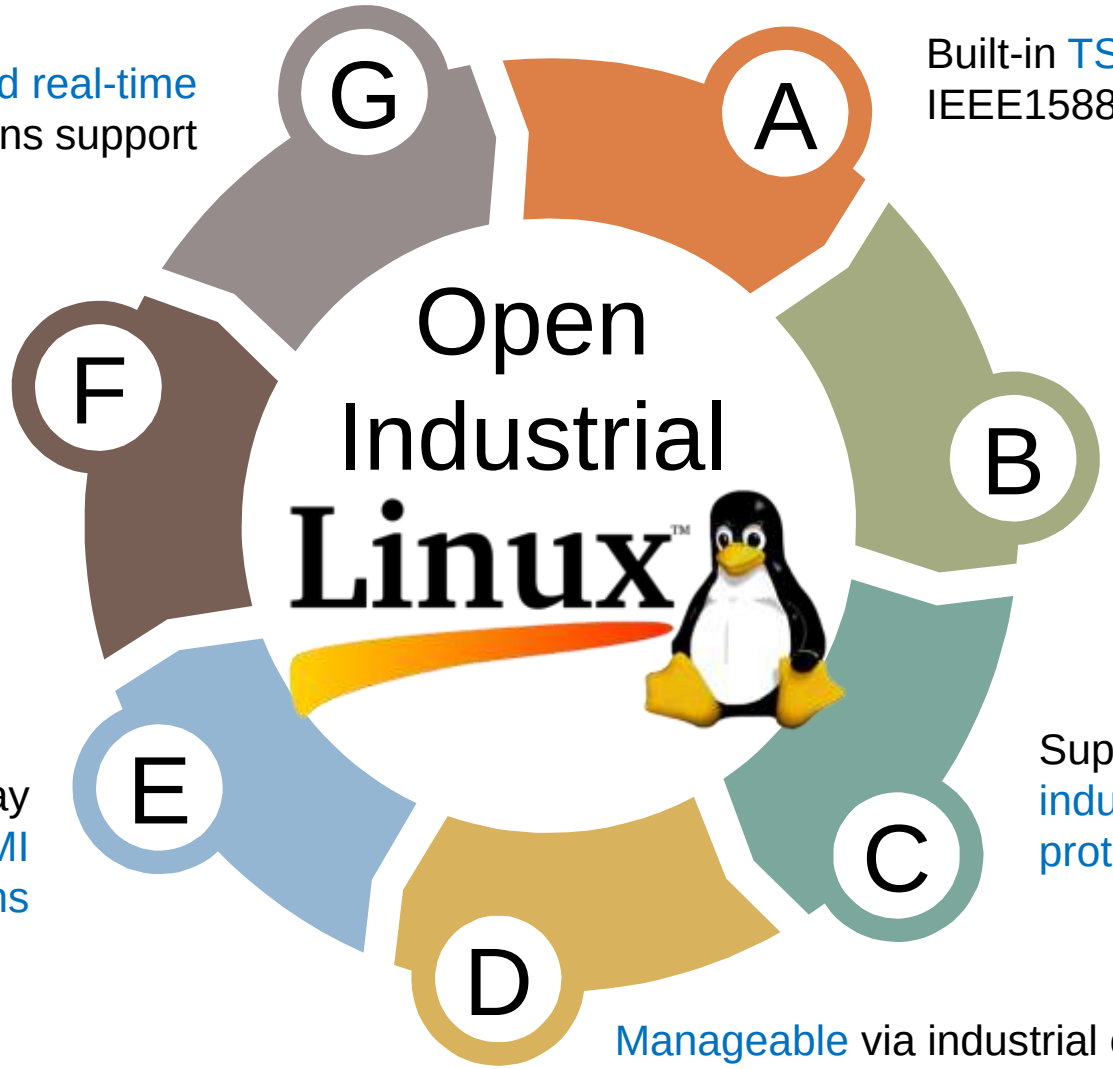
Control loops run every 25-150 usecs

Requires low, deterministic latency
All elements must be synchronized
Control loop period determines how fast and how smoothly a mechanical system can run

Communications IC

Will be replaced by TSN

OpenIL.org



Hard real-time applications support

Built-in TSN and IEEE1588 Support

Open Software Repository and Community

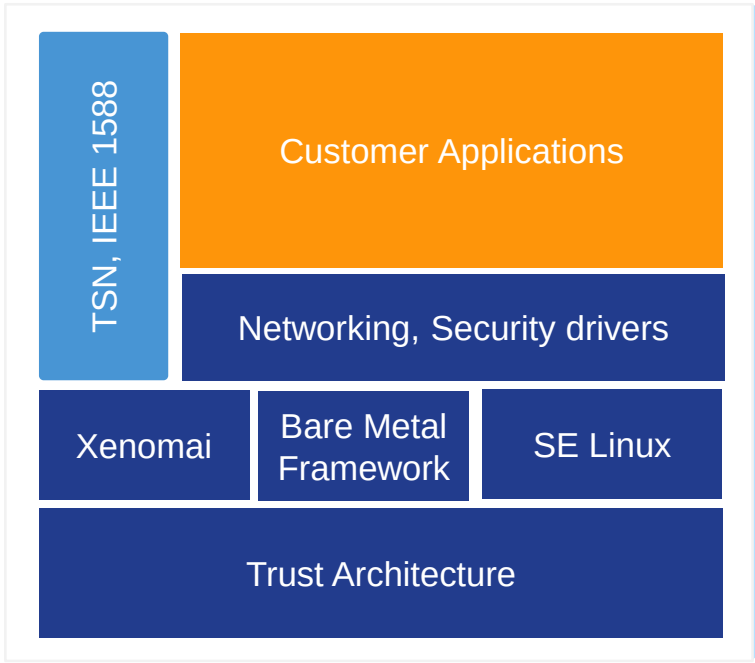
Built-in industrial-grade security

Built-in graphic display support for HMI Applications

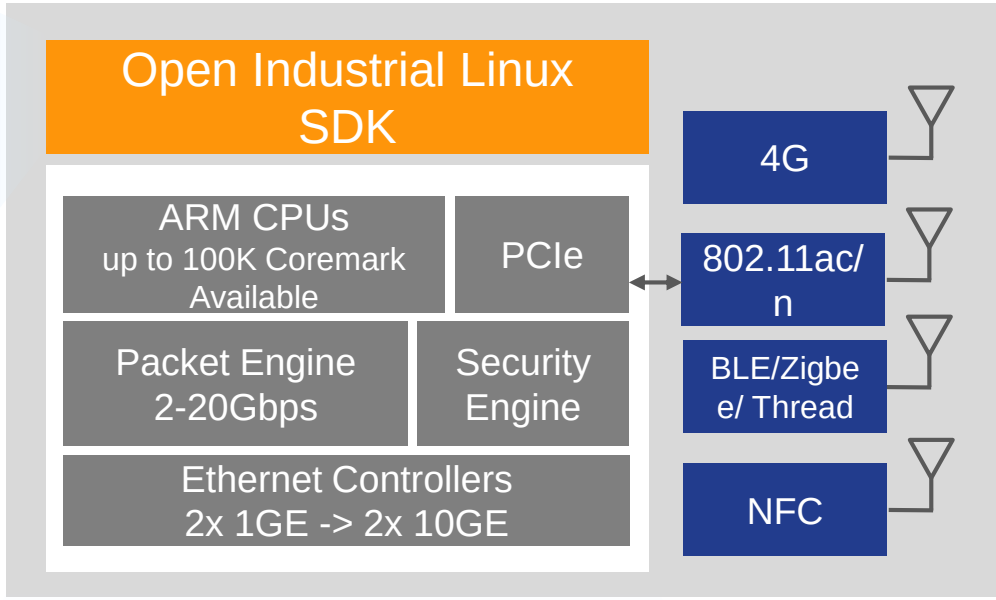
Support for various industrial networking protocols

Manageable via industrial control and networking protocols

OpenIL for Industrial Automation



Scalable Hardware



Determinism

Xenomai Linux, Bare Metal Framework
IEEE 1588, TSN

Security

SE Linux
OP-TEE

OpenIL Running on Scalable Portfolio of Devices

Currently Supported Devices
Single to Quad Core
32 and 64 bit Arm

LS1043A
- Cortex-A53
- 2-4 cores
- 1.6GHz
- 1/10G Ethernet, USB, PCI
- 5-10W

LS1046A
- Cortex-A72
- 2-4 cores
- 1.8GHz
- 1/10 G Ethernet, USB, PCI
- 10-12W

LS1012A
- Cortex-A53
- 1 core
- 1GHz
- 1-2W
- Ethernet, USB, PCI

LS1021A
- Cortex-A7
- 2 cores
- 1.2GHz
- 2W
- Ethernet, USB, PCI

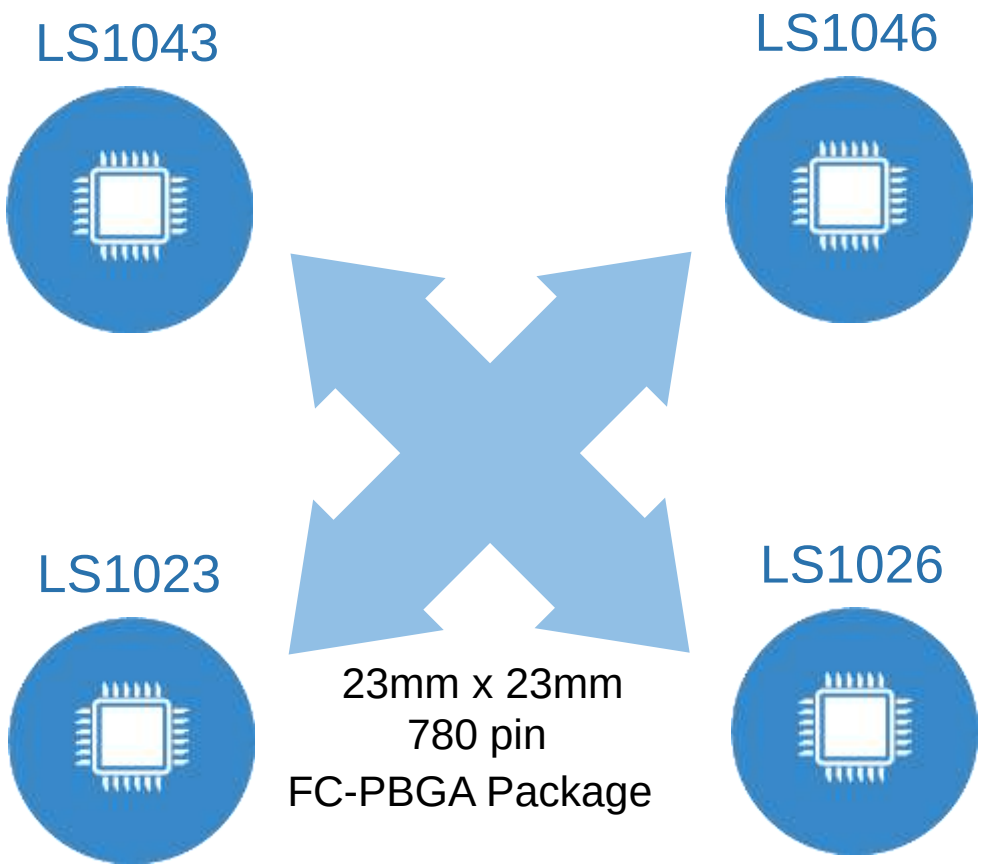
New Device Support in 2H 2018
Adding 3D GPU
Adding Integrated TSN

i.MX 6Dual/6Quad
- Cortex-A9
- 2-4 cores
- 800 MHz (Industrial)
- *2D/3D GPU*

LS1028A
- Cortex-A72
- 2 cores
- 1.3GHz
- 4-9W
- *Integrated TSN switch*
- *2D/3D GPU*

One Package – Four SoC Options

4x A53 1.6 GHz
4.2 W Typical
26,650 Coremark
Per core SpecINT
Per core SpecFP



4x A72 1.8 GHz
8.5 W Typical
45,330 Coremark
Per core SpecINT
Per core SpecFP

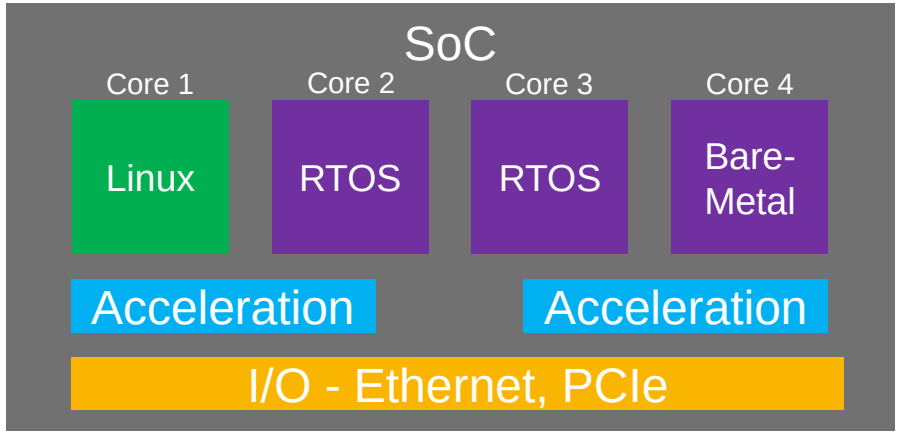
2x A53 1.0 GHz
2.5 W Typical
8,360 Coremark
Per core SpecINT
Per core SpecFP

2x A72 1.2 GHz
5.6 W Typical
15,000 Coremark
Per core SpecINT
Per core SpecFP

Deterministic Computing

Deterministic Computing for Industrial Workloads

Heterogeneous Software Model

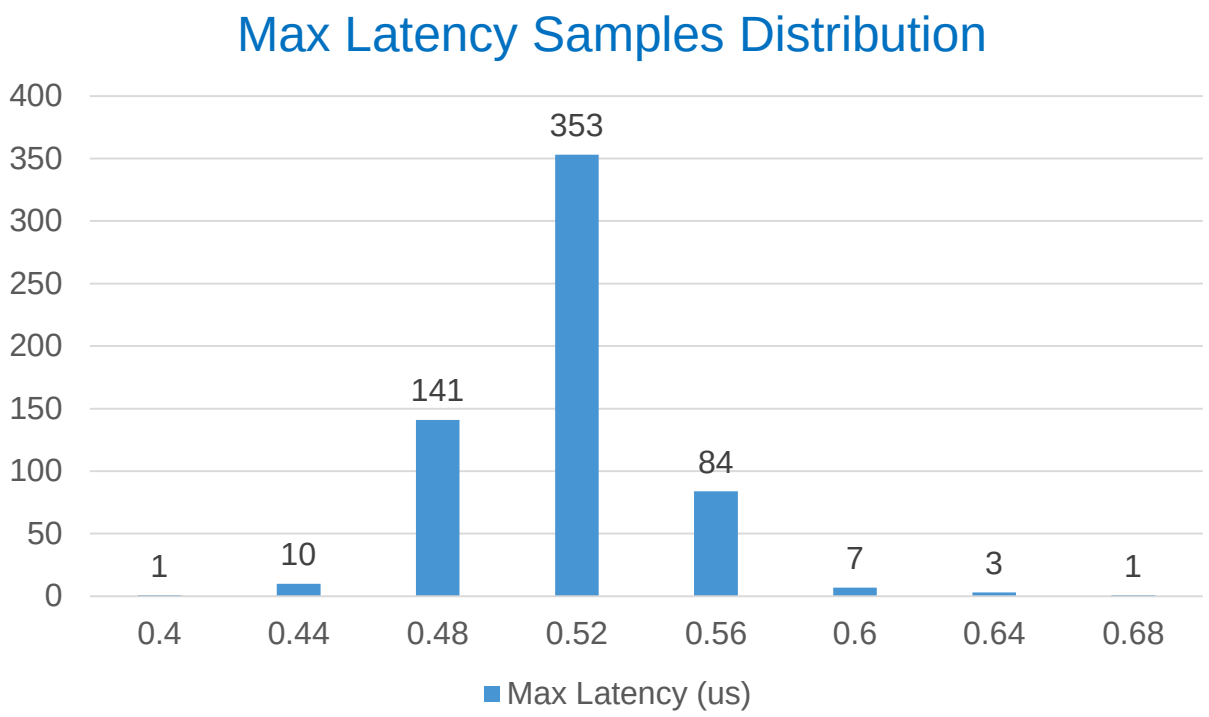


3 Levels of Real-Time Performance:

- Xenomai Mercury (PREEMPT-RT Patches)
  - LS10XX (Q1 2017)
- Xenomai Cobalt (Real-Time Co-Kernel)
  - LS10XX (Q2 2017)
- Bare-Metal Framework
  - LS10XX (Available Now!)

- Run management, communication software in Linux on 1 core
- Real-time applications running with RTOS (Xenomai) or Bare-Metal on other cores

Xenomai Latency Distribution on LS1043A



- Xenomai Cobalt 64-bit mode on LS1043A @ 1.6 GHz
- Measured using Xenomai latency tool
- Jitter < 450 ns
- Max latency of 680 ns

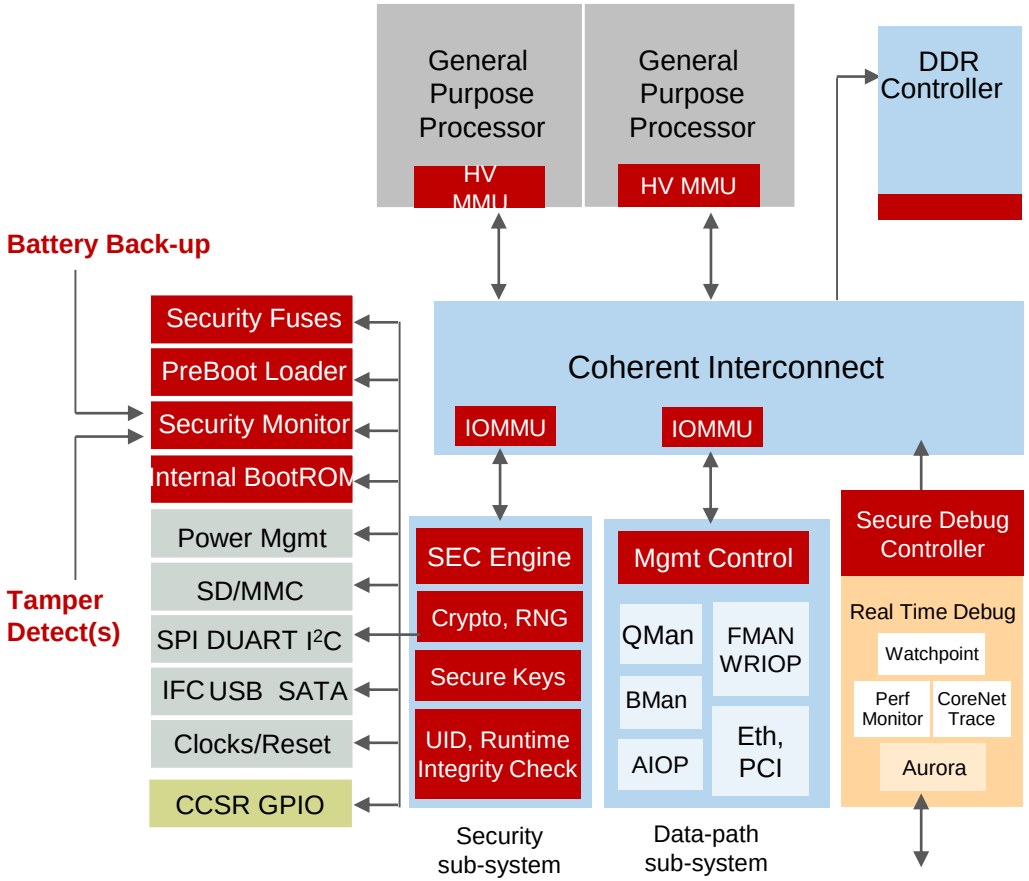
latency min (us)	latency avg (us)	latency max (us)	Duration
0.24	0.279	0.68	00:10:00

Protecting Industrial Devices

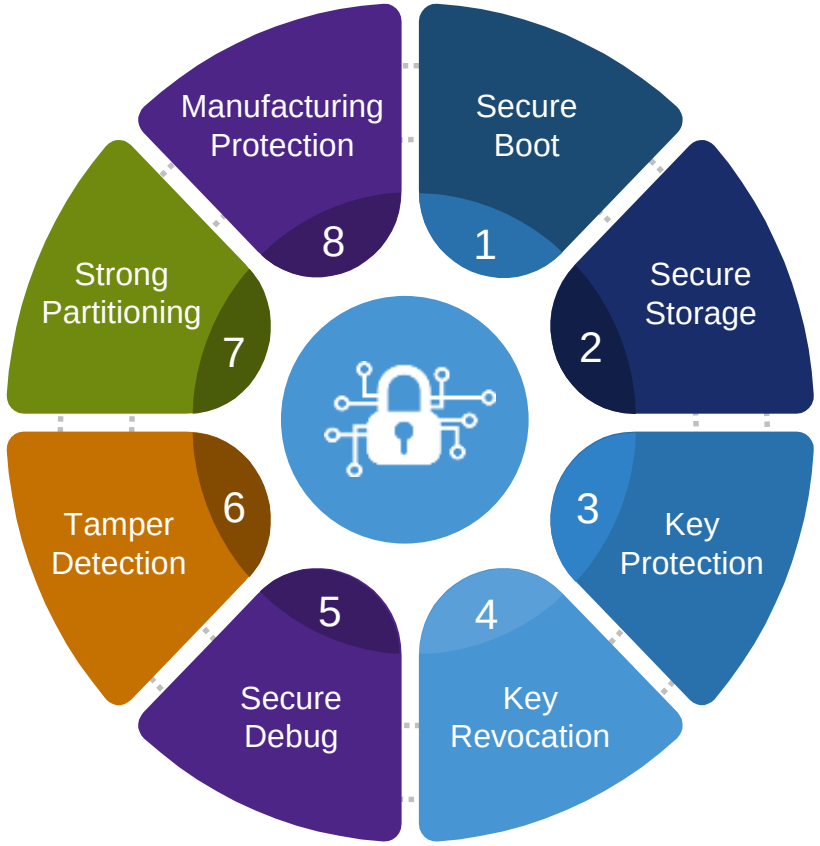
Root of Trust

Trust Architecture Provides a Trusted Platform

Hardware based security features to ease the development of trustworthy systems



All QorIQ SoCs support Trust Architecture



Runtime Access Control With SELinux

- Improved access control
- Policies control file access, network resources, and IPC
  - Finer grain access control
- Use cases:
  - Prevent remote login for certain types of users
  - Restrict access to files from the web

Time Synchronization

linuxptp

IEEE 1588 for Timing Synchronization

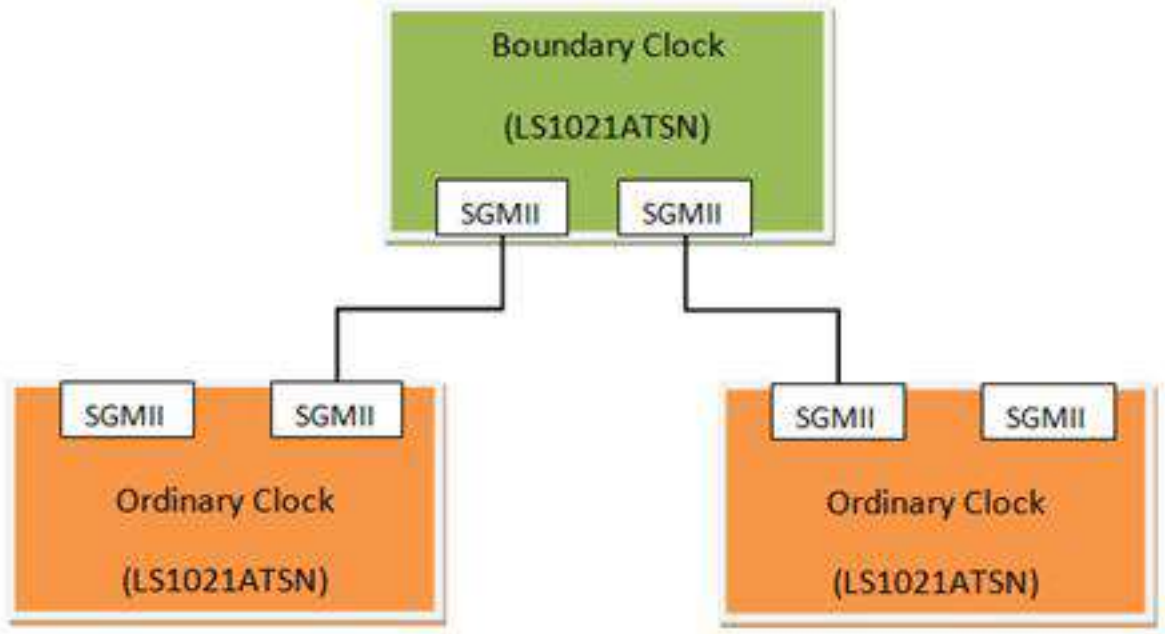
linuxptp support:

- LS1021A
- LS1043A
- LS1046A

Master/Slave
Boundary Clock Mode
802.1AS End Station

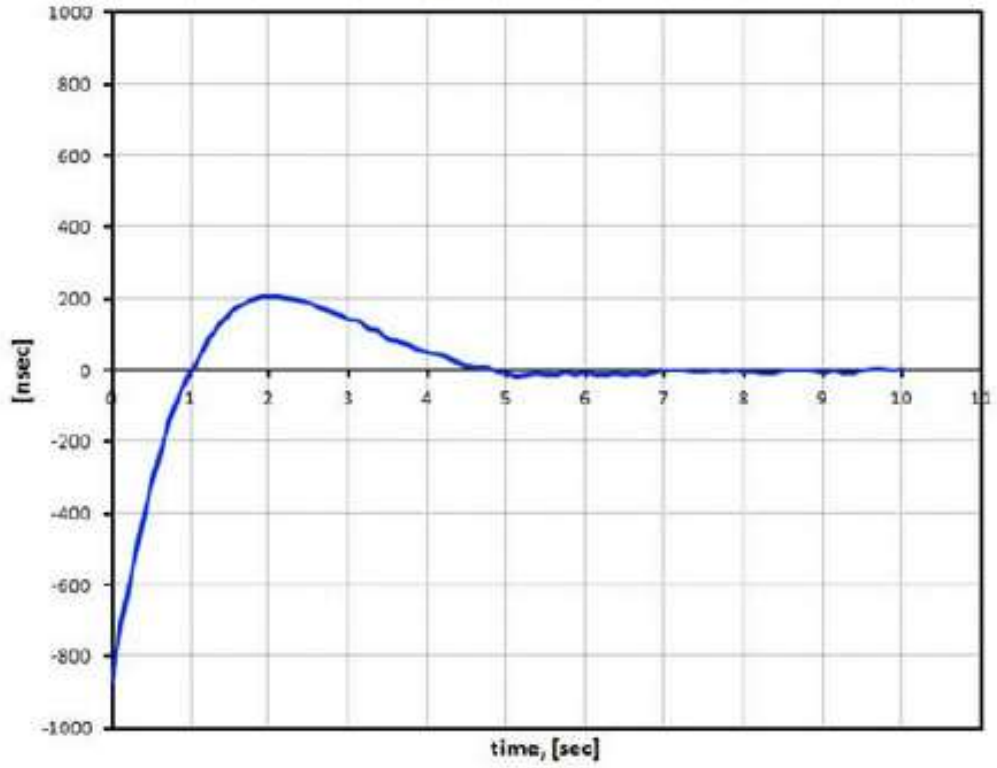
Synchronization within +/- 23 nsec for back to back boards

Example configurations and test results



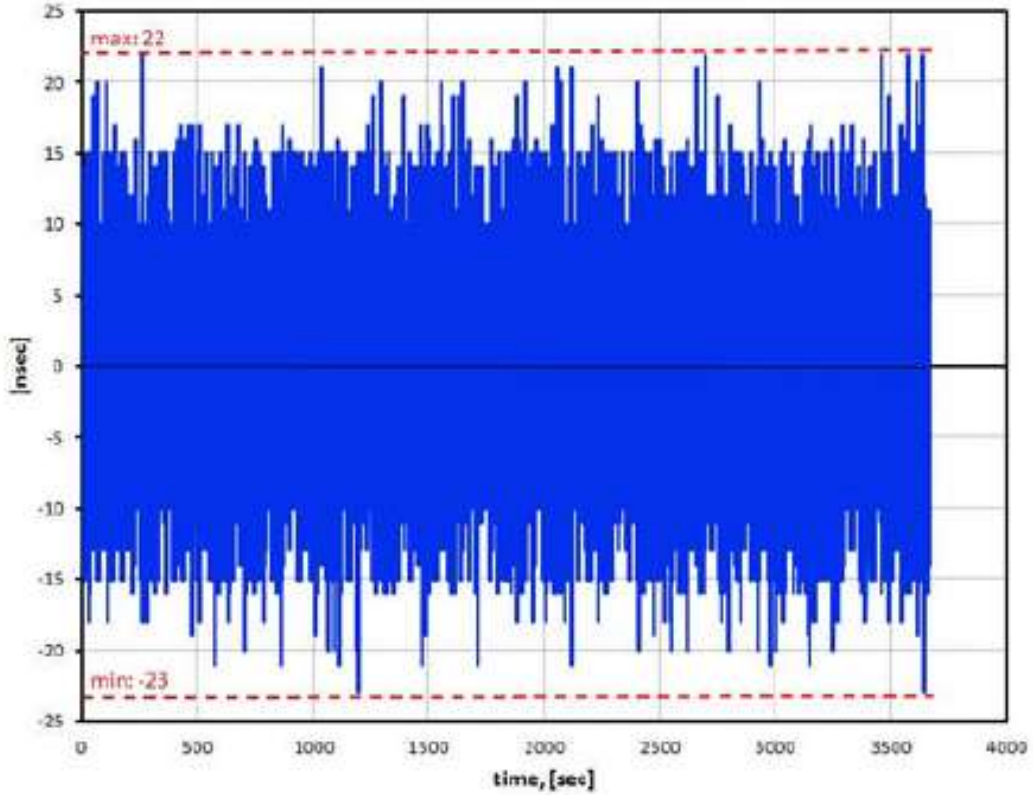
1588 Performance

Offset from Master, Startup



Timing settles within 5 seconds

Offset from Master, Stable State

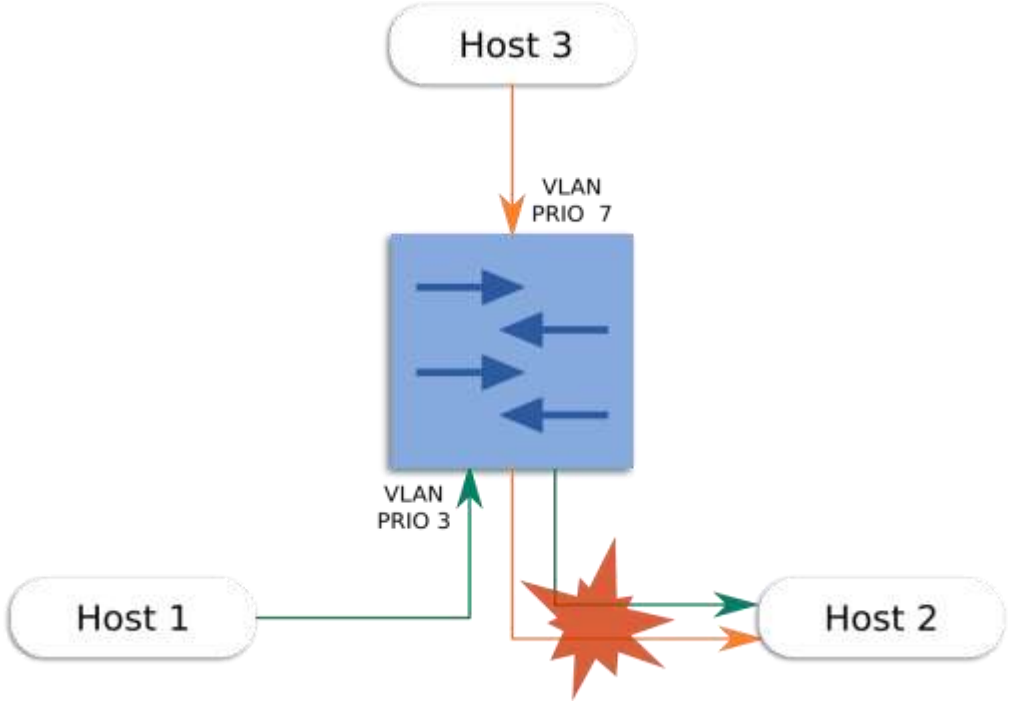


Accuracy within ±23 nsec

Deterministic Networking

Single Board TSN Demonstration

- 3 host Linux machines connected through a switch
- 2 TCP flows competing for bandwidth
- Flows bottlenecked because they are sharing the same link towards Host 2
- Combined throughput cannot exceed 1000Mbps
- Utilize TSN features to isolate flows
  - *Ingress Policing*: rate-limit traffic coming from Host 3
  - *Time Gating*: schedule the 2 flows on different time slots



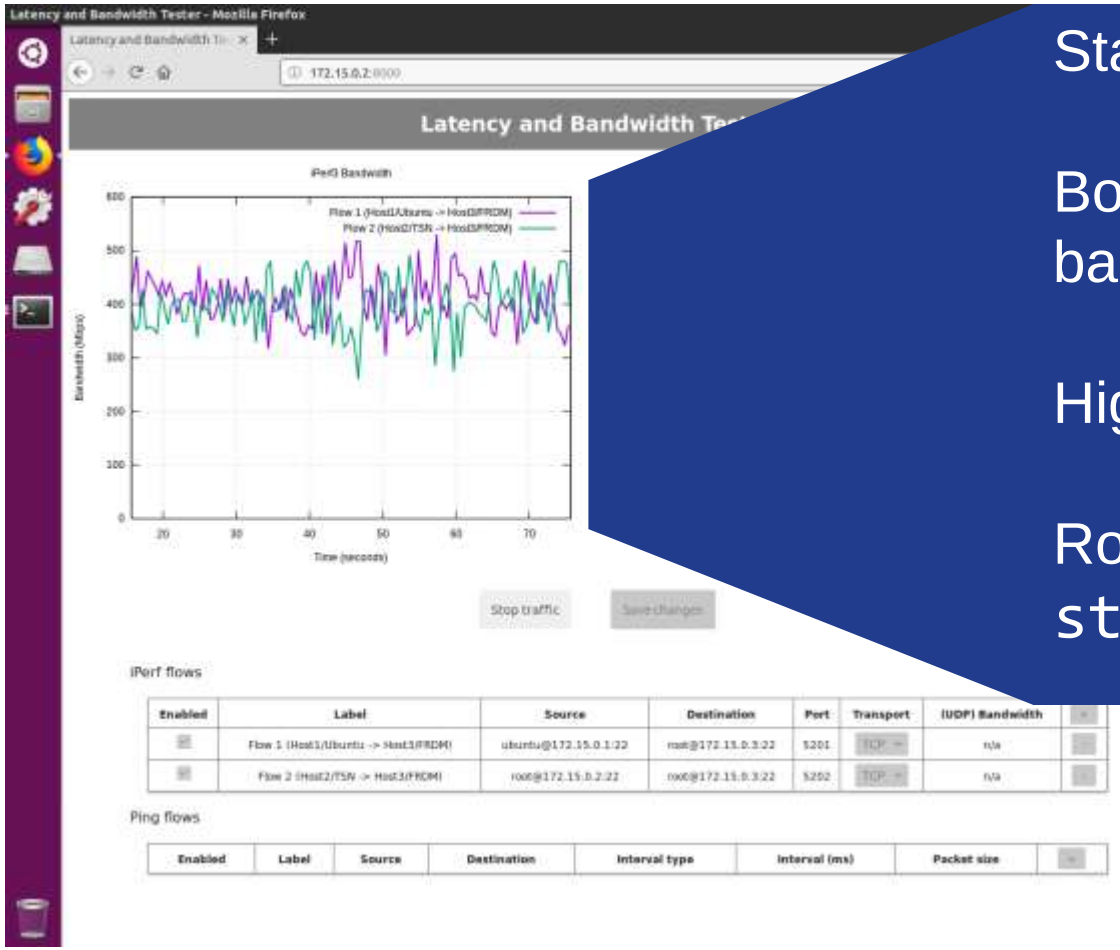
Demonstration Setup

LS1012A-FRDM

LS1021ATSN

ubuntu

Standard Ethernet Switch Settings



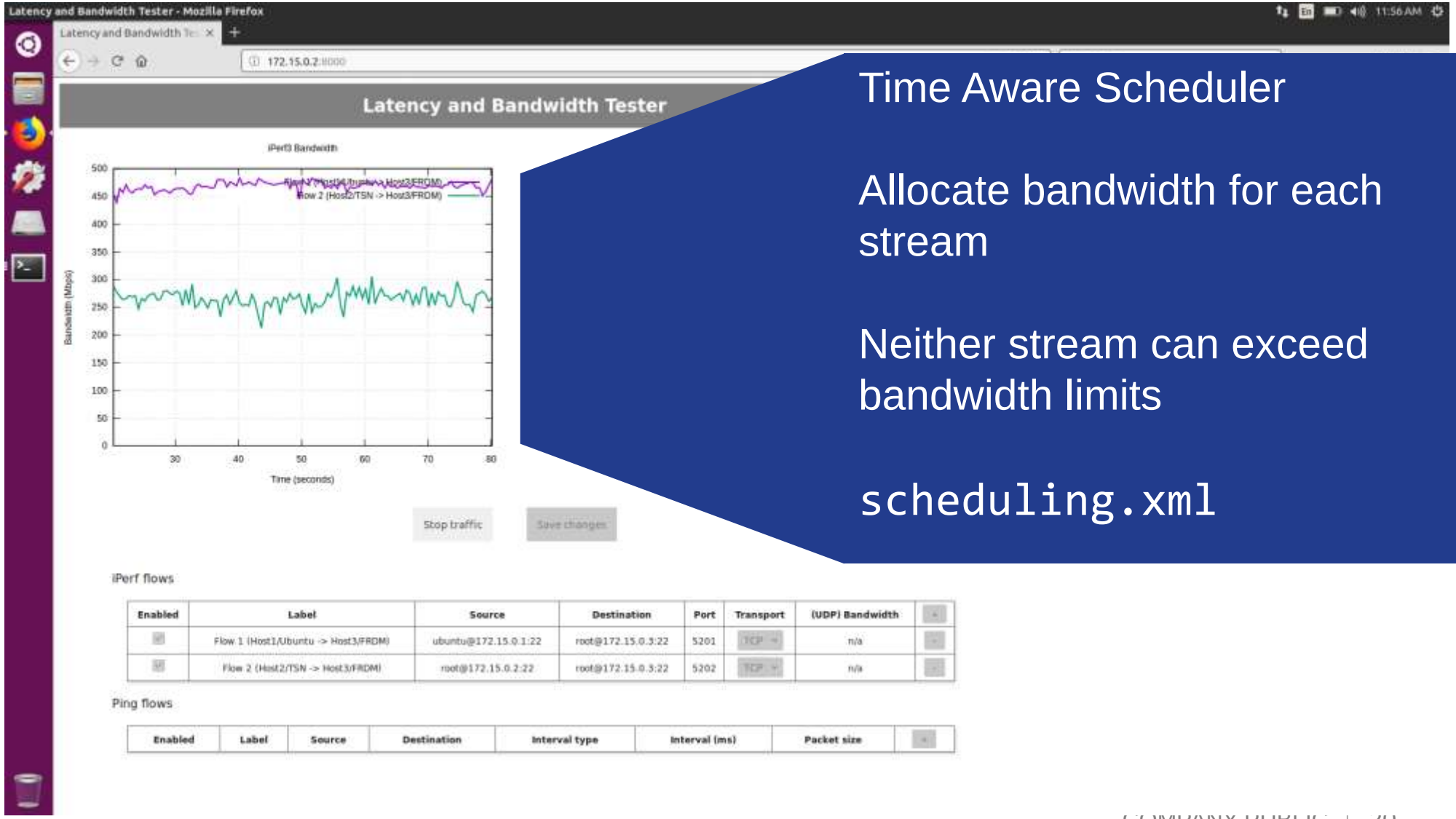
Standard Switch Settings

Both streams compete for bandwidth

High variation

Roughly equal distribution `standard.xml`

Time Aware Shaper



Time Aware Scheduler

Allocate bandwidth for each stream

Neither stream can exceed bandwidth limits

`scheduling.xml`

Start TSN on LS1021A-TSN – Enhance with LS1028A

LS1021A-TSN

TSN Features

- Time Aware Shaper (802.1Qbv)
- Per-Stream Filtering & Policing (802.1Qci)
- Credit Based Shaper (802.1Qav)
- Time Synchronization (802.1AS)

LS1028A

New TSN Features

- Frame Pre-emption (802.1Qbu)
- Frame Replication and Elimination (802.1CB)
- Cut-through Switching
- Cyclic Queuing and Forwarding (802.1Qch)
- 802.1AS-Rev

Supported by one SDK – Open Industrial Linux

LS1028A Reference Design

Front Panel

2x CAN FD Interfaces

2x UART

Back Panel

Full Size SD Card Slot

Up to 4K Display via DisplayPort

USB 3.0 Type C and Type A

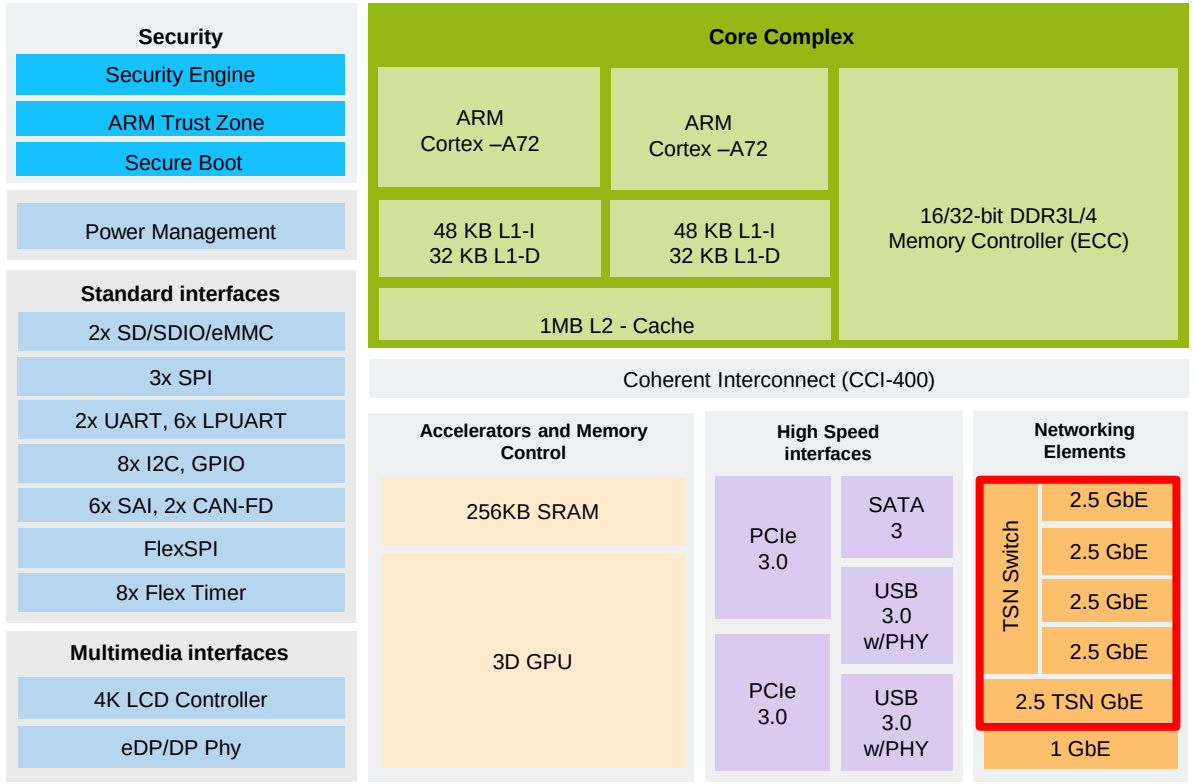
1G/100M/10M TSN Ethernet Controller

4 Switched 1G/100M/10M TSN Ethernet Ports

- Internal M.2 PCIe, SATA slots
- 2x mikroBUS™ sockets for Click Boards

Compelling Combination of IO, Computing and TSN

LS1028A: Dual ARM Cortex A72 Processor



Target Applications:

- Industrial Control, PLCs, Gateways
- Automotive
- Professional Audio/Video
- IoT Gateways
- Human Machine Interface

Package

- 17x17mm, 0.75mm pitch FC-PBGA

Core complex

- 2x 64-bit Cortex-A72 with Neon SIMD engine
- Speed up to 1300 MHz
- Parity and ECC protected 48 KB L1 instruction and 32 KB L1 data cache
- 1 MB L2 cache with ECC protection

Basic peripheral and Interconnect

- 2x USB 3.0 OTG controllers with integrated PHY
- 2x eSDHC controllers supporting SD/SDIO 4.0
- 2x CAN-FD controllers
- 8x UART serial ports

Networking elements

- Four Port TSN Ethernet Switch up to 2.5 Gbps on each port
- Up to four SGMII supporting 1 Gbps
- Up to one USXGMII supporting 2.5 Gbps
- Up to one QSGMII
- Up to one RGMII
- 2x PCI Express Gen 3 controllers
- 1x SATA Gen 3.0 controller

Accelerators and Memory Control

- 1x 16/32-bit DDR3L/4 Controller with ECC support up to 1.6 GT/s
- Time Sensitive Networking (TSN) Ethernet Switch
- Security Engine (SEC)
- QorIQ Trust architecture: Secure boot, ARM Trust zone and security monitor

Qualification

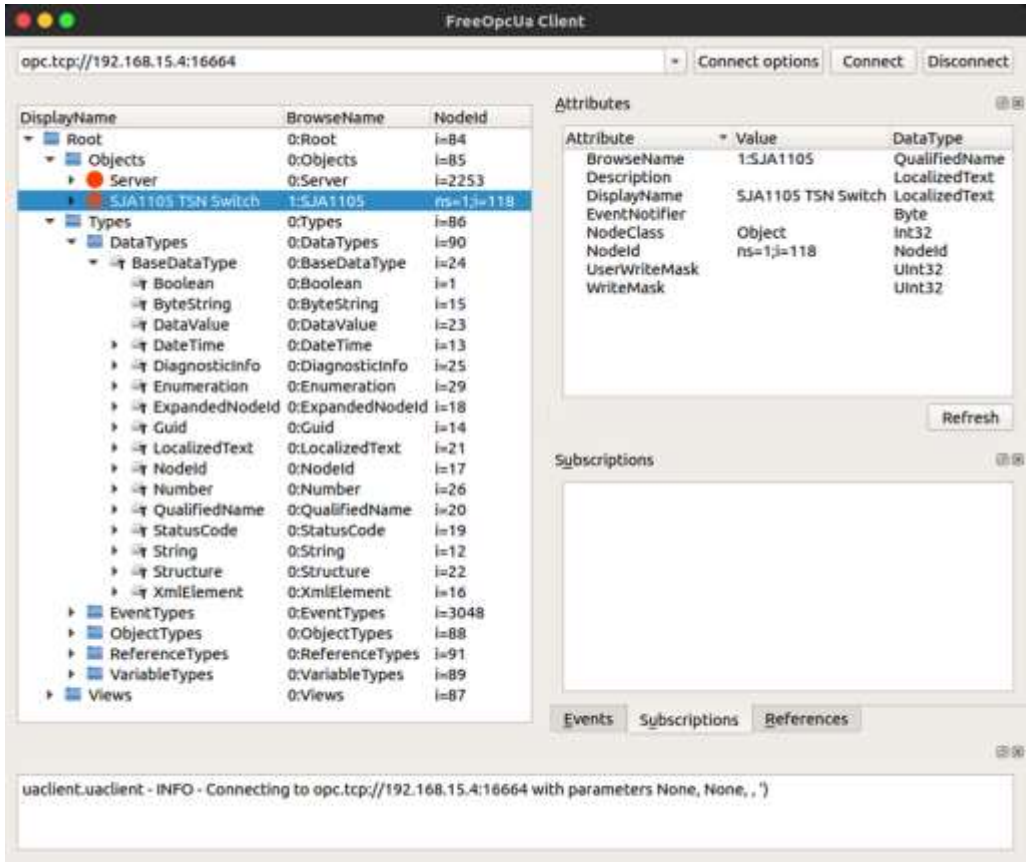
- Commercial and extended temperature (support for 125C Tj)

Power

- 5W TDP

OPC UA over TSN for Industry 4.0 Communications

- OpenIL integrates with Open62541
  - Open source C implementation of OPC UA
  - Mozilla Public License v2.0
  - server side capabilities
- LS1021A Running OPC UA Server
  - Providing switch statistics
  - Access via FreeOpcUa Client GUI



Open Industrial Linux Driving Industrial Control

- Growing set of supported processors
  - Coverage across Layerscape and i.MX
- Deterministic Processing
  - Xenomai Linux
  - Bare Metal Framework
- Secure industrial systems with root of trust and SELinux
- Synchronized and Deterministic Networking
  - 1588
  - TSN

Open Industrial

References and Additional Information

- Open Industrial Linux User Guide
- Open Industrial Linux Bare Metal Framework Developer Guide
- Application Note: AN3423 – Support for IEEE™ 1588 Protocol in PowerQUICC and QorIQ Processors
- LS1046A Reference Design Board
- LS1043A Reference Design Board
- LS1012A Reference Design Board
- LS1021ATSN Reference Design Board
- LS1028A Layerscape SoC with integrated TSN

SECURE CONNECTIONS
FOR A SMARTER WORLD

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