MCF5307 PLL

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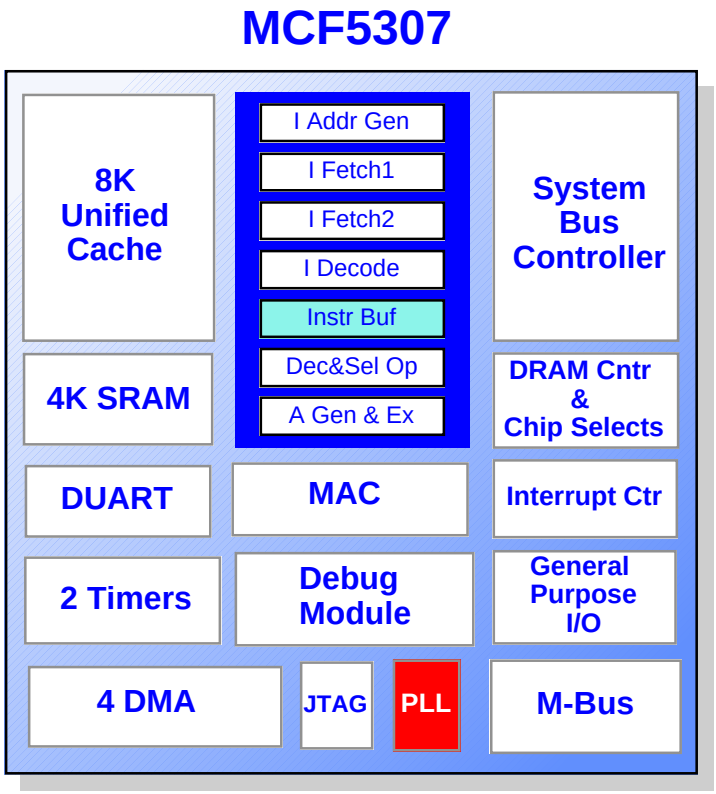
- Clock multiplied PLL
- Low power mode supported
- 75 MIPs at 90MHz core clock frequency
- 55 MIPs at 66 MHz core clock frequency
- Offered at 45/90 MHz, 30/90 MHz, 22.5/90 MHz at standard temperature
- Offered at 33/66 MHz, 22/66 MHz, 16.5/66 MHz at standard and extended temperature
- Fully Static 3.3-volt operation w/ 5V tolerant pads
- 208 QFP package



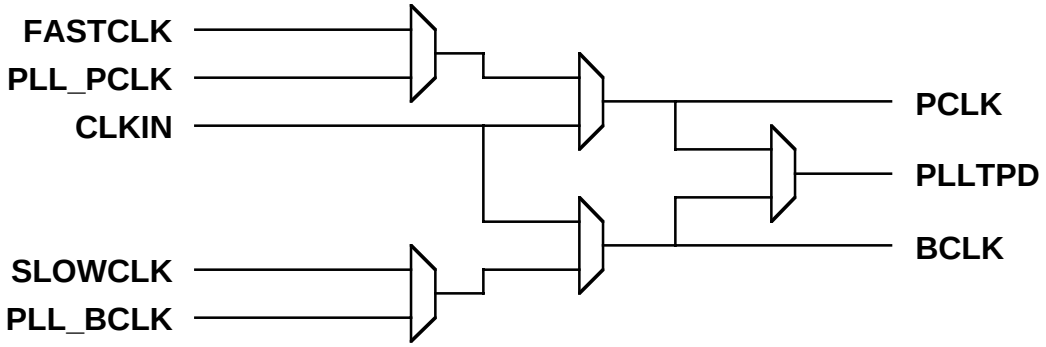
PLL OPERATION MODES

- **NORMAL MODE- User supplies a range of 16.67 to 50 MHz that will be used to create the processor clock (PCLK) and the bus clock output (BCLKO). The bus clock output can be programmed to 1/2, 1/3, or 1/4 of the frequency of PCLK. This divisor and the frequency input range is programmed by two input pins on the 5307 during RESET.**

- **REDUCE POWER MODE- The PLL output PCLK can be shut off and turned on again without loss of state in the core Igoic. This state is entered by a combination of executing the STOP instruction and programming a control bit in the System Configuration Register.**

- **RESET- The PLL is reset when it receives the RESET* signal input directly from the 5307 pin. The PLL then delivers RESETO* to the rest of the 5307 and as an external pin. Eight configuration signals are also sampled during reset.**

5307 PLL Specification



- PLL lock time: 2ms
- Input frequency(CLKIN): 16.67 to 50 MHz
- Output Frequency(BCLK): PCLK/2 (16.7MHz through 50MHz)
PCLK/3 (11.1 MHz through 33.3MHz)
PCLK/4 (8.25 MHz through 25 MHz)
- Internal Processor Clock PCLK=CLKINx2 (33.3MHz through 100MHz)
- Duty Cycle (PCLK & BCLK) (50+/-5)%
- Operating temperature -40 to +85 C
- Normal Operating Voltage 3V-3.6V +-50mV
- Output Jitter <1ns
- Reduced Power PCLK can be shut off
- Output skew(PCLK to BCLK) +-225ps

MCF5307 RESET OPERATION

• During reset six configuration signals are sampled by the PLL logic. These configuration signals are muxed with data lines and are only sampled at reset.

- •FREQ[1:0]- determine frequency range of CLKIN
- •DIVIDE[1:0]- determine BCLK/PCLK ration
- •CS_CONFIG[2:0]- determine global chip select0's (CS0*) default port size and wait state configuration out of reset.

FREQ[1:0]	Freqency of CLKIN(MHz)
00	16.6-27.999
01	28-39.999
10	39-50
11	RSVD

DIVIDE[1:0]	Ratio of BCLK/PCLK
01	RSVD
10	1/2
11	1/3
00	1/4

CS_CONFIG1	CS_CONFIG0	Boot CS0* Port Size
0	0	32-bit
0	1	8-bit
1	0	16-bit
1	1	16-bit

CS_CONFIG2	Boot CS0* Auto Ack
0	Disabled
1	Enabled w/ 15 wait states

MCF5307 RESET OPERATION