



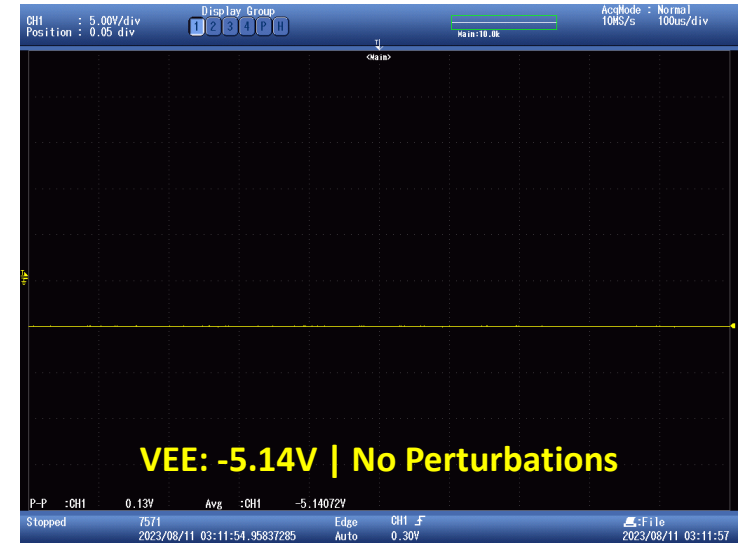
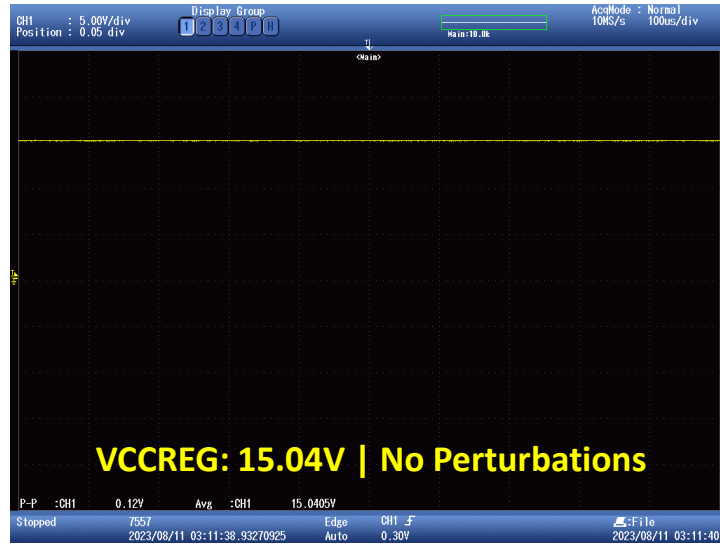
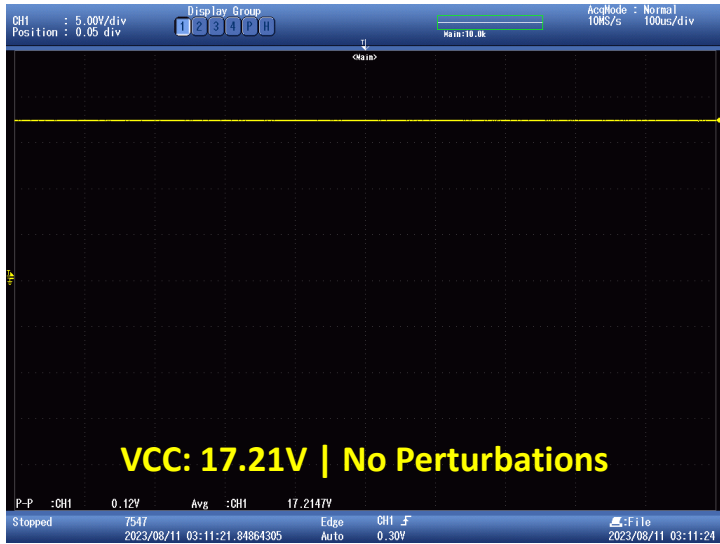
# GD3160 Gate Drive Board | Supply Rail Measurements

PASSION FOR TECHNOLOGY.



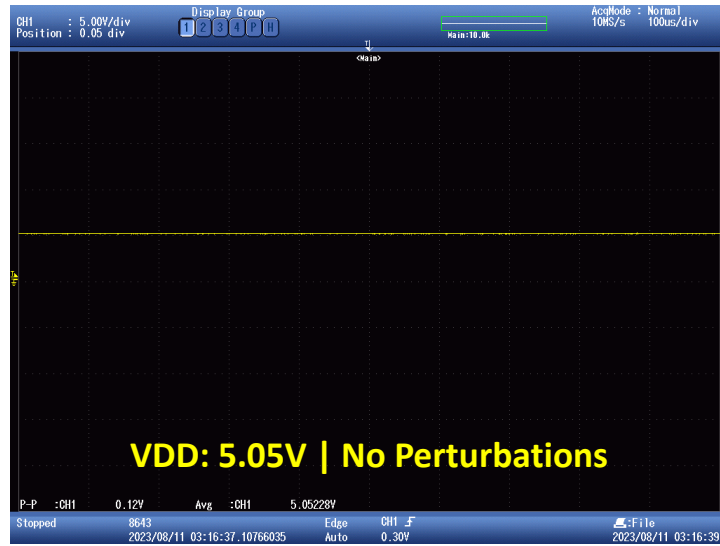
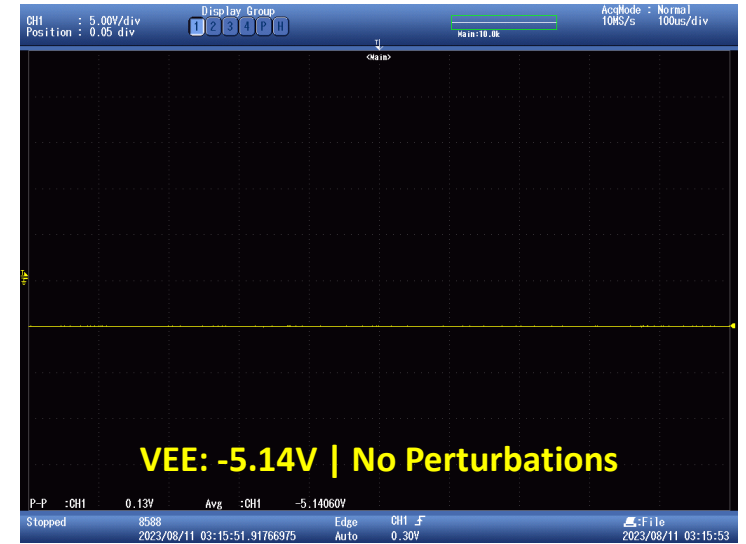
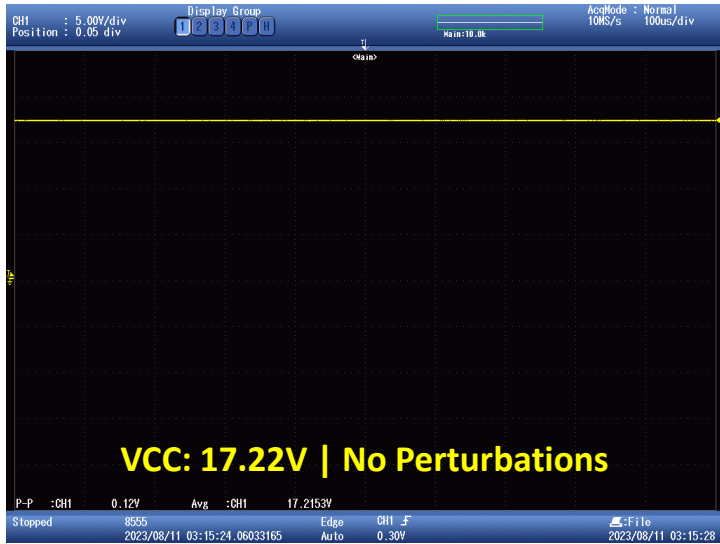
## High Side | Phase A Supply Rail Measurements

# High Side Phase A | Static Load (VCC, VCCREG, VEE, VREF, VDD)



10MS/s  
100µs per horizontal division

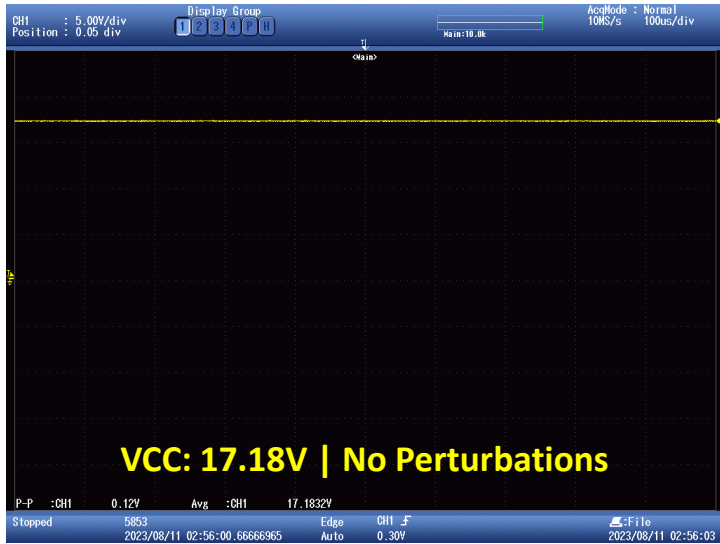
# High Side Phase A | SPI Polling (VCC, VCCREG, VEE, VREF, VDD)



10MS/s  
100µs per horizontal division

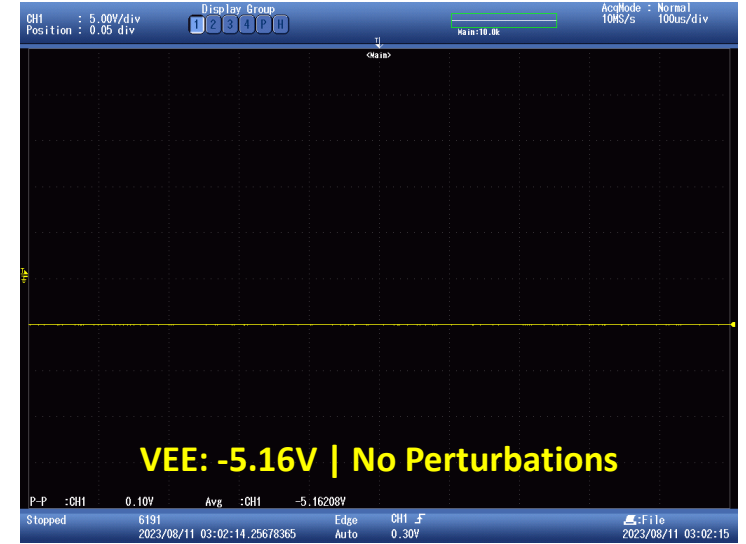
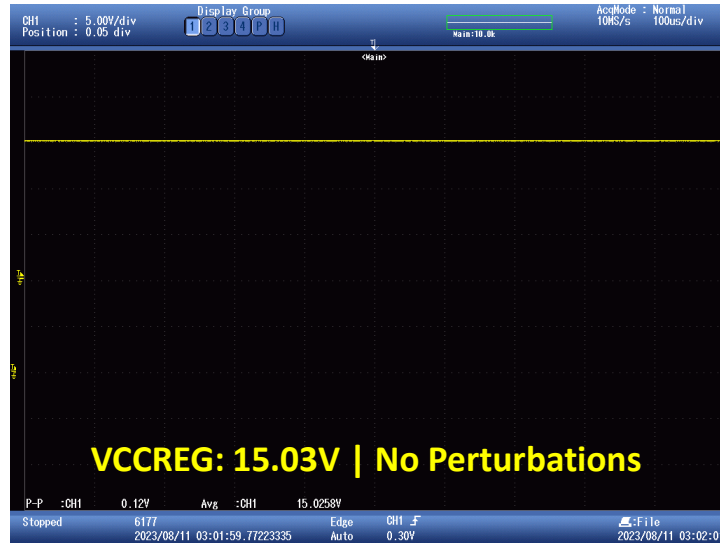
## High Side | Phase B Supply Rail Measurements

# High Side Phase B | Static Load (VCC, VCCREG, VEE, VREF, VDD)



10MS/s  
100 $\mu$ s per horizontal division

# High Side Phase B | SPI Polling (VCC, VCCREG, VEE, VREF, VDD)

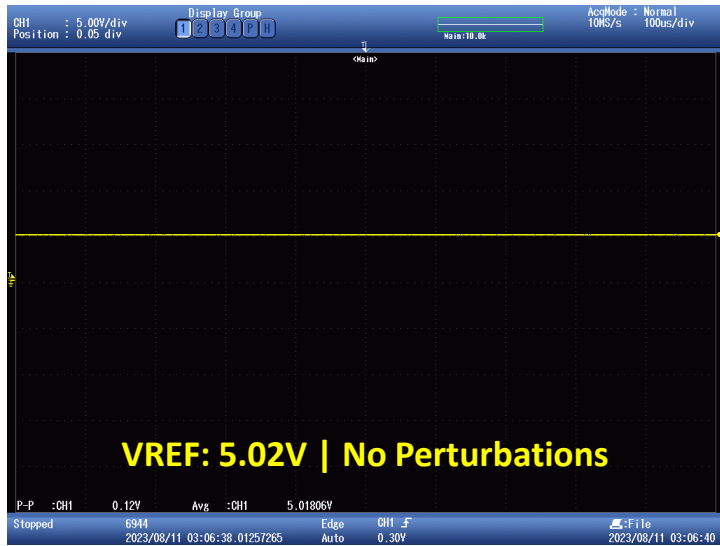
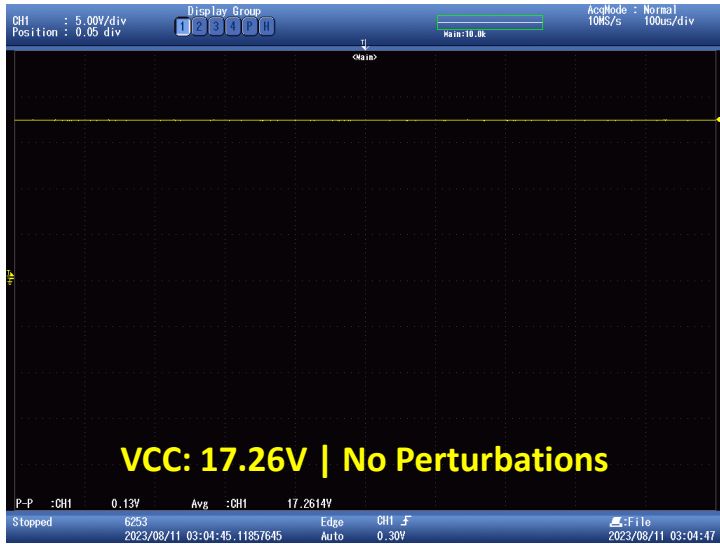


10MS/s  
100µs per horizontal division

## High Side | Phase C Supply Rail Measurements

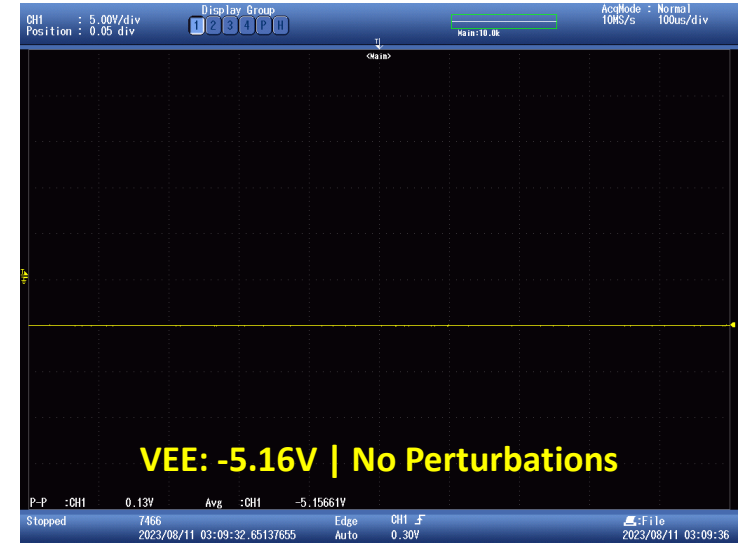
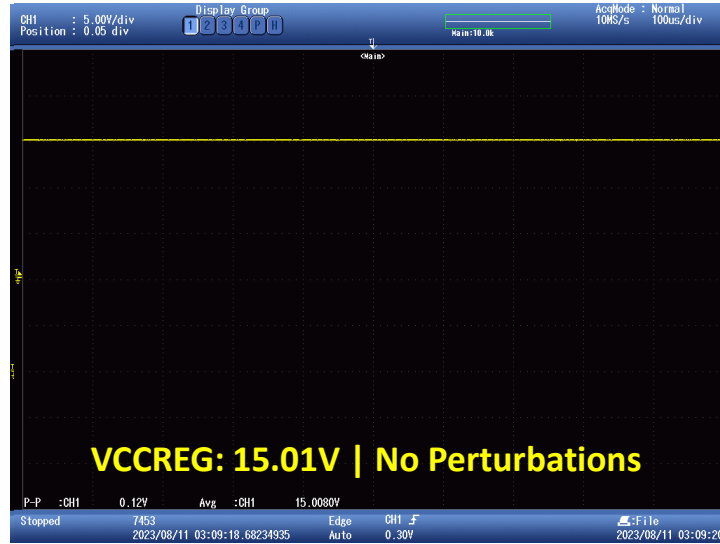
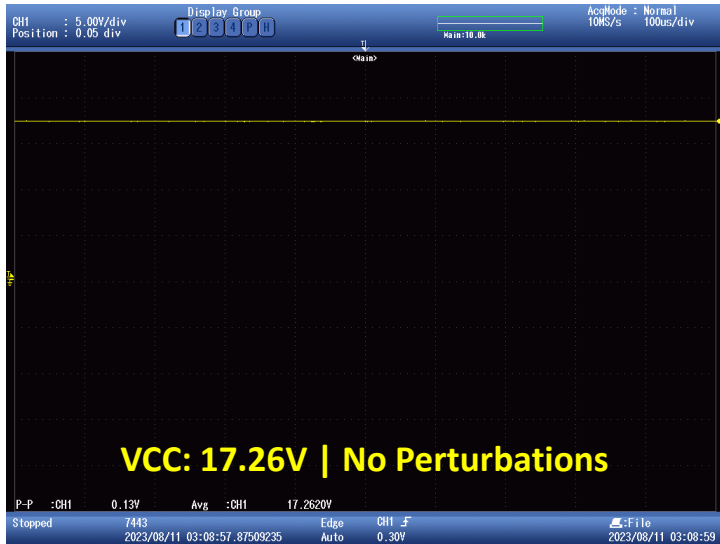


# High Side Phase C | Static Load (VCC, VCCREG, VEE, VREF, VDD)



10MS/s  
100µs per horizontal division

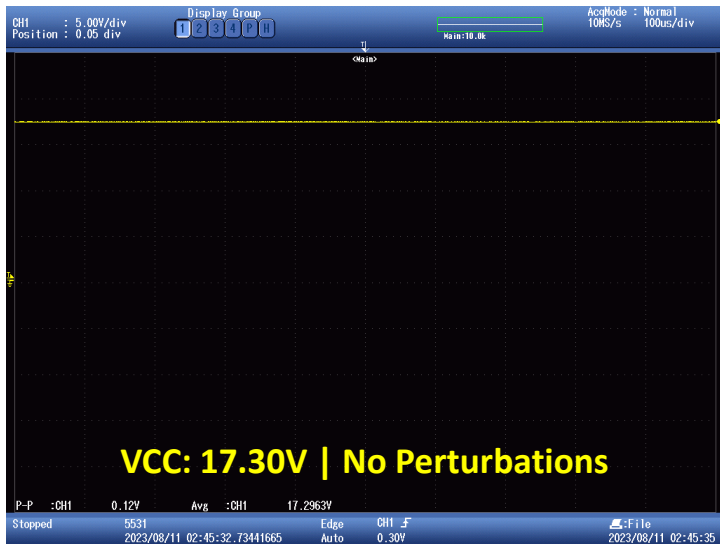
# High Side Phase C | SPI Polling (VCC, VCCREG, VEE, VREF, VDD)



10MS/s  
100µs per horizontal division

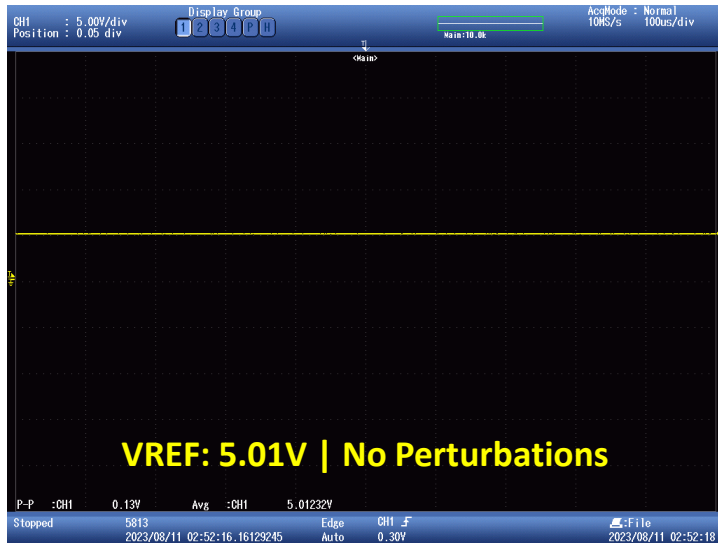
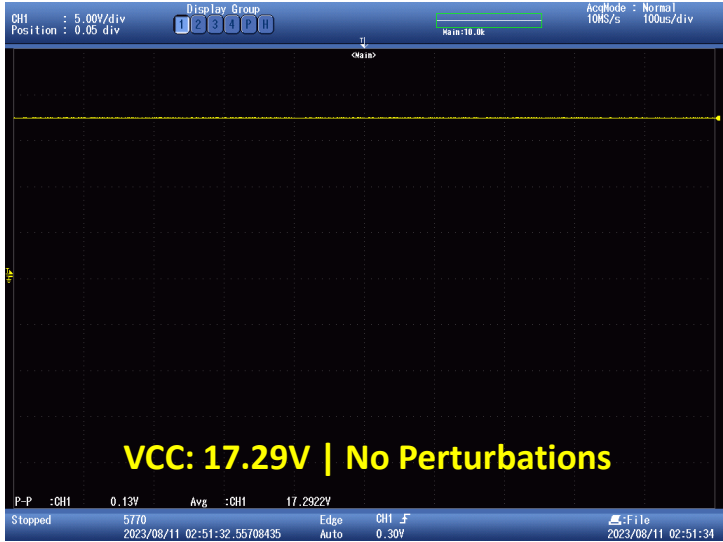
## Low Side | Phase A Supply Rail Measurements

# Low Side Phase A | Static Load (VCC, VCCREG, VEE, VREF, VDD)



10MS/s  
100µs per horizontal division

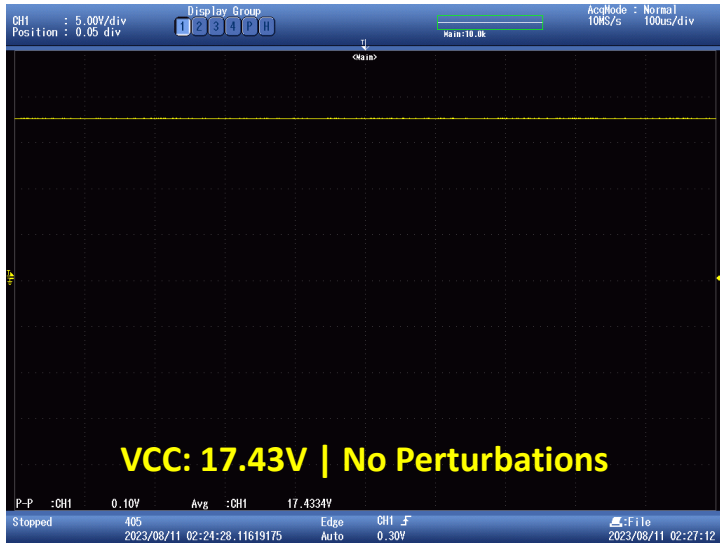
# Low Side Phase A | SPI Polling (VCC, VCCREG, VEE, VREF, VDD)



10MS/s  
100 $\mu$ s per horizontal division

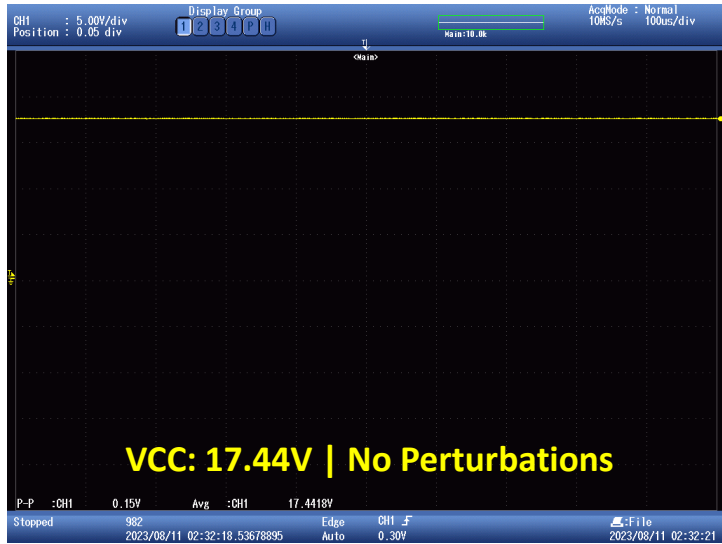
## Low Side | Phase B Supply Rail Measurements

# Low Side Phase B | Static Load (VCC, VCCREG, VEE, VREF, VDD)



10MS/s  
100µs per horizontal division

# Low Side Phase B | SPI Polling (VCC, VCCREG, VEE, VREF, VDD)

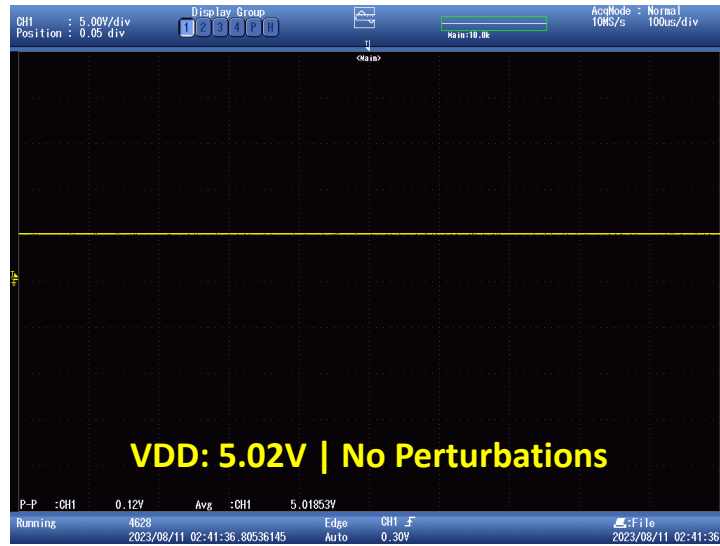
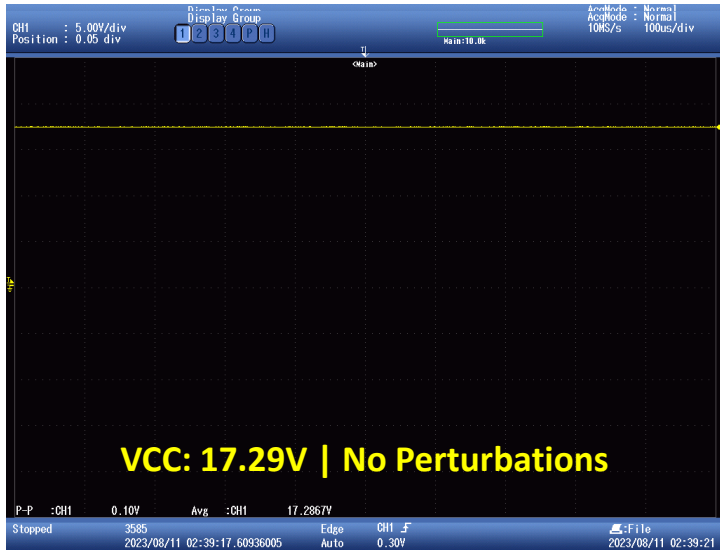


10MS/s  
100µs per horizontal division



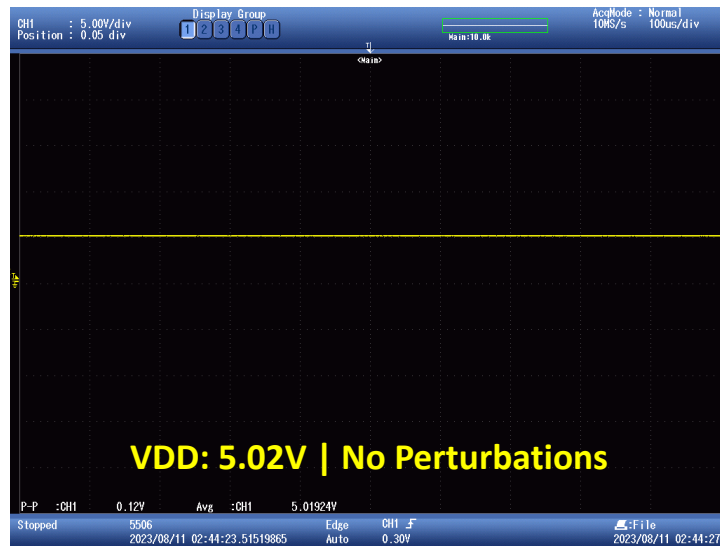
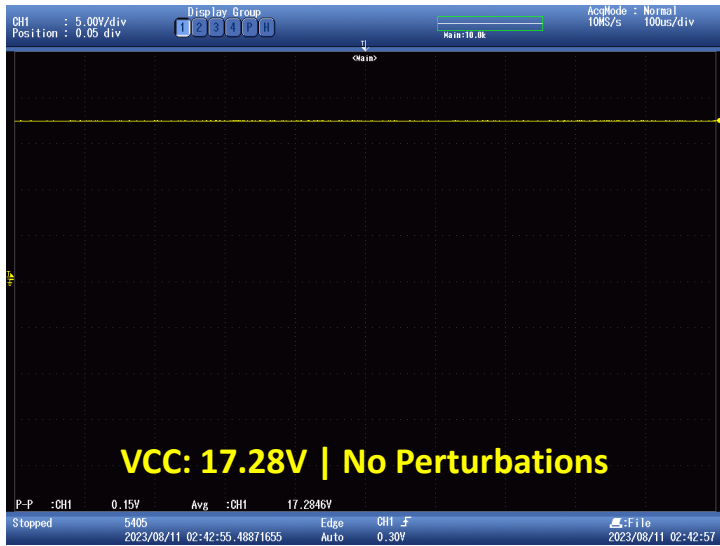
## Low Side | Phase C Supply Rail Measurements

# Low Side Phase C | Static Load (VCC, VCCREG, VEE, VREF, VDD)



10MS/s  
100 $\mu$ s per horizontal division

# Low Side Phase C | SPI Polling (VCC, VCCREG, VEE, VREF, VDD)



10MS/s  
100µs per horizontal division

# Supply Rail Measurement Summary

# Supply Rail Measurement Summary

## Static Conditions

Supply Rail	High Side Drivers			Low Side Drivers		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
VCC	17.21	17.18	17.26	17.30	17.43	17.29
VCCREG	15.04	15.03	15.01	14.99	14.99	14.99
VEE	-5.14	-5.16	-5.16	-5.13	-5.09	-5.14
VREF	5.02	5.02	5.02	5.01	5.02	5.02
VDD	5.05	5.06	5.02	5.05	5.04	5.02

## Continuous SPI Bus Polling

Supply Rail	High Side Drivers			Low Side Drivers		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
VCC	17.22	17.19	17.26	17.29	17.44	17.28
VCCREG	15.04	15.03	15.01	14.99	14.99	14.99
VEE	-5.14	-5.16	-5.16	-5.13	-5.08	-5.14
VREF	5.02	5.02	5.02	5.01	5.02	5.02
VDD	5.05	5.08	5.03	5.05	5.04	5.02

## Supply Rail Voltages Measured by GD3160 | SPI Readouts

## GD3160 | High Side Measurements

### Phase A

### Phase B

### Phase C

#### ADC overview

DEVICE 4 Values (VREF = 5.0V)				DEVICE 5 Values (VREF = 5.0V)				DEVICE 6 Values (VREF = 5.0V)			
Signal name:	User value:	Raw ADC value:		Signal name:	User value:	Raw ADC value:		Signal name:	User value:	Raw ADC value:	
ADC_IGBT_TEMP	3.96 V	812	OK	ADC_IGBT_TEMP	3.97 V	813	OK	ADC_IGBT_TEMP	3.97 V	814	OK
ADC_AMUX	0.0 V	0		ADC_AMUX	0.0 V	0		ADC_AMUX	0.0 V	0	
ADC_VCC	17.0 V	580	OK	ADC_VCC	17.0 V	579	OK	ADC_VCC	17.1 V	582	OK
ADC_VCCREG	14.9 V	507	OK	ADC_VCCREG	14.8 V	506	OK	ADC_VCCREG	14.8 V	504	OK
ADC_VEE	-5.18 V	670	OK	ADC_VEE	-5.19 V	669	OK	ADC_VEE	-5.19 V	669	OK
ADC_DIE_TEMP	36.0 degC	666		ADC_DIE_TEMP	37.01 degC	664		ADC_DIE_TEMP	35.5 degC	667	

## GD3160 | Low Side Measurements

### Phase A

### Phase B

### Phase C

#### ADC overview

DEVICE 1 Values (VREF = 5.0V)				DEVICE 2 Values (VREF = 5.0V)				DEVICE 3 Values (VREF = 5.0V)			
Signal name:	User value:	Raw ADC value:		Signal name:	User value:	Raw ADC value:		Signal name:	User value:	Raw ADC value:	
ADC_IGBT_TEMP	0.13 V	26	OK	ADC_IGBT_TEMP	2.96 V	607	OK	ADC_IGBT_TEMP	3.0 V	615	OK
ADC_AMUX	0.0 V	0		ADC_AMUX	0.0 V	0		ADC_AMUX	0.0 V	0	
ADC_VCC	17.1 V	585	OK	ADC_VCC	17.2 V	586	OK	ADC_VCC	17.0 V	581	OK
ADC_VCCREG	14.8 V	505	OK	ADC_VCCREG	14.7 V	503	OK	ADC_VCCREG	14.8 V	504	OK
ADC_VEE	-5.18 V	670	OK	ADC_VEE	-5.12 V	674	OK	ADC_VEE	-5.18 V	670	OK
ADC_DIE_TEMP	26.92 degC	684		ADC_DIE_TEMP	27.93 degC	682		ADC_DIE_TEMP	26.92 degC	684	



# PASSION FOR **TECHNOLOGY.**

## Disclaimer

Rheinmetall does not guarantee the accuracy or completeness of the information contained in this document, nor of that contained in any other document provided at any other time. While this information has been prepared in good faith, no representation or warranty, express or implied, is or will be made, and no responsibility or liability is or will be accepted.