External components calculation for MPC5634L ADC application

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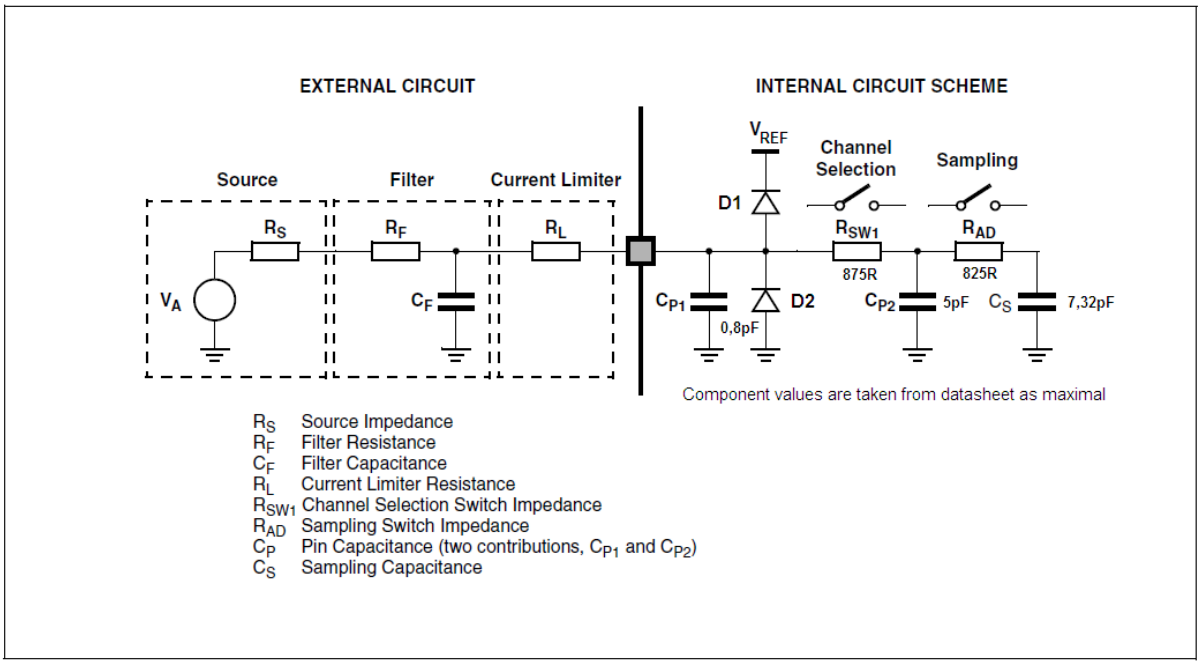
This document explains evaluation of components for passive external ADC input circuitry for MPC5634L. Following picture shows all components used in this ADC application:



R_L - Current limiter

This resistor limits current flowing from filter capacitor C_F into the analog input pin (otherwise during power down an excessive current will flow through D1):

$$R_L = \frac{V_{REF}}{I_{INJPAD}}$$

where V_{REF} is reference voltage (always the same as maximal input voltage) and I_{INJPAD} is maximal input current for the pad.

Example: For V_{REF} = 5V:

$$R_L = \frac{5V}{10mA} = 500\Omega$$ *you can use resistor **510R***

C_F – Filter capacitor

Filter capacitor is used together with R_F to create passive RC filer for reduction of input signal bandwidth. Anyhow, in ADC sampling phase, the sampling capacitor C_S is charged from C_F. Thus C_F should have sufficient charge to fill the C_S without noticeable voltage drop:

$$C_F = 2^{(N+1)} * C_S \qquad \text{for voltage drop} < ½ \text{ LSB}$$

where **N** is number of ADC bits.

Example: For 12bit ADC:

$$C_F = 2^{13} * 7{,}32pF = 59{,}9\ nF$$ *you can use **68n** cap*

R_F – Filter resistor

Filter resistor is used together with C_F to create passive low-pass RC filer for reduction of input signal bandwidth. According to Nyquist theorem:

$$R_F = \frac{1}{\pi f_S C_F}$$

where f_S is sampling frequency.

Example: For $\mathbf{f_S}$ = 1 kHz and $\mathbf{C_F}$ = 68nF:

$$\mathbf{R_F} = 1/ (3.14 * 1E3 *68E-9) = \mathbf{4681\Omega}$$ *you can use resistor* ***4K7***

Note: Remember, that source internal resistance $\mathbf{R_S}$ is a part of filter resistor and in this example was expected to be zero. When $\mathbf{R_S}$ is not zero, then its value must be subtracted from above calculated $\mathbf{R_F}$.

This calculation is suitable for low sampling frequencies and expects sampling capacity $\mathbf{C_S}$ is fully charged from filter capacity $\mathbf{C_F}$. Thus the filter resistor value is not limited in this case. For higher sampling frequencies, the filter resistance $\mathbf{R_F}$ goes too low (for $\mathbf{f_S}$ =40 kHz we have $\mathbf{R_F}$=120Ω only) and alternative approach must be taken to calculate filter components.

Alternative approach expects that sampling capacitor is not charged from filter capacity $\mathbf{C_F}$ but directly from source $\mathbf{V_A}$. In this calculation the filter resistance is limited to allow charging of sampling capacity $\mathbf{C_S}$ to required precision within sampling time:

$$\mathbf{t_s \geq \tau * (N+1) \ln 2}$$

where $\mathbf{t_s}$ is time, necessary to charge RC network ($\mathbf{\tau = RC}$) in sampling circuit of **N** bit ADC within ½ LSB accuracy. For 12 bit ADC we have:

$$\mathbf{t_s \geq RC * 9}$$

Thus maximal allowed input resistance **R** should be lower than:

$$\mathbf{R < t / 9C_S}$$

Sampling RC network is created by sampling capacity $\mathbf{C_S}$ and sum of input resistances **R**:

$$\mathbf{R = R_S + R_F + R_L + R_{SW} + R_{AD}}$$
$$\mathbf{R_F = R - (R_S + R_L + R_{SW} + R_{AD})}$$

Filter capacity $\mathbf{C_F}$ we evaluate the same way as in previous case, using Nyquist theorem:

$$\mathbf{C_F} = \frac{1}{\pi f_S R_F}$$

Example: ADC clock f_{CK} = 10MHz, standard sampling time $\mathbf{t_s}$ is 7 T_{CK} periods:

$$\mathbf{R} < 700ns / 9*7,32pF \qquad \mathbf{R< 10625\ \Omega}$$
$$\mathbf{R_F} = 10625 – (0+500+875+825) = \mathbf{8425\Omega}$$

Assuming $\mathbf{R_S = 0}$ you can use **8K2** resistor; otherwise you should subtract $\mathbf{R_S}$ from this value. AD conversion takes 20 ADC clocks (IMPCMP=1) so we have possible sampling frequency up to f_s = 0,5MHz:

$$\mathbf{C_F} = 1/ (3.14 * 0.5E6 *8.2E3) = \mathbf{78pF}$$ *you can use* **82p** *capacitor*

Note: Calculated $\mathbf{R_F}$ is a maximal limit value. You can use any smaller value (recommended) of course. Then $\mathbf{C_F}$ will have higher value than in this example.

Note: Maximal value of filter resistor $\mathbf{R_F}$ is also limited by leakage current $\mathbf{I_{IL}}$, flowing through ADC input. This current is caused mainly by diodes $\mathbf{D_1}$ and $\mathbf{D_2}$ in input protection. Maximal leakage current is given in datasheet and is defined for temperature 125°C, the value is 500nA for analog input plus leakage of channel selector switch 250nA gives 750nA in total. This current is flowing through $\mathbf{R_S}$, $\mathbf{R_F}$ and $\mathbf{R_L}$ causing leakage drop voltage $\mathbf{U_{LD}}$:

$$\mathbf{U_{LD} = I_{IL} * (R_S + R_F + R_L)}$$
$$\mathbf{R_F = (U_{LD} / I_{IL}) - R_S - R_L}$$

This voltage directly affects ADC accuracy thus for 1/2LSB error this should be:

$$\mathbf{U_{LD} < U_{REF} / 2^{(N+1)}}$$

For 12 bit ADC with 5V reference voltage, the $\mathbf{U_{LD} < 610\mu V}$. For defined maximal leakage current, assuming that R_S=0, the filter resistance R_F < 313Ω.
In practice the designed device does not operate at such high temperature as T_A=125°C, mostly temperature range up to 85°C is sufficient. In this case, using rule that *for temperature increase of 10°C the leakage current is doubled*, we have $\mathbf{I_{IL}}$ = 750nA/16 = 47nA which gives $\mathbf{R_F < 12k\Omega}$.

Do not forget:

- Decouple ADC supply and reference supply with **0,1µF** (ceramics) capacitors.
- If you are using switching power supply to power your design or using ADC supply as reference voltage or using the same supply to power digital and analog part of MPC5634L (3.3V), then use additional LC filters (**10µH** and **10µF** low ESR electrolytic cap) for ADC supply and reference supply decoupling. Add a **10nF** (ceramics) capacitor to reference supply decoupling.
- When routing MPC5634L modules supplies (V_{DD_xx} and V_{SS_xx}) use **star connection** (separate trace for each module supply) close to supplying regulator output to avoid sharing of voltage drops on supply rails.
- Reference voltage source should provide as much as **5mA** (for V_{REF} = 5V)
- You can extend sampling time by changing **INPSAMP** value in Conversion Timing Register (CTR0, CTR1), for details see below.
- You can extend bit evaluation time $T_{biteval}$ (time to evaluate each bit during SAR conversion) by changing **IMPCMP** value in Conversion Timing Register (CTR0, CTR1), for details see below:

The minimum sampling phase duration is: $T_{sample} = 7 \bullet T_{ck}$

For INPSAMP > 8, duration is: $T_{sample} = (INPSAMP - 1) \bullet T_{ck}$

The total evaluation phase duration is: $T_{eval} = 12 \bullet T_{biteval}$

The total conversion duration is : $T_{conv} = T_{sample} + T_{eval} + T_{ck}$

$T_{biteval} = 1 \bullet T_{ck}$ for IMPCMP = 1 when ADCclk > 3MHz (default)

$T_{biteval} = 2 \bullet T_{ck}$ for IMPCMP = 2 when ADCclk > 6MHz

$T_{biteval} = 3 \bullet T_{ck}$ for IMPCMP = 3 when ADCclk > 9MHz

$T_{biteval} = 4 \bullet T_{ck}$ for IMPCMP = 0 when ADCclk > 12MHz

- For higher sampling rates (f_{CK}>20MHz) you must extend sampling time (t_s>383ns) and evaluation time (t_{EVAL}>600ns) using **INPSAMP** and **IMPCMP** values otherwise ADC performance is affected. For maximal f_{CK} (60MHz) INPSAMP = 24 and IMPCMP = 3.
- If there is a possibility that $\mathbf{V_A}$ could exceed $\mathbf{V_{REF}}$ on any of analog inputs, current limiting resistor $\mathbf{R_L}$ for this input should be calculated with respect to this (maximal injected current during operation is only 3mA comparing to 10mA as maximal "survival" current that was used for R_L calculation in example). In this case input voltage will be clamped by $\mathbf{D_1}$ and then additional decoupling capacitor for $\mathbf{V_{REF}}$ is needed (20µF to 100µF electrolytic capacitor).
- If you will use operational amplifier to buffer signal source $\mathbf{V_A}$ then components $\mathbf{R_F}$, $\mathbf{C_F}$ and $\mathbf{R_L}$ are not needed. Best solution is to use Rail-to-Rail amplifier (for example AD8651, AD8652). In this case, amplifier is supplied from V_{REF}. Anyhow, you should limit signal source bandwidth according to Nyquist rule, for example by low-pass filter created using this buffering operational amplifier.