

Peripherals	Hex	Binary	Address	Description
LBSSW0	0x00000000	0000000000000000	0x403A004C	STCU2 Online LBIST Status
LBRMSW0	0x00000000	0000000000000000	0x403A006C	STCU2 Online LBIST Reset Management
MB_CTRL11	0x00000000	0000000000000000	0x403A2240	STCU2 MBIST Control
CFG	0x1001E000	0001000000000000	0x403A000C	STCU2 Configuration
CLK_CFG (bits 0-2)	0x0	000		sys_clk/1
WRP (bit 0)	0x0F	00001111		Write Protection 0: Specific STCU2 registers can be written through I2S bus interface 1: STCU2 registers cannot be written through I2S bus interface
LB_DELAY (bits 13-20)	0x00	00000000		Delay LBIST run LB_DELAY defines the delay between the LBIST starts when more than a single LBIST is selected
PTR (bits 21-30)	0x00	0010000000		First LBIST or MBIST pointer PTR defines the logical pointer to the first LBIST or MBIST to be scheduled when multiple LBISTs or MBISTs are selected
LB_MISRHSW0	0x00000000	0000000000000000	0x403A022C	STCU2 Online LBIST MISR Read High
LB_MISRRLSW0	0x00000000	0000000000000000	0x403A0228	STCU2 Online LBIST MISR Read Low
MB_CTRL7	0x00000000	0000000000000000	0x403A2230	STCU2 MBIST Control
LBUFFM0	0x00000000	0000000000000000	0x403A007C	STCU2 Online LBIST Unrecoverable FM
MB_CTRL5	0x00000000	0000000000000000	0x403A2228	STCU2 MBIST Control
MB_CTRL9	0x00000000	0000000000000000	0x403A2238	STCU2 MBIST Control
LBESW0	0x00000000	0000000000000000	0x403A005C	STCU2 Online LBIST End Flag
MB_CTRL3	0x00000000	0000000000000000	0x403A2220	STCU2 MBIST Control
MB_CTRL1	0x00000000	0000000000000000	0x403A2218	STCU2 MBIST Control
LB_MISRLSW0	0xFFFFFFFF	1111111111111111	0x403A0220	STCU2 Online LBIST MISR Expected Low
WDG	0x000186A0	0000000000000000	0x403A0014	STCU2 Watchdog Granularity
MB_CTRL10	0x00000000	0000000000000000	0x403A223C	STCU2 MBIST Control
LB_CTRL0	0x00000000	0000000000000000	0x403A0200	STCU2 LBIST Control
BSTART	0x00000000	0000000000000000	0x403A2210	STCU2 BIST Start
MBSW0	0x00000000	0000000000000000	0x403A010C	STCU2 Online MBIST Status
MBSW0 (bit 0)	0x1	1		<input type="checkbox"/> No fault detected during the MBIST execution
MBSW1 (bit 1)	0x1	1		<input type="checkbox"/> No fault detected during the MBIST execution
MBSW2 (bit 2)	0x1	1		<input type="checkbox"/> No fault detected during the MBIST execution
MBSW3 (bit 3)	0x1	1		<input type="checkbox"/> No fault detected during the MBIST execution
MBSW4 (bit 4)	0x1	1		<input type="checkbox"/> No fault detected during the MBIST execution
MBSW5 (bit 5)	0x0	0		<input type="checkbox"/> Failed MBIST execution
MBSW6 (bit 6)	0x0	0		<input type="checkbox"/> Failed MBIST execution
MBSW7 (bit 7)	0x0	0		<input type="checkbox"/> Failed MBIST execution
MBSW8 (bit 8)	0x0	0		<input type="checkbox"/> Failed MBIST execution
MBSW9 (bit 9)	0x0	0		<input type="checkbox"/> Failed MBIST execution
MBSW10 (bit 10)	0x0	0		<input type="checkbox"/> Failed MBIST execution
MBSW11 (bit 11)	0x0	0		<input type="checkbox"/> Failed MBIST execution
MBUFFM0	0x00000000	0000000000000000	0x403A018C	STCU2 MBIST Unrecoverable FM
LB_MISRHSW0	0xFFFFFFFF	1111111111111111	0x403A0224	STCU2 Online LBIST MISR Expected High
LB_PCSD0	0x00000000	0000000000000000	0x403A0204	STCU2 LBIST PC Stop
MB_CTRL8	0x00000000	0000000000000000	0x403A2234	STCU2 MBIST Control

Peripherals	Hex	Binary	Address	Description
SAC	(write only)	(write only)	0x403A0008	STCU2 SK Code
MBSW0	0x00000000	0000000000000000	0x403A014C	STCU2 Online MBIST End Flag
MBSW0 (bit 0)	0x1	1		<input type="checkbox"/> MBIST execution finished
MBSW1 (bit 1)	0x1	1		<input type="checkbox"/> MBIST execution finished
MBSW2 (bit 2)	0x1	1		<input type="checkbox"/> MBIST execution finished
MBSW3 (bit 3)	0x1	1		<input type="checkbox"/> MBIST execution finished
MBSW4 (bit 4)	0x1	1		<input type="checkbox"/> MBIST execution finished
MBSW5 (bit 5)	0x0	0		<input type="checkbox"/> MBIST execution still ongoing
MBSW6 (bit 6)	0x0	0		<input type="checkbox"/> MBIST execution still ongoing
MBSW7 (bit 7)	0x0	0		<input type="checkbox"/> MBIST execution still ongoing
MBSW8 (bit 8)	0x0	0		<input type="checkbox"/> MBIST execution still ongoing
MBSW9 (bit 9)	0x0	0		<input type="checkbox"/> MBIST execution still ongoing
MBSW10 (bit 10)	0x0	0		<input type="checkbox"/> MBIST execution still ongoing
MBSW11 (bit 11)	0x0	0		<input type="checkbox"/> MBIST execution still ongoing
MB_CTRL6	0x00000000	0000000000000000	0x403A222C	STCU2 MBIST Control
ALGOSEL	0x00000000	0000000000000000	0x403A2200	STCU2 Algorithm Select
ERR_STAT	0x00000000	0000000000000000	0x403A0024	STCU2 Error
ERR_FM	0x00000000	0000000000000000	0x403A0028	STCU2 Error FM
MB_CTRL0	0x00000000	0000000000000000	0x403A2214	STCU2 MBIST Control
MB_CTRL4	0x77F00000	0111111111111111	0x403A2224	STCU2 MBIST Control
RUNSW	0x00000000	0000000000000000	0x403A0004	STCU2 Run Software
RUNSW (bit 0)	0x0	0		<input type="checkbox"/> Idle
LSWPLEN (bit 8)	0x0	0		<input type="checkbox"/> Online LBIST is executed without using the on-chip PLL
MBSWPLEN (bit 9)	0x0	0		<input type="checkbox"/> Online MBIST is executed without using the on-chip PLL
MB_CTRL2	0x00000000	0000000000000000	0x403A221C	STCU2 MBIST Control
BSEL (bit 20)	0x1	1		<input type="checkbox"/> Selected BIST is selected for execution.
PTR (bits 21-30)	0x03	0010000011		PTR
CSM (bit 31)	0x1	1		<input type="checkbox"/> Concurrent mode
STGGR	0x00000000	0000000000000000	0x403A220C	STCU2 MBIST Stagger
LPDEBUG	0x00000000	0000000000000000	0x4028C02C	Low Power Debug Control Register
DES	0x00000001	0000000000000000	0x4028C000	Destructive Event Status Register
FRET	0x0000000F	0000000000000000	0x4028C018	Functional Reset Escalation Threshold Register
FRET (bits 0-3)	0xF	1111		Functional Reset Escalation Threshold
FRED	0x00000000	0000000000000000	0x4028C00C	Functional Event Reset Disable Register
FREC	0x00000001	0000000000000000	0x4028C014	Functional Reset Escalation Counter Register
FREC (bits 0-3)	0x1	0001		Functional Reset Escalation Counter
ERCTRL	0x00000000	0000000000000000	0x4028C020	External Reset Control Register
DRET	0x0000000F	0000000000000000	0x4028C01C	Destructive Reset Escalation Threshold Register
FBRE	0x00000000	0000000000000000	0x4028C010	Functional Bidirectional Reset Enable Register
FRENTIC	0x00000001	0000000000000000	0x4028C028	Functional Reset Entry Timeout Control Register
FRENTIC (bit 0)	0x1	1		<input type="checkbox"/> Functional reset entry timer is enabled
FRET_TIMEOUT (bits 1-31)	0x00000000	0000000000000000		Functional Reset Entry Timer Value

FES	0x20000000	0010000000000000	0x4028C008	Functional /External Reset Status Register
F_EXR (bit 0)	0x0	0		<input type="checkbox"/> No external reset event has occurred since either the last clear or the last power-on reset assertion.
FCCU_RST (bit 3)	0x0	0		<input type="checkbox"/> Functional reset event FCCU_RST has not occurred since either the last clear or the last power-on reset as...
ST_DONE (bit 4)	0x0	0		<input type="checkbox"/> Functional reset event ST_DONE has not occurred since either the last clear or the last power-on reset as...
SWTO_RST (bit 6)	0x0	0		<input type="checkbox"/> Functional reset event SWTO_RST has not occurred since either the last clear or the last power-on reset as...
JTAG_RST (bit 9)	0x0	0		<input type="checkbox"/> Functional reset event JTAG_RST has not occurred since either the last clear or the last power-on reset as...
HSE_SWT_RST (bit 16)	0x0	0		<input type="checkbox"/> Functional reset event HSE_SWT_RST has not occurred since either the last clear or the last power-on res...
HSE_BOOT_RST (bit 20)	0x0	0		<input type="checkbox"/> Functional reset event HSE_BOOT_RST has not occurred since either the last clear or the last power-on re...
SW_FUNC (bit 29)	0x1	1		<input type="checkbox"/> Functional reset event SW_FUNC has occurred.
DEBUG_FUNC (bit 30)	0x0	0		<input type="checkbox"/> Functional reset event DEBUG_FUNC has not occurred since either the last clear or the last power-on res...
RDS	0x00000000	0000000000000000	0x4028C024	Reset During Standby Status Register
DES_RES (bit 0)	0x0	0		<input type="checkbox"/> No destructive reset event occurred during standby mode.
FES_RES (bit 1)	0x0	0		<input type="checkbox"/> No functional reset event occurred during standby mode.

### 31.3.5 Functional reset sources

Table 174. Functional reset sources

Source module	Field in MC_RGM.FES	RESET_b assertion	Demotable to IRQ <sup>1</sup>	Escalation <sup>2</sup>	Description
FCCU soft reaction <sup>3</sup>	FCCU_RST	Always	Yes <sup>4</sup>	Yes	FCCU reset reaction
STCU2	ST_DONE	Configurable	No	No	Self-test done
SWT_0	SWT0_RST	Always	Yes <sup>5</sup>	Yes	SWT reset request
SWT_1 <sup>6</sup>	SWT1_RST	Always	Yes <sup>7</sup>	Yes	SWT reset request
SWT_2 <sup>8</sup>	SWT2_RST	Always	Yes <sup>9</sup>	Yes	SWT reset request
SWT_3 <sup>10</sup>	SWT3_RST	Always	Yes <sup>11</sup>	Yes	SWT reset request
PLL_AUX <sup>12</sup>	PLL_AUX_RST <sup>13</sup>	Always	Yes <sup>14</sup>	Yes	PLL reset request
JTAGC	JTAG_RST	Always	Yes <sup>15</sup>	No	JTAG reset
HSE_B	HSE_SWT_RST	Always	No	Yes	HSE_B SWT timeout
HSE_B	HSE_BOOT_RST	Always	No	Yes	HSE_B boot reset
MC_ME	SW_FUNC	Always	No	Yes	Software functional reset
MDM_AP	DEBUG_FUNC	Always	Yes <sup>16</sup>	Yes	Debug functional reset