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Revisions			
Rev	Description	Date	Approved
C	Formal Release(added C151)	26-Jun-18	Didier Pagnoux

# KITFS85FRDMEVM

		<b>Analog Sensor Product Group</b>	
		6501 William Cannon Drive West Austin, TX 78725-8550	
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ICAP: Classification: CP: IJO: X PUBL:			
Designer: Didier Pagnoux	Drawing Title: <b>KITFS85FRDMEVM</b>		
Drawn by: Didier Pagnoux	Page Title: <b>TITLE, TOC &amp; REV</b>		
Approved: Didier Pagnoux	Size C	Document Number SCH-29838 PDF: SPF-29838	Rev C
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**Board Configuration - Main Target**  
**(Other configuration possible thanks to OTP)**

Vpre : 450K / 3A / 4.1V  
 BUCK1 : 2.5A / 1.25V  
 BUCK2 : 2.5A / 3.3V (Standalone or Multiphase)  
 BUCK3 : 2.5A / 2.3V  
 VBOOST : 5.74V In = VPRE  
 LDO1 : 3.3V / 400mA / In = Vpre  
 LDO2 : 5V / 150mA  
 VDDIO : Assigned on VDDI2C (set to 3.3V) by default)

**LPRE Coil Proposal (Primary)**

VPRE	LPRE
455KHz	SFM7054VT-4R7M-D Isat 10.9 / Itemp@40 6.4A ( 7.5mm x 7mm)
2.2MHz	SFM6545VT-1R5M-D 6A / 2.2MHz Isat 13.4A / Itemp@40 9.2A ( 7mm x 6.5mm) 8x2mm

**LPRE Coil Proposal (Alternate)**

VPRE	LPRE
455KHz	KAL6060-6S2ME SFM7054VT-6R8M-D 6A / 455KHz Isat 9.9A / Itemp@40 5.3A ( 7.5mm x 7mm)
2.2MHz	SFM7054VT-1R5M-D Isat 13.9A / Itemp@40 10.9A ( 7.5mm x 7mm)

**Vpre Frequency Configuration :**

- 450KHz :
  - \* Vpre Coil set to 4.7nH or 6.8nH
  - \* Comp Network : C5=150pF / C4=8.8nF / R3=3.57K
- 2.2MHz :
  - \* Vpre coil set to 1.5nH or 4.7nH
  - \* Comp. Network : C5=22pF / C4=1.5nF / R3=16.9K

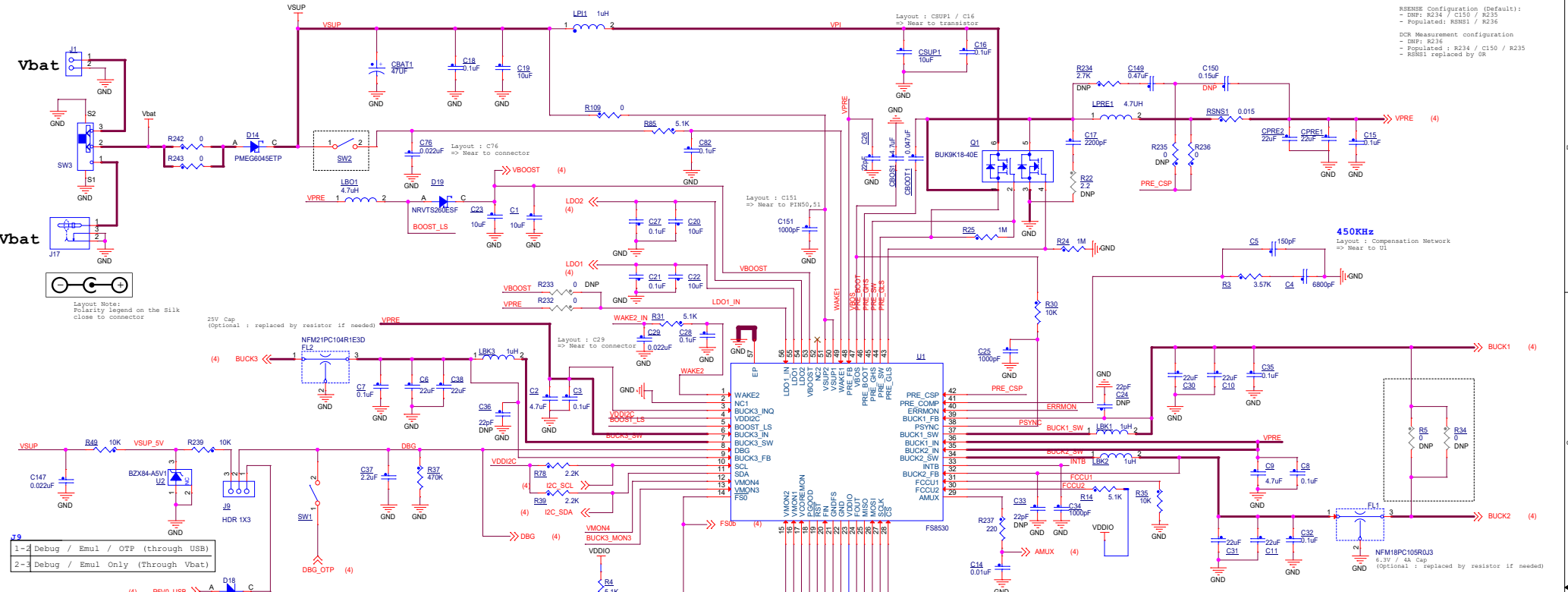
Default coil on this board is 4.7nH to allow evaluation at both frequencies.  
 Recommended values are 1.5nH to minimize size at 2.2MHz, and 6.8nH to minimize ripple at 450KHz

**3-Terminal Capacitors**

Mounted for evaluation purpose only.  
 Optional feature. Can be replace by a 0603 0 ohm resistors.



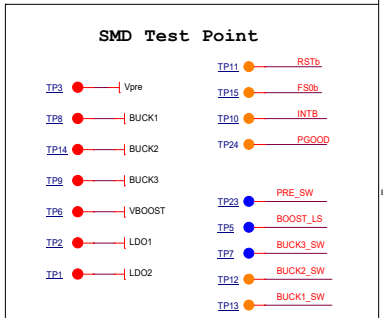
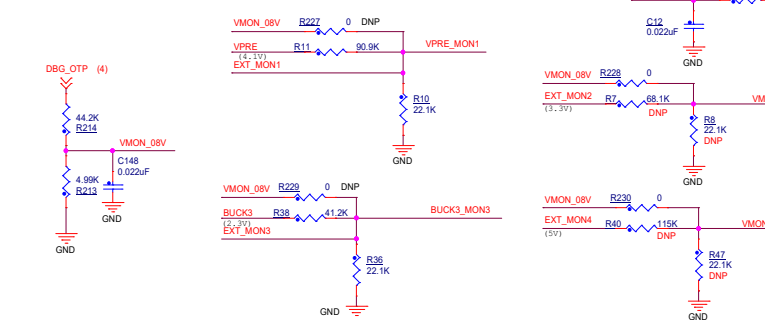
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Drawing Title: <b>KITFS85FRDMEVM</b>	
Page Title: <b>NOTES</b>	
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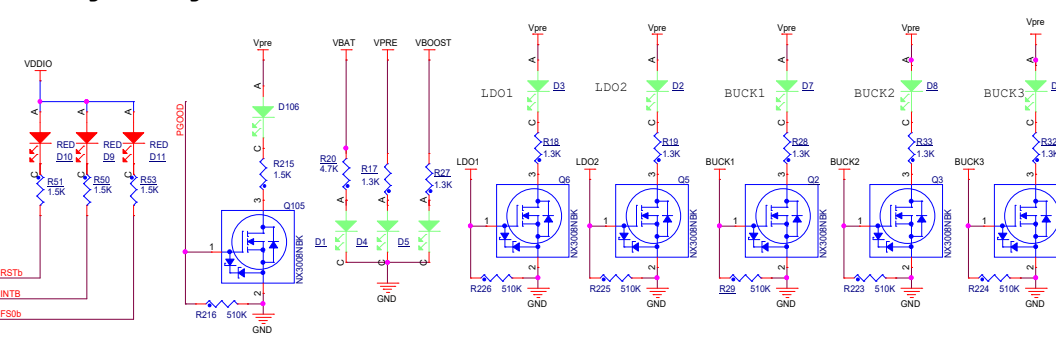
RSense Configuration (Default):  
 - DNP: R234 / C150 / R235  
 - Populated: R234 / R235  
 DCR Measurement configuration  
 - DNP: R236  
 - Populated: R234 / C150 / R235  
 - R236 replaced by DR

Layout Note:  
 Polarity legend on the Silk close to connector

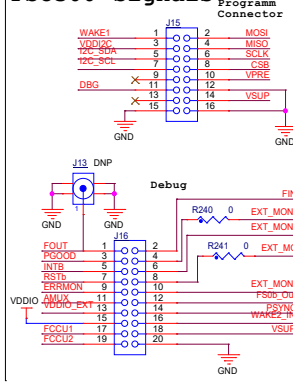
T9	1-2 Debug / Emul / OTP (through USB)
	2-3 Debug / Emul Only (Through Vbat)



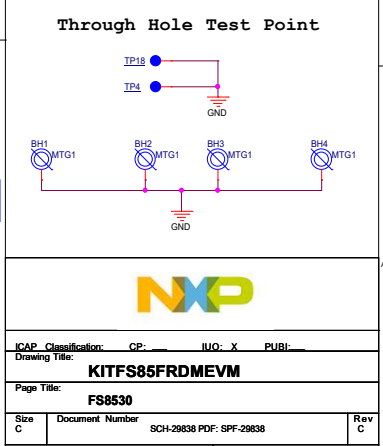
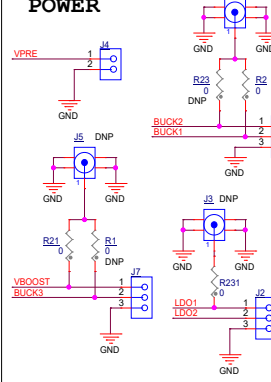
### LED Signalling



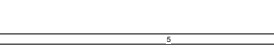
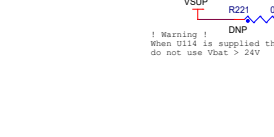
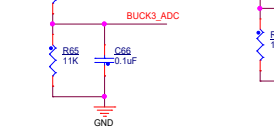
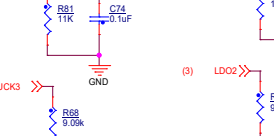
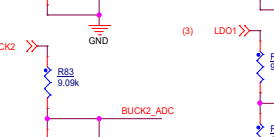
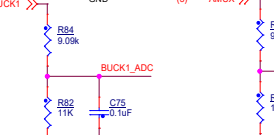
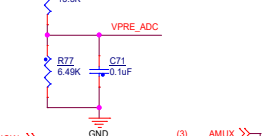
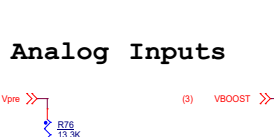
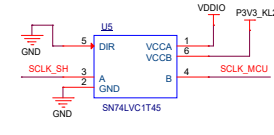
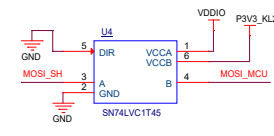
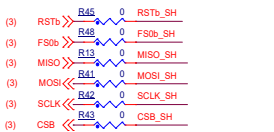
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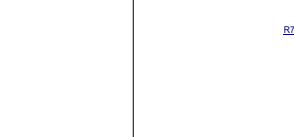
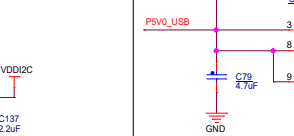
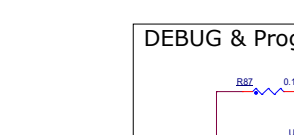
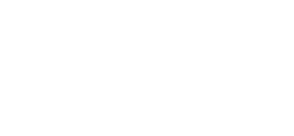
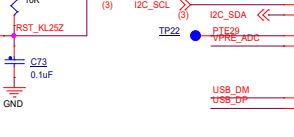
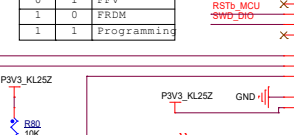
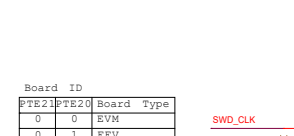
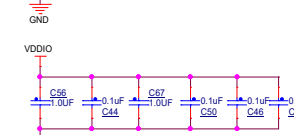
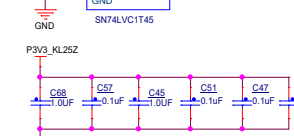
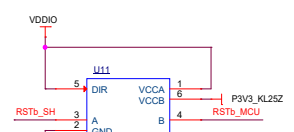
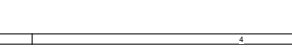
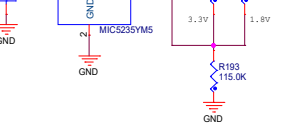
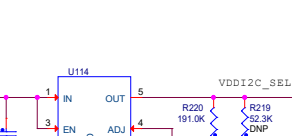
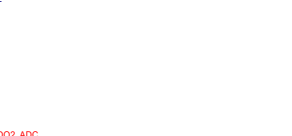
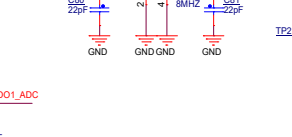
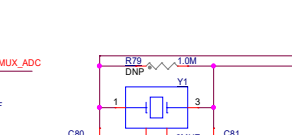
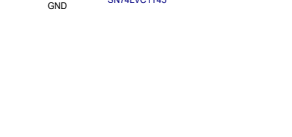
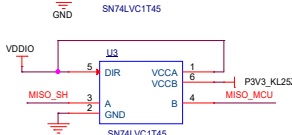
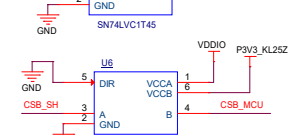
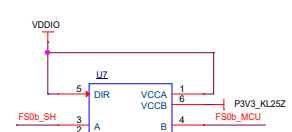
### POWER



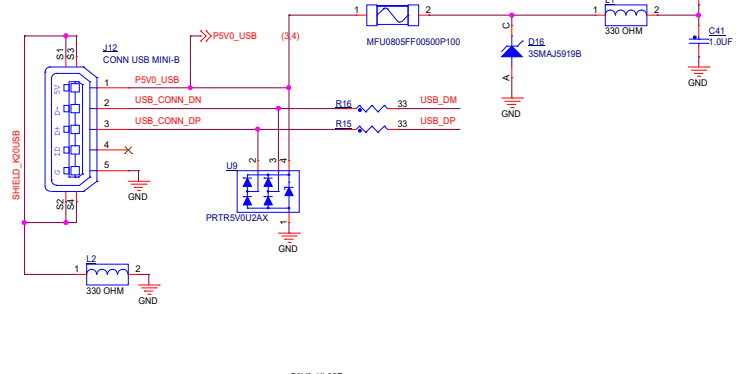
SPI / Reset / Fai Safe 0



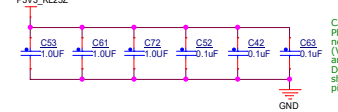
Level Shifter (1.65V / 5.5V)



KL25Z USB CONNECTOR

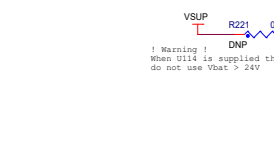
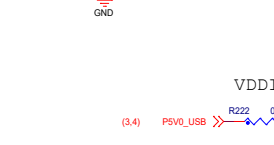
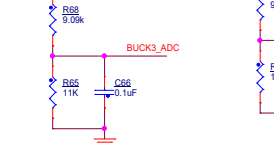
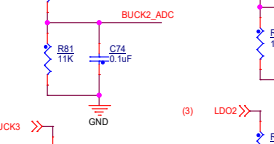
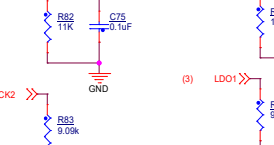
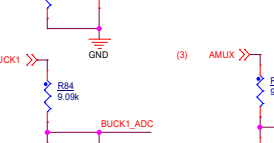
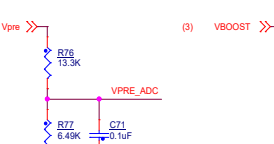


KL25Z Decoupling Caps

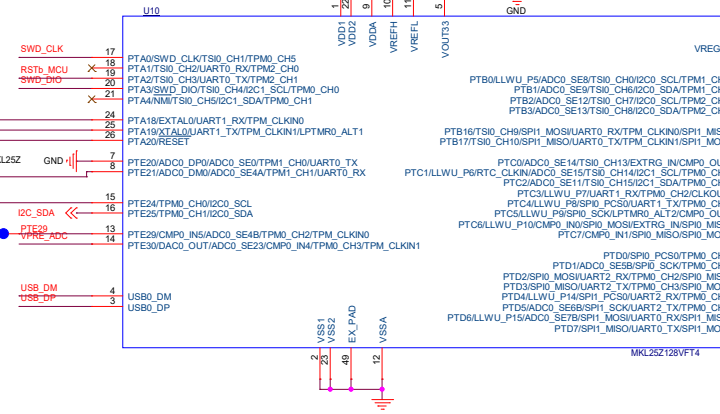


CAD NOTE: Please place these capacitors near their respective CPU pin (VREFH to VREFL and VDDA to VSSA). Decoupling capacitors shall be used for these pins: VDD1, VDD2, VDDA.

Analog Inputs

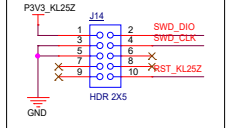


Board ID	Board Type
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0	1
1	0
1	1

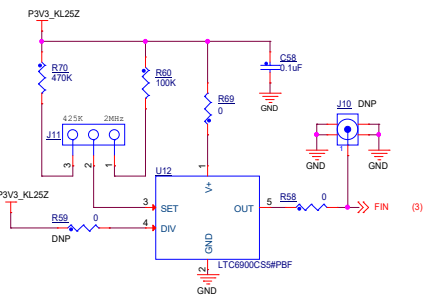
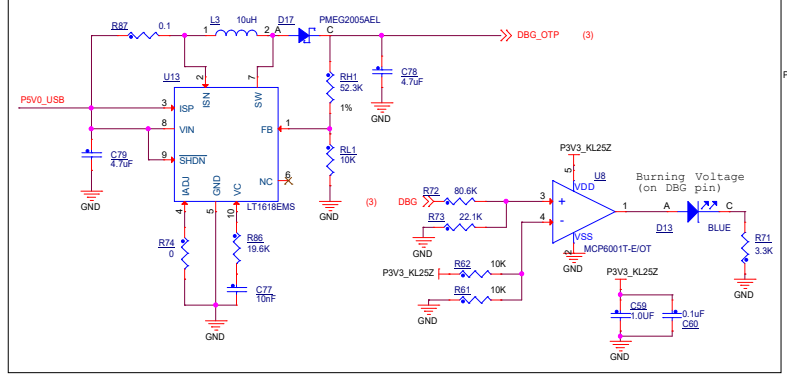


CAD NOTE: Please place P3V3\_KL25Z capacitor close to the VOLT13 pin.

SWD CONNECTOR



DEBUG & Programming Mode Voltage



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