Agenda

- Hardware Considerations
- CPU Differences
- System (Peripherals, Clocks, Power Modes)
- Safety Features
- Tools and Enablement

Objectives: Migration to S32K is Easy

- Overview on the hardware and software differences of MPC56xx and S32K
- Learn what is necessary to migrate from MPC56xx to S32K
- Learn the benefits of the ARM Cortex platform

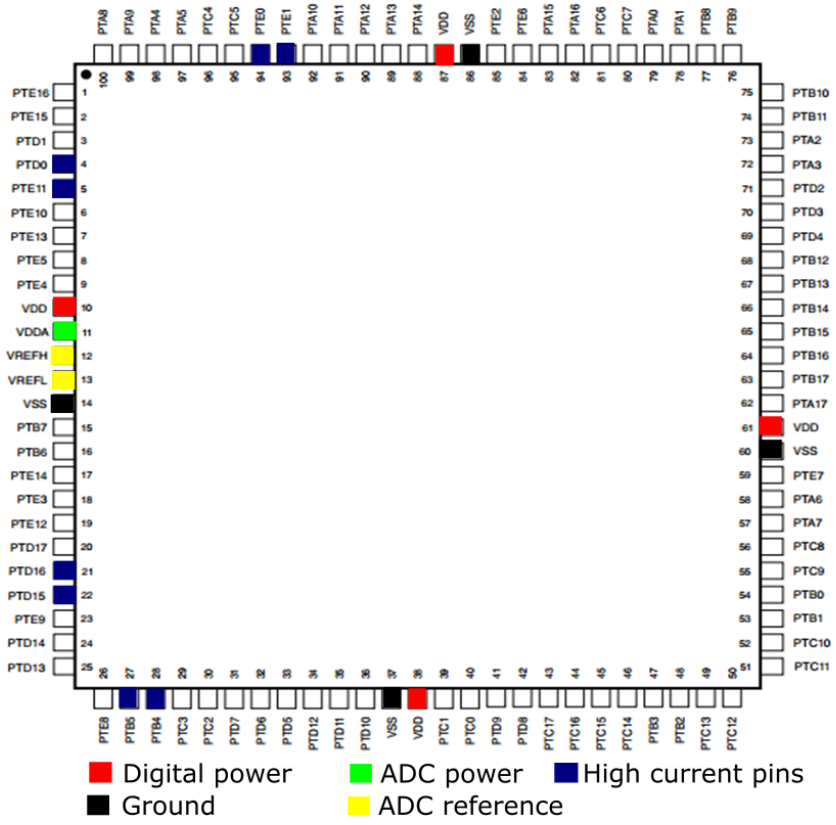
Hardware Considerations

- Package options
- Power supplies
- Decoupling
- Reset sequence

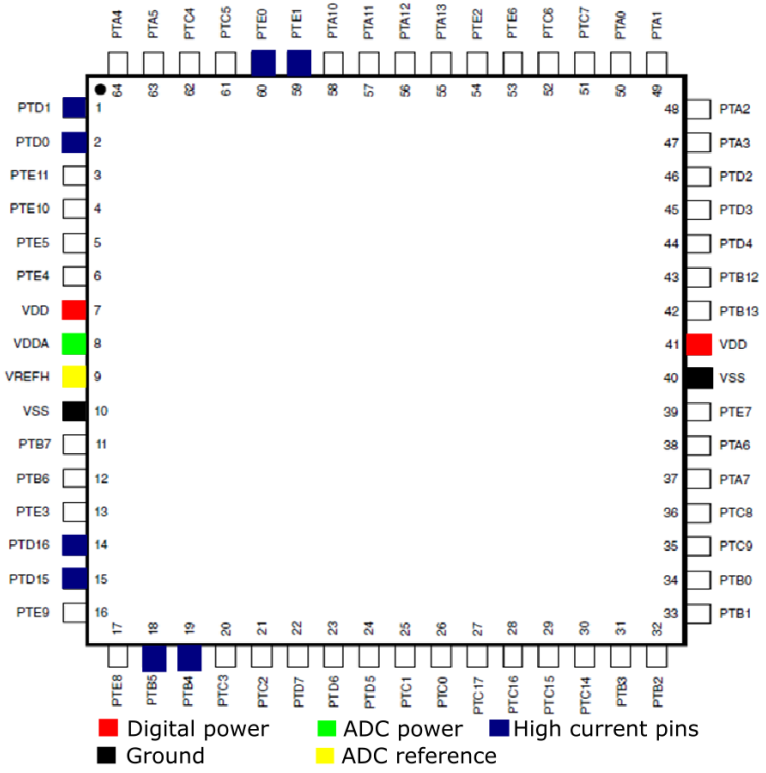
Package Options

Device	Package	Digital Power	ADC Power	ADC Reference	GPIOs	20 mA capable Pins
S32K	64 LQFP	4	1	2	58	8
S32K	100 LQFP	8	1	2	89	8
MPC560xB	100 LQFP	9	1	3	77	None
MPC560xP	100 LQFP	10	2	2	64	None

ARM Cortex Platform 100LQFP



ARM Cortex Platform 64LQFP

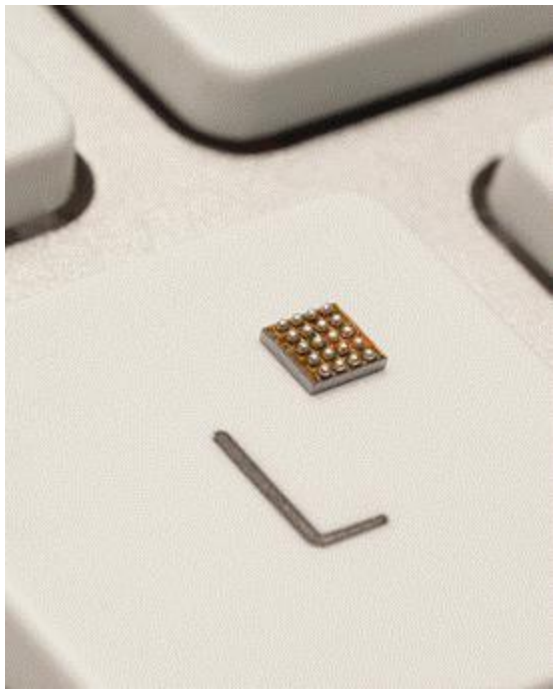


Power Supply Comparison
Example LQFP100 MPC56xxB vs. S32K

MPC5604B Description	MPC5604B	#	S32K Description	S32K	#
Digital ground	VSS_HV	5	Ground	VSS	4
Digital supply voltage	VDD_HV	4	Voltage for core, I/O, clock and memory of the device	VDD	4
1.2V decoupling pins GND	VSS_LV	3	NA	NA	NA
1.2V decoupling pins	VDD_LV	3	NA	NA	NA
Internal regulator supply voltage	VDD_BV	1	NA	NA	NA
Reference ground and analog ground for the ADC	VSS_HV_ADC	1	Voltage Reference Select Low	VREFL	1
Reference voltage and analog supply for ADC	VDD_HV_ADC	1	Voltage Reference Select High	VREFH	1
			Analog Power Supply	VDDA	1
	SUM	18		SUM	11

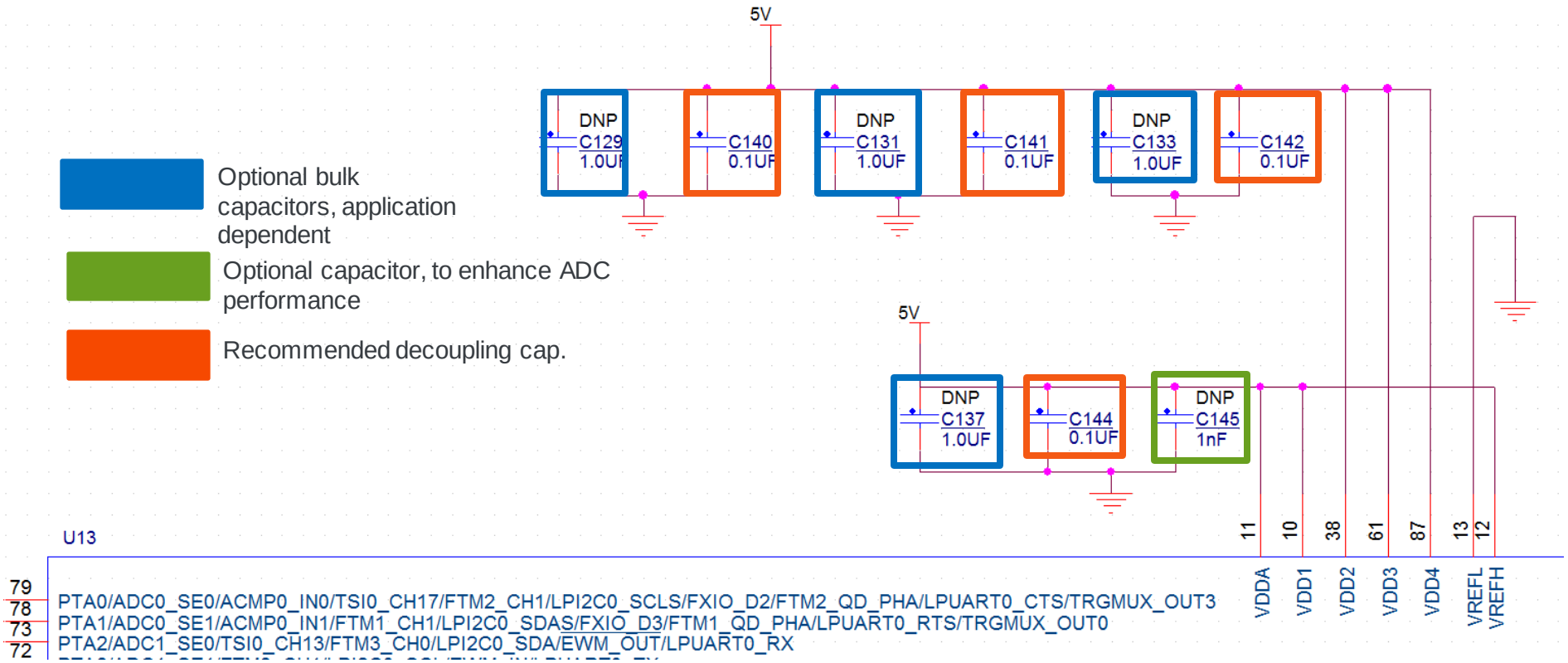
Do not leave any of the supply pins unconnected

Power: S32K Platform



- S32K voltage range: 2.7 V to 5.5 V
- Power to Vdd pins can be supplied with a Freescale Power System Basis Chip (SBC) device or a discrete voltage regulator
- Recommended SBC: 33903CS5 or 33903CS3
- Decoupling capacitor and bulk capacitor placed between Vdd/Vdda/Vss and Vrefh/Vrefl
- Do not leave any of the supply pins unconnected

Powering S32K144

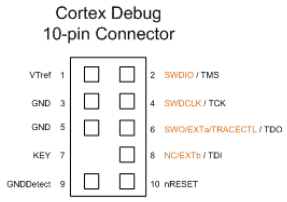


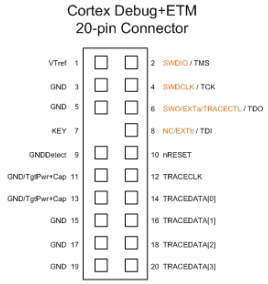
Reset: S32K Platform

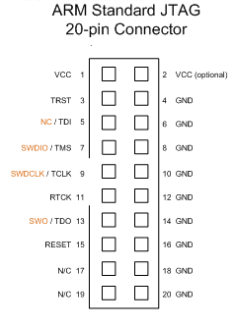
- PTA5 is default functionality after POR is RESET.
- PTA5 can be changed to other functions.
- This pin is open drain and has an internal pullup device. Asserting RESET wakes the device from any mode.
- Internal Resets drive low Reset pin.
- Pull up resistor enabled by default in PTA5 after Reset.
- The RESET pin filter supports filtering from both the 128 kHz LPO clock and the bus clock.
- A minimum of 100 ns pulse width is necessary in the RESET pin to be recognized by the MCU.

Debugger: S32K Platform

- Connect desired debug header to S32K SWD and JTAG interface pins.

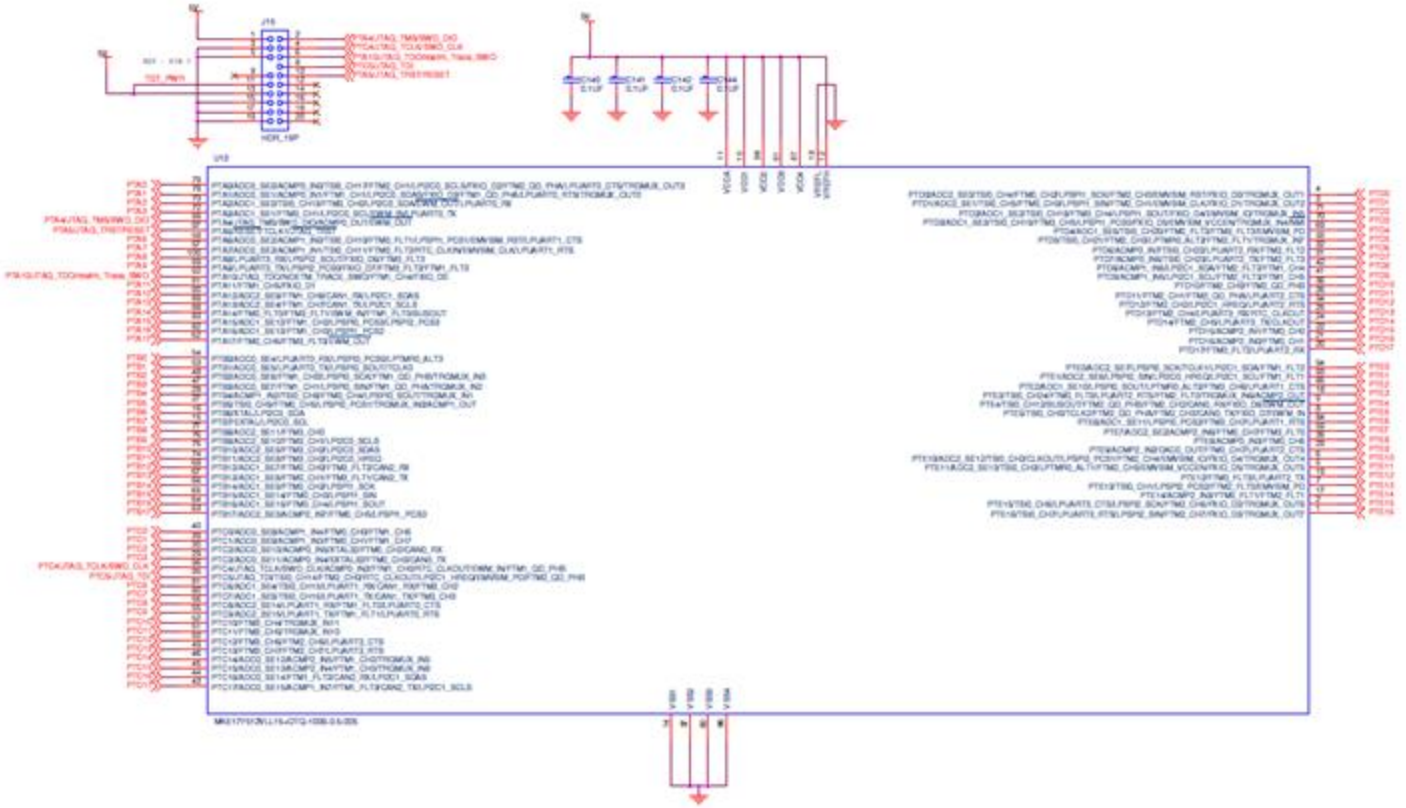






Debugger signal SWD/JTAG	Description	Connects to
SWDIO/TMS	SWD: Data I/O pin. JTAG: Test Mode State pin.	PTA4
SWDCLK/TCK	SWD: Clock pin. JTAG: Test Clock pin.	PTC4
SWO/TDO	SWD: Optional trace output pin. JTAG: Test Data Out pin.	PTA10
NC/TDI	SWD: N/A JTAG: Test Data In pin	PTC5
Reset	Reset pin.	PTA5
TRST	Test ReSeT	PTA5
TRACECLK	ETM trace clock pin.	NA
TRACEDATA[0-3]	4-bit, trace data output pins	NA
VCC(Vtref)	Power supply for JTAG	Positive supply voltage
GND	Ground	Ground

Minimum external circuitry

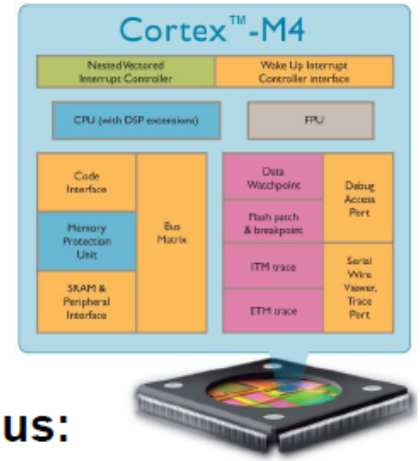


CPU Differences

Comparison between the ARM Cortex M4 and the PowerPC e200z0 cores

ARM Cortex-M4 Processor

- **Most energy efficient CPU for 32-bit digital signal control**
  - Builds on the success of ARM Cortex-M3, fully upwards compatible, delivering 1.25 DMIPS/Mhz
  - Combines MCU and DSP functionality in a single CPU
  - Brings high performance signal processing to the standard MCU programmer
- **Powerful signal processing features**
  - Same powerful 16/32-bit Thumb-2 ISA as Cortex-M3
  - Single-cycle MAC for efficient integer maths
  - 8/16-bit SIMD, saturating maths
  - Optional single-precision FPU
  - Free optimised DSP Library available
- **Same design options as Cortex-M3, plus:**
  - FP unit can be powered down for energy saving



CPU Differences

Feature	S32K	MPC560xB
CPU	ARM Cortex M4	PowerPC e200z0h
Max CPU frequency	112 MHz	64 MHz
DSP	Yes	No
FPU	Yes	No
MPU	Yes	Yes
I/D cache	4 KB	No
Interrupt controller	NVIC, 16 prio.	16 prio.
Wake up controller	Yes	Yes
DMA	16 channels	16 channels
Watchdog	Hardware and software	Software
Debug	SWD, JTAG, Trace	JTAG

System Differences

Comparison between the S32K and the MPC56xx SoC features

- **Peripherals**
- **Clocks**
- **Power modes**

S32K Block diagram

Preliminary and subject to change

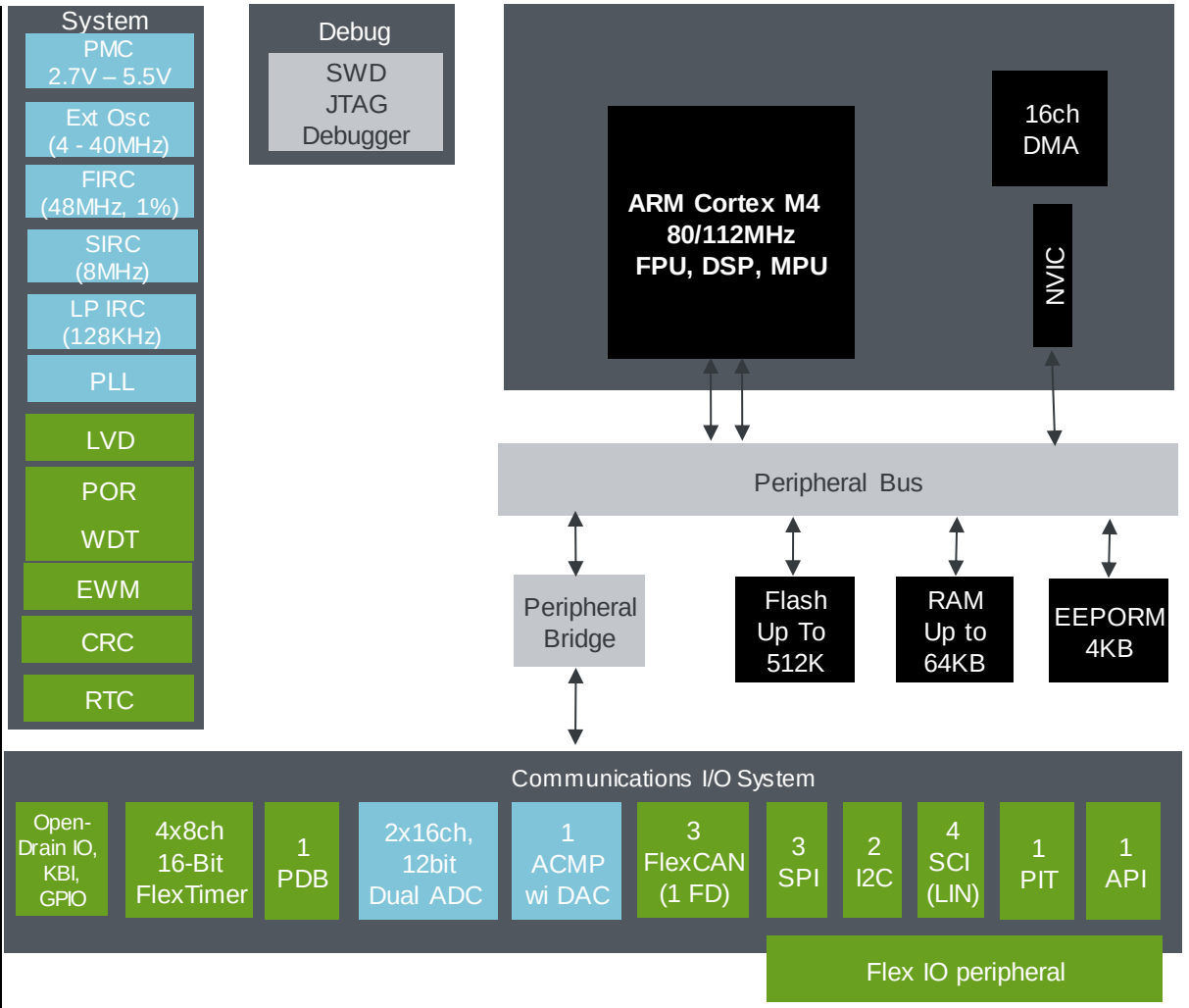
Digital Components | 5V Analogue Components | MCUCore and Memories | Archi/support

High performance
- ARM Cortex M4 up to 112MHz w FPU
- eDMA from Power Architecture family

Low power
- Low leakage technology
- Multiple VLP modes and IRC combos
- Wake-up on analog thresholds

Software Friendly Architecture
- High RAM to Flash ratio
- Independent CPU and peripheral clocking
- 48MHz 1% IRC – no PLL init required in LP
- Registers maintained in all modes
- Programmable triggers for ADC → no SW delay counters or extra interrupts

Functional safety
- ISO26262 support for ASIL B or higher
- MPU
- ECC on Flash/Dataflash and RAM
- Independent internal OSC for Watchdog
- Diversity between ADC and ACMP
- Diversity between SPI/SCI and FlexIO
- Core self test libraries
- Scalable LVD protection
- CRC

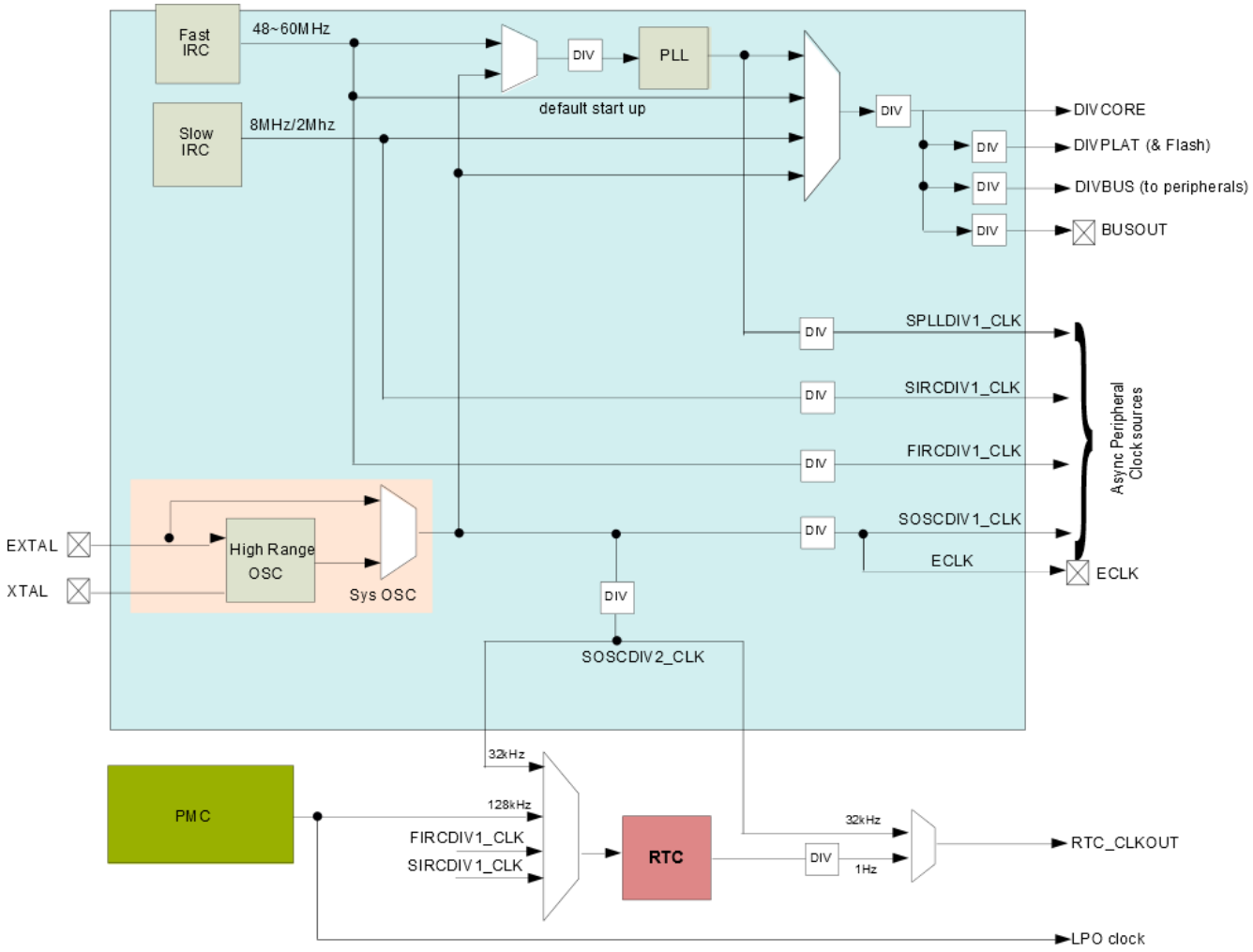


Operating Characteristics
- Voltage range: 2.7 to 5.5 V
- Temperature (ambient): -40 to 125°C

Packages and IO
64/100pin compatible within product Family
GPIO quantity optimization

ARM

S32K High Level Clocking Architecture



S32K: Clocking

Clock Sources

- FIRC: 48 MHz – 60 MHz
  - <1% accuracy after trimming, across PVT
  - 300 uA consumption
- SIRC: 8 MHz
  - <10% accuracy
  - 20 uA consumption
- LPO: 128 KHz
  - -<10% accuracy
  - 2 uA consumption
- XOSC
  - High range: 4 MHz – 40 MHz
- PLL: Up to 112 MHz
  - Choice of FIRC or the XOSC as input sources

Peripheral Clock Options – Example of Flexibility

Peripherals	Core Interface Clock	Optional peripheral ('protocol') Clock	Other Clock sources	Comments / max_freq
Communications				
LPUART0 – LPUART2	DIVBUS	SIRCDIVx_clk, FIRCDIVx_clk, SPLLDIVx_clk, DIVBUS	XOSC	80Mhz
LPSPI0 – LPSPI2	DIVBUS	SIRCDIVx_clk, FIRCDIVx_clk, SPLLDIVx_clk, DIVBUS	XOSC	80MHz
LPI2C0 – LPI2C1	DIVBUS	SIRCDIVx_clk, FIRCDIVx_clk, SPLLDIVx_clk, DIVBUS	XOSC	40MHz
FlexCAN0 – FlexCAN2	DIVBUS	SIRCDIVx_clk, FIRCDIVx_clk, SPLLDIVx_clk, DIVBUS	XOSC	40MHz from XOSC DIVBUS must be >1.5x the protocol clock

System (Peripherals, Clocks, Power Modes)

Clocks	ARM Cortex	MPC560xB
External crystal	4 to 40 MHz	4 to 16 MHz
External wave input	DC to 50 MHz	DC to 16 MHz
Internal clocks	48 MHz FIRC 8MHz SIRC 3% max deviation 128 kHz LPO	16 MHz FIRC 128 kHz LPO

Preliminary and subject to change

ADC

- Two ADC modules (ADC0, ADC1)
- 16 channels per ADC module
- 32 ADC channels total
- Linear successive approximation algorithm with up to 12-bit resolution
- Automatic compare functionality
- Software and Hardware trigger
- ADC Hardware average feature
- DMA support
- Programmable delay block (PDB)

FlexTimer Module

- FTM has a 16-bit counter
- The counting can be up or up-down
- Each channel can be configured for input capture, output compare, or PWM generation
- New combined mode to generate a PWM signal (with independent control of both edges of PWM signal)
- Complementary outputs, include the deadtime insertion
- Up to 4 fault inputs for global fault control
- Dual edge capture for pulse and period width measurement
- Quadrature decoder with input filters, relative position counting and interrupt on position count or capture of position count on external event

FlexTimer vs eMIOS

Feature	MPC560xB	ARM® Cortex® Platform
Unit	2x eMIOS 32 ch. each	4x FlexTimer 8 ch. each
Channels	Up to 64	Up to 32
Channel width	16-bit	16-bit
Count direction	Up	Up / Down
IC / OC	Yes	Yes
PWM	Yes	Yes
PWM center aligned mode	No	Yes
PWM Trigger Option to ADC	Yes	Yes
Input Period and Pulse width measurement	Yes	Yes
Synchronized loading of write buffered registers	Per channel	Whole FTM module
Fault control inputs	No	Yes
Complementary outputs with deadtime insertion	No	Yes
Quadrature decoder with input filters	No	Yes
Dead Time insertion	No	Yes

FlexIO

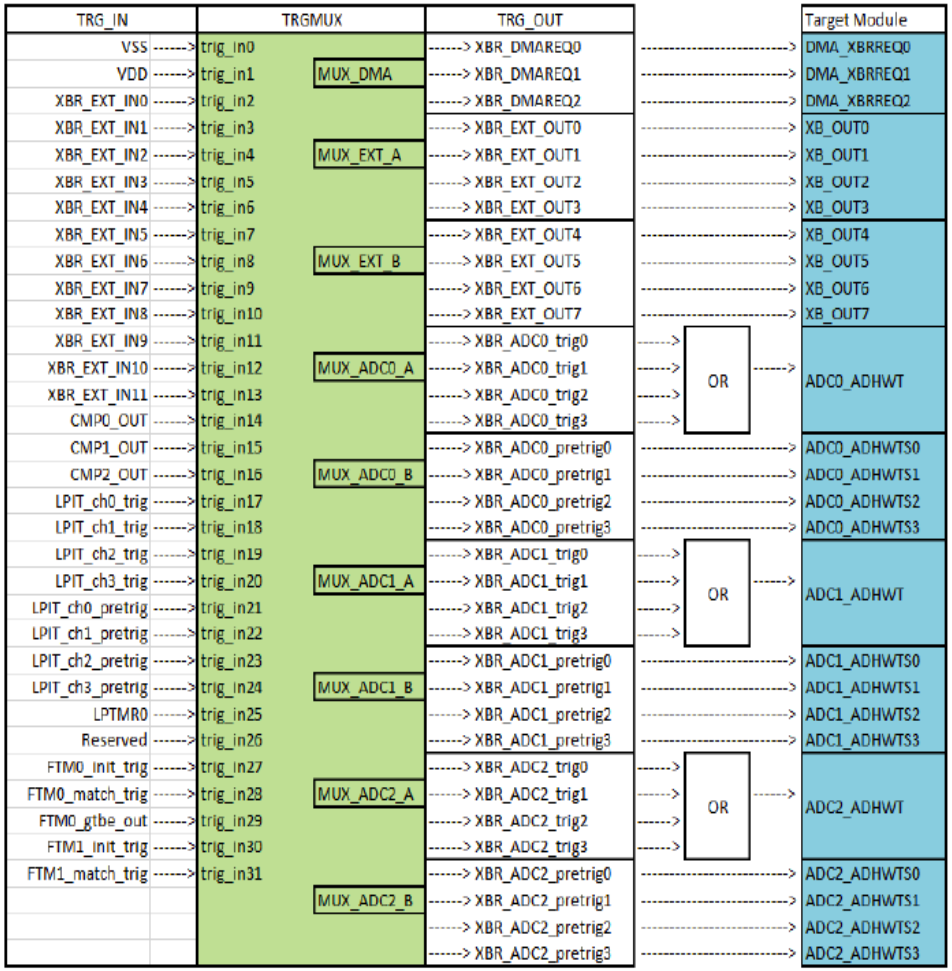
"FlexIO" — **Flexible input and output peripheral**

- Highly configurable module providing a wide range of functionality including:
  - Emulation of a variety of communication protocols: UART, I2C, SPI, I2S, etc.
  - Flexible 16-bit timers with support for a variety of trigger, reset, enable and disable conditions
- Creates an interlink between GPIO method of software emulation and exact hardware peripheral module
- Can continue operating under debug / stop modes
- Support of polling/interrupt/DMA (RX/TX) operation
- Low software/CPU overhead

- The FlexIO peripheral was initially introduced on the Freescale Kinetis KL43 family

Trigger Multiplexer

- **Flexible signal interconnection among peripherals**
- Connects any of 64 signals on left side to the output on right side (multiplexer)
- Total 27 multiplexers
- Increase flexibility of peripheral configuration according to user needs
- Each peripheral which accept external triggers will usually have one specific 32-bit trigger control register
- Each control register support up to 4 triggers
- Each trigger can be selected from up to 64 inputs



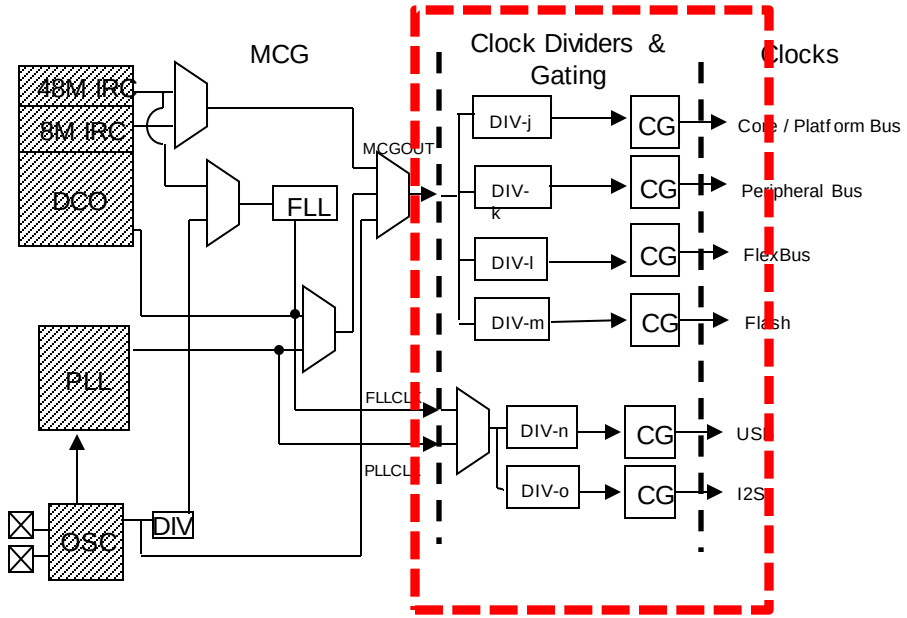
TRGMUX vs CTU

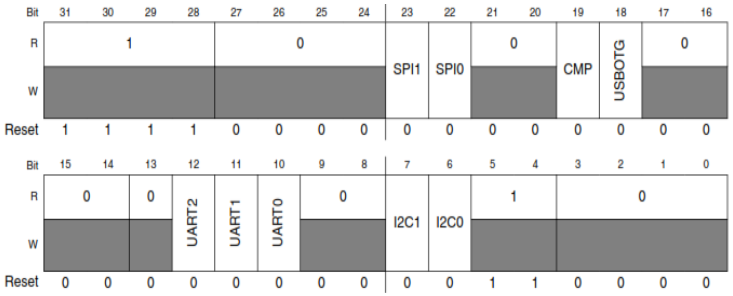
Feature	MPC560xB	ARM® Cortex® Platform
Trigger Units	Cross Trigger Unit	Trigger Multiplexer Programmable Delay Block
Trigger signals	64 inputs 64 outputs	64 inputs 54 outputs (each output selectable from 64 inputs)
Trigger Sources	eMIOS (PWM) PIT Timer	TRIGMUX CMP, LPIT, FTM ADC, PDB, RTC FlexIO, CMP, LPUART, LPI2C LPSPI, SIM
Trigger Targets	DMA ADC	DMA, ADC, TRGMUX, CMP, FTM PDB, FlexIO, LPIT LPUART, LPI2C, LPSPI LPTMR, TSI_HW

Keep the Energy Budget Low with ARM Cortex Platform

Intelligent Clock/Speed Selection

- This what we call clock scaling & gating
- Peripheral clocks are disabled by default so there is no wasted power consumption
- Various clock sources :
- Slow or high speed, internal or external with PLL/FLL to reach higher frequencies
- OUTDIV prescaler allow to divide main frequency to supply internal peripherals
- CG allow to cut clock “manually” per peripherals (in standby or run mode)
- Automatic platform clocking control in Compute Operation and Partial STOP options further reducing dynamic power consumption

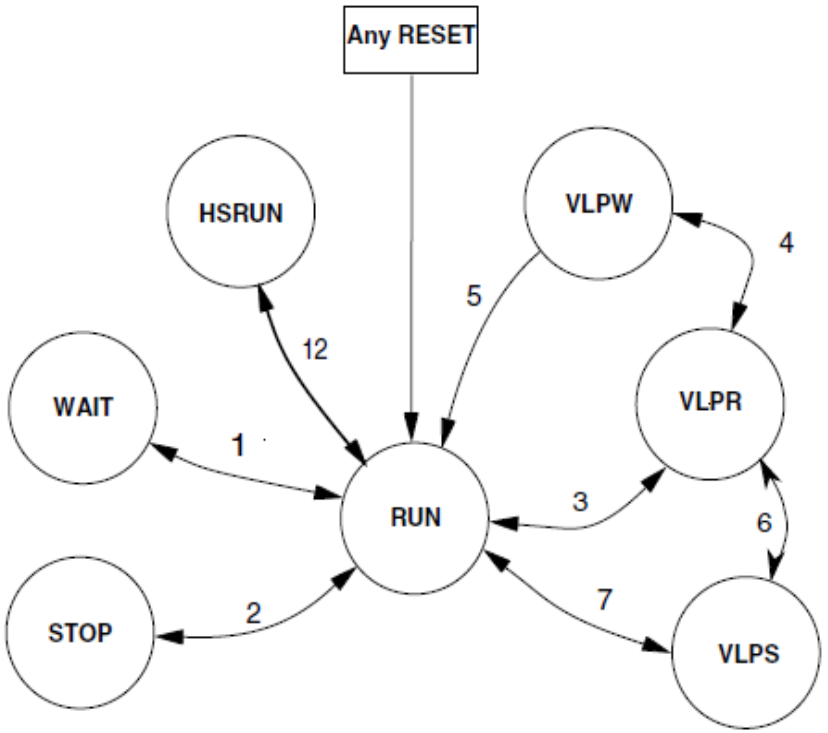




SIM_SCGx registers

Power Modes

- **Simplified Mode control**
  - Ease of software use
  - Ease of power mode transitions
  - All modules maintained in ALL modes
  - All RAM content maintained in ALL modes
  - All I/O maintained in ALL modes
  - Software friendly architecture
  - Autosar certified drivers available



ALL memory and ***ALL*** registers and ***ALL*** I/O are ***ALWAYS*** maintained in ***ALL*** modes!!!

Power Consumption Comparison

Feature	MPC5604B @25C	MPC5604B @125 Max		ARM Cortex platform @25C	ARM Cortex platform @125C
RUN		TYP: 51 mA MAX: 125mA @64Mhz	High Speed Run Mode	~40mA @ 112 MHz	TBD @ 112 MHz
			Normal Run mode (all periph enabled)	19 mA @ 80 MHz	43 mA @ 80 MHz
HALT	TYP: 8mA MAX: 15mA	TYP: 14mA MAX: 25mA	Wait	10mA	TBD
STOP (No clock, FIRC 16 MHz off, SIRC (28 kHz on, PLL off, HPvreg off, ULPVreg/LPVreg on)	TYP: 180uA MAX: 700uA	TYP: 4.5mA MAX: 12mA	STOP (static mode, maintaining LVD detection, regulator in LPM)	250uA	TBD
			VLPR (code from Flash, IRC clock, ADC on)	2.7mA @8MHz	TBD
			VLPW (similar to VLPR, CPU in SLEEP mode)	<1.9mA @8Mhz	TBD
STANDBY1 (ULPreg on, HP/LPVreg off, 8 KB RAM on	TYP: 20uA MAX: 60uA	TYP: 280uA MAX: 900uA	VLPS (static mode, all registers and RAM maintained.LVD off)	25uA	TBD
STANDBY2 (ULPreg on, HP/LPVreg off, 32 KB RAM on)	TYP: 30uA MAX: 100uA	TYP: 560uA MAX: 1700uA			

Safety Features

Safety/Security hardware features + Freescale SafeAssure program

- **Cyclic Redundancy Check (CRC)**
- **Internal & External Watchdog (WDOG)**
- **Error correcting code (ECC) on Flash memories**
- **128-bit unique ID number**
- **Memory Protection Unit (MPU)**

Safety Features

SAFE ASSURE™ by Freescale

ARM Cortex Platform Safety Measures

Single Point Fault Metric

- RAM ECC
- Flash ECC
- Undervoltage monitoring
- Clock Monitoring
- Temporal protection – Software Watch dog
- Register protection
- CRC
- Individual Peripheral safety support measures

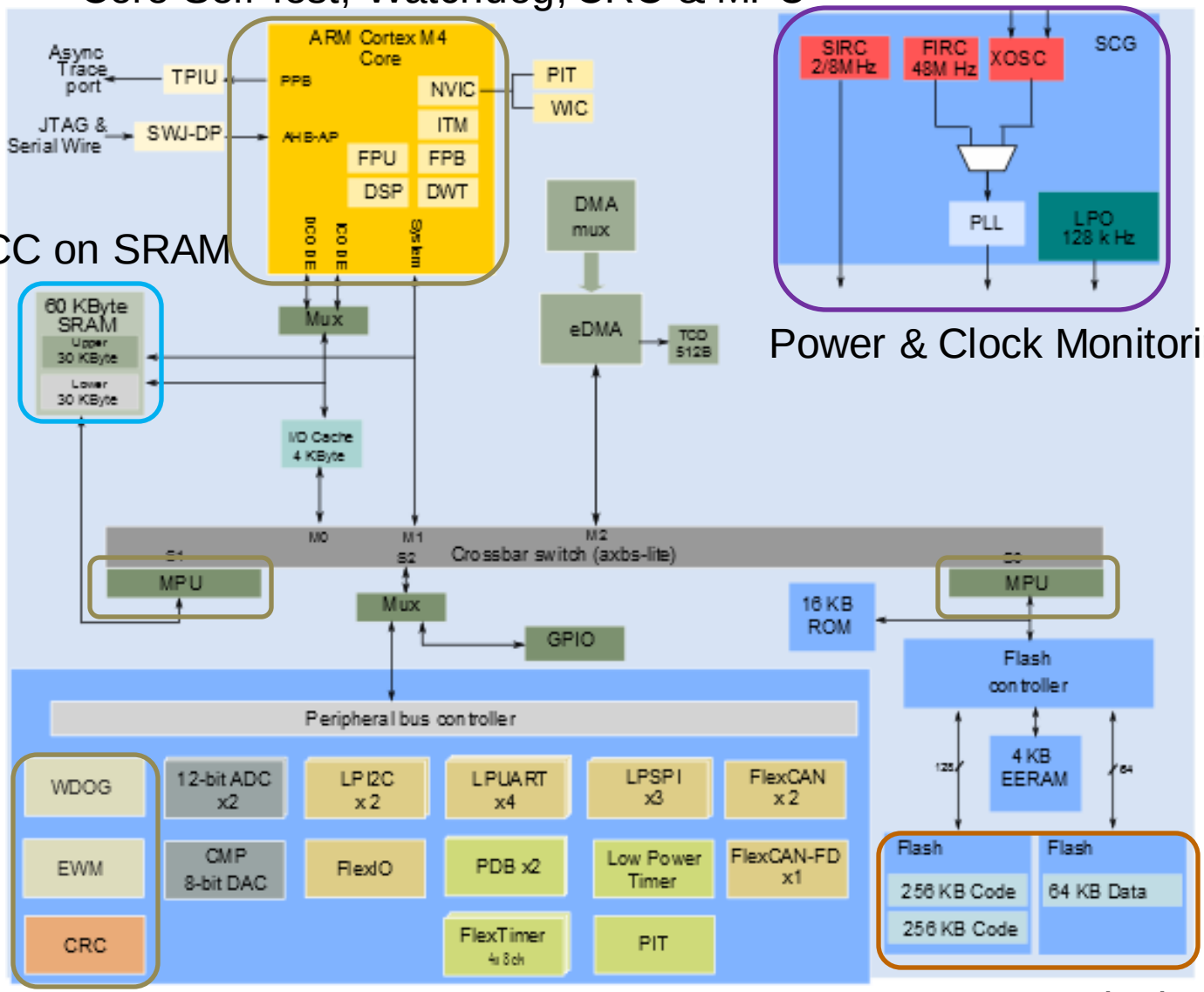
Error Management Modules

- Error Reporting Module
  - Error address capturing
  - Interface for error managemen of ECC errors, E2E ECC, etc.

S32K High Level Architecture

Core Self Test, Watchdog, CRC & MPU

ECC on SRAM



Power & Clock Monitoring

ECC on Flash

Tools and Enablement

- **Software enablement**
  MCAL, Low level drivers, LIN driver, Header file
- **Hardware enablement**
  Evaluation board
- **Tool support**
  IDE, Debugger, Compiler

Reduce Your R&D Effort/Time-to-Market

- Complete enablement with tools and software ecosystem
- Quick to prototype (out of the box)
- Quick to take to production (prototype with Freescale auto quality software)
- Expand software offering into higher levels of abstraction / model-based design

Future-proof Your Design

- See software as an investment, not a cost
- Scalability / ARM portfolio

ARM Cortex Platform Easy Enablement: Rapid Prototyping for Quality Software Development

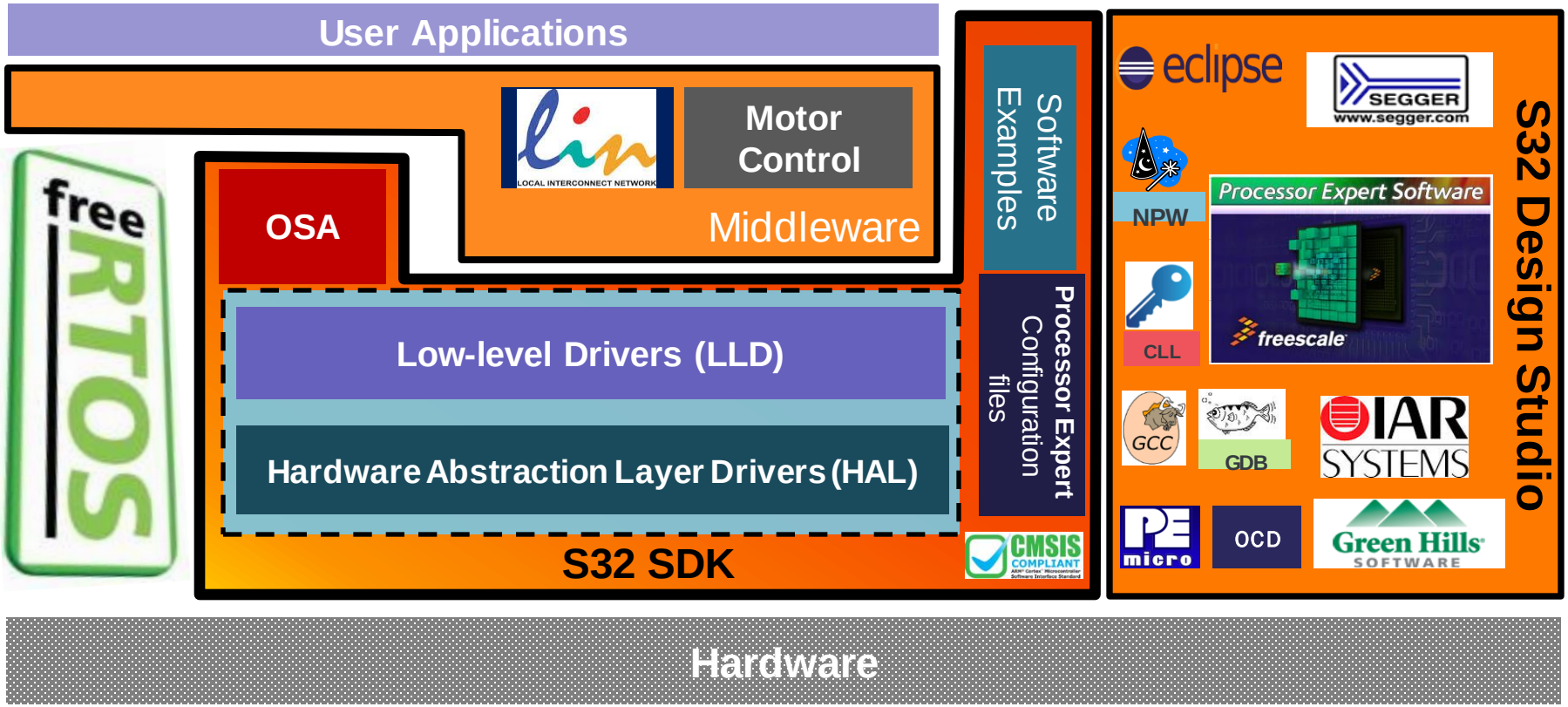
- **Freescale Enablement:**
  - Math and Motor Control Library
  - S32K Self Test Functional Safety Software
  - FreeMASTER
  - MISRA compliant Header File
- **IDE Debugger/Compiler**
  - S32Design Studio
  - IAR
  - Keil
  - GHS Compiler
- **Operating Systems:**
  - AUTOSAR OS
- **Drivers**
  - LIN Stack
  - Bare Metal Drivers
  - AUTOSAR MCAL
- **Debugger Interface**
  - P&E Micro: Umultilink
  - Lauterbach
  - Segger
  - iSystem Debugger

Start your application with S32 Design Studio

- Leverage the Eclipse Updater and Marketplace into a one-stop-shop IDE
- Integrated with Freescale S32K SDK and Middleware Software Products
- Model Based Design support
- Embedded Tools
  - Processor Expert Configurator
  - Initialization Tools
  - Pin Settings
  - Motor Control Toolbox
  - Bootloader
- Integrated Build Toolchains
  - GHS
  - IAR
  - Linaro GCC
- Integrated Debuggers
  - Seeger, P&E

SDK Software Ecosystem

- **Freescale Software Products** feature the **S32 SDK, Middleware** like **Motor Control Libraries** and a **LIN Communication Stack** as well as the **S32 Design Studio.**
- A large variety of **Open Source Software and Tools** including the **freeRTOS** Operating System can be leveraged from the Cortex-M4 software ecosystem.



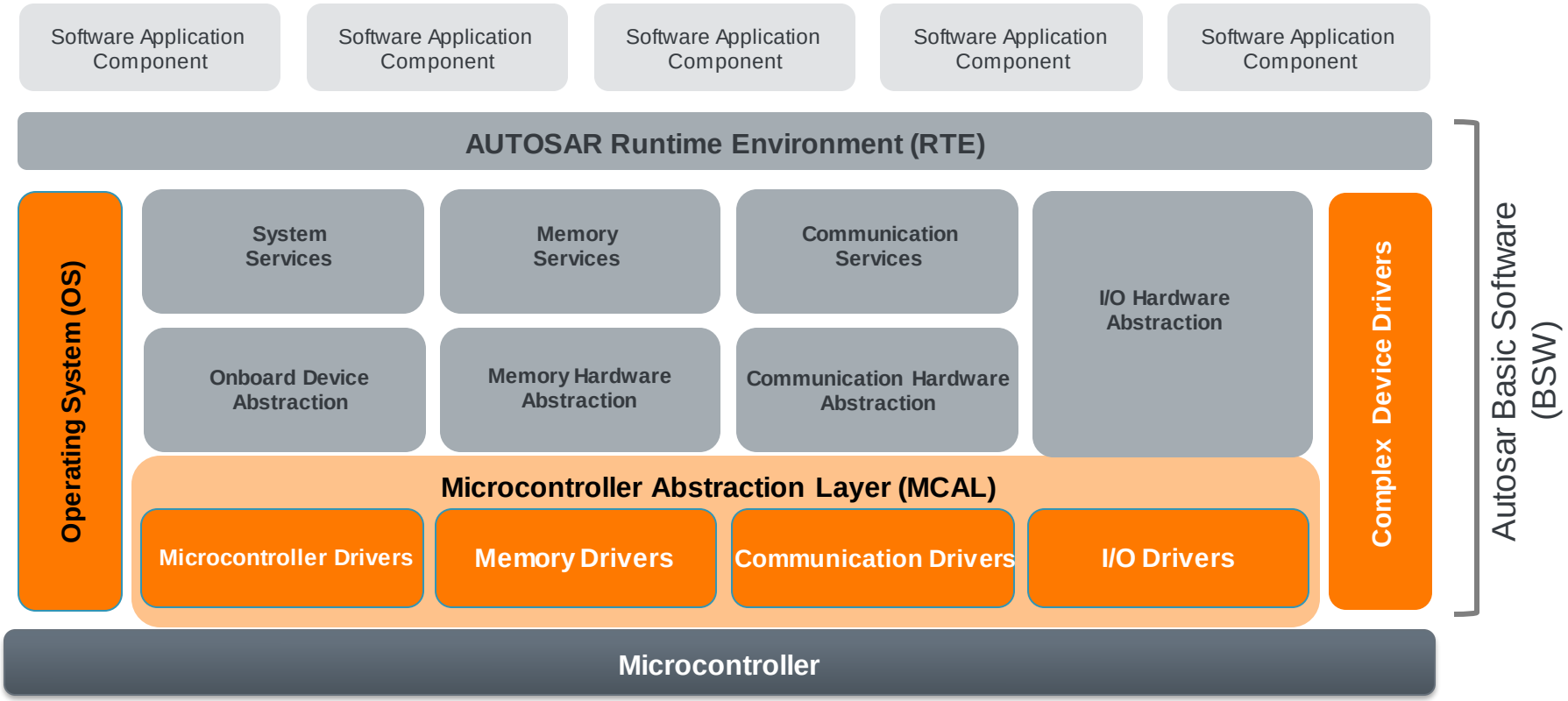
ARM Cortex Platform SDK

What's inside the package:

- **A complete solution for application development containing:**
  - Low Level Drivers (LLD) and Hardware Abstraction Layer Drivers (HAL) implementing the CMSIS industry standard for ARM Cortex-M software
  - An OS Abstraction Layer (OSA) allowing the SDK to be integrated with a variety of real time operating systems
  - Drivers Configuration Models to best fit your application
  - LIN Protocol Stack (also available separately)
  - eNVM (NVM and EEPROM Emulation) Drivers (also available separately)
- **Integrated in the S32 Design Studio**

AUTOSAR Software Ecosystem

- **Freescale Software Products** include the AUTOSAR Operating System, AUTOSAR MCAL Drivers and Complex Device Drivers
- **The full AUTOSAR RTE** (Run Time Environment) stack is available through our integration partners



AUTOSAR MCU Abstraction Layer (MCAL)

What's inside the package:

- Complete set of drivers implementing the AUTOSAR 4.x specification
- Fully configurable to best fit any application compatible with all AUTOSAR standard configuration tools.
- Certified SPICE Level 3 and ready for automotive production
- Delivered as source code, integrating support for industry leading build toolchains
- Example of integration with AUTOSAR OS and other basic usage scenarios included in the package
- Complex Device Drivers enabling dedicated peripherals (like DMA)

AUTOSAR Operating System

What's inside the package:

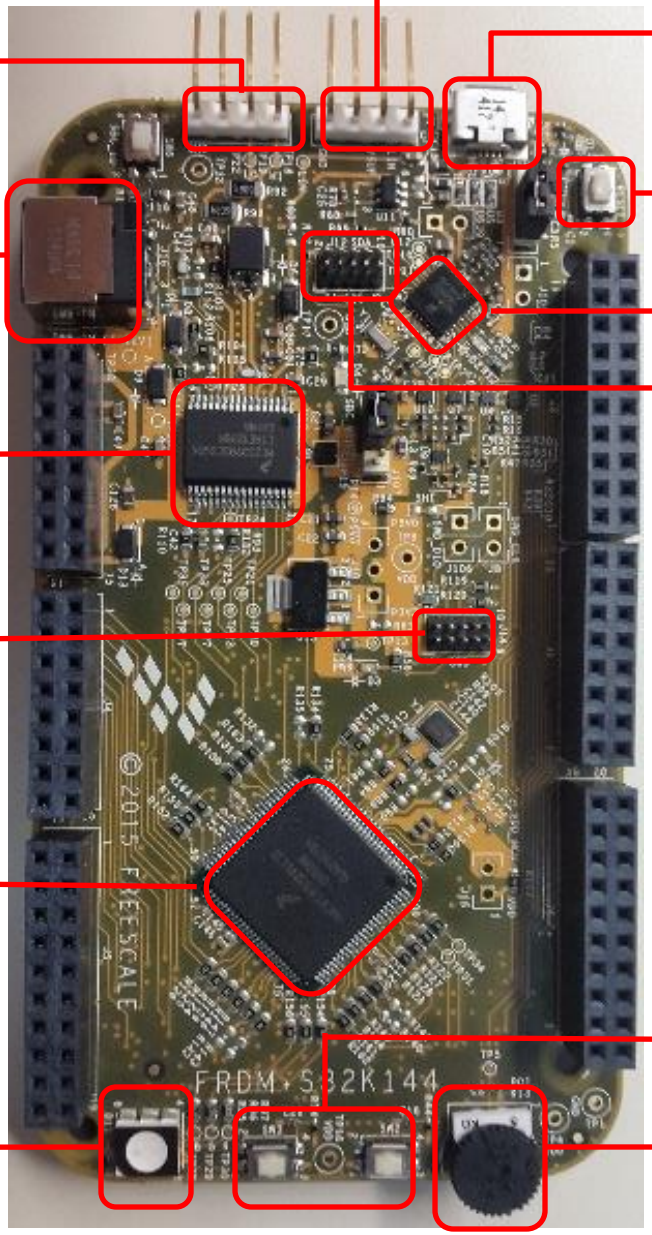
- A Real Time Operating System (RTOS) implementing the AUTOSAR 4.x specification
- Fully configurable to best fit any application compatible with all AUTOSAR standard configuration tools.
- Unleashing the full performance potential of Freescale MCUs at a minimal footprint
- Certified SPICE Level 3 and ready for automotive production
- Delivered as source code, integrating support for industry leading build toolchains

Self Test Functional Safety Software

Freescale Software Products for ISO 26262 applications feature the **Self Test Software Library for Cortex M**:

- Structural Core Self Test Library (SCST) is a safety measure against permanents faults in the cores
- Developed for detecting hardware permanent faults in a core by means of executing machine op-codes with fixed set of operands and comparing their execution results
- This library is designed as a Safety Element out of Context and was developed according to **ASIL B**

S32K EVB



CAN Bus

LIN Bus

OpenSDA USB

External Power Supply (5-12V)

Reset Button

OpenSDA MCU

OpenSDA JTAG

System Basis Chip MCZ33903

S32K144 JTAG

S32K144 MCU

User Buttons

RGB LED

Potentiometer

Summary

- **S32K requires less external components and less power connectons**
  Than MPC560xB
- **ARM Cores will come to other modules in the car**
  Cortex M4 core offers performance and low power consumtption in the S32K
- **Safety all around**
  S32K was made with automotive safety in mind
- **Tools and enablement like never before**
  S32 design studio, MCAL, third party compilers and debuggers

www.Freescale.com