AN5271

MC33771 / MC33772 / MC33664 Daisy chain guidelines

Rev. 1.0 — 24 June 2016 Application note

1 Introduction

NXP Semiconductors has developed a battery cell controller IC supporting both centralized and distributed battery management architectures.

Centralized battery monitoring systems contain a controller module that senses individual differential cell voltages through a wiring harness.

Distributed systems locate monitoring devices close to the Lithium-ion cells and use a communication interface to transfer data to the main controller MCU.

The MC33771/MC33772 (battery cell controller) and MC33664 (TPL transceiver) communication solution is based on a passive electrical bus (no repeater, no amplifier). High-speed differential isolated communication is achieved through the use of transformers.

The benefits of such a solution are:

- more robust Electromagnetic Compatibility (EMC) characteristics (intrinsic transformer common mode rejection)
- greater high-voltage isolation
- better communication speeds and synchronized measurements
- lower cost

Because four bits are reserved to address each node in the 40-bit message frame, a TPL daisy chain is limited to a maximum of 15 nodes. The topology (distributed, centralized) of the system, the min/max temperature and the characteristics of the transformer may reduce the length below 15 nodes.

This application note provides guidelines on how to build a multi-node daisy chain for high-voltage systems when more than two nodes are required.

2 Daisy chain operating mode

2.1 TPL communication protocol

The transformer physical layer in the pack controller (see Figure 1) creates a pulse phase modulated signal transmitted to the bus through the transformer.

The MC33664 receives SPI transmit signals from the MCU and creates bit-by-bit pulse phase encoded differential signals which are transmitted to the bus through an isolating transformer. SPI data to transmit is determined on the falling edge of SCLK_TX. Bus messages received by the MC33664 through the isolation transformer are converted bit by bit and transferred through CSB_RX, SCLK_RX and DATA_RX to the MCU.

To start a message transmission, the MCU sets (low active) CSB_TX. The falling edge of CSB_TX is a start of message (SOM) indicator causing the MC33664 to initiate a message transmission. On the falling edge of CSB_TX, the MC33664 generates

a positive phase-encoded double pulse signal on the bus. With each SPI SCLK_TX from the MCU, the MC33664 generates a single differential positive or negative pulse, depending on the level of the DATA_TX signal. On the rising edge of CSB_TX the 33664 generates two negative pulses indicating an end of message (EOM) transmission.

Receiving messages from the bus begins with the SOM pulse. On reception of the SOM, the MC33664 sets the CSB_RX signal to low. Each following single pulse generates a logic 1 or a logic 0 depending on the pulse phase. The bit information is clocked to the MCU through the SCLK_RX and DATA_RX pins. Receiving the EOM transmission ends the message and transitions the CSB_RX signal to high.

Command and response message frames are sent and received at a 2.0 Mb/s bit rate.

2.2 Bus structure description / distributed daisy chain configuration

A typical initialized daisy chain configuration is shown in Figure 1, with one TPL connected to a series (from 1 to 15) of battery cell controllers. Two pulse transformers are inserted between each node to insure higher EMC robustness and fully isolated, potential free connections. Connections between nodes are done with unshielded twisted pair cables.

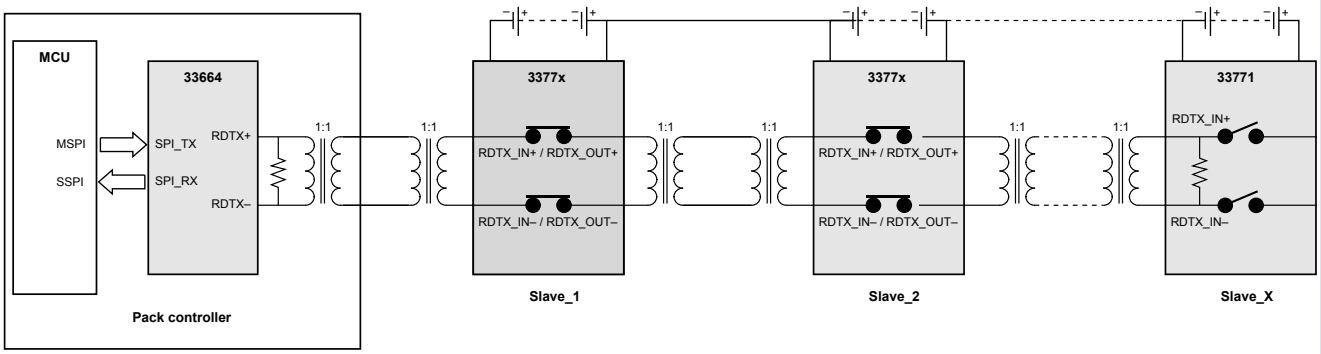

Figure 1. Distributed daisy chain block diagram

2.2.1 Initialization sequence

For impedance matching and network stability, the MC3377x contains a 300 Ω embedded termination resistor external to the MC33664.

Each node on the daisy chain is dynamically initialized at power-up (or after a reset) by the pack controller. Using a 4-bit register, an address (CID) from 1 to 15 is attributed sequentially to each node.

At power-up (or after a reset), the MC3377x cluster identification (CID) is set to 0, the embedded resistor is connected and the bus switches are opened. After each MC3377x initialization, a CID (between 1 and 15) is given. The pack controller closes the bus switches to communicate to the next MC3377x in the chain, which then automatically disconnects its embedded resistor. The last MC3377x in the system should remain with the bus switches open, which automatically connects the embedded resistor.

2.3 Message structure

Command and response message frames are sent and received at 2.0 Mb/s bit rate. The message bits are Manchester encoded at a frequency of 4.0 MHz.

Messages are made of 40 bits encapsulated by a SOM (two positive-phase pulses), and an EOM (two negative-phase pulses). See Figure 2.

The integrity of the message is checked for all transmissions. Any of the following conditions is flagged as a communication failure:

- Incorrect message length (40 bits)
- Incorrect CRC

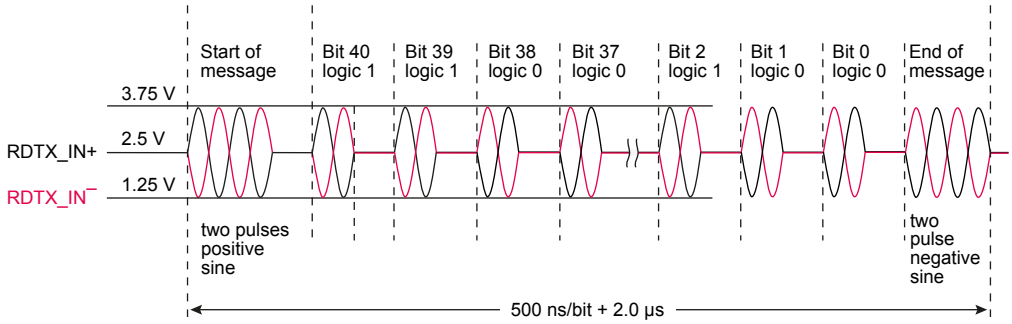

Figure 2. Message format

2.4 Electrical signalling

For RDTX pins on the IC side (MC3377x or MC33664), the transformer is biased with a nominal voltage of 2.5 V when the transmitter is in a tri-state mode. When sending or receiving, this voltage is modulated with a ±1.25 V sine wave in opposite phases on RDTX+ and RDTX-.

The differential peak voltage on the transformer input is (RDTXIN+) − (RDTXIN−) = 2.5 V_{PP} nominal; the differential peak to peak voltage is 5 V_{PP} nominal. See Figure 3.

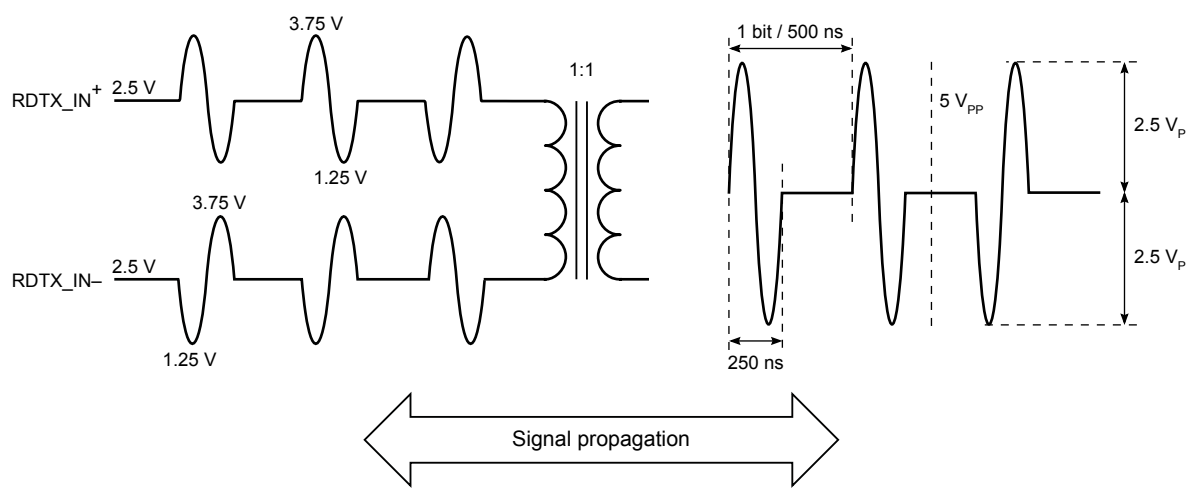

Figure 3. Signal waveform

A single bit consists of a 250 ns phase-modulated signal followed by 250 ns of no activity. With amplitude, both parts should comply with specific requirements described later in this document.

In this application note, all measurements are done by referring to differential measurements of both signal lines on the transformer side.

2.5 TPL message detection

Both the MC33771 and the MC33664 have the same TPL receiver circuitry and both perform the same. Later in this document, any reference to TPL applies to both the MC33771 and the MC33664.

The TPL receiver consists of an analog differential input comparator that detects when the input sine wave positive phases (pos_det) and negative phases (neg_det) exceed a specific threshold.

A logic 1 is represented by a pos_det signal followed by a neg_det signal. A logic 0 is represented by a neg_det signal followed by a pos_det signal. To be valid, two successive bits must be separated by a specified blanking time with no bit detection allowed. If this does not occur, the whole message is discarded. A SOM is identified by two successive pos_det bits with no blanking time in between. An EOM is identified by two successive neg_det signals with no blanking time in between. An EOM is valid only if 40 bits have been received before the EOM occurs. If this condition is not met, the whole message is discarded.

3 Attenuation and overshoots description

Because of the passive nature of the daisy chain, a signal sent by a given node may be progressively attenuated and distorted as it propagates along the chain.

3.1 Attenuation

Attenuation is the main critical parameter in the daisy chain. Communication fails if both sine wave amplitude phase levels on all node inputs do not reach a minimum value.

Attenuation results from the cumulative effect of factors such as an unbalanced daisy chain, cable loss, loss of transformers and so forth. Attenuation varies depending on conditions such as the number of initialized nodes and the temperature.

All the voltage values in the following plots are the minimum differential peak value measured on the specified node (BCC) on the lowest positive or negative sine wave phase. See Figure 4.

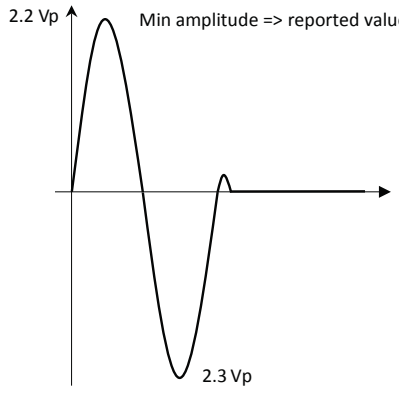

Figure 4. Sine wave amplitude

3.1.1 Eight-node daisy chain attenuation example

With a typical daisy chain component (Sumida 4180/C transformer and recommended MC33771/MC33664 component setups) and a typical daisy chain configuration (1.0 m between master and slave_1; 0.5 m between slave nodes) at room temperature, attenuation along the daisy chain is non-linear, as illustrated in Figure 5.

Figure 5. Attenuation along an eight-node chain

The lowest amplitude is approximatively in the middle of the chain: Slave_5 for a message from Master and Slave_3 for a message from Slave_8.

Thereafter, due to resonance effects, the amplitude increases up to the last node input (either Slave_8 or Master).

This bath tub curve effect can be either greater or lesser, depending on the number of nodes in the chain, the load and the transformer characteristics.

3.1.2 Eight-node daisy chain: sine wave aspect

In this case, a bit 1 sent by the master was observed all along the daisy chain, with two Sumida 4180/C transformers per slave and specified capacitors on the TPL and BCC evaluation boards (see the MC33771 data sheet section **TPL Bus components** for more information).

Figure 6 shows the shape on the Master output, Slave_4 input (middle of the chain), and Slave_8 input (end of daisy chain).

Master output : Differential 5.0 V_{PP} sine wave (2.5 V_P)

Slave_4 : Note the attenuation effect on the first sine wave (2.2 V_P), and the appearance of a ringing at the end of the bit modulation (0.4 V_P). Note also the non-symmetrical effect with the negative sine wave amplitude (2.3 V_P) slightly higher than the first one (2.2 V_P).

Slave_8 : Compared with the signal on the middle of the chain, notice the amplitude gain due to a resonance effect. Both sine wave amplitudes increased. The positive amplitude is around 2.4 V_P; the negative is around 3.0 V_P and the ringing is around 0.9 V_P .

The same affect applies when a negative pulse occurs first, followed by a positive pulse for bit value = 0.

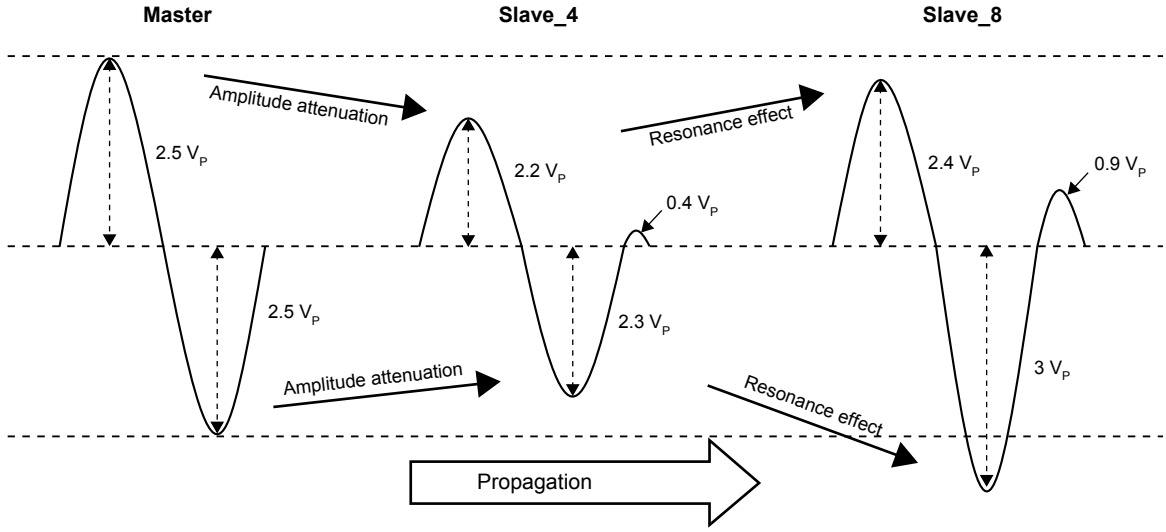

Figure 6. Message attenuation and overshoot

3.1.3 Fifteen-node daisy chain attenuation example

With a typical daisy chain component (Sumida 4180/C transformer and recommended MC33771/MC33664 component setups) and a typical daisy chain configuration (1.0 m between Master and Slave_1; 0.5 m between slave nodes), at room temperature, attenuation along the daisy chain is non-linear, as illustrated in Figure 7.

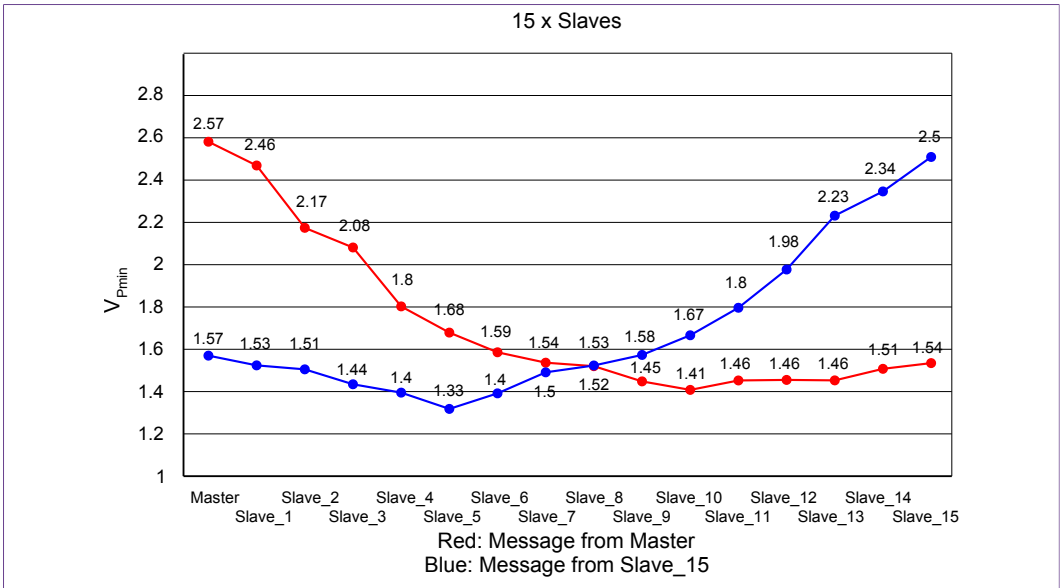

Figure 7. Attenuation along a fifteen node chain

The lowest amplitude is observed on Slave_10 input. Because of the resonance effect, the amplitude slightly increases up to the last node input (Slave_15).

3.2 Overshoots

Due to the RLC model of the line, some resonance effects may induce overshoots (or ringing). The equivalent impedance depends on the number of nodes and the cable length. The overshoots shape and level change accordingly.

A bit message can be split in two 250 ns periods. One (named the **active bit** period) is used by the TPL receiver to detect the bit information. During the second period (named the **quiet** period), no activity should be detected. Overshoots may impact both periods, with associated drawbacks as well as benefits.

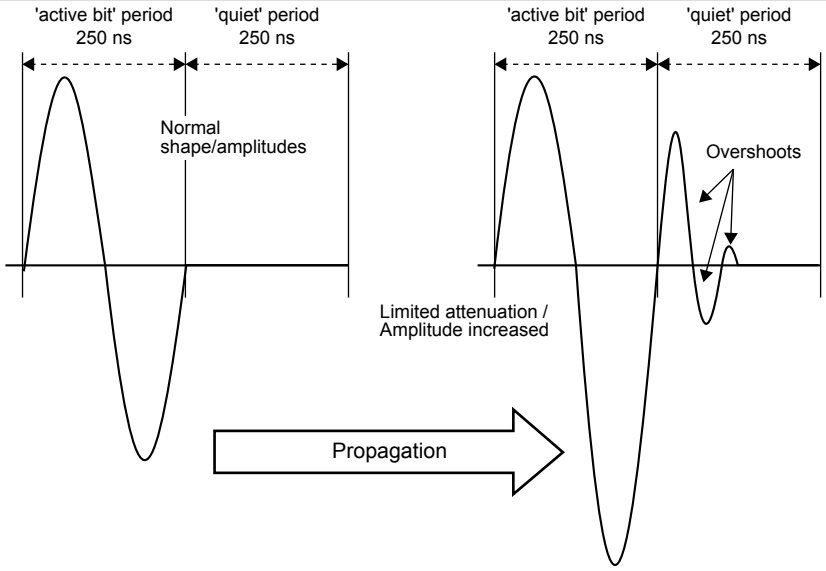

Figure 8. Signal overshoots

3.2.1 Drawbacks

An overshoot might be detected by the TPL receiver outside of a normal bit pattern (or SOM/EOM) during the quiet period. This would invalidate the incoming message and the communication would fail.

The TPL receiver is relatively robust against overshoots, which are transparent if they comply with certain patterns.

The higher overshoots are observed with short initialized daisy chains (below 8 slaves) with a maximum around slave 6 or slave 7. After slave 8, the attenuation becomes preponderant and limits the size of the overshoot.

Daisy chain behavior must also be verified during initialization. As the initialization progresses, the daisy chain behaves successively as a one slave chain, than a two slave chain, and so forth. Overshoots may occur during this progression and cause initialization failure.

To load the chain and limit high overshoots, the chain must be terminated with the embedded 300 Ω resistor in the last initialized MC3377x.

3.2.2 Benefits

The main benefit of overshoots is that they limit attenuation. The active bit pulses may have their amplitudes increased by the overshoot effects, which is a critical consideration for long daisy chains.

4 Attenuation and overshoot limits

Attenuation and overshoots are the main parameters that should be evaluated when designing and debugging a daisy chain setup. This section examines the limitations associated with both parameters.

4.1 MC33771 and MC33664 RDTX characteristics

4.1.1 TPL receiver threshold voltages

Below are minimum and maximum threshold input voltages at three temperatures (V_{PEAK}).

Vin_max

Vin_max at 125 °C : 1.16 V_P
Vin_max at 25 °C : 1.16 V_P
Vin_max at −40 °C : 1.07 V_P

Vin_min

Vin_min at 125 °C : 0.99 V_P
Vin_min at 25 °C : 0.9 V_P
Vin_min at −40 °C : 0.89 V_P

Vin_max : To guarantee a detection by the TPL receiver, the sine wave amplitude (either positive or negative) for all nodes should exceed Vin_max. This factor must be taken into account with respect to attenuation.

Vin_min : To guarantee a non-detection by the TPL receiver, the sine wave amplitude (either positive or negative) should not exceed Vin_min. This factor must be taken into account with respect to overshoot.

4.1.2 RDTX output levels

The MC33664 and the MC33771 both have the same TPL transceiver circuitry.

According to the MC33664 data sheet, the differential peak RDTX output level is nominal 2.5 V_P, min 2.2 V_P, max 3.0 V_P, with VCC5 = 5.0 V. The TPL transceiver circuit supply is VCC5. By specification, the minimum value for VCC5 is 4.75 V. However, to obtain the maximum RDTX output voltage, VCC5 should be set at no less than 5.0 V.

For MC33771, the TPL transceiver circuit supply is internal.

4.2 Bit timing description

One 500 ns bit signal can be split into three areas, as shown in Figure 9 .

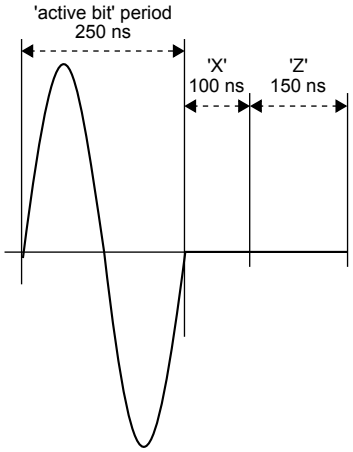

Figure 9. Bit timing structure

4.2.1 Active bit period

This is the useful phase modulated signal. To be detected by the internal TPL receiver, a pulse's amplitude must exceed Vin_min (see Section 4.1.1 "TPL receiver threshold voltages"). Depending on transformer characteristics, the amplitude may be lower at cold temperatures and should be verified.

4.2.2 X window

This 100 ns timing window corresponds to a ‘blanking’ window for the TPL receiver. All detections due to a high overshoot exceeding Vin_min are discarded. There are no overshoot voltage level constraints during this period.

4.2.3 Z window

During this period, the TPL receiver is enabled to allow detection of SOM or EOM bits. When a bit transmission is in progress, a ripple that reaches Vin_min is detected and can lead to a communication failure.

4.3 Examples of sine wave aspects in a daisy chain

This section provides examples of possible sine wave distortions that may lead to communication issues.

4.3.1 Attenuation

During active bit periods, the sine wave should exceed Vin_max for both positive and negative sine waves at all node inputs.

Figure 10 shows a node input where the positive amplitude drops below Vin_max (dark grey area). In this case, the bit is not detected and communication fails for that node.

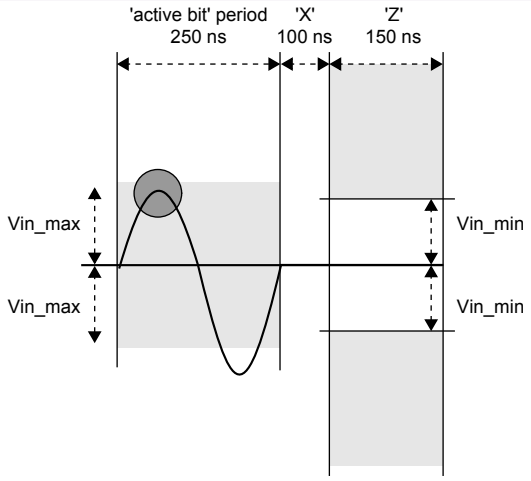

Figure 10. Attenuation

4.3.2 High-voltage smooth overshoots

During a Z window, the sine wave should not exceed Vin_min.

In Figure 11, a potential communication issue may arise because the signal amplitude (dark grey circle) exceeds Vin_min.

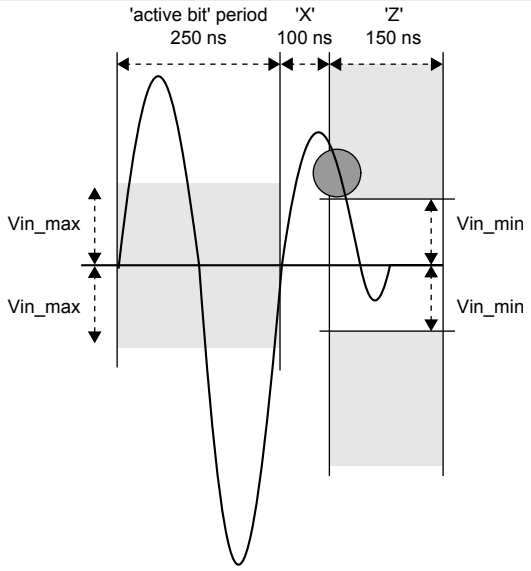

Figure 11. Smooth overshoot

4.3.3 High-voltage sharp overshoots

Figure 12 shows a strong overshoot occurring during the X period. However, no communication issues arise because both the Vin_min requirement in the active bit period and the Vin_max requirement in the Z period are maintained.

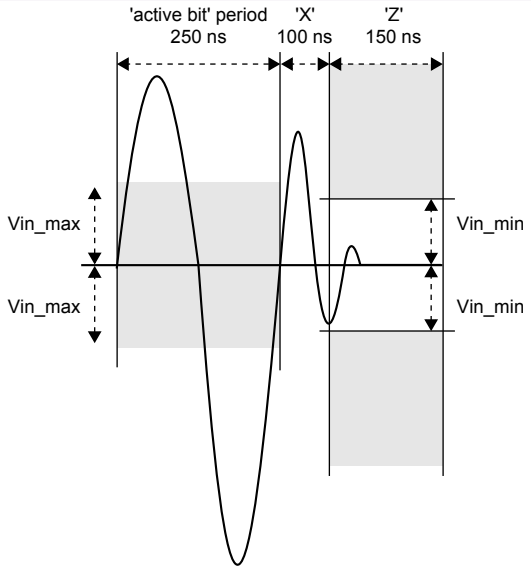

Figure 12. Sharp overshoots

5 System verification

5.1 Transformer and wire characteristics

5.1.1 Transformer characteristics

See the schematic recommendations in the MC33771 data sheet. The use of the Sumida transformer ESMIT 4180/C or a similar pulse transformer is highly recommended. The transformer must comply with the electrical characteristics in Table 1 .

Table 1. Transformer characteristics

Characteristic	Value
Primary Inductance at 100 KHz	200 µH min / 300 µH max
Turn ratio	1:1 (2 %)
Insertion loss	0.3 dB max
DC resistance	0.15 Ω max

5.1.2 Wire characteristics

The wires that connect the BCC and TPL evaluation boards should be 2x1 conductor twisted pair wire (no shielded wire required). Wire characteristics are described in Table 2.

Table 2. Wire characteristics

Characteristic	Value
AWG	22
Capacitance	18.5 pf/ft at 1 kHz, nominal conductor to conductor

Characteristic	Value
Conductor DCR	15.3 /1000 ft at 20 °C, nominal
Inductance	0.17 µH/ft, nominal
Characteristic Impedance	84 Ω
Twists	12.0 twists/foot (min)

5.1.3 Wire lengths

Table 3 shows the indicative maximum wire lengths (based on experimental data) with respect to the number or nodes in the daisy chain.

Table 3. Wire lengths

Number of nodes	Indicative maximum length between two nodes (meters)	Total length (meters)
≤ 5	2.0 m	2.0 m to 10 m
6 to 8	1.0 m	6.0 m to 8.0 m
9 to 12	0.5 m	4.5 m to 6.0 m
13 to 15	0.3 m	3.6 m to 4.5 m

5.2 Identification of communication failures

The first objective is to determine whether the communication failure is being caused by too much attenuation or by excessive overshoots.

For daisy chains with more than eight nodes, the behavior of the chain changes dynamically during initialization. Initially the chain exhibits short (< 8 nodes) daisy chain behavior, with failures typically related to overshoots. As initialization progresses, the chain begins to exhibit long (≥ 8 nodes) daisy chain behavior, with attenuation failures being more typical. During daisy chain development, communication testing should be applied to both the initialization phase and the post-initialization phase.

5.2.1 Procedure

The following verification procedure must be performed at room temperature:

1. Connect the complete daisy chain
2. Initialize the daisy chain and verify that there are no initialization issues. Initialization issues may occur for chains with fewer than eight nodes. If initialization issues are observed, see Section 5.2.2 "For failures related to overshoots"
3. After initialization, if communication failures are observed with the 8th node and beyond, the cause is likely to be too much attenuation (see Section 5.2.3 "For failures related to attenuation").
4. If no communication issues occur, measure the differential voltage on all nodes when the TPL sends a message. Evaluate the margin budget (see Section 5.3 "Margin"). Do the same characterizations (initialization and communication) at cold temperatures.

5.2.2 For failures related to overshoots

- Check the sine wave waveforms on the slave and master input nodes. See Section 4 "Attenuation and overshoot limits".
- Verify that the 300 Ω termination resistor is correctly switched on the last initialized slave.
- Verify that the external 300 Ω resistor is placed between RDTX pins of the TPL MC33664 IC.
- Verify the RDTX input/output pins capacitor values on the slave and master evaluation boards. On the MC3377x, it is recommended that the total capacitance per line stays between 10 pf and 50 pF (including common mode capacitors and TVS parasitic capacitance). See KIT33771TPLEVB schematic.
- Increase the wire lengths.

5.2.3 For failures related to attenuation

The maximum attenuation budget at cold temperature is 20 log(1.09/2.2) = −6.0 dB including wires, connectors and transformers.

(1.09 V_P is the Vin_max TPL receiver thresholds voltage at −40 °C. 2.2 V_P is the minimum RDTX output level.)

- Verify transformer, wire and connector characteristics (insertion loss).
- Check the sine wave waveforms and identify which communication aspect is failing.
- Check the sine wave amplitudes on the master input, the slaves around the middle of the chain and the last slave in the chain.
- Increase the VCC5 voltage for the MC33664.
- Reduce wire lengths.
- Use less inductive wires.
- Verify the RDTX input/output pins capacitor values on the slave and master evaluation boards. On the MC3377x, it is recommended that the total capacitance per line stays between 10 pf and 50 pF (including common mode capacitors and TVS parasitic capacitance). See KIT33771TPLEVB schematic.

Improving attenuation in long daisy chains may induce overshoots and lead to initialization failure. A compromise must be found between reducing attenuation and reducing overshoots.

5.2.3.1 Daisy chain split

To solve long daisy chains setup issues related to attenuation, split the daisy chain into several sub-chains, each with a lower number of nodes.

For example, a daisy chain of fourteen nodes can be split into two daisy chains of seven nodes each. One TPL IC per chain is required, which uses three SPI ports on the MCU side—two for RX and one for TX.

The address range is limited to 15 nodes. If more than 15 nodes are required, use additional MCU TX ports.

5.3 Margin

To compensate for attenuation issues, some margin 'budget' should be kept when designing a daisy chain. First characterizations are usually done at room temperature on a limited quantity of boards and transformers.

Based on measurements done with Sumida 4180/C transformers, additional attenuation may occur at cold temperatures (see Section 5.3.1 "Example of the low temperature (−40 °C) effect with a Sumida 4180/C transformer").

If another transformer is used, perform characterizations at the required temperatures to evaluate this additional attenuation.

5.3.1 Example of the low temperature (−40 °C) effect with a Sumida 4180/C transformer

Decreasing temperature increases attenuation. The plot below shows the simulation results of voltage attenuation along a 15-node daisy chain at room temperature (red plot: −40 °C) and cold temperature (blue plot).

Simulations were done with a Sumida 4180/c transformer and the recommended MC33771/MC33664 component setups. Daisy chain configuration characteristics are as follows:

- 1.0 m between Master and Slave_1
- 0.5 m between Slave nodes
- Signal sent by Master IC: 2.55 V_P

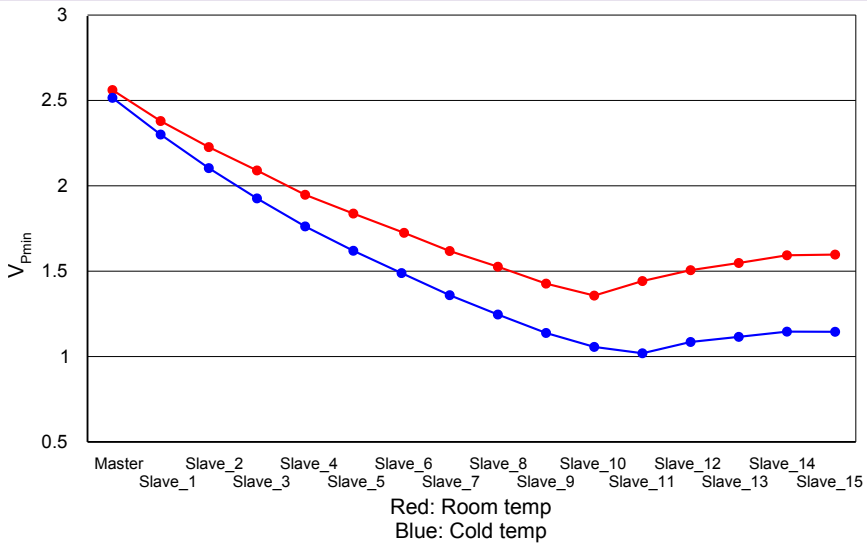

Figure 13. Comparison of Vpmin for a 15 node daisy chain at room and cold (-40 °C) simulation

With this setup, the relative voltage drop is between 0.4 V_P and 0.5 V_P on the lowest nodes (Slave_10 and Slave_11). If the voltage drop is greater than or equal to 0.5 V_P, the sine wave amplitude falls to 1.0 V_P on the Slave_11 input.

The RDTX input threshold is 1.09 V_P at −40 °C (see Section 4.1.1 "TPL receiver threshold voltages"). Slave_11 cannot capture the message sent by the Master.

5.3.2 TPL output voltage

MC33664 RDTX output voltages may be in the range 2.2 V_P to 3.0 V_P (see Section 4.1.2 "RDTX output levels"). It is best to evaluate the daisy chain behavior with the worst case 2.2 V_P because it shifts all the node voltages down.

6 References

The following are URLs where the user can obtain information on related NXP products and application solutions.

NXP.com support pages	Description	URL
MC33771	Product summary page	http://www.nxp.com/MC33771
Advanced Automotive Analog home page		http://www.nxp.com/analog

7 Revision history

Table 4. Revision history

Revision	Date	Description
1.0	6/2016	Initial public release

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Released on 24 June 2016