Optimizing Bias of LDMOS RF Power Amplifiers

Linear Power Amplifiers (PA's) based on LDMOS FET transistors are used widely in cellular base station transmission systems. These LDMOS transistors are used in CDMA and GSM PA's, and will also be used in the new W-CDMA applications which will require even better linearity at very high power (50 watts and more). Base station PA's, which are inherently nonlinear, can now be built to very tight specifications and fulfill the requirements of a "linear amplifier." Proper Biasing of the transistor in these amplifiers is essential to maximizing their performance and meeting the tight RF performance specifications.

Bias control of an LDMOS FET is done with DC control of the gate voltage. The gate voltage controls quiescent drain current, or I_{DQ}, which is set with no RF present. Each LDMOS transistor will require a unique gate voltage setting for the optimum drain current in a particular power amplifier design.

The process for setting the class AB Idq of the device is as follows:

1, With no RF drive present, adjust the Vdd drain voltage to the nominal setting as indicated in the functional test section of the data sheet..
2, Freescale LDMOS devices are enhancement mode parts, so the gate connection needs a positive voltage to initiate drain current. Starting with the gate setting at a zero voltage, slow increase the gate voltage setting while monitoring the drain current. The current should be very near zero mA until the gate voltage approaches the Vgs(th) value as noted in the data sheet.
3, Once the drain current starts to occur, slowly adjust the gate voltage until the proper recommended Idq value is reached as indicated on the data sheet. The Vgs voltage will be in the range listed in the data sheet and VgsQ and it varies from part to part.

This VgsQ setting is only a recommendation and it can be easily varied as much as +/- 50% in order to optimize the trade offs between improved back off linearity, P1dB compression and overall DC to RF conversion efficiency.