The power-down mode power consumption is very important for i.MX6UL VDD_SNVS_IN battery powered applications. To get an idea power consumption figure, the following items shall be well considered in system design:

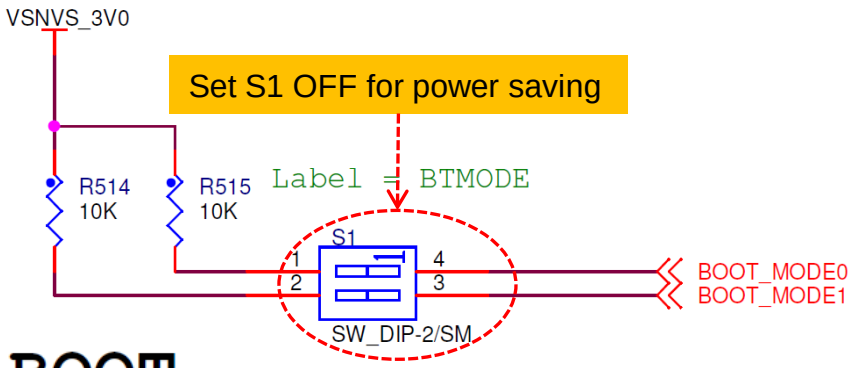
- **BOOT_MODE[1:0] pins connection.**
- **POR_B and SNVS_PMIC_ON_REQ pins connection.**
- **Tamper pins connection.**

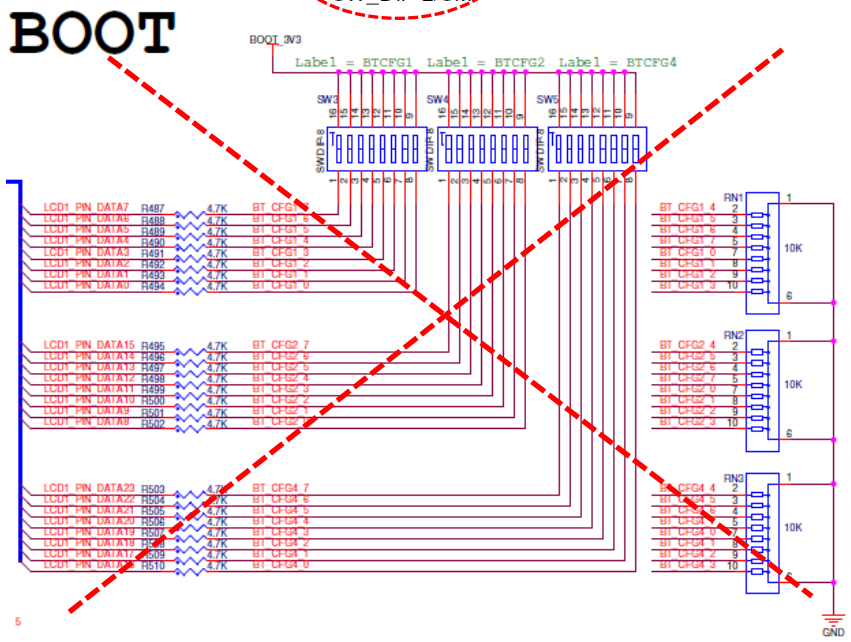
i.MX6UL BOOT_MODE[1:0] Pins Connection

1) There are 100KΩ pull-down resistors on BOOT_MODE[1:0] pins internally.
2) If set BOOT_MODE[1:0] = 01 for Serial Downloader, or set BOOT_MODE[1:0] = 10 for Internal Boot with the external 10KΩ resistor pulled up to VDD_SNVS_IN (VSNVS_3V0), it will cause around [3.0V / (100KΩ + 10KΩ) = 27uA] consumption current from VDD_SNVS_IN (VSNVS_3V0).
3) In system power-down mode, VDD_SNVS_IN (VSNVS_3V0) is powered from battery. 27uA consumption current from the battery is too large. To reduce it, it is better to set BOOT_MODE[1:0] = 00 for Boot From Fuses.
4) While the system boots from Fuses, the external bootstraps on LCD IF could be removed to optimize the PCB layout.

Table 95. 14x14 mm Functional Contact Assignments

Ball Name	14x14 Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
BOOT_MODE0	T10	VDD_SNVS_IN	GPIO	ALT5	BOOT_MODE0	Input	100 kΩ pull-down
BOOT_MODE1	U10	VDD_SNVS_IN	GPIO	ALT5	BOOT_MODE1	Input	100 kΩ pull-down



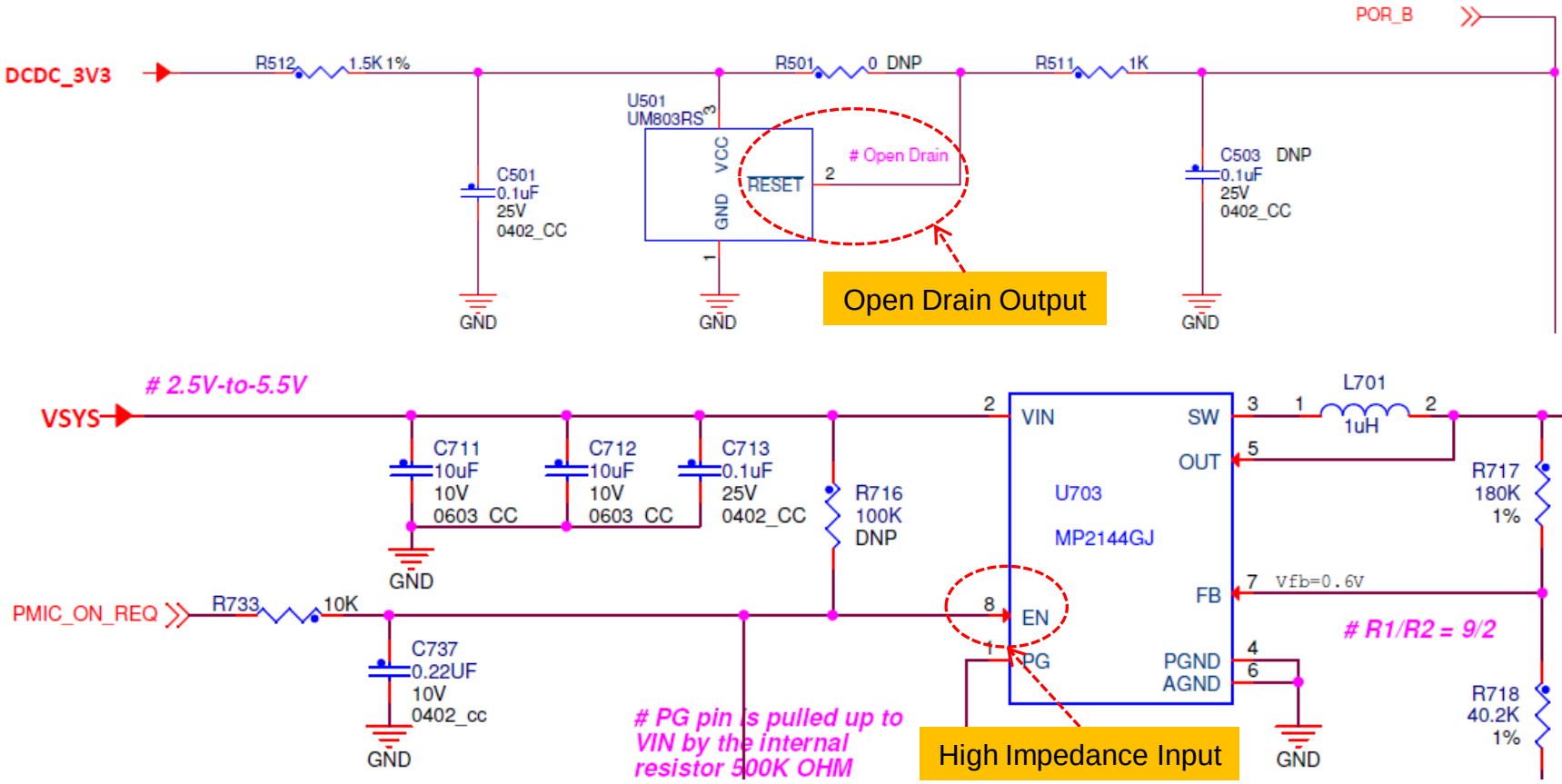


i.MX6UL POR_B and SNVS_PMIC_ON_REQ Pins Connection

1) There are 100KΩ resistors pulled up to VDD_SNVS_IN on POR_B and SNVS_PMIC_ON_REQ pins internally.
2) In system power-down mode, VDD_SNVS_IN is powered from battery.
3) To prevent power leakage from the battery in system power-down mode, external POR_B shall be open drain output, and SNVS_PMIC_ON_REQ shall be connected to high impedance input.

Table 95. 14x14 mm Functional Contact Assignments

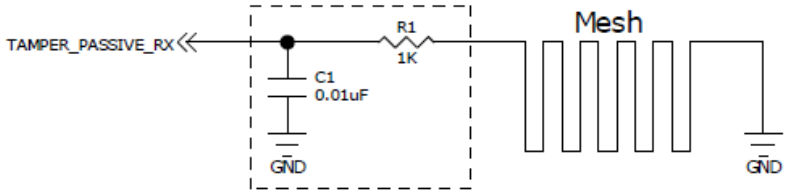
Ball Name	14x14 Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
POR_B	P8	VDD_SNVS_IN	GPIO	ALT0	POR_B	Input	100 kΩ pull-up
SNVS_PMIC_ON_REQ	T9	VDD_SNVS_IN	GPIO	ALT0	SNVS_PMIC_ON_REQ	Output	100 kΩ pull-up



i.MX6UL Tamper Pins Connection

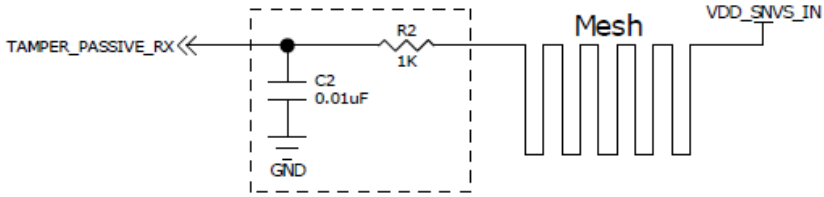
1) In system power-down mode, VDD_SNVS_IN is powered from battery.
2) When system is power-down, the only consumption current from VDD_SNVS_IN is around 20uA with Tamper detections disabled.
3) When system is power-down, the only consumption current from VDD_SNVS_IN is around 22uA - 23uA with all Passive Tamper and/or Active Tamper detections enabled.
4) When Tamper detection is enabled and tamper input pin is left floating (attack detected), it will cause 50uA – 60uA consumption current on each tamper input because they are high impedance input and are high sensitive to noises.
5) Since the Mesh traces connected to tamper input s are very long, this makes them induce high noises on the corresponding pins sensitively.
6) To reduce the consumption current when attack detected and improve the system EMC immunity, RC filters shall be added on tamper detection inputs and they shall be placed close to the corresponding tamper pins on the PCB.
7) For i.MX6UL G3 chip, all tamper pins are fused as tamper detection function, they can not be reassigned as GPIOs. For unused tamper pins, they can be just left floating.

Passive Tamper - Active High



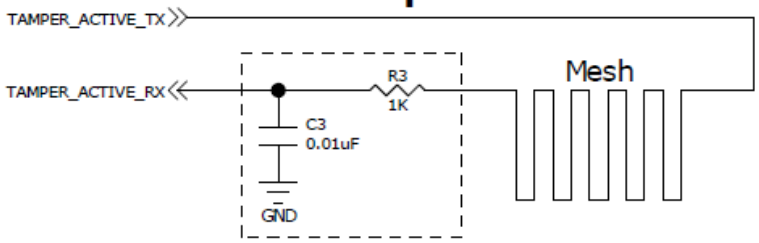
Place close to corresponding Tamper pin on PCB

Passive Tamper - Active Low



Place close to corresponding Tamper pin on PCB

Active Tamper Pair



Place close to corresponding Tamper pin on PCB

Tamper Pin Unused

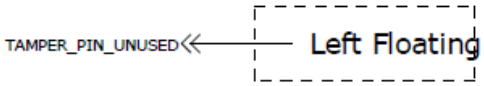


Table 15. Low Power Mode Current and Power Consumption (continued)

SNVS (RTC)	• All SOC digital logic, analog module are shut off • 32 kHz RTC is alive • Tamper detection circuit remains active	VDD_SOC_IN (0 V)	0	mA
		VDD_HIGH_IN (0 V)	0	
		VDD_SNVS_IN (3.0 V)	0.02	
		Total	0.06	mW

SECURE CONNECTIONS
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