Name	Bit	R/W	Default	Description
THERM125M	2	RW	1	Die temperature crosses 125 °C interrupt mask **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.
UNUSED	7 to 3	—	—	Unused

Table 102. Register TEMP_INT_SENSE0 - ADDR 0x22

Name	Bit	R/W	Default	Description
THERM110S	0	R	0	110 °C interrupt sense **0 —** Die temperature below 110 °C **1 —** Die temperature above 110 °C
UNUSED	1	—	—	Unused
THERM125S	2	R	0	125 °C interrupt sense **0 —** Die temperature below 125 °C **1 —** Die temperature above 125 °C
UNUSED	7 to 3	—	—	Unused

Table 103. Register ONKEY_INT_STAT0 - ADDR 0x24

Name	Bit	R/W	Default	Description
ONKEY_PUSHI	0	RW1C [1]	0	Interrupt to indicate a push of the ONKEY button. Goes high after debounce. **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared. Interrupt occurs whenever ONKEY button is pushed low for longer than the falling edge debounce setting. Interrupt also occurs whenever ONKEY button is released high for longer than the rising edge debounce setting, provided it went past the falling edge debounce time. In other words, this interrupt occurs whenever a change in status of the ONKEY_PUSHS sense bit occurs.
ONKEY_1SI	1	RW1C	0	Interrupt after ONKEY pressed for > 1 s **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared
ONKEY_2SI	2	RW1C	0	Interrupt after ONKEY pressed for > 2 s **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared
ONKEY_3SI	3	RW1C	0	Interrupt after ONKEY pressed for > 3 s **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared
ONKEY_4SI	4	RW1C	0	Interrupt after ONKEY pressed for > 4 s **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared
ONKEY_8SI	5	RW1C	0	Interrupt after ONKEY pressed for > 8 s **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared
UNUSED	7 to 6	—	—	Unused

[1] Read or Write 1 to clear the bit

Table 104. Register ONKEY_INT_MASK0 - ADDR 0x25

Name	Bit	R/W	Default	Description
ONKEY_PUSHM	0	RW	1	Interrupt mask for ONKEY_PUSH_I **0** — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1** — Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.
ONKEY_1SM	1	RW	1	Interrupt mask for ONKEY_1SI **0** — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1** — Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.
ONKEY_2SM	2	RW	1	Interrupt mask for ONKEY_2SI **0** — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1** — Mask enabled. INTB pin is NOT pulled low if corresponding interrupt status bit is set.
ONKEY_3SM	3	RW	1	Interrupt mask for ONKEY_3SI **0** — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1** — Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.
ONKEY_4SM	4	RW	1	Interrupt mask for ONKEY_4SI **0** — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1** — Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.
ONKEY_8SM	5	RW	1	Interrupt mask for ONKEY_8SI **0** — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1** — Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.
UNUSED	7 to 6	—	—	Unused

Table 105. Register ONKEY_INT_SENSE0 - ADDR 0x26

Name	Bit	R/W	Default	Description
ONKEY_PUSHS	0	R	0	Push interrupt sense **0** — ONKEY not pushed low. This bit follows debounced version of the ONKEY button being released. **1** — ONKEY pushed low. This follows the ONKEY button after the debounce circuit (debounce is programmable).
ONKEY_1SS	1	R	0	1 s interrupt sense or cleared after ONKEY button is released **0** — ONKEY not pushed low for >1 s or cleared after ONKEY button is released. **1** — ONKEY pushed and being held low > 1 s. This bit is cleared when ONKEY_PUSHS goes back to 0 when the push-button is released.
ONKEY_2SS	2	R	0	2 s interrupt sense or cleared after ONKEY button is released **0** — ONKEY not pushed low for >1 s or cleared after ONKEY button is released. **1** — ONKEY pushed and being held low > 1 s. This bit is cleared when ONKEY_PUSHS goes back to 0 when the push-button is released.

Name	Bit	R/W	Default	Description
ONKEY_3SS	3	R	0	3 s interrupt sense or cleared after ONKEY button is released **0 —** ONKEY not pushed low for >1 s or cleared after ONKEY button is released **1 —** ONKEY pushed and being held low > 1 s. This bit is cleared when ONKEY_PUSHS goes back to 0 when the push-button is released.
ONKEY_4SS	4	R	0	4 s interrupt sense or cleared after ONKEY button is released **0 —** ONKEY not pushed low for >1 s or cleared after ONKEY button is released. **1 —** ONKEY pushed and being held low > 1 s. This bit is cleared when ONKEY_PUSHS goes back to 0 when the push-button is released.
ONKEY_8SS	5	R	0	8 s interrupt sense or cleared after ONKEY button is released **0 —** ONKEY not pushed low for >1 s or cleared after ONKEY button is released. **1 —** ONKEY pushed and being held low > 1 s. This bit is cleared when ONKEY_PUSHS goes back to 0 when the push-button is released.
UNUSED	7 to 6	—	—	Unused

Table 106. Register MISC_INT_STAT0 - ADDR 0x28

Name	Bit	R/W	Default	Description
PWRUP_I	0	RW1C[1]	0	Interrupt to indicate completion of transition from STANDBY to RUN and from SLEEP to RUN **0 —** Interrupt cleared or has not occurred **1 —** Interrupt has occurred
PWRDN_I	1	RW1C	0	Interrupt to indicate completion of transition from RUN to STANDBY and from RUN to SLEEP **0 —** Interrupt cleared or has not occurred **1 —** Interrupt has occurred
PWRON_I	2	RW1C	0	Power on button event interrupt **0 —** Interrupt cleared or has not occurred **1 —** Interrupt has occurred
LOW_SYS_WARN_I	3	RW1C	0	LOW_SYS_WARN threshold crossed interrupt **0 —** Interrupt cleared or has not occurred **1 —** Interrupt has occurred
SYS_OVLO_I	4	RW1C	0	SYS_OVLO threshold crossed interrupt **0 —** Interrupt cleared or has not occurred **1 —** Interrupt has occurred
UNUSED	7 to 5	—	—	Unused

[1] Read or Write 1 to clear the bit