AH1306

Application Hints - Mini high speed CAN system basis chips UJA116x / UJA116xA

Rev. 02.01 — 18 January 2016

Info	Content
Title	**Application Hints - Mini high speed CAN system basis chips UJA116x / UJA116xA**
Authors	André Ix, Janett Habermann, Rainer Evers, Matthias Muth
Department	Systems & Applications
Keywords	HSCAN, UJA1161, UJA1161A, UJA1162, UJA1162A, UJA1163, UJA1163A, UJA1164, UJA1164A, UJA1167, UJA1167A, UJA1168, UAJ1168A, UJA1169, UJA1169L, System Basis Chip, SBC, Companion Chip, ISO11898-2, ISO11898-5, ISO11898-6, partial networking, watchdog, external sensor supply, LIMP

Abstract

The intention of this application hints document is to provide the necessary information for hardware and software designers developing automotive applications using the mini high speed CAN SBC family members (including their variants denoted by different suffixes) UJA1163, UJA1163A, UJA1164, UJA1164A, UJA1167, UJA1167A, UJA1168, UJA1168A, UJA1169 and UJA1169L. Please note, that the standard suffix “TK” is intentionally not mentioned since it describes the package variant only (TK = HVSON package).

Revision history

Rev	Date	Description
01.00	2013-04-23	Initial Version
01.01	2013-06-04	Following chapters added: - Software flow (chapter 12) - Software code examples and header files (attached) - Attached files (chapter 13.3) - Printed Circuit board design rules (chapter 13.1)
02.00	2015-09-03	Added application information for UJA1169 family variants and a power dissipation calculator
02.01	2016-01-18	Document name shortened, device names adapted to the final device production marking, typos removed, WAKE hardware picture corrected: Normal Mode activates WAK comparator

Contact information

For additional information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

Contents

1. Introduction 7
1.1 Mini high speed CAN System Basis Chips 7
1.2 Customer benefits of the mini high speed CAN SBC family 9
1.3 A-version of UJA116x family 9
2. Overview of UJA116x Family Members 10
2.1 The UJA1163(A) – Mini SBC with Standby mode w/o watchdog 10
2.1.1 Block diagram and pinning 10
2.1.2 Hardware application 12
2.2 The UJA1164(A) – Mini SBC with Standby mode 13
2.2.1 Block diagram and pinning 13
2.2.2 Hardware application 15
2.3 The UJA1167(A) – Mini SBC with Sleep mode 16
2.3.1 Block diagram and pinning 16
2.3.2 Hardware application (devices with INH pin) 18
2.4 The UJA1168(A) – Mini HS-CAN SBC for partial networking 19
2.4.1 Block diagram and pinning 19
2.4.2 Hardware application (devices with sensor supply VEXT) 21
2.5 The UJA1169 – Mini SBC with high supply current capability 22
2.5.1 Block diagram and pinning UJA1169 22
2.5.2 Hardware application UJA1169 24
2.5.3 UJA1169L Derivative – SBC Companion Chip with VIO function 25
2.5.3.1 Pinout of UJA1169L family 26
2.5.3.2 Block Diagrams of UJA1169L family 26
2.5.3.3 Typical applications of UJA1169L variants 27
2.5.3.4 Software considerations using the UJA1169L variants 28
3. Power supply 29
3.1 BAT pin 29
3.2 Transients on the battery line 30
3.3 Operation during and after cranking 30
4. Voltage regulators 32
4.1 V1 – 5V / 3V3 microcontroller supply voltage 32
4.1.1 V1 output capacitor 33
4.2 V1 – 5V / 3V3 regulator with external PNP transistor (UJA1169) 33
4.2.1 Details on the PNP concept 37
4.3 RAM retention feature 40
4.4 V2 – 5V CAN supply voltage 41
4.4.1 V2 output capacitor 42
4.5 VEXT – 5V sensor supply 43
4.5.1 VEXT output capacitor 43
4.5.2 VEXT short to BAT detection 44
4.5.3 VEXT thermal considerations 45
5. Thermal Considerations 46
5.1 Generic thermal model 46
5.2 HVSON14 Package 48
5.3 HVSON20 Package 49
5.4 Power Dissipation Calculator 50
5.4.1 Battery supply 50

5.4.2 V1 parameter ... 51
5.4.3 VEXT / V2 parameter ... 51
5.4.4 CAN Interface ... 51
5.4.5 Ambient Temperature ... 52
5.4.6 Thermal Resistance ... 52
5.4.7 Calculations ... 52
6. LIMP output (UJA1169) ... 53
6.1 Introduction ... 53
6.2 Functional description of LIMP pin ... 53
7. WAKE pin Interface (UJA1167(A) / UJA1168(A) / UJA1169) ... 56
7.1 Introduction ... 56
7.2 Hardware application ... 56
7.3 Functional description ... 56
8. Microcontroller interface ... 58
8.1 Reset interface ... 58
8.1.1 Functionality of RSTN pin ... 58
8.1.2 Configuration of the reset length ... 59
8.1.2.1 Reset length at cold start (V1 off during reset event) ... 59
8.1.2.2 Reset length at cold start for the UJA1163(A) ... 59
8.1.2.3 Reset length at warm start (V1 on during reset event) ... 59
8.1.3 RSTN input function ... 60
8.2 Wake-up and interrupt event diagnosis via pin RXD in CAN Offline ... 60
8.2.1 Overview of events ... 60
8.2.2 Event control & detection ... 62
8.2.3 Limiting microcontroller disturbance by events ... 62
8.2.4 Sleep mode protection ... 62
8.3 STBN Pin (UJA1163(A) only) ... 63
8.4 CTS Pin (UJA1163(A) only) ... 63
8.5 SPI (UJA1164(A) / 67(A) / 68(A) / 69) ... 64
8.5.1 Functionality of the SPI pins ... 64
8.5.2 Configuration of the SPI Interface ... 65
8.5.3 SPI register architecture ... 66
9. CAN transceiver interface ... 71
9.1 High speed CAN basics ... 71
9.2 Autonomous CAN voltage biasing ... 72
9.3 CAN Partial Networking ... 73
9.3.1 CAN FD passive ... 73
9.4 CAN transceiver operating voltage range ... 74
9.5 CAN transceiver operating modes ... 75
9.5.1 Active mode ... 75
9.5.1.1 CAN transmitter status check in Active mode ... 75
9.5.1.2 TXD clamping check in Active mode ... 75
9.5.2 Listen-only mode ... 76
9.5.3 Offline mode with autonomous bus biasing ... 77
9.5.3.1 Entering Sleep mode at CAN bus silence only ... 77
9.5.3.2 Standard CAN wake-up in Offline mode ... 78
9.5.3.3 Selective CAN wake-up in Offline mode ... 79
9.5.4 Off mode ... 79
9.5.5 CAN supply undervoltage detection ... 80

9.6 CAN transceiver RXD/TXD interface ... 82
9.7 CAN bus termination ... 82
9.8 CAN ESD protection ... 83
9.9 CAN Transceiver supply current ... 84
9.9.1 CAN - Average supply current during active sending, no fault ... 84
9.9.2 CAN – Frame repetition rate ... 84
9.9.3 CAN – Average current while sending, normal operation ... 85
9.9.4 CAN – Average current while sending, wake-up of system ... 85
9.9.5 CAN – Average current during bus short circuits ... 86
9.9.6 CAN – Supply Summary ... 87
10. Watchdog Interface ... 88
10.1 Watchdog overview ... 88
10.2 Watchdog software development process ... 88
10.2.1 1st step: Forced Normal mode ... 88
10.2.2 2nd step: Software Development mode ... 88
10.2.3 3rd step: Full Operation ... 89
10.3 Configuration of Watchdog mode and Period ... 90
10.4 Watchdog triggering ... 91
10.4.1 Exceptional Watchdog Behavior ... 93
10.5 Functionality of the Software Development mode ... 94
10.6 Cyclic watchdog wake-up from Sleep ... 95
10.7 Summary on watchdog settings & basic access rules ... 96
11. Non-volatile SBC configuration ... 97
11.1 Programming procedure of the MTPNV memory ... 97
11.1.1 Step 1: Check if the SBC is ready for programming the MTPNV memory ... 97
11.1.2 Step 2: Program the MTPNV memory ... 98
11.1.3 Step 3: Check whether the MTPNV programming was successful ... 99
11.2 Reset of the MTPNV memory to factory preset settings ... 99
11.2.1 Step 1: Apply external settings to reset the MTPNV memory ... 99
11.2.2 Step 2: Check whether the MTPNV reset was successful ... 100
12. Software flow ... 101
12.1 Startup Operation [STARTUP_OP] ... 103
12.1.1 Microcontroller initialization [INIT_MCU] ... 105
12.1.2 Application initialization [INIT_APPL] ... 105
12.1.3 Check device identification [CHECK_DEVICE] ... 105
12.1.4 Flash programming [FLASH] ... 105
12.1.5 Programming and checking the MTPNV [MTP_PROG] ... 106
12.1.6 Watchdog configuration [CONF_WD] ... 108
12.1.7 Reset Source Detection [RST_SOURCE] ... 110
12.1.8 Event Handling during Startup [EVENT_HANDLING] ... 111
12.1.9 Transition to Normal mode [ENTER_NORMAL1] ... 111
12.2 Normal Operation [NORMAL_OP] ... 112
12.2.1 Transition to Normal mode [ENTER_NORMAL2] ... 113
12.2.2 Trigger the Watchdog [WD_TRIGGER] ... 115
12.2.3 Transceiver Control ([TRCV_CONTROL] ... 118
12.2.4 Run Default Application [APPLICATION] ... 120
12.2.5 Event Handling [EVENT_HANDLING] ... 121
12.2.6 Transition to Low Power Operation [ENTER_LP] ... 126
12.3 Low Power Operation [LOWPOWER_OP] ... 127
12.3.1 Wake-Up Handling [WAKEUP_HANDLING] ... 128

12.3.1.1 RXD Low Handling [RXD_LOW] 129
12.3.2 Sleep Operation [SLEEP] 135
12.3.3 Standby Operation [STANDBY] 138
12.3.3.1 Stop mode / Sub Clock mode [STOP] 139
12.3.3.2 Cyclic Wake-up out of Stop mode / Sub Clock mode 141
12.4 Software Development mode 143
12.5 In-Vehicle Flash Operation [FLASH_OP] 143
12.6 UJA1168/VX/FD (A/X/F) Software Flow compared to other derivatives 147
12.6.1 UJA1167/VX (A/X) vs. UJA1168/VX/FD (A/X/F) 147
12.6.2 UJA1164(A) vs. UJA1168/VX/FD (A/X/F) 150
12.6.3 UJA1169/X/F vs. UJA1168/VX/FD (A/X/F) 150
13. Appendix 153
13.1 Printed Circuit board design rules 153
13.2 Pin FMEA 154
13.3 Associated files 173
13.4 NXPs self-supplied high speed CAN transceiver 176
13.4.1 UJA1161(A) – Self supplied high CAN transceiver with Standby mode 176
13.4.2 UJA1162(A) – Self supplied high CAN transceiver with Sleep mode 176
13.5 PCB Soldering Footprints (HVSON Packages) 177
13.5.1 UJA1163(A), UJA1164(A), UJA1167(A), UJA1168(A) derivatives (HVSON14) 177
13.5.2 UJA1169 derivatives (HVSON20) 178
13.6 Abbreviations 179
14. References 180
15. Legal information 181
15.1 Definitions 181
15.2 Disclaimers 181

1. Introduction

1.1 Mini high speed CAN System Basis Chips

The UJA1163(A), UJA1164(A), UJA1167(A), UJA1168(A), UJA1169 and their variants from NXP's family of mini High Speed CAN System Basis Chips (SBCs), offering an ISO11898-2:2003, ISO11898-5:2007 compliant high speed CAN interface and an integrated 5V or 3V3 supply for a microcontroller. The variants provide different extensions of functionality like a watchdog, an additional external sensor supply, ISO11898-6:2013 compliant selective wake-up functionality for partial networking support and many more.

Table 1. Feature overview of UJA116x high-speed CAN family and the TJA1145

Device	Modes			Supplies								Host interface				Additional features						Package		
	Normal + Standby Mode	**Sleep Mode**	**Reset Mode**	**V1:** 5V, µC only	**V1**: 5V, µC and CAN	**V1:** 3V3, µC only	**VBuf:** 5V, CAN only	**VIO:** Host interface reference	**V2:** 5V, CAN + on-board loads	**VEXT:** 5V, external loads	**INH:** High voltage output	**STBN** or **SLPN**: mode control	**SPI:** for control & diagnosis	**RSTN:** Reset pin	**CTS:** CAN Transmitter Status	**Watchdog**	**Local WAKE pin**	**LIMP pin**	**Non-volatile memory**	**CAN Partial Networking**	**CAN FD passive**	**SO14**	**HVSON14**	**HVSON20**
UJA1161 (A)	●						●	●				●			●								●	
UJA1162 (A)	●	●					●	●				●			●								●	
UJA1163 (A)	●		●		●							●		●	●								●	
UJA1164 (A)	●		●		●								●	●		●			●				●	
UJA1167 (A)	●	●	●		●						●		●	●		●			●				●	
UJA1167/VX (A/X)	●	●	●		●					●			●	●		●	●		●				●	
UJA1168 (A)	●	●	●		●						●		●	●		●	●		●	●			●	
UJA1168/VX (A/X)	●	●	●		●					●			●	●		●	●		●	●			●	
UJA1168/FD (A/F)	●	●	●		●						●		●	●		●	●		●	●	●		●	
UJA1168/VX/FD (A/X/F)	●	●	●		●					●			●	●		●	●		●	●	●		●	
UJA1169	●	●	●	●					●				●	●		●	●	●	●					●
UJA1169/X	●	●	●		●					●			●	●		●	●	●	●					●
UJA1169/F	●	●	●	●					●				●	●		●	●	●	●	●	●			●
UJA1169/X/F	●	●	●		●					●			●	●		●	●	●	●	●	●			●
UJA1169/3	●	●	●			●			●				●	●		●	●	●	●					●
UJA1169/F/3	●	●	●			●			●				●	●		●	●	●	●	●	●			●
UJA1169L	●	●		●				●	●				●			●	●	●	●					●
UJA1169L/F	●	●		●				●	●				●			●	●	●	●	●	●			●
UJA1169L/X	●	●			●			●		●			●			●	●	●	●					●
UJA1169L/X/F	●	●			●			●		●			●			●	●	●	●	●	●			●
TJA1145	●	●						●			●		●				●			●		●	●	
TJA1145/FD	●	●						●			●		●				●			●	●	●	●	

Note: The TJA1145 is a stand-alone CAN transceiver coming from the same family like the UJA116x SBCs and is based on the same silicon with different configuration.

The mini high speed CAN SBCs share a common package and pinning. Except of UJA1169 they are available in the same 14-pin HVSON package, allowing easy switching within the UJA116x variants, as well as migration from / to:

- the self-supplied transceivers UJA1161 and UJA1162 (see chapter 13.3 for more details), also available in 14-pin HVSON packages;
- the high speed CAN standalone transceivers for partial networking, called TJA1145 and TJA1145/FD also available in 14-pin HVSON packages, as well as SO packages.

The small sized mini high speed CAN SBC family is targeted for applications requiring up to 100mA microcontroller supply. The UJA1161 to UJA1168 devices are as well available with an enhanced EMC immunity performance notified with the extension “A”.

With the UJA1169 variants the supply current can be extended up to 250mA by making use of an optional external PNP transistor and a HVSON20 housing. The feature set is optimized for use e.g. in alarm systems, power seating, park distance control, rain light sensor modules, roof modules and garage opener, HVAC applications (heating, ventilation and air conditioning), trunk modules, trailer interfaces and many more. The enhanced output drive capability of the UJA1169 variants opens even more potential applications based on the scalable V1 power supply. With the UJA1169 additionally the 3V3 microcontroller supply option is added.

Furthermore there is UJA1169L variant offering a VIO level shifter input pin adapting the digital IO interface to any specific microcontroller supply voltage. This allows using the UJA1169L as a companion chip for applications with separate power supply of the microcontroller (e.g. from another SBC).

1.2 Customer benefits of the mini high speed CAN SBC family

Benefits offered by the UJA116x SBC family approach are:

- Reduced complexity, time and cost of ECU development and validation, due to the family approach of many IC variants, operating with one main software driver.
- Reduction of board space due to integration of 5V LDO, watchdog and other common components into a single, compact HVSON package.
- Greater reuse and flexibility of board layout design due to common small footprint across the majority of family members, allowing simple migration for different application requirements.
- Flexible ECU development due to eight family members with different feature sets targeting different applications and a smooth migration path towards the new partial networking standard possible within the same family.
- High speed CAN variants offer excellent EMC and ESD performance, compliant with industry standards including autonomous CAN biasing according the new standard ISO11898-6:2013 and a variant providing selective wake-up for the new industry trend towards CAN partial networking and CAN FD communication (CAN FD passive).
- Future proof supporting active CAN FD communication with up to 2Mbit/s payload.

1.3 A-version of UJA116x family

The SBC family members UJA1163, UJA1164, UJA1167 and UJA1168 are going to be releases as well in a so-called “A” version, which is covering a minor EMC related immunity upgrade, which might be relevant for a few customers only. The product functionality of the A-version is identical to the devices without “A”.

The observed immunity effect takes place, if the devices are used without CAN common mode choke only. With CAN common mode choke, all EMC related tests are pass for all derivatives. Since the immunity violation is so marginal, most OEMs have released the UJA116x family already without requesting for the A-version. Nevertheless NXP decided to optimize the family regarding that immunity observation in order to allow operation without common mode chokes as well.

It should be noted, that the UJA1169 is not affected at all by the observed effect and as such, there is no A-version.

2. Overview of UJA116x Family Members

2.1 The UJA1163(A) – Mini SBC with Standby mode w/o watchdog

2.1.1 Block diagram and pinning

The figure below shows the block diagram of the UJA1163(A).

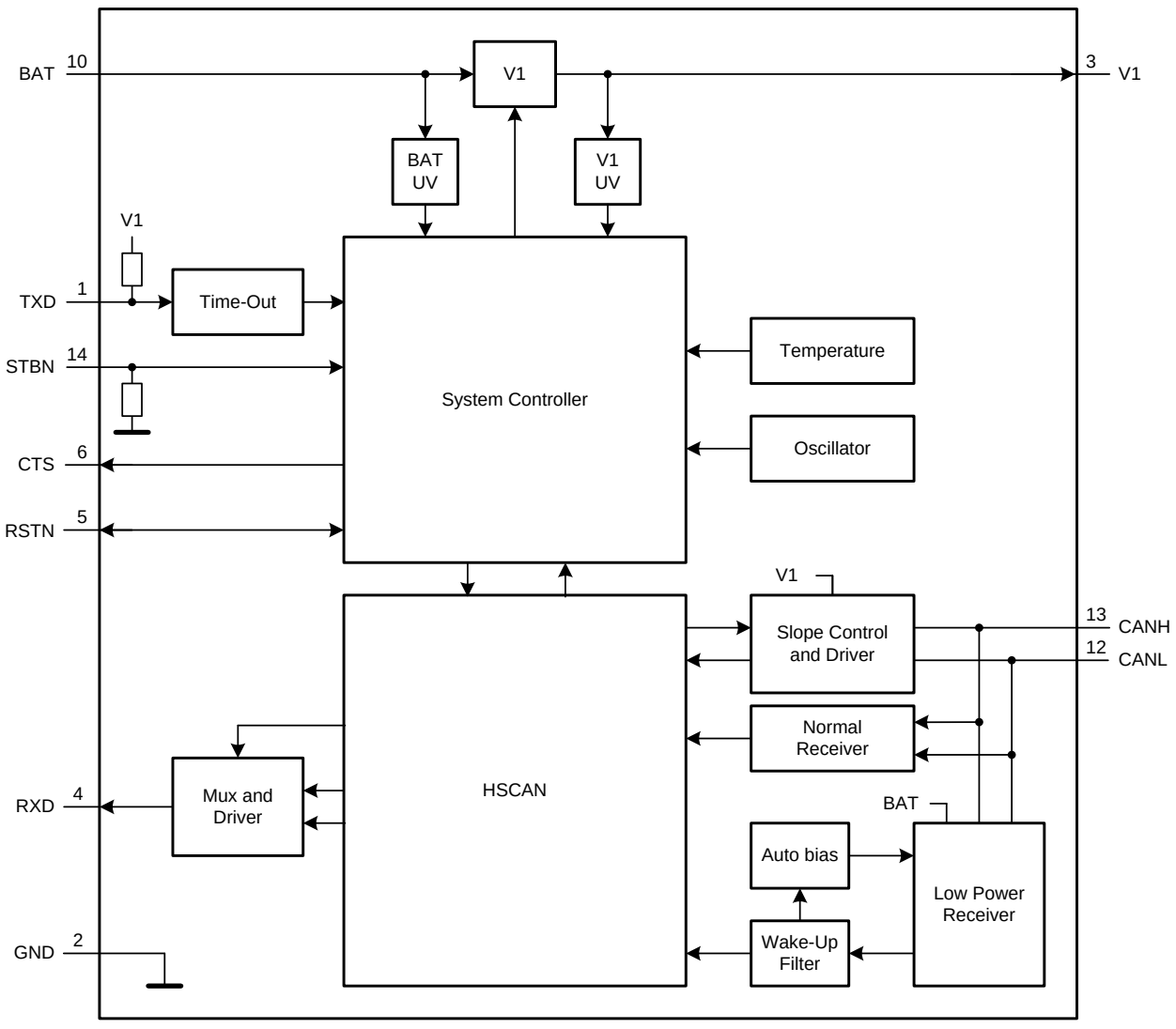


Fig 1. Block diagram of the UJA1163(A)

The UJA1163(A) includes a high-speed CAN transceiver which is fully compliant to the ISO11898-2:2003 / ISO11898-5:2007 specification and an integrated 5V/100mA supply (V1) for e.g. an application microcontroller. It can be run in Normal operation mode with full CAN communication capabilities as well as in Standby mode with very low-current, but continuous bus wake-up capabilities.

In both operation modes, the microcontroller supply V1 is enabled. With this basic feature set, the UJA1163(A) is optimized for small “Clamp-15” applications connected to the CAN bus which only needs to be active at ignition-key switched on (see connection to KL15 in Fig 3). In case the ignition- key is switched off the battery line (BAT) gets unpowered and the UJA1163(A) switches to a passive off mode, consuming no current. To save current in case the ignition-key is switched on, the Standby mode offers low current consumption at a continuous supplied microcontroller via V1. The normal CAN transceiver gets disabled. Only a low power receiver with auto biasing capability (regarding ISO11898-6:2013 / see section 9.2) keeps active.

The UJA1163(A) offers several safety measures including battery (BAT) and microcontroller supply (V1) under voltage detection, TXD dominant detection and over temperature detection. A bidirectional reset (RSTN) pin allows external system reset triggering as well as internal resets at fail conditions. In order to prevent the CAN controller from transmitting CAN frames while the SBC is still transitioning to CAN Active, a CAN Transmit Status (CTS) pin optionally reports the CAN transmitter condition back to the microcontroller. Mode control can be performed via a single mode control input pin, called STBN.

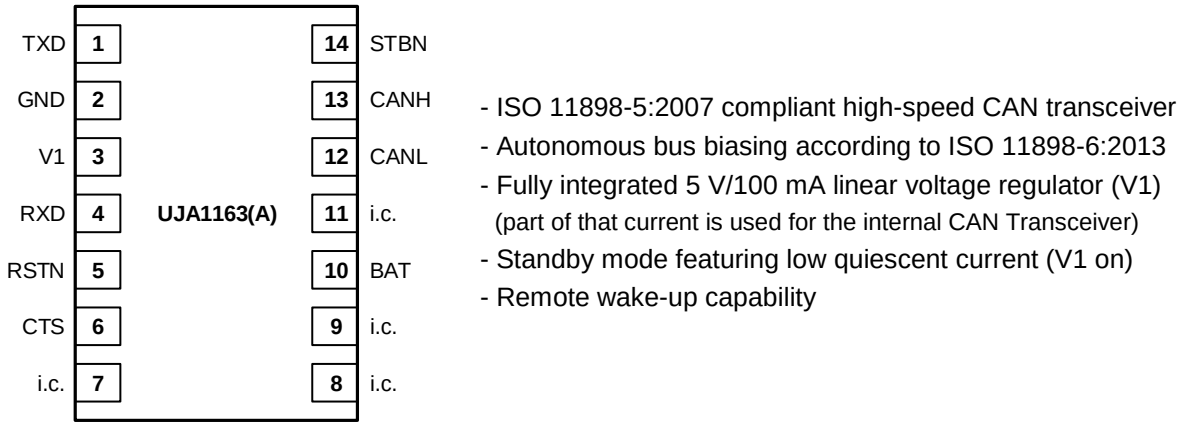
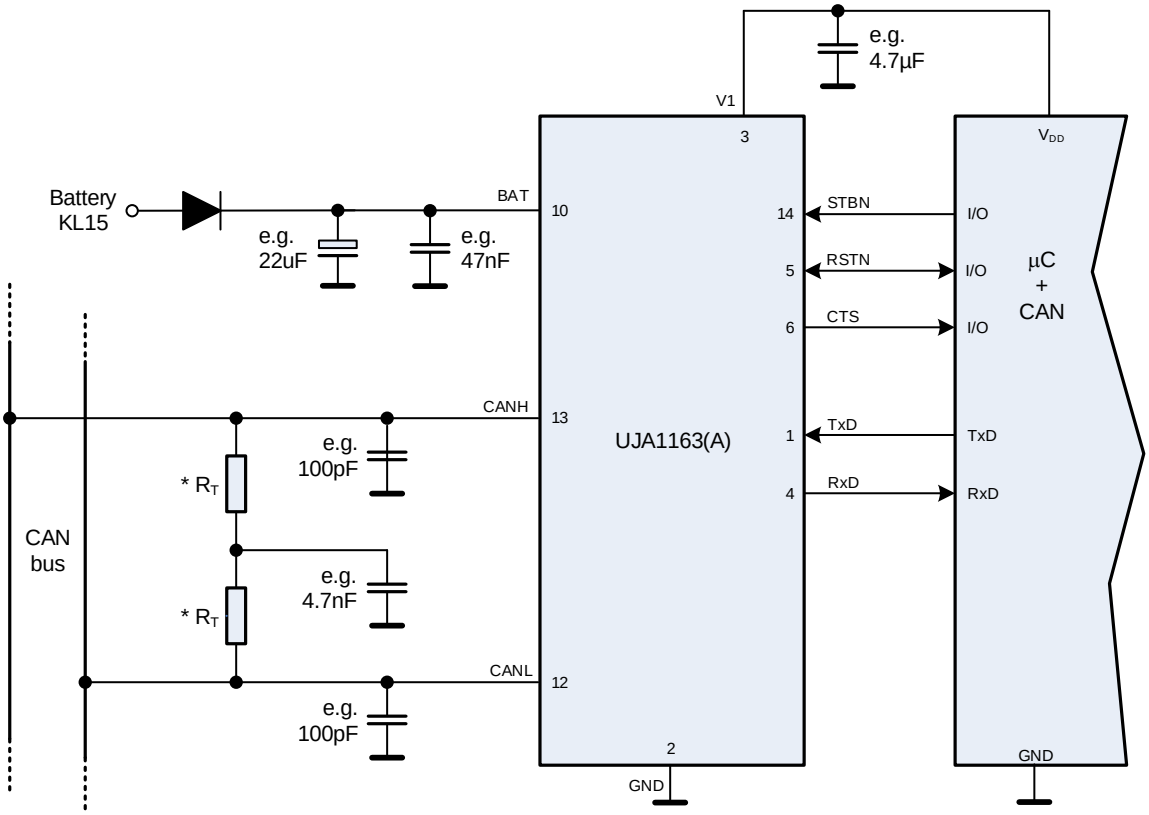


Fig 2. Pin configuration and short functional description of the UJA1163(A)

Detailed information on the UJA1163(A) control and behavior can be found in the UJA1163(A) datasheet [3].

2.1.2 Hardware application

The figure below shows the typical hardware application of the UJA1163(A).



* For bus line end nodes R_T = 60 Ω in order to support the „Split termination approach“
For stub nodes an optional „weak“ termination of e.g. R_T = 1,3 kΩ can be used, if required by the OEM.

General remark: A dedicated application may depend on specific OEM requirements.

Fig 3. Typical application of the UJA1163(A)

2.2 The UJA1164(A) – Mini SBC with Standby mode

2.2.1 Block diagram and pinning

The figure below shows the block diagram of the UJA1164(A). The highlighted blocks show the additional functionality compared to the UJA1163(A).

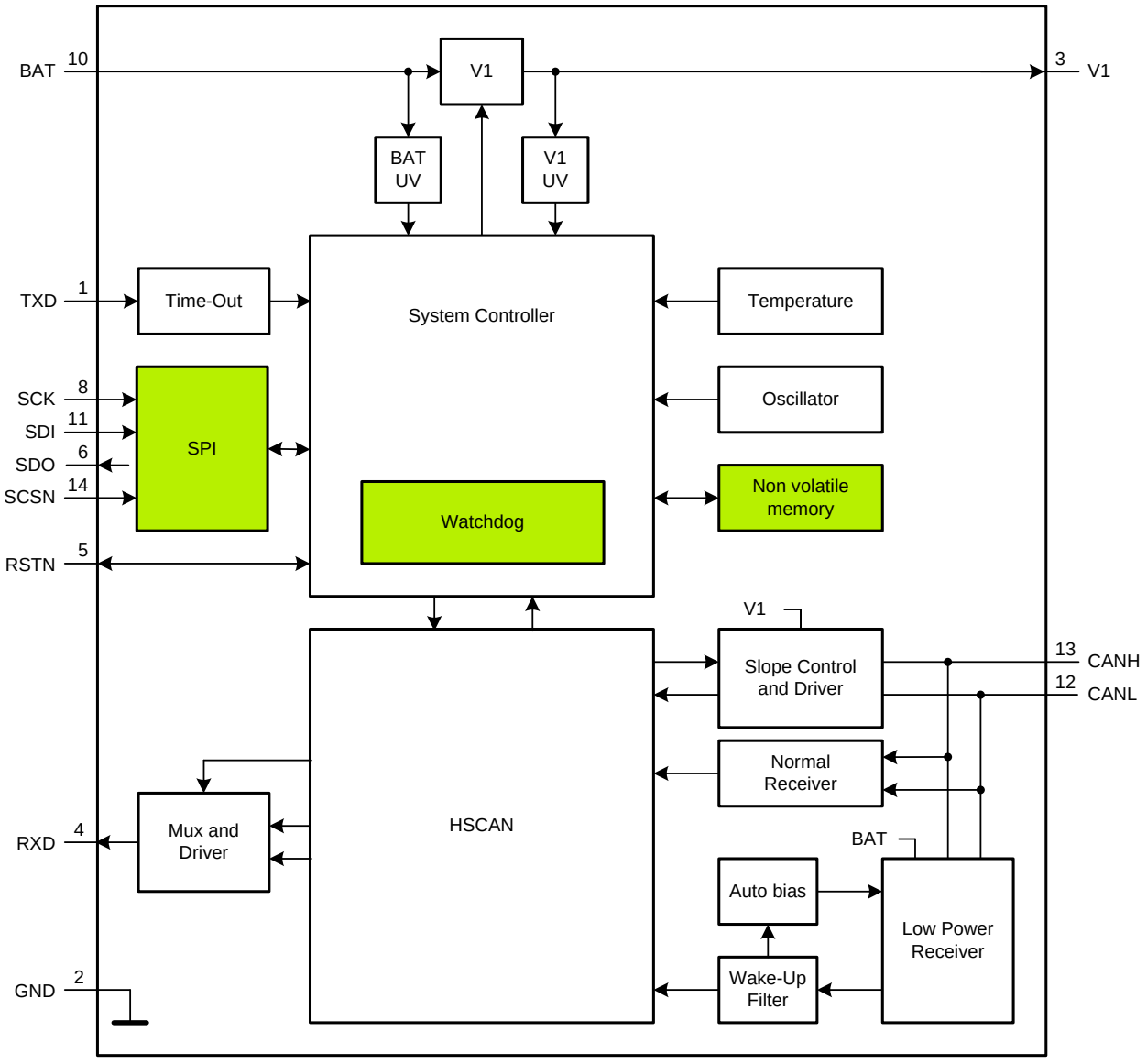


Fig 4. Block diagram of the UJA1164(A)

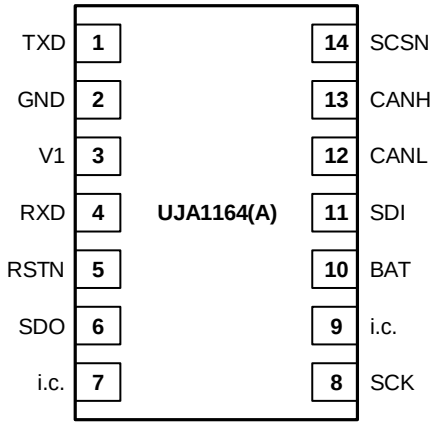
The UJA1164(A) offers an enhanced feature set compared to the UJA1163(A) mini high-speed CAN SBC. As addition to all UJA1163(A) features, it offers an SPI interface for control and diagnosis, a watchdog with independent clock source to control correct operation of the microcontroller and non-volatile memory for re-programming and storage of default power-on device settings.

Similar to the UJA1163(A), both operation modes (Normal and Standby) are offering a permanent supply for the microcontroller via pin V1. This also features the UJA1164(A) to be used within “Clamp-15” applications from power management point of view (see connection to KL15 in Fig 6).

The SPI interface enables the application to dedicatedly control the devices behavior (e.g. adapt under voltage thresholds, enable wake-up and event capturing, etc.) as well as to diagnose the applications behavior (e.g. on reset sources, wake-up events, voltage conditions, etc.).

The watchdog helps to supervise the microcontroller’s behavior via the SPI interface with different levels of security. For quick usage and remote flash programming via the CAN bus, the UJA1164(A) watchdog is disabled in factory preset (Forced Normal Mode [FNM], default at delivery). To allow easy software development, a dedicated software development mode [SDM] is offered to test the behavior of the software with respect to the watchdog setting. Finally, in the end application the watchdog can be run in so-called window, timeout or autonomous modes depending on the applications need. The timing of the watchdog can as well be adjusted via SPI settings.

Selected power-on settings of the UJA1164(A) (e.g. default reset length, default watchdog behavior, default V1 reset threshold, etc.) can be adjusted via Multiple Time Programmable (MTP) non-volatile memory cells. The settings of these cells keep saved at battery disconnection. Thus a customer specific start-up behavior of the UJA1164(A) and its application can be adjusted through the MTP. Mode control is performed via the SPI interface.



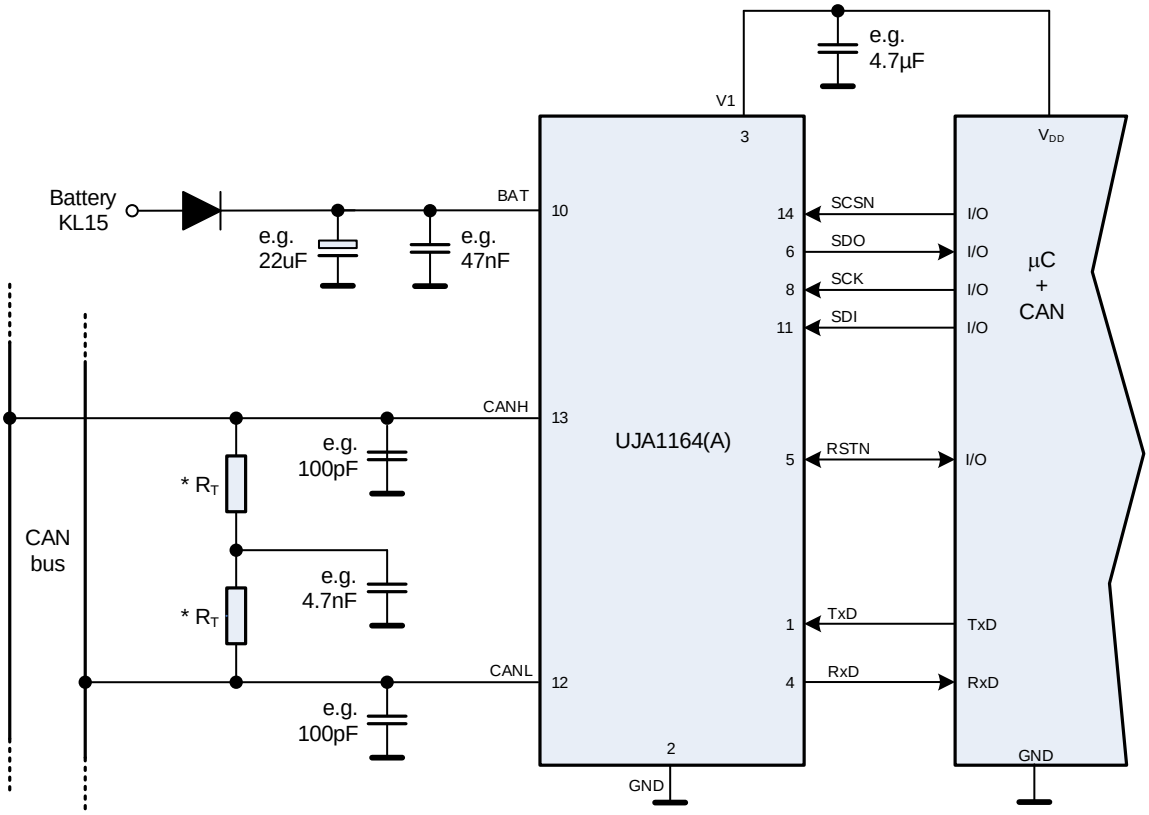
- ISO 11898-5:2007 compliant high-speed CAN transceiver
- Autonomous bus biasing according to ISO 11898-6
- Fully integrated 5 V/100 mA linear voltage regulator (V1)
  (part of that current is used for the internal CAN Transceiver)
- Standby mode featuring low quiescent current (V1 on)
- Remote wake-up capability
- Mode control via the Serial Peripheral Interface (SPI)
- Watchdog with independent clock source
- Configuration of selected functions via non-volatile memory

Fig 5. Pin configuration and short functional description of the UJA1164(A)

Detailed information on the UJA1164(A) control and behavior can be found in the UJA1164(A) datasheet [4].

2.2.2 Hardware application

The figure below shows an example hardware application of the UJA1164(A).



* For bus line end nodes R_T = 60 Ω in order to support the „Split termination approach“
For stub nodes an optional „weak“ termination of e.g. R_T = 1,3 kΩ can be used, if required by the OEM.

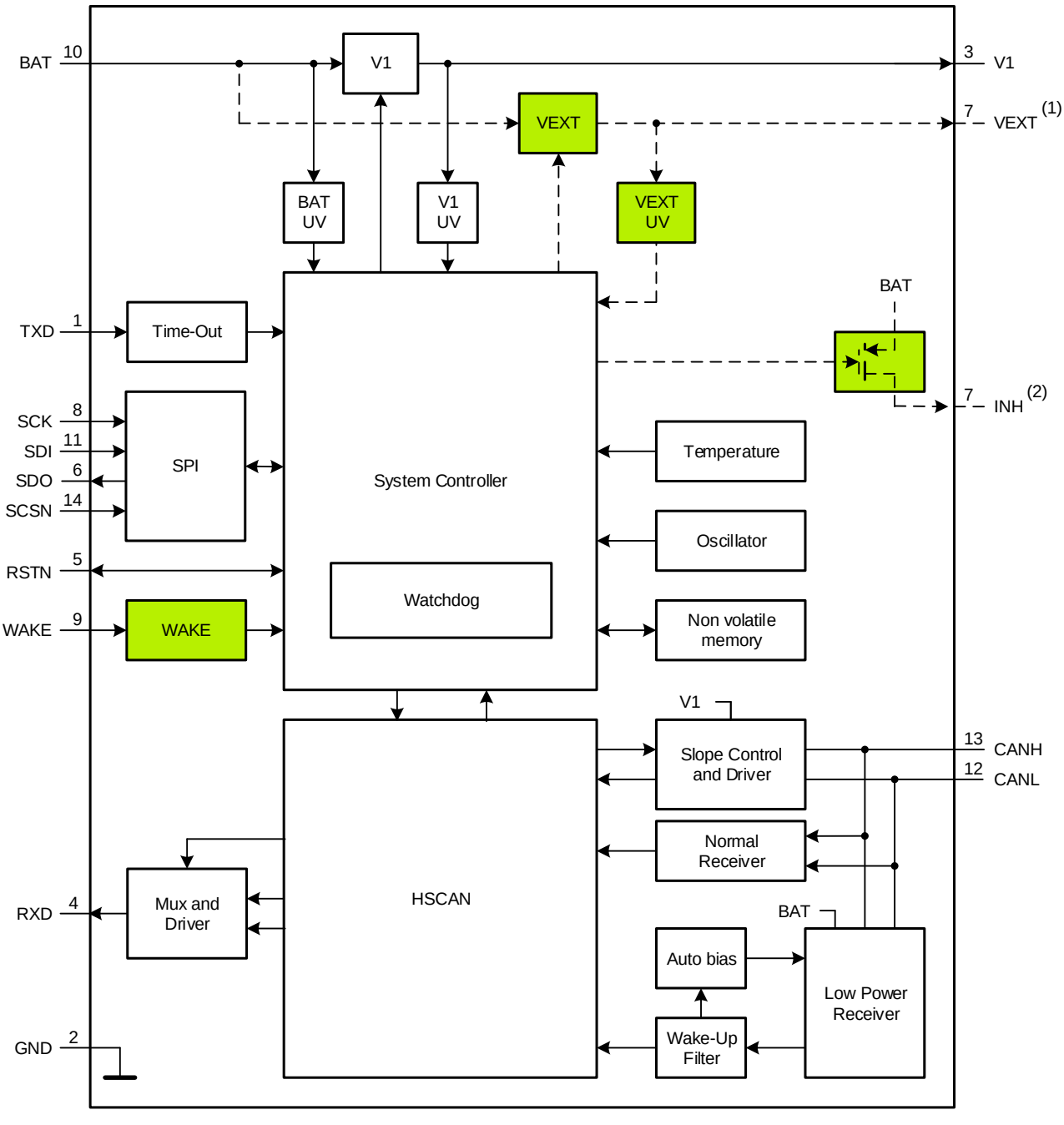
General remark: A dedicated application may depend on specific OEM requirements.

Fig 6. Typical application of the UJA1164(A)

2.3 The UJA1167(A) – Mini SBC with Sleep mode

2.3.1 Block diagram and pinning

The figure below shows the block diagram of the UJA1167(A) variants. The highlighted blocks show the additional functionality compared to the UJA1164(A).



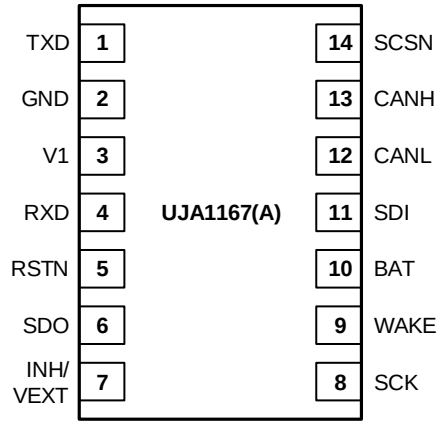
(1) Only present in UJA1167/VX (A/X)
(2) Only present in UJA1167(A)

Fig 7. Block diagram of the UJA1167(A)

The UJA1167(A) offers a further enhanced feature set compared to the UJA1164(A). As an additional low-power mode, the UJA1167(A) offers the Sleep mode function. Within Sleep mode, V1 gets disabled switching off the microcontroller's power supply in order to further save current of the application by keeping the wake-up capability of the UJA1167(A) alive. With this feature the UJA1167(A) can perfectly be used within "Clamp-30" applications which are continuously connected with the cars battery line (see connection to KL30 in Fig 9).

For that reason the UJA1167(A) offers an additional wake-up input via pin WAKE in order to allow activation of the UJA1167(A) and its application via a local ECU wake-up condition without global CAN bus activation. The pin WAKE can be configured to be sensitive on falling and/or rising edges and might be additionally polled via software control through SPI.

The UJA1167(A) is available in two functional versions. The UJA1167(A) variant offers a BAT voltage level related INH output pin for power control of additional ECU components like voltage regulators. The UJA1167/VX (A/X) variant offers an additional 5V/30mA fully protected (-18V … +40V) regulator e.g. for an external off-board sensor.



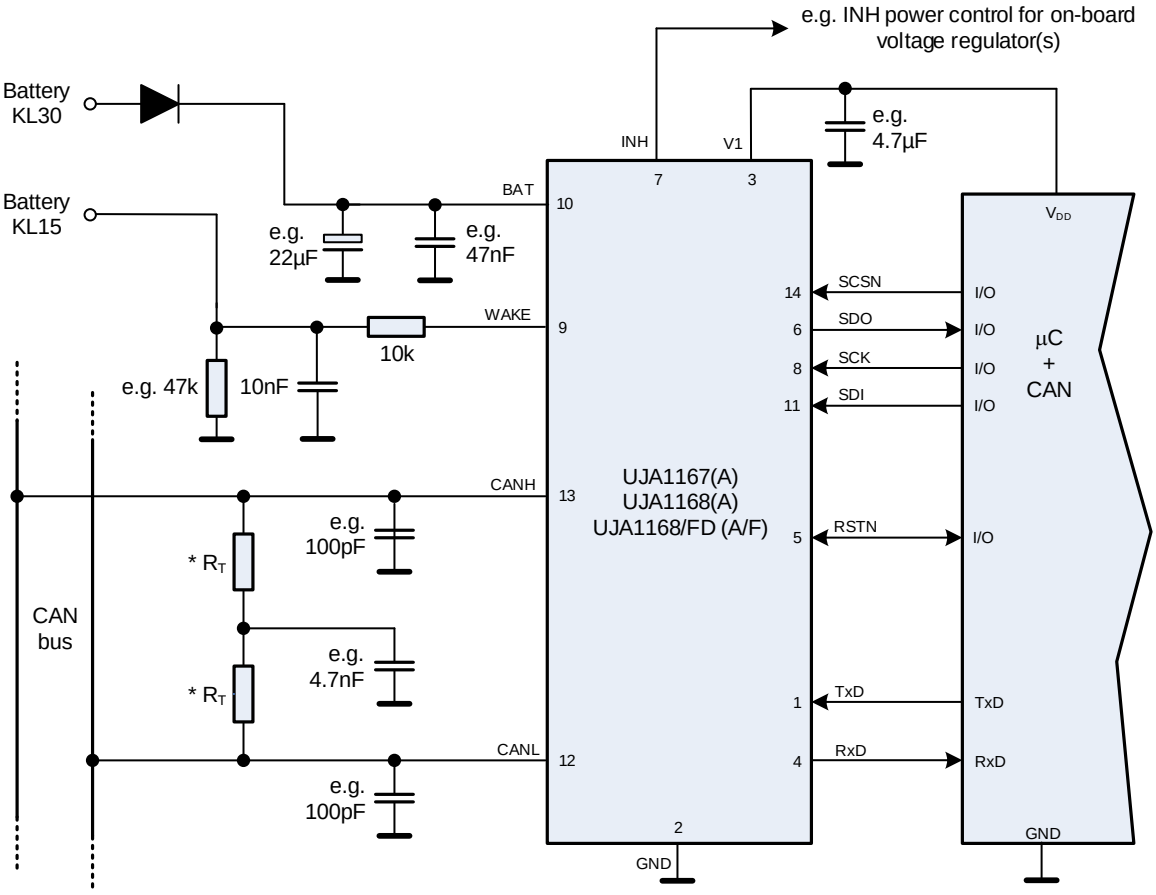
- ISO 11898-5:2007 compliant high-speed CAN transceiver
- Autonomous bus biasing according to ISO 11898-6:2013
- Fully integrated 5 V/100 mA linear voltage regulator (V1)
  (part of that current is used for the internal CAN Transceiver)
- Standby & Sleep (V1 off) mode featuring low quiescent current
- Remote and local wake-up capability
- Optional INH output for controlling an external voltage regulator
- Optional 5V sensor supply voltage regulator, fully protected
- Mode control via the Serial Peripheral Interface (SPI)
- Watchdog with independent clock source
- Configuration of selected functions via non-volatile memory

Fig 8. Pin configuration and short functional description of the UJA1167(A)

Detailed information on the UJA1167(A) control and behavior can be found in the UJA1167(A) datasheet [5].

2.3.2 Hardware application (devices with INH pin)

The figure below shows an example hardware application of the UJA1167(A), UJA1168(A) or UJA1168/FD (A/F).



* For bus line end nodes R_T = 60 Ω in order to support the „Split termination approach“
For stub nodes an optional „weak“ termination of e.g. R_T = 1.3 kΩ can be used, if required by the OEM.

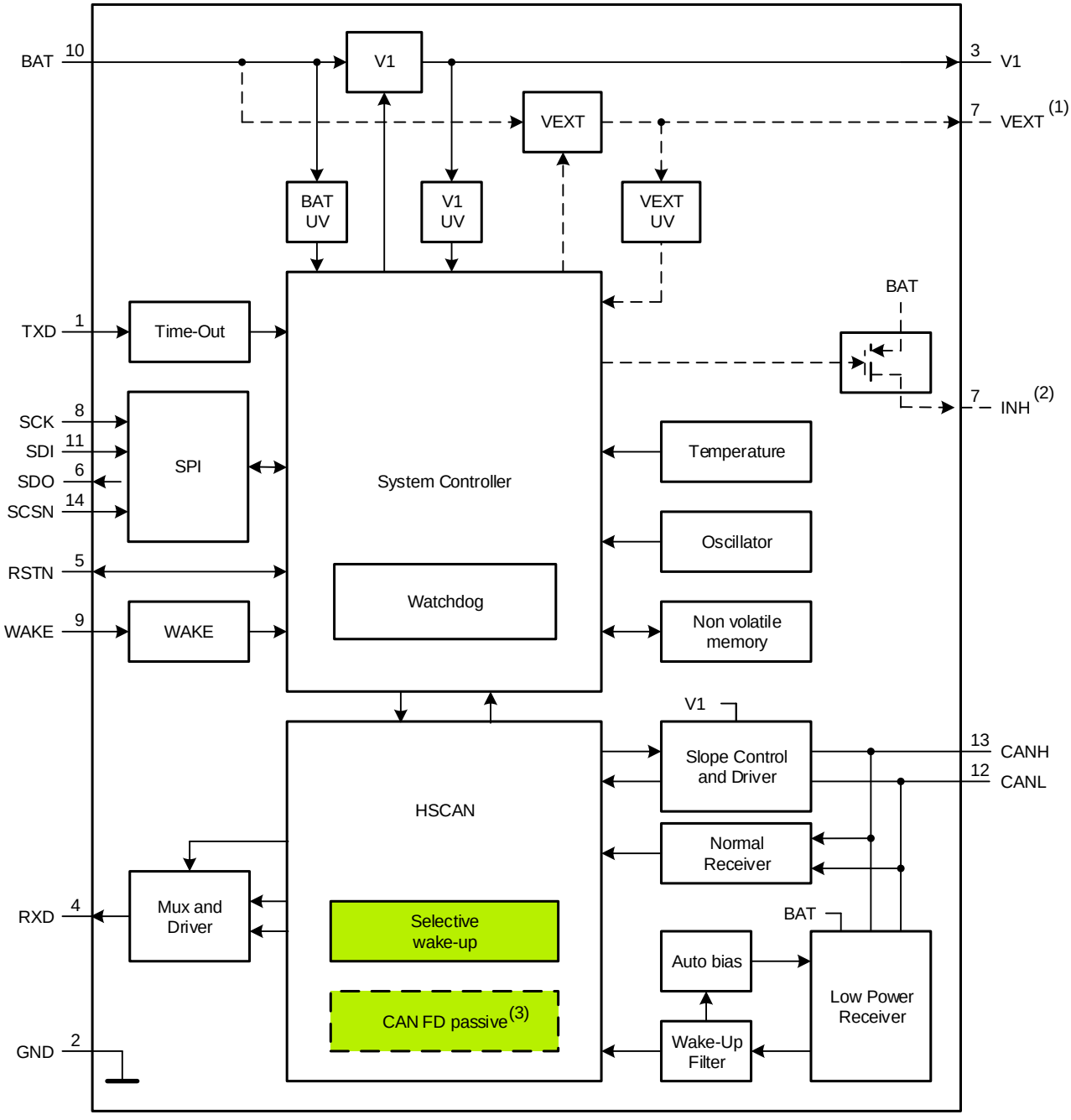
General remark: A dedicated application may depend on specific OEM requirements.

Fig 9. Typical application with the UJA1167(A), UJA1168(A) or UJA1168/FD (A/F) ; all with INH pin

2.4 The UJA1168(A) – Mini HS-CAN SBC for partial networking

2.4.1 Block diagram and pinning

The figure below shows the block diagram of the UJA1168(A) variants. The highlighted blocks show the additional functionality compared to the UJA1167(A).



(1) Only present in UJA1168/VX (A/X) and UJA1168/FD/VX (A/F/X)
(2) Only present in UJA1168(A) and UJA1168/FD (A/F)
(3) Only present in UJA1168/FD (A/F) and UJA1168/FD/VX (A/F/X)

Fig 10. Block diagram of the UJA1168(A)

The UJA1168(A) provides the same features as the UJA1167(A), but with the addition of full ISO11898-6:2013 compliant CAN selective wake-up capability supporting partial networking (see section 9.3) and the option of CAN FD passive behavior (see section 9.3.1).

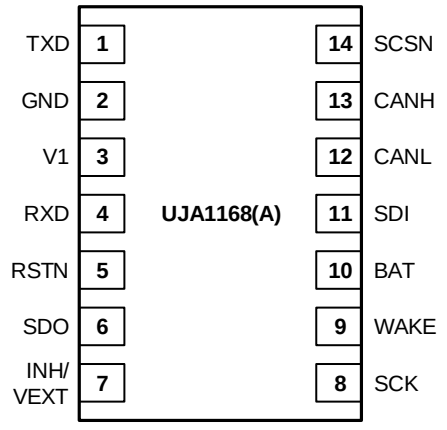
Similar to the UJA1167(A), the UJA1168(A) is supporting “Clamp-30” applications (Sleep mode) with the addition that it optionally only wakes-up by bus traffic based on dedicated pre-defined wake-up frames sent by other nodes on the bus (selective wake-up). With this partial networking capability, the ECU up-time and current consumption can be squeezed to a minimum for applications which only need to be available temporarily.

In high-speed CAN networks which implement CAN FD for fast data transmission, the UJA1168(A) offers as add on two versions that can be set to CAN FD passive mode. This feature, when used in combination with partial networking, is an enabler for hybrid networks in which only part of the network nodes require CAN FD operation, allowing the other nodes to use classic high speed CAN on the same network. This is achieved by placing the non-CAN FD nodes into Standby or Sleep mode with selective wake-up and the CAN FD passive feature active. This causes the UJA1168(A) to not wake-up by CAN FD frames including a higher speed data field and without generating bus errors. Based on that function, ECUs without CAN FD protocol engine embedded can be temporarily disabled while the rest of the nodes within the same network can make use of CAN FD communication. This is very powerful for e.g. vehicle flashing of ECUs with CAN FD capability and speed.

The UJA1168(A) comes in four functional versions, all with CAN Partial Networking support:

- UJA1168(A) (with INH pin / not CAN FD passive)
- UJA1168/VX (A/X) (with VEXT pin / not CAN FD passive)
- UJA1168/FD (A/F) (with INH pin / CAN FD passive)
- UJA1168/VX/FD (A/X/F) (with VEXT pin / CAN FD passive)

All selective wake-up and CAN FD settings are handled via the UJA1168(A)’s SPI interface.



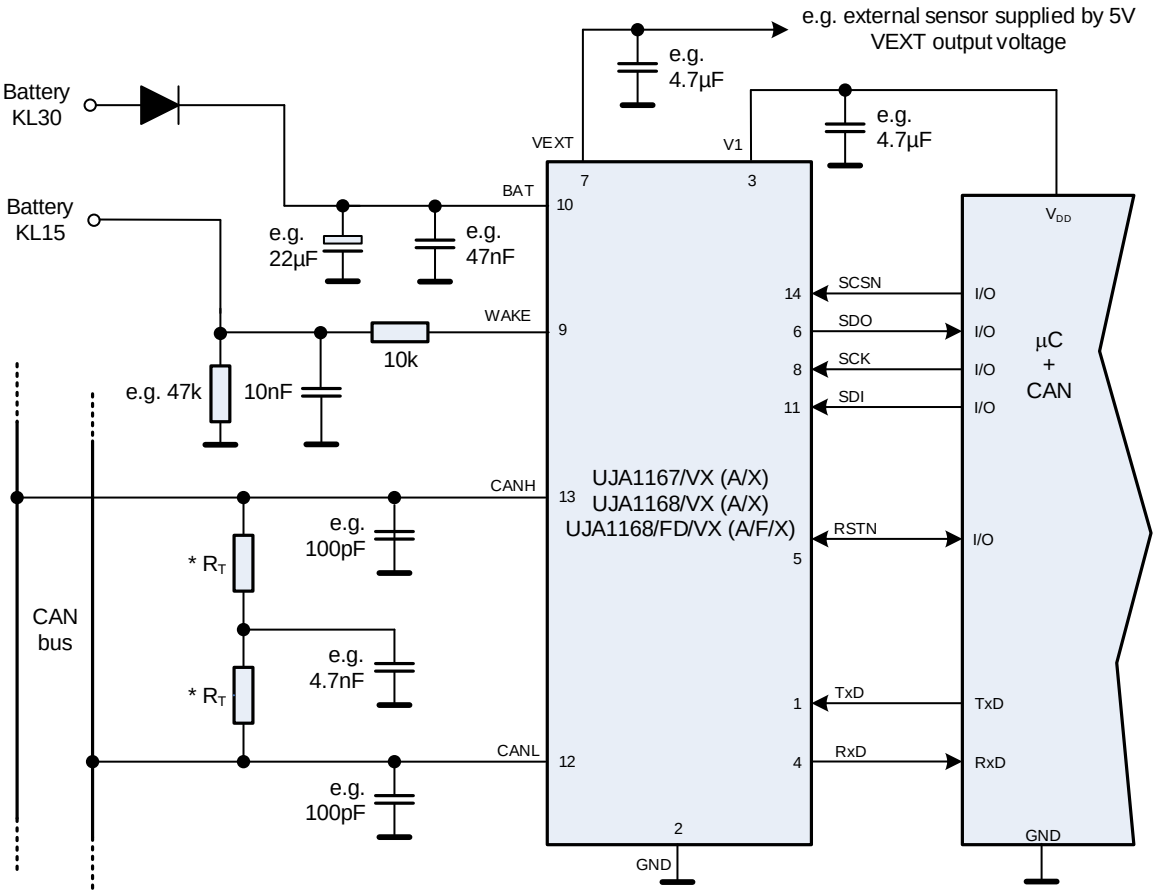
- ISO 11898-6:2013 compliant HSCAN for Partial Networking
- Autonomous bus biasing according to ISO 11898-6:2013
- Fully integrated 5 V/100 mA linear voltage regulator (V1)
  (part of that current is used for the internal CAN Transceiver)
- Standby & Sleep (V1 off) mode featuring low quiescent current
- Remote and local wake-up capability
- Optional INH output for controlling an external voltage regulator
- Optional 5V sensor supply voltage regulator, fully protected
- Mode control via the Serial Peripheral Interface (SPI)
- Watchdog with independent clock source
- Configuration of selected functions via non-volatile memory
- CAN FD passive variant

Fig 11. Pin configuration and short functional description of the UJA1168(A)

Detailed information on the UJA1168(A) control and behavior can be found in the UJA1168(A) datasheet [6].

2.4.2 Hardware application (devices with sensor supply VEXT)

The figure below shows an example hardware application of the UJA1167/VX (A/X), the UJA1168/VX (A/X) or the UJA1168/VX/FD (A/X/F) (all offering the VEXT sensor supply pin).



* For bus line end nodes R_T = 60 Ω in order to support the „Split termination approach“
For stub nodes an optional „weak“ termination of e.g. R_T = 1.3 kΩ can be used, if required by the OEM.

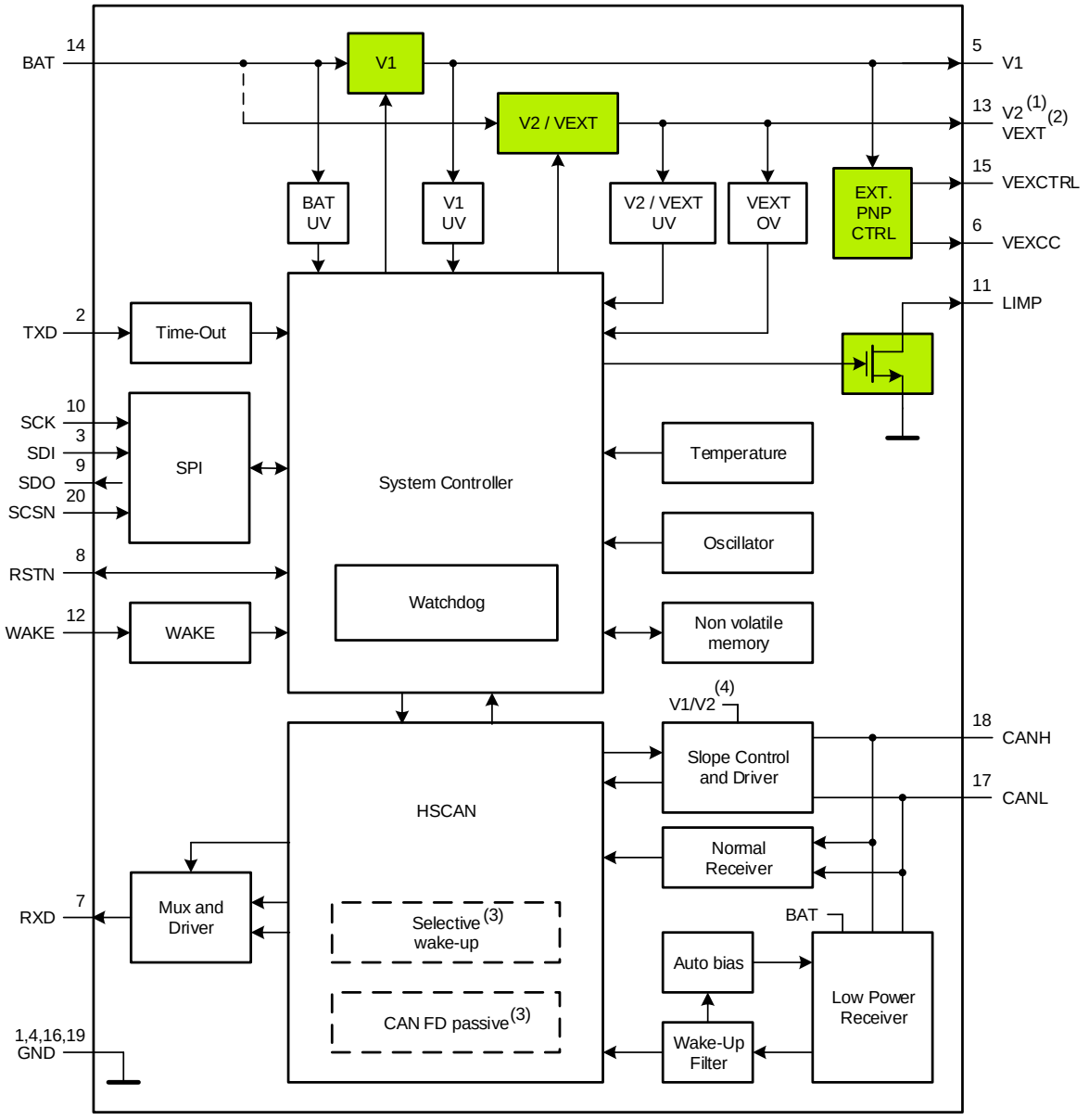
General remark: A dedicated application may depend on specific OEM requirements.

Fig 12. Typical application with the UJA1167/VX (A/X), UJA1168/VX (A/X) or UJA1168/VX/FD (A/X/F) ; all with sensor supply VEXT

2.5 The UJA1169 – Mini SBC with high supply current capability

2.5.1 Block diagram and pinning UJA1169

The figure below shows the block diagram of the UJA1169 variants. The highlighted blocks show the additional functionality compared to the UJA1168(A).



(1) Only present in UJA1169, UJA1169/F, UJA1169/3 and UJA1169/F/3
(2) Only present in UJA1169/X and UJA1169/X/F
(3) Only present in UJA1169/F UJA1169/X/F and UJA1169/F/3
(4) HS-CAN transceiver is supplied from V1 in UJA1169/X and UJA1169/X/F and from V2 in UJA1169, UJA1169/F, UJA1169/3 and UJA1169/F/3

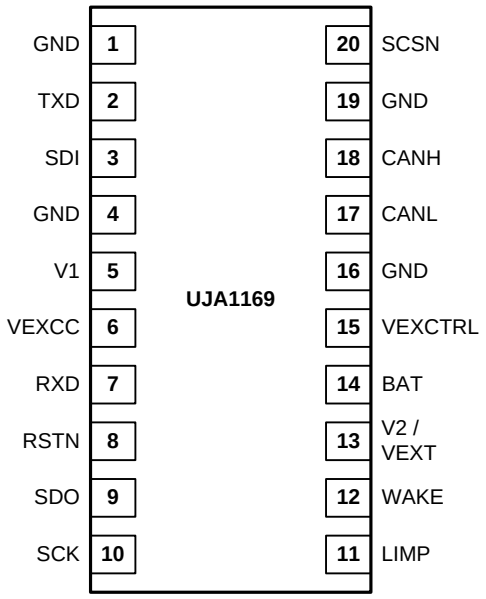
Fig 13. Block diagram of UJA1169

As base line the UJA1169 has a similar feature set like the UJA1168/VX/FD (A/X/F), but with the capability to drive higher supply currents. In comparison to the UJA1168(A) the

UJA1169 supports supply currents of up to 250 mA on V1 and up to 100 mA on V2 or VEXT. The extended V1 current drive capability with up to 250mA can be achieved with an external PNP transistor. The transistor is used to outsource some power dissipation from the UJA1169 package in order to better distribute thermal heat on the ECU. An additional option is the output voltage on V1, which can be either 5V or 3V3 depending on the selected variant.

Depending on the selected derivative the internal CAN Transceiver is connected to V1 (variants with sensor supply VEXT) or V2 (variants without sensor supply VEXT). Consequently parts of the above mentioned current drive capabilities are reserved for the internal CAN Transceiver. Due to the very low CAN short circuit current feature of the embedded CAN Transceiver, this current is always significantly lower than 55mA.

Furthermore the UJA1169 provides a LIMP output, which indicates system failures in combination with the embedded watchdog and temperature monitoring.



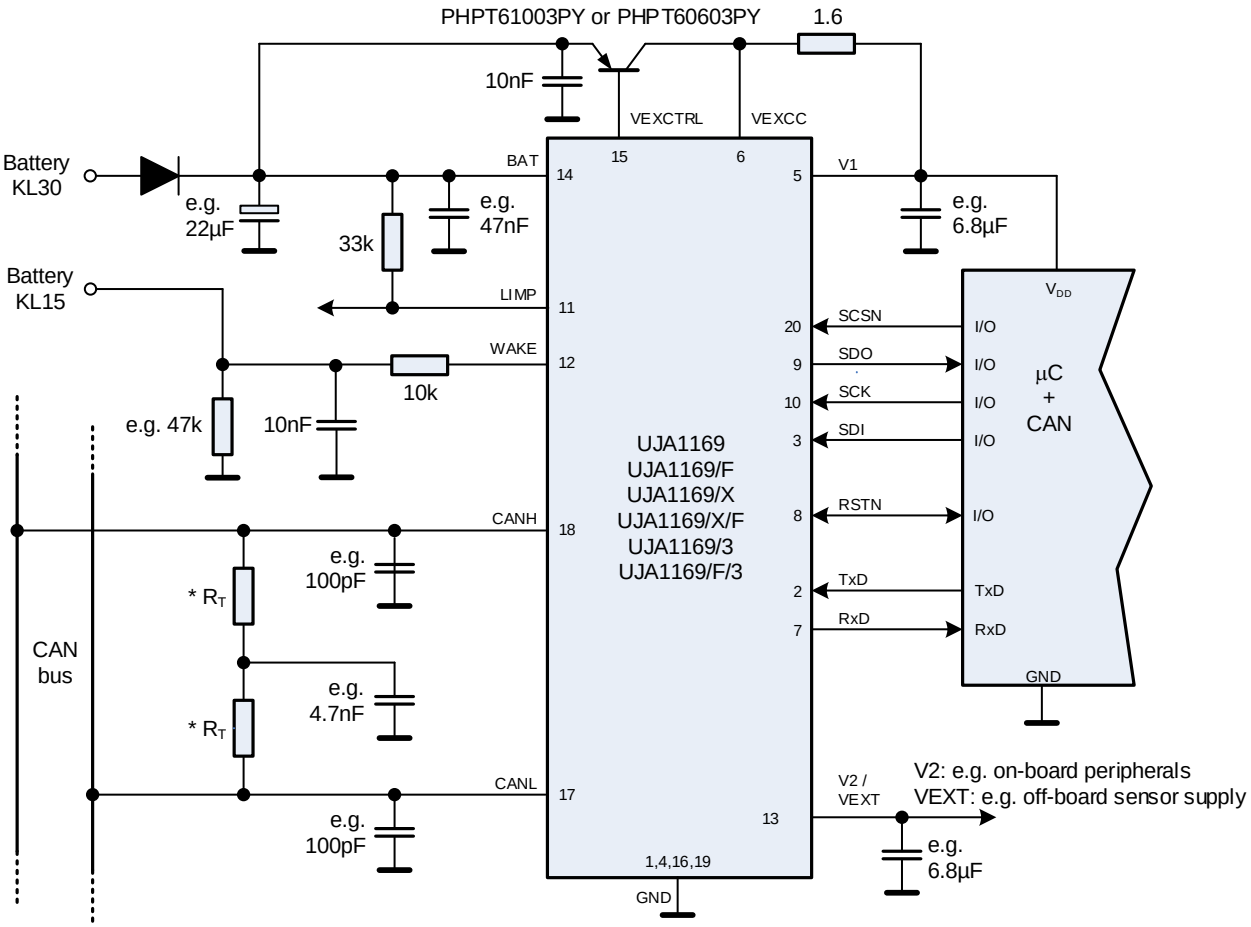
- ISO 11898-6:2013 compliant HS-CAN with Partial Networking including FD passive feature (FD variants)
- CAN FD active communication up to 2 Mbit/s
- Autonomous bus biasing according to ISO 11898-6:2013
- Fully integrated 5V or 3V3 LDO regulator (V1) for up to 250 mA (depending on derivative, some current used by internal CAN)
- Enhanced thermal distribution with external PNP transistor
- Second integrated 5V LDO regulator (V2) for up to 100 mA (depending on derivative, some current used by internal CAN)
- Optional protected 5V sensor supply variant (VEXT)
- Standby & Sleep mode with very low supply current
- Remote and local wake-up capability
- LIMP output to signal system failures
- Mode control via the Serial Peripheral Interface (SPI)
- Watchdog with independent on-chip clock source
- Configuration of selected power-up functions via non-volatile memory

Fig 14. Pin configuration and short functional description of the UJA1169

Detailed information on the UJA1169 control and behavior can be found in the UJA1169 data sheet [10].

2.5.2 Hardware application UJA1169

The figure below shows an example hardware application of the UJA1169.



* For bus line end nodes R_T = 60 Ω in order to support the „Split termination approach“
For stub nodes an optional „weak“ termination of e.g. R_T = 1.3 kΩ can be used, if required by the OEM.

General remark: A dedicated application may depend on specific OEM requirements.

Fig 15. Typical application of the UJA1169

2.5.3 UJA1169L Derivative – SBC Companion Chip with VIO function

Besides the standard UJA1169 family members, there is a dedicated bond out variant, which can be used as companion chip for applications with another SBC dedicated to the application microcontroller.

The special functionality of the UJA1169L family members is dealing with the problem that a host SBC is supplying the application microcontroller and with that, providing the under-voltage reset function and the ECU wide interface voltage of the microcontroller. This can be a 5V based system or even a 3V3 based system. For applications, which require more transceiver resources or more power supply resources it is not easily possible adding a secondary SBC to that host controller, because that secondary SBC has a different interface supply domain. In case, both SBCs would share the same voltage (5V or 3V3) in theory it would be possible to simply combine both control interfaces with the host microcontroller, but there is a high risk of reverse supplying one of the 2 SBCs at power-up or power-down ramps because it cannot be guaranteed, that both SBC supplies are ramping up and down exactly synchronously. In case both SBCs are making use of different supply systems (5V <-> 3V3), there would be always a severe cross current between these two supply domains.

This problem is solved with the UJA1169L by a dedicated VIO pin of the SBC. Through this VIO pin the “Companion” SBC UJA1169L can be adapted to any other supply domain through the VIO pin. Since the companion SBC is not mastering the RSTN of the host controller, the RSTN pin function is replaced with a dedicated VIO pin function.

Based on this companion SBC any application can easily be extended with further resources like power supply, CAN transceiver, Sensor supply or even a secondary independent Watchdog function with independent LIMP output for special ASIL related applications.

The UJA1169L makes use of the same silicon like the UJA1169 standard family and distinguishes only through a different bonding. The VIO pin function within the standard UJA1169 is internally bonded to the V1 supply of the SBC and now separated in the UJA1169L.

Following derivatives of the UJA1169L are available, all with 5V output voltage on V1:

- UJA1169L V2 for integrated CAN
- UJA1169L/F V2 for integrated CAN, Partial Networking
- UJA1169L/X V1 for integrated CAN, Sensor supply VEXT
- UJA1169L/X/F V1 for integrated CAN, Sensor supply VEXT, Partial Netw.

2.5.3.1 Pinout of UJA1169L family

The main difference in the pinout is dealing with the replacement of the RSTN pin with the VIO pin function. Since all UJA1169 derivatives are coming from the same silicon, there are some constraints for the location of the VIO pin function. In order to not violate internal bonding rules, the pins RXD and VEXCC have to be moved downwards in the package as shown in Fig 16.

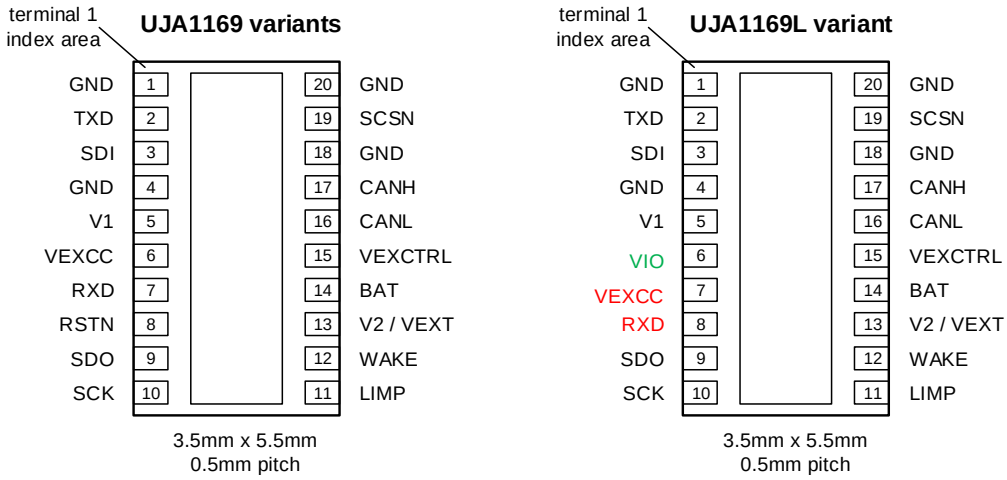


Fig 16. Pin out of the UJA1169L variants compared to the standard versions

2.5.3.2 Block Diagrams of UJA1169L family

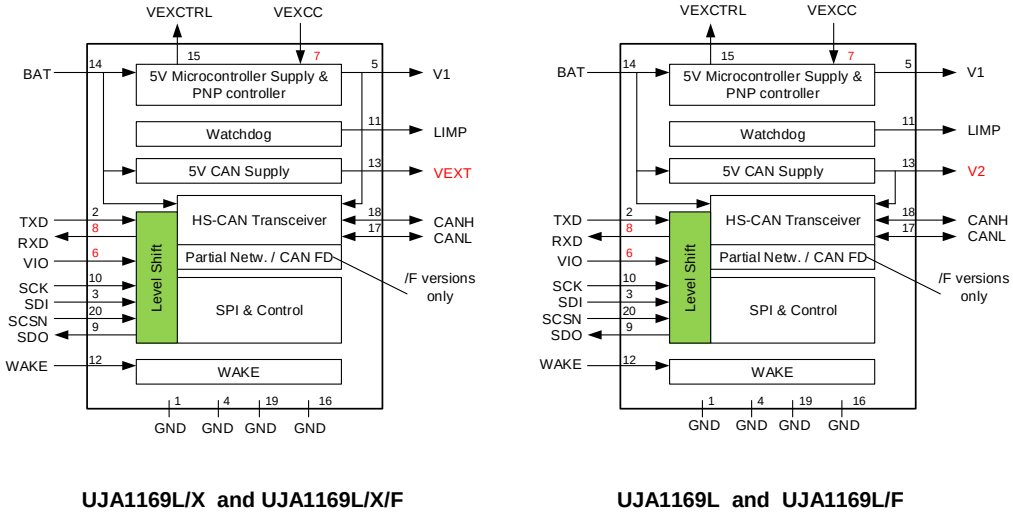


Fig 17. UJA1169L family members

2.5.3.3 Typical applications of UJA1169L variants

In Fig 18 a typical application of the UJA1169L is shown. Within this example, a Gateway application based on the UJA113x SBC is proposed (here the 3V3 variant), which is extended with the UJA1169L/X/F version allowing to supply a row of CAN transceivers as well as a FlexRay transceiver from the 5V rail. The VIO pin allows adaptation of the UJA1169L to the interface voltage of the host microcontroller.

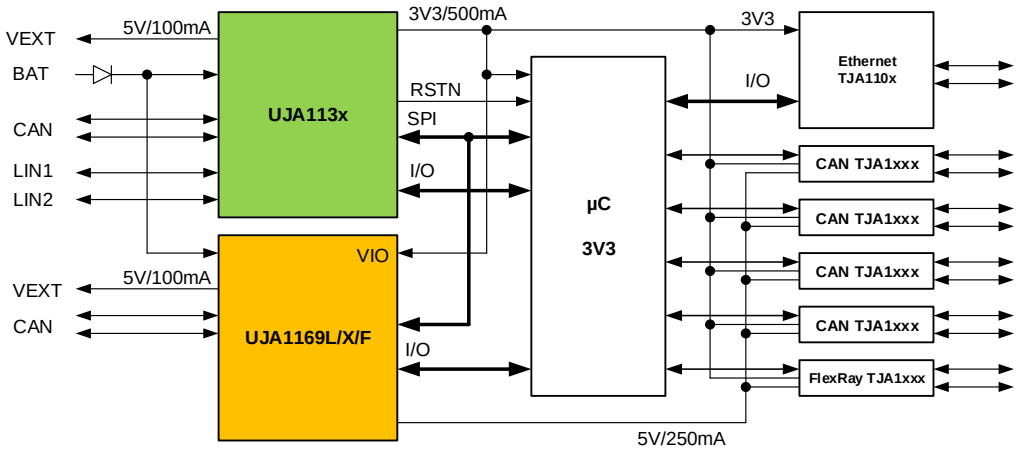


Fig 18. Simplified Application Diagram UJA1169L, Standby Application

The shown architecture makes use of the Standby Mode for low-power operation, keeping the regulators active all time while the transceivers are shut down in order to reduce the Q-current of the application.

In case the Sleep Mode of the UJA1169L shall be used (regulators all off), a small application hardware is required to wake-up the UJA1169L out of sleep mode again.

Background is the fact, that the SPI interface of the UJA1169L is completely disabled during Sleep Mode and with that, it is not possible to activate the UJA1169L through SPI even if VIO is already present and supplied. For such applications a simple RET (Resistor Equipped Transistor) can be applied, which is controlled through the host controller as shown in Fig 19.

Similar applications are possible combining the UJA1169L with any other system basis chip like the complete UJA116x family.

Based on the UJA1169L systems can be scaled easily with more Transceivers including the necessary 5V supply domain.

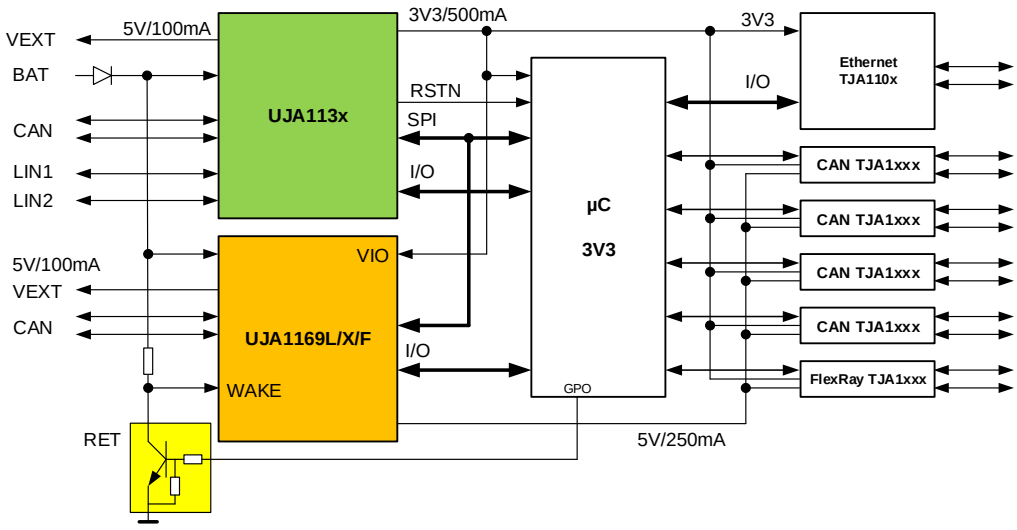


Fig 19. Simplified Application Diagram UJA1169L, Sleep Application

2.5.3.4 Software considerations using the UJA1169L variants

Since the UJA1169L does not offer a dedicated RSTN output pin there is no automatic synchronization of the application software with the still available integrated Watchdog circuit. In case the WD and LIMP function are not required for the application, the UJA1169L can be used in Software Development Mode all time. With that, there is no impact on the application and the WD can be ignored. The LIMP pin may still be used as a general purpose output pin, if desired.

In case a secondary Watchdog is of interest and/or the LIMP pin function shall be used as an independent safety feature, the UJA1169L may be used without Software Development Mode and the application can trigger the WD normally. The big advantage of such a system is, that the application now gets a secondary completely independent LIMP hardware compared to the main SBC.

In case the main SBC would get severely damaged and does not operate properly anymore, this might have an impact on the LIMP function of that SBC as well. With the UJA1169L companion chip in the same application, there is now a second Watchdog and LIMP function available, which can take-over the system LIMP function. From ASIL perspective, this might be an interesting option for some safety critical applications.

3. Power supply

3.1 BAT pin

The BAT pin is the supply pin of UJA116x family. The BAT specification is “gap free” starting from 0 V up to 28 V. This is illustrated in Fig 20. The maximum operating voltage is 40V. In the supply range between 28 V and 40 V general functionality is still available, but not all parameters are within the specified limits like e.g. quiescent currents, and because of the higher power dissipation and the thermal consequences (mainly by the regulators V1 and V2/VEXT) such high supply voltage should not be applied for a longer time than the duration of a “load dump” condition (max 400 ms) in order to avoid over-temperature shut-down of the SBC. In particular, the V1 and V2/VEXT regulators, CAN, µC interface, digital control, watchdog and V1 undervoltage monitor work properly up to 40 V.

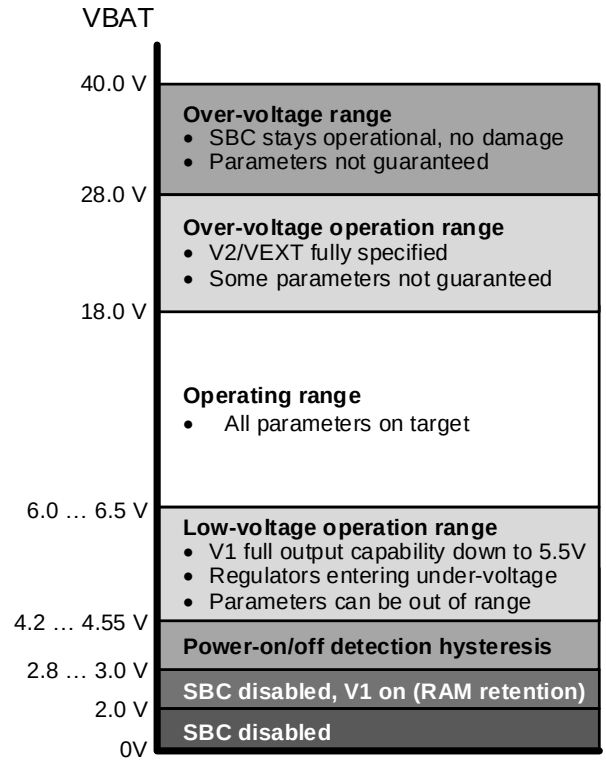


Fig 20. Supply “Gap Free” operation

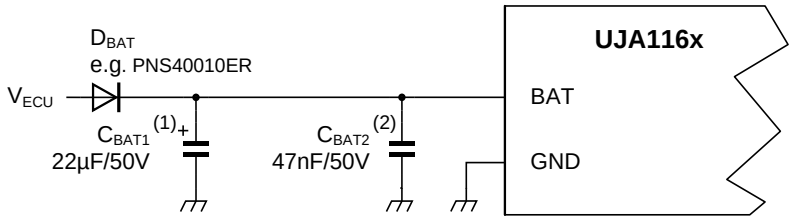
The main electrical parameters with respect to the BAT pin are the power-on and -off detection thresholds. If the UJA116x is disabled (BAT ramping up from 0V), it remains disabled as long as the BAT voltage is below 4.2 V to 4.55 V ($V_{th(det)pon}$). Once being above that voltage it will stay active until the BAT voltage falls below 2.8 V to 3.0 V ($V_{th(det)poff}$).

At each power-on event of the UJA116x a dedicated event bit is set to indicate the power-on event to the software. The indication is done by the power-on event status bit PO, which can be found in the system event status register. This allows application software detecting e.g. “first module connection” events or very deep cranking events, which might require a dedicated module handling like system calibration.

3.2 Transients on the battery line

A basic requirement for automotive ECUs is that they need to be capable of sustaining automotive transients as, for example, defined in ISO 7637.

Fig 21 shows the recommended circuitry on pin BAT. First of all a reverse polarity protection diode D_{BAT} is required, because the UJA116x family does not provide internal reverse polarity protection. Such external reverse polarity protection diode D_{BAT} (e.g. PNS40010ER [11] or PMEG6010ER [12] or PMEG10020AELR) protects the ECU (including the UJA116x) against negative automotive transients, such as specified in ISO 7637. In addition D_{BAT} protects the ECU against transients, which can be caused by charge equalization between ECUs during hot-plugging.



(1) C_{BAT1} value is exemplary. On principle the value depends on application.

(2) C_{BAT2} value is a typical value. Typically it is an open mode ceramic capacitor or two capacitors in series.

Fig 21. Typical circuitry on pin BAT

The buffer capacitors C_{BAT1} and C_{BAT2} in Fig 21 should be applied on pin BAT to suppress spikes, noise and automotive transients. Further they are used to buffer supply voltage dropping. For reduction of high-frequency noise the small capacitor C_{BAT2} should be located close to the BAT pin of the UJA116x.

Note, that so-called “Open-mode” capacitors are recommended on BAT inputs of ECUs in general. Alternatively two capacitors in series can be used, which are mounted with 90 deg. turn relative to each other on the PCB preventing mechanical shorts on BAT during bending of PCBs. Non “open mode” capacitors might tend to an internal hard short circuit after/during mechanical stress, which can be mitigated with 2 capacitors in series and 90deg. turn.

3.3 Operation during and after cranking

During and after engine start (cranking) the battery supply voltage can drop. Such battery supply starting profiles are specified in older versions of the specification ISO 7637 and in the specification ISO 16750-2. Typical starting profiles consist of an initial voltage drop to a very low voltage level U_S for 70 ms, followed by a slightly higher level U_A for several seconds.

The following measures can be done to achieve operation without microcontroller reset during deep cranking:

- Use of reverse polarity protection diodes with low forward voltage, e.g. Schottky barrier diodes: PMEG6010ER [12] or PMEG10020AELR

- Use a low V1 under-voltage detection voltage V_{uvd}, e.g. 60% (5V variants only; note that the detection threshold can be defined as well in the non-volatile memory of the UJA116x family and would be available as default for the device after power-on)
- Choose a capacitance value for the battery supply buffer capacitor C_{BAT1} that bridges the initial voltage drop of the starting profile.

4. Voltage regulators

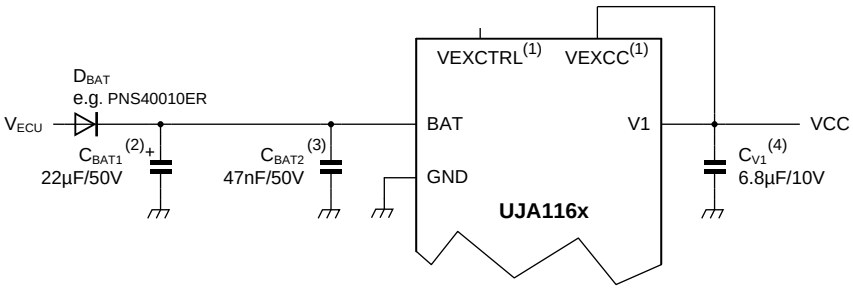
4.1 V1 – 5V / 3V3 microcontroller supply voltage

The V1 voltage regulator is intended to supply the application microcontroller, the internal CAN transceiver (except of UJA1169, UJA1169/F, UJA1169/3, UJA1169/F/3, UJA1169L and UJA1169L/F) and potential other on-board hardware. The V1 regulator output voltage is 5 V or 3.3V depending on the ordered variant and delivers depending on the type number either up to 150 mA or 250 mA. In Table 2 the V1 regulator variants of the UJA116x SBC family are listed.

Table 2. V1 versions of UJA116x SBC family

Type number	V1 voltage	CAN supply	MIN output current before current limitation kicks in
UJA1163 (A) UJA1164 (A) UJA1167 (A) UJA1167/VX (A/X) UJA1168 (A) UJA1168/VX (A/X) UJA1168/FD (A/F) UJA1168/VX/FD (A/X/F)	5V	CAN transceiver internally connected to V1	150 mA *Note: Part of that current is used by the internal CAN transceiver.*
UJA1169/X UJA1169/X/F UJA1169L/X UJA1169L/X/F	5V	CAN transceiver internally connected to V1	250 mA *Note: Part of that current is used by the internal CAN transceiver.*
UJA1169 UJA1169/F UJA1169L UJA1169L/F	5V	CAN transceiver internally connected to V2	250 mA
UJA1169/3 UJA1169/F/3	3V3	CAN transceiver internally connected to V2	250 mA

In Fig 22 the typical V1 output circuitry is illustrated. For the UJA1169 variants if no external PNP is required, VEXCTRL shall be left open and VEXCC must be connected to V1. In addition a V1 output capacitor C_{V1} is required. The requirements for C_{V1} are given in section 4.1.1.



(1) UJA1169 family only.

(2) C_{BAT1} value is exemplary. On principle the value depends on application.

(3) C_{BAT2} value is a typical value. Typically it is an open mode ceramic capacitor or two capacitors in series.

(4) C_{V1} value is a typical value to buffer load changes.

Fig 22. Typical V1 application

4.1.1 V1 output capacitor

The value of the V1 output capacitor C_{V1} depends on the requirements for line and load regulation. The V1 regulator is stable with a large range of capacitor values. Table 3 lists the recommended minimum capacitor value to be applied to the V1 output.

Table 3. V1 output capacitor

Effective minimum capacitance	Recommended minimum nominal capacitor value	Typical nominal capacitor value
1.76 µF with 5 V DC offset	4.7 µF	6.8 µF

The effective capacitance of a capacitor depends heavily on temperature and the DC charge voltage (DC offset). In order to cope with these effects it is recommended to use 6.8µF nominal capacitors. With that there should be enough margin for temperature and DC offset impact on the effective capacitance. For details please refer to the data sheet of the selected capacitor.

For small effective capacitor values the MIN ESR of the capacitor shall be at least 50mΩ. The UJA1169 allows to go for even lower ESR values down to 0mΩ as a result of the updated higher current capability of up to 250mA. Bigger capacitances in general allow lower ESR values. In general the MAX ESR shall not exceed 2Ω. The higher the ESR value, the bigger a potential output voltage impact is on steep load current changes.

4.2 V1 – 5V / 3V3 regulator with external PNP transistor (UJA1169)

The V1 voltage regulator of the UJA1169 can deliver up to 250 mA even without external PNP transistor. To prevent overheating of the device in case of high ambient temperature or high average currents or BAT supply voltages, it is possible to connect an external PNP transistor (e.g. PHPT61003PY or PHPT60603PY) as shown in Fig 23. In this configuration the power dissipation of the V1 voltage regulator is distributed between the UJA1169 and the external PNP transistor. The PNP transistor will be switched on, when the load current is above the selected PNP activation threshold current $I_{th(act)PNP}$ and the BAT supply voltage is above the PNP activation threshold voltage $V_{th(act)PNP}$. The main regulation loop stays fully within the UJA1169 device handling all dynamic load changes locally inside the

package while the external PNP just delivers some average supply current to the application. With that, the regulation loop stays always stable independently of the physical location of the PNP and the detailed characteristic of that PNP.

In Fig 23 the shunt resistor R_{SHUNT} between V1 and VEXCC is required for measuring the current of the transistor. It is used to limit the current delivered by the external PNP transistor and to protect the PNP transistor against V1 short-circuit to ground. In case the VEXCC to V1 voltage reaches the current limiting activation threshold voltage $V_{th(act)Ilim}$ the PNP current is not increased anymore. For calculating the R_{SHUNT} value, the resistor voltage drop caused by the PNP current $V_{th(act)Ilim}$, the minimum V1 input sink current I_{IN}, the ambient temperature and the thermal characteristics of the transistor (e.g. thermal resistance from junction to solder point) and the PCB have to be considered.

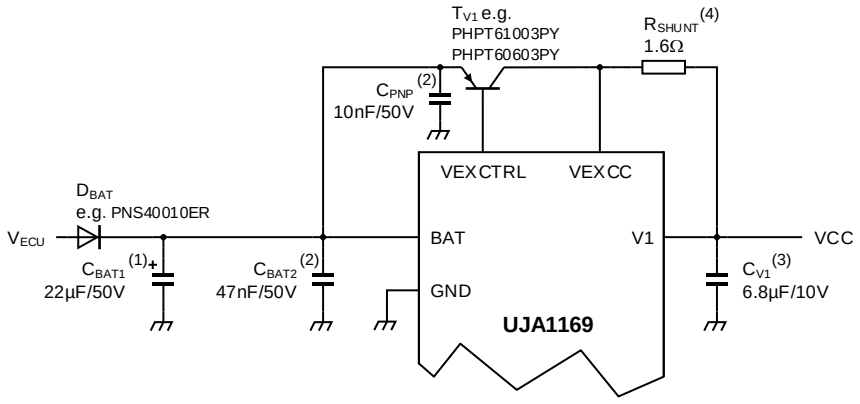
On one hand the maximum PNP collector current $I_{C(PNP)max}$ shall not exceed the minimum V1 input sink current I_{sink}. On the other hand the maximum application current through the PNP $I_{C(PNP)app}$ should be supported. Based on these requirements the minimum value for R_{SHUNT} can be calculated as follows:

$$R_{SHUNT,min} = \frac{V_{th(act)Ilim,max}}{I_{sink,min}} = \frac{330mV}{214mA} = 1.54\ \Omega$$

With that minimum shunt resistance it is guaranteed, that the external PNP current never exceeds the maximum V1 regulator current sink capability. Application use case behind is a situation, where the application current is on the maximum level and suddenly drops to zero current (e.g. entering a low power mode of the application or a sudden load loss). In that moment, the PNP might carry the full 214mA while no load is connected anymore. Since the PNP cannot be closed within zero time, the internal sink path of the UJA1169 takes over that current until the PNP is off.

Optionally it is possible so go beyond such boundary with loading the PNP (or multiple PNPs) with more current than 214mA, but in that case there is some application risk for sudden load current interruptions (dynamic changes higher than 250mA, 214mA in the PNP + 46mA internally of V1), which cannot be managed anymore with the internal sink path. One potential solution might be a bigger buffer capacitor avoiding a voltage overshoot on V1 at sudden load loss until the PNP is regulated down. Anyway such design needs to be balanced carefully avoiding unwanted side effects.

Due to PNP constraints (e.g. maximum total PNP power dissipation and thermal characteristics) the minimum R_{SHUNT} value might also be higher and dominated by the PNP transistor instead of the UJA1169.



(1) C_{BAT1} value is exemplary. On principle the value depends on application.

(2) C_{BAT2} and C_{PNP} value are typical values. Typically they are open mode ceramic capacitors or two capacitors in series. C_{PNP} shall be placed close to the emitter of the PNP

(3) C_{V1} value is a typical value to buffer load changes.

(4) R_{SHUNT} value is a typical value (minimum R_{SHUNT} value is 1.5 Ω).
(NXP PNP proposals: PHPT63003PY or PHPT61003PY)

Fig 23. Typical V1 application with external PNP transistor (UJA1169)

The maximum value of R_{SHUNT} depends on the maximum V1 application current $I_{O(app),max}$ and the used minimum PNP activation threshold current $I_{th(act)PNP,min}$, which is set with the power distribution control bit PDC:

$$R_{SHUNT,max} = \frac{V_{th(act)Ilim,min}}{I_{O(app),max} - I_{th(act)PNP,min}} \geq R_{SHUNT,min}$$

If the calculated $R_{SHUNT,max}$ is smaller than $R_{SHUNT,min}$, then the $R_{SHUNT,min}$ overrules $R_{SHUNT,max}$. Basically, a R_{SHUNT} value higher than $R_{SHUNT,max}$ can be chosen. As a result just the PNP portion on the V1 application current is limited and less current is outsourced to the PNP.

Example: The maximum average V1 application current $I_{O(app),max}$ is 200 mA and the PDC bit is reset to 0:

$$R_{SHUNT,max} = \frac{V_{th(act)Ilim,min}}{I_{O(app),max} - I_{th(act)PNP,min}} = \frac{240\ mV}{200\ mA - 60\ mA} = 1.71\ \Omega \geq R_{SHUNT,min} = 1.54\ \Omega$$

Thus for above example a resistor value of R_{SHUNT} = 1.6 Ω (1%) could be chosen. Note: A higher R_{SHUNT} value might be required, because of PNP constraints.

As long as the DC current gain h_{FE} (also named β) is in the range from 50 to 500 any PNP can be used. For product validation the transistor type PHPT61003PY (NXP Semiconductors) was used.

One advantage of this scalable voltage regulator concept is that there are no specific PCB layout restrictions for using the external PNP. The distance between the UJA1169 and the

external PNP has no negative impact on the stability of the regulator loop because the loop is realized within the UJA1169. Hence, there is no influence of signal resonances. For a better thermal distribution on the PCB it is even recommended to increase the distance between the UJA1169 and PNP. Only PCB layout constraint is coming from the C_{PNP} (10nF) which need to be placed close to the Emitter of the external PNP for EMI optimization.

The requirements on the V1 output capacitor C_{V1} are the same as described in section 4.1.1, if an external PNP transistor is used.

For adjusting the power distribution between the SBC and the PNP, the UJA1169 provides the power distribution control bit (PDC), which is located in the regulator control register. The UJA1169 has two PNP activation threshold currents ($I_{th(act)PNP}$). With the PDC bit the user can choose the PNP activation threshold current, which fits best to the application needs. A configuration of PDC=1 means for example that for rising load currents, the SBC delivers typically 50 mA at Tvj=150°C, whereas the rest of the load current is provided from the PNP transistor.

As an example a system with a maximum average V1 application current $I_{O(app),max}$ of 200 mA and a battery voltage of 16 V the power dissipation of the V1 regulator can be calculated as follows (example for 5V version):

$$P_{V1(UJA1169)} = (V_{BAT} - V_{V1}) \times I_{V1} = 11\,V \times 200\,mA = 2.2\,W$$

As a result the junction temperature rise could be significantly high, e.g. 88K with a PCB-related thermal resistance of e.g. 40 K/W. With making use of an external PNP transistor the UJA1169 power dissipation can be considerably decreased:

- With PDC=0 the typ. power dissipation of above example will divide as following:

  $P_{V1(UJA1169)} = (V_{BAT} - V_{V1}) \times I_{V1} = 11\,V \times 83\,mA = 0.91\,W$

  $P_{PNP} = (V_{BAT} - V_{V1}) \times I_{PNP} = 11\,V \times 117\,mA = 1.29\,W$

- With PDC=1 the typ. power dissipation of above example will divide as following:

  $P_{V1(UJA1169)} = (V_{BAT} - V_{V1}) \times I_{V1} = 11\,V \times 50\,mA = 0.55\,W$

  $P_{PNP} = (V_{BAT} - V_{V1}) \times I_{PNP} = 11\,V \times 150\,mA = 1.65\,W$

Although the UJA1169 power dissipation of V1 can be significantly decreased, the thermal and power characteristics of the PNP transistor as well as the thermal characteristics of the PCB must be examined, too.

In case the thermal dissipation for the PNP is still too high, it is possible to connect multiple PNP transistors in parallel.

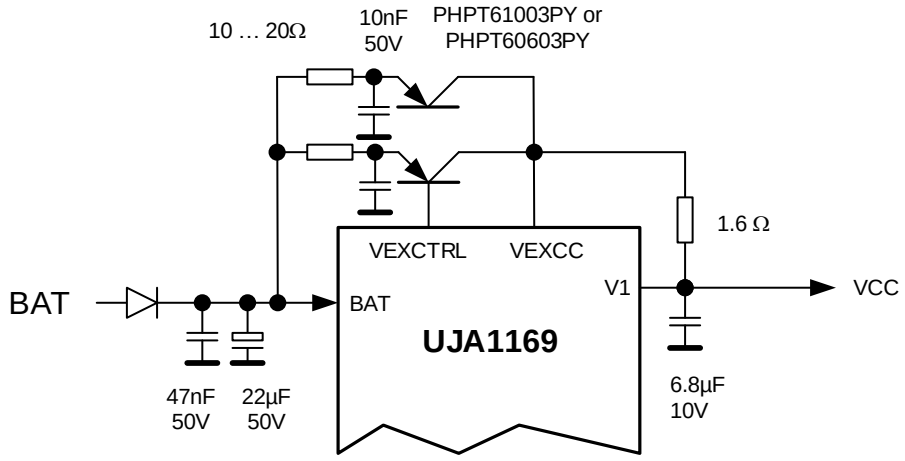


Fig 24. Multi-PNP solution for extended heat spreading

Due to the thermal characteristics of PNP transistors, an additional emitter resistor per PNP is required to balance the current between the used PNPs. The additional voltage drop across these resistors (as well as for the collector resistor) does not hurt the application performance, because at low battery supply voltages the full application current will run through the internal V1 regulator loop. At low battery voltages there is no thermal dissipation problem and thus, the internal regulator takes over the full current while the PNP does not need to carry any current and with that, the higher voltage drop in the PNP path is irrelevant. Only at higher battery voltage conditions the thermal energy needs to be shifted out of the SBC and with the higher battery voltage the additional drop on the series resistors are not hurting. So, even with multiple PNPs, the low-drop requirement can be fulfilled.

The filter capacitor C_{PNP} is required to protect V1 against overvoltage during RF-injection on the battery line. C_{PNP} shall be placed close to the emitter pin of the PNP to GND.

4.2.1 Details on the PNP concept

By use of the external PNP the application load current I_{VCC} is divided into two supply paths, the UJA1169 internal current I_{V1} and the external PNP current I_{PNP}. Besides the thermal advantages this current splitting allows keeping 5V output voltage stable (for the 5V variants) at even lower battery supply conditions since there is less voltage drop on the internal V1 regulator caused by the lower internal current I_{V1}.

With e.g. I_{PNP} = 150mA and I_{VCC} = 250mA the internal current I_{V1} would be 100mA. This can even be supported down to 5.5V Battery Supply, while without an external PNP a current of 200mA (I_{VCC}) would be available for the application at 5.5V Battery.

Using the 3V3 variants of the UJA1169 allows to go for even lower battery voltages with full output current capabilities. It should be noted, that with battery supply voltages below $V_{th(act)PNP}$ on pin BAT, the external PNP regulation loop gets stopped at the lowest value and close to the full application current will run through the internal V1 regulator loop regardless of the selected V1 variant (5V or 3V3 variant).

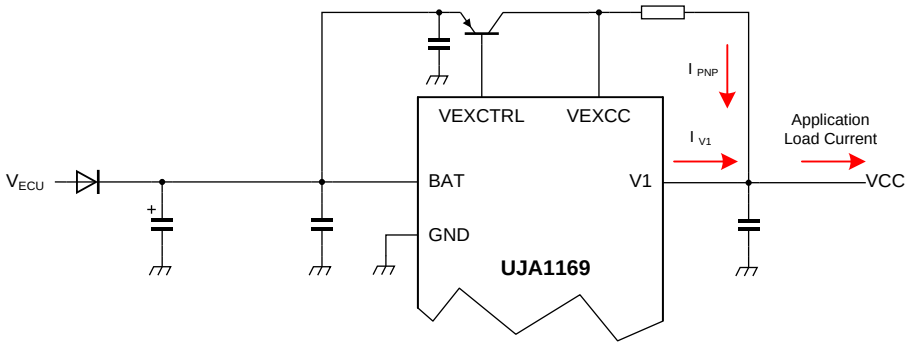


Fig 25. Application supply current split between PNP and SBC

Fig 26 illustrates how V1 and the PNP transistor combine to supply a slow ramping load current of 250 mA. Any additional load current requirement will be supplied by the PNP transistor, up to its current limit. If the load current continues to rise, I_{V1} will increase above the selected PDC threshold.

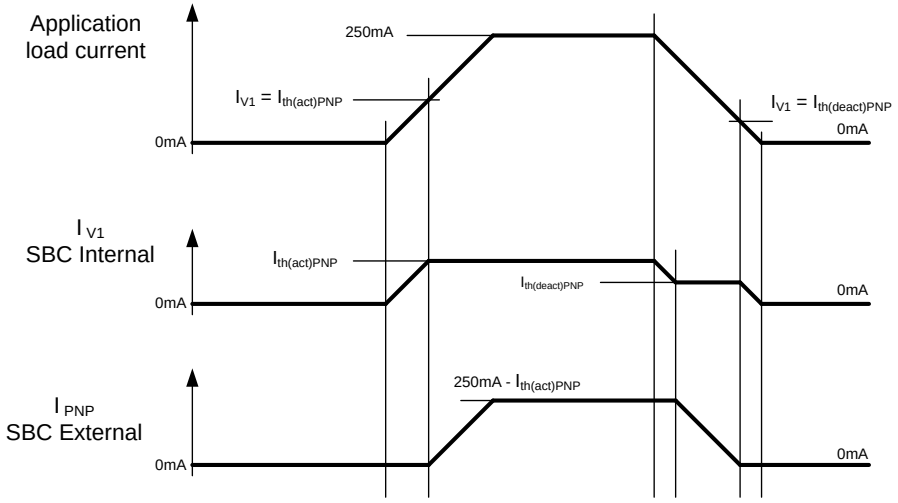


Fig 26. V1 and PNP currents at slow ramping load current up to 250mA

For a fast ramping load current, V1 will deliver the required load current (to a maximum of 250 mA) until the PNP transistor has switched on. Once the transistor has been activated, V1 will deliver at least the current defined with $I_{th(act)PNP}$ with the transistor contributing the balance of the load current (see Fig 27).

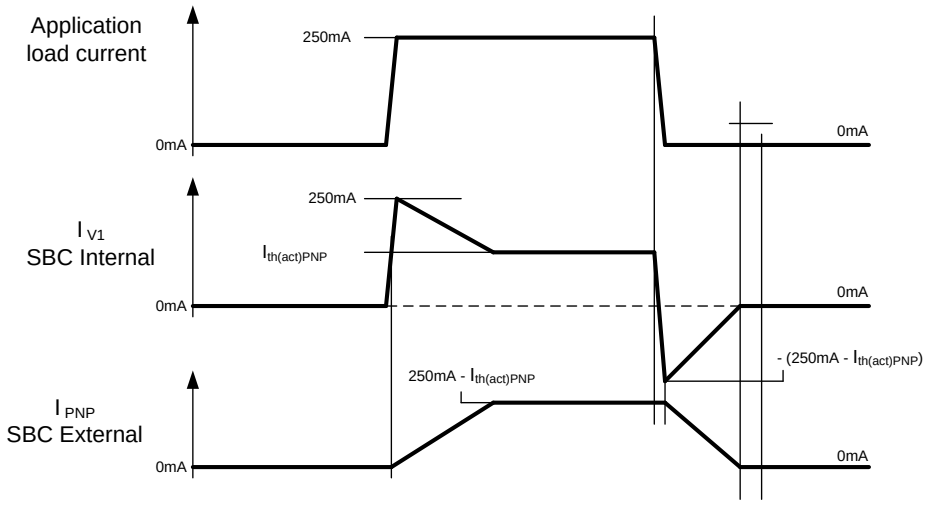


Fig 27. V1 and PNP currents at fast ramping load current up to 250mA

If now the load current rapidly would drop with more than the internal SBC regulator is actually delivering, the remaining PNP current would be higher than the application current, which would result in an output voltage overshoot, since the PNP needs some time to ramp down its output current. Such potential overshoot is prevented by the internal V1 sink regulator path, which temporarily takes over the current from the external PNP up to a current of I_{SINK} = 214mA. Now the PNP current is ramping down while the internal V1 regulator takes care of the correct output voltage through its internal sink regulator path.

The PNP control loop is operating based on a 128 bit up-down counter clocked with 64µs steps. With a current gain h_{FE} (also known as β or BETA) of 50 of the external PNP the max counter value corresponds to the maximum PNP current of at least 214mA. With higher β values, the PNP current can get higher than 214mA and it is recommended to limit the max PNP current based on the shunt resistor as explained earlier. Nevertheless if the PNP current shall intentionally get higher than 214mA, the reaction speed of the PNP regulation loop needs to be taken into account for sudden load changes. A good estimate of the PNP regulation speed for high PNP currents (linear approximation between 100mA and 200mA) is 150mA/ms with 64µs steps. The typical behavior is nonlinear with a characteristic as shown in Fig 28.

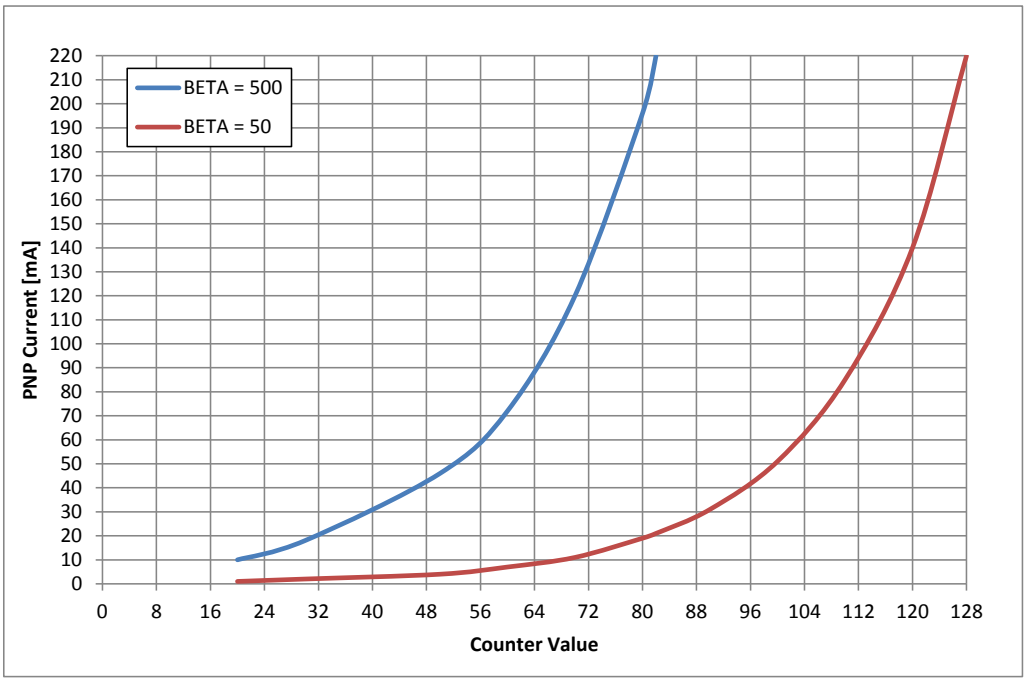


Fig 28. Typical relation between counter value and PNP current

In fact, the V1 regulator is a push-pull regulator being able to keep the V1 voltage stable regardless of the reaction speed of the external PNP. This fundamental behavior enables the high PCB design freedom with placing the PNP at any location on the PCB without the risk of an instable output voltage.

It should be noted, that there is an internal current source of typ 160µA active on VEXCTRL towards BAT, which makes sure that the PNP does not leak current to V1 while being turned off. This current source is disabled while the PNP is actively used and with that, there is no extra load current for PNP activation caused by this current source.

4.3 RAM retention feature

The V1 regulator of the UJA116x family provides a so-called “RAM retention feature”. This function makes sure, that the V1 regulator of the 5V derivatives in the UAJ116x family continues to deliver an output voltage even at very low battery voltages in order to keep the memory content of the host microcontroller alive.

In case the BAT voltage drops into regions, where the V1 regulator has detected its under-voltage threshold, typically the host controller gets reset through the RSTN pin of the SBC. If RSTN is LOW, the current consumption of the application gets reduced significantly allowing to keep the V1 voltage alive with just a few mA of output current. As such the SBC activates a parallel current source to the V1 regulator, which delivers the required output current to keep the RAM within the µC supplied. Depending on the remaining BAT voltage a certain voltage MAX drop according ΔVret(RAM) is provided at low application currents.

The RAM retention feature allows to keep the system alive at least down to 2V on the pin BAT of the SBC.

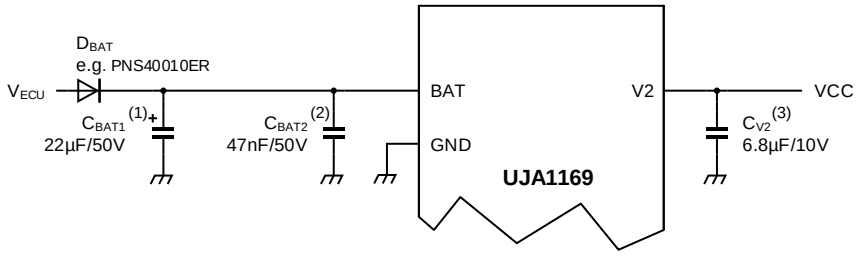
Since the V1 regulator is turned off in this region, there is a ZENER diode implemented limiting the output voltage on V1 for the case of a sudden BAT ramp-up during the RAM retention phase. This ZENER makes sure, that V1 does not raise above 5.5V until the regulator is re-started and RSTN is released.

4.4 V2 – 5V CAN supply voltage

The V2 voltage regulator is available in the UJA1169, UJA1169/F, UJA1169/3, UJA1169/F/3, UJA1169L and UJA1169L/F. It is used to supply the integrated CAN transceiver. So the V1 voltage regulator is separated from the CAN transceiver supply. In addition V2 can be used to supply other on-board hardware, e.g. stand-alone CAN transceiver.

In Fig 29 the typical V2 output circuitry is illustrated. For the V2 voltage regulator the output buffer capacitor C_{V2} is required. The requirements for C_{V2} are given in section 4.4.1.

V2 is able to drive up to 100 mA, but the internal CAN transceiver current consumption needs to be taken into account and subtracted from the overall V2 supply current budget.



(1) C_{BAT1} value is exemplary. On principle the value depends on application.

(2) C_{BAT2} value is a typical value. Typically it is an open mode ceramic capacitor or two capacitors in series.

(3) C_{V2} value is a typical value to buffer load changes.

Fig 29. Typical V2 application (UJA1169, UJA1169/F, UJA1169/3, UJA1169/F/3, UJA1169L and UJA1169L/F)

Please note that V2 has to be turned on actively via software control in order to activate the proper CAN supply for active communication on CAN. V2 is not required for wake-up detection on the CAN interface. The CAN wake-up hardware is supplied directly from the BAT input pin.

The regulator V2 provides a dedicated undervoltage and overvoltage monitoring capability, which can be assessed through the Supply Voltage Status Register (V2S).

It is not recommended to supply the V2 pin backwards from an external voltage regulator since an input current into the V2 pin in the range of about 300µA will occur if V2 internally is turned off in software. That would increase the overall quiescent current of the system in this condition. In case such reverse supply cannot be avoided, it has to be sure that the limiting values of the V2 pin are not exceeded (V_{V2} : -0.3V … +6.0V).

4.4.1 V2 output capacitor

The value of the V2 output capacitor C_{V2} depends on the requirements for line and load regulation. The V2 regulator is stable with a large range of capacitor values. Table 4 lists the recommended minimum capacitor value to be applied to the V2 output.

Table 4. V2 output capacitor

Effective minimum capacitance	Recommended minimum nominal capacitor value	Typical nominal capacitor value
1.76 µF with 5 V DC offset	4.7 µF	6.8 µF

The effective capacitance of a capacitor depends heavily on temperature and the DC charge voltage (DC offset). In order to cope with these effects it is recommended to use 6.8µF nominal capacitors. With that there should be enough margin for temperature and DC offset impact on the effective capacitance. For details please refer to the data sheet of the selected capacitor.

For small effective capacitor values the MIN ESR of the capacitor shall be at least 50mΩ. Bigger capacitances allow lower ESR values. In general the MAX ESR shall not exceed 2Ω. The higher the ESR value, the bigger a potential output voltage impact is on steep load current changes.

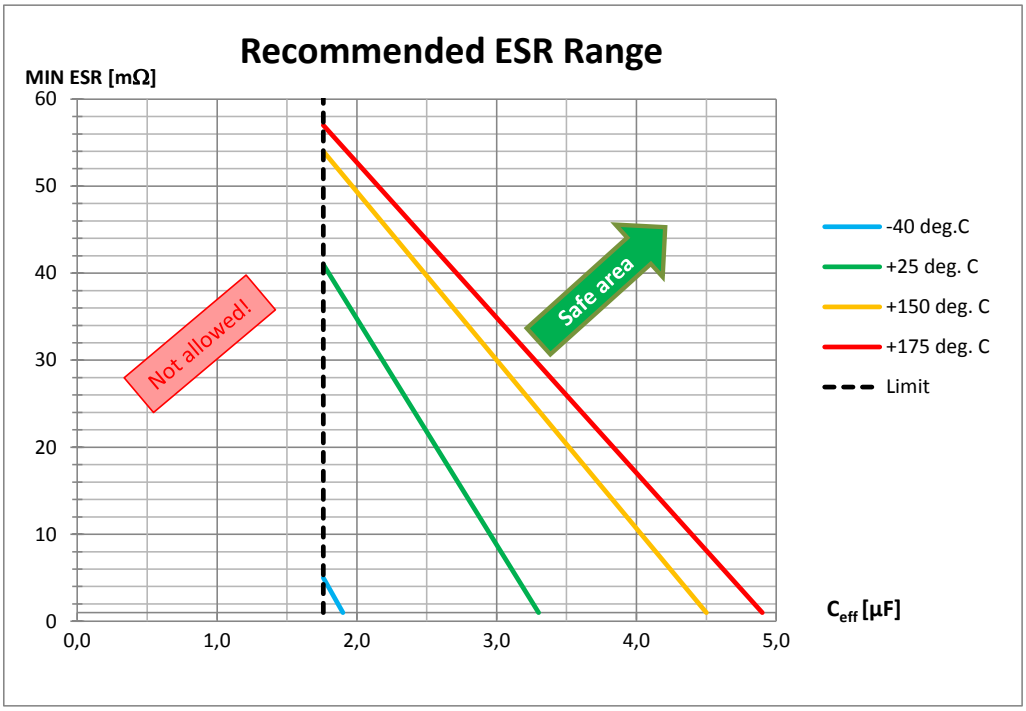


Fig 30. Recommended ESR range for V2 regulator

4.5 VEXT – 5V sensor supply

The VEXT voltage regulator is available in the UJA116x variants with the type number extension VX. Within the UJA1169 derivative, the extension /X indicates this option. This regulator is protected against battery supply voltages up to +40V and negative voltages down to -18V to support off-board hardware supply, e.g. for sensors. Two VEXT versions with different supply current capability are available. In Table 5 an overview of the VEXT versions is listed.

Table 5. VEXT versions of UJA116x SBC family

Type number	MIN output current before current limitation kicks in
UJA1167/VX (A/X) UJA1168/VX (A/X) UJA1168/VX/FD (A/X/F)	30 mA
UJA1169/X UJA1169/X/F UJA1169L/X UJA1169L/X/F	100 mA

In Fig 31 the typical VEXT output circuitry is illustrated. For the VEXT voltage regulator the output buffer capacitor C_{VEXT} is required. The requirements for C_{VEXT} are given in section 4.5.1.

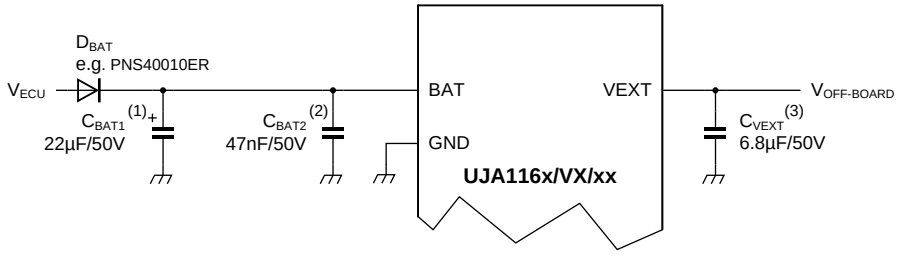


Fig 31. Typical VEXT application (UJA116x/VX/… and UJA1169/X/…)

Please note that VEXT has to be turned on actively via software within the Regulator Control Register.

The regulator VEXT provides a dedicated undervoltage and overvoltage monitoring capability, which can be assessed through the Supply Voltage Status Register (VEXTS). Please note, that there is no further autonomous action of the SBC detecting an overvoltage besides bare signaling.

4.5.1 VEXT output capacitor

The value of the VEXT output capacitor C_{VEXT} depends on the requirements for line and load regulation. The VEXT regulator is stable with a large range of capacitor values. Table 6 lists the recommended minimum capacitor value to be applied to the VEXT output.

Table 6. VEXT output capacitor

Actual minimum capacitance	Recommended minimum nominal capacitor value	Typical nominal capacitor value
1.76 µF with 5 V DC offset	4.7 µF	6.8 µF

The effective capacitance of a capacitor depends heavily on temperature and the DC charge voltage (DC offset). In order to cope with these effects it is recommended to use 6.8µF nominal capacitors. With that there should be enough margin for temperature and DC offset impact on the effective capacitance. For details please refer to the data sheet of the selected capacitor.

For the VEXT regulator there is no requirement on a MIN ESR due to the internal series protection element inside of the regulator, which adds already some minimum ESR to the supply. Nevertheless the MAX ESR shall not exceed 2Ω. The higher the ESR value, the bigger a potential output voltage impact is on steep load current changes.

4.5.2 VEXT short to BAT detection

After the VEXT over-voltage detection time $t_{det(ov)}$ expires, the internal protection transistor is switched off to prevent reverse current from further raising the level at pin BAT. A VEXT over-voltage capture event will be generated if enabled (via bit VEXTOE in Supply event enable register).

During the over-voltage detection time $t_{det(ov)}$, high current can still flow into the pin VEXT. This will not cause any damage to the internal circuit and has only very little influence on the overall junction temperature, since the detection time is very short ($t_{det(ov)}$ max = 32 µs).

4.5.3 VEXT thermal considerations

Since this regulator is short circuit proof against shorts to BAT or to GND, the potentially higher power dissipation during a short circuit needs to be taken into account. This is especially relevant for the UJA1169 derivatives delivering at least 100mA short circuit current.

In case the VEXT is shorted to GND, the regulator will change towards a current source like behavior, if the short circuit limitation current is achieved. With that, the output voltage on that regulator will get reduced quite rapidly towards 0V while the output current stays with the short circuit current until the short is removed. In Fig 32 a typical current limitation curve is shown as an example for the UJA1169 derivative.

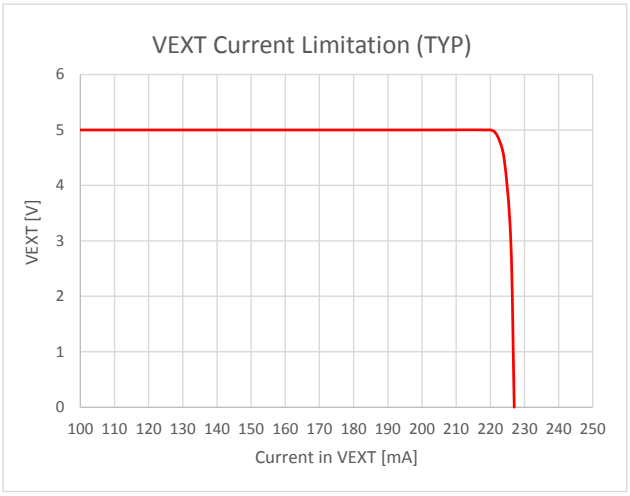


Fig 32. Typical short circuit current behavior of VEXT (UJA1169 example)

In order to deal with the increased power dissipation following strategy is recommended:

The UJA116x family offers a temperature warning information within the Main Status Register (OTWS). If this flag is set, the chip temperature has been increased above the warning threshold. Furthermore the undervoltage flag of VEXT within the Supply Status Register (VEXTS) gives an indication that the regulator might be overloaded. If both information are present in the same time, this is a very strong indicator for an overloaded VEXT supply caused by a short to GND. From software perspective it might be useful to disable VEXT in this case temporarily and check, whether the Temperature falls below the warning threshold again.

For failure recovery it might be useful enabling VEXT cyclically and check for the VEXTS flag, whether VEXT reaches the nominal output voltage again.

It should be noted, that a low battery condition may as well cause a VEXT undervoltage event. As such, it would be useful to monitor the BAT supply of an ECU independently as done in most applications anyway. Nevertheless, at low battery conditions, there will not be an overtemperature signaled due to the lower power dissipation at low BAT condition and the combination of overtemperature and VEXT undervoltage should be sufficient to distinguish a true short on VEXT from a low battery situation without dedicated BAT monitoring.

5. Thermal Considerations

5.1 Generic thermal model

For thermal estimations a so-called “compact thermal model” is used for the UJA116x SBC family similar to other SBCs from NXP. Such a thermal model is based on an artificial thermal network developed for the specific chip size and package used for the device. This thermal model makes use of a standardized description of the package while the parameters are derived out of an accurate finite elements analysis of the chip and the package.

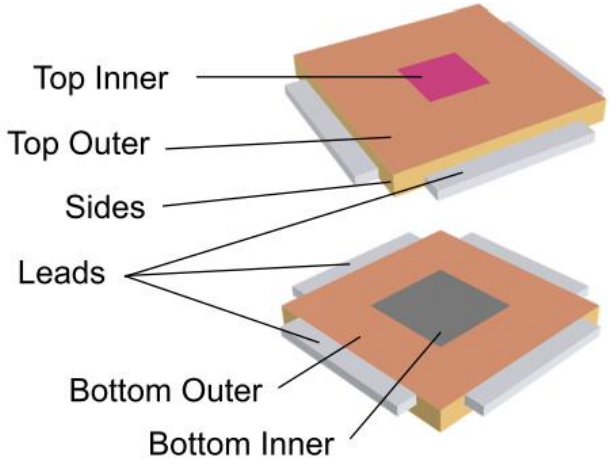


Fig 33. Package Definitions

Within Fig 33 the different paths for the thermal flow in a design are shown based on a standard squared package, which can be translated to any other IC package like the HVSON type packages used for the UJA116x family.

The red square in the picture is representing the chip inside the housing while the grey square is representing the exposed die pad (metal underneath the package). Following thermal paths are defined:

- Top Inner: The area above the chip to the top plastic
- Top Outer: The area around the chip to the top plastic
- Sides: The side area of the package (plastic part)
- Leads: The metal pins leaving the package to the sides (all in parallel)
- Bottom Outer: The area around the exposed die pad to the plastic
- Bottom Inner: The metal area of the exposed die pad

From the IC inside of the package (junction) there is an individual thermal resistance towards the above mentioned outside points of the package. Besides these direct paths

from the chip to the outside, there are thermal paths between the peripheral points of above list. This results in a simplified thermal model as shown in Fig 34.

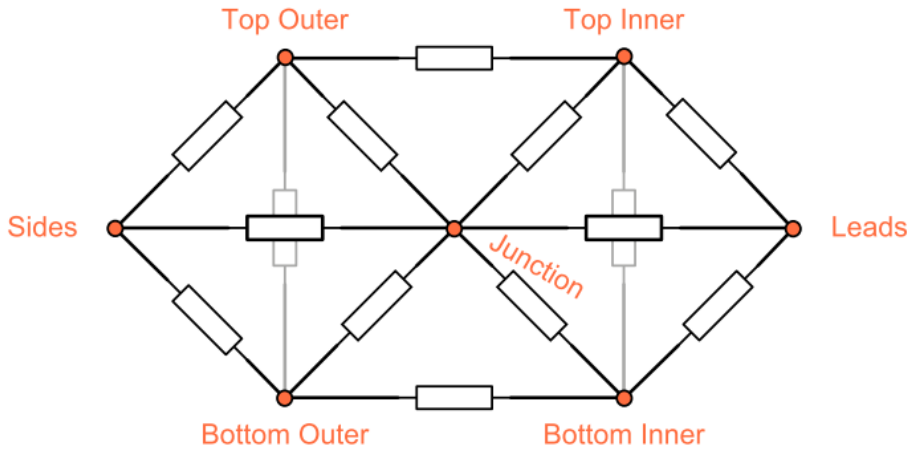


Fig 34. Simplified thermal resistor model

For the UJA116x family these thermal resistor values can be found in the following chapters for the HVSON14 and HVSON20 package. The given numbers can be imported in typical thermal simulation tools like FloTHERM.

5.2 HVSON14 Package

Following table provides the thermal resistances for the UJA116x family, which is mounted into the HVSON14 package

Table 7. Thermal Resistance HVSON14

R[K/W]	Top Inner	Top Outer	Bottom Inner	Bottom Outer	Sides	Leads	Surface [mm²]
Junction	306.66	∞	7.32	397.78	∞	∞	
Top Inner		3088.08	2478.98	3527.04	∞	∞	1.44
Top Outer			63.45	124.15	∞	502.67	12.06
Bottom Inner				6735.15	190.49	75.53	8.23
Bottom Outer					∞	202.33	4.01
Sides						101.54	12.75
Leads							1.26

For a typical board following thermal resistances are possible depending on board details:

:

Table 8. Thermal Resistance of Example PCBs

HVSON14	2-Layer 100mm x 100mm	4-Layer 100mm x 100mm
Rth of the system [K/W]	**50 … 60**	**40 … 50**

These numbers are giving a good first estimate for a concrete PCB development. For a more detailed analysis the concrete PCB data needs to be put into a thermal simulation tool.

5.3 HVSON20 Package

Following table provides the thermal resistances for the UJA1169 family, which is mounted into the HVSON20 package.

Table 9. Thermal Resistance HVSON20

R[K/W]	Top Inner	Top Outer	Bottom Inner	Bottom Outer	Sides	Leads	Surface [mm²]
Junction	107.73	∞	4.09	∞	822.38	∞	
Top Inner		9072.04	558.10	1112.63	∞	∞	4.83
Top Outer			128.11	69.95	∞	223.73	14.42
Bottom Inner				67.23	244.68	39.55	9.98
Bottom Outer					∞	96.16	6.78
Sides						86.49	15.30
Leads							2.50

For a typical board following thermal resistances are possible depending on board details:

Table 10. Thermal resistance of example PCBs

HVSON20	2-Layer 100mm x 100mm	4-Layer 100mm x 100mm
Rth of the system [K/W]	**50 … 60**	**33 … 45**

These numbers are giving a good first estimate for a concrete PCB development. For a more detailed analysis the concrete PCB data needs to be put into a thermal simulation tool.

5.4 Power Dissipation Calculator

For power dissipation estimates of applications there is a simple power dissipation calculator available for the UJA116x family, which is based on an EXCEL spread sheet. This calculator is added to this Application Note package.

Power Dissipation of UJA116x Family (V1.0)

Battery Supply in Normal Mode		
Supply voltage (VBAT)	16,0	V
Quiescent current IBAT (Standby)	83	µA
Additional quiescent current ΔIBAT(add) @ CAN bias on	55	µA
Quiescent power dissipation	0,002	W

V1 active	On	
V1 voltage (3.3V for UJA1169/3 only)	5	V
PNP available ? (for UJA1169 only)	Yes	
BETA external PNP (50 ... 500)	200	-
Base Emitter Voltage external PNP	0,70	V
PDC bit setting (0 --> 83mA typ hot / 1 --> 50mA typ hot)	50	mA
V1 load current (116x 100mA MAX / 1169 250mA MAX)	150	mA
PNP output current (external part of the regulator)	112	mA
V1 output current (internal part of regulator)	50	mA
Average VCAN current (from V1, if VEXT selected and not 3V3)	11,50	mA
CHECK: Total V1 current (116x ≤ 100mA / 119x ≤ 250mA)	161,50	mA
Dissipation PNP driver	0,009	W
V1 incl PNP driver (incl. CAN supply, if from V1)	0,559	W

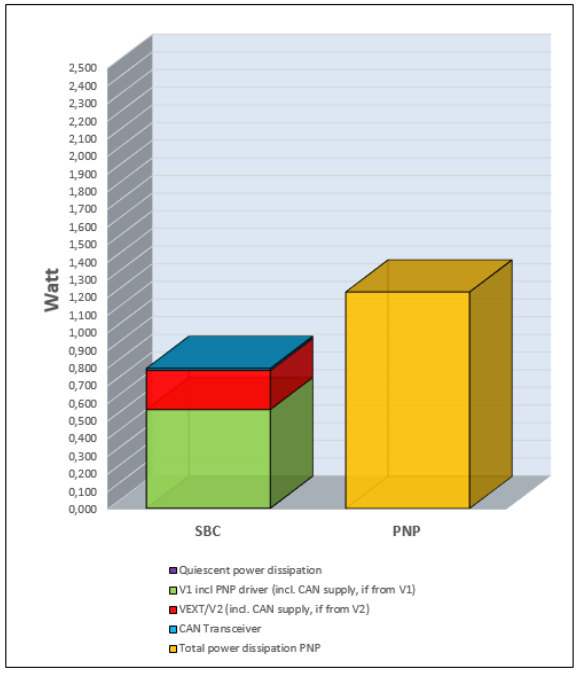
VEXT/V2 active	On	
VEXT or V2 version	VEXT	
VEXT/V2 output current (out of Pin)	20	mA
Average VCAN current (from V2, if V2 selected)	0,00	mA
CHECK: Total VEXT/V2 current (116x ≤ 30mA / 1169 ≤ 100mA)	20,00	mA
VEXT/V2 (incl. CAN supply, if from V2)	0,221	W

CAN Interface Active	On	
CAN bus termination R(CANH-CANL), [45 ... 65 Ohms]	60	Ω
CAN bus utilization [typ OEM bus load is 60% MAX]	60%	
CAN sending contribution of this node [10% ... 50%]	20%	
CAN dominant ratio [≤ 80% due to CAN protocol rules]	80%	
CAN Short Circuit	No	
VCAN recessive supply current	7,50	mA
VCAN dominant supply current (2.5V differential assumed)	49,17	mA
Average VCAN current	11,50	mA
CAN Transceiver	0,012	W

Total power dissipation SBC	0,794	W

T ambient	85	°C
T junction	113	°C

Thermal resistance SBC:
Rth(junction - ambient) *[depends on PCB-design]* 35 K/W



Total power dissipation PNP	1,227	W

T junction	121	°C

Thermal resistance PNP:
Rth(junction - ambient) *[depends on PCB-design]* 29 K/W

Fig 35. UJA116x Power Dissipation Calculator

All grey fields are input fields and allow to select a specific application use cases. Some of these fields allow any entry while others are opening a select menu depending on the parameter to change. As a result of an entry, the power dissipation of the various contributors is calculated and displayed graphically. Please note, that there is not necessarily an automatic consistency check, whether a certain combination of parameter is technically feasible or makes sense for a specific UJA116x derivative. It is in the responsibility of the user to select logical combinations and values in accordance with the used device specification.

5.4.1 Battery supply

First thing to select is the overall BAT supply. This voltage is regarded to be the BAT input voltage on the BAT pin of the SBC and not the ECU BAT voltage. In cases there is a polarity protection diode in the system, a potential voltage drop across that diode has to be anticipated when selecting the BAT voltage in the calculator.

5.4.2 V1 parameter

V1 can be activated or deactivated. In case V1 is deactivated, all currents related to V1 are regarded to be zero. This includes a potential CAN Transceiver current, if CAN is supplied from V1, which is the standard case for the UJA116x family. (Note: UJA1169 provides derivatives with CAN supplied from V2). If CAN is supplied from V2 (some UJA1169 derivatives) and V1 is switched off, there will still be CAN current in V2 although in reality it is not possible to have CAN active with V1 off (Sleep Mode). Please make sure, that your parameter combination makes sense.

Some UJA1169 derivatives offer a 3V3 option on V1. If this option is selected, it is not possible to run CAN from V1, because CAN needs a 5V supply. Consequently, if CAN is still assigned to V1 while 3V3 is selected, the CAN transceiver is simply switched off and does not consume any current. As such, if 3V3 is selected, please switch the VEXT/V2 selector to V2 some rows lower in the sheet. All 3V3 versions of the UJA1169 family are providing a V2 regulator as CAN supply and no VEXT regulator.

The third parameter deals with the external PNP transistor. If it is turned on, parts of the current is outsourced to the PNP and with that, the dissipation of the SBC goes down.

The dissipation caused by driving the external PNP is taken into account through the next two parameters, the BETA of the PNP and the voltage drop across the Base Emitter connection.

The PDC bit setting selects, how much current actually is outsourced towards the PNP transistor. Here you can select the current threshold according to the data sheet. Please note, that the threshold current of the SBC gets lower at higher temperatures. So, it is recommended to select the 150 deg.C values from the data sheet (50 or 83 mA).

The last selectable parameter is the application current drawn from the V1 output pin.

When modifying any of the parameter it is important to check the yellow field, whether the overall current, which is calculated, stays within the derivative boundaries. Keep in mind that in some constellations, the CAN supply current runs out of V1 as well and adds to the overall current of the regulator.

5.4.3 VEXT / V2 parameter

Again the first field allows activation or deactivation of that regulator. In case CAN is assigned to that regulator (V2 selection), the CAN block is turned off as well, if this regulator is off.

Within the next field the derivative can be selected. In case VEXT is chosen, the CAN supply automatically moves to V1. As such, in all derivatives without V2 you need to select the VEXT version and turn it simply off even if VEXT is not provided by the device. With that, CAN is supplied from V1. Only for the UJA1169 there are derivatives with V2 and only here it makes sense to select V2.

Next field allows to define the V2/VEXT pin output current. Similar to V1, please select a current, which is supported by the device. Keep in mind, that the CAN supply current may be delivered to this regulator as well. Therefore please check again the yellow field, whether the overall current stays within the boundaries of the device.

5.4.4 CAN Interface

CAN may be activated or deactivated with the first selector. In case CAN is off, there is no current contribution by this block at all. The potential wake-up current is included in the overall quiescent current on the top of the sheet.

The second selector allows to define the CAN termination resistance of the overall CAN system. This is normally 60 Ohms. Nevertheless in bigger systems the resistance may be slightly lower. This parameter should stay between 45 … 65 Ohms according to the CAN standard.

The following 3 parameter are dealing with the sending rate of the CAN Transceiver as explained in more detail within chapter 9.9. The CAN bus utilization is the so-called bus load on CAN – it defines to what percentage there is real active CAN traffic. Normally OEMs do not load the CAN systems with more than 60% traffic and 40% idle time in order to keep room for event driven CAN frames on the bus.

The CAN sending contribution defines, how many of the frames per time are transmitted by this node – actually it depends on the number of nodes in the system, how much of the 60% time this node is actively sending. For a 5 nodes system, each node can only send 20% of the overall available time in average. As such, 20% is a good estimate for this parameter.

Finally the CAN dominant ratio can be selected, which defines how many dominant bit times are within one CAN frame. Due to the CAN protocol rules, a maximum of about 80% of the bits can be dominant. This is already the worst case. In typical frames there are far less dominant bit times included. Since the dominant phase causes the highest currents, a high percentage value gives the worst thermal system situation.

The last parameter deals with CAN short circuit conditions. If this is activated, the dominant currents are going up to the short circuit limit of the CAN Transceiver. For the UJA116x family, there is a quite unique and low short circuit protection limit of 55mA. Due to that, there is only a very small impact of a potential bus short to the overall dissipation of the ECU! (Mind: during normal communication the dominant current is already in the range of 40mA).

5.4.5 Ambient Temperature

Close to the end of the sheet the ambient temperature of the application can be selected. A typical value is 85 deg.C. Anyway, any other temperature can be selected here.

5.4.6 Thermal Resistance

The thermal resistance of the application is a PCB dependent number. For a 4-layer board using the HVSON20 package for example, a thermal resistance of 35 K/W is manageable. For more details please refer to chapter 5.

For the thermal resistance of a potentially used PNP please check the data sheets or Application Notes of the used component. Within the example a resistance of 29K/W is anticipated as an example.

5.4.7 Calculations

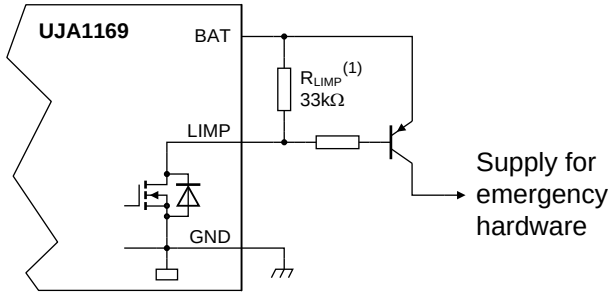
Based on all inputs the power dissipation of all contributors is calculated and summed up for the SBC and for the optional PNP. This results in a potential internal junction temperature of the devices based on the PCB assumptions taken within the Thermal Resistance parameter. As long as the junction temperature stays within 150 deg. C the Junction temperature field stays green. If the temperature exceeds that range it will get orange and finally red, if it is far above that.

As mentioned earlier, the calculations shall be taken as a good estimation of the power dissipation and not regarded as a guarantee. The results have to be interpreted and checked for consistence by the user of the spread sheet.

6. LIMP output (UJA1169)

6.1 Introduction

In case of a serious system malfunction it is possible to enable emergency hardware via the battery-related, active-LOW, open-drain output pin LIMP. In Fig 36 a typical circuitry for the LIMP pin is shown.



(1) R_{LIMP} value is exemplary. On principle the value depends on application.

Fig 36. Typical Limp application

The LIMP pin is implemented with an open-drain low-side driver transistor with a robustness up to +40V and -0.3V. As such it can be used to directly drive signals in the BAT supply environment as shown in Fig 36.

The pin is designed to guarantee a MAX voltage drop of 0.4V in active state with current of 0.8mA. It should be noted, that this performance is guaranteed in the full temperature range of the SBC up to the MAX over-temperature shut-down of +185 deg. C. Thus, the LIMP function is guaranteed to be operational even under these extreme conditions. Based on the above specification a maximum RDS_{on} of the LIMP switch can be calculated as follows:

$$RDS_{on\ LIMP}\ (MAX) = \frac{0.4\ V}{0.8\ mA} = 500\ \Omega$$

The LIMP pin shall not carry more than 20mA continuous current in the application due to life time limitations.

6.2 Functional description of LIMP pin

The LIMP pin function is associated with the LHC bit within the FailSafe Control Register of the SBC. Whenever LHC is set “1”, the LIMP output pin will be driven active LOW. On clearance of that bit, the LIMP pin will be set floating again. Setting of the bit can happen based on internal SBC events or with direct SPI access. Clearing is possible only with software interaction through the SPI interface.

Failure conditions triggering a LIMP activation include SBC over-temperature events, loss of watchdog service, short-circuits on V1 or RSTN and user-initiated or external reset events. Table 11 summarizes all conditions, which will finally lead to LIMP pin activation (LHC bit set).

For detecting serious failures, the UJA1169 uses the Reset Counter Control bits RCC that are located in the Fail-Safe control register. Each time when the SBC enters Reset Mode, the reset counter RCC will be incremented by one. In a regular running system it is expected that the RCC bits are reset by software. But in case of a system malfunction this is not the case and the RCC will further increase until the maximum value of 3. An overflow of this counter beyond the level of 3 causes the SBC to set the Limp Home Control bit (LHC in the Fail-safe control register) with the RCC counter overflowing to zero. LHC directly controls the external LIMP output signal.

- LHC == 0 LIMP is floating
- LHC == 1 LIMP is active LOW

Setting LHC by software directly activates the LIMP output pin to active LOW level as well without influencing RCC. This might be useful for self-test purposes of the LIMP hardware.

Clearing of LHC is possible under software control with write access to LHC or upon a Battery power-on condition coming from OFF Mode of the SBC.

Based on the RCC counter the application software can define, how many reset events shall be tolerated until the LIMP function gets active (LHC is set). Initializing the RCC bits to a level of 3 would cause any reset event to immediately set LHC and with that activate the LIMP pin. Default start-up setting of RCC is 0 after power on.

The reset counter increment is intended mainly for Watchdog reset events or external reset events on the RSTN pin and operates autonomously in the background.

Besides the reset counter overflow there are following additional conditions setting LHC:

- Over temperature for more than $t_{d(LIMP)}$
- SBC in Reset State for more than $t_{d(LIMP)}$ (e.g. by clamped RSTN pin or permanent V1 undervoltage due to overload)

A detailed LIMP state diagram is given in Fig 37.

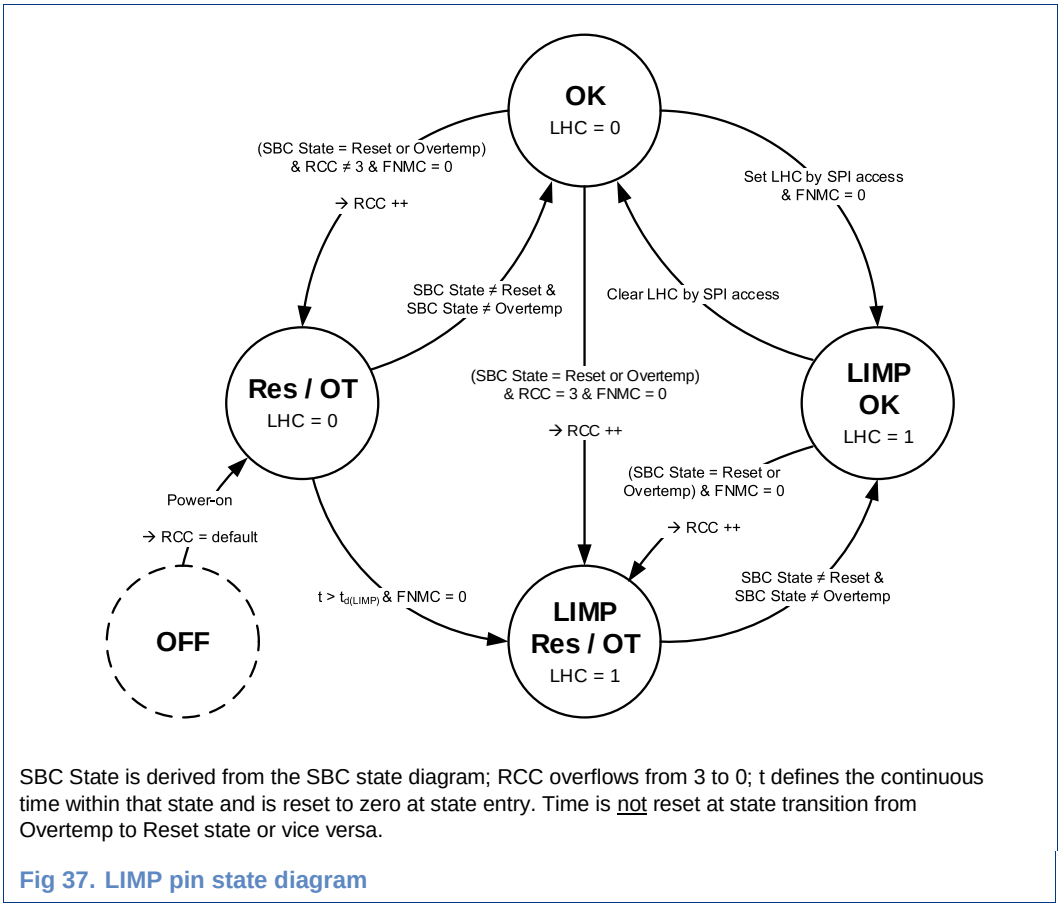
Please note, that leaving Sleep Mode of the SBC causes a reset event as well since the V1 supply was off and the SBC starts-up through the Reset Mode of the SBC. Thus, the RCC will increment by one for each Sleep Mode cycle. The application software needs to take care, that RCC does not overflow caused by multiple Sleep Mode entries by writing actively towards the RCC bits.

For software related details, please refer to chapter 12.6.3.

Table 11. Conditions for LIMP pin activation (LHC bit is set)

Condition	Comment
LHC set by SPI command	Setting (or resetting) of LHC via SPI is possible only, while the SBC is not in Reset Mode or Overtemp Mode
Reset Mode clamped	SBC is continuously in Reset mode due to a clamped RSTN pin or a permanent undervoltage on V1 e.g. due to overload condition. LIMP gets active, if Reset Mode lasts for longer than $t_{d(LIMP)}$ while RCC < 3 or Reset Mode is entered while RCC = 3
Overtemp Event	SBC is in Overtemp mode for more than $t_{d(LIMP)}$ while RCC <3 or Overtemp mode is entered while RCC = 3
RSTN LOW	RSTN was pulled LOW externally while RCC = 3
Watchdog Failure	Watchdog not triggered correctly causing Reset Mode Entry while RCC = 3
Illegal Sleep Mode Entry	Software tries to enter Sleep Mode with pending wake-up or no enabled wake-up source while RCC = 3
Wake-up from Sleep	Reset Mode entered out of Sleep Mode while RCC = 3

The LIMP function (pin and LHC bit) as well as the RCC counter are not operational during Forced Normal Mode of the SBC. While in Forced Normal Mode, pin LIMP stays off, RCC stays unchanged and LHC stays “0”.



SBC State is derived from the SBC state diagram; RCC overflows from 3 to 0; t defines the continuous time within that state and is reset to zero at state entry. Time is not reset at state transition from Overtemp to Reset state or vice versa.

Fig 37. LIMP pin state diagram

7. WAKE pin Interface (UJA1167(A) / UJA1168(A) / UJA1169)

7.1 Introduction

UJA116x family members supporting the Sleep mode function are additionally offering a dedicated local wake-up pin which allows to wake-up an ECU out of low power mode even if the local voltage supply (V1) is completely turned off and the local microcontroller might be turned off.

The WAKE pin is designed to be robust for voltages within the entire battery supply range and as such can be connected to battery or GND related input signals without clamping or draining excessive currents.

7.2 Hardware application

From hardware implementation the WAKE pin is a very high-ohmic input pin with a weak internal pull-down resistance of about 20MOhms to GND. As such there is hardly any input current on this pin if it is applied to e.g. the battery voltage.

For high robustness against transients and ESD events from outside the application and potential backwards supply at loss of GND conditions, the pin shall be applied with a 10k series input resistor as well as a small capacitor of 10nF towards GND.

Depending on the final application a pull-up resistor (for GND related input signals) or a pull down resistor (for BAT related input signals) might need to be added. Some examples are shown in Fig 38.

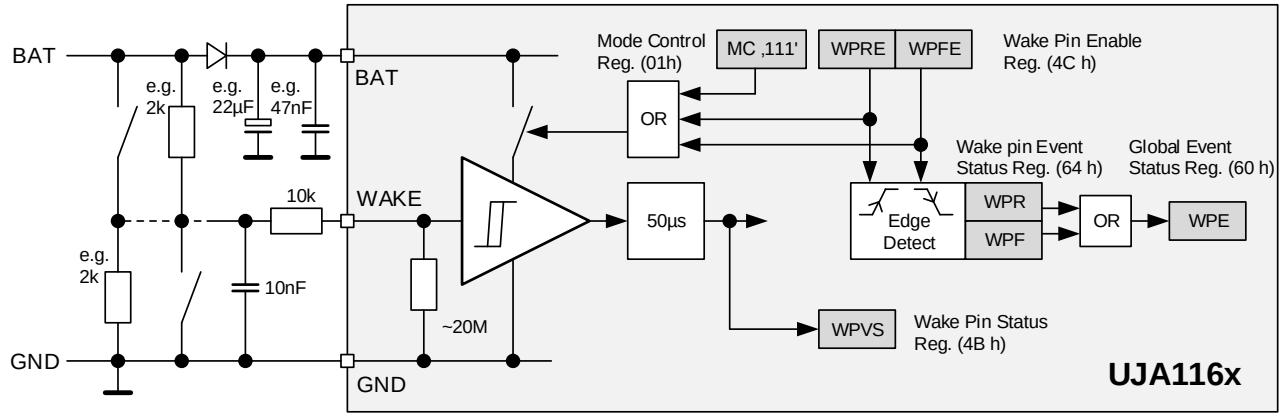


Fig 38. WAKE pin function and application examples

7.3 Functional description

As illustrated in Fig 38 the WAKE pin function needs to be activated through software control before it can be used through one of the WAKE pin enable bits WPRE or WPFE. Default at battery power-on is “OFF” (both bits are cleared). If at least one of these bits is set, the input comparator gets supplied and activated. The comparator is activated as well, if the SBC has entered its Normal Mode selected through the mode control bits (MC) within the Mode control register. This activation causes a slight quiescent current increase for the comparator supply of typically 2µA.

Once active the actual logical state of the WAKE input can be polled through the WPVS flag at any time. Please note, that signal changes are signaled only if the level change was stable for at least 50µs in order to avoid that noise causes permanent signal events.

With the two bits WPRE (WAKE Pin Rising-edge Enable) and WPFE (WAKE Pin Falling-edge Enable) it can be decided, which edge is captured as an event within the UJA116x finally leading to a system wake-up. The result of that evaluation is captured in the according WAKE pin Event Status bits WPR and WPF. For easier wake-up source analysis there is a shadow bit WPE located within the Global Event Status Register allowing to quickly discover the root of a potential wake-up event.

Once an edge event is captured, this event stays valid in the register until it is actively cleared by software access. In order to prevent accidental bit clearance, a simple read access to these flags will not influence their value. Furthermore writing a zero to these flags will NOT change their content – flags will stay set! In order to clear these flags, the according bit has to written with a “1” actively.

The analog input comparator provides fixed input thresholds with a defined hysteresis as follows:

- Threshold rising edge 2.8V … 4.1V
- Threshold falling edge 2.4V … 3.75V
- Hysteresis between edges 250mV … 800mV

This allows to monitor input signals independently from the actual battery voltage with a fixed input threshold.

8. Microcontroller interface

8.1 Reset interface

8.1.1 Functionality of RSTN pin

The mini high-speed CAN SBC UJA116x family offers a bidirectional RSTN pin for triggering a system reset. On the one hand the reset of the SBC is triggered if the RSTN pin is forced active low externally e.g. by the microcontroller. On the other hand the SBC generates a reset pulse on the RSTN pin on power-on or any system condition that requires a system reset (see datasheets [3], [4], [5], [6], [10]).

In general there are three different kinds of possible resets that demand different software handling:

1. Reset at power-on: The complete system is not configured. Therefore, the microcontroller and UJA116x must be initialized (cold start).
2. Reset at Wake-up out of Sleep, at over-temperature shutdown or at V1 under-voltage: As the microcontroller was not supplied in these cases, its configuration is lost and hence it must be completely reinitialized (cold start).
3. Reset at watchdog failure, software Resets, external resets: As these resets are caused by software or hardware failures the application must be checked and reinitialized (warm start).

In Sleep or Over-temperature mode the RSTN pin is always LOW and becomes HIGH again after either the chip has cooled down from overtemperature condition or a wake-up event is detected during Sleep mode. Moreover, the RSTN pin is only released when V1 has left its under-voltage state and the reset length timer (see chapter 8.1.2) has elapsed. In this process it must be considered that the reset length timer is not started before the V1 voltage is above its 90% under-voltage threshold (4.5 V to 4.75 V for the 5V derivatives, 2.97 V to 3.135V for the 3V3 derivatives). This behavior is independent of the RLC bit configuration in the Start-up Control Register.

The RSTN pin voltage is defined by the V1 voltage level and is completely independent of the battery supply. Its characteristics are illustrated in Fig 39 (with the condition of a pull-up resistor to V1 of min. 900Ω):

- If V1<1V, the voltage at RSTN is at most equal to V1 voltage (area 1 in Fig 39).
- If V1>1V, the voltage at RSTN is at most 0.2xV1 (area 2 in Fig 39).

This ensures that in case of low V1 voltage the RSTN pin voltage is always lower than 1V. Hence, it prevents an unsupervised operation of the microcontroller as it remains in reset state.

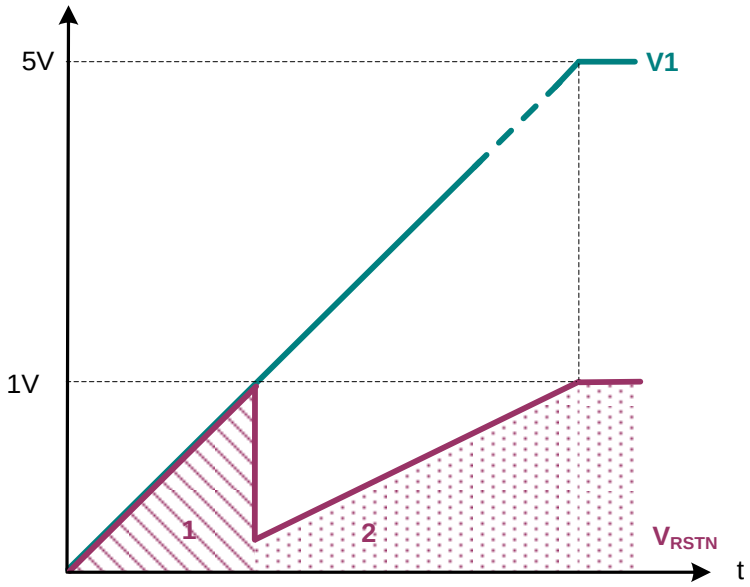


Fig 39. Gap free RSTN pin specification ($R_{pull-up}$ = 900Ω)

8.1.2 Configuration of the reset length

8.1.2.1 Reset length at cold start (V1 off during reset event)

The UJA1164(A), UJA1167(A), UJA1168(A) and UJA1169 provide a selectable startup reset length for the microcontroller. Startup means that the microcontroller was unsupplied (cold start). This is the case at any Power-On, V1 under-voltage, Overtemp and Wake-up out of Sleep mode. These reset events can trigger four different selectable reset length which are 20 to 25ms, 10 to 12.5ms, 3.6 to 5ms or 1 to 1.5ms. With the selectable reset length after V1 under-voltage the UJA116x can serve different kind of microcontrollers that require different start-up length before a system reset can be released.

The selection of one of the four reset pulse width is done via the bits RLC in the Start-up control register in the non-volatile memory of the SBC. Settings in the non-volatile memory are stored even if totally unpowered and thus the configured reset length is available at any power-on event. Writing to the non-volatile memory requires are special procedure in order to avoid unintended re-programming of the SBCs default settings after power-on. Please refer to chapter 11 on the non-volatile memory programming procedure.

8.1.2.2 Reset length at cold start for the UJA1163(A)

The UJA1163(A) does not support a user selectable reset length at cold start because it does not offer a SPI interface. The reset length is preconfigured for any cold start to the longest reset pulse of 20 to 25ms.

8.1.2.3 Reset length at warm start (V1 on during reset event)

All other UJA116x resets like WD failure, external and software resets always trigger the shortest reset pulse of 1 to 1.5ms.

8.1.3 RSTN input function

The pin RSTN is monitored by the SBC for external reset events. In order to force an external reset event to the SBC, the LOW period on that pin has to exceed a pulse width of 18µs (see datasheet, $t_{w(rst)}$). For shorter pulses it cannot be guaranteed, that the SBC recognizes this reset event.

Once an external reset is recognized, the SBC will lengthen the RSTN LOW phase to pulse width of 1 … 1.5ms. The reset length timer starts with RSTN detected to be LOW und runs in parallel to the external LOW signal applied to the RSTN pin. Thus, forcing RSTN LOW externally for a time longer than 1.5ms results in an immediate RSTN HIGH transition with releasing the external RSTN signal.

8.2 Wake-up and interrupt event diagnosis via pin RXD in CAN Offline

8.2.1 Overview of events

The UJA1164(A), UJA1167(A), UJA1168(A) and UJA1169 offer the ability to feedback to the application if conditions apply to the SBC which might be important for the application either to provoke a wake-up from Standby or Sleep Mode or signal interrupts to the running application in case certain conditions are changed which e.g. exceed critical values or are important for the application to perform next steps.

Table 12 shows all supported regular wake-up events while Table 13 introduces the interrupt events of the mini high-speed CAN SBC family.

Since the UJA116x family does not provide a dedicated interrupt output pin, the RXD line can be used signaling interrupts and wake-ups with an active LOW signal, if enabled. Please note, that this RXD-based signaling is provided only while the CAN Transceiver has left CAN Active and CAN Listen-only mode.

Table 12. Regular wake-up events

Event	Description	Supported by	Default function after power-on
CAN wake-up (CW)	A CAN wake-up was detected, either - Standard wake-up pattern in CAN Offline or - Selective wake-up frame (1168 or 69/F only if selective wake-up enabled)	all variants	63: always on 64/67/68/69: off
Rising WAKE edge (WPR)	Rising edge on pin WAKE detected	67(A) / 68(A) / 69	off
Falling WAKE edge (WPF)	Falling edge on pin WAKE detected	67(A) / 68(A) / 69	off

Table 13. Interrupt events

Event	Description	Supported by	Default function after power-on
Power-on (PO)	The SBC has left Off mode (Rising BAT voltage passed $V_{th(det)pon}$)	all variants	always on
CAN bus silence (CBS)	No activity on CAN bus for $t_{to(silence)}$	64(A) / 67(A) / 68(A) / 69	off
CAN failure (CF)	A CAN failure was detected, either - CAN transceiver deactivated due to V1 under-voltage (only if CMC = 01) or - CAN transceiver deactivated due to a dominant clamped TXD pin (only captured if CAN in Active mode)	64(A) / 67(A) / 68(A) / 69	off
V1 under-voltage (V1U)	V1 voltage has dropped below 90% of the nominal voltage level (only captured when V1 is active)	64(A) / 67(A) / 68(A) / 69	off
Watchdog Failure (WDF)	A watchdog failure was detected, either - Watchdog overflow or - Watchdog triggered too early in Window mode	64(A) / 67(A) / 68(A) / 69	always on
SPI failure (SPIF)	A SPI failure was detected, either - SPI clock count error or - Illegal WMC, NWP, MC code - Write attempt to locked registers	64(A) / 67(A) / 68(A) / 69	off
Over temperature warning (OTW)	The IC temperature exceeded $T_{th(warn)ot}$	64(A) / 67(A) / 68(A) / 69	off
VEXT / V2 over-voltage (VEXTO / V2O)	VEXT / V2 voltage has exceeded V_{ovd} (only captured when VEXT / V2 is active)	VEXT for 67VX (A/X); 68VX (A/X) VEXT for 69/X ; 69/X/F;69L/X; 69L/X/F V2 for 69; 69/F; 69/3; 69F/3; 69L; 69L/F	off
VEXT / V2 under-voltage (VEXTU / V2U)	VEXT / V2 voltage has fallen below V_{uvd} (only captured when VEXT / V2 is active)	VEXT for 67VX (A/X); 68VX (A/X) VEXT for 69/X ; 69/X/F;69L/X; 69L/X/F V2 for 69; 69/F; 69/3; 69F/3; 69L; 69L/F	off
Partial Networking Frame Detection Error (PNFDE)	Partial networking frame detection error detected (in 68FD (A/F) and 69/F variants only, if selective wake-up enabled)	68FD (A/F); 69/F;	always on

The UJA1163(A) without SPI interface does not support event control and monitoring, but nevertheless supports power-on and CAN wake-up detection in CAN Offline mode.

8.2.2 Event control & detection

Those events which can be enabled or disabled (except PO, WDF and PNFDE) can be controlled via the Event Capture Enable Registers:

- System event capture enable register (0x04)
- Supply event capture enable register (0x1C)
- Transceiver event capture enable register (0x23)
- WAKE pin event capture enable register (0x04)

where a '1' means capturing enabled while a '0' means capturing disabled. In case an enabled capture function detects an event the following happens:

- The relevant event status bit is set (address range 0x61 to 0x64)
- In case CAN is in Offline mode the RXD pin is forced LOW
- If the SBC is in Sleep mode, a transition to Standby mode (via Reset) is performed including activation of the microcontroller supply V1

Monitoring of events can be done by regular polling of the event status bits in the registers 0x61 to 0x64, e.g. when CAN is Active or Listen-only and thus event detection would not generate a LOW level on pin RXD. In order to allow a shorter polling time the SBCs offer the Global Event Status Register at address 0x60, summarizing whether and which of the other registers have an event status bit currently set.

Clearing event status bit in registers 0x61 to 0x64 can be done by writing a 1 to the relevant bit (writing a 0 will have no effect). During one write access also several status bits can be cleared simultaneously, if needed.

8.2.3 Limiting microcontroller disturbance by events

In order to limit the impact on the software processing time, an event delay timer is incorporated for pin RXD. Whenever a pending event status bit is cleared while in CAN Offline mode, pin RXD is released HIGH and an internal delay timer ($t_{d(event)}$) starts running. Pin RXD will not go LOW again before $t_{d(event)}$ overflows even if there is another pending event or a event gets captured just during $t_{d(event)}$. Nevertheless the event status bits can be read and cleared at any time.

The timer gets stopped immediately when pin RSTN goes LOW. In case the SBCs enter Sleep mode the timer is also stopped. If on top at entering Sleep mode an event is still pending this is immediately shown by a LOW level at RXD indicating the wake-up from Sleep as described in the following chapter.

8.2.4 Sleep mode protection

A distinction is made regarding regular wake-up events and interrupts. In order to be able to wake-up SBCs which support a Sleep mode (UJA1167(A), UJA1168(A) and UJA1169) the application needs to enable at least one of the regular wake-up events (via pin WAKE or the CAN bus) before entering Sleep mode in order to avoid a deadlock situation in which the SBC could not be woken up by external sources. Entering Sleep mode successfully requires as well clearing of all pending events before the Sleep mode command is launched.

If one of those two conditions is not met, the UJA1167(A), UJA1168(A) and UJA1169 will perform a system reset with source "Illegal Sleep mode command received" as a reaction on a Sleep mode attempt. For applications, which shall never enter the Sleep mode a dedicated bit in the MTP (SLPC) allows disabling the Sleep mode completely.

8.3 STBN Pin (UJA1163(A) only)

The pin STBN allows direct control of the UJA1163(A) operating mode. A LOW level sets the SBC into Standby Mode. In Standby Mode the CAN Transceiver is not able to transmit or receive data from the CAN lines (CAN Transmitter is off, TXD signals are ignored). Instead, suitable CAN traffic will force a wake-up through CAN, which is signaled with a LOW level on RXD.

Setting STBN to HIGH level activates the CAN transceiver inside of the SBC (Normal Mode), which connects RXD to the bus signal while the CAN transmitter gets activated again. Please note, that there are several conditions to be fulfilled, before active CAN communication is possible through the TXD input pin:

- TXD needs to be HIGH while STBN is HIGH
- CAN start-up time is elapsed ($t_{startup(CAN)}$, max 220µs)
- V1 has to be above the under-voltage detection threshold

This control input line provides an internal pull-down resistor to GND of typically 60kΩ (40 … 80kΩ). The pull-down makes sure, that the SBC disables the CAN transmit capabilities, if that input pin gets accidentally open-circuit on the board.

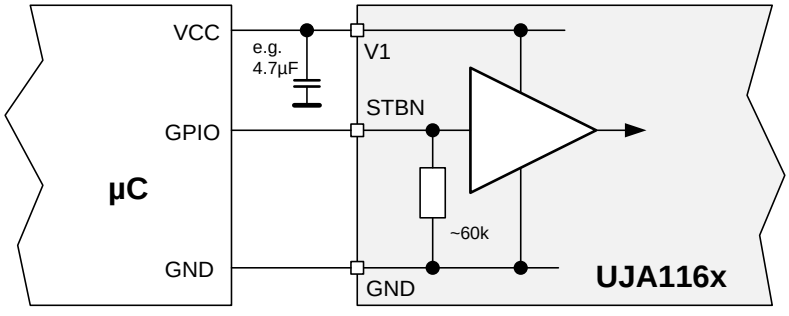


Fig 40. Typical STBN circuitry

8.4 CTS Pin (UJA1163(A) only)

This pin provides optional information about the actual status of the CAN Transceiver. As long as this pin is held LOW by the UJA1163(A), the CAN Transceiver is not able to transmit any data. This information can be used to decide by the application, whether active CAN transmissions can be initiated. In case a CAN transmission would be initiated too early (e.g. after a mode change towards Normal Mode), the CAN protocol controller inside of the microcontroller may run into CAN error handling procedures up to the so-called Bus-Off state because the TXD bit pattern is not reflected back on the bus lines and with that, not on the RXD pin. In order to avoid such unwanted reaction of the CAN controller it is recommended to read-back this signal by the application software before activating any CAN communication. With that the SBC internal $t_{startup(CAN)}$ (max 220µs) can be assessed and shortened individually at start-up of the system.

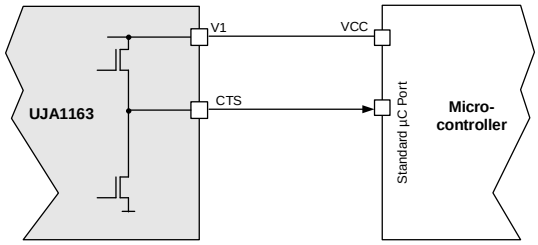


Fig 41. Typical CTS circuitry

8.5 SPI (UJA1164(A) / 67(A) / 68(A) / 69)

The SPI interface is the main communication channel between the SBCs UJA1164(A), UJA1167(A), UJA1168(A) and UJA1169 and the microcontroller. Using the SPI interface, the microcontroller configures the SBCs, reads back status information of the SBCs and triggers the watchdog.

The UJA1163(A) does not offer an SPI interface because its reduced functions can be handled via one mode control input pin (STBN).

8.5.1 Functionality of the SPI pins

The SBCs are controlled via the 4-wire SPI interface as shown in Fig 42. It consists of four digital pins:

- Serial Data Input (SDI)
- Serial Data Output (SDO); floating when SCSN is HIGH
- SPI clock in (SCK); default input level shall be LOW due to low-power-concept
- SPI Chip Select (SCSN); active LOW

The SPI connections can optionally be applied with e.g. 1kΩ series-resistors that may help to reduce EMC emission, especially if there is a long distance between the host controller and the SBC.

To ensure that the SCSN pin and the SCK pin are always on a defined level, the SBCs contain an internal pull-up resistor to V1 at SCSN and an internal pull-down resistor to GND at SCK (both typically with 60kΩ). Pin SDO is driven by an internal push-pull output that is only active if the SCSN pin is LOW. Otherwise the SDO pin is floating. Therefore, it is possible to connect another SPI device in parallel if it has an own chip select pin.

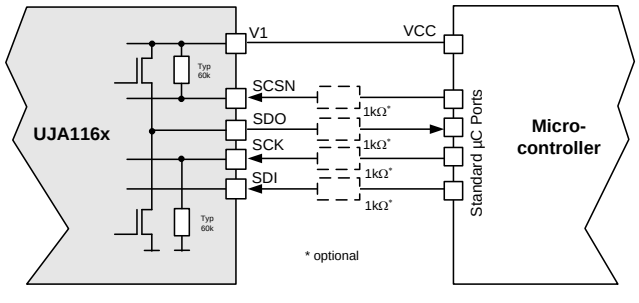


Fig 42. SPI interface

Fig 43 shows an example configuration when an additional SPI device is connected in parallel to the same microcontroller SPI interface. Except for the SCSN all pins can be shared between the SBC and the second slave, provided that the SDO of the second slave is also floating when its SCSN is HIGH. This configuration can be extended by other SPI devices that also have SDO pins with the same characteristic.

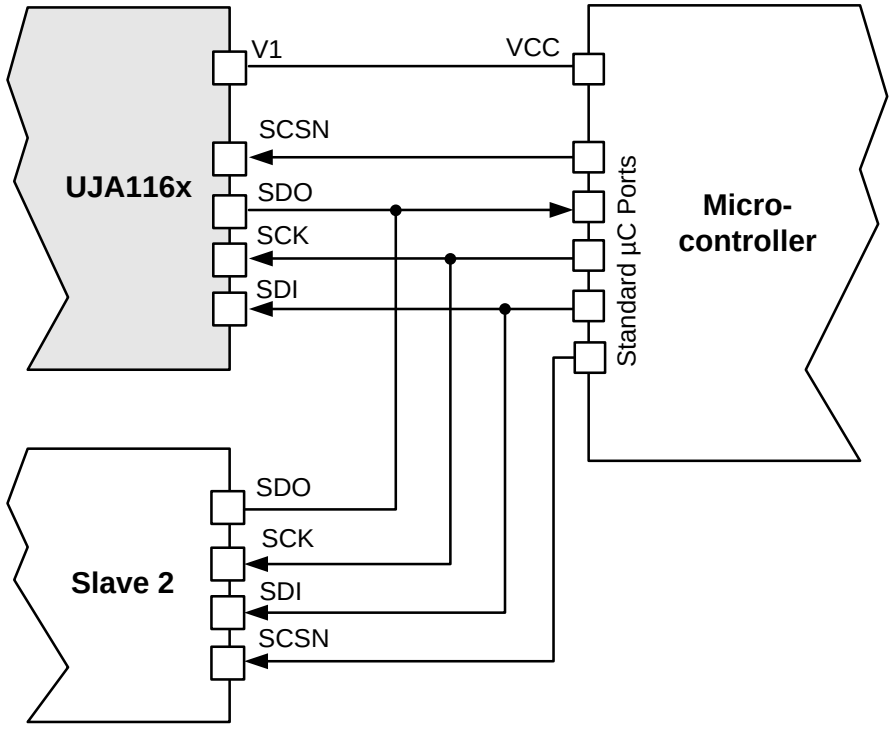


Fig 43. SPI configuration if two slaves are connected to the same MCU SPI Interface

It should be noted, that the microcontroller input/output lines connected to SDO/SDI shall provide a weak pull-up or pull-down behavior in order to avoid a floating net while SCSN is HIGH. If the microcontroller port does not provide such pull-up or pull-down it is strongly recommended to add an external pull-up or –down resistor here in order to avoid extra quiescent current caused by a floating net.

8.5.2 Configuration of the SPI Interface

The UJA116x SPI interface can be used for 16-, 24- or 32 bit SPI read/write accesses. The UJA116x tolerates also SPI messages with more than 32 bits during a read operation, but only the first 32 bits are considered. In this case the SDI is reflected on SDO from bit 33 onwards. SPI messages with less than 16 bits are completely ignored.

According to Fig 44 the SBC shifts data with the rising edge and samples with the falling edge of the pin SCK. The initial setting on the microcontroller side of SCK when SCSN goes down shall be LOW. A HIGH level is tolerated as well, if the SPI Lead time as defined in the data sheets is guaranteed. Furthermore, the SBC expects that the most significant bit is sent first. Any SPI access is a bidirectional data transfer. As one bit is written into SDI, another bit is shifted out of SDO.

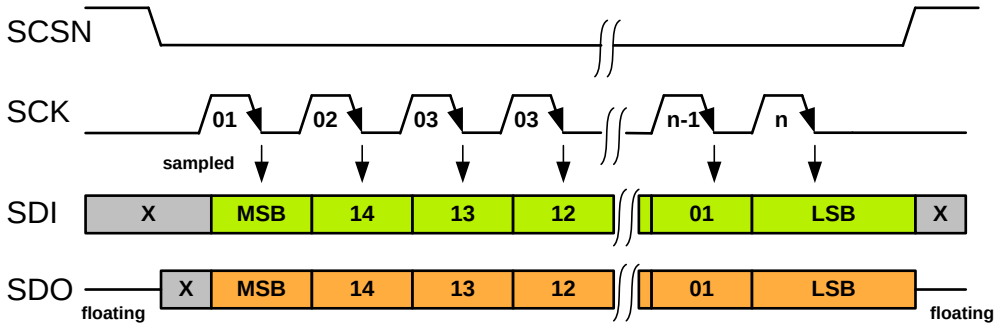


Fig 44. Configuration of SPI interface, example with 16-bit access

8.5.3 SPI register architecture

The SPI allows for full duplex data transfer, meaning that status information is returned when new control data is shifted in. Fig 45 shows the register structure of the UJA116x SBCs. The upper seven bits of the 16-, 24- or 32-bit SPI message determine which register is addressed. Bit number 8 contains the ‘Read-Only’ bit (the LSB). The ‘Read Only’ bit (RO), determines whether something is actually written into the addressed register(s) or not. Hence, this bit allows a read-only access option where registers are read back by the application without changing the register content. If this bit is set to 1 the SPI transfer is a read-only access and all data bits (bit 0 to n) written into SDI are ignored. If the RO bit is 0, the data bits (bit 0 to n) are written into the addressed register. The written data become valid as soon as the SCSN pin returns back to HIGH level.

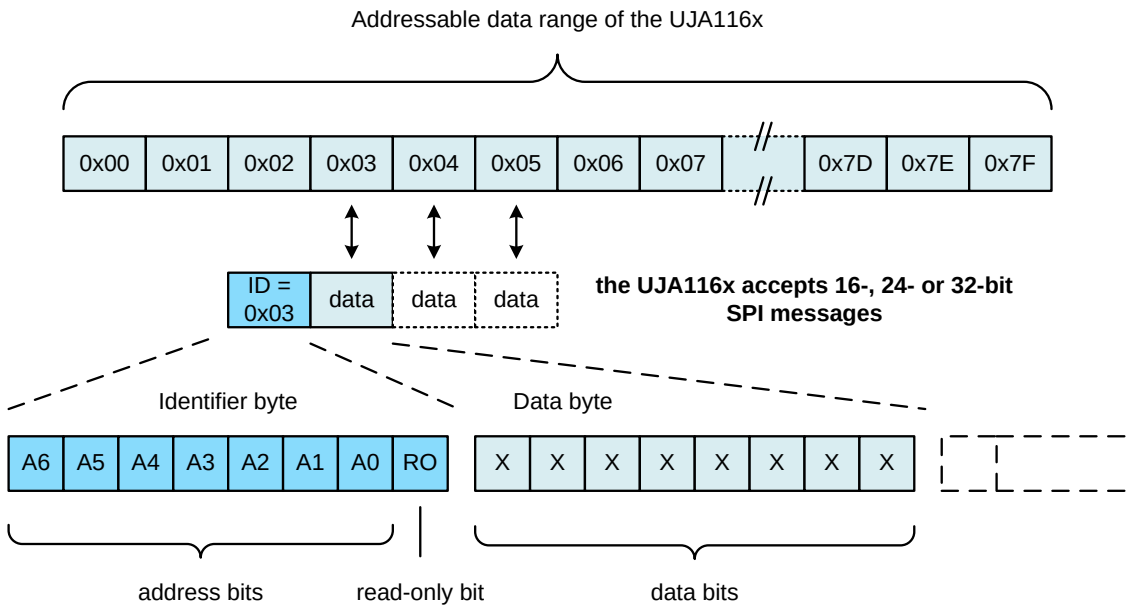


Fig 45. Structure of SPI register

Within a **16-bit SPI** access, the first 7 bits determine the addressed register; bit number 8 determines whether a read-only or read/write access is request. Byte two (bits 9 to 16) represents the data to be written into the addressed register in case of RO = 0.

Within a **32-bit SPI** access the first 7 bits determine the first addressed register; bit number 8 determines whether a read-only or read/write access is request. Bytes two to four (bits 9 to 32) represent the data to be written into the addressed registers in case of RO = 0. The register address is automatically incremented.

The UJA116x also tolerates attempts to write to registers that do not exist. The corresponding data is lost in that case. If the available address space is exceeded during a write operation (possible only with a 24 or 32 bit access), the data overflows into address 0x00 and potentially the following addresses.

During a write operation, the UJA116x SBCs monitor the number of SPI bits transmitted. If the number does not fit 16, 24 or 32, then the write operation gets aborted and an SPI failure event is captured in the SPIF (SPI Failure) bit in the System event status register (address 0x61) if the according event capturing got enabled by the SPIFE (SPI Failure Enable) bit.

Remark: An SPI Failure event is also captured in case of writing an illegal code to the MC (Mode Control) bits as well as with the attempt to write access to a locked register. An SPI failure is not captured in Sleep mode (see chapter 8.2 for more details on failure event detection).

The following tables give an overview on the SPI register map of the UJA116x SBC family. Note that the SPI addresses and bit positions are the same for equal functionalities in the complete UJA116x SBC family as well as within the standalone high-speed transceiver for partial networking TJA1145 (family approach; also NXPs UJA113x family offers the same main SPI register architecture). For devices offering more functionality (like the

UJA1168(A) and UJA1169 with partial networking) SPI register address ranges used for partial networking configuration are ‘reserved’ areas in smaller devices like the UJA1163(A) or UJA1167(A).

Table 14. General Register Map

Address Bits A6 to A0		Register (Read/Write depending on RO)
Primary Control Registers		
0x00	000 0000	Watchdog Control
0x01	000 0001	Mode Control
0x02	000 0010	Fail-safe control (UJA1169 only)
0x03	000 0011	Main Status
0x04	000 0100	System Event Enable
0x05	000 0101	Watchdog Status
General Purpose Memory and Lock Control Registers		
0x06	000 0110	Memory 0
0x07	000 0111	Memory 1
0x08	000 1000	Memory 2
0x09	000 1001	Memory 3
0x0A	000 1010	Lock Control
Supply Control Registers		
0x10	001 0000	Regulator Control // V1 and INH/V2/VEXT Control
0x1B	001 1011	Supply Status
0x1C	001 1100	Supply Event Enable
CAN Transceiver Registers		
0x20	010 0000	CAN Control
0x22	010 0010	Transceiver Status
0x23	010 0011	Transceiver Event Enable
Event Capture Registers		
0x60	110 0000	Global Event Status
0x61	110 0001	System Event Status
0x62	110 0010	Supply Event Status
0x63	110 0011	Transceiver Event Status
Other Registers (MTPNV memory, Identification)		

Address Bits A6 to A0		Register (Read/Write depending on RO)
0x70	111 0000	MTPNV Status
0x73	111 0011	Startup Control
0x74	111 0100	SBC Configuration Control
0x75	111 0101	MTPNV CRC Control
0x7E	111 1110	Identification

Table 15. WAKE Pin Register Map (UJA1167(A), UJA1168(A) and UJA1169xx only)

Address Bits A6 to A0		Register (Read/Write depending on RO)
WAKE Pin Registers		
0x4B	100 1011	WAKE Pin Status
0x4C	100 1100	WAKE Pin Enable
0x64	110 0100	WAKE Pin Event Status

Table 16. Partial Networking Register Map (UJA1168(A) and UJA1169/F variants only)

Address Bits A6 to A0		Register (Read/Write depending on RO)
CAN Partial Networking Registers		
0x26	010 0110	Data Rate
0x27	010 0111	Identifier 0
0x28	010 1000	Identifier 1
0x29	010 1001	Identifier 2
0x2A	010 1010	Identifier 3
0x2B	010 1011	Mask 0
0x2C	010 1100	Mask 1
0x2D	010 1101	Mask 2
0x2E	010 1110	Mask 3
0x2F	010 1111	Frame Control
0x68	110 1000	Data Mask 0
0x69	110 1001	Data Mask 1
0x6A	110 1010	Data Mask 2

Address Bits A6 to A0		Register (Read/Write depending on RO)
0x6B	110 1011	Data Mask 3
0x6C	110 1100	Data Mask 4
0x6D	110 1101	Data Mask 5
0x6E	110 1110	Data Mask 6
0x6F	110 1111	Data Mask 7

9. CAN transceiver interface

9.1 High speed CAN basics

The core function of all the mini high speed CAN System Basis Chips is transmission and reception of CAN signals via the two bus pins CANH and CANL and to the protocol controller via the pins TXD and RXD.

The protocol controller outputs a serial transmit data stream to the TXD input of the SBC. An internal pull-up function sets the TXD input to logic HIGH, which means that the bus output driver stays recessive in the case of a TXD open circuit condition. In the recessive state (Fig 46) the CANH and CANL pins are biased to a voltage level of V1 (or V2 in case of the UJA1169, UJA1169/F, UJA1169/3, UJA1169/F/3, UJA1169L and UJA1169L/F) divided by 2. If a logic LOW level is applied to TXD, the output stage is activated, generating a dominant state on the bus line (Fig 46).

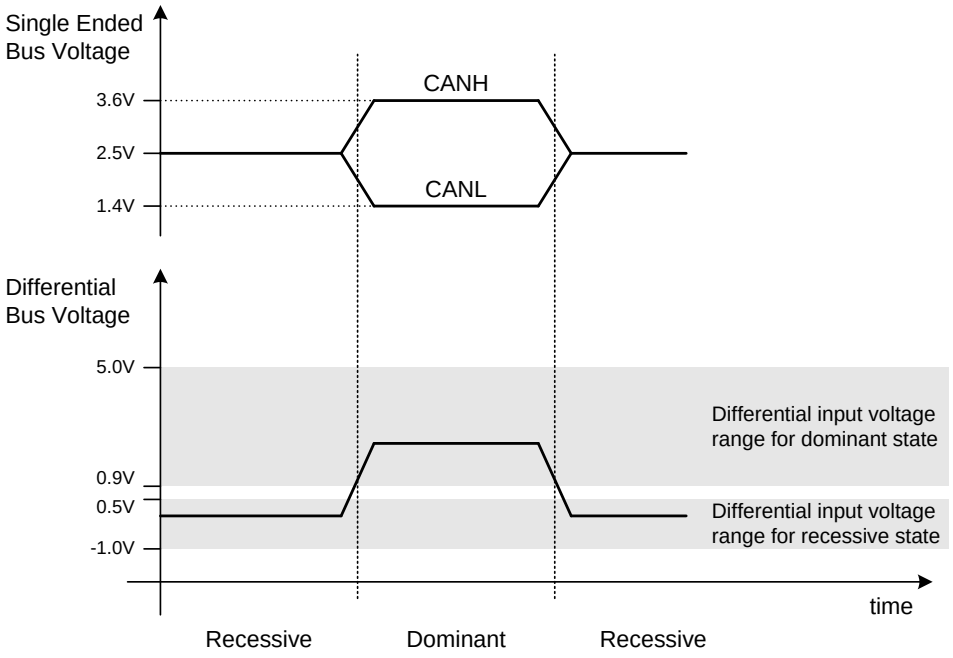


Fig 46. Nominal bus levels according to ISO11898

The receiver converts the differential bus signal to a logic level signal, which is output at RXD. The internal receiver comparator is always active. It monitors the bus while the bus node is transmitting a message. This is required to support the non-destructive bit-by-bit arbitration scheme of CAN.

Details about high speed CAN applications in general are explained in the NXP application hints document “Rules and recommendations for in-vehicle CAN networks” [8].

9.2 Autonomous CAN voltage biasing

High speed CAN transceivers and SBCs which are in a low-power mode according the ISO11898-5:2007 always terminate their bus pins CANH and CANL to GND level (0V). In case of dominant bits on the bus provided by another CAN node each time a common mode step is enforced increasing the entire emission of the communication system.

In order to minimize these unwanted common mode steps the new ISO standard ISO11898-6:2013 introduced “autonomous CAN voltage biasing”. Transceivers and SBCs according to this new standard have to support this functionality.

The device only terminates its CAN bus pins to GND while

- the CAN block is in a low-power mode and
- the bus is idle for longer than approximately one second.

Otherwise the CAN bus pins bias towards 2,5V (Note: Depending on the overall device operating mode, the 2.5V are derived directly from BAT or from the CAN supply voltage).

Each time there is traffic on the bus (see Fig 47) an internal timer is reset and the bus pins bias towards 2.5V. At bus silence the timer starts counting until about one second. After this silence time the bus biasing changes towards 0V. In the example below only a dedicated wake-up message leads to a wake-up of the device resulting in a LOW level on pin RXD and entering Standby mode.

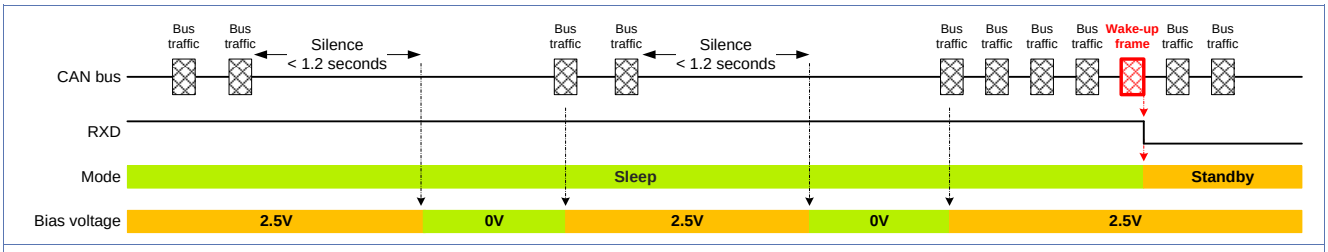


Fig 47. Autonomous bus biasing

The UJA1163(A), UJA1164(A), UJA1167(A), UJA1168(A) and the UJA1169 offer the autonomous biasing functionality to minimize emission in the communication system. A state diagram for the autonomous biasing feature is shown as well in Fig 50.

9.3 CAN Partial Networking

Besides autonomous biasing, the core feature of the ISO11898-6:2013 standard is the “selective wake-up” functionality of a CAN device in order to allow “partial networking” in a CAN bus system.

Partial networking is the ability of a network to allow only a sub group of nodes to actively communicate, while the remaining nodes are inactive and in a low-power mode watching the bus traffic for a wake-up message. Upon reception of a wake-up message the CAN device can activate the entire node. Such wake-up messages may address nodes individually or as a group. The functionality, which is needed in the transceivers for this kind of network operation, is called “selective wake-up”.

The decision to stop active communication of a node needs to be made on application software level and is thus controlled by the microcontroller and not by the CAN device.

Partial Networking is to support following use cases:

1. Saving power and reducing CO_2:

   CAN nodes which offer functionality which is not constantly required like e.g. auxiliary heating, seat heating, and trailer interface can be set into Sleep mode with selective wake-up instead of being active on the bus and wasting power.

2. Minimizing wake-up lines and relays:

   In today’s cars partially used CAN nodes are activated / deactivated by additional wake-up lines and relays (un-powering nodes). Using partial networking allows getting rid of this extra hardware and wiring, reducing cost, weight and enabling higher flexibility in terms of partial networking use case scenarios.

3. Reducing ECU operation and up times:

   Partially running the CAN bus nodes (except of the CAN transceiver) in Sleep mode reduces the up time of components in the module like voltage regulators, capacitors, microcontrollers. This offers a high advantage especially for hybrid and electrical vehicles, where the battery charging time adds to the driving cycle. By use of partial networking it may be avoided to specify longer up times for modules that do not need to take part in the communication related to battery charging.

All UJA1168(A) and UJA1169/F variants offer the selective wake-up functionality to support and build up partial networking networks.

Further details about partial networking are explained in the NXP application hints document “Partial Networking in high speed CAN networks” [9].

9.3.1 CAN FD passive

In 2012, Bosch proposed a new frame format called CAN FD that allows more than 8 bytes of data per frame and moreover a higher bit rate in the data field than in the arbitration field. This is not backward compatible to ISO11898-1 classic CAN format (defining the CAN protocol) and thus CAN FD frames cannot be decoded by partial networking transceivers according to that frame format. A potential CAN FD frame would cause internal format errors within a typical partial networking capable transceiver and thus, wake-up in case of too many CAN FD frames on the bus. The wake-up happens intentionally, because there are lots of obviously corrupt frames (here CAN FD frames) on the bus which might be an indicator for a wrongly configured partial networking transceiver.

To facilitate simple migration towards CAN FD adoption, NXP offers an innovative new feature, used in combination with partial networking. This allows CAN nodes which only

support classic high speed CAN controllers to remain in sleep or standby while CAN FD frames are transmitted on the bus, without generating bus errors. An ISO11898-6:2013 (partial networking) compliant device still can be woken by the configured wake-up frames according ISO11898-1 classic CAN format.

CAN FD passive CAN modules, which are not equipped with a CAN FD capable CAN controller, can be set to Sleep or Standby, while other nodes communicate by means of CAN FD frames. Offering CAN FD tolerance is the only way to operate a network with a mixture of CAN and CAN FD nodes. The CAN FD tolerance feature can be enabled through SPI with a dedicated bit within the CAN Control Register (CFDC).

The devices UJA1168/FD (A/F), UJA1168VX/FD (A/X/F) and all UJA1169/F variants offer CAN FD tolerance via the CAN FD passive feature in order to allow passive behavior in other nodes send CAN FD frames on the bus.

Further details about CANFD tolerance are explained in the NXP application hints document “Partial Networking in high speed CAN networks” [9].

9.4 CAN transceiver operating voltage range

All mini high speed CAN System Basis Chips include a high speed CAN transceiver compliant to the ISO11898-2:2003 and ISO 11898-5:2007 standards. Further on the UJA1168(A) and UJA1169/F variants are on top of that compliant to the ISO11898-6:2013 standard.

The CAN transmitter is supplied by the internal V1 regulator or the dedicated V2 regulator in the UJA1169, UJA1169/F, UJA1169/3 and UJA1169/F/3 variants. Fig 48 shows the operating voltage range for the CAN transmitter. The CAN transmitter is fully specified between $4.75V \leq V_{V1} \leq 5.5V$ for a CAN termination between 45Ω and 65Ω. During CAN Active mode also the recessive 2.5V bias voltage is derived from this supply.

The CAN receiver is supplied directly from the BAT supply pin.

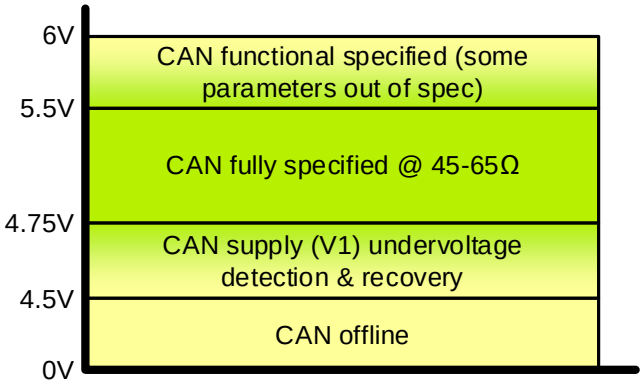


Fig 48. CAN transmitter operating range

Please note, that the CAN block makes use of a dedicated under-voltage comparator assigned to the CAN block only. Thus the CAN under-voltage detection works independent from the V1 or V2 under-voltage detection.

Besides this, there is as well an undervoltage detector on the pin BAT of the SBC. If BAT falls below that voltage, the CAN transceiver disengages from the bus lines getting high-ohmic with respect to GND.

9.5 CAN transceiver operating modes

The SBCs CAN transceiver supports different CAN operating modes depending on the SBC mode, the CAN mode control (CMC) bit settings and certain conditions like supply voltage conditions on V1 and BAT and the device temperature. The table below shows an overview in which SBC modes in combination with the CMC settings certain CAN modes a selected. For details please refer to the CAN state diagrams in the datasheets of the mini high-speed CAN SBC family.

9.5.1 Active mode

The CAN Transceiver is in Active mode if

- The SBCs are in Normal mode (MC = 111) AND
- The CAN transceiver has been enabled (CMC = 01 or 10) AND
- The CAN supply voltage is above the 90% threshold while CMC = 01

  (Provided that BAT<$V_{th(uvd)CAN}$ and there is no over temperature condition)

In CAN Active mode the CAN transceiver is enabled and thus, data can be transmitted and received.

9.5.1.1 CAN transmitter status check in Active mode

In order to check whether the transmitter is active already (e.g. during start-up), the application can read the CAN transmitter status through bit CTS in the Transceiver Status Register. If bit CTS = 1, the CAN transmitter is enabled and ready to transmit data on the bus. Within the UJA1163(A) this bit is made transparent on the CTS pin.

9.5.1.2 TXD clamping check in Active mode

In order to prevent a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications), the SBCs offer two safety features during CAN Active mode selection:

- Entering CAN Active is possible only while the TXD pin is HIGH. If pin TXD pin is LOW at CAN Active selection, the SBCs will not enable the transmitter until TXD was first released HIGH again. The UJA1163(A) will on top also keep the receiver disabled in this case until TXD was first released HIGH again.
- During CAN Active, a LOW level on pin TXD that persists longer than $t_{to(dom)TXD}$ will disable the transmitter, releasing the bus lines to recessive state.

  If the TXD dominant timeout time is exceeded, this will be indicated as well as a CAN failure in bit CFS in the Transceiver Status Register. Additionally, the CF bit in the Transceiver event status register will be set in case this interrupt is enabled via bit CFE.

Note that pin TXD is internally pulled-up (towards V1) to ensure a recessive condition in Active mode on the bus in case the pin is left floating.

The above mentioned TXD dominant protection feature ($t_{to(dom)TXD}$ = 2.7ms MIN) limits the suitable CAN bus speed to about 4.4kBit/s MIN. Below such a CAN speed, normal CAN communication might trigger this time out and with that, may corrupt the running CAN communication. For baud rates above 4.4kBit/s the timer has no impact except of providing a protection against erroneous signals applied to the TXD pin of the SBC.

(Background: 12 dom bits in a row < 2.7ms; Min Baud Rate = 12/2.7ms =4.4kBit/s)

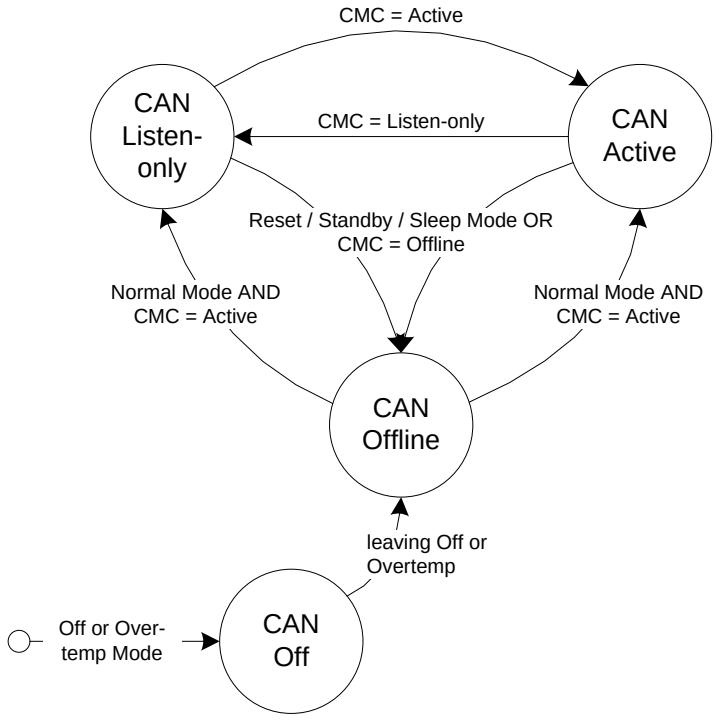


Fig 49. Simplified CAN state diagram (while FNMC = 0)[1]

9.5.2 Listen-only mode

The CAN Transceiver is in Listen-only mode if:

- The SBCs are in Normal mode (MC = 111) AND
- The CAN receiver only has been enabled (CMC = 11)

  (Provided that BAT<$V_{th(uvd)CAN}$ and no over temperature condition consists)

In CAN Listen-only, the normal CAN receiver is enabled while the CAN transmitter is disabled.

This facility could be used by development tools that need to listen to the bus, but do not need to transmit or receive data or for software driven selective wake-up. Dedicated microcontrollers could be used for selective wake-up, providing an embedded low power CAN engine designed to monitor the bus for potential wake-ups.

Note that the UJA1163(A) does not support an SPI interface and thus the selection of the Listen-only mode is not supported by the UJA1163(A).

Users of the UJA113x SBC family might be used to the option, that the Listen-only mode can be entered as well during Standby Mode of the SBC. This is not possible with the UJA116x family due to the fact, that the UJA116x family does not provide a dedicated interrupt pin for event signaling. Since the RXD pin function is used for event signaling, the RXD is already blocked and cannot be used to support a CAN listen only behavior. With that, the Listen-only mode of the CAN Transceiver is limited to the Normal operating mode of the SBC.

[1] Note: the UJA1163 does not support SBC Sleep Mode and the internal CMC setting is always Active

9.5.3 Offline mode with autonomous bus biasing

The CAN Transceiver is in Offline mode if

- The SBCs are in Reset / Standby / Sleep mode OR
- CAN has been actively disabled (CAN = 00) OR
- The CAN supply is below 90% of its nominal value while CMC = 01

  (Provided that BAT<$V_{th(uvd)CAN}$ and no over temperature condition consists)

In CAN Offline mode, the transceiver monitors the CAN bus for a wake-up, provided CAN wake-up detection is enabled (CWE = 1) in the Transceiver Event Enable Register.

As indicated in chapter 9.2, all mini high-speed CAN SBCs offer autonomous bus biasing. The device only terminates its CAN bus pins to GND while

- CAN is Offline mode AND
- The CAN bus is idle for longer than $t_{to(silence)}$, which is approximately one second.

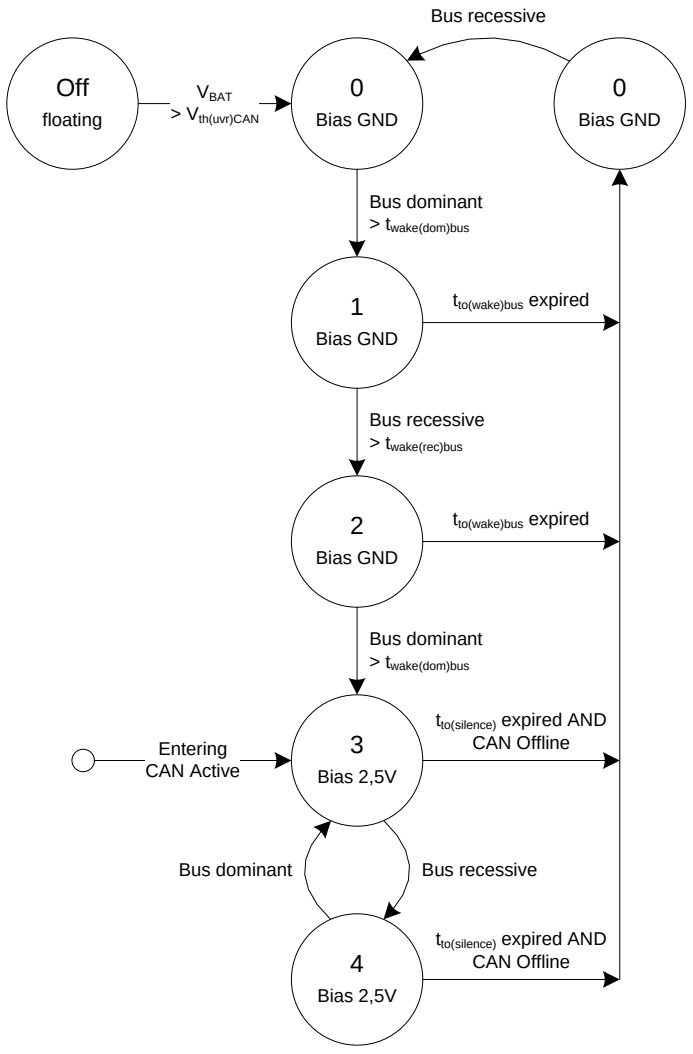
Otherwise the CAN bus pins bias towards 2,5V. See Fig 50 for the autonomous bus biasing principal.

9.5.3.1 Entering Sleep mode at CAN bus silence only

If the $t_{to(silence)}$ timer is exceeded, this will be indicated in bit CBSS in the Transceiver Status Register. Additionally, the CBS bit in the Transceiver event status register will be set in case this interrupt is enabled via bit CBSE.

The CAN bus silence event capturing can be useful in case an SBC is set to Standby mode while CAN traffic persists in order to allow a quick start-up of the application if needed.

When CAN traffic is stopped entirely for $t_{to(silence)}$, the SBC might react by setting the SBC into lowest power Sleep mode, which means a longer start-up time of the application because of an unsupplied microcontroller.



$t_{to(wake)bus}$ = ~700us

$t_{wake(dom)bus}$ = $t_{wake(rec)bus}$ = 0.5µs to 3µs

$t_{to(silence)}$ = ~1s

Fig 50. Autonomous bus biasing

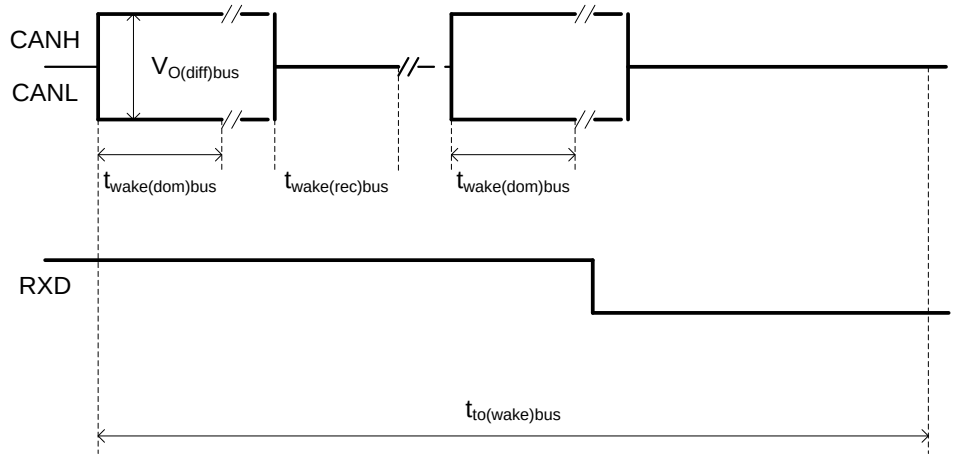
9.5.3.2 Standard CAN wake-up in Offline mode

A dedicated wake-up sequence (specified in ISO11898-5) must be received to wake-up the SBCs from Standby or Sleep mode and also to activate CAN biasing to 2,5V. This filtering improves the robustness against spurious wake-up events due to a dominant clamped CAN bus or dominant phases caused by noise or spikes on the bus.

The wake-up pattern consists of the following sequence on the bus:

- A dominant phase of at least $t_{wake(busdom)}$
- A recessive phase of at least $t_{wake(busrec)}$
- A dominant phase of at least $t_{wake(busdom)}$

The complete dominant-recessive-dominant pattern must be completed within $t_{to(wake)}$ to be recognized as a valid wake-up pattern (see Fig 51). Otherwise, the internal wake-up logic gets reset and the complete wake-up pattern needs to be re-applied to the low power CAN receiver in CAN Offline mode before generating a proper remote wake-up. Pin RXD will remain recessive until the bus wake-up event has been triggered.



$t_{to(wake)bus}$ = ~700us

$t_{wake(dom)bus}$ = $t_{wake(rec)bus}$ = 0.5µs to 3µs

Fig 51. Standard wake-up timing

9.5.3.3 Selective CAN wake-up in Offline mode

The selective wake-up capability is only offered in the UJA1168(A) and UJA1169/F variants. In case of a UJA1168(A) or UJA1169/F with selective wake-up enabled in Standby or Sleep mode, the autonomous biasing is still active as described in the previous chapter upon reception of a standard CAN wake-up.

Nevertheless, this does not lead to trigger a bus wake-up until a so-called complete CAN wake-up frame is detected that fits to the pre-configuration in CAN partial networking registers of the UJA1168(A) and UJA1169/F.

Further details about partial networking and the configuration capabilities of the UJA1168(A) and UJA1169/F are explained in the NXP application hints document "Partial Networking in high speed CAN networks" [9].

9.5.4 Off mode

The CAN Transceiver is in Off mode if the SBC is in Off or Overtemp mode. In CAN Off mode the transceiver is switched off completely with the bus lines floating in order to behave passive to the remaining bus, e.g. if the ECU is unsupplied, but still physically connected to the bus.

9.5.5 CAN supply undervoltage detection

Undervoltage on the CAN transceiver supply can be detected depending on the settings of the CMC bits in CAN Active:

- CMC = 01 → CAN Active (with V_{CAN} undervoltage detection enabled)
- CMC = 10 → CAN Active (with V_{CAN} undervoltage detection disabled)

Hint: V_{CAN} supply depends on the used derivative and may be supplied from V1 or V2 internally of the SBC. As such, a V_{CAN} undervoltage may come in conjunction with a V1 undervoltage event, if CAN is supplied from V1.

Option 1: CMC = 01 → undervoltage detection enabled

In case the CAN transceiver is in Active mode, thus the transmitter and receiver are enabled and the CAN supply decreases below 90% of its nominal value the SBCs take the following consequences:

- The CAN transmitter and receiver get disabled → CAN Offline mode entered
- The VCAN supply bit in the Transceiver Status Register indicates an undervoltage (VCS = 1)
- The CF bit in the Transceiver event status register will be set in case this interrupt is enabled via bit CFE.

On the automatic recovery of the CAN supply above the 90% threshold, CAN Active get entered again and the VCAN bit gets cleared automatically.

This feature can be used for automatic disabling the CAN transmitter in case the CAN supply leaves its allowed operating range and thus the bus level schemes on the CAN bus do not fully comply to the parameters as being requested by the ISO11898-5 any longer.

Remark: When the transmitter gets disabled due to a CAN supply undervoltage condition while

- a dominant condition on pin TXD is applied and
- CFE = 1 event is enabled than

pin RXD gets HIGH for ~8us (CAN transmitter got disabled) until RXD gets LOW again, indicating the captured interrupt of the CAN undervoltage and/or the CAN failure. This makes sure, that an edge event is generated on the pin RXD.

Option 2: CMC = 10 → undervoltage detection disabled

In case the CAN transceiver is in Active mode, thus the transmitter and receiver are enabled and the CAN supply decreases below 90% of its nominal value the SBCs take the following consequences:

- The CAN transmitter and receiver stay enabled until
  - the transmitter is no longer capable of transmitting bits on the CAN bus because of a too low CAN supply or
  - the CAN transmitter gets automatically disabled when the V1 undervoltage reset threshold gets passed (selection of 60% / 70% / 80% / 90% level possible) and Reset mode is entered with CAN Offline
- Both, VCS and CF, do not react on an undervoltage with CMC = 10

This feature can be used in case CAN shall still be functional as long as possible below the 90% nominal value even without guaranteeing the voltage scheme as requested by the ISO11898-5.

9.6 CAN transceiver RXD/TXD interface

The RXD and TXD wires are used for the serial communication between the CAN protocol controller and the UJA116x (see Fig 52). These connections can optionally be applied with e.g. 1kΩ series-resistors for filtering noise. But note that the series-resistors can have a negative impact on the loop delay. Engineers are advised to always refer to the individual OEM hardware specifications.

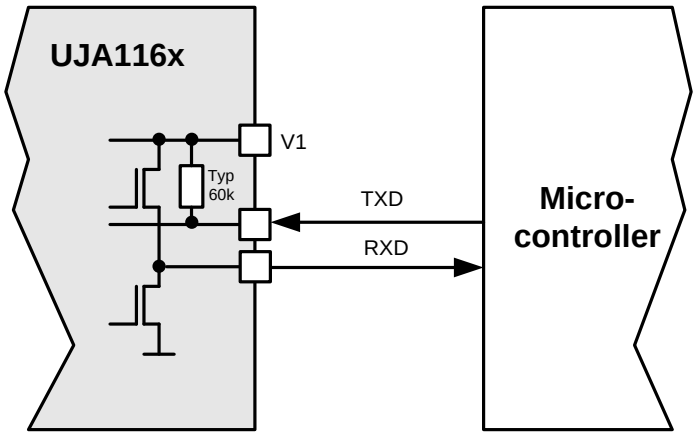


Fig 52. CAN transceiver RXD / TXD interface

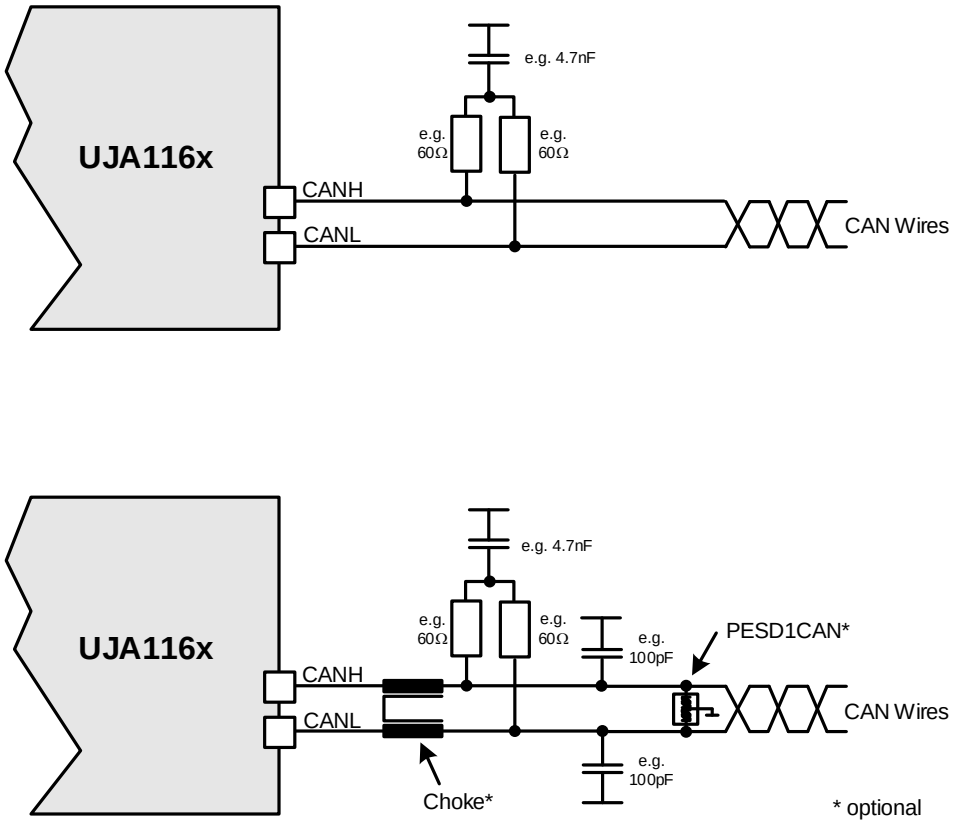
9.7 CAN bus termination

In general, the termination circuitry of the CAN bus shall be designed according to the specification of the car manufacturer.

The two figures below show two examples of a CAN bus termination. On the top a minimum Split termination is shown with two 62Ohm resistances in between CANH and CANL with a 4,7nF capacitance at the center tap. This minimum Split termination approach is recommended for proper CAN bus performance.

On the bottom, an additional common mode choke reduces emission and improves immunity against common mode disturbances and ESD. If recommended by the car manufacturer, a common mode choke can be used to reduce the impact of RF-interferences.

Further details about high speed CAN termination is explained in the NXP application hints document “Rules and recommendations for in-vehicle CAN networks” [8].



(1) Top: example for minimum circuitry needed for full CAN bus functionality

(2) Bottom: example for maximum circuitry with use of common mode choke and ESD protection

Fig 53. Typical Application of the CAN bus pins

9.8 CAN ESD protection

The UJA116x is designed to withstand ESD pulses up to 8kV according to the Human Body Model (HBM, C = 100pF, R = 1.5kΩ) and at least 6kV according to the IEC61000-4-2 (C = 150pF, R = 330Ω) at the bus pins CANH, CANL and thus, typically does not need further external measures. Nevertheless, if higher protection is required, external clamping circuits can be applied to the CANH and CANL line, e.g. PESD1CAN or PESD2CAN (see Fig 53). The IBEE ESD measurements were performed without external bus filters at CANH and CANL and confirmed an ESD robustness for pulses even higher than 6kV according to IEC61000-4-2 (C = 150pF, R = 330Ω).

For the very specific DCC test pulse defined at General Motors, the external PESD1CAN diode is recommended although the UJA116x family members sometimes survive this special test without external protection diodes. Nevertheless for a safe design, it is recommended to have the landing spot for the protection device prepared for this specific customer.

9.9 CAN Transceiver supply current

In order to thermally estimate the impact of the CAN Transceiver supply current, following conditions have to be taken into account:

- A CAN Frame does not consist of dominant bits only
- A node is sending bus traffic with a certain repetition rate (not 100%)
- At start-up of a CAN network there might be temporarily a higher transmission rate, because there is no partner on the bus giving an Acknowledge
- Bus Failure scenarios like bus shorts

9.9.1 CAN - Average supply current during active sending, no fault

The CAN Transceiver supply current strongly depends on the state of the CAN Transmitter. This current is quite low during recessive bus state and increases significantly during dominant bit phases. Furthermore the dominant current reduces again during the so-called “Arbitration Phase”, if many nodes are sending simultaneously. The highest current is appearing after the arbitration phase, which is mainly the data phase and the CRC sequence.

For thermal considerations the average current over time is relevant and can be calculated as follows from the data sheet parameters:

- Additional current for CAN Active Mode, recessive, 4mA TYP / 7.5mA MAX
- Additional current for CAN Active Mode, dominant, 46mA TYP / 67mA MAX

The CAN protocol does not allow to send a permanent dominant signal. At minimum the bit stuffing makes sure, that there are level changes every 5 bit times. A real worst case frame will never drive more than about 80% of the time dominant to the bus. As such, the CAN supply is loaded during active frame sending with an average current of:

$$I_{AverageFrame} = I_{Dom} \times 0.8 + I_{Rec} \times 0.2 = 46mA \times 0.8 + 4mA \times 0.2 = 37.6mA\ (TYP)$$

9.9.2 CAN – Frame repetition rate

A CAN node will not be able to send without any recessive gap between frames. The inter frame space it at least 11 bit times long. Furthermore there are other nodes in the system, which from time to time are sending. On top of that, OEMs are not loading their bus systems with 100% of CAN traffic in order to cope with temporary peak or alarm situations. A typical limit of CAN systems is about 50% loading of the bus system with active traffic.

Assuming 10 nodes in a bus system sharing the available air time on the bus plus the fact, that there is just 50% of the time available for active sending, the overall contribution of one node to the communication time is

$$FrameSendingRate = \frac{50\%}{10\ nodes} = 5\%\ per\ node$$

9.9.3 CAN – Average current while sending, normal operation

Based on that frame sending rate of a single node the overall average current of a CAN Transceiver can be calculated as follows:

$$I_{Average} = I_{AverageFrame} \times FrameSendingRate + I_{Rec} \times (100\% - FrameSendingRate)$$

$$I_{Average} = 37.6mA \times 5\% + 4mA \times 95\% = 5.68\,mA\ (TYP)$$

So, from thermal perspective a CAN node is loading the supply with about 5.68mA only while the regulator has to deliver about 37.6mA while the frame is running. Depending on the buffer capacitor connected to the regulator, the peak load current to the regulator is even lower than 37.6mA while actively sending, because that current is delivered out of the capacitor. The bigger the capacitor, the lower the peak load current. The overall average stays the same. As such, the number of CAN transceivers being able to be supplied from one regulator can be influenced with the buffer cap.

9.9.4 CAN – Average current while sending, wake-up of system

An exceptional operating use case is a node waking up the CAN system the first time. If such a “waking node” is sending out the very first frame on the bus lines, there is no counterpart active yet on the bus lines. As a consequence of that, the waking CAN frame will not be acknowledged by the system and the sending node is automatically repeating the wake-up frame after error handling. This results in a short period of higher frame repetition rate of this waking node. Depending on the reaction speed of the other nodes connected to the system, this node repeats the wake-up frame several times in a row.

For typical CAN networks a MAX reaction time upon bus wake-up is defined, which limits such an exceptional start-up period to some 100ms MAX. As such, it is thermally not really relevant.

A potential failure case might be a disconnected CAN bus during such a wake-up trial. If that waking ECU would be the node carrying the CAN bus termination resistors, this node would try to repeat the wake-up frame forever, because it can read back the CAN signal on RXD (as a consequence of the local bus termination). There is never an acknowledge from the bus lines nor does the node enter the Bus-Off State. In order to mitigate such an exceptional case it might be useful monitoring in the application software, whether the wake-up frame was send out successfully within a reasonable time (e.g. some 100ms) in order to avoid a permanent sending of frames, which just lead to increased system power dissipation.

Since CAN frames cannot be send out without the so-called “Inter Frame Space”, the average sending current is reduced a bit, if there is no ACK from the bus lines received:

$$I_{Wakeup} = I_{AverageFrame} \times 95\% + I_{Rec} \times (100\% - 95\%)$$

$$I_{Wakeup} = 37.6mA \times 95\% + 4mA \times 5\% = 35.92mA\ (TYP)$$

9.9.5 CAN – Average current during bus short circuits

In general the CAN driver stage of a transceiver is current limited. Car makers have explicitly defined such a current limit in order to have no infinite currents on the CAN wires and termination if it comes to CAN bus shorts. This limit is in the order of 115mA according to latest definitions in the ISO11898-2:2015 CAN standard.

For the UJA116x family we defined an even lower short circuit current of MAX 55mA.

There are only a few short circuit situations, which allow a higher current to flow in the CAN drivers as there are:

- CANH to GND
- CANL to GND (from CANH through the termination resistor to GND)
- CANH to CANL (from CANH through CANL driver to GND)

For some of these short circuits, the CAN protocol engine would respond quite rapidly with a so-called Bus-Off state, which ends all active sending from this node. These situations are:

- CANH to CANL short → bus is stuck recessive → ends with bus-off
- CANH to GND short → bus is stuck recessive → ends with bus off

For the time before the CAN engine goes Bus-Off, the transmitter on CANH might drive the full short circuit current to the bus lines for up to 17 bit times. After 17 bit times with no dominant response on RXD the CAN controller goes Error Passive stopping any dominant sending to the bus lines and the short circuit current disappears. After that there are only a few single dominant start of frame bits with long time gaps in between until Bus-Off is reached. These single bits are not relevant thermally.

Nevertheless for the first 17 bit times, there is following supply current possible (Hint: The 15mA dominant current without load is not part of the data sheet):

$$I_{Peak(17\ bit\ times)} = I_{dom(no\ load)} + I_{ShortCircuit} = 15mA + 55mA = 70mA$$

This peak current will flow for just 17 bit times, which corresponds to:

$$t_{PeakCurrent} = 17 \times \frac{1}{BaudRate} = 17 \times \frac{1}{500kBit/s} = 34\mu s$$

Such short current peak is typically handled by the buffer capacitor connected to the voltage regulator and as such not relevant for the current limitation on a voltage supply. Since the peak is very short, it is thermally not relevant as well.

Thermally relevant is the case of CANL to GND short, which allows a bus communication as long as the bus termination is based on a simple resistor (without split termination). Assuming a worst case bus load of 45 Ohms and a CANH driver being able to pull the CANH wire up to 4V a theoretical bus current of 4V / 45 Ohms is possible. This would result in about 88mA. Due to the current limitation in the UJA116x family, this current cannot flow because it is limited to 55mA max. With that, the biggest continuous average load to the CAN supply calculates as follows:

$$I_{AverageSCFrame} = \left(I_{ShortCircuit} + I_{dom(no\ load)}\right) \times 0.8 + I_{Rec} \times 0.2$$

$$I_{AverageSCFrame} = (55mA + 15mA) \times 0.8 + 7.5mA \times 0.2 = 57.5mA\ (MAX)$$

Again this is no permanent current since this node does send only from time to time.

9.9.6 CAN – Supply Summary

The voltage regulator needs to be dimensioned for the average thermal load condition in order to deliver enough supply current for the transceiver. Depending on the connected bus systems a realistic combination of scenarios has to be considered:

- Does each supplied transceiver simultaneously support the „Wake-up scenario“?
- Do all channels have simultaneously the worst-case bus short?
- What is the contribution of the transceiver to the active communication time?

Note, that short peak currents at specific bus shorts are thermally not relevant since present for just 17 bit times (few µs only). These peak currents are typically handled by the buffer caps.

Same holds for the current caused by a sending node with and without bus error condition. The thermal load is quite low (see 9.9.3) and the peak current during the frame again comes from the buffer capacitor.

Taking all these points into account, the normal load current contribution of a CAN channel is far below 10mA on average per connected CAN transceiver. Only in specific temporary cases, the current may be slightly higher. The worst condition is achieved with a specific bus short which may result in an absolute worst case average supply load of 57.5mA within the UJA116x family in combination with a disconnected bus system and as such, no acknowledge coming from the bus interface. Such exceptional case is a dual fault scenario, which might lead to a malfunction of an ECU and it can be questioned, whether such a case is of relevance.

For the UJA116x family one can conclude, that the CAN load current is in the range of 5.68mA (normal communication) to 35.92mA (at sending a wake-up frame) offering a lot of extra supply capability for the remaining application or more CAN transceivers on the same board.

10. Watchdog Interface

10.1 Watchdog overview

The UJA116x SBCs with SPI interface (UJA1164(A), UJA1167(A), UJA1168(A) and UJA1169) contain a programmable watchdog with an independent clock source. This watchdog can be operated in three operating modes:

- **Window mode** (triggering in the 2nd half of the watchdog period)
- **Timeout mode** (triggering at any time in the watchdog period)
- Autonomous mode (allows disabling the watchdog in low power modes)

Furthermore, the UJA116x SBCs provide the possibility to constantly adapt the behavior of the watchdog by changing certain control bits in the non-volatile memory SPI register range in order to make use of the so-called

- **Forced Normal mode**

  (Watchdog completely disabled) or

- **Software Development mode**

  (Watchdog can be enabled / disabled as needed during software development)

The UJA116x SBCs support 8 watchdog periods: 8ms, 16ms, 32ms, 64ms, 128ms, 256ms, 1024ms and 4096ms. The default watchdog period at start-up is 128ms.

10.2 Watchdog software development process

10.2.1 1st step: Forced Normal mode

In order to get started with the UJA116x at first battery connection after factory delivery the UJA116x with SPI interface are provided in Forced Normal mode which is selected by the Forced Normal mode Control (FNMC = 1) bit in the SBC Configuration Control Register (see Fig 54).

In Forced Normal mode the SBC will directly enter the Normal operation mode with the V1 microcontroller supply enabled and full high-speed CAN transmit and receive capability. The watchdog is completely disabled. Thus with the Forced Normal mode setting no software is required for basic normal mode operation of the UJA116x SBCs.

The Forced Normal mode can be used for

- initial prototyping during development and
- first flashing of the microcontroller in production

Further details on the Forced Normal mode with respect to the influence on the CAN mode control are explained in chapter 9.

10.2.2 2nd step: Software Development mode

During software design it gets necessary to enable or disable the watchdog for testing and debugging purposes. Therefore the Software Development mode can be used (see Fig 54), which keeps the watchdog disabled after battery connection until it gets actively enabled via a mode change in the Watchdog mode Control (WMC) bits in the Watchdog Control Register.

Other functionality of the UJA116x SBCs than the watchdog is not influenced, thus the main software functionality with respect to the SBC can be tested without triggering the watchdog.

The Software Development mode can be selected by re-programming the Start-up Control Register in the non-volatile memory (see chapter 11.1) during Forced Normal mode.

Remark: If desired by the final application the UJA116x SBCs can also be operated continuously in Software Development mode if the watchdog functionality is not used.

10.2.3 3rd step: Full Operation

After finalizing the software or after flashing the microcontroller during production it gets necessary to get the watchdog completely active already at power-on via the battery connection.

Therefore the Full Operation (see Fig 54) needs to be selected by re-programming the SBC Start-up Configuration Control Register in the non-volatile memory (see chapter 11.1) during the initial Forced Normal mode.

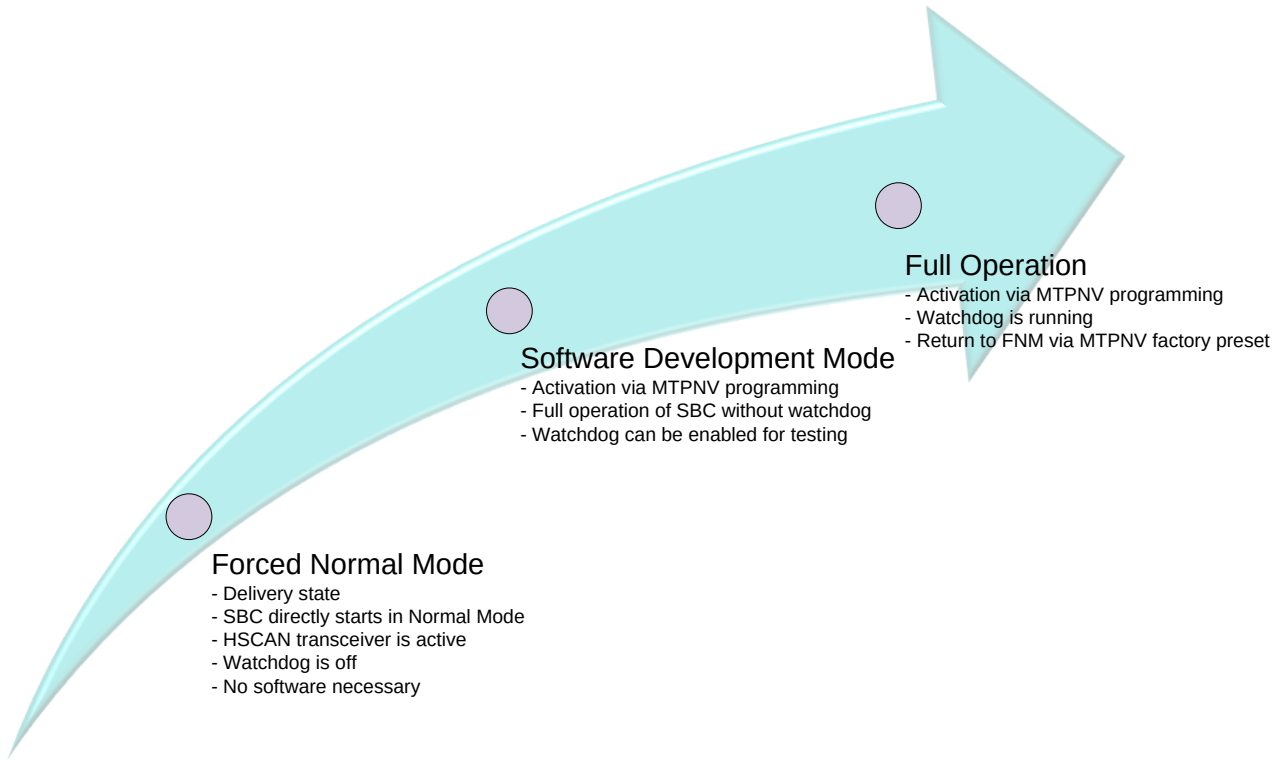


Fig 54. Watchdog software development process in the UJA116x SBC family

These three described steps ease software development in the design phase as well as flashing of the ECUs microcontroller via the CAN bus before the UJA116x SBCs get enabled for full operation with active watchdog control.

10.3 Configuration of Watchdog mode and Period

The UJA116x SBCs support three different watchdog modes and 8 different watchdog periods: 8ms, 16ms, 32ms, 64ms, 128ms (default), 256ms, 1024ms and 4096ms. The watchdog is controlled and configured by read or write accesses to the Watchdog Control (address 0x00) and Watchdog Status (address 0x05) Register. An additional influence on the watchdog functionality is given by the settings in the SBC Configuration Control Register (address 0x74) in the non-volatile memory for selection of the Forced Normal or Software Development mode.

The watchdog mode is controlled by the Watchdog mode Control bits (WMC) and the watchdog period by the Nominal Watchdog Period bits (NWP).

Table 17 shows the watchdog functionality in each SBC operation mode based on the settings in the Watchdog mode Control bits during full watchdog operation (FNMC = SDMC = 0).

Table 17. Watchdog functionality in full operation (FNMC = 0; SDMC = 0)

	Normal Watchdog triggering (always running)	Relaxed Watchdog triggering (always running)	Relaxed Watchdog triggering (off in low power)
UJA116x watchdog configuration			
WMC[1] (Watchdog mode)	100 (window)	010 [default] (timeout)	001 (autonomous)
Watchdog behavior in different modes			
Normal mode	Window	Timeout	Timeout
Standby mode, RXD HIGH	Timeout	Timeout	Off
Standby mode, RXD LOW	Timeout	Timeout	Timeout
Sleep mode	Timeout	Timeout	Off
Other modes	Off	Off	Off

As every valid write access to the Watchdog Control Register is interpreted as a watchdog trigger, the watchdog configuration is only allowed during an open watchdog window.

In Normal mode the microcontroller has unlimited access to all system functions including CAN bus networking and thus a strict observation of the system behavior by the watchdog is required. Therefore in Normal mode the watchdog configuration cannot be changed. A try to change the watchdog configuration within Normal mode will trigger an immediate system reset.

Changing the watchdog configuration (bit change of either WMC or NWP) is only allowed in Standby mode.

When writing an invalid code to the WMC (e.g. 011) or NWP bits in Standby mode the SPI operation will get ignored and an SPI failure event gets captured (SPIF bit in System Event Status Register (0x61)) which can be handled by the application.

[1] WMC setting can be changed in Standby Mode only

Here some SPI command examples for watchdog trigger commands:

- *Watchdog triggering in SBC Normal mode, watchdog Timeout mode (010) and watchdog period of 16ms (0001):*
  - *SPI command: 0000 0000 **010**X **0001**$_b$*
- *Watchdog triggering in SBC Normal mode, watchdog Window mode (100) and watchdog period of 8ms (1000):*
  - *SPI command: 0000 0000 **100**X **1000**$_b$*
- *Watchdog triggering in SBC Standby mode, watchdog Autonomous mode (001) and watchdog period of 256ms (1101):*
  - *SPI command: 0000 0000 **001**X **1101**$_b$*

It must be recognized that the watchdog mode does not only change by writing the WMC bits in Standby mode, but also when a SBC mode change is performed. Table 17 shows the relation between WMC bits and the SBC modes.

Example 1: The SBC is in Standby mode with watchdog in Timeout mode active (but WMC = 100 = Window mode) configured (with NWP = 16ms) and then enters Normal mode (MC = 111). Simultaneously with entering Normal mode the watchdog is configured to work in Window mode. Nevertheless, the watchdog trigger SPI command remains the same as before entering Normal mode:

*SPI command: 0000 0000 **100**X **0001**$_b$*

The same mechanism is also valid for the opposite direction. When entering Standby mode the watchdog will change to Timeout mode automatically.

Example 2: The SBC is in Standby mode with watchdog in Off mode (WMC = 001 = Autonomous mode) configured and then enters Normal mode (MC = 111). Simultaneously with entering Normal mode the watchdog is configured to work in Timeout mode. If the application requires the watchdog to work in Window mode instead (e.g. NWP = 32ms), the WMC bits must be configured in Standby mode before entering the Normal mode (MC change from 001 to 100). For the new watchdog configuration as well as for the triggering in Normal mode following command has to be used:

*SPI command: 0000 0000 **100**X **0010**$_b$*

10.4 Watchdog triggering

In Timeout mode the watchdog can be reset at any time within the watchdog period by a watchdog trigger. If the watchdog overflows due to a missing trigger event, the watchdog failure (WDF) bit is set in the System Event Status Register. If a WDF is already pending, a reset is performed.

In Window mode the watchdog can only be reset in the second half of the watchdog period (“open window”) by a watchdog trigger. If the watchdog is triggered in the first half of the watchdog period (“closed window”) or overflows, a system reset is immediately performed.

To select the correct trigger moment the tolerances of the watchdog timer must be taken into account. The software has to send the trigger signal after the latest possible window opening and before the earliest end of a period. For additional information see the software explanations later in this document.

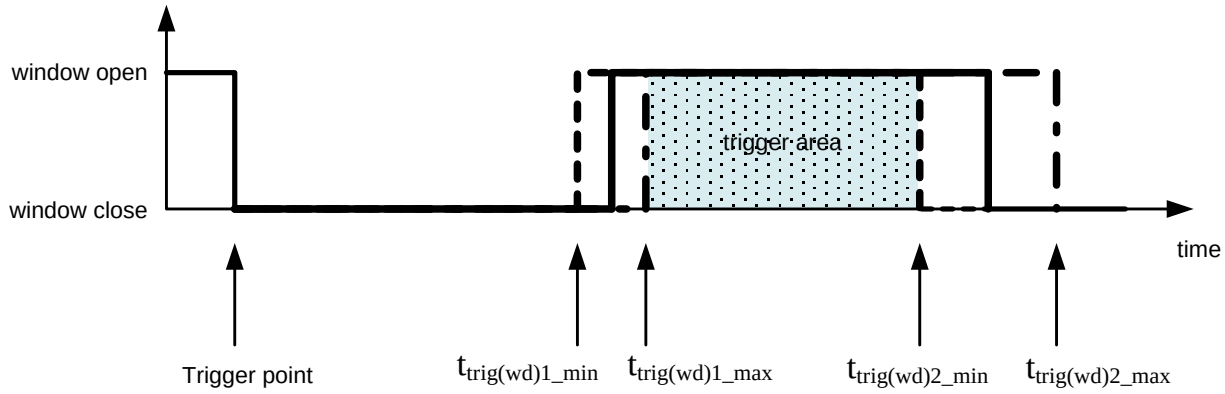


Fig 55. Allowed trigger area, when watchdog is in Window mode

As shown in Fig 55, the trigger moment has to be located between the maximum value of $t_{trig(wd)1}$ (earliest watchdog trigger point) and the minimum value of $t_{trig(wd)2}$ (latest watchdog trigger point). The related values can be found in the datasheets [4] [5] [6]. In case the tolerances of the microcontroller's clock generator cannot be neglected, the following equations should be used to define the correct trigger moment:

$$t_{trigger\_min} > \frac{t_{trig(wd)1\_max}}{1-F}, \qquad t_{trigger\_max} < \frac{t_{trig(wd)2\_min}}{1+F}.$$

F here is the magnitude of relative deviation of the microcontroller's clock frequency. It is calculated by:

$$F = \left| \frac{f - f_0}{f_0} \right|,$$

where f is the actual frequency and f_0 is the nominal frequency. $t_{trigger\_min}$ and $t_{trigger\_max}$ limit the area where the software has to choose the trigger point supposing the nominal frequency of the clock generator.

A watchdog trigger is performed with every valid write access to the Watchdog Control Register. After a successful SPI transfer the watchdog is reset. The transmitted value for the Nominal Watchdog Period NWP defines the duration of the next watchdog cycle. This is illustrated in Fig 56. Remind that the NWP value can only be changed in Standby mode.

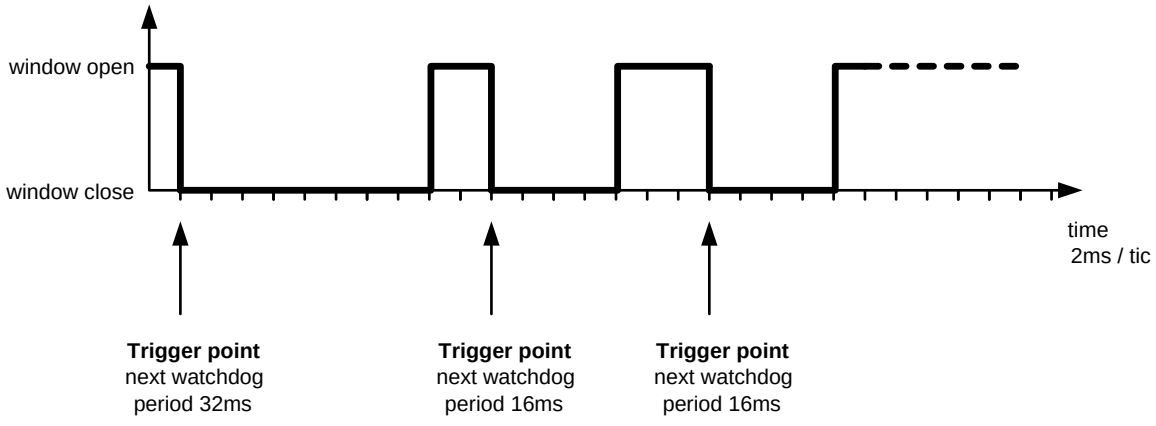


Fig 56. Watchdog triggering with different periods

10.4.1 Exceptional Watchdog Behavior

A successful write operation to the Watchdog control register resets the watchdog timer. Bits WDS are set to 01 and the watchdog restarts at the beginning of the watchdog period (regardless of the selected watchdog mode). However, the watchdog may restart unexpectedly in the second half of the watchdog period or a WDF interrupt may be captured under the following conditions.

Case A: When the watchdog is running in Timeout mode (see Table 6) and a new watchdog period is selected (via bits NWP) that is shorter than the existing watchdog period, one of both of the following events may occur:

Status bits WDS can be set to 10. When this happens, the timer restarts at the beginning of the second half of the watchdog period, causing the watchdog to overflow earlier than expected. This can be avoided by writing the new NWP (or NWP + WMC) code twice whenever the watchdog period needs to be changed. The write commands should be sent consecutively. The gap between the commands must be less than half of the new watchdog period.

If the watchdog is in the second half of the watchdog period when the watchdog period is changed, the timer will be reset correctly. The watchdog will restart at the beginning of the watchdog period and WDS will be set 01. However, a WDF event may be captured unexpectedly. To counteract this effect, the WDF event should be cleared by default after the new watchdog period has been selected as described above (two consecutive write commands).

Case B: If the watchdog is triggered in Timeout mode at exactly the same time that WDS is set to 10, it will start up again in the second half of the watchdog period. As in Case A, this will cause the watchdog to overflow earlier than expected. This behavior appears identical to an ignored watchdog trigger event and can be avoided by issuing two consecutive watchdog commands. The second command should be issued before the end of the first half of the watchdog period. It is recommended to use this trigger scheme if it is possible that the watchdog could be triggered exactly in the middle of the watchdog window.

10.5 Functionality of the Software Development mode

As explained in chapter 10.2.2 the software development mode is intended to ease software development or to be used in case the final application does not require watchdog functionality. The difference to full watchdog operation is that with SDMC = 1 the default WMC setting is 001 and thus the autonomous mode is selected instead of the timeout mode (see Table 18).

Further on with SDMC = 1 the autonomous mode behaves different than with SDMC = 0. With SDMC = 1 the watchdog is “always Off” in autonomous mode, whereas with SDMC = 0 it is “only Off until a wake-up event or until Normal mode gets entered” (compare Table 17 with Table 18).

Nevertheless the watchdog can be activated in Software Development mode by changing the Watchdog mode Control (WMC) bit settings to Window or Timeout respectively. Beside of the changed default WMC value and the changed autonomous mode behavior the UJA116x SBCs operate as in normal operation.

Table 18. Watchdog functionality in Software Development mode (FNMC = 0; SDMC = 1)

	Normal Watchdog triggering (always running)	Relaxed Watchdog triggering (always running)	Disabled (until WMC change)
UJA116x watchdog configuration			
WMC[1] (Watchdog mode)	100 (window)	010 (timeout)	001 [default] (autonomous)
Watchdog behavior in different modes			
Normal mode	Window	Timeout	Off
Standby mode, RXD HIGH	Timeout	Timeout	Off
Standby mode, RXD LOW	Timeout	Timeout	Off
Sleep mode	Timeout	Timeout	Off
Other modes	Off	Off	Off

In order to test the watchdog functionality during software development certain tests can be considered:

1) **Let the watchdog overflow in window mode / Normal mode**

   The watchdog overflow causes system reset

   ➔ Reset Source Status (RSS) information in the Main Status Register shall report “Watchdog Overflow” (01111)

2) **Let the watchdog overflow in timeout mode / Standby mode**

   The Watchdog overflow causes interrupt event

   ➔ At the watchdog overflow pin RXD is driven LOW (indicating the interrupt event). Reading the Global Event Status Register (address 0x60) indicates a

[1] WMC setting can be changed in Standby Mode only

System event (SYSE = 1). Reading the System Event Register (address 0x61) indicates a Watchdog Failure (WDF = 1).

3) **Read Watchdog Status bit (WDS)**

The WDS bit (address 0x05) shows if the watchdog is in the first or second half of the window

Read WDS bit before and after watchdog triggering

➔ A toggling WDS bit shows that watchdog is running

10.6 Cyclic watchdog wake-up from Sleep

In order to allow a cyclic wake-up of the UJA1167(A), 68(A), 69 SBCs for cyclically processing certain application routines the timeout mode can be used in Sleep mode (the timeout mode is disabled only if autonomous mode WMC = 001 selected).

Since the microcontroller supply V1 is off in Sleep mode the microcontroller will not trigger the watchdog. After the watchdog time overflow the UJA1167(A), 68(A), 69 generate a watchdog failure interrupt and thus pin RXD goes LOW, V1 gets switched on and the UJA1167(A), 68(A), 69 enters Standby mode via Reset.

Now the application can process its cyclic routines before it enters the Sleep mode of the UJA1167(A), 68(A), 69 again and for waiting on the next cyclic wake-up by the watchdog timeout.

If this cyclic wake-up is not desired than simply the autonomous mode needs to be selected before entering Sleep mode.

10.7 Summary on watchdog settings & basic access rules

The table below gives as a summary a complete overview on the behavior of the watchdog in all SBC operating modes depending on bits FNMC, SDMC and WMC

Table 19. Supported watchdog modes

	Normal Watchdog triggering (always running)	Relaxed Watchdog triggering (always running)	Relaxed Watchdog triggering (off in low power)	Disabled (until WMC change)	Disabled (always)
UJA116x watchdog configuration					
FNMC[1] (Forced Normal mode)	0	0	0	0	1
SDMC1 (SW Development mode)	x[2]	x	0	1	x
WMC[3] (Watchdog mode)	100 (window)	010 (timeout)	001 (autonomous)	001 (autonomous)	not accessible
Watchdog behavior					
Normal mode	Window	Timeout	Timeout	Off	Off
Standby mode, RXD HIGH	Timeout	Timeout	Off	Off	Off
Standby mode, RXD LOW	Timeout	Timeout	Timeout	Off	Off
Sleep mode	Timeout	Timeout	Off	Off	Off
Other modes	Off	Off	Off	Off	Off

Watchdog behavior:

In Window mode: triggering in the 2nd half of the watchdog period only

➔ Too early or too late trigger provokes system reset

In Timeout mode: triggering at any time in the watchdog period

➔ Too late trigger provokes watchdog failure event (WDF = 1)

➔ Too late trigger with pending watchdog failure provokes system reset

In Off mode: no watchdog trigger required

Watchdog control register write access:

Trigger: allowed in both, Normal and Standby mode

Configuration: allowed in Standby mode only, else system reset

[1] FNMC / SDMC setting can be changed via protected MTPNV write procedure only

[2] 'x' = don´t care

[3] WMC setting can be changed in Standby Mode only

11. Non-volatile SBC configuration

The mini high-speed CAN SBCs with an SPI interface (UJA1164(A), 67(A), 68(A), 69) offer Multiple Time Programmable Non-Volatile (MTPNV) memory cells which can be adjusted in order to continuously change the default power-on settings of the SBCs to serve different application requirements.

The following power-on default settings can be adjusted by the MTPNV memory in the registers Start-up Control (0x73) and SBC configuration control (0x74).

Table 20. Configurable power-on default settings via the MTPNV memory

Bits	Function	Options
RLC	Default reset length at V1 undervoltage related resets (a V1 undervoltage related reset typically requires a longer reset lengths in order to allow the microcontroller to start-up again)	00 = reset pulse width 1 (20 to 25ms) 01 = reset pulse width 2 (10 to 12.5ms) 10 = reset pulse width 3 (3.6 to 5ms) 11 = reset pulse width 4 (1 to 1.5ms)
VEXTSUC	Default VEXT / INH configuration (not valid for UJA1164(A))	0 = VEXT / INH off in all modes 1 = VEXT / INH on
V1RTSUC	Default V1 reset threshold level	00 = 90% of nominal value 01 = 80% of nominal value 10 = 70% of nominal value 11 = 60% of nominal value
SLPC	Protecting the SBC to go into Sleep mode (not valid for UJA1164(A))	0 = the SBC supports Sleep mode 1 = Sleep mode will be ignored
FNMC	Start-up in Forced Normal mode after power-on	0 = Forced Normal mode disabled 1 = Forced Normal mode enabled
SDMC	Start-up in Software Development mode after power-on	0 = SW Development mode disabled 1 = SW Development mode enabled

Since a change on the MTPNV memory might have a significant impact to the start-up behavior of the application a change of this memory is protected by a CRC value calculation which has to be written into the MTPNV CRC control register for confirmation before any change in the MTPNV memory gets active.

All other configurations of the SBCs which are not done in the MTPNV memory will be reset to their default at each power-on event and thus require a re-configuration to the desired values after battery reconnection.

11.1 Programming procedure of the MTPNV memory

11.1.1 Step 1: Check if the SBC is ready for programming the MTPNV memory

As part of a save protection mechanism the MTPNV can only change once during normal operation by software access in order to protect against unwanted behavioral changes in the vehicle. During mass production the MTPNV is expected to be written only once in the production line of the module maker. After that, the MTPNV memory shall be locked in order to guarantee save operation in the car. Therefore resetting can only be performed by external hardware measures (see chapter 11.2.1 for further details).

As preparation for the programming it shall be checked if the device is in its factory preset state and if it is ready to accept a write access.

Remind: In its factory preset state the SBC is per default in Forced Normal mode (FNMC = 1) and therefore no other SPI accesses need to be performed than programming the MTPNV.

First the value of the NVM Protection Status bit (NVMPS) in the MTPNV Status Register shall be checked. If this is set to 1 the MTPNV memory is not locked and thus can be programmed. Continue with step 2 (chapter 11.1.2).

In case bit NVMPS = 0, than the MTPNV memory is locked and a reset of this memory section first needs to be performed in order to unlock the MTPNV for a new programming cycle. Continue with chapter 11.2.1.

An internal counter increments each time when programming the MTPNV cells in order to indicate how many times the MTPNV got already programmed. Therefore the WRCNTS bits in the MTPNV Status Register can be read. The counter is limited to count up to 63 (6 bits width) and keeps at the value of 63 at any further write access. Nevertheless it is allowed to program the MTPNV up to 200 times. At further write accesses (>200) proper functionality cannot be guaranteed. This limitation might only be valid during an ECU software development which might need changes in the MTPNV memory when debugging the software, but in production the write accesses are expected to be limited to one time only.

11.1.2 Step 2: Program the MTPNV memory

In the second step, when the SBC is ready for programming its MTPNV, the desired values shall be written into the SPI registers

- Start-up Control (0x73) and
- SBC configuration control (0x74)

Remind: Before the new settings in the two registers 0x73 and 0x74 get valid, any read access will still feedback the previous settings which indicate how the SBC is currently configured.

Based on the written values into those two registers 0x73 and 0x74 a CRC checksum needs to be calculated. The following rules apply to the CRC calculation:

Modulo-2 division with the generator polynomial:

$$x^8 + x^5 + x^3 + x^2 + x + 1$$

The result of this operation needs to be bitwise converted.

After calculation of the CRC checksum the 8 bit result needs to be written into the MTPNV CRC Control Register at address 0x75 in order to kick-off the programming of the MTPNV cells 0x73 and 0x74.

Example with UJA1168/VX (A/X):

a. Write to Startup Control Register (Address 0x73): 0x28

   RLC = 10 = reset pulse width 3 (3.6 to 5ms)

   VEXTSUC = 1 = VEXT on

b. Write to SBC Configuration Control (Address 0x74): 0x10

   V1RTSUC = 01 = 80% of nominal value

   FNMC = 0 = Forced Normal mode disabled

SDMC = 0 = Software Development mode disabled

SLPC = 0 = the SBC supports Sleep mode

c. Calculate CRC checksum → Result: 0x26

d. Write to MTPNV CRC Control Register (Address 0x75): 0x26

CRCC = 0010 0110 = calculated CRC checksum

After correct writing to the CRCC bits the SBC starts re-programming of the MTPNV cells. In case the re-programming was successful a system reset is triggered. If the CRC value was not correct, re-programming is aborted. Please note, that it takes about 25µs to copy the values from the registers 0x73 and 0x74 to the MTPNV calls. As such the content of these registers shall not be changed anymore in that time window starting with the rising edge of the SCSN signal writing to the CRCC bits.

11.1.3 Step 3: Check whether the MTPNV programming was successful

After leaving the reset mode into Standby mode it can be checked whether the MTPNV programming was successful.

First the register settings in the registers 0x73 and 0x74 needs to match the desired values from step 2.

Secondly the MTPNV memory cells are now protected against re-programming (NVMPS = 0), the write counter (WRCNTS) is incremented by 1 and the bit ECCS shall indicate that there was no error during the programming procedure (ECCS = 0).

11.2 Reset of the MTPNV memory to factory preset settings

11.2.1 Step 1: Apply external settings to reset the MTPNV memory

In order to reset the MTPNV settings to their initial factory preset values again the following three conditions need to be applied externally to the SBC while the BAT pin is unsupplied:

- Pin RSTN is externally held LOW (VIO pin for the UJA1169L variants)
- CANH is pulled to battery level & CANL is pulled to GND level, thus provoking a dominant condition on the bus

Then the BAT pin needs to be supplied and the conditions need to be hold for > $t_{d(MTPNV)}$, which is about 1 second.

When the timer overflows the factory preset settings get restored and the procedure is ended by an SBC system reset and then entering Forced Normal mode.

An indication for the end of the factory preset procedure is a falling edge on pin RXD because of the power-on bit being set. During the factory preset restore process pin RXD is kept HIGH. (Note: For the L version there is no edge visible on RXD because VIO is held LOW. If VIO gets supplied again after successful factory preset, the RXD pin is signaling the LOW condition. If that is not the case, the factory preset was not completed correctly).

11.2.2 Step 2: Check whether the MTPNV reset was successful

Reading the MTPNV Status Register should indicate NVMPS = 1 (ready for programming) and reading the SBC Configuration Control Register should indicate FNMC = 1 (Forced Normal mode enabled) in order to confirm that the SBC is back in its factory preset state. Furthermore the write counter (WRCNTS) is incremented by 1, because the MTP was written again

12. Software flow

This chapter introduces the software perspective of the UJA116x family. It discusses the different operations, which are used in automotive applications. Fig 57 illustrates the different operations between “Power-on” and “Power-off”. Moreover, the figure below provides a quick overview about the different kind and the order of the operations

The following subchapters discuss each operation in more detail.

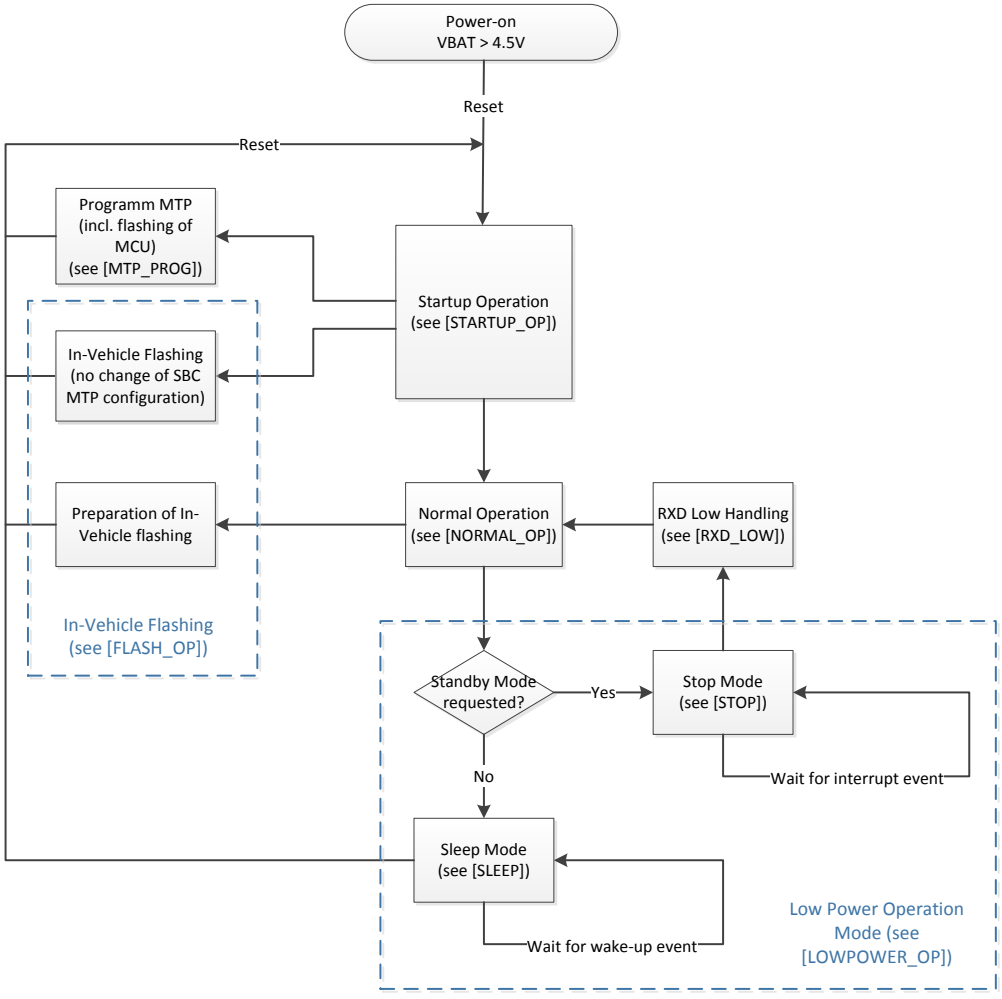


Fig 57. Abstract view in Software Flow

Example code of all different operations can be found in the appendix chapter 13.3.

To illustrate the software flow of the UJA116x family this chapter concentrates on the device family members UJA1168/VX/FD (A/X/F) or rather UJA1168/FD (A/F).

The differences to all other SPI derivatives are discussed subsequently. In general the software flow is similar, only dedicated features are left out that can be neglected during software implementation of smaller UJA116x derivatives.

The figure below shows the simplified state diagram of the UJA1168(A) family from software perspective. This state diagram will be used in the following subchapters to establish the link between the different software operations and the related UJA1168(A) family operating modes.

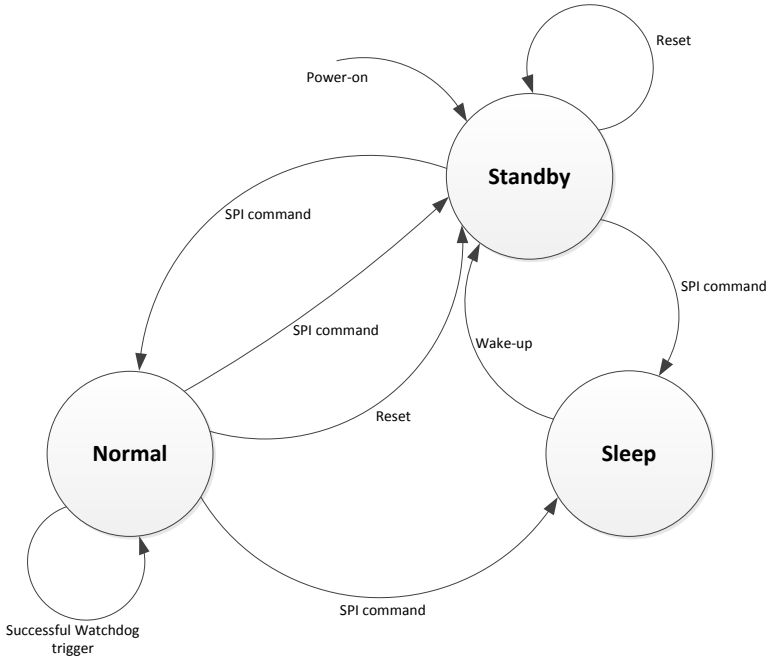


Fig 58. Simplified mode diagram from SW perspective for UJA1168(A)

12.1 Startup Operation [STARTUP_OP]

This section introduces the software operations, which are related to the startup of the application. The Startup Operation is always executed after leaving the Reset mode and it takes place in Standby mode of the UJA1168(A) family (see picture below). Moreover, the figure below shows the different hardware events that trigger the execution of the Startup Operation. All kinds of resets (e.g. external reset, watchdog failure, V1 under-voltage, etc.) trigger the execution of the Startup Operation. Furthermore, the “Power-on” and any “Wake-up” hardware event trigger the Startup Operation. At the end of the Startup Operation a transition to Normal Operation mode is performed via the related SPI command.

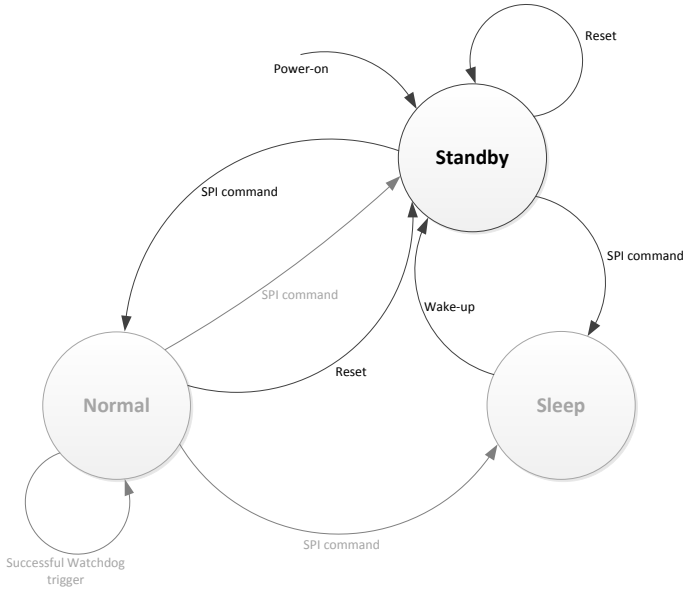


Fig 59. Simplified mode diagram with focus on Startup Operation

The Startup Operation typically consists of the following parts:

- Microcontroller initialization
- Application initialization
- Check device identification
- In-vehicle Flashing of ECUs (if implemented)
- Program and check of MTPNV
- Watchdog configuration
- Reset source detection
- Event handling
- Transition to Normal Operation mode

Fig 60 shows the complete flow of the Startup Operation with its different parts. Moreover, it guides to the related subchapters for a detailed explanation.

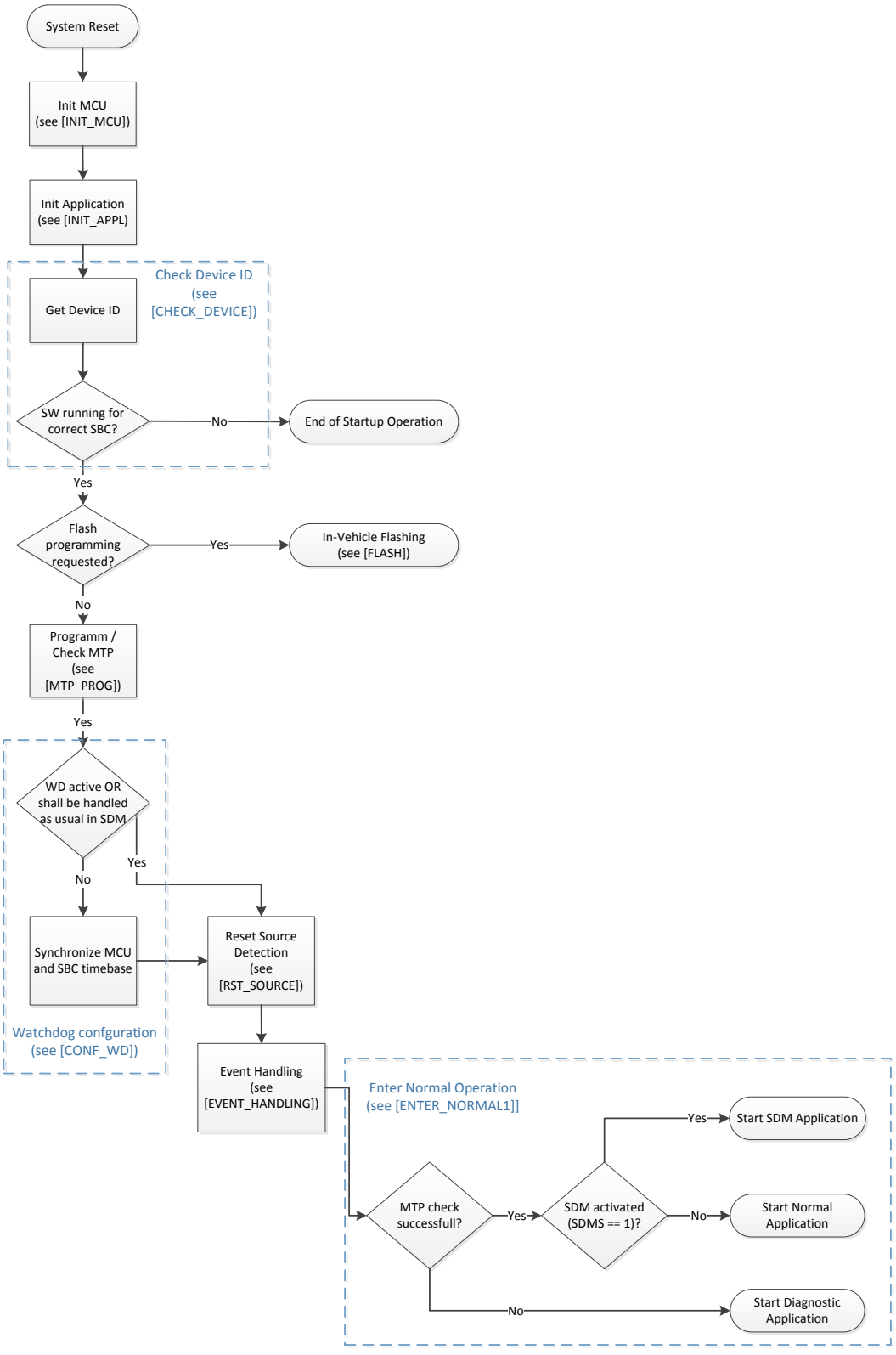


Fig 60. Startup Operation Software Flow

12.1.1 Microcontroller initialization [INIT_MCU]

The microcontroller initialization is always the first part of the startup routine. It is a microcontroller specific routine that configures the microcontroller and its periphery. With respect to the UJA1168(A) SBC, it has at least to be insured that after the initialization the SPI periphery of the microcontroller is working properly. Otherwise no communication with the UJA1168(A) can take place.

12.1.2 Application initialization [INIT_APPL]

The application initialization is also necessary at the beginning of the startup routine. It is an application specific routine that initializes the global application specific variables. Hence, it is insured that after the initialization the application software is working properly. Otherwise e.g. the scheduler or counters may not work correctly.

12.1.3 Check device identification [CHECK_DEVICE]

In order to check, if the running application software is used for the correct UJA1168(A) device type, the identification register is read and the UJA1168(A) type is determined. This is required to ensure that the software runs on the correct SBC device type.

12.1.4 Flash programming [FLASH]

Here it is checked whether a re-flashing of the microcontroller is requested (flash signature invalid) or not. In case the microcontroller must be flashed, Startup Operation is aborted and Flash programming (see chapter 12.5) is started.

12.1.5 Programming and checking the MTPNV [MTP_PROG]

The programming and checking of UJA1168(A) multi-time programmable non-volatile memory (MTPNV) is a major part of the startup process. On the one hand this function ensures that the MTPNV is programmed and on the other hand it guarantees that the MTPNV programming is still consistent to the configuration stored in flash.

As programming the MTPNV is not only needed after 1st factory flashing, but also in the laboratory during evaluation, the family supports a mechanism to restore the factory preset. Hence, the MCU software has to ensure that the MTPNV is reprogrammed correctly at every startup. In order to program the MTPNV registers, the SBC must perform a factory preset before. Only if this is done, the MTPNV can be reprogrammed, indicated by the Non-Volatile Memory Programming Status (NVMPS) bit.

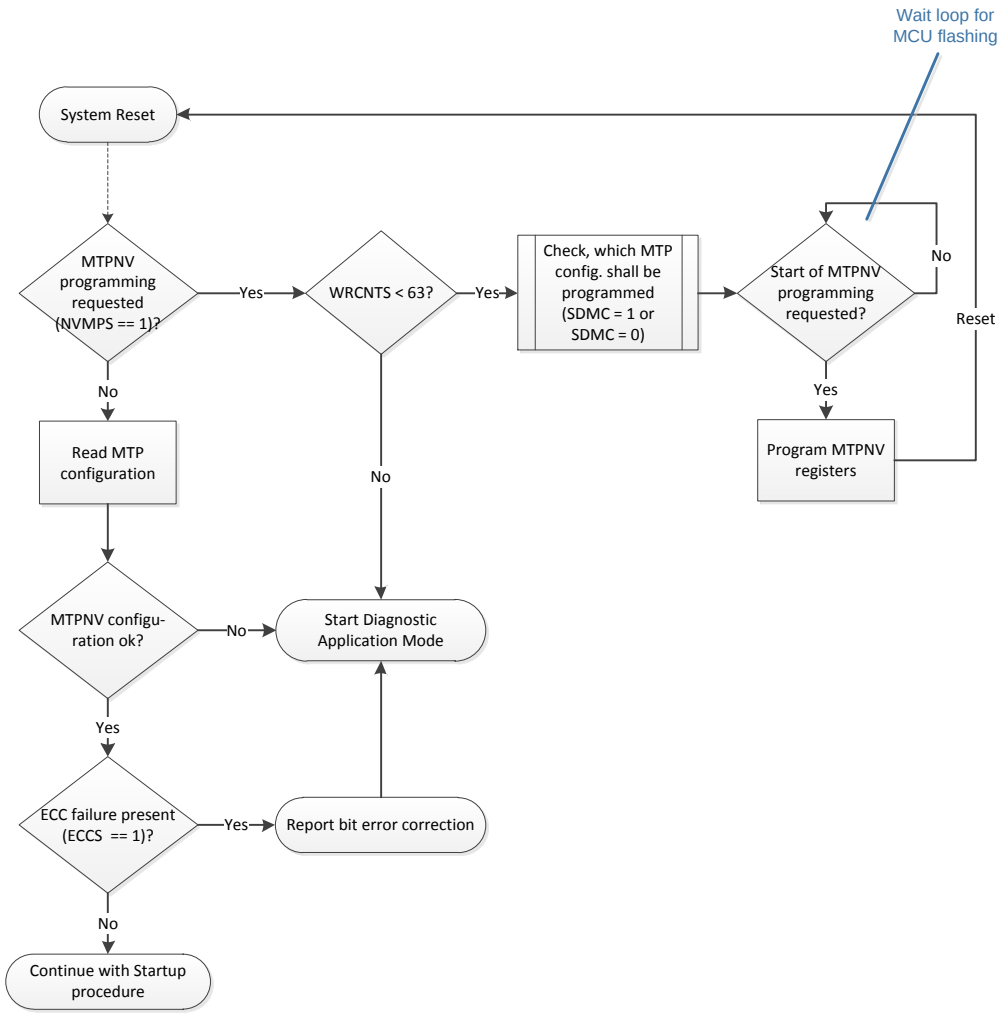


Fig 61. Software Flow of MTPNV Programming and Checking

Fig 61 shows the software flow of the function responsible for programming and checking the MTPNV. The first step of the MTPNV programming and checking function is reading

the MTPNV Status Register (SPI command = 0xE100). This register shows the current Non-Volatile Memory Programming Status (NVMPS), Error Counter Status (ECCS) and Write Counter Status (WRCNTS). Depending on the NVMPS bit the MTPNV is rather checked or can get reprogrammed afterwards.

If the MTPNV is ready for reprogramming (NVMPS = 1), the Write Counter Status (WRCNTS) is checked afterwards. If the WRCNTS has the maximum value of 63, the programming process is stopped and a special diagnostic function can be started, that reveals the issue.

If the WRCNTS is below 63, the programming process is started. At first the configuration of the SDMC bit in the SBC Configuration Control Register is determined by special port input signal. This allows entering software development mode and reprogramming the SBC MTP during runtime without flashing the microcontroller memory. To be sure that all signals are stable and that there are no disturbing environmental influences, an additional signal (e.g. port pin toggle) must be given to finally start the MTPNV programming.

The MTPNV is programmed in two steps:

- First the desired values are written into the register 0x73 and 0x74,
- Second the programming has to be confirmed by writing the correct CRC sum to the register 0x75.

Programming of the SBC is indicated by a system reset afterwards.

Waiting for the MTPNV programming start signal not only ensures stability of all signals, it also offers the possibility to flash the MCU with new software (e.g. new MTPNV configuration) in a defined system environment. After restoring the factory preset the SBC enters Forced Normal mode. Hence, the watchdog is disabled and can be ignored during flashing in this “waiting loop” (see Fig 61).

If the MTPNV is not ready for programming (NVMPS = 0), the MTPNV configuration (register 0x73 and 0x74) is read back and compared to the MTPNV configuration stored in the MCU flash. Furthermore, the Error Counter Status (ECCS) is checked. In case a single bit failure is detected and corrected (ECCS = 1), the bit error correction is reported and a special diagnostic function can be started.

Please consider that the MTPNV configuration cannot be read back until the MTPNV programming is finished.

12.1.6 Watchdog configuration [CONF_WD]

The next part of the Startup Operation is the watchdog configuration. This part must be executed within 256ms after the Reset mode is released. Otherwise a watchdog overflow reset can be triggered and the Startup Operation restarts.

To find out, if the watchdog is running or disabled, a read access to the Watchdog Status Register of the UJA1168(A) must be performed (SPI command = 0x0B00). The 1st two bits of the register are called Watchdog Status (WDS) and indicate if the watchdog is running (1st half, 2nd half) or not.

If WDS = 0, the watchdog is disabled due to MTPNV configuration (FNMC = 1 or SDMC = 1) and no watchdog related resets are possible. In this case watchdog triggering is not required. Nevertheless, it might be necessary to activate the watchdog for test purposes in Software Development mode. Hence, the watchdog can be reactivated via a change of the WMC bits to Timeout or Window mode. If this behavior is desired, it must be signaled via a special signal (MCU port input) and the watchdog configuration is started even though the watchdog is off per default at startup.

Otherwise, if WDS = 1, the watchdog is enabled at startup. Consequently, the microcontroller time base and the UJA1168(A) watchdog timer have to be synchronized in order to allow a proper watchdog service in software, especially for the Window mode. After the synchronization the watchdog can be triggered with the required period. The previous described flow can also be seen in the Fig 60.

Fig 62 illustrates why synchronization between the UJA1168(A) watchdog timer and the microcontroller time base is required. Background is that with a cold start of the entire system both time domains are completely unsynchronized since timers in the SBC as well as timers in the microcontroller start at different moments in time. The synchronization mechanism depends on the general software architecture of the application. In general two strategies exist, how to synchronize both timers or rather time domains.

1. Restart/Start the microcontroller time base short before a watchdog trigger (synchronize microcontroller timer)
2. Trigger the watchdog with respect to the microcontroller time base (synchronize watchdog timer)

Strategy 1 is the most common one in applications without Operating System (OS). Here a dedicated time base within the microcontroller can be adapted to the watchdog time base in the SBC.

The situation is different in applications containing a time triggered OS. The OS time base cannot be reset during operation, because this would corrupt the entire software schedule. Therefore strategy 2 is required synchronizing the SBC time base towards the already running operating system time base.

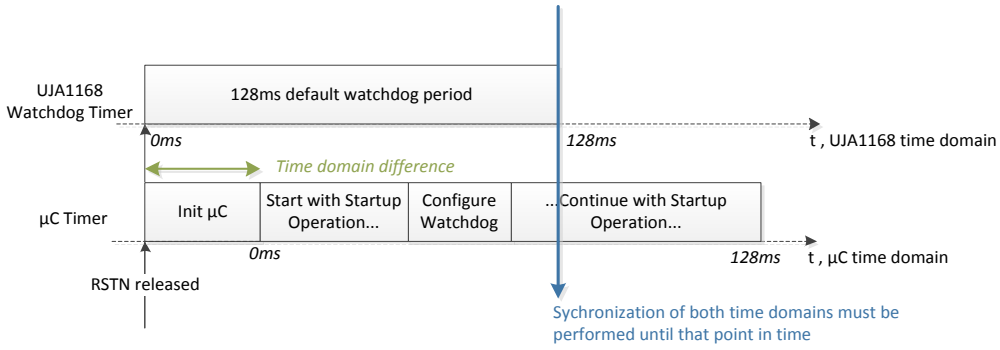


Fig 62. Microcontroller and watchdog synchronization

In the figure above it is illustrated that the SBC time domain starts with the release of the reset (RSTN) signal. After that, the microcontroller starts its software with a device specific and software specific delay (time domain difference). In order to give the application enough time to settle all peripherals and starting the Operating System, the SBC provides up to 128ms, until the watchdog needs his first service trigger. This first service has to come before the 128ms are elapsed (see blue line in the picture above). After the software has been started and the watchdog service is initialized, the first watchdog service takes place at the end of the “Configure Watchdog” phase. With this first trigger, the watchdog is synchronized and starts to operate with the software defined nominal watchdog period.

For more information on how to trigger the UJA1168(A) watchdog please refer to chapter 10.

12.1.7 Reset Source Detection [RST_SOURCE]

The next step in the Startup Operation is the reset source detection. It depends on the application, if reset source detection is required.

In case reset source detection is desired, the SBC Main Status Register must be read (SPI command = 0x0700) and the content of the RSS bits can be stored in a global variable for further evaluation in the application software (see Fig 63). Evaluation of the reset source is application specific, but e.g. it can be checked, whether the stored reset source is an untypical reason and further handling by software is necessary. The information can for example be stored in the failure memory or specific actions in software can be initiated, e.g. SBC re-initialization.

Untypical reset reasons may be all reset sources that reveal an error in the system and which cannot be recognized as an event , e.g.:

- Watchdog triggered too early
- Illegal watchdog mode control register access
- RSTN pin externally pulled down
- Leaving Overtemp mode
- Illegal Sleep mode command received

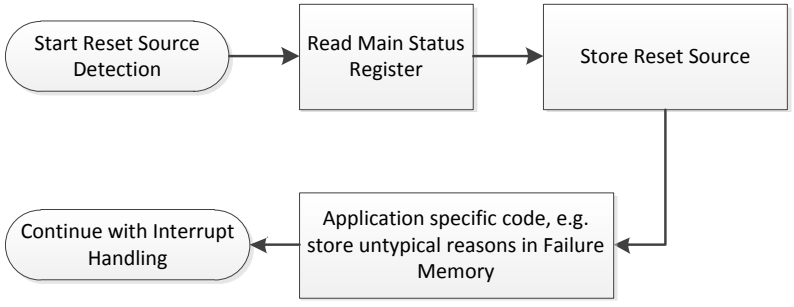


Fig 63. Software flow, if reset source is of interest (Reset Source Detection)

12.1.8 Event Handling during Startup [EVENT_HANDLING]

The reset source detection only determines one reason for the preceding reset. Nevertheless, several events might cause the reset and need further handling. For that reason the Startup Operation must handle and clear all pending events in any case, independent from whether the reset source detection has been done or not. As long as the CAN transceiver is not in Active or Listen-only mode, the RXD pin signals whether an event is pending or not. If events are pending after Startup Operation and CAN is not in Active or Listen-only mode the RXD pin connected to the CAN Controller, cannot trigger any further software actions because it remains low.

It must be ensured that all event sources are cleared to release the RXD pin and that an initialization of the UJA1168(A) is performed. If the Power-On (PO bit) event is set, the reset was caused by leaving the Off mode. In this case the UJA1168(A) must be initialized, which means an initial configuration of:

- V1 and INH/VEXT
- CAN transceiver incl. Partial Networking, if desired
- General Purpose Memories
- System events
- Supply events
- Transceiver events
- Wake pin events

Additionally, if desired, register configurations can be locked by writing to the related bits in the Lock Control Register (register address 0x0A).

The event handling in Startup Operation mode does not differ from the Event Polling and Handling done during Normal Operation. Therefore further information on this topic incl. software flows can be found in chapter 12.2.5.

12.1.9 Transition to Normal mode [ENTER_NORMAL1]

Normal mode is entered by writing 0x0207 to the mode Control Register. For more information on Normal Operation refer to chapter 12.2.

12.2 Normal Operation [NORMAL_OP]

This section introduces the software operations which are associated to Normal Operation of the application. Normal Operation is related to the Normal mode of the UJA1168(A) family. This mode can only be entered after a successful startup operation. Therefore the beginning of Normal Operation is a transition from Standby to Normal mode caused by the related SPI command.

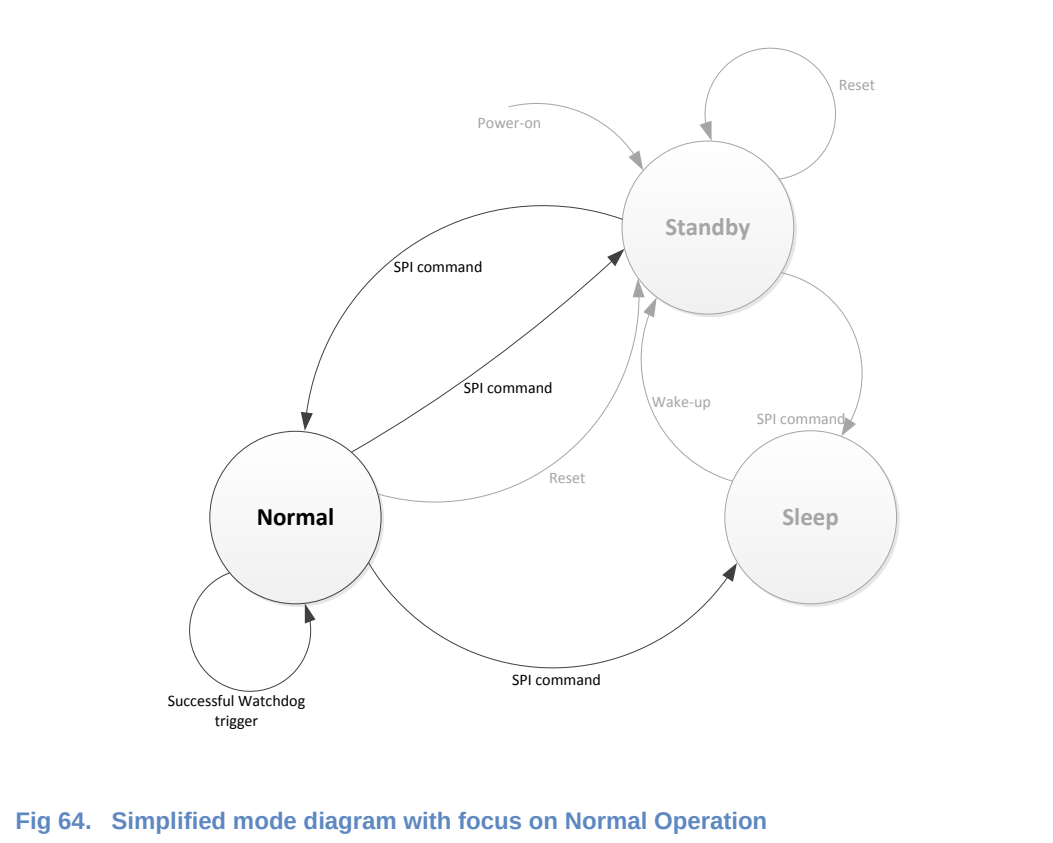


Fig 64. Simplified mode diagram with focus on Normal Operation

The most important operations of the Normal Operation are

- watchdog handling,
- transceiver control,
- event polling and
- application execution.

For that reason this chapter shows, how to realize successful watchdog triggers and to enable the CAN Transceiver. At the end of the Normal Operation a transition to Low Power Operation (Standby mode, Sleep mode) is performed via the related SPI command.

Fig 64 shows the different parts of Normal Operation. Normal Operation consists of:

- Entering Normal Operation
- Watchdog triggering
- CAN Transceiver control
- Event Handling
- Running the default application
- Transition to Low Power Operation (Standby, Sleep)
-

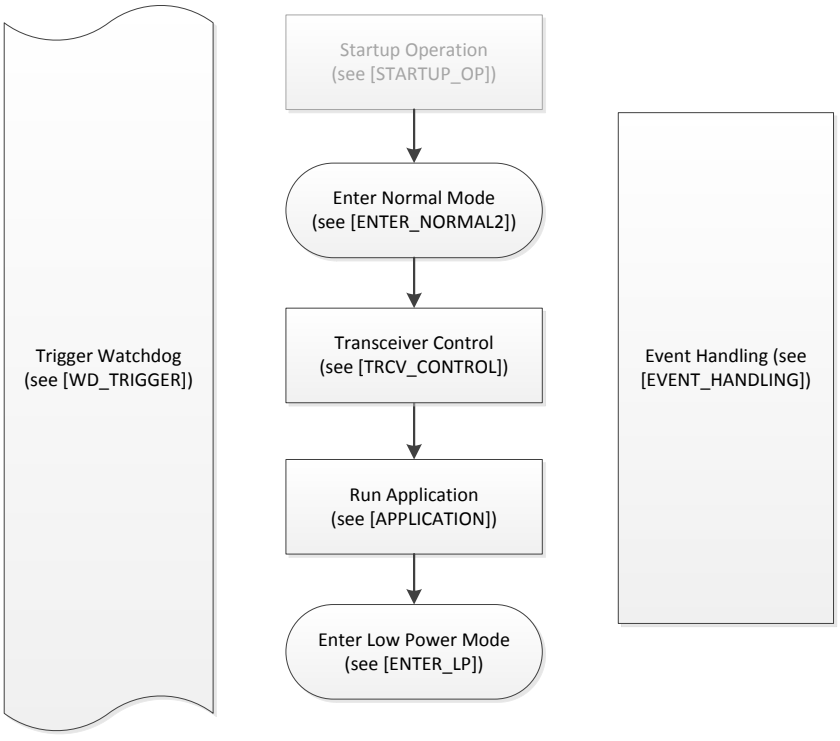


Fig 65. Normal Operation Software Flow

12.2.1 Transition to Normal mode [ENTER_NORMAL2]

Fig 66 illustrates the software flow of the transition to Normal Operation and summarizes all steps that are recommended.

The transition to Normal Operation is done by changing the UJA1168(A) mode from Standby mode to Normal mode. This is done by writing the value 0x7 to the mode Control (MC) bits of the mode Control Register (SPI command = 0x0207). As a transition to Normal mode will not trigger the watchdog, it is possible to change the modes at any point in time.

Please note that neither the watchdog mode nor the watchdog period can be changed in Normal mode. Therefore, in case this is needed, the watchdog has to be triggered with the new settings right before entering the Normal mode.

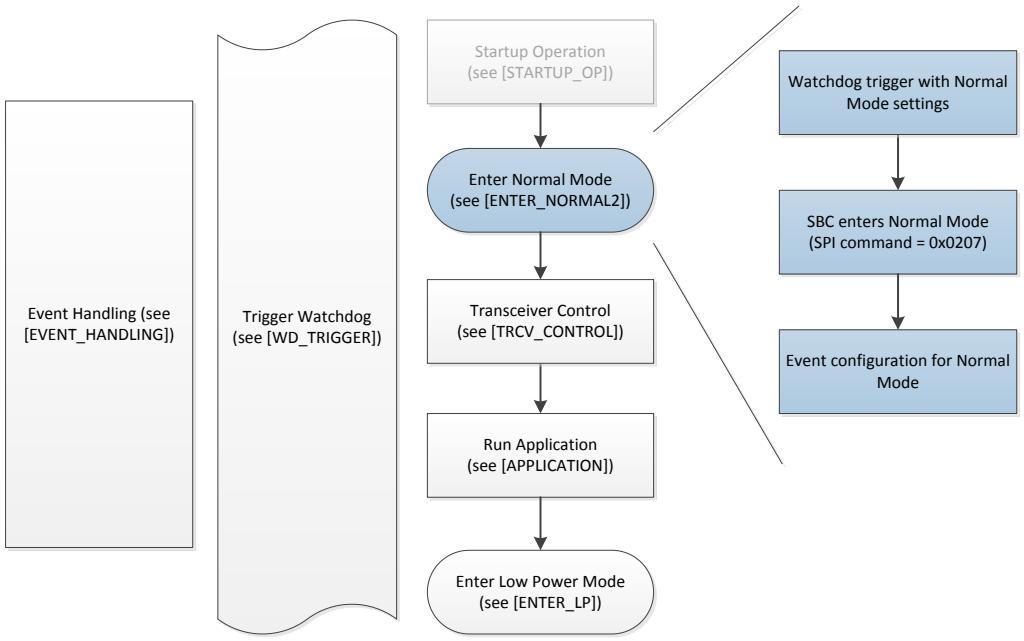


Fig 66. Transition to Normal Operation

In Normal mode additional functionality of the SBC becomes available. If configured, the CAN Transceiver becomes active. The CAN transceiver enters its Active mode automatically, if the CAN mode Control (CMC) bits in the CAN Control Register have been initialized with value 0x1 or 0x2 before. If CMC is 0x0, the CAN transceiver is Offline and if CMC is 0x3, the CAN transceiver is in Listen-only mode.

Additionally the behavior of VEXT (UJA1168/VX (A/X), UJA1168/VX/FD (A/X/F)) or rather INH pin (UJA1168(A), UJA1168/FD (A/F)) may change during the transition from Standby to Normal mode. This depends on the configuration of the VEXT/INH bit in the V1 and INH/VEXT Control Register. If VEXT/INH is initialized with 0x1, VEXT/INH is only active in Normal mode. Hence, the VEXT regulator or rather INH is enabled when the SBC enters Normal mode. In all other configurations there is no behavioral change of VEXT/INH between Standby and Normal mode, it is either “off” (VEXT/INH = 0x0), “on in Normal, Standby, Reset” (VEXT/INH = 0x2) or “on in Normal, Standby, Sleep and Reset” (VEXT/INH = 0x3).

Due to the new functionalities in Normal mode, it is recommended at least to enable following events, in order to monitor events at under-voltage, overvoltage and at failures:

- VEXT Under-voltage Event (depending on VEXTC) in Supply Event Enable Register (bit VEXTUE)
- VEXT Overvoltage Event (depending on VEXTC) in Supply Event Enable Register (bit VEXTOE)
- CAN Failure Event (depending on CMC) in Transceiver Event Enable Register (bit CFE)

In general it is recommended to disable all regular wake-up sources while in Normal mode. Benefit of this is that any unintended exit out of Normal mode would immediately cause a system reset. This is to prevent a dead-lock situation of the system with having

all wake-up sources disabled and leaving Normal Operating mode. Therefore, it is recommended not only to clear the CWE bit but also to clear the WPRE and WPFE bits, which disable the local wake-up via pin WAKE. Therefore SPI write accesses are necessary to the Transceiver Event Enable Register (SPI command: 0x4602) and WAKE Pin Enable Register (0x9800). The result of these SPI commands is that all regular wake-up sources are disabled. The CAN Failure detection feature is still enabled.

12.2.2 Trigger the Watchdog [WD_TRIGGER]

Successful watchdog triggers on a regular basis are required to keep the UJA1168(A) in Normal mode. This must be ensured by the application software. If the watchdog is enabled in Window or Timeout mode, it must always be triggered regardless of the UJA1168(A) mode. Therefore, it is recommended to treat the Timeout Watchdog in Standby mode like a Window Watchdog in Normal mode. This makes the software architecture easier by just having one common watchdog service principle. So, there is no need to distinguish between the SBC operating modes. Anyhow, in some applications it might be of benefit to have a relaxed watchdog trigger mechanism during Standby or Normal mode. This depends on the overall software architecture used and is supported by the timeout behavior of the SBC. Additionally, the watchdog can be completely disabled in Standby mode (if WMC = Autonomous mode), when no event is pending. If Autonomous Watchdog is selected for Standby mode, any wake-up will immediately enable the watchdog with timeout behavior.

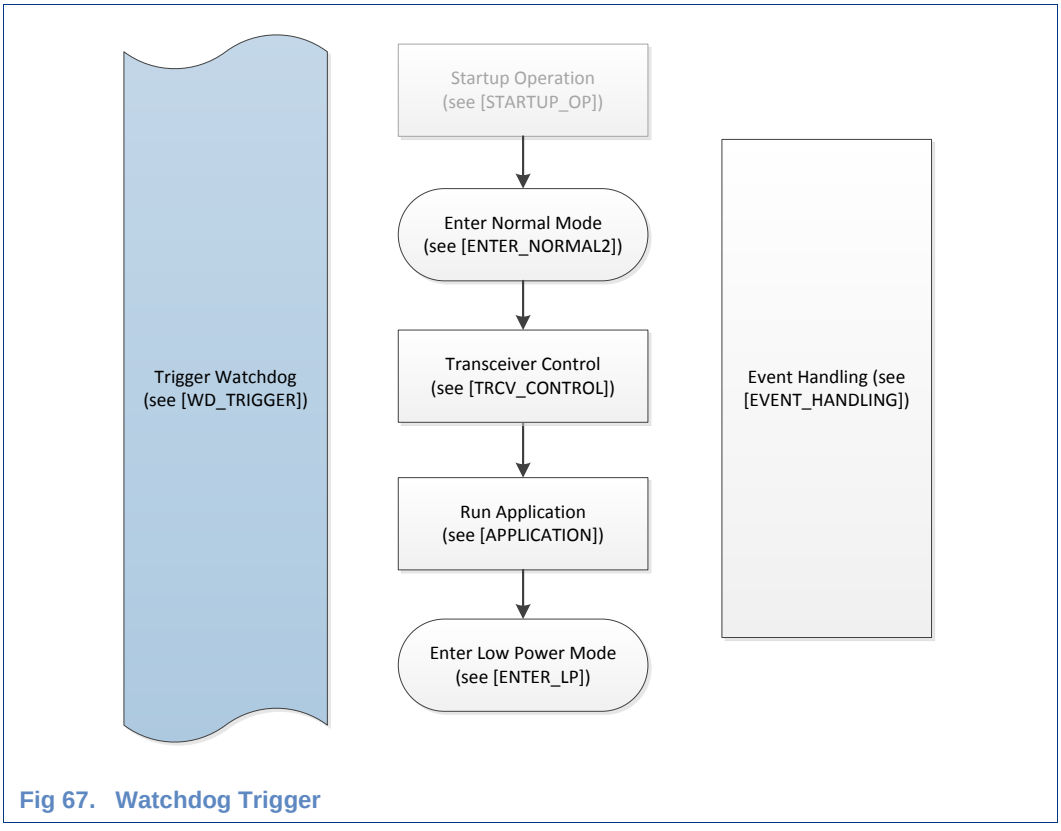


Fig 67. Watchdog Trigger

In general, it is not recommended to trigger the watchdog directly within a related timer interrupt service routine, because a hardware timer within a microcontroller might still

operate properly, while the main microcontroller core is crashed already. Instead, it is recommended to install software flags which indicate proper operation of the application. This way, the main part of the watchdog trigger task is to check whether all expected flags are set. If all flags are set correctly the watchdog can be triggered with the related period. In case of incorrect flags a software reset can be performed or the watchdog trigger can be skipped. Both actions will end up in a reset as desired.

In Normal mode the watchdog is running in Window or Timeout mode. It is recommended to use the Window Watchdog mode for Normal Operation.

The watchdog is in Window mode when the Watchdog mode Control (WMC) bits of the Watchdog Control Register are set to the value 0x4 in Normal mode. A watchdog trigger command for Window Watchdog mode with e.g. 8ms Nominal Watchdog Period (NWP) is 0x0088. This code must be written to the Watchdog Control Register within the open watchdog window (in case of 8ms the open window is 4.4ms to 7.2ms because of 10% oscillator accuracy).

Moreover, a change of the WMC bit in Normal mode causes a system reset. This feature makes sure that an unintended change of the watchdog setting is detected by the system. Therefore, it is recommended to change to Standby mode before changing the WMC bit, if this is desired.

In Software Development mode the watchdog is disabled per default (WMC = Autonomous mode), but can be reactivated by a change of the WMC bits. If this behavior is desired, it must be signaled via a special signal (MCU port input). In this case the watchdog trigger command is processed as in the Normal Application and the WMC bit is changed to the watchdog modes defined in the software (Window, Timeout and Autonomous). Otherwise, the watchdog shall exclusively be triggered with WMC bits set to Autonomous mode and the watchdog is kept disabled during Software Development mode.

Due to exceptional behavior of the watchdog (see data sheet for further details), it is recommended to send the watchdog trigger command twice, if the watchdog is in timeout mode and to clear a potential watchdog interrupt (WDI) afterwards. In order not to handle this special behavior in the application the watchdog trigger mechanism should be hidden in the watchdog trigger routine that is called each time the watchdog is triggered or reconfigured. The recommended software flow is shown below.

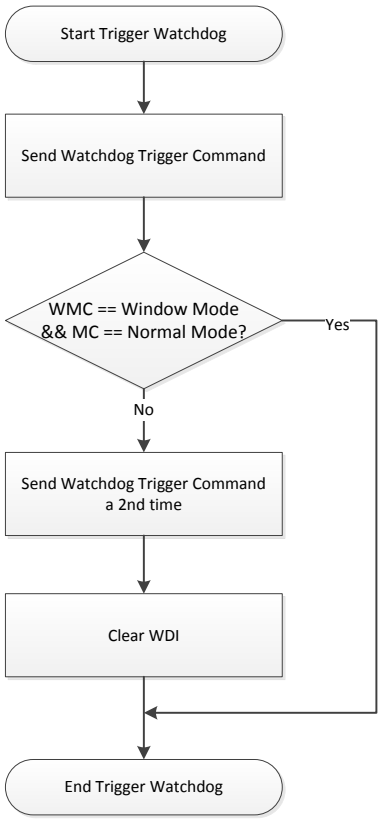


Fig 68. Recommended Watchdog Trigger Mechanism

For more information on the watchdog functionality and configurations please refer to chapter 10.

12.2.3 Transceiver Control ([TRCV_CONTROL]

The next step after the transition to Normal mode is the control of the UJA1168(A) CAN transceiver. The transceiver control is done by the Transceiver mode Control bits (CMC) in the CAN Control Register. Enabling the transceiver in Normal mode is done by initializing CMC with 0x1 or 0x2 during SBC initialization or later on.

Before starting CAN communication, or rather enabling CAN Protocol Engine (CAN PE) it is recommended to check if the CAN Transceiver is supplied and everything is working properly. Hence, the VCAN Status (VCS) bit, the CAN Failure Status (CFS) bit and the CAN Transmitter Status (CTS) bit in the Transceiver Status Register should be read. Only if

- VCAN is above its under-voltage threshold,
- no CAN failure is present and
- the CAN transmitter is ready to transmit

the CAN PE should be activated and CAN communication should be started. If this sequence is not considered, active sending on CAN may lead to error messages on the bus.

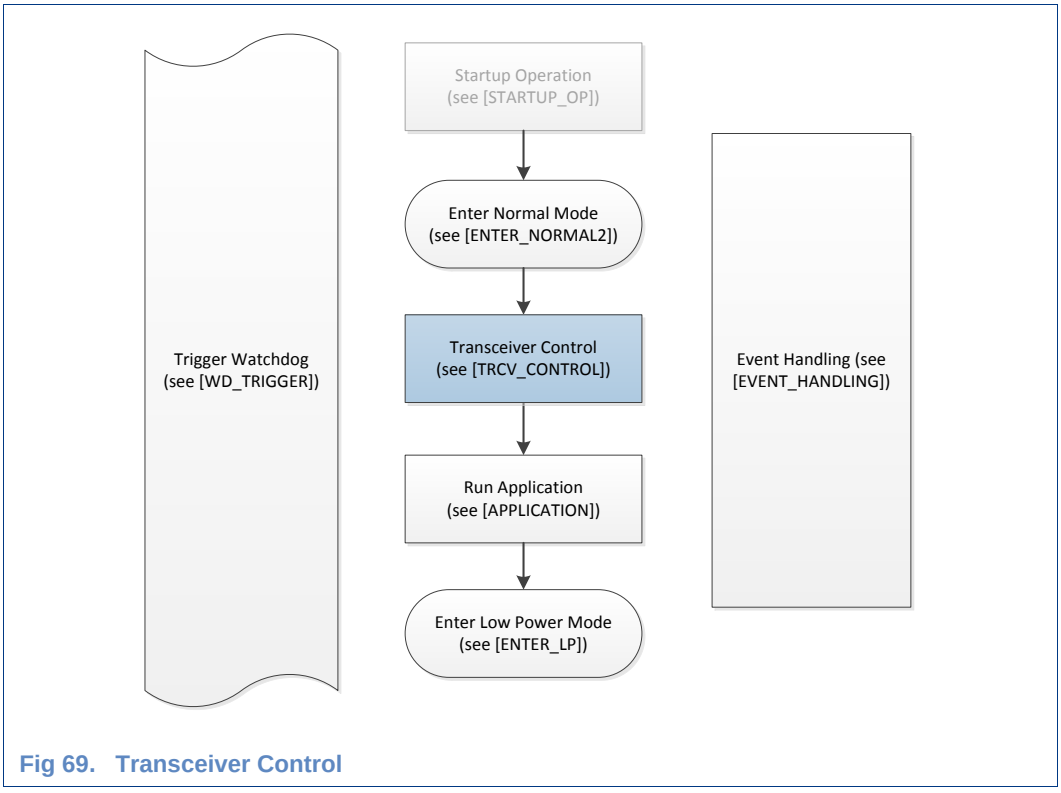


Fig 69. Transceiver Control

Any system reset will automatically deactivate the UJA1168(A) CAN transceiver. Moreover, if CMC = 0x1, a V1 under-voltage (V1 < 90%) will make the CAN Transceiver leaving CAN Active mode. The CAN transceiver will automatically recover when the under-voltage is gone and CMC is still configured for Active mode in SBC Normal mode.

The CAN Failure Event (CF) and the status flags CAN Failure Status (CFS), CAN Transmitter Status (CTS) and VCAN Status (VCS) can be used to control the CAN Protocol Engine within the microcontroller in case of a CAN transceiver failure. This is illustrated by the Fig 70.

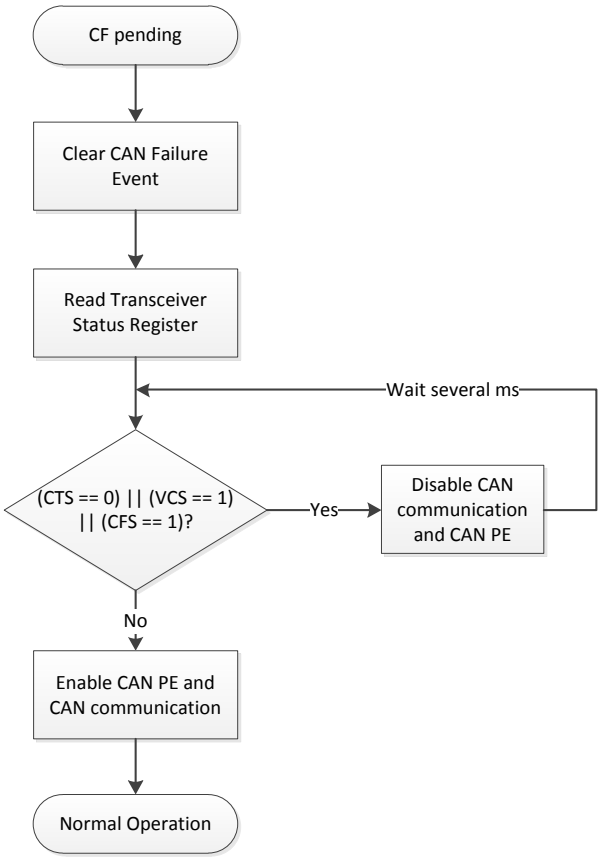


Fig 70. CAN failure operation (Poll Transceiver Status Function)

The CAN failure event (CF) indicates a deactivated transceiver due to a V1 under-voltage or a dominant clamped TXD pin. Evaluating the transceiver status bits is necessary to get further information, when a CAN failure event was triggered. Hence, at first the Transceiver Status Register is read (SPI command: 0x4500). If VCS is ok (VCS = 0), TXD is not clamped dominant (CFS = 0) and the CAN transmitter is enabled (CTS = 1), the CAN communication can continue because the transceiver is active again. If any failure condition persists, it is recommended to disable the CAN PE or at least stop transmitting CAN frames because the CAN transceiver is no active. Active sending on CAN would lead to an increase of the CAN PE failure counter. The CAN PE can be re-enabled or data can be transmitted again, when all failure conditions are gone. Therefore, it is recommended to poll the Transceiver Status Register with a timeout of several ms to prevent a lock of the application in case of a long lasting or permanent CAN failure.

12.2.4 Run Default Application [APPLICATION]

This is the most important part of the software flow and highly depends on the dedicated application. Therefore this chapter only gives an example of what is possible. The execution of the application can e.g. include CAN message routing, periodic microcontroller input pin polling, Wake Pin status polling, periodic event handling. From UJA1168(A) family perspective it is important to keep the SBC in Normal mode with the related watchdog triggers and stop the CAN communication in case of a CAN failure. Therefore the user of the UJA1168(A) has the freedom to adopt the software to its individual needs. Transition to Low Power Operation like Standby and Sleep mode is always possible at any point in time regardless of the actual watchdog expiration time.

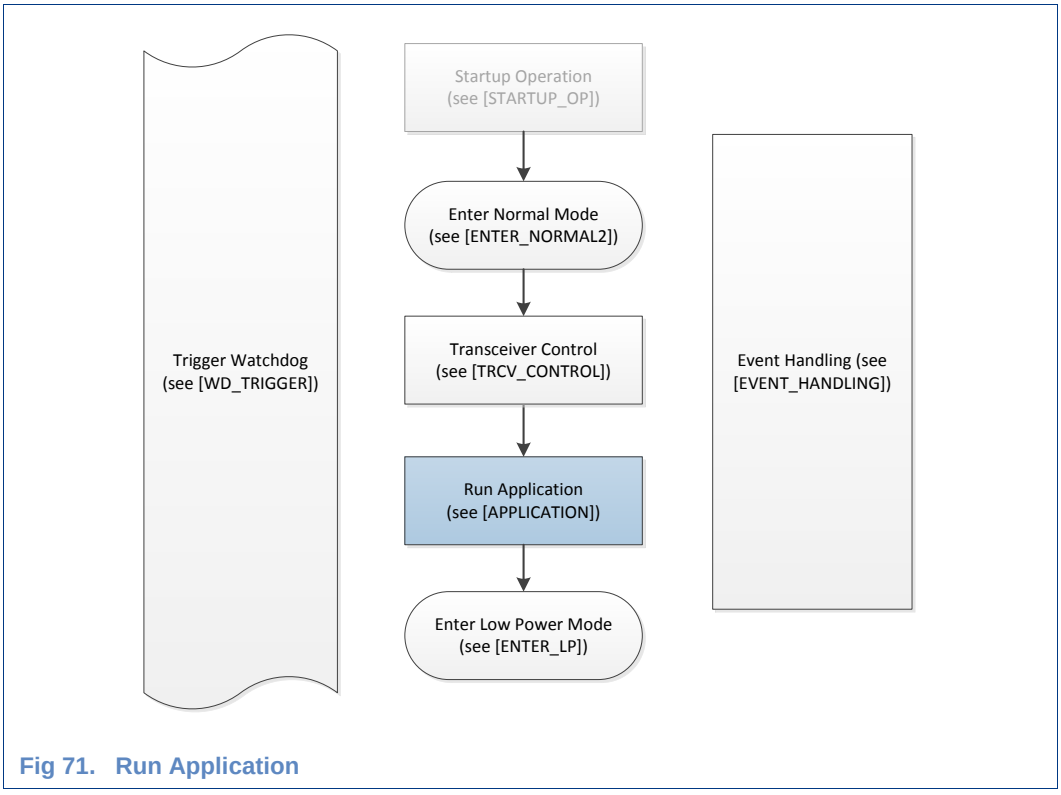


Fig 71. Run Application

12.2.5 Event Handling [EVENT_HANDLING]

The UJA1168(A) SBC has no dedicated pin that signals pending events. In both, Standby and Sleep mode, the RXD pin is used to not only signal a pending CAN wake-up, but also other wake-up and diagnosis events, which are enabled. In Normal mode the RXD pin is used for CAN communication and therefore the Event Status bits need to be polled periodically and pending events need to be handled and cleared.

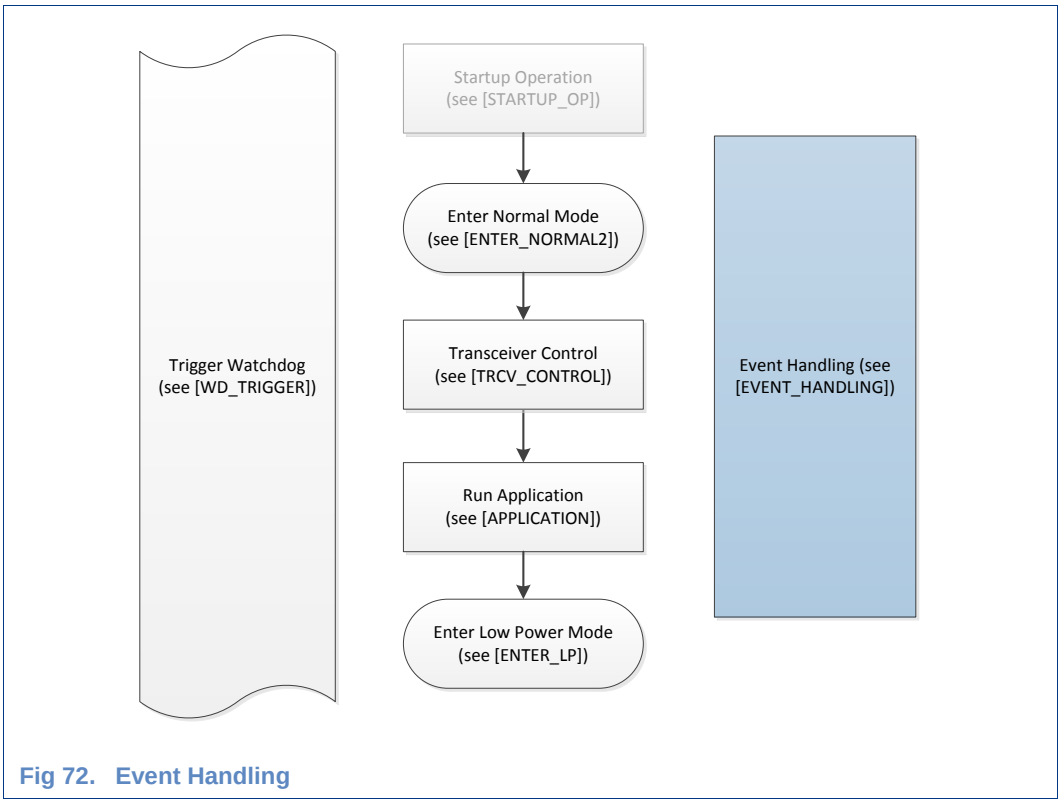


Fig 72. Event Handling

Fig 73 - Fig 77 illustrate the software flow of the Event Handler that is periodically called during Normal Operation. Within the Event Handler the Global Event Status Register is read. This register gives a summary of all possible kinds of pending events and allows getting an overview about event sources by only reading out one register. Hence, having read the Global Event Status Register, the registers in which events are pending are known and should be read out afterwards to identify the pending event sources in detail.

After reading the detailed event registers (e.g. System Event Status Register, Supply Event Status Register, etc.) the read data is evaluated. If a pending event is determined, the associated event service routine is called. The service routine clears the pending event and contains application specific functionality. For example, in case of the CAN failure service routine the CAN PE is disabled according to Fig 70.

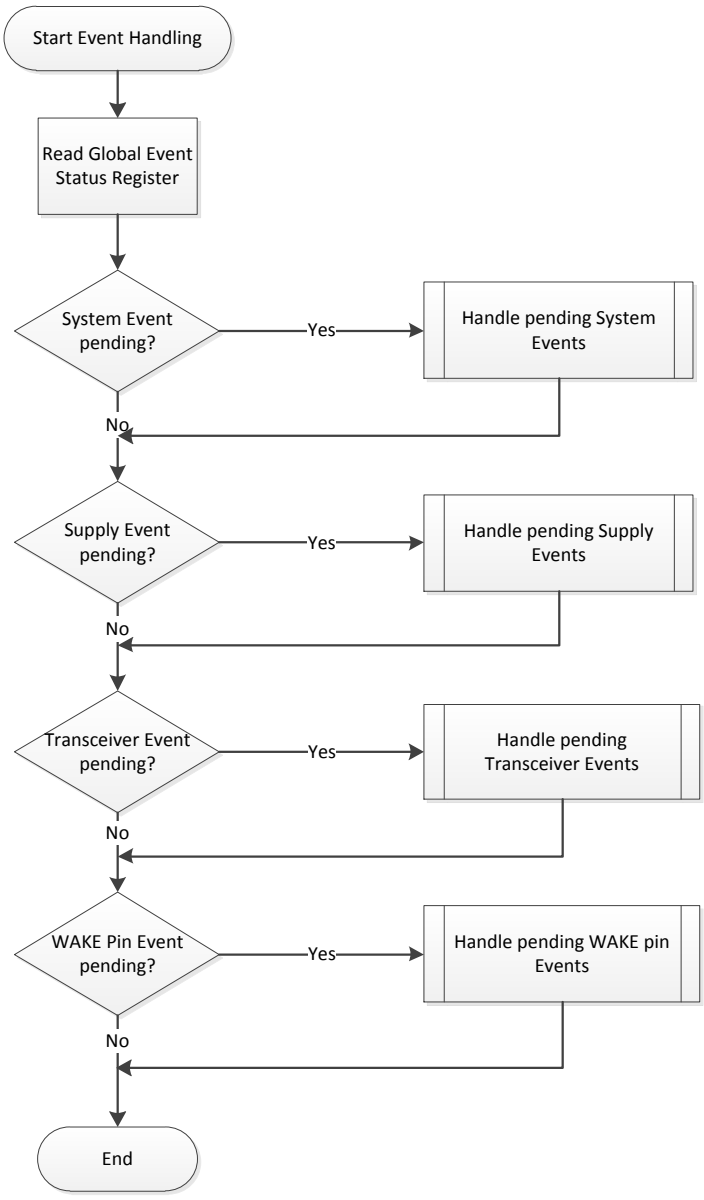


Fig 73. Software Flow of Event Handling

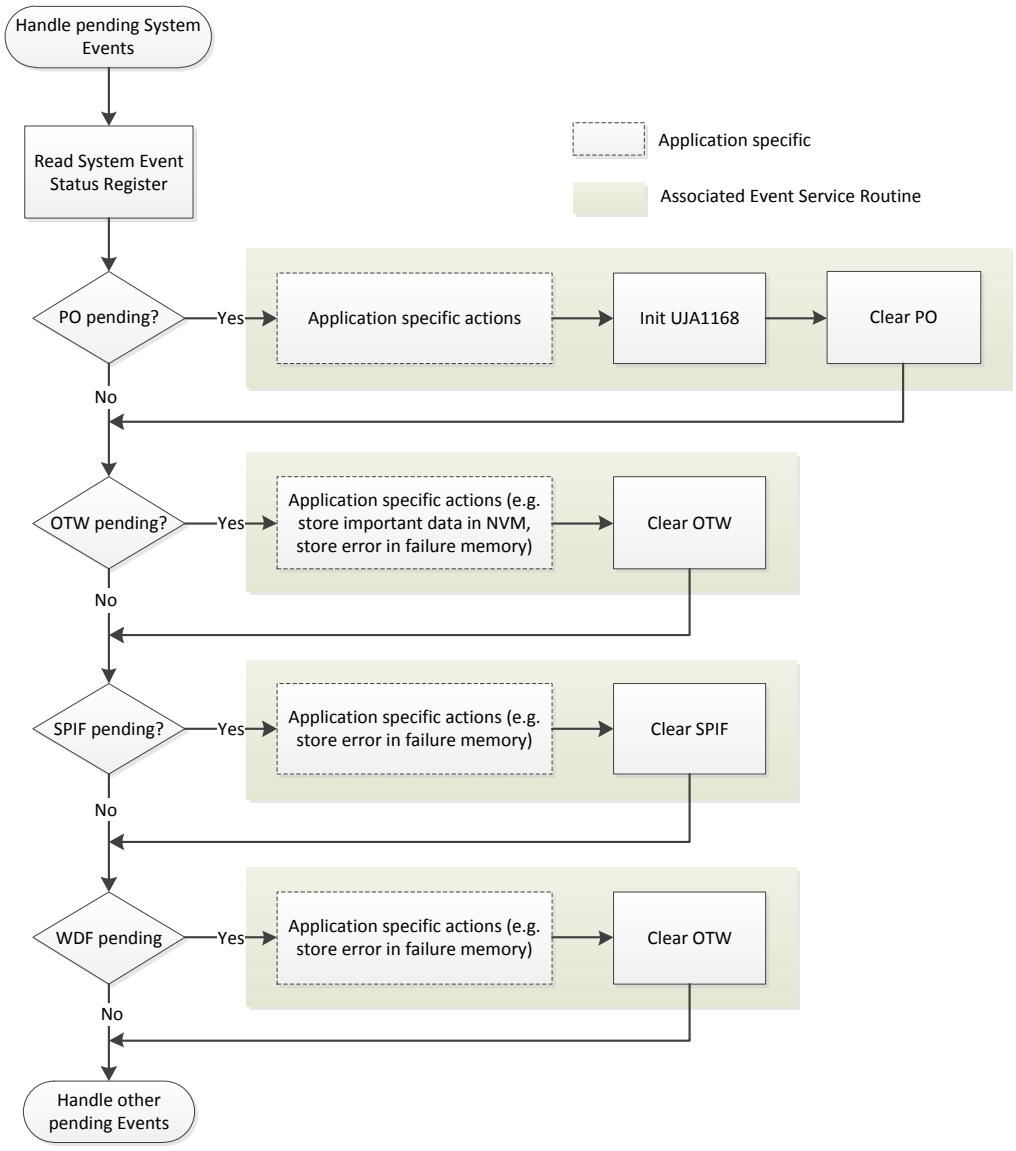


Fig 74. Handle pending System Events in Event Handler

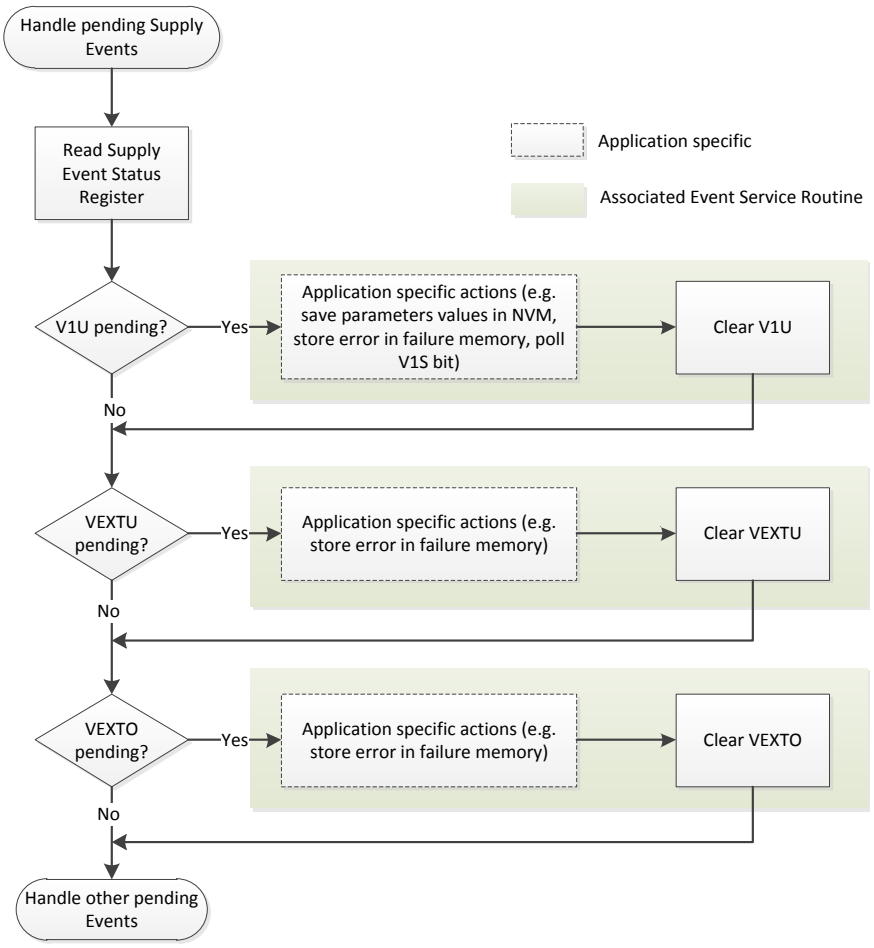


Fig 75. Handle pending Supply Events in Event Handler

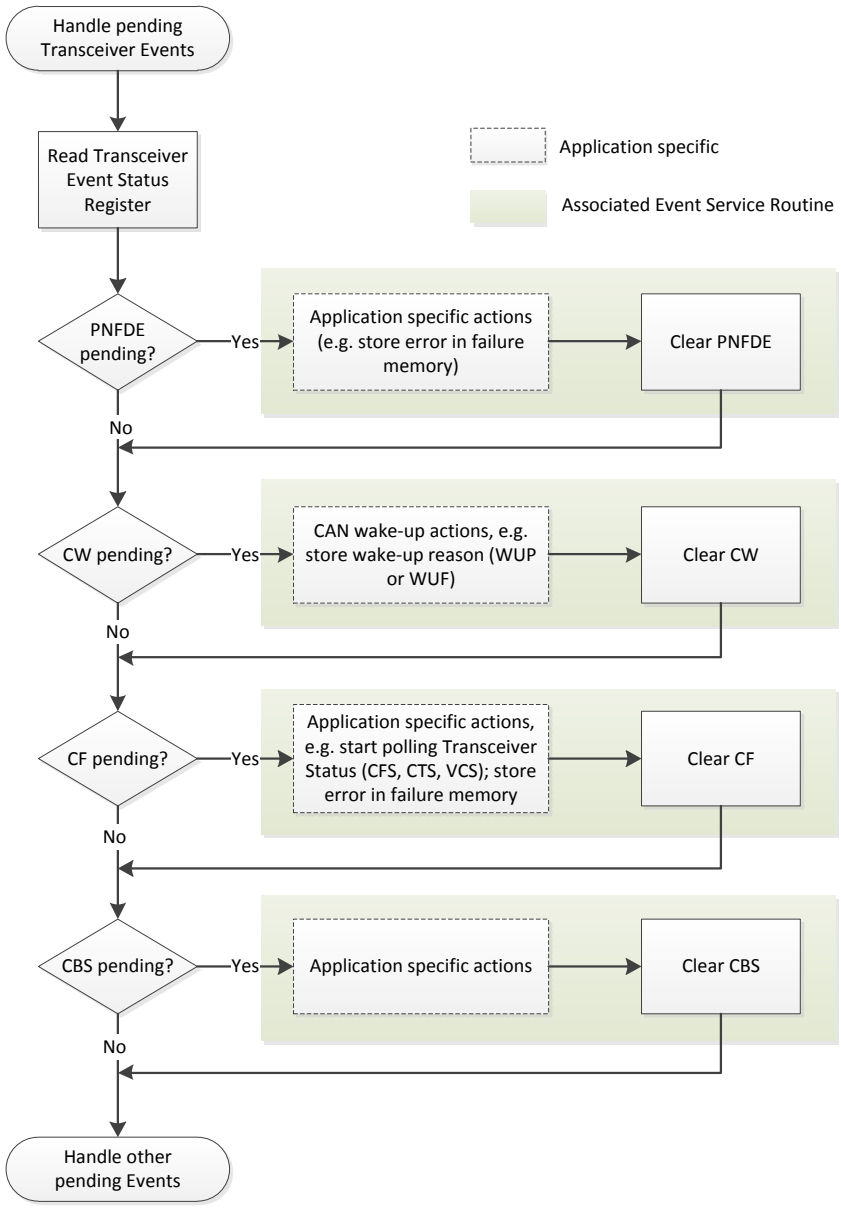


Fig 76. Handle pending Transceiver Events in Event Handler

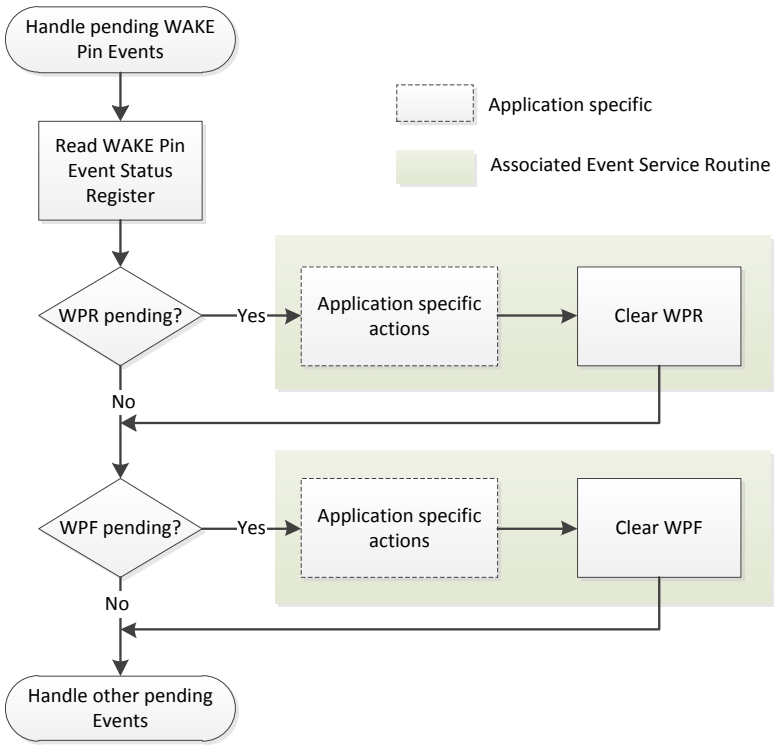


Fig 77. Handle pending WAKE Pin Events in Event Handler

12.2.6 Transition to Low Power Operation [ENTER_LP]

Low Power mode is entered by writing e.g. 0x0201 (Sleep mode) or 0x0204 (Standby mode) to the Mode Control Register. It is important to enable at least on wake-up source before entering SBC Sleep mode. Without having any wake-up source active (CAN or WAKE) the SBC will perform a reset in order to prevent a dead-lock situation (Sleep mode forever). For more information on Low Power Operations refer to chapter 12.3.

12.3 Low Power Operation [LOWPOWER_OP]

This section introduces the software operations, which are associated to Low Power Operation of the application. It is related to the Standby and Sleep mode of the UJA1168(A) family. The difference between both modes is the amount of power that can be saved. In Sleep mode the current consumption is at its minimum but the delay between a wake-up event and restart of the application is longer, because the system has to start from an un-powered condition, since V1 is disabled in Sleep mode. In Standby mode the current consumption is slightly higher compared to Sleep mode with the benefit of a much shorter delay between a wake-up event and re-start of the application. Therefore the following subchapters discuss the Standby and Sleep mode in more details.

As illustrated in Fig 78, Low Power Operation can be entered directly from Normal mode via an SPI command. Moreover, Sleep mode can also be entered via a temporary transition to Standby mode by using two consecutive SPI commands (1st: enter Standby mode, 2nd: enter Sleep mode). All mode transitions are performed by the dedicated SPI commands.

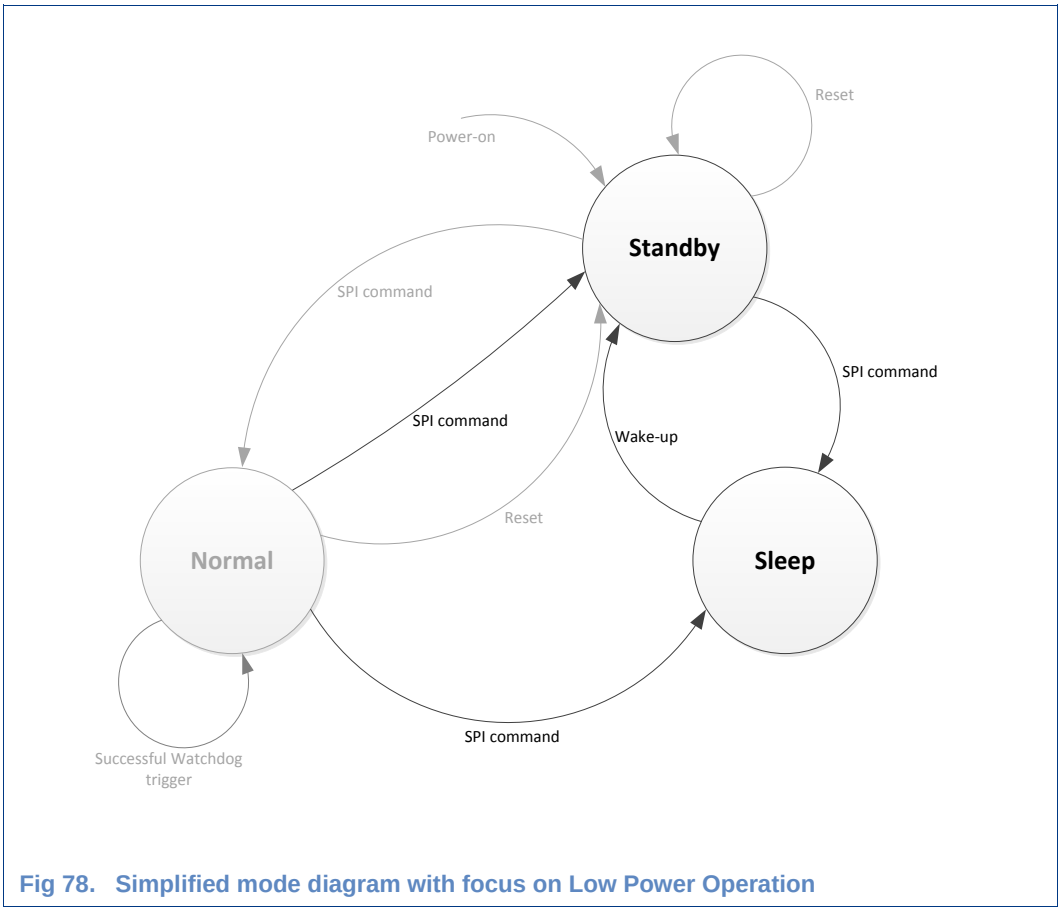


Fig 78. Simplified mode diagram with focus on Low Power Operation

12.3.1 Wake-Up Handling [WAKEUP_HANDLING]

All different events located in the Event Status registers can be used as a wake-up event from Low Power Operation. A watchdog failure (WDF), VEXT over- (VEXTO) or undervoltage (VEXTU), Partial Networking frame detection error (PNFDE) and CAN Bus Silence can be used as wake-up even from Sleep mode beside the regular wake-ups via CAN and WAKE.

The UJA1168(A) SBC does not distinguish between regular wake-up events and diagnostic events. For that reason every enabled event source also causes a wake-up out of Low Power. So after awaking out of Low Power mode the RXD pin is forced low, as long as the event is pending.

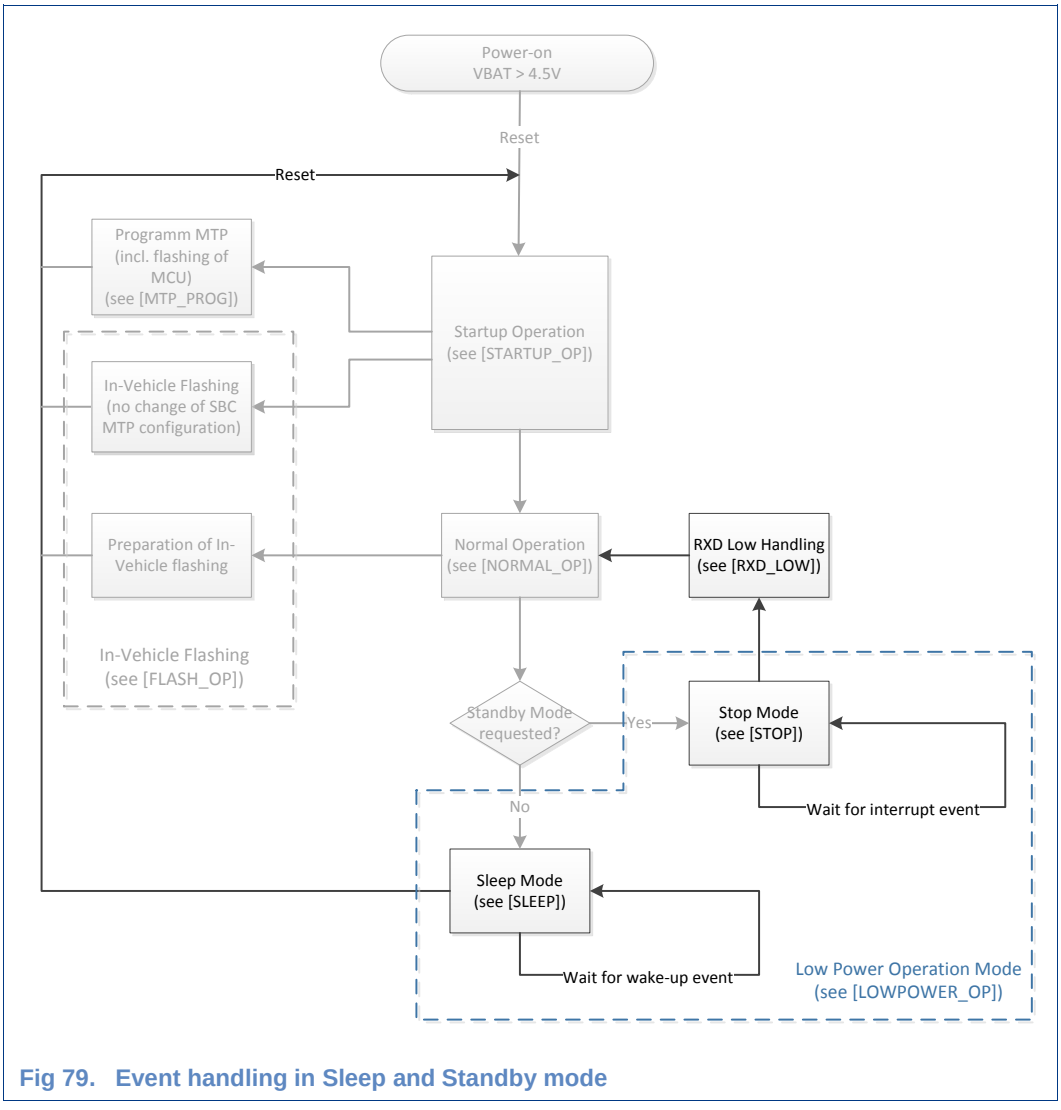


Fig 79. Event handling in Sleep and Standby mode

In case of wake-up out of Sleep the “event handling” is performed by the Startup Operation because it is linked to a system reset event with powering up the application (chapter 12.1). The only difference is the trigger root of the Startup Operation, which is a wake-up event and not a reset. For further information please read chapter 12.1.8.

In case of wake-up out of Standby the “event handling” is performed by the interrupt service routine, triggered by the falling edge of the RXD pin. Hence, event handling is called “RXD Low Handling” in this case. This function differs slightly from the Event Handling done after Startup or during Normal Operation because additional actions are required for some events e.g. Enter Stop mode again. Further information is given in the following chapter.

12.3.1.1 RXD Low Handling [RXD_LOW]

Fig 80 illustrates the software flow of the RXD Low Handling. When any kind of event is pending in Standby mode, the RXD pin is forced on low level. The interrupt service can be implemented in the microcontroller with an CAN Controller Wake-up interrupt that is triggered with a falling edge of the RXD pin or by reading the Global Event Status Register on a regular basis (polling).

The Global Event Status Register gives a summary of all possible kinds of pending events and allows getting an overview about event sources by only reading out one register. After a read access to the Global Event Status Register, the registers are known in which events are pending and which should be read out afterwards to identify the pending event sources in detail.

After reading the detailed event registers (e.g. Transceiver Event Status Register, System Event Status Register, Supply Event Status Register) the read data are evaluated. If a pending event is determined, the related service routine is called. The service routines are application specific functions and depend on the need of the application. For example, in case of the V1 under-voltage warning event important information can be stored in NVM in order not to lose it.

Fig 80 illustrates the general software flow, if RXD is pulled low. Fig 81 to Fig 84 show the recommended flow of the sub processes in case of an RXD Low (CAN wake-up) interrupt.

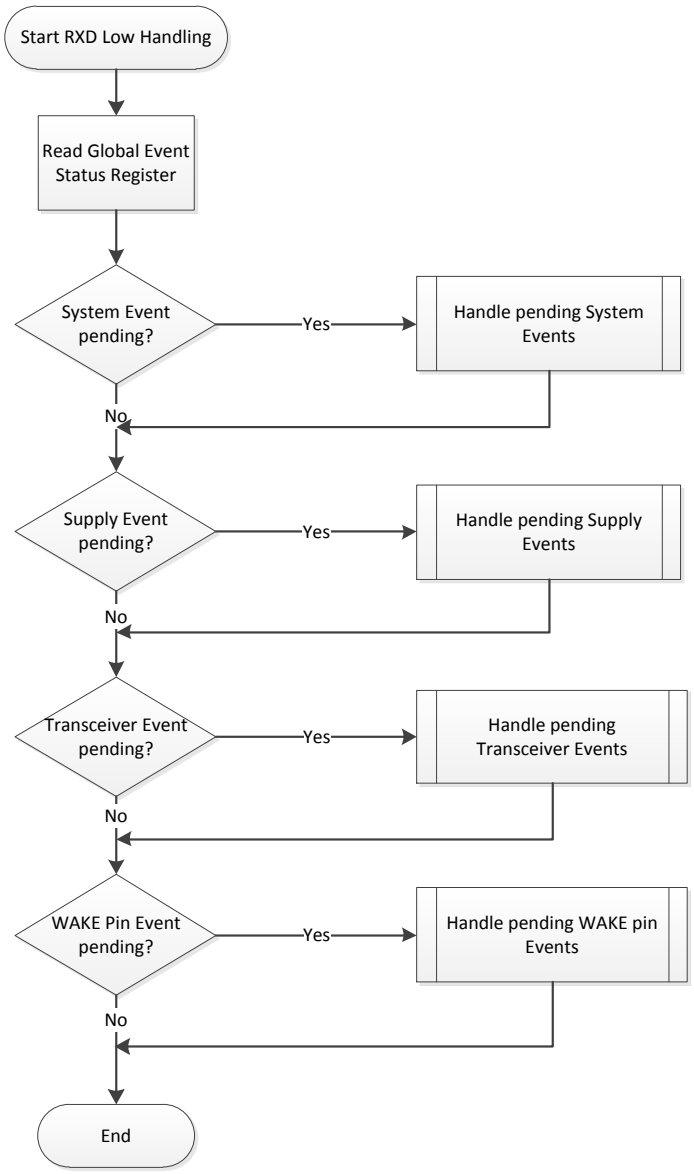


Fig 80. Software flow of RXD Low Handler

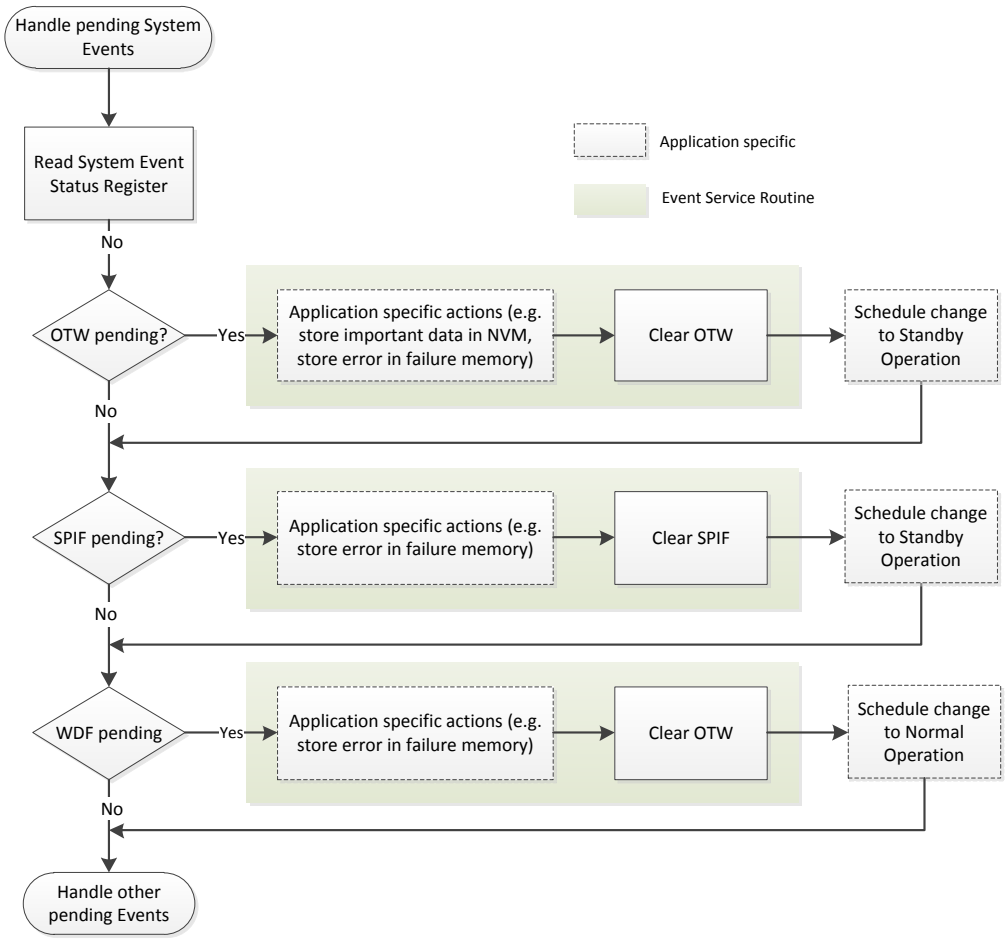


Fig 81. Handle pending System Events in RXD Low Handler

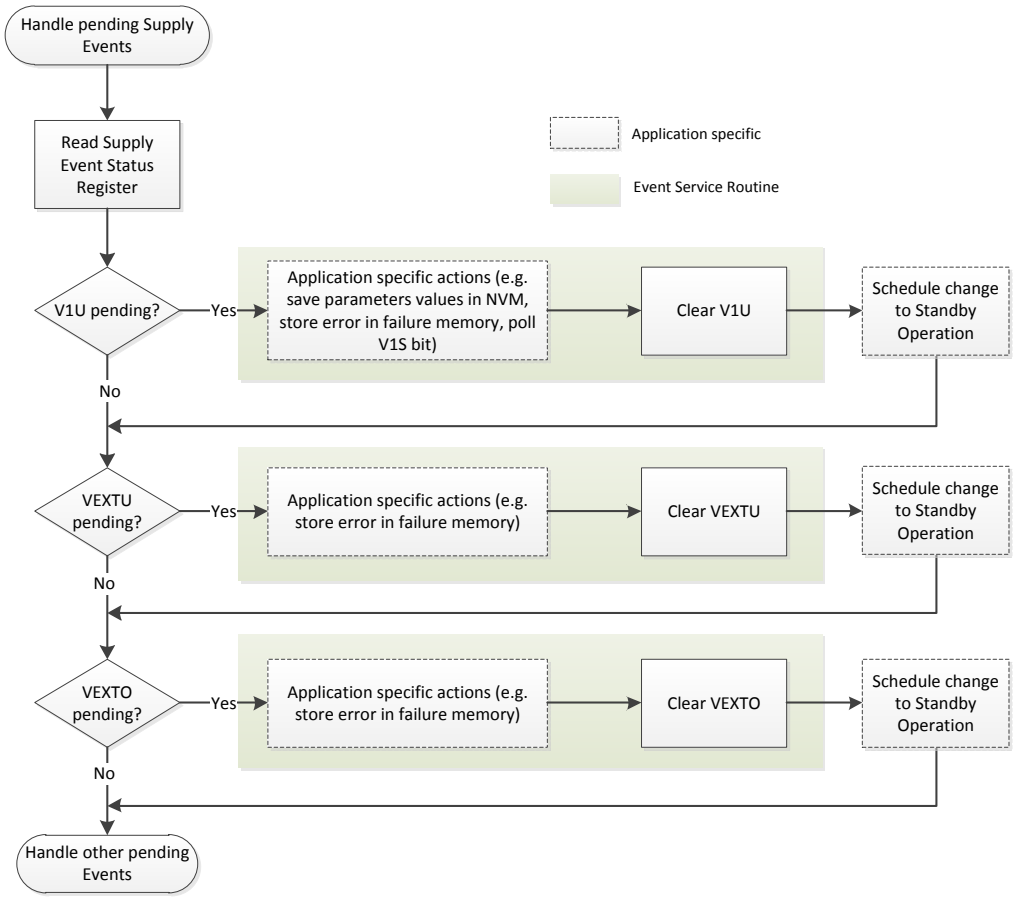


Fig 82. Handle pending Supply Events RXD Low Handler

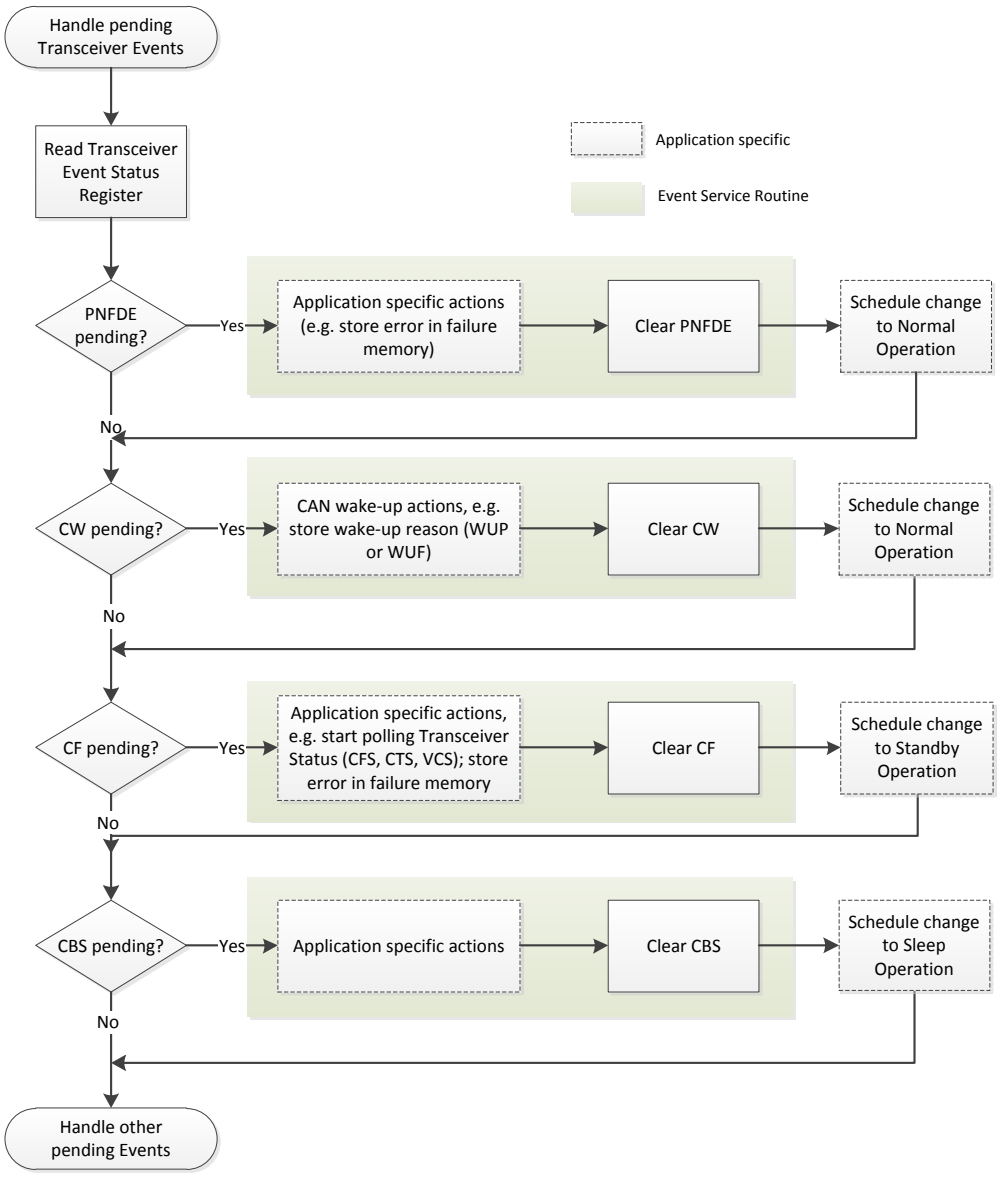


Fig 83. Handle pending Transceiver Events RXD Low Handler

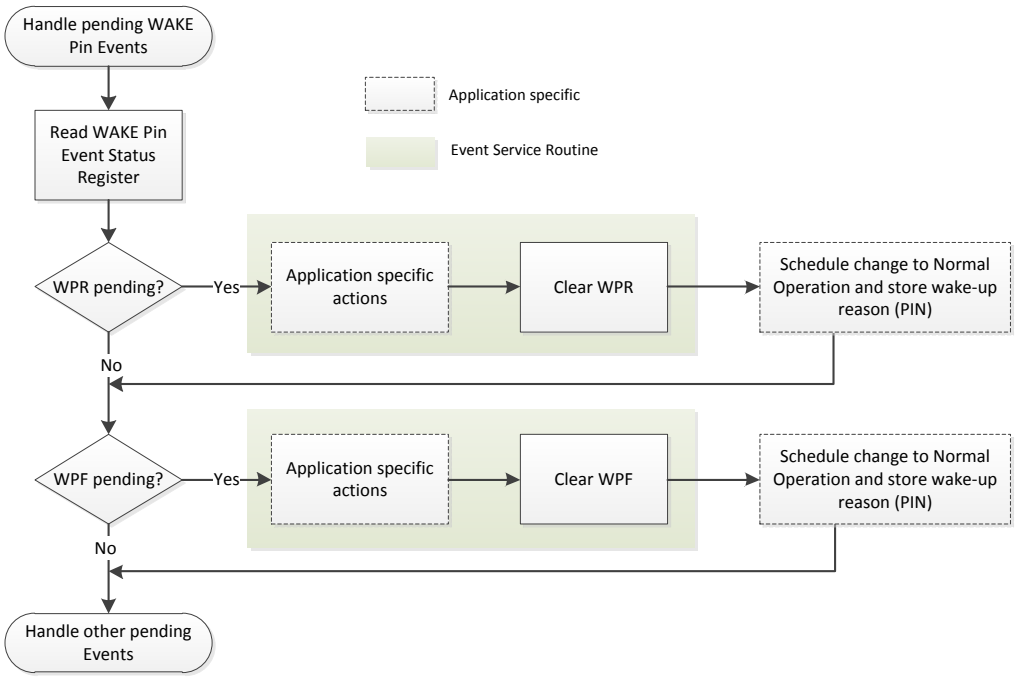


Fig 84. Handle pending WAKE Pin Events RXD Low Handler

12.3.2 Sleep Operation [SLEEP]

Sleep mode is a special kind of Low Power Operation. It can be entered from Standby and Normal mode via the SPI command 0x0201, which is a write access to the Mode Control Register. There are several possibilities to leave Sleep mode and to enter Standby mode, e.g. wake-up event on CAN or on the WAKE pin or diagnostic events. How to leave Sleep mode depends on the events which are enabled when entering Sleep mode.

After a wake-up event the startup operation is performed. For more information on startup operations refer to chapter 12.1.

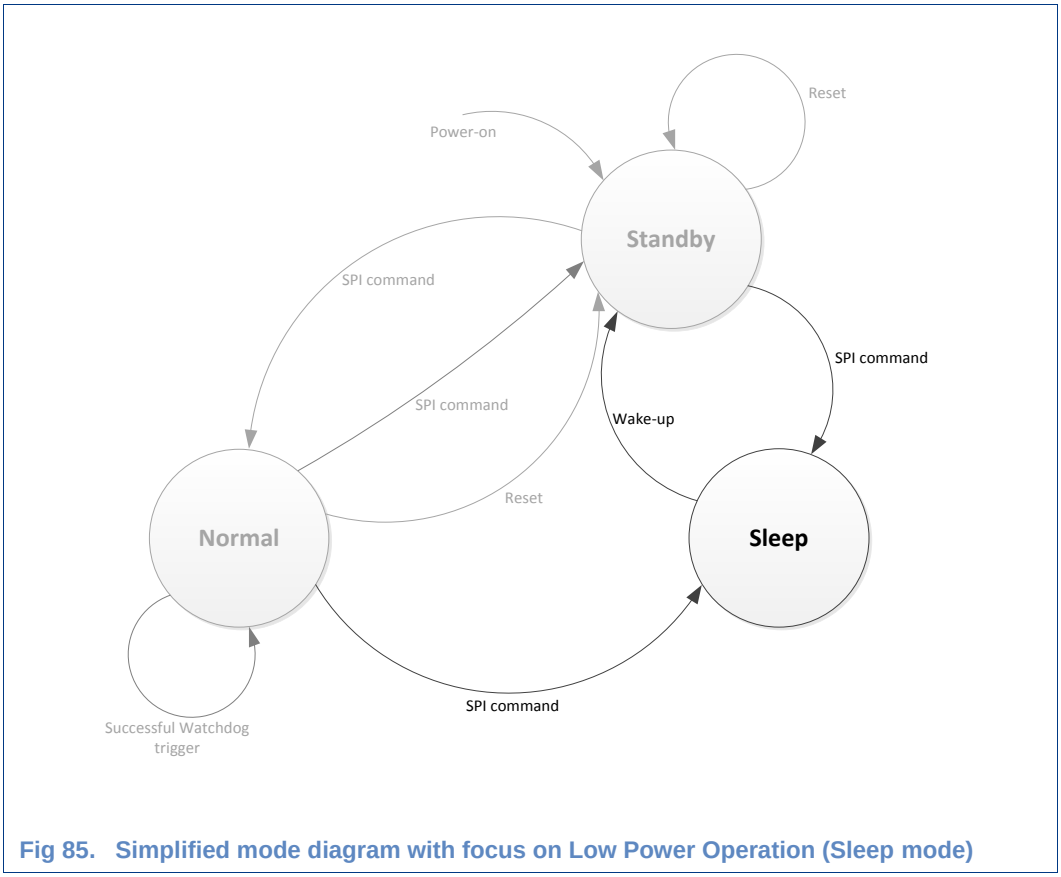


Fig 85. Simplified mode diagram with focus on Low Power Operation (Sleep mode)

The software flow for entering Sleep mode is shown in Fig 86 on the next page.

The first action during Sleep mode preparation is to check if the required wake-up sources are enabled in Sleep mode. Entering Sleep mode without any active wake-up source will end up into a reset in order to prevent a possible dead-lock without any wake-up activated. Therefore at least one regular wake-up source must be enabled.

If the wake-up configuration in Sleep mode is successfully checked, CAN communication is stopped (if still enabled) and all wake-up sources for Sleep mode are enabled by write accesses to the related Event Enable Registers. For example, the SPI command 0x4601 enables the CAN wake-up. Furthermore, the CAN Partial Networking Control (CPNC) bit can be configured, if desired, in the CAN Control Register.

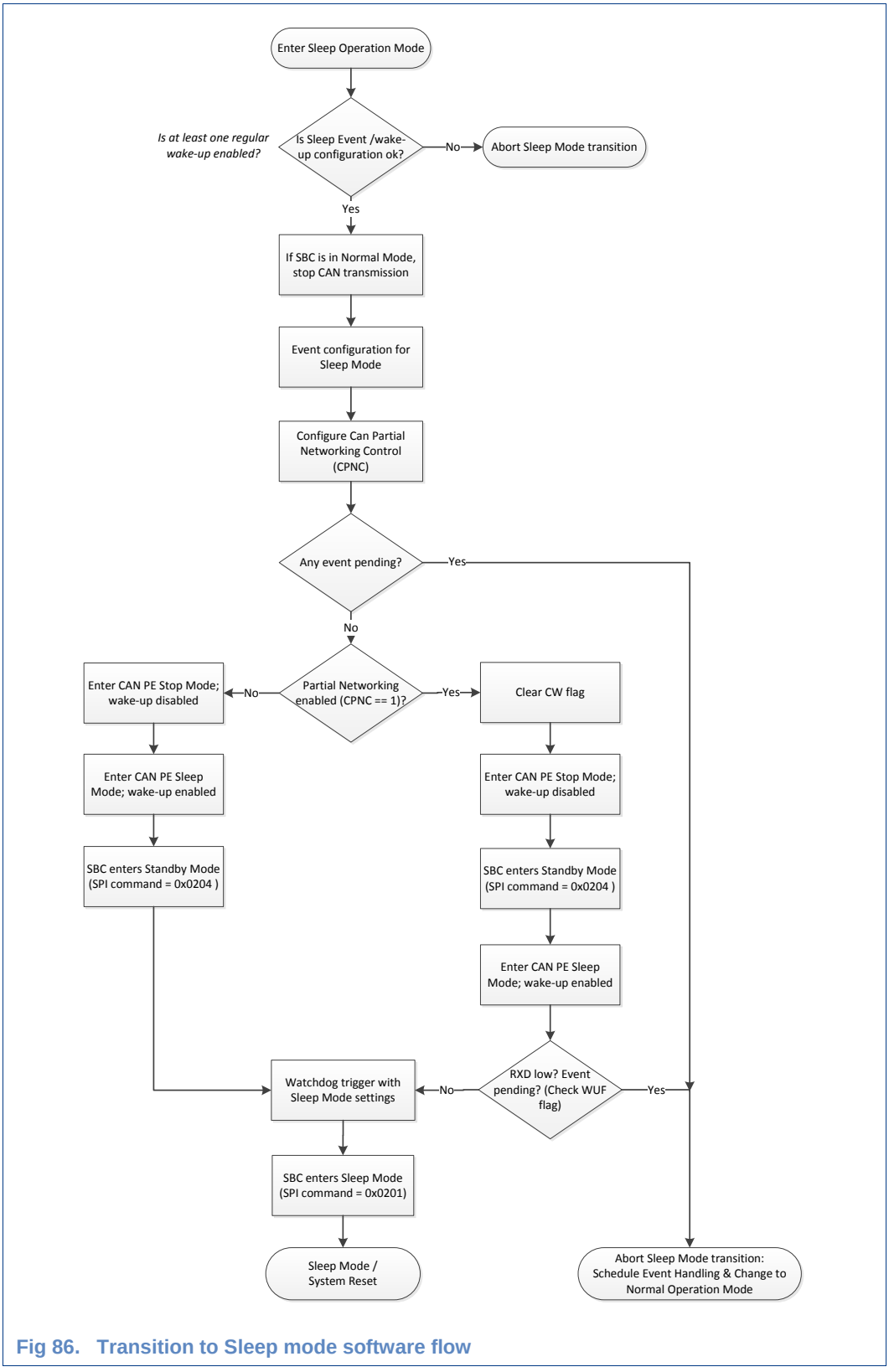


Fig 86. Transition to Sleep mode software flow

When the wake-up sources and CPNC bit are configured properly, the software can check if events are still pending. Therefore a read access to the Global Event Status

Register is performed (SPI command: 0xC100). If any event is pending the UJA1168(A) cannot enter Sleep mode and an attempt to enter Sleep mode would lead to a system reset. Therefore, the Sleep transition should be aborted (change to Normal Operation and Event Handing). If no event is pending and CAN Partial Networking is disabled, the CAN PE is put into Sleep mode and afterwards the UJA1168(A) enters Standby mode, by a write access to the Mode Control Register (SPI command: 0x0204).

If no event is pending and CAN Partial Networking is enabled, a special shutdown sequence is necessary in order not to lose any event:

1. The CW flag in the SBC is cleared.
2. The CAN PE is put into Stop mode (wake-up disabled) in order not to wake-up on any CAN communication, until the SBC has entered Standby mode.
3. Then SBC is put into Standby mode (SPI command = 0x0204)
4. The CAN PE is put into Sleep mode (wake-up enabled) to allow signalling every SBC event by a CAN wake-up interrupt.
5. As there might have occurred an event in between change of CAN PE from Stop to Sleep mode and RXD might be on low level (especially for edge sensitive CAN Controller), e.g. due to CAN wake-up frame, a read access to the Global Event Status Register must be performed (SPI command: 0xC100). If an event is pending, the Sleep transition should be aborted (Change to Normal Operation and Event Handing).

Having successfully configured the CAN PE to Sleep mode and the SBC to Standby mode, the watchdog can be reconfigured, if desired, and finally the SBC can enter Sleep mode with a SPI write access (SPI command: 0x0201) to the Mode Control Register.

12.3.3 Standby Operation [STANDBY]

A different kind of Low Power Operation is the so called Stop or Sub Clock operation. This operation is related to the Standby mode of the UJA1168(A) because it requires a supplied microcontroller. Stop or Sub Clock operation is a low power feature of the microcontroller itself. Therefore, it will take place in Standby mode of the UJA1168(A) and a wake-up from Stop/Sub Clock operation will not lead to mode changes of the UJA1168(A).

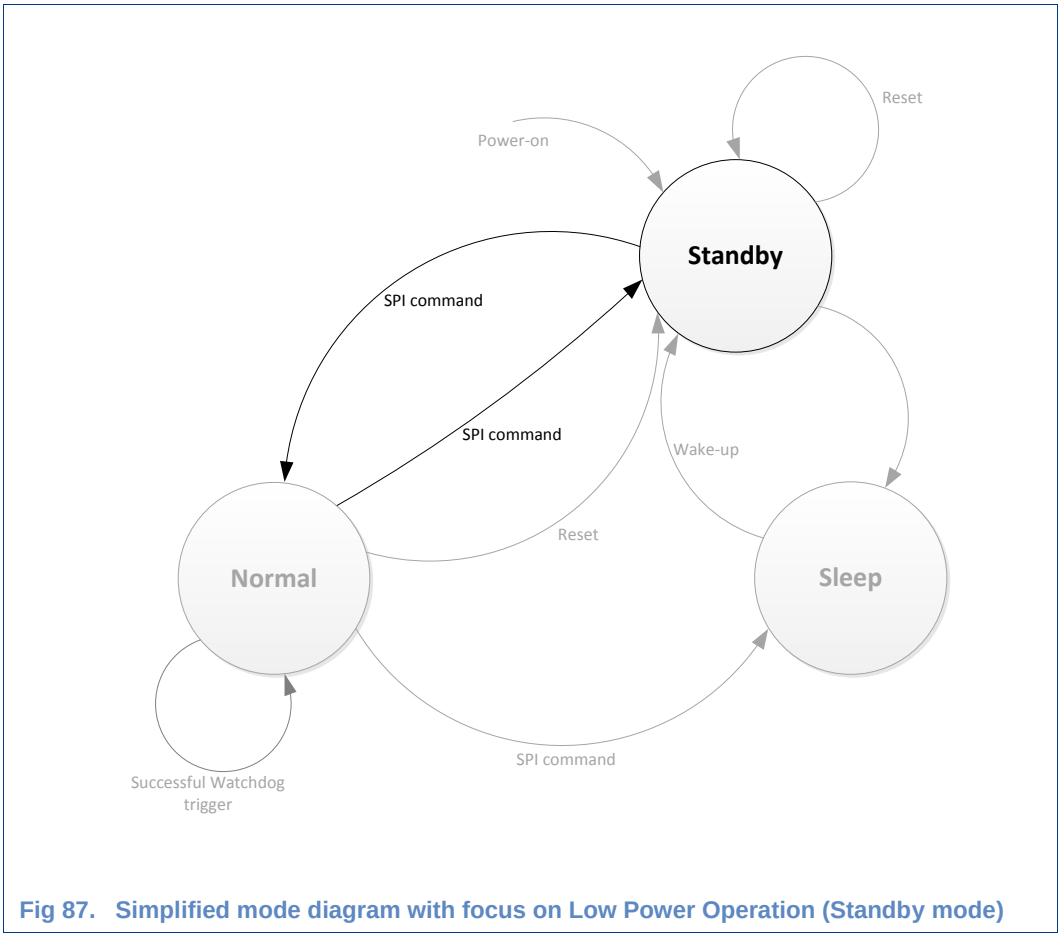


Fig 87. Simplified mode diagram with focus on Low Power Operation (Standby mode)

Stop or Sub clock operation can be realized by two different ways that are discussed within the next subchapter. One part is the pure Stop operation and the other one is the cyclic wake-up out of Stop operation.

12.3.3.1 Stop mode / Sub Clock mode [STOP]

Fig 88 shows the required actions before entering Stop mode. The first part of the Stop Operation is to check if the necessary wake-ups will be enabled in Stop mode. If the wake-up configuration in Standby mode or rather Stop Operation is successfully checked, the CAN communication is stopped (if still enabled) and the wake-up sources for Standby mode are enabled by write accesses to the related Event Enable Registers. For example, the SPI command 0x4601 enables the CAN wake-up source. Furthermore, the CAN Partial Networking Control (CPNC) bit must be configured in the CAN Control Register.

When the event sources and CPNC bit are configured properly, the software can check if events are still pending. This is done by a read access to the Global Event Status Register (SPI command: 0xC100). If an event is pending for safety reasons the watchdog of the UJA1168(A) cannot be disabled and therefore no Stop mode of the microcontroller is possible; hence also no SBC Standby mode is feasible. As consequence the transition to Stop Operation should be aborted (change to Normal Operation and handle event).

If no event is pending, than depending on the CPNC configuration the CAN PE is brought into Sleep mode and the UJA1168(A) is put into Standby mode in a special sequence (chapter 12.3.2 or Fig 88). In case CPNC is set to 1 (Partial Networking enabled) an additional check of the Global Event Register is required, to ensure that no event has occurred in the meantime.

If still no event is pending, the watchdog can be disabled by setting the Watchdog mode Control bit in the Watchdog mode Control Register to Autonomous mode (WMC = 1). Any event will automatically re-enable the watchdog. When the watchdog is disabled, and RXD is high, the Stop/Sub Clock operation of the microcontroller can be entered by disabling the oscillator completely or switching to a lower clock frequency.

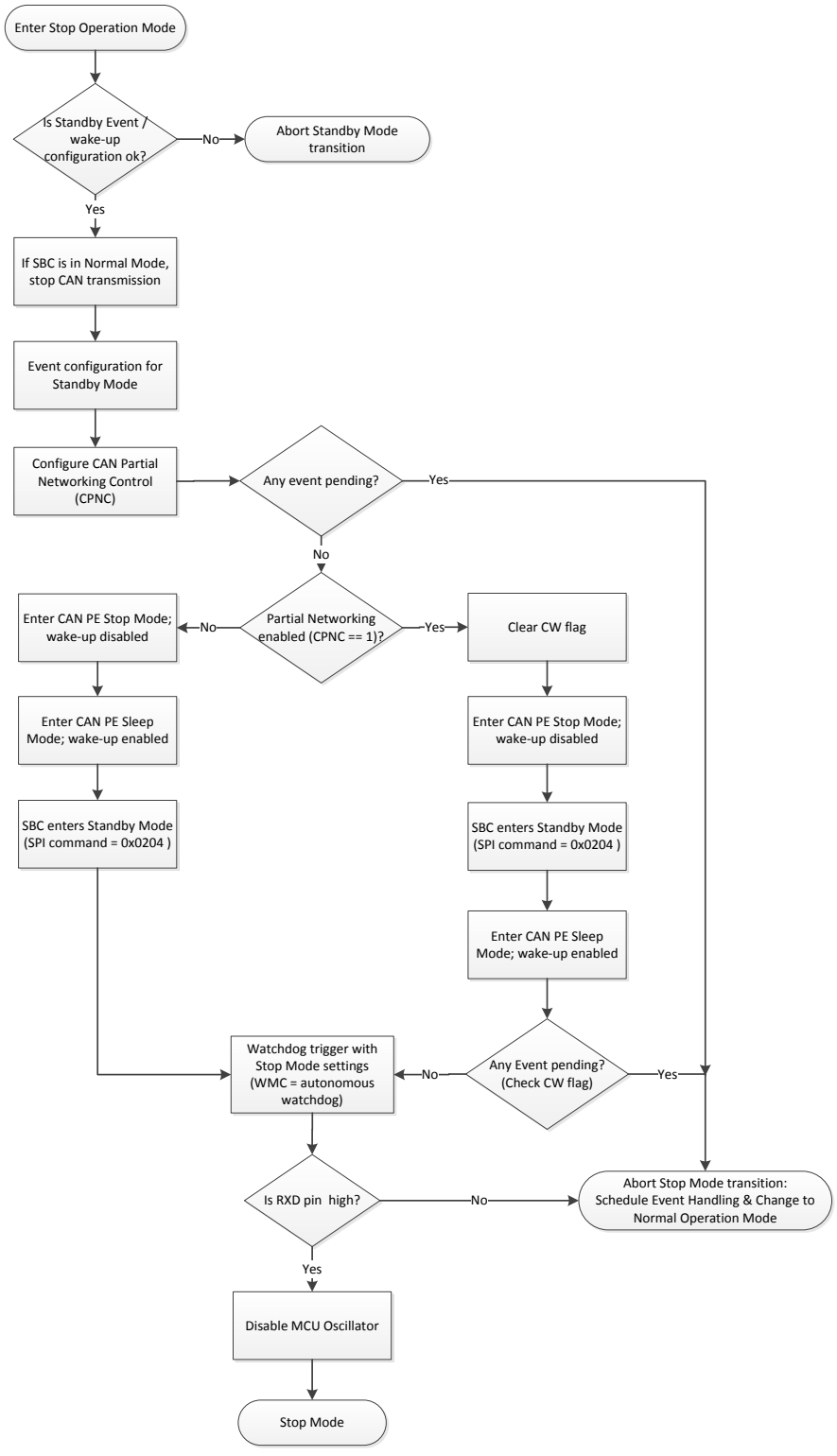


Fig 88. Transition to Stop mode software flow

12.3.3.2 Cyclic Wake-up out of Stop mode / Sub Clock mode

The software flow of entering Stop mode with cyclic wake-up is similar to that one introduced in the previous subchapter about pure Stop mode. The only difference is the configuration of the watchdog (see Fig 89). Here the watchdog continues to run while the microcontroller stops operation. The idea is that an overflowing watchdog wakes-up the microcontroller cyclically depending on the selected watchdog period time.

Therefore, the UJA1168(A) must be in Standby mode, the related events must be enabled and no events are pending. If all these conditions are fulfilled the UJA1168(A) watchdog must still be enabled while disabling the microcontroller's oscillator. The watchdog is enabled in Standby mode by e.g. writing 0x0047 via SPI to the Watchdog Control Register. This SPI command enables the Timeout Watchdog and hence, the Cyclic Wake with a period of 4096ms because the configured nominal watchdog period (NWP) is 0x7. A watchdog overflow (after 4096ms) triggers the WDF bit and wakes up the microcontroller out of stop mode with a falling edge on the RXD pin. The release of the WDF bit should not be done within the interrupt service routine because the interrupt mechanism could still work when the rest of the application is broken. Therefore it is recommended to handle the WDF within the application.

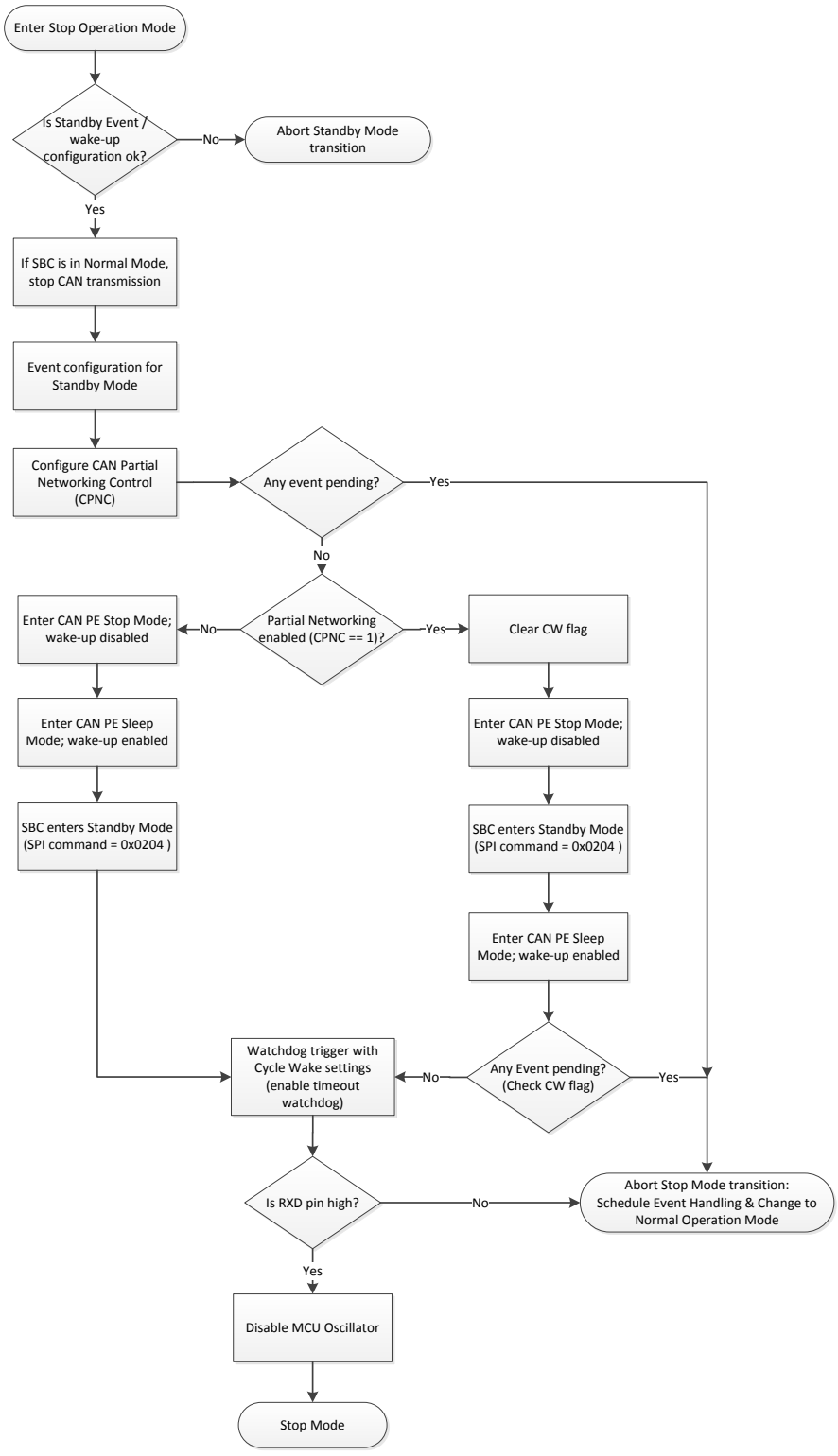


Fig 89. Software flow of transition to Stop mode with Cyclic Wake feature

12.4 Software Development mode

For software development support the UJA1168(A) provides a special mode to ease software design. This mode is configured via the Software Development mode Control (SDMC) bit in the SBC Configuration Control register. Hence, if Software Development mode shall be activated the MTPNV must be reprogrammed at first.

In Software Development mode the watchdog is off by default. After a reset or power-on in Software Development mode the WMC bits in the Watchdog Control Register are set to 0x1 (Autonomous mode). In contrast, WMC is 0x2 (Timeout Watchdog) after a reset or power-on, if Software Development mode is deactivated.

In Software Development mode no watchdog control is required, thus by default no watchdog resets are possible and no cyclic wake is available. Nevertheless, it is possible to activate and reactivate the watchdog via change of the WMC bits, if desired for test purposes.

The status of the watchdog can be identified by software by reading the Watchdog Status (WDS) bits in the Watchdog Status Register (SPI command: 0x0B00). The WDS bits indicate the current status of the watchdog: off, 1st half or 2nd half of the watchdog period. If the read data of the SPI command is e.g. 0x0B04 the SBC is in Software Development mode and the watchdog is off.

The watchdog can be activated at any point in time in Software Development mode, when the WMC bit is reconfigured to either Timeout mode (WMC = 0x2) or Window mode (WMC = 0x4). Otherwise, it can also be deactivated again by setting Autonomous mode (WMC = 0x1). This should be considered in software design, in order to prevent that the WMC bit is not unintentionally changed by a watchdog trigger. To prevent unintended watchdog activation in Software Development mode, the watchdog should always be triggered with WMC = 0x1 or rather watchdog trigger should be suppressed.

12.5 In-Vehicle Flash Operation [FLASH_OP]

This chapter will not explain how to flash a device within a vehicle according e.g. the H.I.S. Standard (Hersteller Initiative Software). It only shows, what needs to be considered and how to put the UJA1168(A) into a relaxed watchdog mode, which allows watchdog services and flash programming in parallel. The advantage of the Timeout Watchdog is that the trigger period is 2 times the Nominal Watchdog Period (NWP). Therefore, the longest period in Timeout Watchdog mode is 2x4096ms. This time is sufficient even for slow Flash memories with long sector erase times.

Fig 91 shows the flow chart of the In-Vehicle Flash operation according to H.I.S. and Fig 90 illustrates the impact of the In-Vehicle flashing for the UJA1168(A) software flow. Fig 90 shows what needs to be done at which point in time during the In-Vehicle Flashing process and summarizes the most important steps.

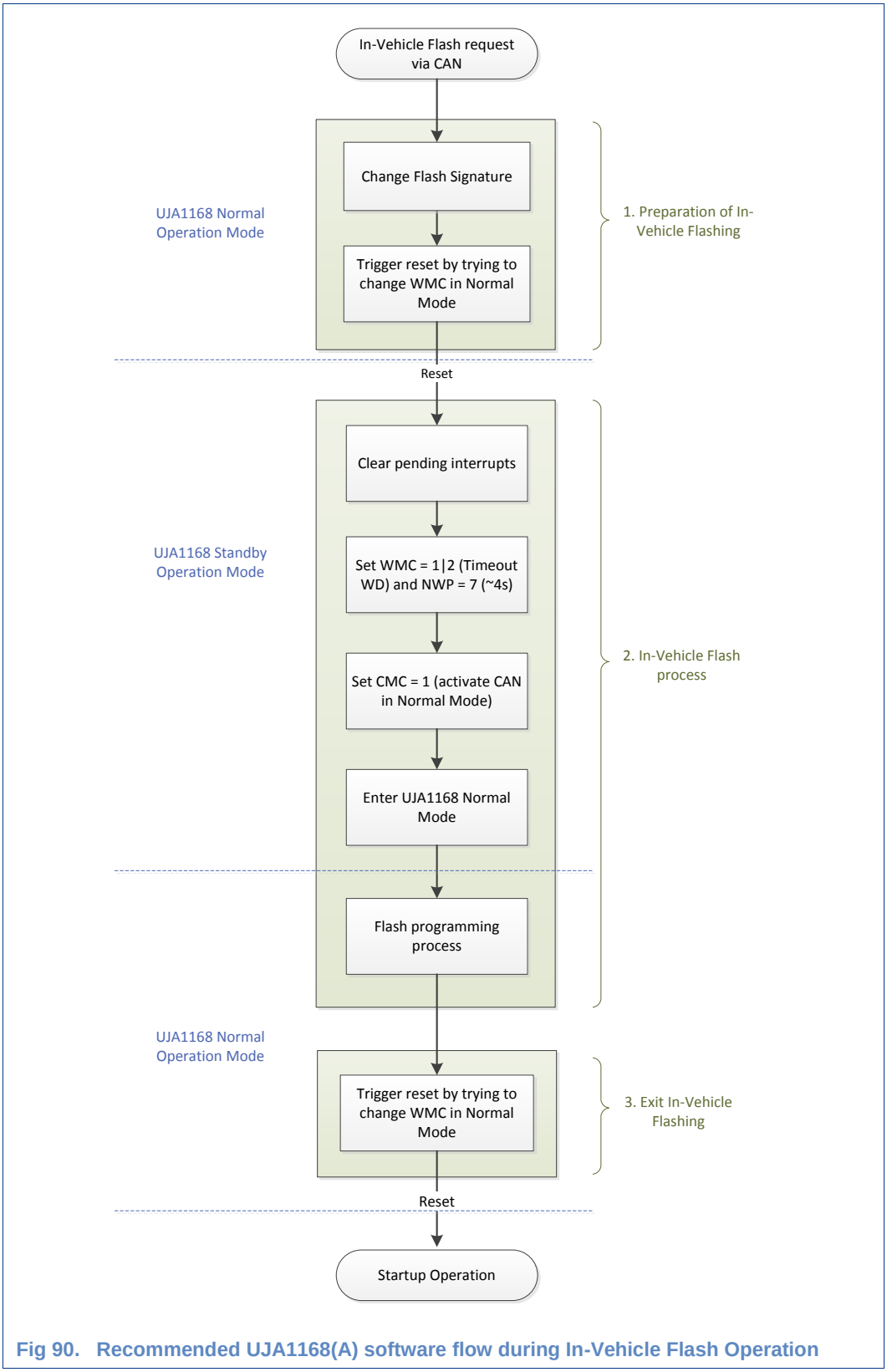


Fig 90. Recommended UJA1168(A) software flow during In-Vehicle Flash Operation

The typical starting point of the Flash Operation is the reception of the flash request via CAN in Normal Operation, which usually sets corresponding user defined control bits in the memory of the system or changes the flash signature in the Flash Memory Controller (FMC) of the microcontroller.

The first step of the software flow is the preparation of the programming process. After that process a system reset is requested. This can easily be done by changing the Watchdog Mode Control (WMC) bit in UJA1168(A) Normal mode. A change of the WMC bit in Normal mode immediately forces a system reset.

After the reset the Startup Operation is not entered because of the request for a flash update (user defined control bits or an evaluation of the flash signature cause this branch in the software flow). Now step 2 takes place. Before entering Normal mode it has to be ensured that:

- No event is pending
- The watchdog is configured to Timeout mode in UJA1168(A) Normal mode (WMC = 1 | 2). If this is not the case a transition to Normal mode will change the watchdog to Window mode and this is not the intended behavior during flashing the application.
- The watchdog is configured to a long nominal watchdog period, e.g. 4096ms (NWP = 7).
- The CAN Transceiver is enabled by setting CMC = 1 in CAN Control Register.

As long as the watchdog is triggered within a time that is shorter than 2xNWP (no window required to be met), the UJA1168(A) will stay in Normal mode.

If the complete data packages are flashed, the software consistency is checked and the user defined control bits are refreshed accordingly, the third step is executed. This requires an additional reset that can be done by changing the WMC bit back to the original setting. After that the normal Startup Operation starts again without entering the flash routines.

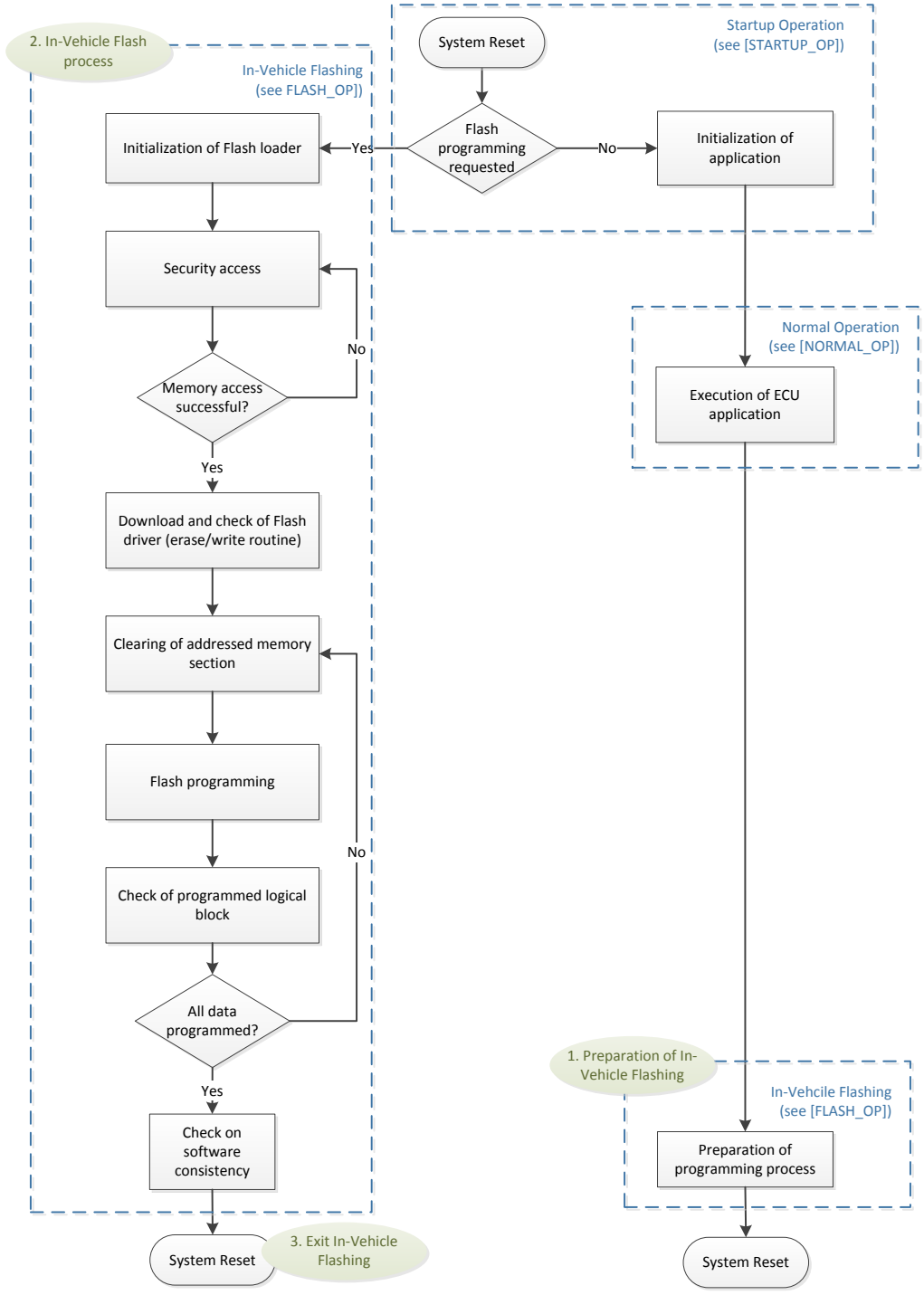


Fig 91. In Vehicle Flash operation flow chart according to H.I.S.

12.6 UJA1168/VX/FD (A/X/F) Software Flow compared to other derivatives

Beside Example Code for the UJA1168/VX/FD (A/X/F) also example software for the UJA1167/VX (A/X) and the UJA1164(A) is included in this Application Hints. See Table 24 for further information.

12.6.1 UJA1167/VX (A/X) vs. UJA1168/VX/FD (A/X/F)

The UJA1167/VX (A/X) SBC is similar to the UJA1168/VX/FD (A/X/F). The main difference is that all configuration bits belonging to the features Partial Networking and the CAN FD tolerance are not supported. This applies to:

- CAN FD tolerance control bit (CFDC)
- Partial Networking Configuration OK bit (PNCOK)
- CAN Partial Networking Control bit (CPNC)
- Status bits CPNERR, CPNS, COSCS
- Partial Networking Frame Detect Error Event bit (PNFDE)
- Partial Networking Configuration Registers 0x26-0x2F and 0x68-0x6F.

In general the UJA1167/VX (A/X) software flow only differs from the UJA1168/VX/FD (A/X/F) in the configuration of Partial Networking and CAN FD. The according configuration bits are not available. For this reason also the change to the Low Power Operation becomes shorter.

Fig 92 and Fig 93 show the software flow implemented in the UJA1167/VX (A/X) example software (see Table 24) for change to Standby or rather Sleep Operation mode. The CAN PE can directly be put into Sleep mode before the UJA1167(A) enters Standby mode. No special sequence to ensure that no wake-ups are lost, like for UJA1168(A) with Partial Networking enabled, is necessary.

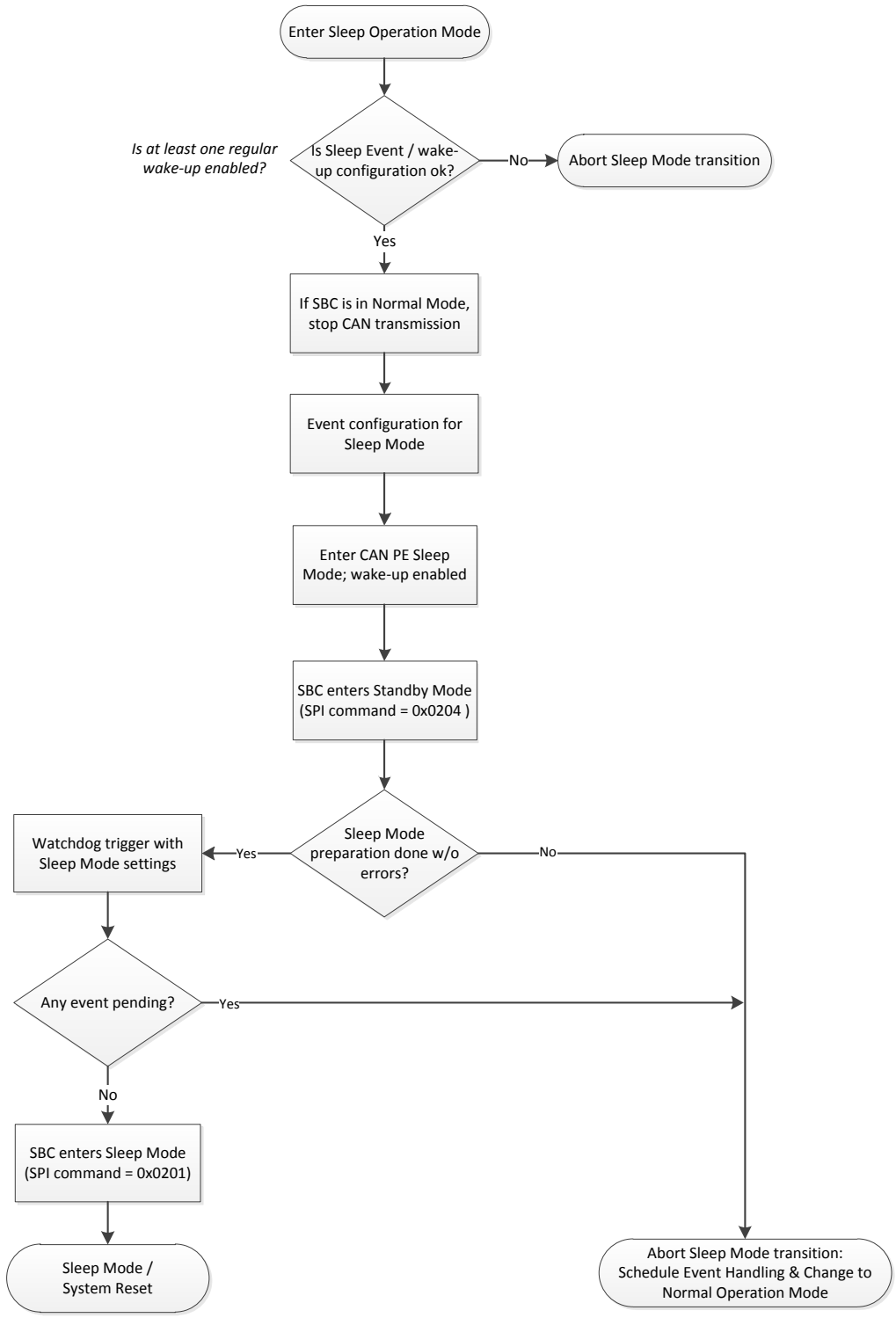


Fig 92. Transition to UJA1167(A) Sleep mode software flow

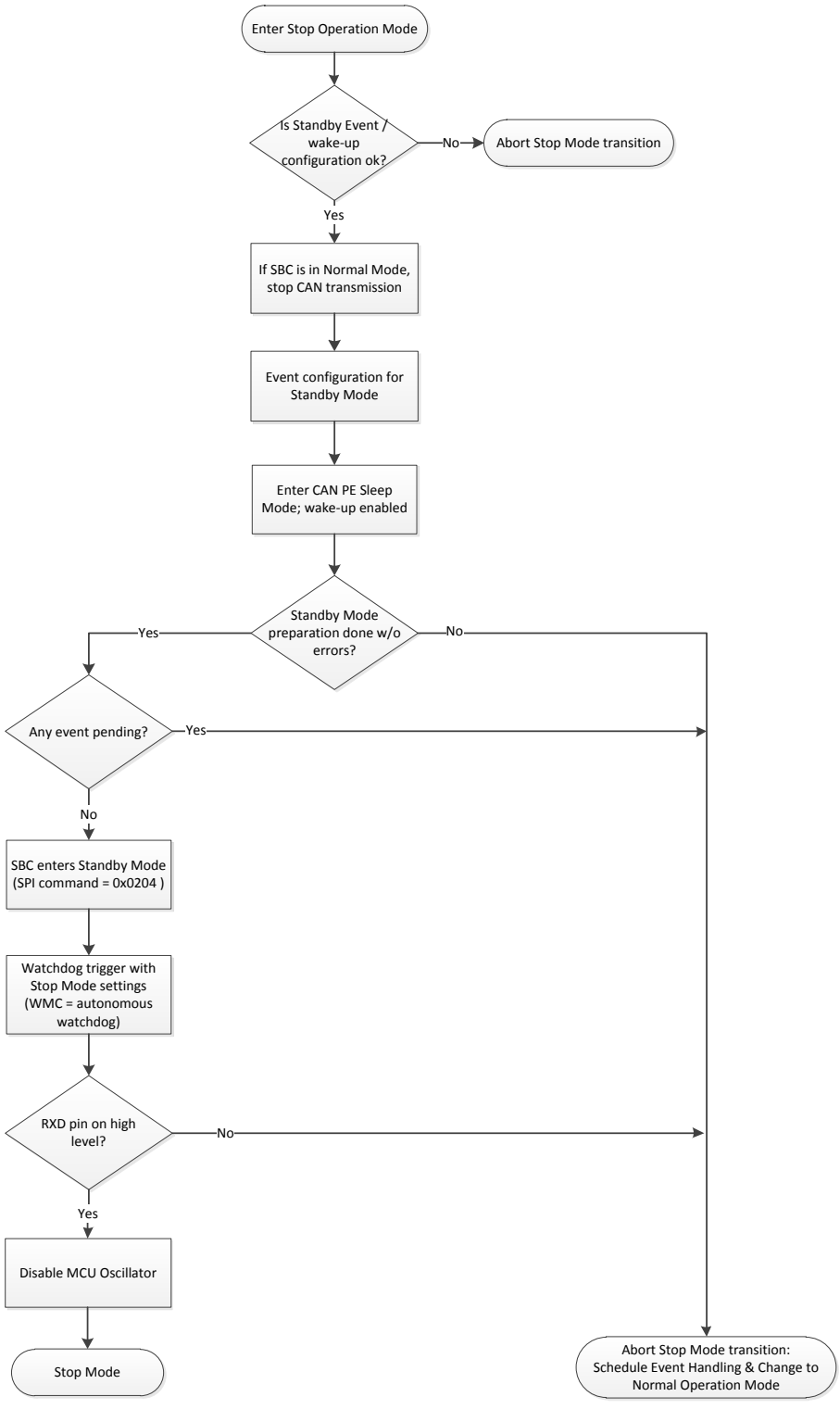


Fig 93. Transition to UJA1167(A) Stop mode software flow

12.6.2 UJA1164(A) vs. UJA1168/VX/FD (A/X/F)

The UJA1164(A) SBC is similar to the UJA1168/VX/FD (A/X/F), but contains fewer features. On the one hand all configuration bits belonging to the features Partial Networking and the CAN FD tolerance are missing. This applies to:

- CAN FD tolerance control bit (CFDC)
- Partial Networking Configuration OK bit (PNCOK)
- CAN Partial Networking Control bit (CPNC)
- Status bits CPNERR, CPNS, COSCS
- Partial Networking Frame Detect Error Event bit (PNFDE)
- Partial Networking configuration Registers 0x26-0x2F and 0x68-0x6F.

Furthermore, the SBC Sleep mode, local WAKE and VEXT pins are not available in the UJA1164(A). Thus, additionally following bits are reserved in the UJA1164(A) and cannot be initialized, configured or read:

- Wake pin control, status and event bits (WPVS, WPRE, WPFE, WPR, WPF, WPE)
- VEXT control, status and event bits (VEXTSUC, VEXTC, VEXTS, VEXTOE, VEXTUE, VEXTU, VEXTO)
- Write access to MC bits with value “1” is ignored
- Sleep mode protection bit SLPC

The change of the UJA1164(A) from Normal to Standby Operation mode is similar to that of UJA1167/VX (A/X). Please find the relevant software flow illustrated in Fig 93.

12.6.3 UJA1169/X/F vs. UJA1168/VX/FD (A/X/F)

The UJA1169 SBC is similar to the UJA1168/VX/FD (A/X/F), but contains some additional features. As the UJA1169 has the capability to drive up to 250 mA on V1 by use of an external PNP transistor, there is an additional bit to define the application output current threshold activating and deactivating the external PNP:

- Power distribution control (PDC) in the Regulator control register.

Additionally the UJA1169 provides the LIMP feature that allows indicating system failures. To use this features, the Fail safe control register is introduced and two new bits for reading the status and configuring the LIMP feature are located there:

- Reset Counter Control (RCC)
- Limp Home Control (LHC)

The Reset counter Control value is increased with each reset, while SBC is not in Forced Normal Mode. The LHC bit is set, if the RCC overflows and the LIMP output is set.

To ensure that the LIMP features works as assumed, a new sub routine during Startup Operation is necessary: Reset Counter Handling (see Fig 94).

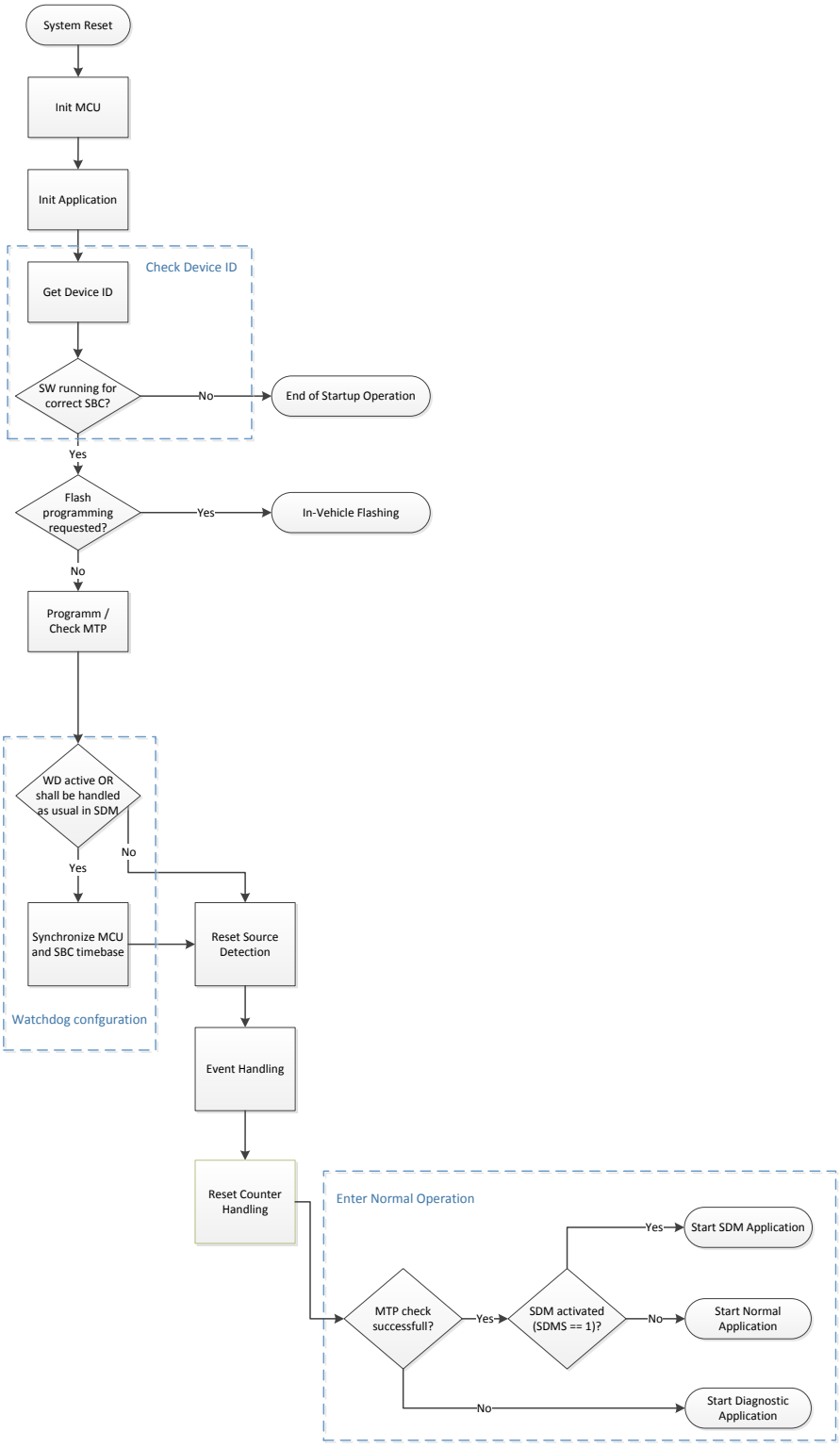


Fig 94. UJA1169 Reset Counter Handling

One of the last steps before entering Normal Operation Mode is the configuration of the Reset Counter Control (RCC), see Fig 94. The two bits can be configured with a write

access to the Fail-safe Control Register. Therefore at first the Fail-safe Control Register is read (SPI command = 0x0500), then the two least significant bits are modified as desired and afterwards the manipulated data is written back.

If RCC is set to 0, 1, 2 or 3 depends on the safety level of the application. If every system reset without software interaction should trigger the LIMP activation immediately, the application should set RCC = 3 and always write 0000 0100 xxxx xx11b to the Fail-safe Control Register accordingly. If two consecutive resets without software interaction should trigger Forced Sleep Preparation Mode, it is recommended to configure RCC = 2. With RCC cleared, the first 3 system resets without software interaction will not lead to a change in operation and give the application the chance to re-start again properly.

With every system reset event the RCC is incremented. If now a reset occurs and RCC overflows (RCC > 3) (e.g. because the software is seriously damaged) the Limp Home Control bit in the Fail-safe Control Register is set to activate the Limp Home function.

Moreover, compared to the UJA1168/VX/FD (A/X/F), the VEXT voltage regulator is changed to V2 within the UJA1169 variants without Sensor Supply VEXT and internally connected to the CAN Transceiver. Hence V2 has to be turned on actively via software control in order to activate the proper CAN supply for active communication on CAN. V2 is not required for wake-up detection.

13. Appendix

13.1 Printed Circuit board design rules

Following rules should be considered for the PCB layout:

- The SBCs are delivered in HVSON14 and HVSON20 package with an exposed die pad. In order to enhance thermal and electrical performance, it is recommended to also solder the exposed center pad to board GND.
- Additional PCB layout options improve the thermal resistance:
  - Number of PCB layers (the more the better)
  - Cu thickness (35µm/70µm; the thicker the better)
  - Heat sink area on the PCB available for the SBC (the bigger the better)
  - Number of vias (the more the better)
  - An increase of the heat sink area on the top layer is more efficient than an extension of the heat sink on the bottom layers. Hence, for a good thermal performance of the PCB it is recommended to exploit as much area on the top layer as heat sink as possible and use the other layers for further optimization.
- When a common mode choke is used, it should be placed close to the bus pins CANH and CANL (Transceiver side).
- The PCB tracks for the bus signals CANH and CANL should be routed close together in a symmetrical way. Its length should not exceed ~10cm.
- Avoid routing other “off-board” signal lines parallel to the CANH/CANL lines on the PCB due to potential “single ended” noise injection into CAN wires.
- In case further ESD protection is required it should be connected close to the ECU connector bus terminals.
- The track length between communication controller / µC and the SBC should be as short as possible.
- The ground impedance between communication controller (µC) and SBC should be as low as possible.
- Avoid applying filter elements into the GND signal of the µC or the SBC. GND has to be the same for the SBC and µC.

13.2 Pin FMEA

This chapter provides an FMEA (Failure mode and Effect Analysis) for typical failure situations, when dedicated pins of the SBCs are short-circuited to supply voltages like BAT, V1, GND or neighbored pins or simply left open. The individual failures are classified, due to their corresponding effect on the SBC, the application and the CAN bus communication. Following classes of severity are distinguished:

Table 21. Classification of severity of effects

Severity Class	Effects
A	• Damage to device • Serial communication on CAN may be affected globally
B	• No damage to device • Serial communication in the overall system not possible (global problem)
C	• No damage to device • Bus communication of other nodes in the system possible • Corrupted node not able to communicate (local problem) • Application might shut-down
D	• No damage to device • Bus communication in the overall system possible • Reduced functionality of application
-	• Not affected at all

Table 22. Pin FMEA for UJA1163(A) / UJA1164(A) / UJA1167(A) / UJA1168(A) and its variants

Pin Name	Failure	Remark	Severity Class
Pin 1: TXD	Shorted to neighbor (GND)	SBC detects this short and disables the CAN transmitter; no effects on other nodes. Consider functionality of connected MCU pin.	D
	Shorted to V1	No transmission of CAN messages possible; node runs bus off; no effect on the communication of the other nodes; reception still possible, if there are at least two other nodes in the system giving CAN acknowledge. Consider functionality of connected MCU pin.	D
	Shorted to BAT (>6V)	SBC damaged by exceeding limiting value of pin TXD.	A
	Shorted to GND	No transmission of CAN frames possible, SBC detects this short and disables the CAN transmitter; no effects on other nodes. Consider functionality of connected MCU pin.	D
	Open Circuit	No transmission of CAN frames possible; CAN controller runs bus off; no effect on other nodes communication; reception still possible, if there are at least two other nodes in the system giving CAN acknowledge.	D
Pin 2: GND	Shorted to neighbor (V1)	V1 off; permanent system reset, connected µC is unsupplied.	C
	Shorted to BAT	Fundamental problem of ECU; no supply available; SBC not affected (C), fuse in car might be triggered affecting more vehicle functions (B)	B / C
	Shorted to GND	Normal Operation	-
	Open Circuit	Fundamental problem of ECU; no supply available; SBC and components on ECU might become damaged through other GND paths on the board.	(A)
Pin 3: V1	Shorted to neighbor (RXD)	Short-term disturbance of CAN communication until CAN error counter reaches limit and CAN protocol engine stops CAN transmission; CAN Bus Off state entered upon a CAN transmission trial; other nodes not affected	C
	Shorted to V1	Normal Operation	-
	Shorted to BAT (>6V)	SBC damaged by exceeding limiting value of pin V1.	A
	Shorted to GND	V1 off; permanent system reset, connected µC is unsupplied.	C

Pin Name	Failure	Remark	Severity Class
	Open Circuit	Microcontroller unpowered, If V1 is activated, there is no buffer capacitance and with that, there is no stable operation of the regulator. Voltage overshoots cannot be excluded and damage is possible.	A / C
Pin 4: RXD	Shorted to neighbor (RSTN)	LOW level at wake-up detection or bus traffic cause permanent system reset.	C
	Shorted to V1	Short-term disturbance of CAN communication until CAN error counter reaches limit and CAN protocol engine stops CAN transmission; CAN Bus Off state is entered upon a CAN transmission trial; other nodes not affected	C
	Shorted to BAT (>6V)	SBC damaged by exceeding limiting value of pin RXD.	A
	Shorted to GND	Short-term disturbance of CAN communication until CAN error counter reaches limit and CAN protocol engine stops CAN transmission; CAN protocol engine waits for a free CAN bus; other nodes not affected	C
	Open Circuit	Short-term disturbance of CAN communication until CAN error counter reaches limit and CAN protocol engine stops CAN transmission; CAN Bus Off state entered upon a CAN transmission trial; other nodes not affected	C
Pin 5: RSTN	Shorted to neighbor (CTS) (valid for UJA1163(A))	LOW level on pin CTS cause permanent system reset.	C
	Shorted to neighbor (SDO) (valid for UJA1164(A) and 67(A) and 68(A))	LOW level on pin SDO cause permanent system reset.	C
	Shorted to V1	No system reset possible. ECU might not start correctly, WD failures cannot reset the controller and with that a severe software problem cannot be detected.	C / B
	Shorted to BAT (>6V)	SBC damaged by exceeding limiting value of pin RSTN.	A
	Shorted to GND	Permanent system reset.	C
	Open Circuit	No system reset via SBC possible. ECU might not start correctly, WD failures cannot reset the controller and with that a severe software problem cannot be detected.	C / B
Pin 6: CTS (UJA1163(A))	Shorted to V1	CAN transmit functionality continuously reported to microcontroller even if this is not the case. This might lead to an too early CAN transmission trial on pin TXD and cause local CAN error counter increase; other nodes not affected	D

Pin Name	Failure	Remark	Severity Class
	Shorted to BAT (>6V)	SBC damaged by exceeding limiting value of pin CTS.	A
	Shorted to GND	CAN transmit status cannot be reported to microcontroller. Regardless full SBC functionality available (D). Depending of software handling, the node might not start communication (C)	D / C
	Open Circuit	CAN transmit status cannot be reported to microcontroller. Regardless full SBC functionality available (D). Depending on default input level of the connected µC port and software handling, the node might not start communication or start too early CAN transmission trials. (C)	D / C
Pin 6: SDO (UJA1164(A) and 67(A) and 68(A))	Shorted to neighbor (INH) (valid for UJA1167(A) and 68(A))	In case of activated INH pin (BAT level) this pin is pulled with about 4kOhms to BAT driving a current of about 3mA into SDO. Internal ESD structures of SDO will take that current flowing towards V1. This might reverse charge V1 with about 3mA towards BAT. As long as the application is active and draining more than about 3mA from V1, the device will not be damaged and work normally (D). As soon as the application current falls below about 3mA (low power modes), SDO and with that V1 might be pulled beyond the limiting values and might damage the SBC (A) In case of deactivated INH pin SDO will work normally (with slight increased leakage), because the INH is open drain to BAT and only has ~4MOhm to GND.	D / A -
	Shorted to neighbor (VEXT) (valid for UJA1167**/VX (A/X)** and 68**/VX (A/X)**)	In case of activated VEXT pin (5V) application cannot read from SBC; behavior depends on software. In case of deactivated VEXT pin SDO will work normally.	C / D -
	Shorted to V1	Cannot read from SBC; behavior depends on software.	C / D
	Shorted to BAT (>6V)	SBC damaged by exceeding limiting value of pin SDO.	A
	Shorted to GND	Cannot read from SBC; behavior depends on software.	C / D
	Open Circuit	Cannot read from SBC; behavior depends on software.	C / D

Pin Name	Failure	Remark	Severity Class
Pin 7: i.c. (UJA1163(A) and 64(A))	Shorted to GND	Recommended i.c. pin	-
	Open Circuit	Recommended i.c. pin	-
	Shorted to >40V	SBC damaged by exceeding internal limiting value.	A
Pin 7: INH (UJA1167(A) and 68(A))	Shorted to V1	In case of activated INH pin (BAT level) V1 is pulled up reversely through about 4kOhms resulting in about 3mA of current flowing to V1. As long as the application is active and draining more than about 3mA from V1, the device will not be damaged and work normally (D). As soon as the application current falls below about 3mA (low power modes), V1 might be pulled beyond the limiting values and might damage the SBC (A).	D / A
	Shorted to BAT	INH controlled components keep permanently on.	D
	Shorted to GND	INH controlled components keep permanently off (C). In case INH is turned on a permanent current is flowing which is higher than the recommended about 1mA. This might have an impact on life time for this pin and lead to damage of the INH function over time (A).	C / A
	Open Circuit	INH controlled components keep permanently off.	C
Pin 7: VEXT (UJA1167**/VX (A/X)** and 68**/VX (A/X)**)	Shorted to V1	In case of activated VEXT pin (5V) microcontroller keeps continuously supplied in Sleep mode (D). Stability of the 5V supply cannot be guaranteed and depends on load situation (C) In case of de activated VEXT pin V1 will remain at 5V and with that continue to supply hardware connected to VEXT. Depending on the load situation, V1 might run into overcurrent situation and reset the application permanently. In case VEXT is facing an external short to BAT (which is a use case of VEXT), the limiting values of V1 are violated and the device gets damaged.	D / C D / C A
	Shorted to BAT	VEXT supplied components will get BAT supplied and might not work normally, SBC not affected.	D
	Shorted to GND	VEXT supplied components get unsupplied, SBC not affected.	D
	Open Circuit	VEXT supplied components get unsupplied, If VEXT is activated, there is no buffer capacitance and with that, there is no stable operation of the regulator. Voltage overshoots cannot be excluded.	D

Pin Name	Failure	Remark	Severity Class
Pin 8: i.c. (UJA1163(A))	Shorted to GND	Recommended i.c. pin	-
	Shorted to >6V	SBC damaged by exceeding internal limiting value.	A
	Shorted to neighbor (Pin 9 i.c.)	Pin 9 Is the disabled WAKE pin function with floating behavior, no impact to SBC	-
	Open Circuit	Recommended i.c. pin	-
Pin 8: SCK (UJA1164(A) and 67(A) and 68(A))	Shorted to neighbor (WAKE) (valid for UJA1167(A) and 68)	In case of WAKE pin input voltage related to BAT supply SBC damaged by exceeding limiting value of pin SCK.	A
		In case of WAKE pin input voltage related to SCK limiting value range, no communication towards SBC. Consider functionality of connected MCU pin.	C
	Shorted to V1	No communication towards SBC. Consider functionality of connected MCU pin.	C
	Shorted to BAT (>6V)	SBC damaged by exceeding limiting value of pin SCK.	A
	Shorted to GND	No communication towards SBC. Consider functionality of connected MCU pin.	C
	Open Circuit	No communication towards SBC.	C
Pin 9: i.c. (UJA1163(A) and 64(A))	Shorted to GND	Recommended i.c. pin	-
	Shorted to neighbor (BAT)	Pin 9 is the disabled WAKE pin function with floating behavior and battery robustness, no impact to SBC	-
	Open Circuit	Recommended i.c. pin	-
	Shorted to >40V	SBC damaged by exceeding internal limiting value.	A
Pin 9: WAKE (UJA1167(A) and 68(A))	Shorted to neighbor (BAT)	No local wake-up possible	D
	Shorted to V1	In case of WAKE pin input voltage related to BAT supply SBC damaged by exceeding limiting value of pin V1.	A
		In case of WAKE pin input voltage related to V1 limiting value range, a LOW input level on pin WAKE cause a permanent system reset.	C

Pin Name	Failure	Remark	Severity Class
	Shorted to GND	No local wake-up possible	D
	Open Circuit	No local wake-up possible	D
Pin 10: BAT	Shorted to neighbor (SDI)	In case of BAT>6V SBC damaged by exceeding limiting value of pin SDI.	A
	Shorted to V1	In case of BAT>6V SBC damaged by exceeding limiting value of pin V1.	A
	Shorted to BAT	Normal operation	-
	Shorted to GND	Fundamental problem of ECU; no supply available; SBC not affected (C), fuse in car might be triggered affecting more vehicle functions (B)	C / B
	Open Circuit	SBC not supplied, no further impact	C
Pin 11: i.c. (UJA1163(A))	Shorted to GND	Recommended i.c. pin	-
	Shorted to neighbor (CANL)	In case of CANL peak >6V SBC damaged by exceeding limiting value of disabled internal SDI.	A
	Open Circuit	Recommended i.c. pin	-
	Shorted to >6V	SBC damaged by exceeding internal limiting value.	A
Pin 11: SDI (UJA1164(A) and 67(A) and 68(A))	Shorted to neighbor (CANL)	No communication towards SBC. Consider functionality of connected MCU pin. In case of CANL peak >6V SBC damaged by exceeding limiting value of pin SDI. Serial communication on CAN may be affected globally.	C A B
	Shorted to V1	No communication towards SBC. Consider functionality of connected MCU pin.	C
	Shorted to BAT	In case of BAT>6V SBC damaged by exceeding limiting value of pin SDI.	A
	Shorted to GND	No communication towards SBC. Consider functionality of connected MCU pin.	C
	Open Circuit	No communication towards SBC.	C

Pin Name	Failure	Remark	Severity Class
Pin 12: CANL	Shorted to neighbor (CANH)	No communication possible (no differential signal)	B
	Shorted to V1	No communication possible (no differential signal)	B
	Shorted to BAT	No communication possible (no differential signal)	B
	Shorted to GND	Communication still possible (differential signal still available; CANH recessive level lowered to GND level)	D
	Open Circuit	No communication possible (no differential signal). Depending on bus termination and system size the still connected CANH wire might corrupt the overall CAN communication in the car with random transmission trials.	B
Pin 13: CANH	Shorted to neighbor (STBN) (valid for UJA1163(A))	SBC is not able to enter Standby mode when the bus is driven dominant In case of CANH peaks >6V SBC damaged by exceeding limiting value of pin STBN. Serial communication on CAN may be affected globally.	A
	Shorted to neighbor (SCSN) (valid for UJA1164(A) and 67(A) and 68(A))	No communication towards SBC. Consider functionality of connected MCU pin. In case of CANH peak >6V SBC damaged by exceeding limiting value of pin SCSN. Serial communication on CAN may be affected globally.	A
	Shorted to V1	Communication still possible (differential signal still available; CANH recessive level increased to V1 level)	D
	Shorted to BAT	Communication still possible (differential signal still available; CANH recessive level increased to BAT level)	D
	Shorted to GND	No communication possible (no differential signal)	B
	Open Circuit	No communication possible (no differential signal)	B
Pin 14: STBN (UJA1163(A))	Shorted to V1	SBC is not able to enter Standby mode when V1 ramped up	D
	Shorted to BAT (>6V)	SBC damaged by exceeding limiting value of pin STBN.	A
	Shorted to GND	SBC is not able to enter Normal mode.	C
	Open Circuit	SBC is not able to enter Normal mode.	C

Pin Name	Failure	Remark	Severity Class
Pin 14: SCSN (UJA1164(A) and 67(A) and 68(A))	Shorted to V1	No communication towards SBC. Consider functionality of connected MCU pin.	C
	Shorted to BAT (>6V)	SBC damaged by exceeding limiting value of pin SCSN.	A
	Shorted to GND	No communication towards SBC. Consider functionality of connected MCU pin.	C
	Open Circuit	No communication towards SBC.	C

Table 23. Pin FMEA for UJA1169 and its variants

Pin Name	Failure	Remark	Severity Class
Pin 1: GND	Shorted to neighbor (TXD)	SBC detects this short and disables the CAN transmitter; no effects on other nodes. Consider functionality of connected MCU pin.	D
	Shorted to V1	V1 off; permanent system reset, connected µC is unsupplied.	C
	Shorted to BAT	Fundamental problem of ECU; no supply available; SBC not affected (C), fuse in car might be triggered affecting more vehicle functions (B)	C / B
	Shorted to GND	Normal Operation	-
	Open Circuit	There are redundant GND pins, no functional impact	-
Pin 2: TXD	Shorted to neighbor (SDI)	No communication towards SBC. Consider functionality of connected MCU pin.	C
	Shorted to V1	No transmission of CAN messages possible; node runs bus off; no effect on the communication of the other nodes; reception still possible, if there are at least two other nodes in the system giving CAN acknowledge. Consider functionality of connected MCU pin.	D
	Shorted to BAT (>6V)	SBC damaged by exceeding limiting value of pin TXD.	A
	Shorted to GND	No transmission of CAN frames possible, SBC detects this short and disables the CAN transmitter; no effects on other nodes. Consider functionality of connected MCU pin.	D
	Open Circuit	No transmission of CAN frames possible; CAN controller runs bus off; no effect on other nodes communication; reception still possible, if there are at least two other nodes in the system giving CAN acknowledge.	D
Pin 3: SDI	Shorted to neighbor (GND)	No communication towards SBC. Consider functionality of connected MCU pin.	C
	Shorted to BAT	SBC damaged by exceeding limiting value of pin SDI.	A
	Shorted to GND	No communication towards SBC. Consider functionality of connected MCU pin.	C
	Open Circuit	No communication towards SBC.	C

Pin Name	Failure	Remark	Severity Class
Pin 4: GND	Shorted to neighbor (V1)	V1 off; permanent system reset, connected µC is unsupplied.	C
	Shorted to BAT	Fundamental problem of ECU; no supply available; SBC not affected (C), fuse in car might be triggered affecting more vehicle functions (B)	B / C
	Shorted to GND	Normal Operation	-
	Open Circuit	There are redundant GND pins, no functional impact	-
Pin 5: V1	Shorted to neighbor (VEXCC)	Normal application use case if no external PNP is used	-
		With external PNP the external resistor measuring the PNP current is bypassed and as such, there is no current limitation available for the PNP. SBC not affected (D) but PNP might overheat at overload of V1 (C)	C / D
	Shorted to neighbor (VIO) (UJA1169L versions)	No impact if VIO is connected to a 5V system	-
		Potential damage to other components on a connected 3V3 system (C), V1 of UJA1169L may be overloaded, but not damaged (A)	A / C
	Shorted to V1	Normal Operation	-
	Shorted to BAT (>6V)	SBC damaged by exceeding limiting value of pin V1.	A
	Shorted to GND	V1 off; permanent system reset, connected µC is unsupplied.	C
	Open Circuit	Microcontroller unpowered, If V1 is activated, there is no buffer capacitance and with that, there is no stable operation of the regulator. Voltage overshoots cannot be excluded and damage is possible.	A / C
Pin 6: VEXCC	Shorted to neighbor (RXD)	Short-term disturbance of CAN communication until CAN error counter reaches limit and CAN protocol engine stops CAN transmission; CAN Bus Off state is entered upon a CAN transmission trial; other nodes not affected	C
	Shorted to V1	Normal application use case if no external PNP is used	-
		With external PNP the external resistor measuring the PNP current is bypassed and as such, there is no current limitation available for the PNP. SBC not affected (D) but PNP might overheat at overload of V1 (C)	C / D

Pin Name	Failure	Remark	Severity Class
Pin 6: VIO (1169L)	Shorted to BAT (>6V)	SBC damaged by exceeding limiting value	A
	Shorted to GND	V1 off; permanent system reset, connected µC is unsupplied.	C
	Open Circuit	Application without external PNP no impact	-
		Application with external PNP would have no current limitation available for the PNP. SBC not affected (D) but PNP might overheat at overload of V1 (C)	C / D
	Shorted to neighbor (VEXCC)	If VIO is connected to a 5V system and no external PNP used, there is no impact.	-
		If VIO is connected to a 5V system and an external PNP is used, there might be no current limitation available for the PNP. SBC not affected (D) but PNP might overheat at overload of V1 (C)	C / D
		If VIO is connected to a 3V3 system and no external PNP used, there is no impact.	-
		If VIO is connected to a 3V3 system and an external PNP is used there is potential damage to the 3V3 system because of 5V overvoltage (A). UJA1169L not affected (C)	A / C
	Shorted to BAT (>6V)	SBC damaged by exceeding limiting value of pin VIO.	A
	Shorted to GND	Normal Operation without supply on this pin, reduced functionality	D
	Open Circuit	Normal Operation without supply on this pin, reduced functionality	D
Pin 7: RXD	Shorted to neighbor (RSTN)	LOW level at wake-up detection or bus traffic cause permanent system reset.	C
	Shorted to V1	Short-term disturbance of CAN communication until CAN error counter reaches limit and CAN protocol engine stops CAN transmission; CAN Bus Off state is entered upon a CAN transmission trial; other nodes not affected	C
	Shorted to BAT (>6V)	SBC damaged by exceeding limiting value of pin RXD.	A
	Shorted to GND	Short-term disturbance of CAN communication until CAN error counter reaches limit and CAN protocol engine stops CAN transmission; CAN protocol engine waits for a free CAN bus; other nodes not affected	C

Pin Name	Failure	Remark	Severity Class
	Open Circuit	Short-term disturbance of CAN communication until CAN error counter reaches limit and CAN protocol engine stops CAN transmission; CAN Bus Off state entered upon a CAN transmission trial; other nodes not affected	C
Pin 7: VEXCC (1169L)	Shorted to neighbor (RXD)	If VIO is connected to 5V system, short-term disturbance of CAN communication until CAN error counter reaches limit and CAN protocol engine stops CAN transmission; CAN Bus Off state is entered upon a CAN transmission trial; other nodes not affected	C
		If VIO is connected to a 3V3 system and no external PNP used, there is no impact. (Note: RXD is related to VIO voltage)	-
		If VIO is connected to a 3V3 system and an external PNP is used there is potential damage to the 3V3 system because of 5V overvoltage (A) . (Note: RXD is related to VIO voltage). UJA1169L not affected (C)	A / C
	Shorted to V1	Normal application use case if no external PNP is used	-
		With external PNP the external resistor measuring the PNP current is bypassed and as such, there is no current limitation available for the PNP. SBC not affected (D) but PNP might overheat at overload of V1 (C)	C / D
	Shorted to BAT (>6V)	SBC damaged by exceeding limiting value	A
	Shorted to GND	V1 off; SBC out of use, but not damaged	D
	Open Circuit	Normal Operation without supply on this pin, reduced functionality	D
Pin 8: RSTN	Shorted to neighbor (SDO)	LOW level on pin SDO cause permanent system reset.	C
	Shorted to V1	No system reset possible. ECU might not start correctly, WD failures cannot reset the controller and with that a severe software problem cannot be detected.	C / B
	Shorted to BAT (>6V)	SBC damaged by exceeding limiting value of pin RSTN.	A
	Shorted to GND	Permanent system reset.	C
	Open Circuit	No system reset via SBC possible. ECU might not start correctly, WD failures cannot reset the controller and with that a severe software problem cannot be detected.	C / B

Pin Name	Failure	Remark	Severity Class
Pin 8: RXD (UJA1169L)	Shorted to neighbor (SDO)	Temporary disturbance of CAN communication until CAN error counter reaches limit and CAN protocol engine stops CAN transmission; CAN Bus Off state is entered upon a CAN transmission trial; other nodes not affected; SPI communication gives wrong feedback	C
	Shorted to V1	If VIO is connected to a 5V system, short-term disturbance of CAN communication until CAN error counter reaches limit and CAN protocol engine stops CAN transmission; CAN Bus Off state is entered upon a CAN transmission trial; other nodes not affected. (Hint: RXD is related to VIO) If VIO is connected to a 3V3 system, there is potential damage to the 3V3 system because of 5V overvoltage. UJA1169L may be damaged as well due to violation of MAX ratings (VIO + 0.3V)	C A
	Shorted to BAT (>6V)	SBC damaged by exceeding limiting value of pin RXD.	A
	Shorted to GND	Short-term disturbance of CAN communication until CAN error counter reaches limit and CAN protocol engine stops CAN transmission; CAN protocol engine waits for a free CAN bus; other nodes not affected	C
	Open Circuit	Short-term disturbance of CAN communication until CAN error counter reaches limit and CAN protocol engine stops CAN transmission; CAN Bus Off state entered upon a CAN transmission trial; other nodes not affected	C
Pin 9: SDO	Shorted to neighbor (SCK)	Cannot read from SBC; behavior depends on software.	C / D
	Shorted to V1	Cannot read from SBC; behavior depends on software.	C / D
	Shorted to BAT (>6V)	SBC damaged by exceeding limiting value of pin SDO.	A
	Shorted to GND	Cannot read from SBC; behavior depends on software.	C / D
	Open Circuit	Cannot read from SBC; behavior depends on software.	C / D
Pin 10: SCK	Shorted to V1	Cannot read from SBC; behavior depends on software.	C / D
	Shorted to BAT (>6V)	SBC damaged by exceeding limiting value of pin SCK.	A
	Shorted to GND	Cannot read from SBC; behavior depends on software.	C / D
	Open Circuit	Cannot read from SBC; behavior depends on software.	C / D

Pin Name	Failure	Remark	Severity Class
Pin 11: LIMP	Shorted to neighbor (WAKE)	No damage, behavior depends on application circuitry connected to WAKE: In case WAKE is not used (disabled), no impact.	-
		In case WAKE is connected to LOW-active input signal, LIMP function will get active unintentionally with any LOW input signal.	C
		In case WAKE is connected to HIGH active signal, LIMP function may be active all time until the WAKE input gets HIGH	C
	Shorted to V1	Might prevent activation of application specific LIMP Home function (is active LOW).	D
		Depending on connected application hardware, LIMP function gets permanently activated or activated with entering Sleep Mode (V1 off)	C
	Shorted to GND	LIMP function permanently active	C
	Open Circuit	No LIMP Home application function available	D
	Shorted to BAT	SBC not damaged, no LIMP Home application function available, other connected hardware to be assessed	D
Pin 12: WAKE	Shorted to neighbor (V2) (valid for UJA1169 and 1169FD)	In case of WAKE pin input voltage related to BAT supply SBC damaged by exceeding limiting value of pin V2.	A
		In case of WAKE pin input voltage related to V2 limiting value range, a LOW input level on pin WAKE cause an overload of V2 and with that a disable of CAN communication. Local wake-up capability will be lost.	C
	Shorted to neighbor (VEXT) (valid for UJA1169**VX** and 1169**VX**FD)	Wake-pin related wake-up capability might be lost, depending on WAKE input signal the VEXT supply might get overloaded.	C
	Shorted to V1	In case of WAKE pin input voltage related to BAT supply SBC damaged by exceeding limiting value of pin V1.	A
		In case of WAKE pin input voltage related to V1 limiting value range, a LOW input level on pin WAKE cause a permanent system reset.	C
	Shorted to BAT	No local wake-up possible	D
	Shorted to GND	No local wake-up possible	D
	Open Circuit	No local wake-up possible	D

Pin Name	Failure	Remark	Severity Class
Pin 13: V2 (UJA1169 UJA1169/F UJA1169/3 UJA1169/F/3)	Shorted to neighbor (BAT)	In case of BAT>6V SBC damaged by exceeding limiting value of pin V2.	A
	Shorted to V1	In case of activated V2, microcontroller keeps continuously supplied in Sleep mode (D). Stability of the 5V supply cannot be guaranteed and depends on load situation (C)	D / C
		In case of de activated V2 pin V1 will remain at 5V and with that continue to supply hardware connected to V2. This might lead to increased quiescent current.	D
	Shorted to BAT (>6V)	SBC damaged by exceeding limiting value of pin V2.	A
	Shorted to GND	V2 supply in overload, CAN communication not possible anymore.	C / D
	Open Circuit	CAN communication not possible, If V2 is activated, there is no buffer capacitance and with that, there is no stable operation of the regulator. Voltage overshoots cannot be excluded and damage is possible.	A / C
Pin 13: VEXT (UJA1169/X UJA1169/X/F)	Shorted to neighbor (BAT)	VEXT supplied components will get BAT supplied and might not work normally, SBC not affected.	D
	Shorted to V1	In case of activated VEXT pin (5V) microcontroller keeps continuously supplied in Sleep mode (D). Stability of the 5V supply cannot be guaranteed and depends on load situation (C)	D / C
		In case of de activated VEXT pin V1 will remain at 5V and with that continue to supply hardware connected to VEXT. Depending on the load situation, V1 might run into overcurrent situation and reset the application permanently.	D / C
		In case VEXT is facing an external short to BAT (which is a use case of VEXT), the limiting values of V1 are violated and the device gets damaged.	A
	Shorted to BAT	VEXT supplied components will get BAT supplied and might not work normally, SBC not affected.	D
	Shorted to GND	VEXT supplied components get unsupplied, SBC not affected.	D
	Open Circuit	If VEXT is activated, there is no buffer capacitance and with that, there is no stable operation of the regulator. Voltage overshoots cannot be excluded.	D

Pin Name	Failure	Remark	Severity Class
Pin 14: BAT	Shorted to neighbor (VEXCTRL)	Without external PNP there is no impact on functionality	-
		With external PNP, the PNP cannot be turned on and the full application current is running inside of the SBC, this might lead to an over temperature shut down depending on load and environmental temperature condition	C / D
	Shorted to V1	In case of BAT>6V SBC damaged by exceeding limiting value of pin V1.	A
	Shorted to BAT	Normal operation	-
	Shorted to GND	Fundamental problem of ECU; no supply available; SBC not affected (C), fuse in car might be triggered affecting more vehicle functions (B)	C / B
	Open Circuit	SBC not supplied, no further impact	C
Pin 15: VEXCTRL	Shorted to neighbor (GND)	Without external PNP no impact	-
		With external PNP, the PNP might be damaged due to high basis current; V1 level temporarily raised above specification (up to BAT), increased current consumption; battery voltage drop; SBC not supplied	A
	Shorted to V1	Without external PNP there is small current flowing from BAT to V1. No further impact.	-
		With external PNP, the PNP might be damaged due to high basis current; V1 level temporarily raised above specification (up to BAT), increased current consumption; battery voltage drop; SBC not supplied	A
	Shorted to BAT	Without external PNP there is no impact on functionality	-
		With external PNP, the PNP cannot be turned on and the full application current is running inside of the SBC, this might lead to an over temperature shut down depending on load and environmental temperature condition	C / D
	Shorted to GND	Without external PNP no impact	-
		With external PNP, the PNP might be damaged due to high basis current; V1 level temporarily raised above specification (up to BAT), increased current consumption; battery voltage drop; SBC not supplied	A

Pin Name	Failure	Remark	Severity Class
	Open Circuit	Without external PNP there is no impact on functionality With external PNP, the PNP cannot be turned on and the full application current is running inside of the SBC, this might lead to an over temperature shut down depending on load and environmental temperature condition	- C / D
Pin 16: GND	Shorted to neighbor (CANL)	Communication still possible (differential signal still available; CANH recessive level lowered to GND level)	D
	Shorted to V1	V1 off; permanent system reset, connected µC is unsupplied.	C
	Shorted to BAT	Fundamental problem of ECU; no supply available; SBC not affected (C), fuse in car might be triggered affecting more vehicle functions (B)	B / C
	Shorted to GND	Normal Operation	-
	Open Circuit	There are redundant GND pins, no functional impact	-
Pin 17: CANL	Shorted to neighbor (CANH)	No communication possible (no differential signal)	B
	Shorted to V1	No communication possible (no differential signal)	B
	Shorted to BAT	No communication possible (no differential signal)	B
	Shorted to GND	Communication still possible (differential signal still available; CANH recessive level lowered to GND level)	D
	Open Circuit	No communication possible (no differential signal). Depending on bus termination and system size the still connected CANH wire might corrupt the overall CAN communication in the car with random transmission trials.	B
Pin 18: CANH	Shorted to neighbor (GND)	No communication possible (no differential signal)	B
	Shorted to V1	Communication still possible (differential signal still available; CANH recessive level increased to V1 level)	D
	Shorted to BAT	Communication still possible (differential signal still available; CANH recessive level increased to BAT level)	D
	Shorted to GND	No communication possible (no differential signal)	B
	Open Circuit	No communication possible (no differential signal)	B

Pin Name	Failure	Remark	Severity Class
Pin 19: GND	Shorted to neighbor (SCSN)	No communication towards SBC. Consider functionality of connected MCU pin.	C
	Shorted to V1	V1 off; permanent system reset, connected µC is unsupplied.	C
	Shorted to BAT	Fundamental problem of ECU; no supply available; SBC not affected (C), fuse in car might be triggered affecting more vehicle functions (B)	B / C
	Shorted to GND	Normal Operation	-
	Open Circuit	There are redundant GND pins, no functional impact	-
Pin 20: SCSN	Shorted to V1	No communication towards SBC. Consider functionality of connected MCU pin.	C
	Shorted to BAT (>6V)	SBC damaged by exceeding limiting value of pin SCSN.	A
	Shorted to GND	No communication towards SBC. Consider functionality of connected MCU pin.	C
	Open Circuit	No communication towards SBC.	C

13.3 Associated files

Within the package of these application hints you can find source code for an UJA1168/VX/FD (A/X/F) SBC, UJA1167/VX (A/X) SBC, UJA1164(A) SBC and UJA1169/FD example project and its software documentation as well as a power dissipation estimator. Table 24 lists the attached files and Table 25 to Table 27 give an overview and a detailed description of the content of the attached files.

Table 24. Attached files and folders in archive

Attached File	Description
Example_SW_UJA1168FDVX	Example Project for UJA1168/VX/FD (A/X/F) incl. software and documentation
Example_SW_UJA1167VX	Example Project for UJA1167/VX (A/X) incl. software and documentation
Example_SW_UJA1164	Example Project for UJA1164(A) incl. software and documentation
Example_SW_UJA1169FD	Example Project for UJA1169FD incl. software and documentation
UJA116x_Power_Dissipation_Calculator_v1_1.xlsx	EXCEL Spread Sheet for power dissipation estimations

Table 25. Content of Archive Example_SW_UJA1168FDVX

Attached File	Description
UJA1168FDVX_ApplHint.c	C-file containing the main function
NXP_UJA1168FDVX_Functions.c	Header file for UJA1168/VX/FD (A/X/F) SBC low level driver
NXP_UJA1168FDVX_Functions.h	C-file implementing UJA1168/VX/FD (A/X/F) SBC low level driver
NXP_UJA1168FDVX_Sim.h	Header file containing typedefs for the UJA1168/VX/FD (A/X/F) SBC registers
NXP_UJA11XX_defines.h	Header file defining data types and general typedefs
UJA1168FDVX_Application_Specific_Functions.h	Header file defining application specific functions
UJA1168FDVX_Application_Specific_Functions.c	C-file implementing application specific functions
uC_Specific_Functions.h	Header file defining microcontroller specific functions
uC_Specific_Function.c	C-file containing microcontroller specific functions that must be implemented by the SW designer
UJA1168FDVX_Configuration.h	Header file containing the application configuration of the UJA1168/VX/FD (A/X/F) SBC in different operating modes
UJA1168FDVX_Appl_Hints_Software_Documentation.zip	Documentation of the example project; Please remove the suffix ".txt" and extract the ZIP-archive afterwards.

Table 26. Content of Archive Example_SW_UJA1167(A)VX

Attached File	Description
UJA1167VX_ApplHint.c	C-file containing the main function
NXP_UJA1167VX_Functions.c	Header file for UJA1167/VX (A/X) SBC low level driver
NXP_UJA1167VX_Functions.h	C-file implementing UJA1167/VX (A/X) SBC low level driver
NXP_UJA1167VX_Sim.h	Header file containing typedefs for the UJA1167/VX (A/X) SBC registers
NXP_UJA11XX_defines.h	Header file defining data types and general typedefs
UJA1167VX_Application_Specific_ Functions.h	Header file defining application specific functions
UJA1167VX_Application_Specific_ Functions.c	C-file implementing application specific functions
uC_Specific_Functions.h	Header file defining microcontroller specific functions
uC_Specific_Function.c	C-file containing microcontroller specific functions that must be implemented by the SW designer
UJA1167VX_Configuration.h	Header file containing the application configuration of the UJA1167/VX (A/X) SBC in different operating modes
UJA1167VX_Appl_Hints_Software_ Documentation.zip	Documentation of the example project; Please remove the suffix ".txt" and extract the ZIP-archive afterwards.

Table 27. Content of Archive Example_SW_UJA1164(A)

Attached File	Description
UJA1164_ApplHint.c	C-file containing the main function
NXP_UJA1164(A)_Functions.c	Header file for UJA1164(A) SBC low level driver
NXP_UJA1164_Functions.h	C-file implementing UJA1164(A) SBC low level driver
NXP_UJA114_Sim.h	Header file containing typedefs for the UJA1164(A) registers
NXP_UJA11XX_defines.h	Header file defining data types and general typedefs
UJA1164_Application_Specific_Functions.h	Header file defining application specific functions
UJA1164_Application_Specific_Functions.c	C-file implementing application specific functions
uC_Specific_Functions.h	Header file defining microcontroller specific functions
uC_Specific_Function.c	C-file containing microcontroller specific functions that must be implemented by the SW designer
UJA1164_Configuration.h	Header file containing the application configuration of the UJA1164(A) SBC in different operating modes

Attached File	Description
UJA1164_Appl_Hints_Software_ Documentation.zip	Documentation of the example project; Please remove the suffix ".txt" and extract the ZIP-archive afterwards.

Table 28. Content of Archive Example_SW_UJA1169FD

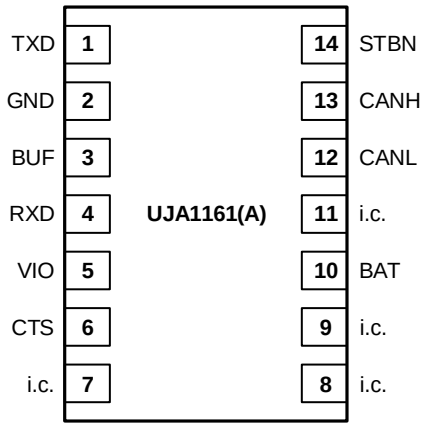
Attached File	Description
UJA1169FD_ApplHint.c	C-file containing the main function
NXP_UJA1169FD_Functions.c	Header file for UJA1169FD SBC low level driver
NXP_UJA1169FD_Functions.h	C-file implementing UJA1169FD SBC low level driver
NXP_UJA1169FD_Sim.h	Header file containing typedefs for the UJA1169FD registers
NXP_UJA11XX_defines.h	Header file defining data types and general typedefs
UJA1169FD_Application_Specific_Functions.h	Header file defining application specific functions
UJA1169FD_Application_Specific_Functions.c	C-file implementing application specific functions
uC_Specific_Functions.h	Header file defining microcontroller specific functions
uC_Specific_Function.c	C-file containing microcontroller specific functions that must be implemented by the SW designer
UJA1169FD_Configuration.h	Header file containing the application configuration of the UJA1169FD SBC in different operating modes
UJA1169FD_Appl_Hints_Software_ Documentation.zip	Documentation of the example project; Please remove the suffix ".txt" and extract the ZIP-archive afterwards.

13.4 NXPs self-supplied high speed CAN transceiver

Two further devices are part of the UJA116x SBC family, which are just providing the CAN Transceiver function plus the 5V supply for the CAN Transceiver. These devices can ideally be used for applications, which require another CAN channel without having another 5V supply available.

13.4.1 UJA1161(A) – Self supplied high CAN transceiver with Standby mode

UJA1161 – Self supplied high speed CAN transceiver with Standby mode

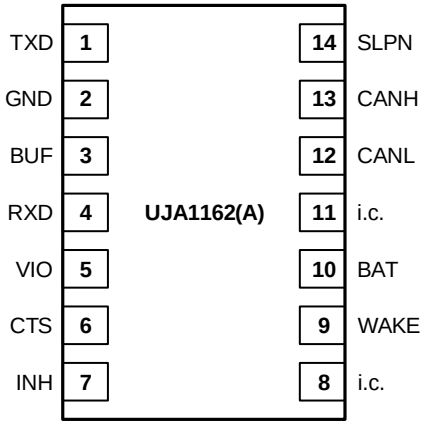


- Self-supplied high-speed CAN transceiver
- ISO 11898-5:2007 compliant
- Autonomous bus biasing according to ISO 11898-6:2013
- Fully integrated 5 V supply (BUF) for CAN transmitter/receiver
- VIO allows for direct interfacing with 3.3 V to 5 V microcontrollers
- Standby mode featuring low supply current
- Remote wake-up capability

Fig 95. Pin configuration and short functional description of the UJA1161(A)

13.4.2 UJA1162(A) – Self supplied high CAN transceiver with Sleep mode

UJA1162 – Self supplied high speed CAN transceiver with Sleep mode



- Self-supplied high-speed CAN transceiver
- ISO 11898-5:2007 compliant
- Autonomous bus biasing according to ISO 11898-6:2013
- Fully integrated 5 V supply (BUF) for CAN transmitter/receiver
- VIO allows for direct interfacing with 3.3 V to 5 V microcontrollers
- Sleep mode featuring low supply current (BUF off)
- Remote wake-up capability
- Local wake-up capability via the WAKE pin
- Entire node can be powered down via the inhibit output, INH

Fig 96. Pin configuration and short functional description of the UJA1162(A)

13.5 PCB Soldering Footprints (HVSON Packages)

13.5.1 UJA1163(A), UJA1164(A), UJA1167(A), UJA1168(A) derivatives (HVSON14)

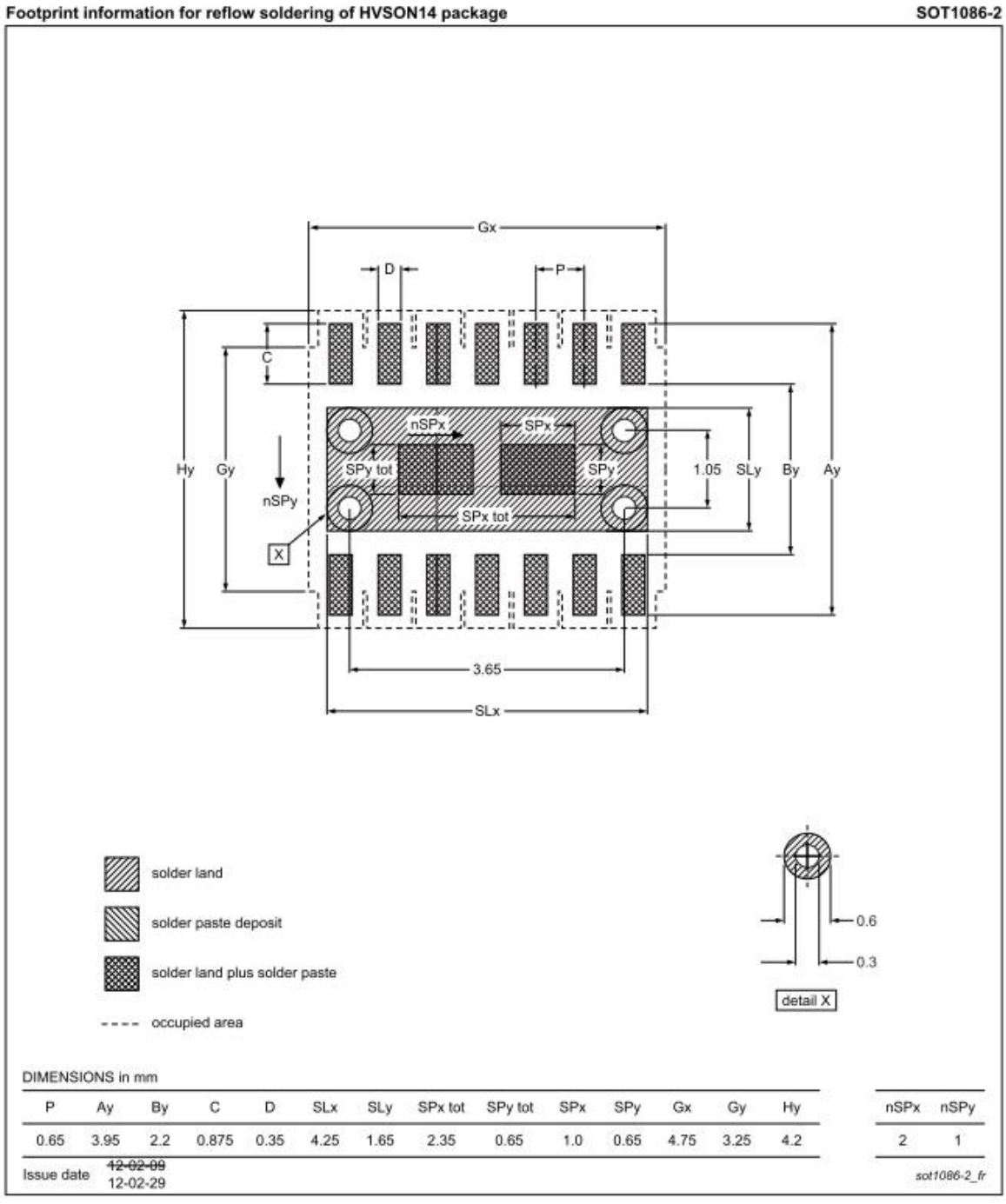


Fig 97. UJA1163(A), UAJ1164, UJA1167(A) and UJA1168(A) Soldering Layout (HVSON14)

13.5.2 UJA1169 derivatives (HVSON20)

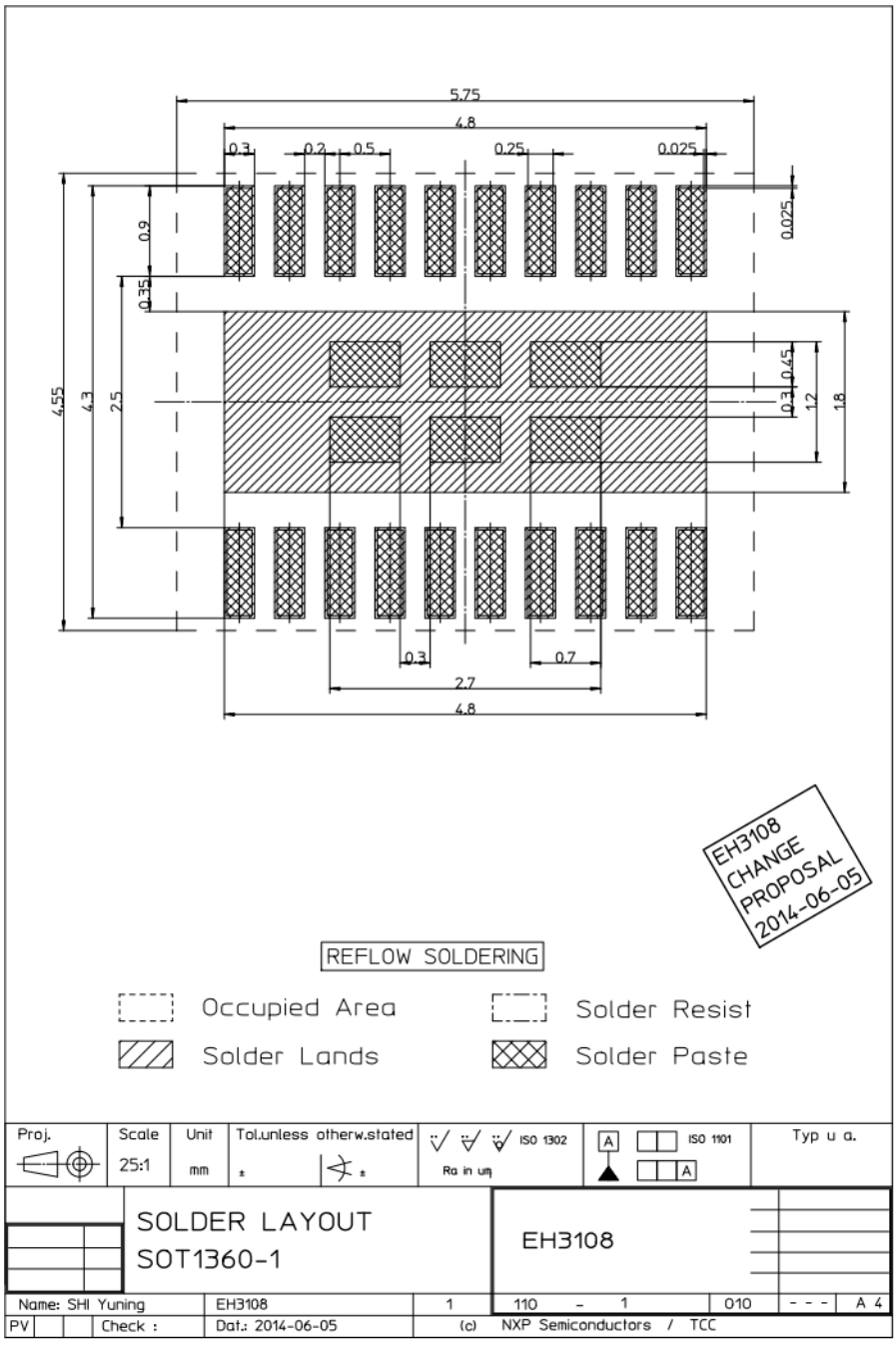


Fig 98. UJA1169 Soldering Layout (HVSON20)

13.6 Abbreviations

Table 29. Abbreviations

Acronym	Description
CAN	Controller Area Network
ECU	Electronic Control Unit
EMC	Electromagnetic Compatibility
EME	Electromagnetic Emission
EMI	Electromagnetic Immunity
ESD	Electrostatic Discharge
FMEA	Failure mode and Effects Analysis
MTP	Multi Time Programmable
NVM	Non Volatile Memory
OEM	Original Equipment Manufacturer
PE	Protocol Engine
PCB	Printed Circuit Board
SBC	System Basis Chip
SPI	Serial Peripheral Interface

14. References

[1] Product datasheet UJA1161, Self-supplied high-speed CAN transceiver with Standby mode – NXP Semiconductors
Product datasheet UJA1161A, Self-supplied high-speed CAN transceiver with Standby mode – NXP Semiconductors

[2] Product datasheet UJA1162, Self-supplied high-speed CAN transceiver with Sleep mode – NXP Semiconductors
Product datasheet UJA1162A, Self-supplied high-speed CAN transceiver with Sleep mode – NXP Semiconductors

[3] Product datasheet UJA1163, Mini high-speed CAN system basis chip with Standby mode – NXP Semiconductors
Product datasheet UJA1163A, Mini high-speed CAN system basis chip with Standby mode – NXP Semiconductors

[4] Product datasheet UJA1164, Mini high-speed CAN system basis chip with Standby mode & Watchdog – NXP Semiconductors
Product datasheet UJA1164(A), Mini high-speed CAN system basis chip with Standby mode & Watchdog – NXP Semiconductors

[5] Product datasheet UJA1167, Mini high-speed CAN system basis chip with Standby / Sleep mode & Watchdog – NXP Semiconductors
Product datasheet UJA1167(A), Mini high-speed CAN system basis chip with Standby / Sleep mode & Watchdog – NXP Semiconductors

[6] Product datasheet UJA1168, Mini high-speed CAN system basis chip for partial networking – NXP Semiconductors
Product datasheet UJA1168(A), Mini high-speed CAN system basis chip for partial networking – NXP Semiconductors

[7] Product datasheet TJA1145, High-speed CAN transceiver for partial networking – NXP Semiconductors

[8] Application Hints, Rules and recommendations for in-vehicle CAN networks, TR1135 – NXP Semiconductors

[9] Application Hints, Partial Networking, AH1203 – NXP Semiconductors

[10] Product objective data sheet UJA1169, Mini high-speed CAN system basis chip family – NXP Semiconductors
Product objective data sheet UJA1169L, Mini high-speed CAN system basis chip family – NXP Semiconductors

[11] Product data sheet PNS40010ER, 400 V, 1 A high power density, standard switching time PN-rectifier – NXP Semiconductors

[12] Product data sheet PMEG6010ER, 1 A low V_F MEGA Schottky barrier rectifier – NXP Semiconductors

15. Legal information

15.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

15.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

For more information, please visit: http://www.nxp.com
For sales office addresses, email to: salesaddresses@nxp.com

Date of release: 18 January 2016

Document identifier: AN-002164