MIMXRT1170-PMIC

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Revision History

Rev. Code	Date	By	Description
A	2020-12-31	Shawn Shi	Initial release

1. Unless Otherwise Specified:

   All resistors are in ohms, 1/16 Watt,0402
   All capacitors are in uF,0402
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

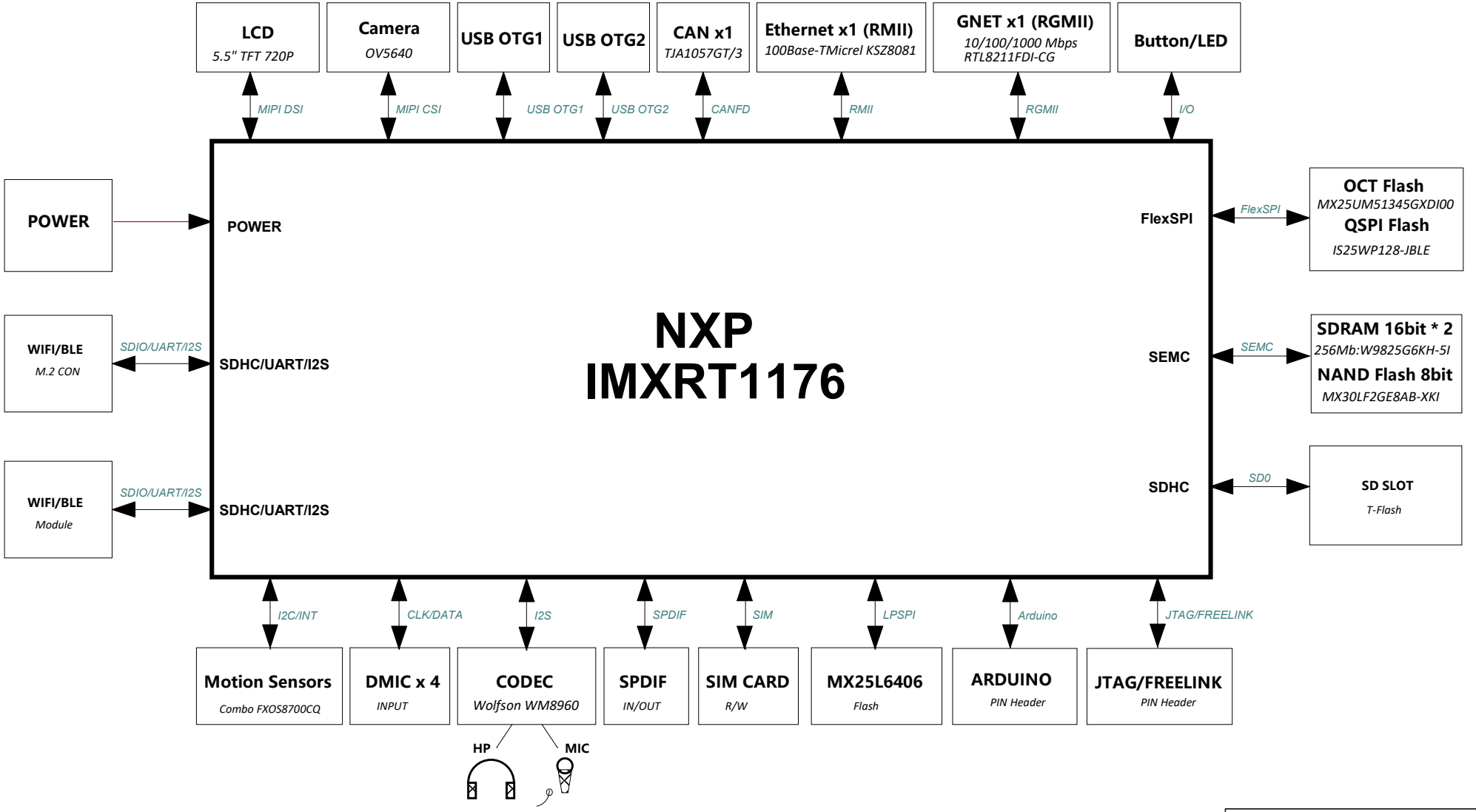
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: PUBI:

Designer: Shawn Shi	Drawing Title: MIMXRT1170-PMIC	
Drawn by: Shawn Shi	Page Title: COVER	
Approved: Yes	Size C	Document Number SCH-48118, PDF: SPF-48118 Rev A
	Date: Tuesday, January 05, 2021	Sheet 1 of 28

MIMXRT1170-PMIC

Block Diagram Rev A



ICAP Classification:	CP:	IUO:	PUBI:
Drawing Title:	MIMXRT1170-PMIC		
Page Title:	BLOCK DIAGRAM		
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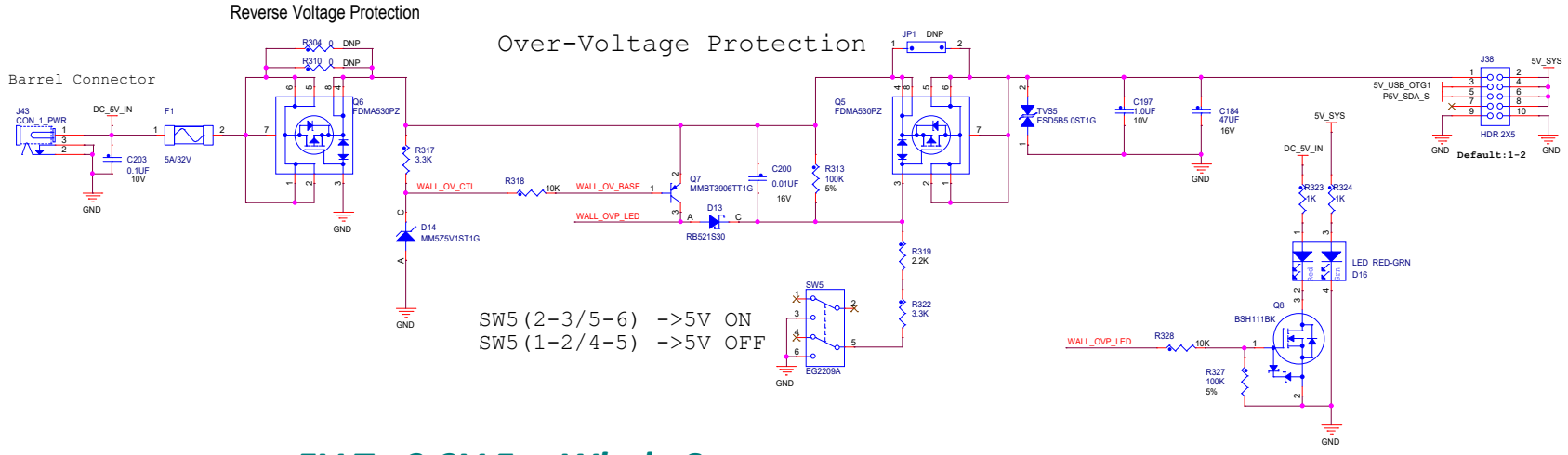
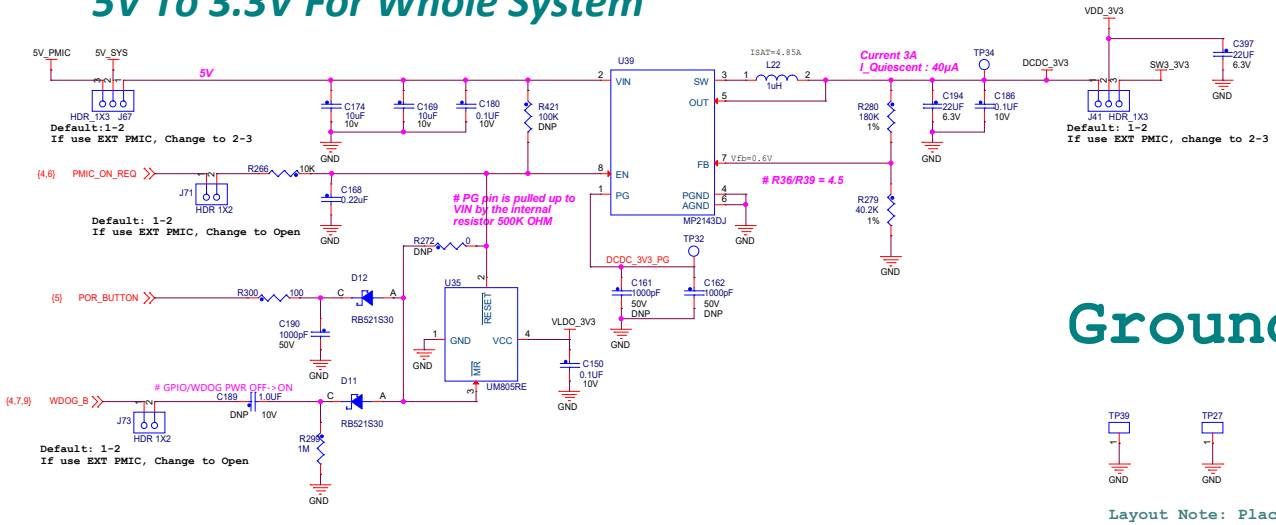
Main Power



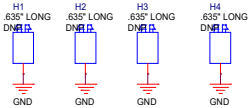
5V To 3.3V For Whole System



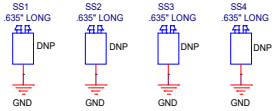
Ground TPs

Layout Note: Place Ground TPs to assist signal measurement.

Board Mounting Holes



LCD Mounting Holes



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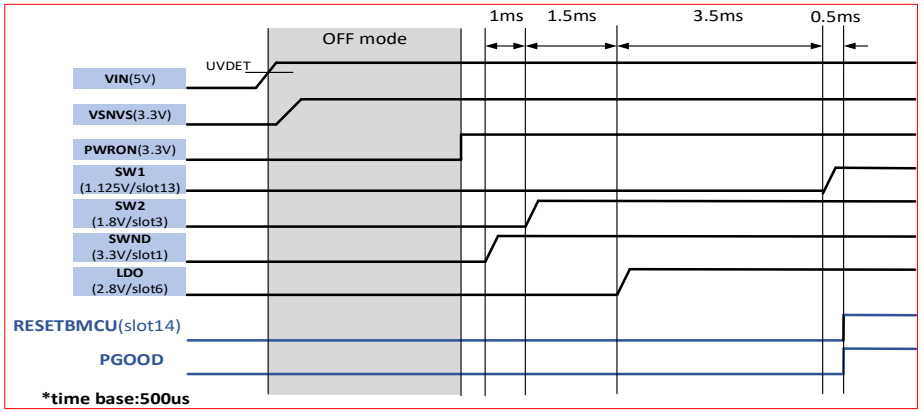
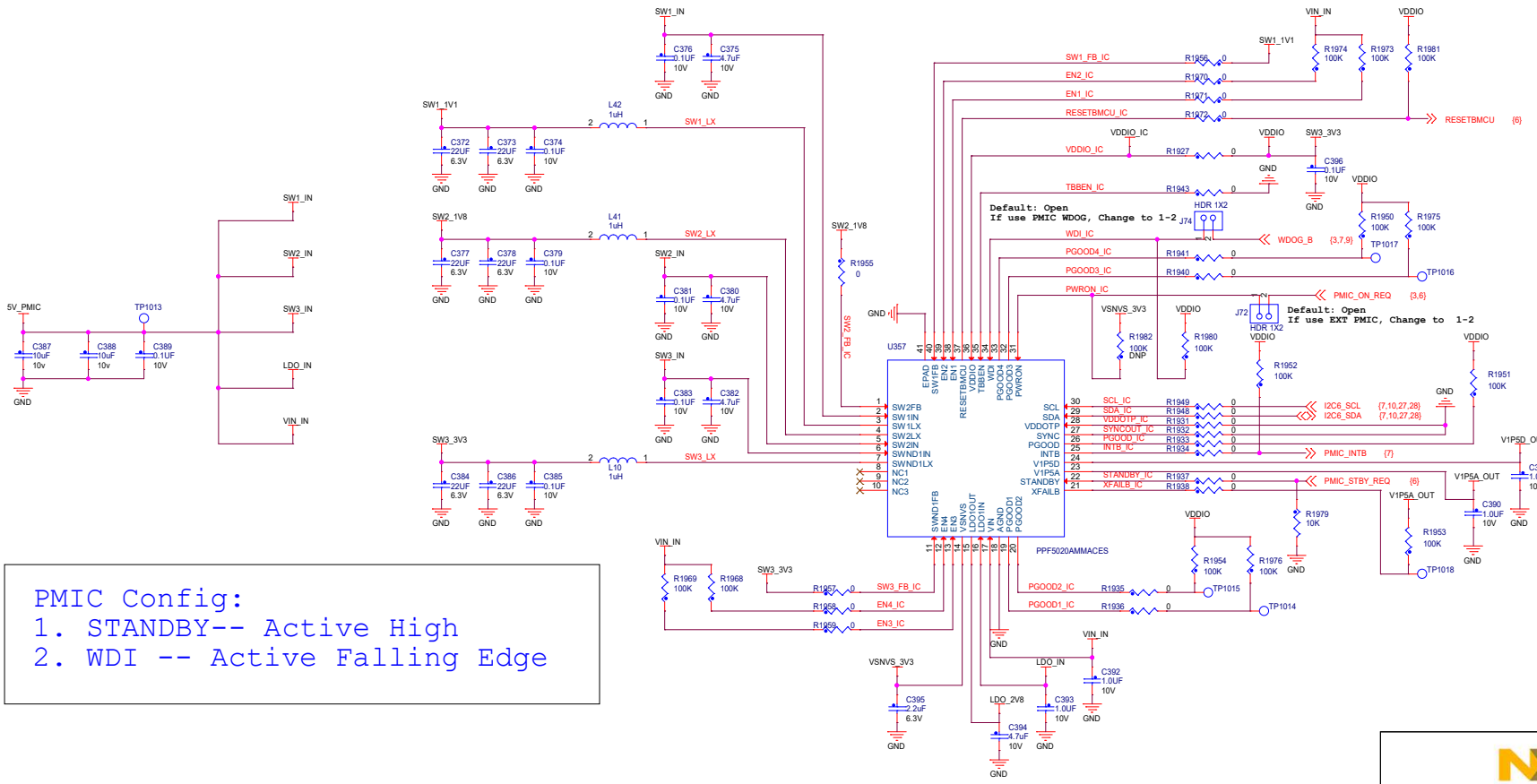
To use EXT PMIC:

1. Change J41 from 1-2 to 2-3
2. Change J53 from 1-2 to 2-3
3. Change J67 from 1-2 to 2-3
4. Change J68 from 1-2 to 2-3
5. Change J69 from 1-2 to 2-3
6. Change J71 from 1-2 to OPEN
7. Change J72 from OPEN to 1-2
8. Change J73 from 1-2 to OPEN
9. Change J74 from OPEN to 1-2
10. DNP R194,R1851,R1853
11. Populate R395,R1852,R1854





PMIC Config:

1. STANDBY-- Active High
2. WDI -- Active Falling Edge

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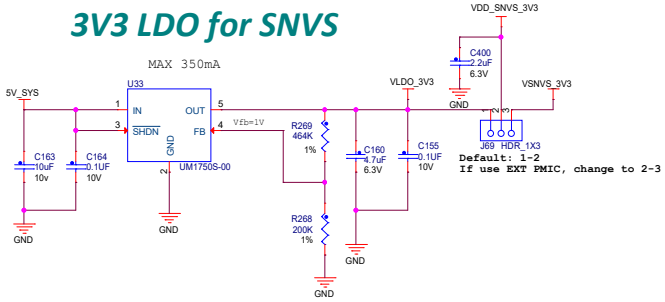
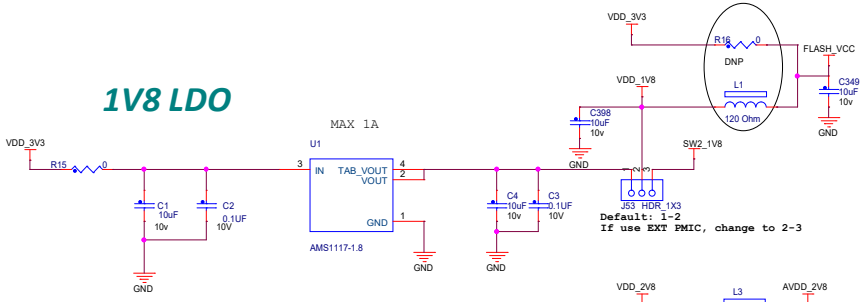
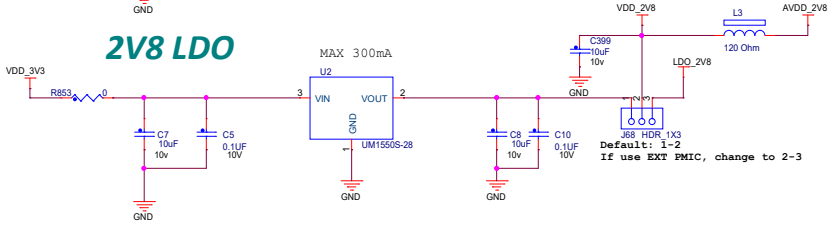
3V3 LDO for SNVS



1V8 LDO

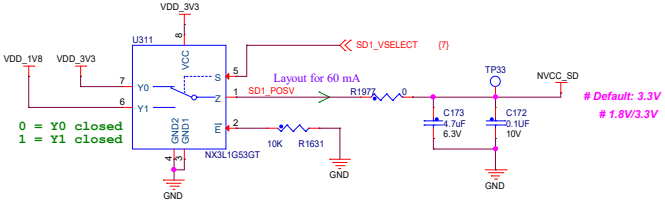


2V8 LDO

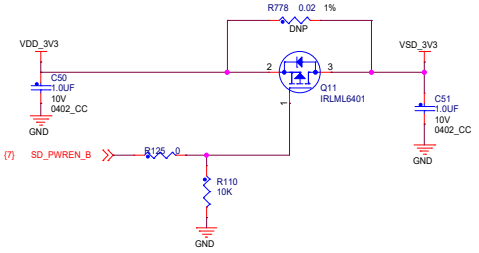


Flash VCC Option
1.8V default

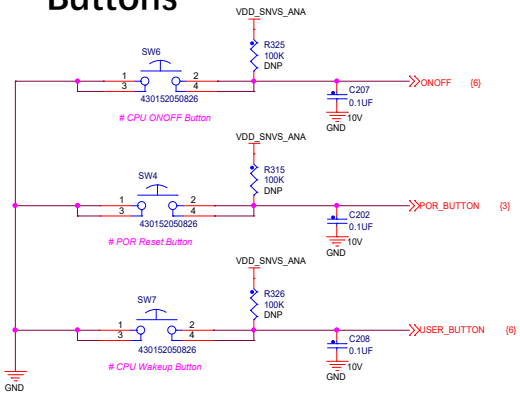
NVCC_SD <SD3.0>



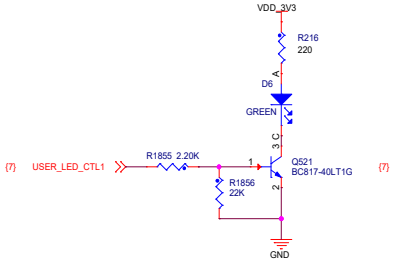
SD Card Power Switch



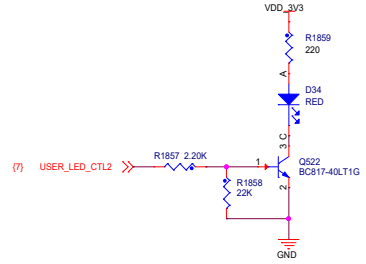
Buttons



USER LED1



USER LED2



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Drawing Title: **MIMXRT1170-PMIC**

Page Title: **POWER DOMAIN**

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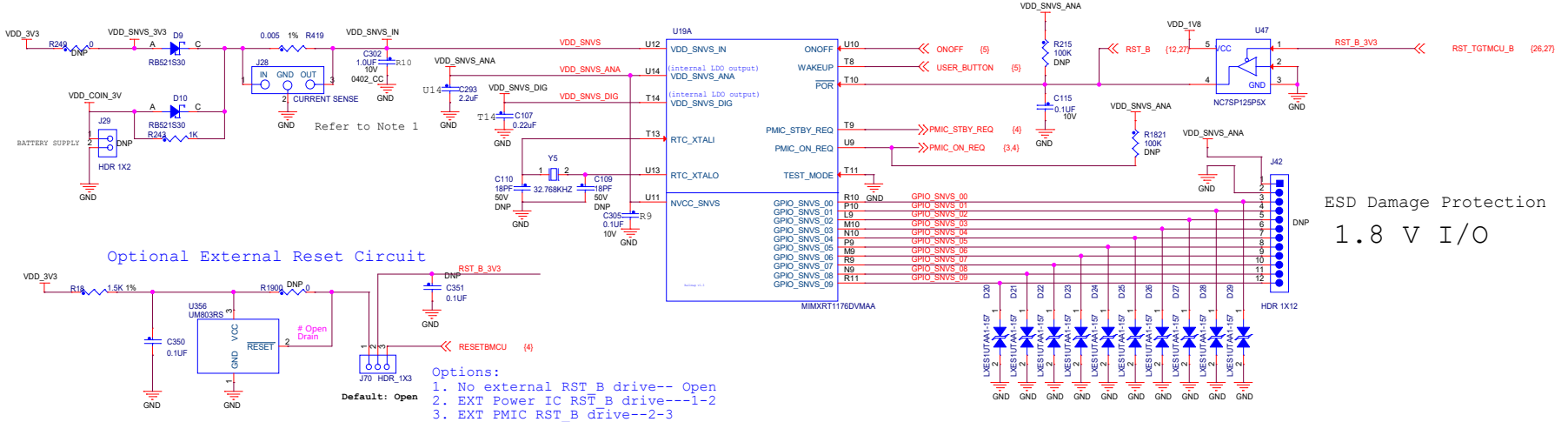
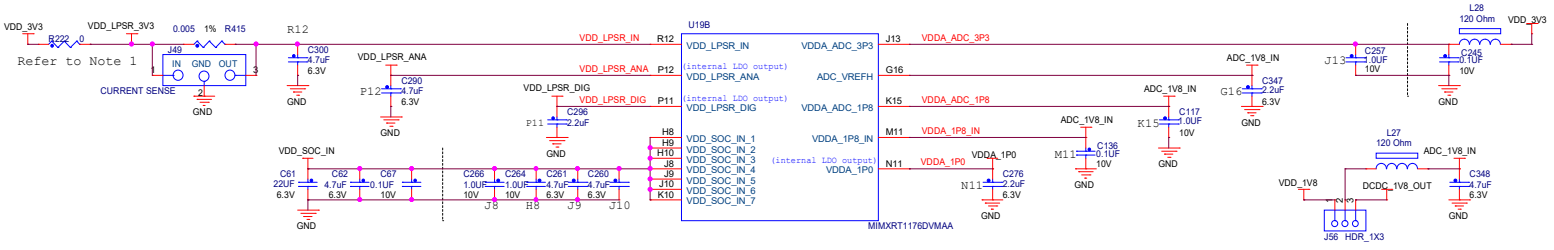
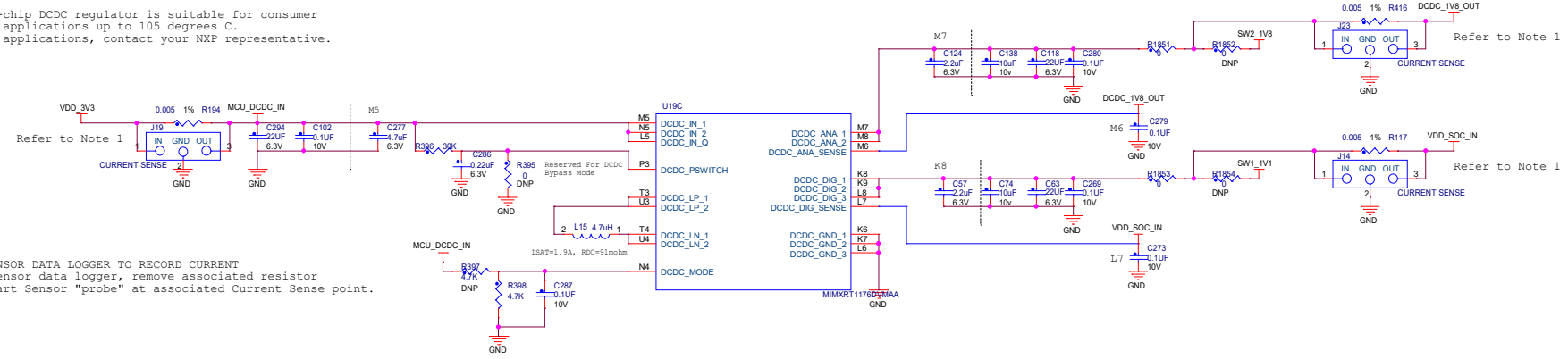




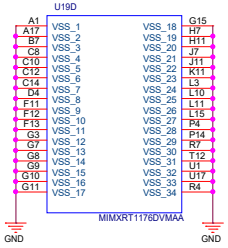
Note 1

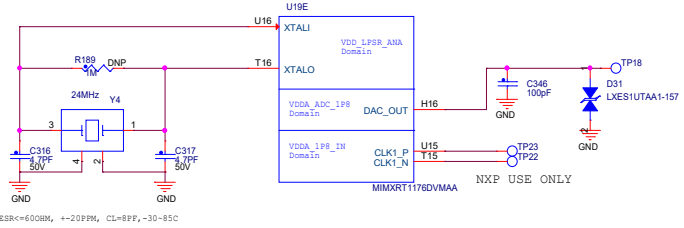
Processor's on-chip DCDC regulator is suitable for consumer
and industrial applications up to 105 degrees C.
For automotive applications, contact your NXP representative.



Note 2

USING SMART SENSOR DATA LOGGER TO RECORD CURRENT
To use Smart Sensor data logger, remove associated resistor
and install Smart Sensor "probe" at associated Current Sense point.





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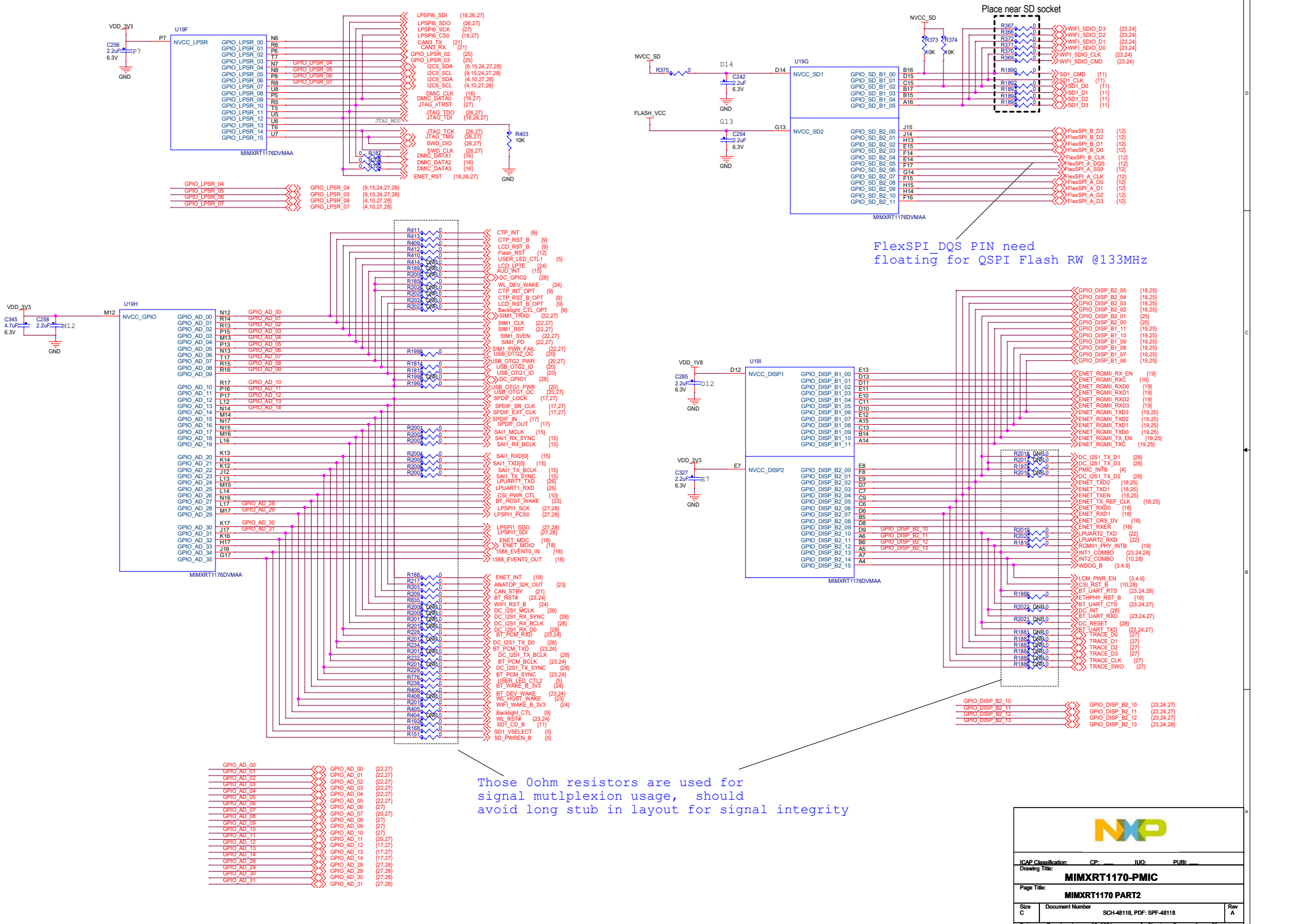
Place near SD socket
FlexSPI_DQS PIN need
floating for QSPI Flash RW @133MHz
Those 0ohm resistors are used for
signal mutlplexion usage, should
avoid long stub in layout for signal integrity
MIMXRT1176DVMAA
ICAP Classification:
CP:
IUO:
PUBI:
Drawing Title:
MIMXRT1170-PMIC
Page Title:
MIMXRT1170 PART2
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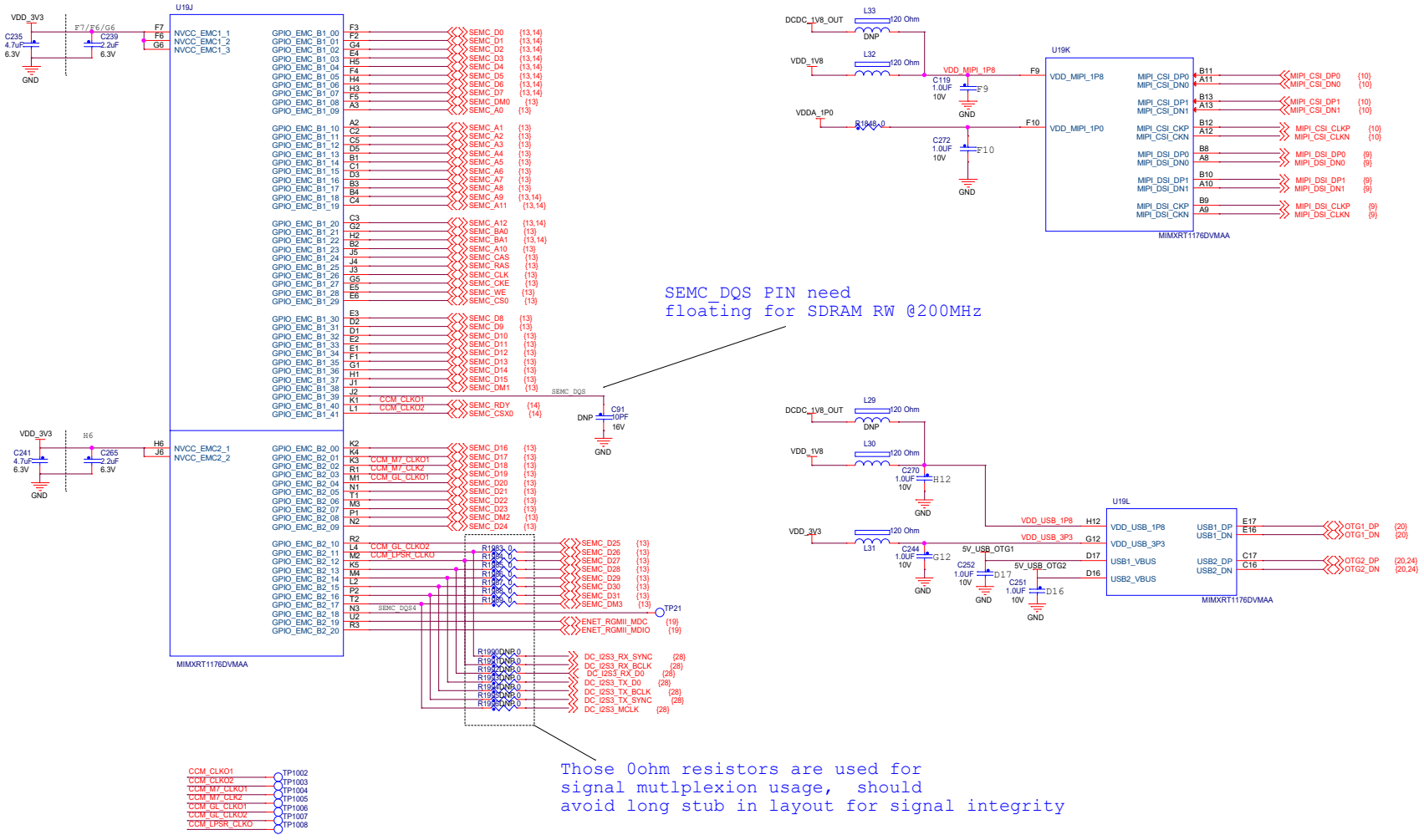

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Page Title:	MIMXRT1170 PART3		
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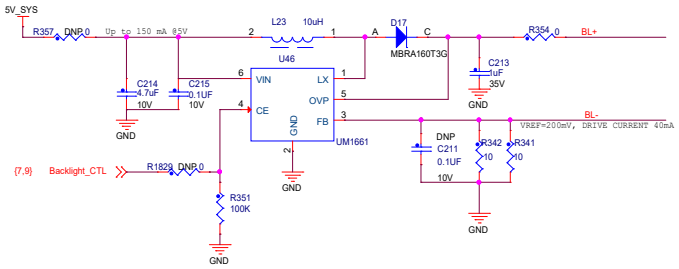
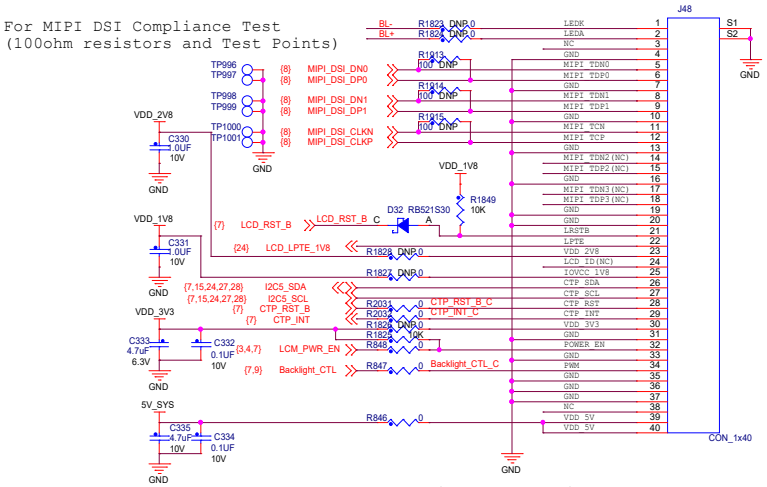
Backlight Control

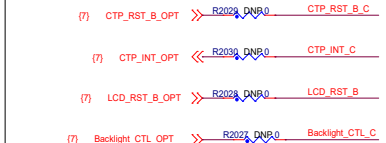


LCD P/N From Rocktech:
RK055AHD091-CTG(720P) -- Default
*RK055IQH091-CTG(540*960) -- Optional*



I2C ADD: 0X28/0X29 or 0XBA/0XBB

Resereved for use case which need both LCD and Motor Control



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Drawing Title:	MIMXRT1170-PMIC		
Page Title:	MIPI LCD		
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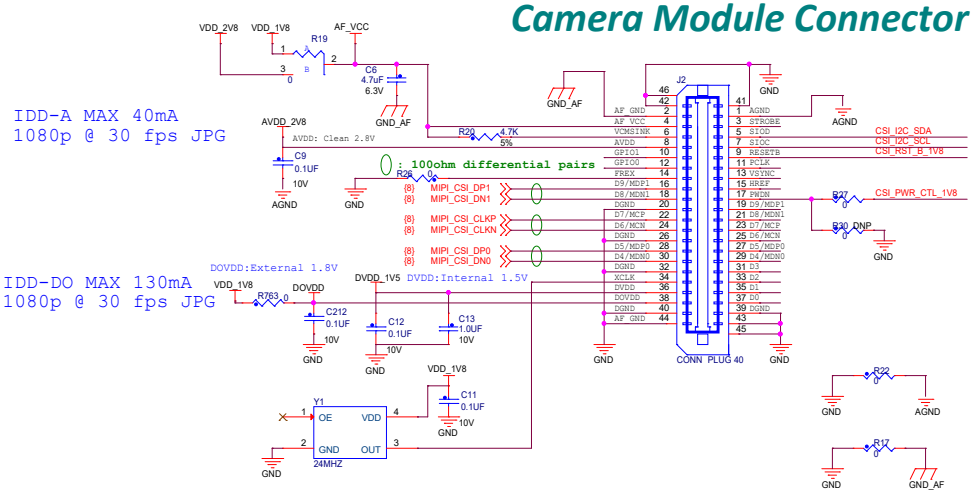
Wuxi A-KERR Science & Technology

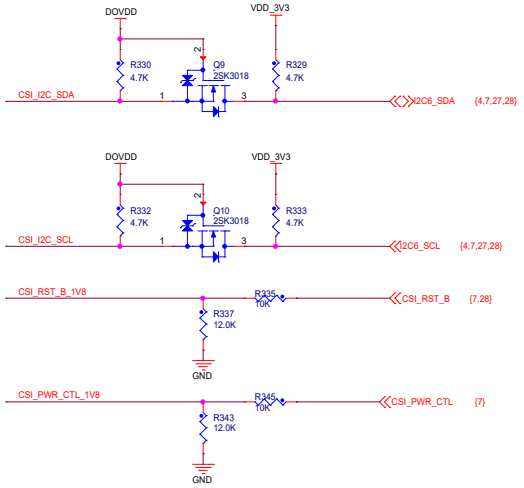
Camera# OV5640

Camera Module Connector

IDD-A MAX 40mA
1080p @ 30 fps JPG

IDD-DO MAX 130mA
1080p @ 30 fps JPG





ICAP Classification:	CP: ___ IUO:	PUBI: ___
Drawing Title:	MIMXRT1170-PMIC	
Page Title:	MIPI CAMERA	
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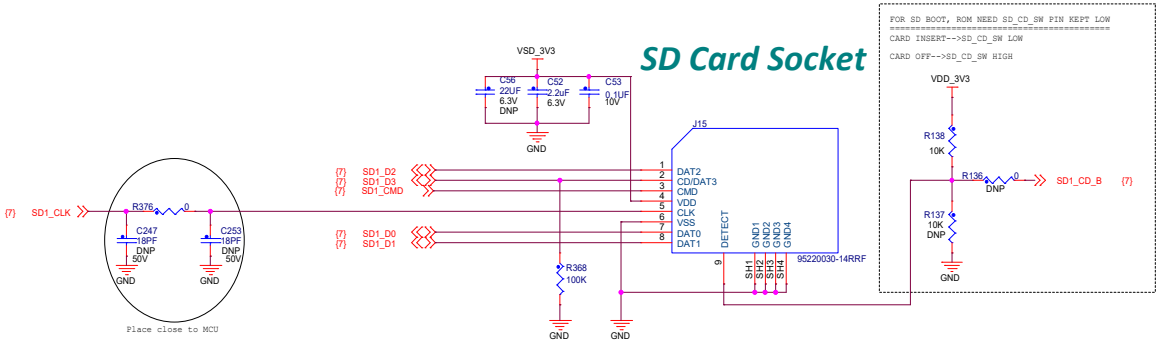

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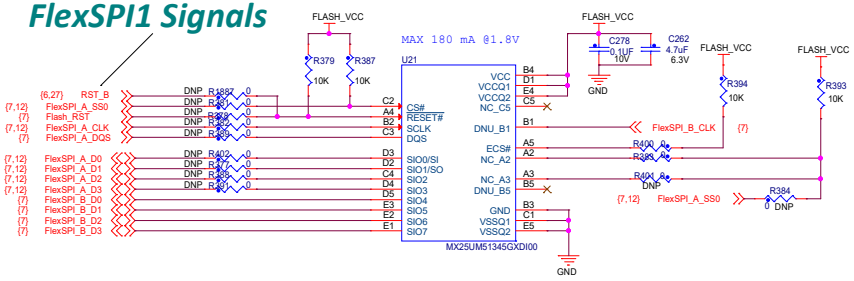
QSPI Flash as default Through FlexSPI1

OPTION1: USE QSPI FLASH(Mount R380/R399/ R386/R390/R392/R385,DNP R381/R378/R382/R389/R402/R377/R388/R391)
OPTION2: USE Octal Flash(Mount R381/R378/R382/R389/R402/R377/R388/R391, DNP R380/R399/R386/R390/R392/R385)

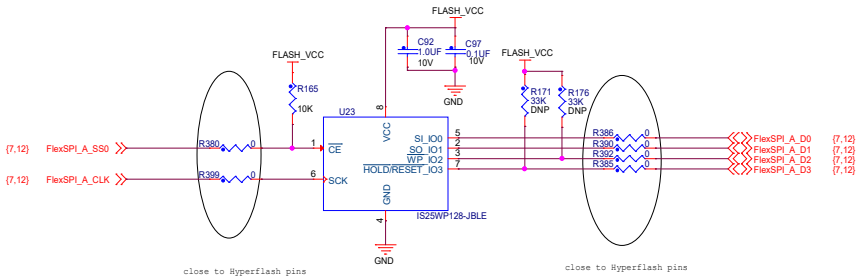
FlexSPI1 Signals

1V8 Octal Flash



Share the same package with S27KS0641DPBHI023
(if HYPERRAM is used, DNP R383/R400,Mount R401/R384)

1V8 QSPI Flash



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Drawing Title:	MIMXRT1170-PMIC		
Page Title:	FLEXSPI FLASH		
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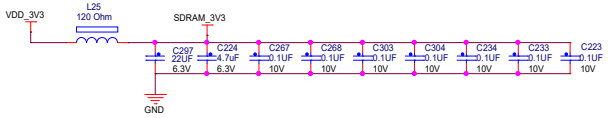
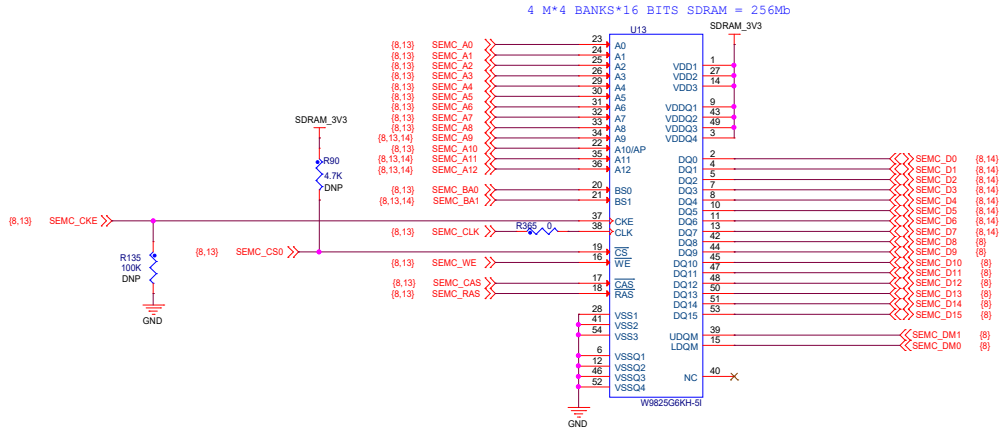
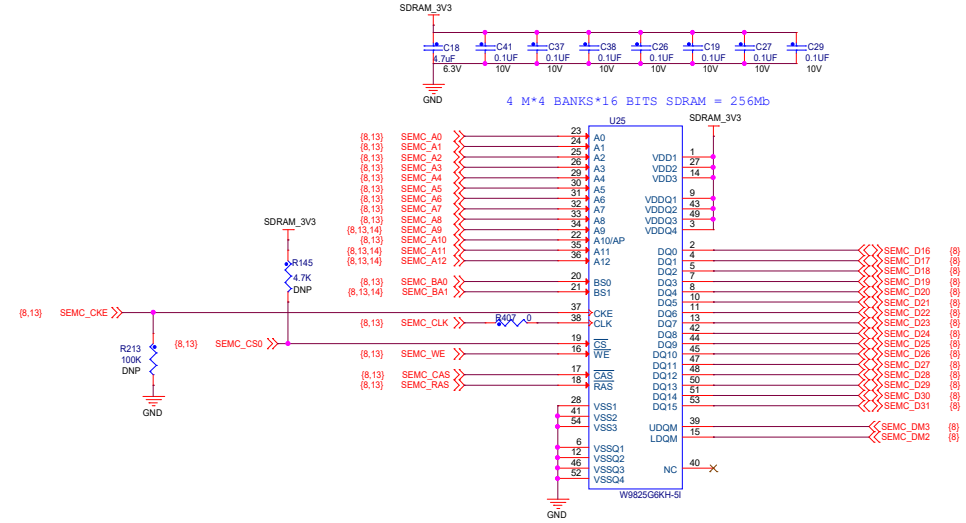


SDRAM





ICAP Classification: CP: ___ IUO: PUBI: ___

Drawing Title: **MIMXRT1170-PMIC**

Page Title: **SDRAM**

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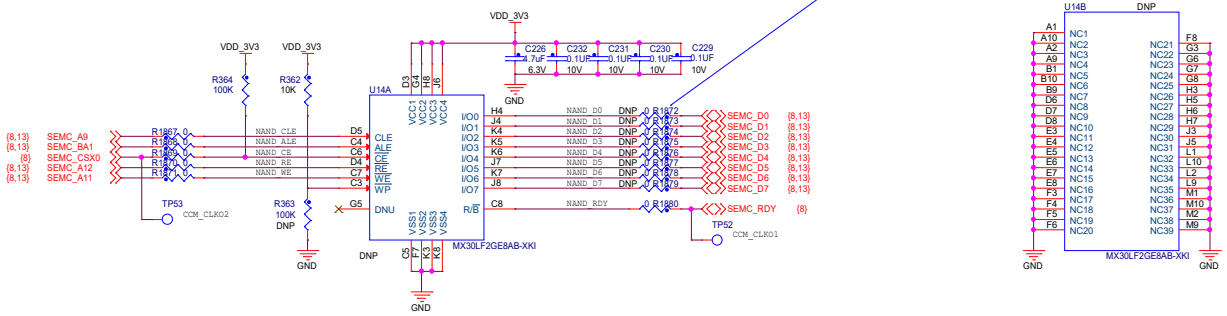
NAND FLASH

Populate R1872~R1879 to use NANDFlash



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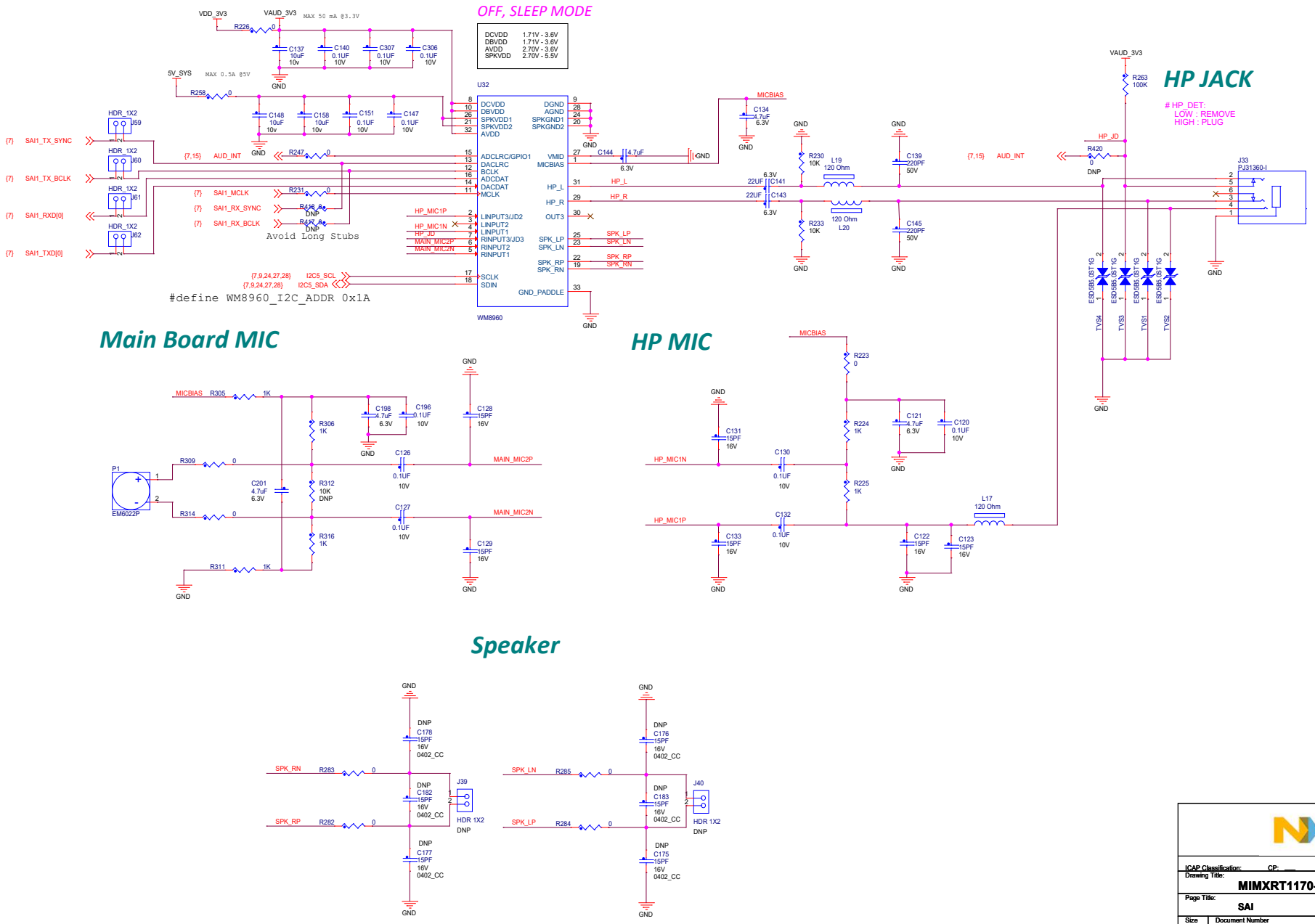
OFF, SLEEP MODE
DCVDD 1.71V - 3.6V
DBVDD 1.71V - 3.6V
AVDD 2.70V - 3.6V
SPKVDD 2.70V - 5.5V
VDD_3V3
VAUD_3V3
MAX 50 mA @3.3V
5V_SYS
MAX 0.5A @5V
U32
WM8960
#define WM8960_I2C_ADDR 0x1A
Avoid Long Stubs
HP JACK
HP_DET:
LOW : REMOVE
HIGH : PLUG
Main Board MIC
HP MIC
Speaker
ICAP Classification:
CP:
IUO:
PUBI:
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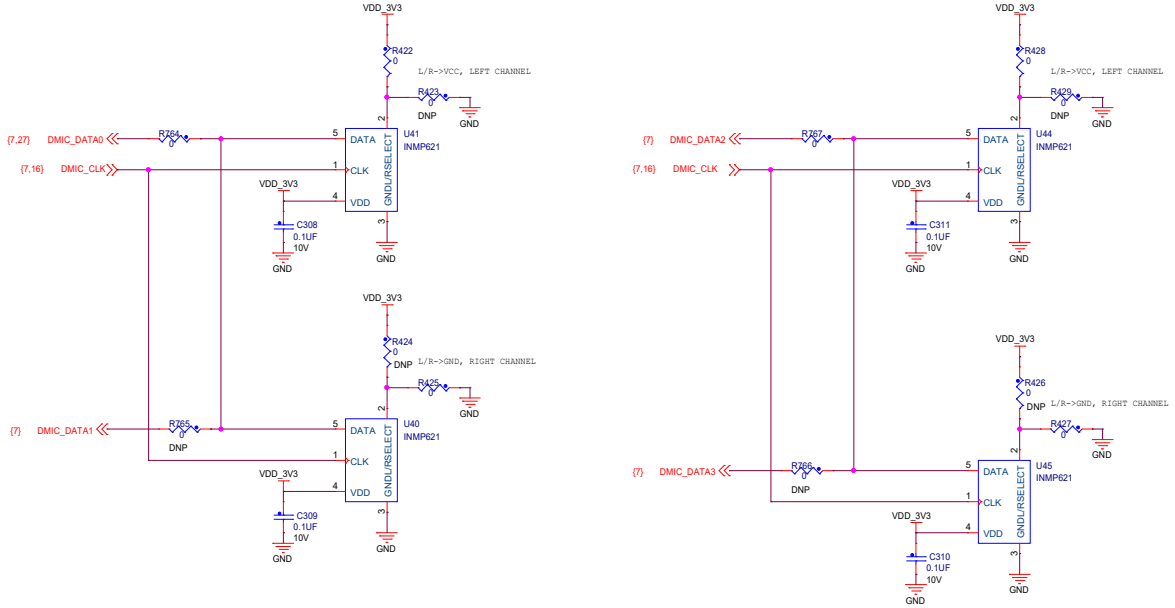
DMIC Interface



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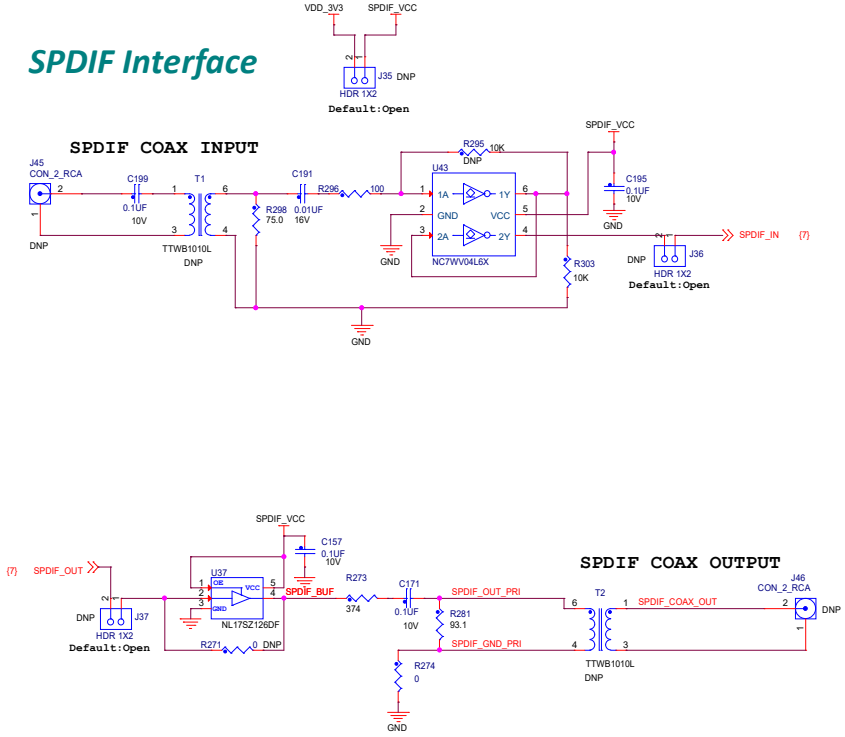
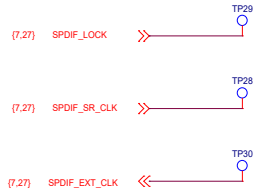
SPDIF Interface





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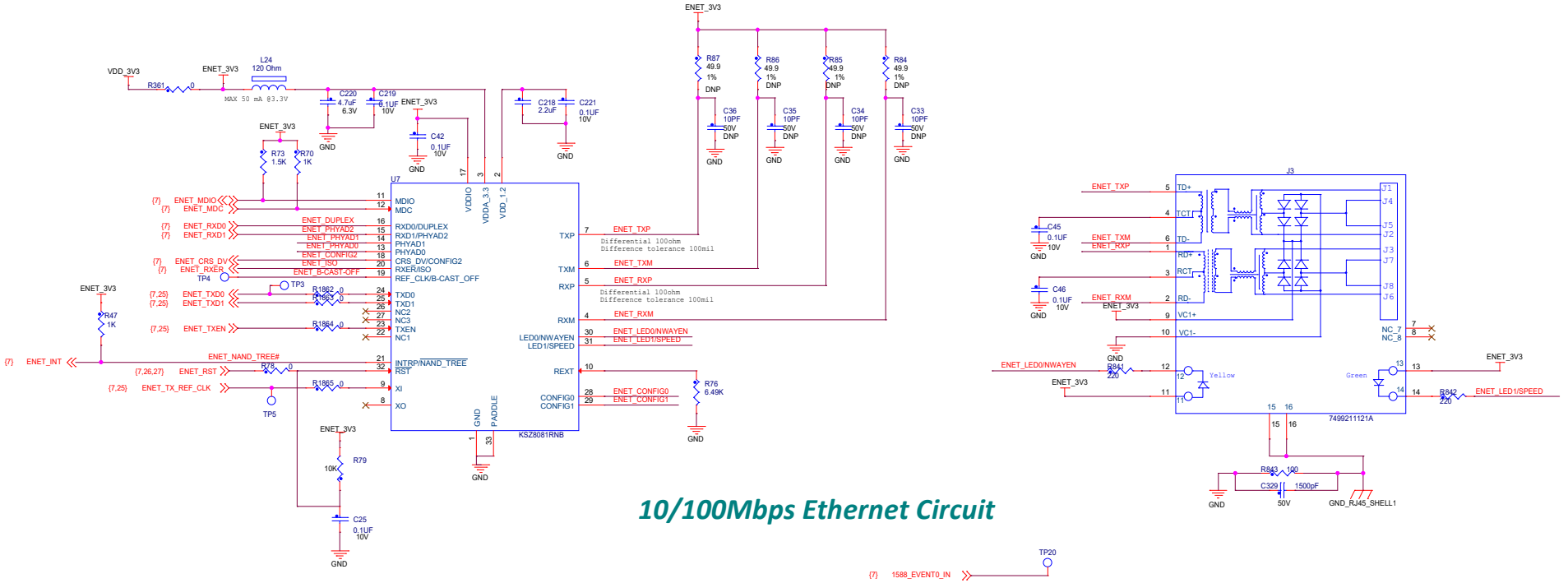
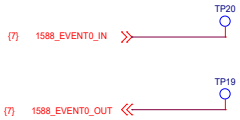
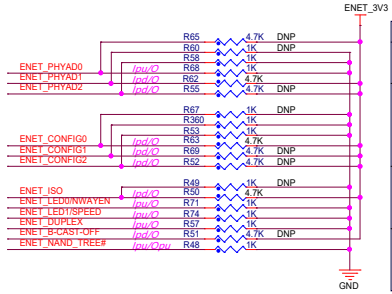


10/100Mbps Ethernet Circuit

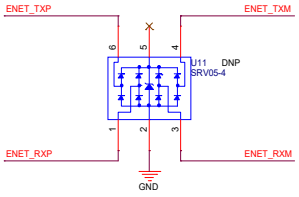




# CFG	Description
PHYAD[2:0]	PHY ADDR 00-XXX (00010 DEFAULT)
CONFIG[2:0]	IF MODE 001 RMII 101 RMII Back-to-Back xxx Reserved-not used
ISO	ISOLATE mode Pull-up = Enable Pull-down (default) = Disable
SPEED	SPEED mode Pull-up (default) = 100Mbps Pull-down = 10Mbps

# CFG	Description
DUPLEX	DUPLEX mode Pull-up (default) = Half Duplex Pull-down = Full Duplex
NWAYEN	Nway Auto-Negotiation Pull-up (default) = Enable Pull-down = Disable
B_CAST_OFF	Broadcast Off - for PHY Address 0 Pull-up = PHY Address 0 set as unique PHY addr Pull-down (default) = PHY Address 0 set as broadcast PHY addr
NAND_TREE#	NAND Tree Mode Pull-up (default) = Disable Pull-down = Enable

ESD PROTECTION



ICAP Classification: CP: ___ IUO: PUBI: ___

Drawing Title: **MIMXRT1170-PMIC**

Page Title: **10M/100M ETHERNET**

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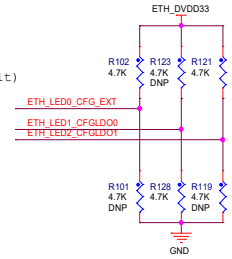
SOC RGMII 1.8V SIGNALS

{7,25} ENET_RGMII_TXC — ENET_RGMII_TXC
{7,25} ENET_RGMII_TX_EN — ENET_RGMII_TX_EN
{7,25} ENET_RGMII_TXD0 — ENET_RGMII_TXD0
{7,25} ENET_RGMII_TXD1 — ENET_RGMII_TXD1
{7,25} ENET_RGMII_TXD2 — ENET_RGMII_TXD2
{7,25} ENET_RGMII_TXD3 — ENET_RGMII_TXD3

{7} ENET_RGMII_RXC — ENET_RGMII_RXC
{7} ENET_RGMII_RX_EN — ENET_RGMII_RX_EN
{7} ENET_RGMII_RXD0 — ENET_RGMII_RXD0
{7} ENET_RGMII_RXD1 — ENET_RGMII_RXD1
{7} ENET_RGMII_RXD2 — ENET_RGMII_RXD2
{7} ENET_RGMII_RXD3 — ENET_RGMII_RXD3

CFG_EXT
EXTERNAL: 1(Default)
INTERNAL: 0

CFG_LDO[1:0]
1.8V: 10 (Default)
2.5V: 01
3.3V: 00



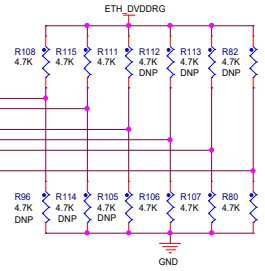
Pull-up for additional 2ns delay to TXC/RXC for data latching.

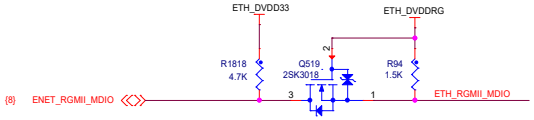
TXC Delay Config — RXD1_TXDLY
RXC Delay Config — RXD0_RXDLY

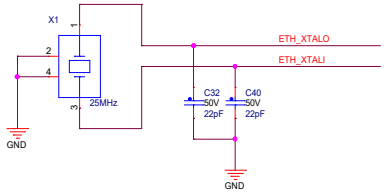
PHY_ADDR0 — RXD3_PHYAD0
PHY_ADDR1 — RXC_PHYAD1
PHY_ADDR2 — RXCTL_PHYAD2
PHY_ADDR: 00001

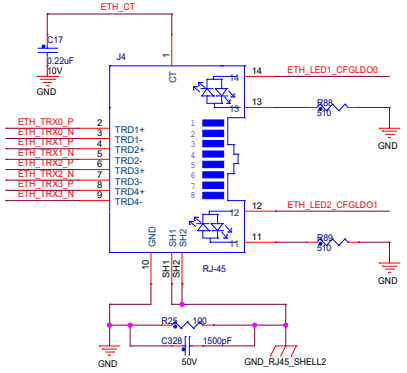
RXD2_PLLOFF

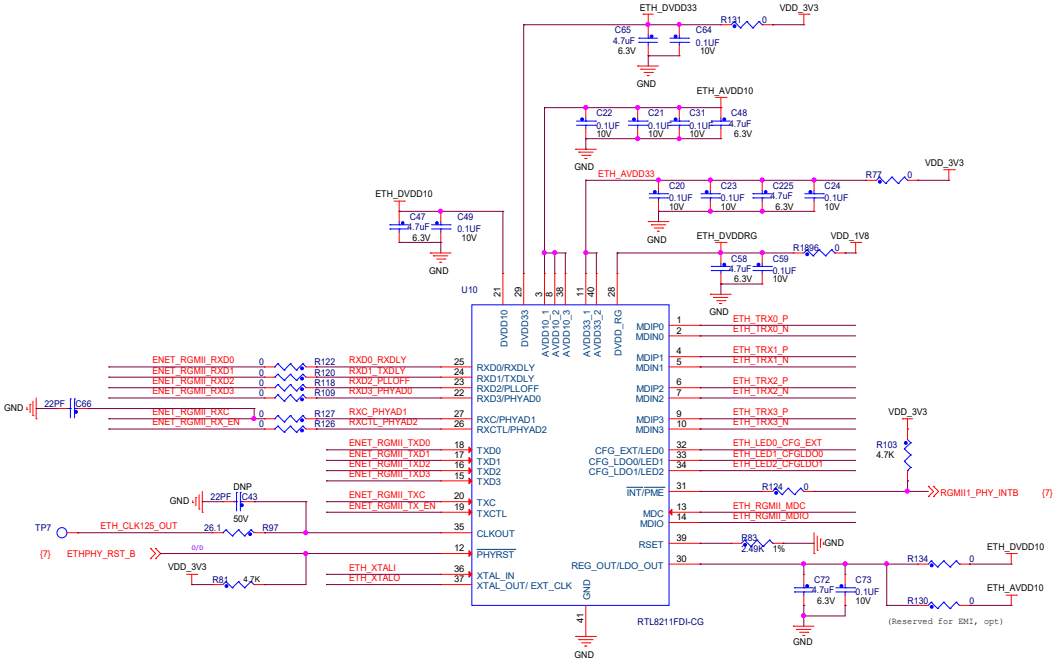
Pull-up to disable PLL @ ALDPS mode.

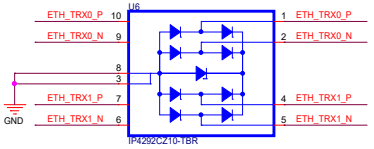


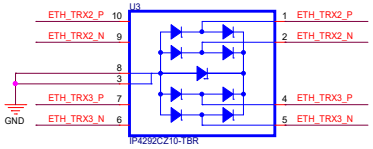












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Drawing Title:	MIMXRT1170-PMIC		
Page Title:	GIGABIT ETHERNET		
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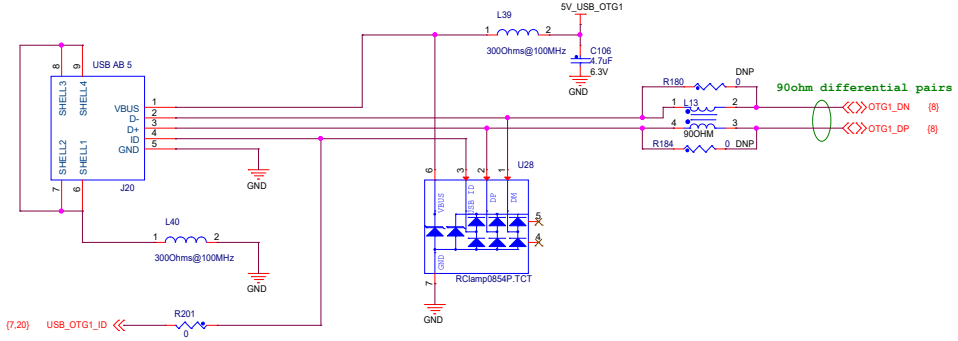
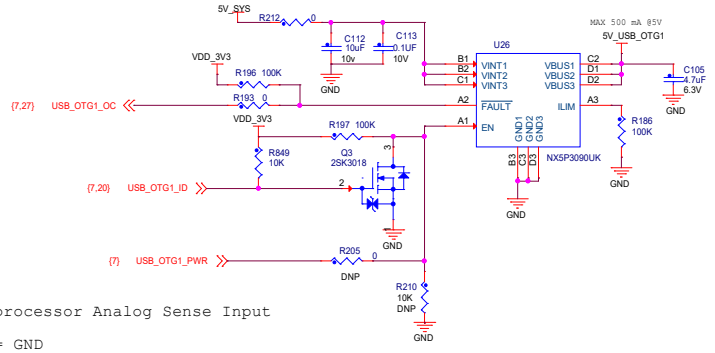
USB OTG1



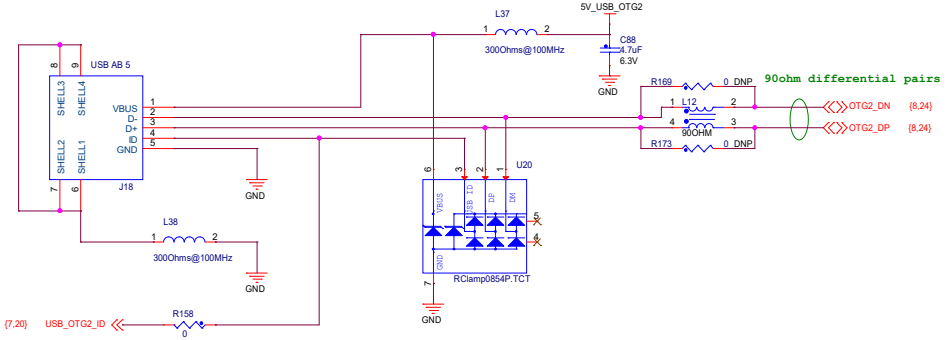
USB Power

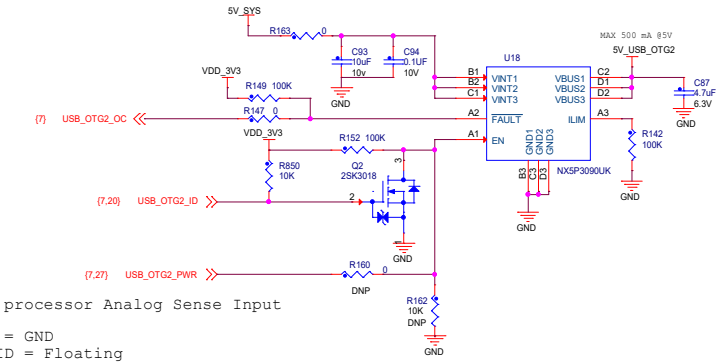


USB ID is a processor Analog Sense Input

Host --> ID = GND
Device --> ID = Floating

USB OTG2





USB ID is a processor Analog Sense Input

Host --> ID = GND
Device --> ID = Floating

ICAP Classification: CP: ___ IUO: PUBI: ___

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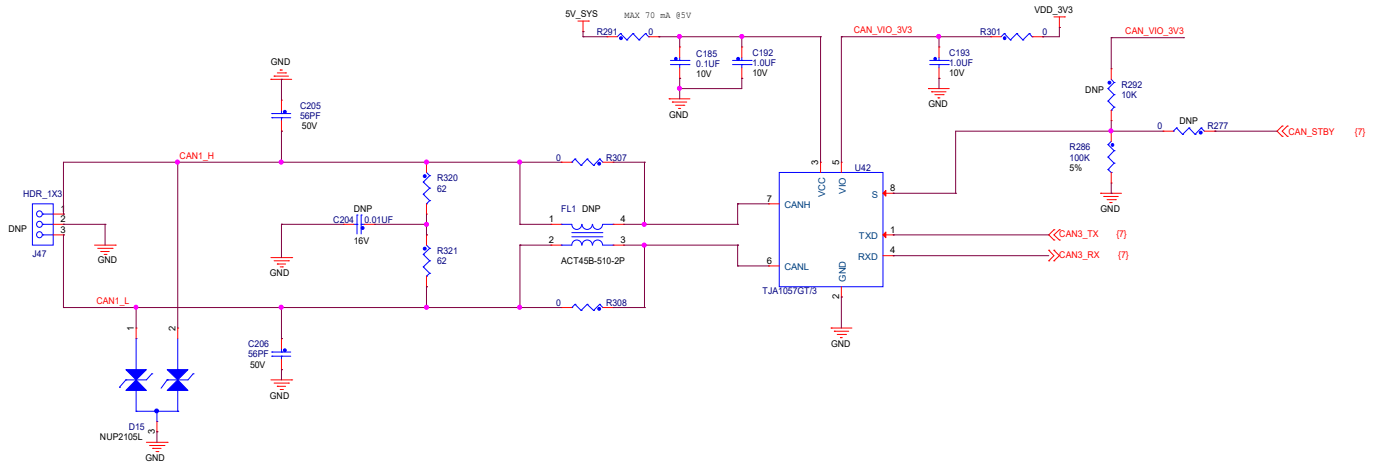
CAN Bus



ICAP Classification:	CP: ___ IUO:	PUBI: ___
Drawing Title:	MIMXRT1170-PMIC	
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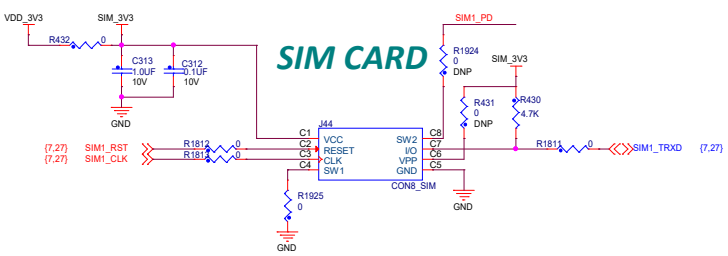
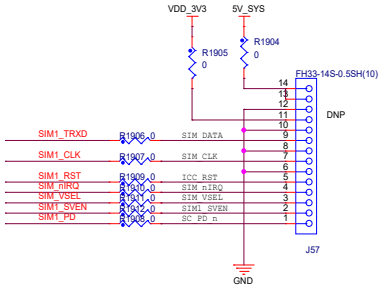
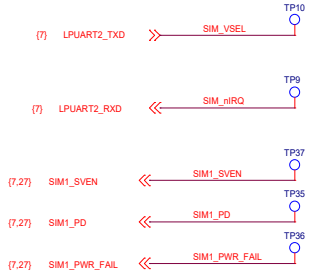
If using detection function:
Populate R1924, DNP R410

Connector reserved for EMV L1 test







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Drawing Title: **MIMXRT1170-PMIC**

Page Title: **SIM CARD**

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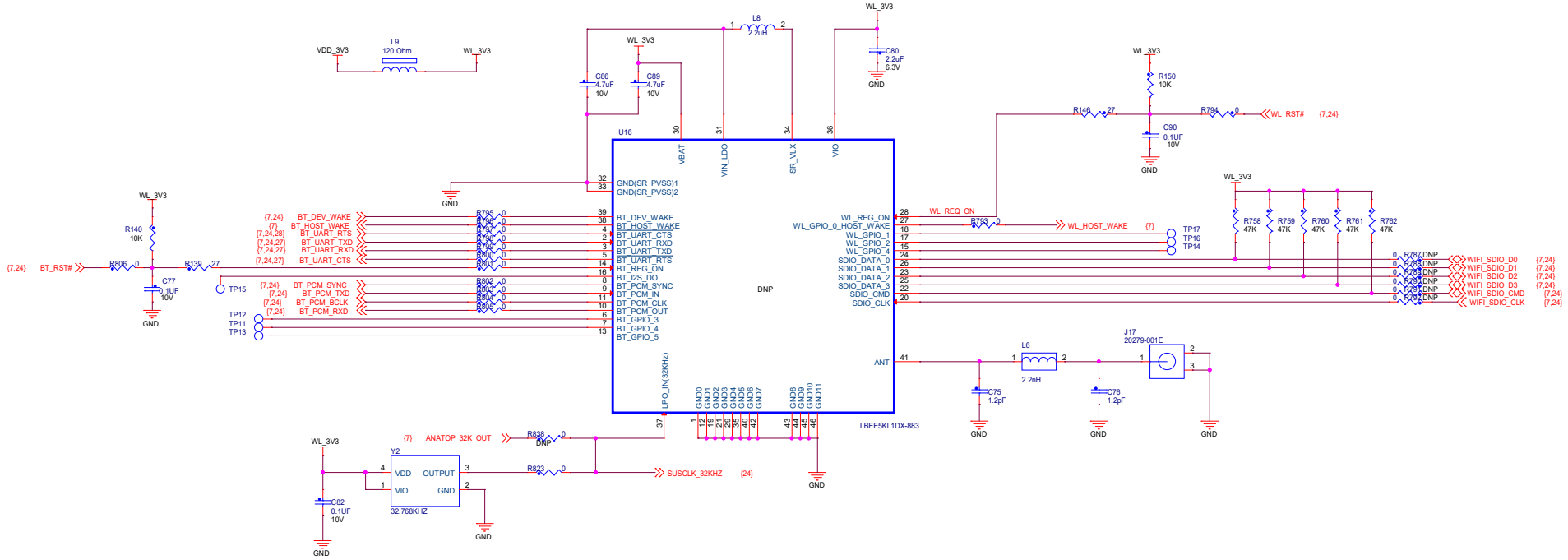
WIFI# LBEE5KL1DX-883



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Drawing Title:	MIMXRT1170-PMIC	
Page Title:	WiFi&BT	
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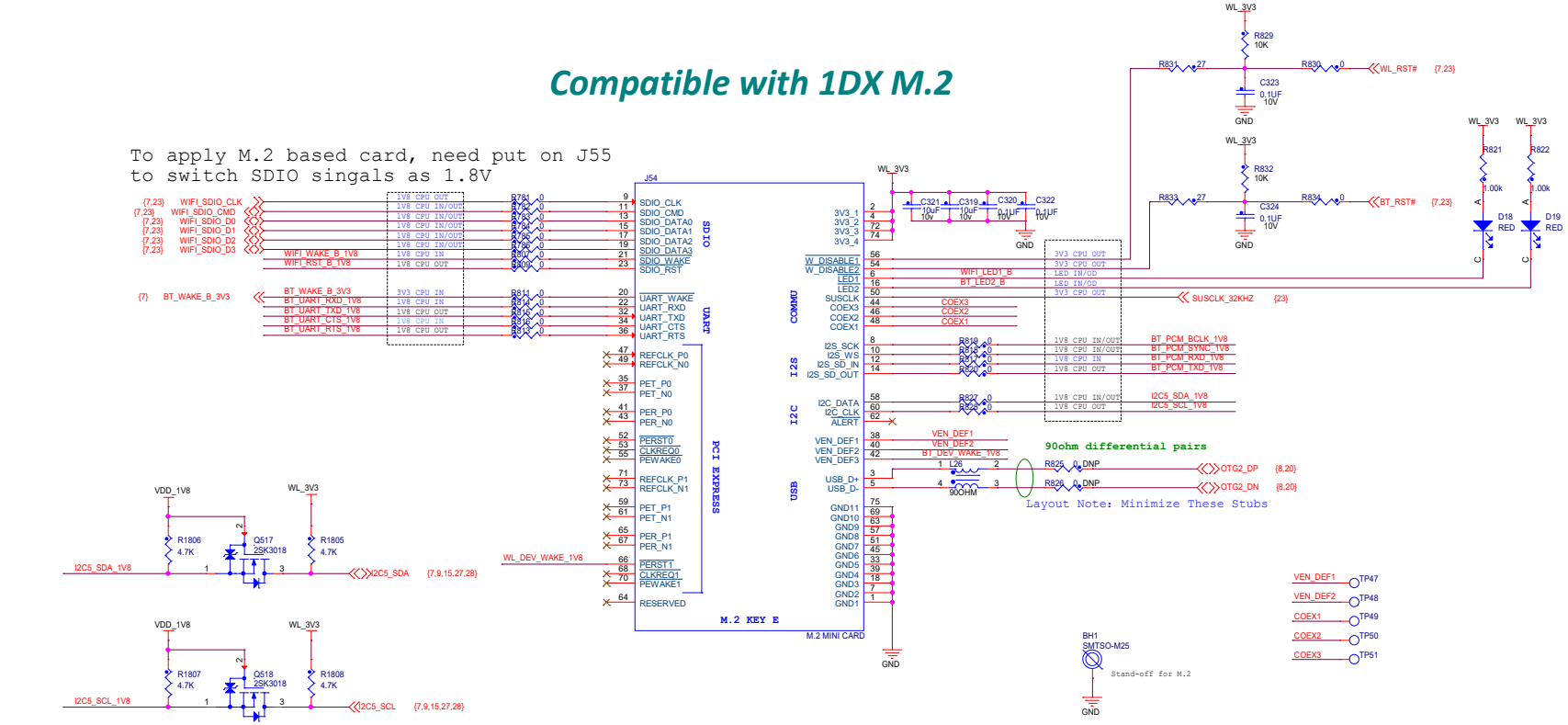
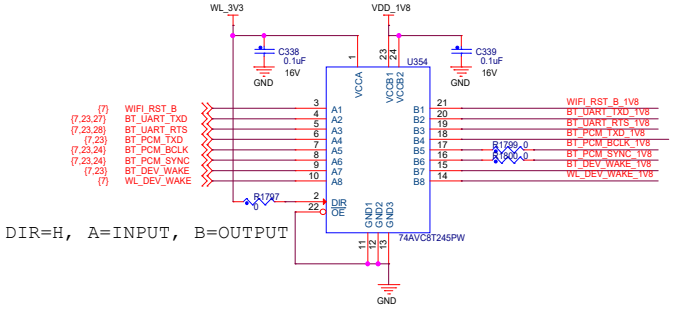
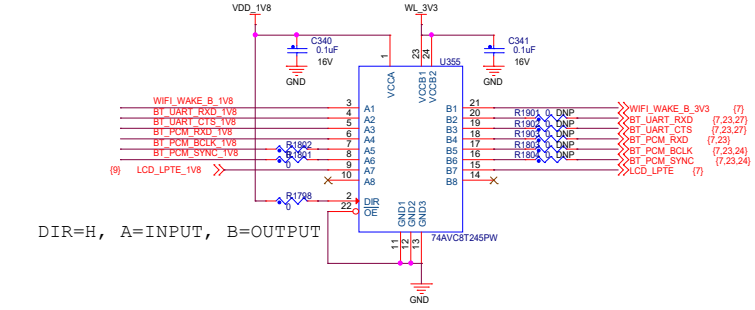
Compatible with 1DX M.2

To apply M.2 based card, need put on J55
to switch SDIO singals as 1.8V







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Page Title:	M.2 SOCKET		
Size: C	Document Number: SCH-48118, PDF: SPF-48118		Rev: A
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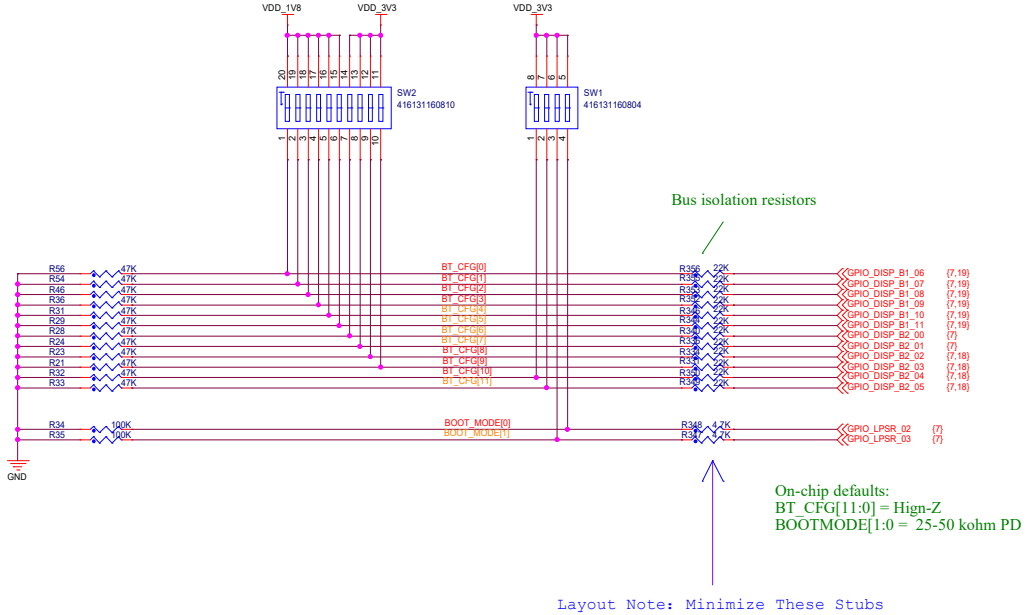
Boot Configuration

	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
TYPE	**BOOT_CFG[11]**	**BOOT_CFG[10]**	**BOOT_CFG[9]**	**BOOT_CFG[8]**	**BOOT_CFG[7]**	**BOOT_CFG[6]**	**BOOT_CFG[5]**	**BOOT_CFG[4]**	**BOOT_CFG[3]**	**BOOT_CFG[2]**	**BOOT_CFG[1]**	**BOOT_CFG[0]**
FlexSPI1 - Serial NOR	FLEXSPI_INSTANCE 0 - FLEXSPI1 1 - FLEXSPI2	xSPI_FLASH_TYPE 0 - Boot with default 0x03 Read Enabled / 1 - Reserved 2 - HyperFLASH 1V8 / 3 - HyperFLASH 3V0 4 - MXIC Octal Read / 5 - Micron Octal Read			0	0	0	0	FLASH_PROBE_TYPE 0 - QuadSPI NOR 1 - MXIC Octal 2 - Micron Octal 3 - Adesto Octal		ENCRYPT_XIP_EN	FLALSH_AUTO_PROBE_EN
SD Card	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Reserved	0	1	SD/SDXC Speed: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		SD Power Cycle Enable: '0' - No power cycle '1' - Enabled via USDHC_RST pad	SD Loopback Clock Source Sel: (for SDR50 and SDR104 only) '0' - through SD '1' - direct	Port Select: 0 - eSDHC1 1 - eSDHC2	Reserved
SEMC (NAND)	Reserved	SEMC Access Command: 0 - IPG 1 - AXI	SEMC EDO Mode: 0 - EDO Mode 1 - Non-EDO mode	ONFI compliant: 0 – Yes, ONFI 1 – No, spec	0	0	1	BOOT_SEARCH_STRIDE: Search Stride for FCB and DBBT Search strides in terms of page 0000 - 64 other: Value = 2^(BOOT_SEARCH_STRIDE)				BOOT_SEARCH_COUNT: 0 - 1 1 - 2

Boot MODE pin settings

BOOT_MODE[1:0]	Boot Type
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot
11	Reserved

External Boot Switch



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Drawing Title: **MIMXRT1170-PMIC**

Page Title: **BOOT**

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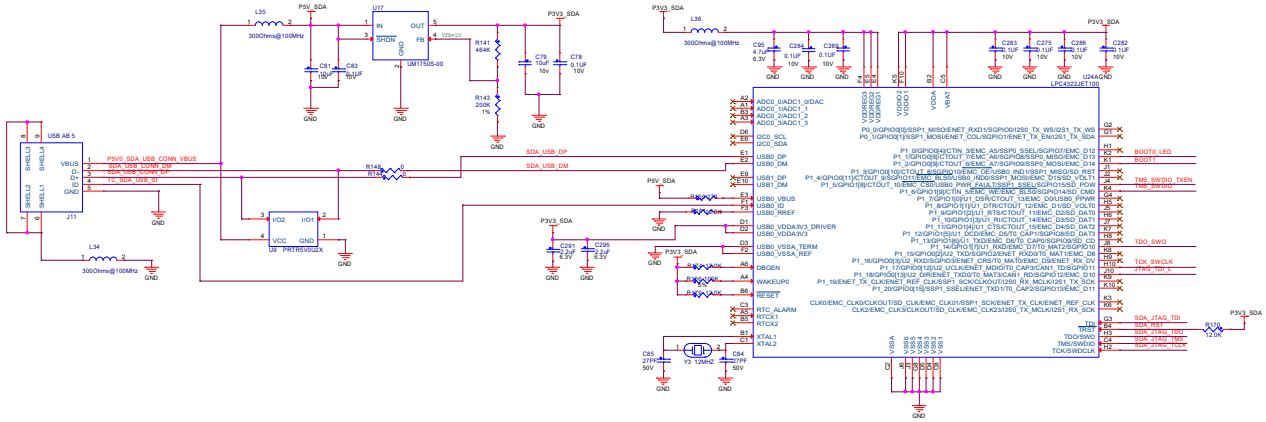
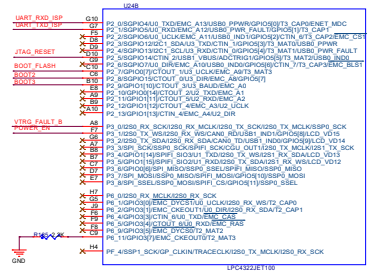
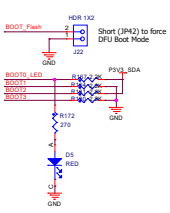
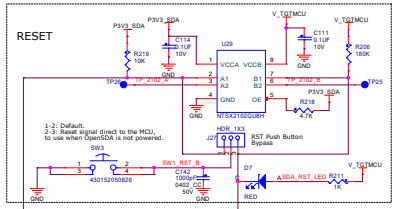
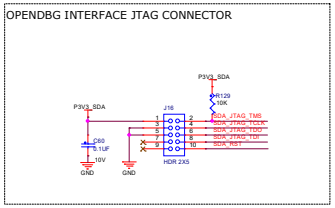
Freelink Interface

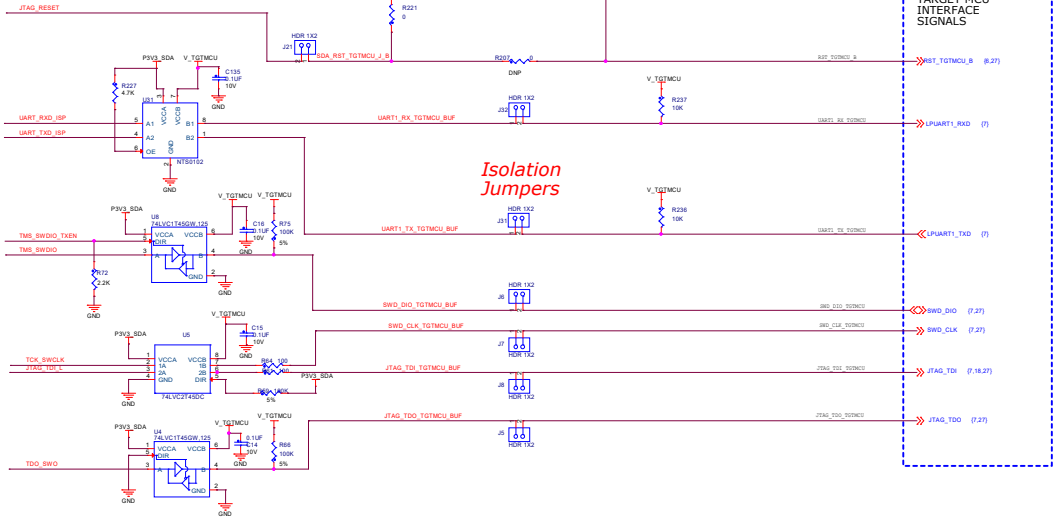


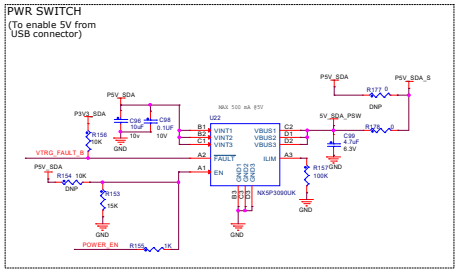












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Page Title:	FREELINK		
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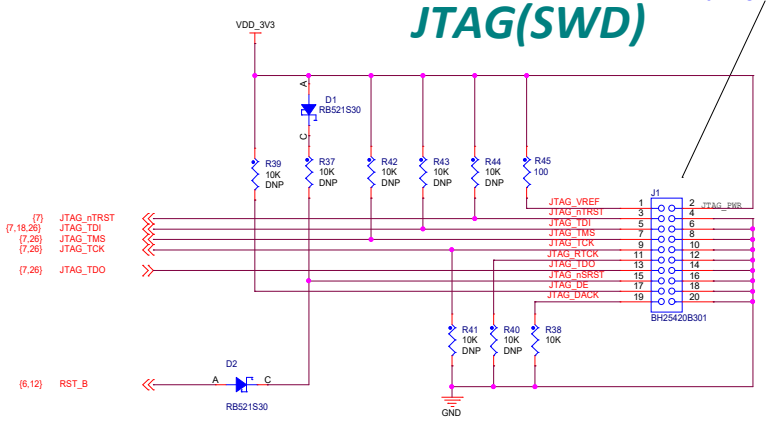
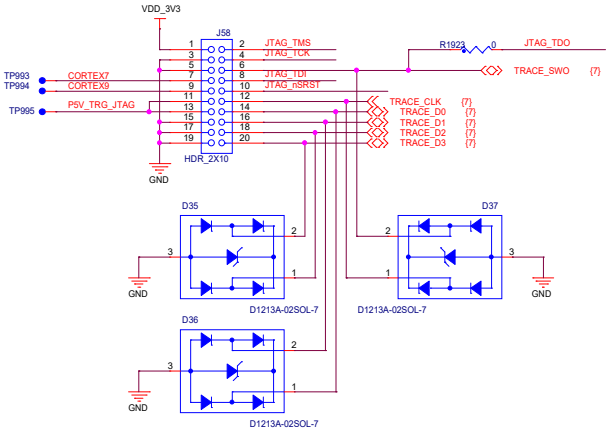
1.SWD debug is enabled by default
2.Board rework are needed to support JTAG debug

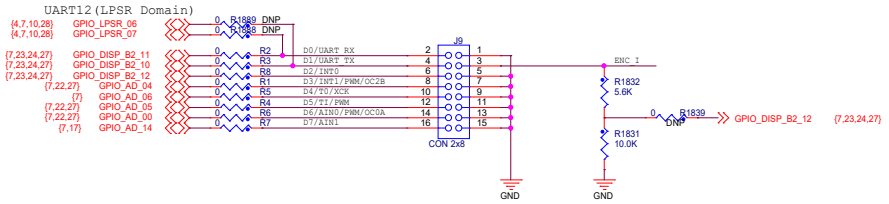
JTAG(SWD)

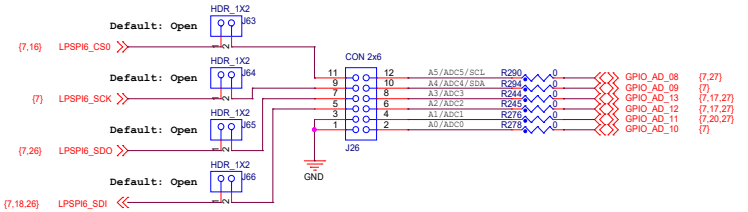


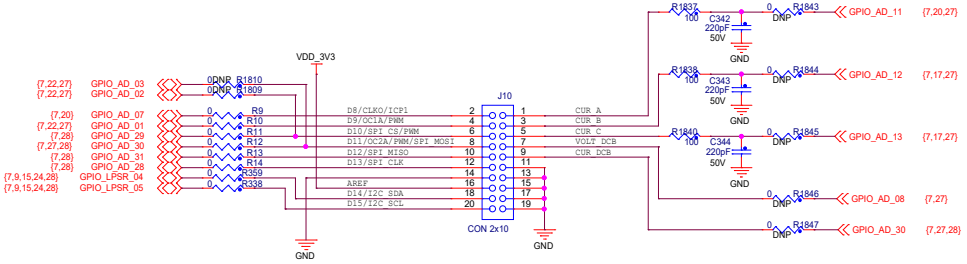
Cortex Debug + ETM

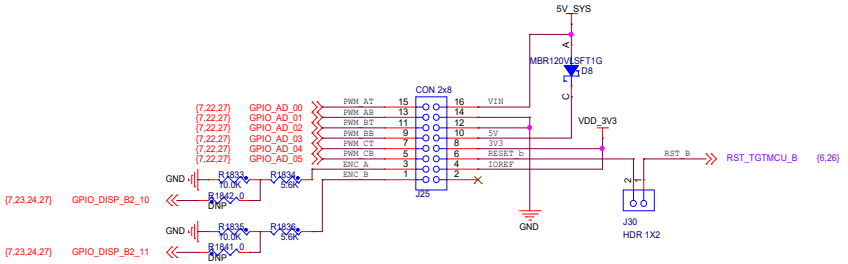


Arduino&MC Interface









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Drawing Title: **MIMXRT1170-PMIC**

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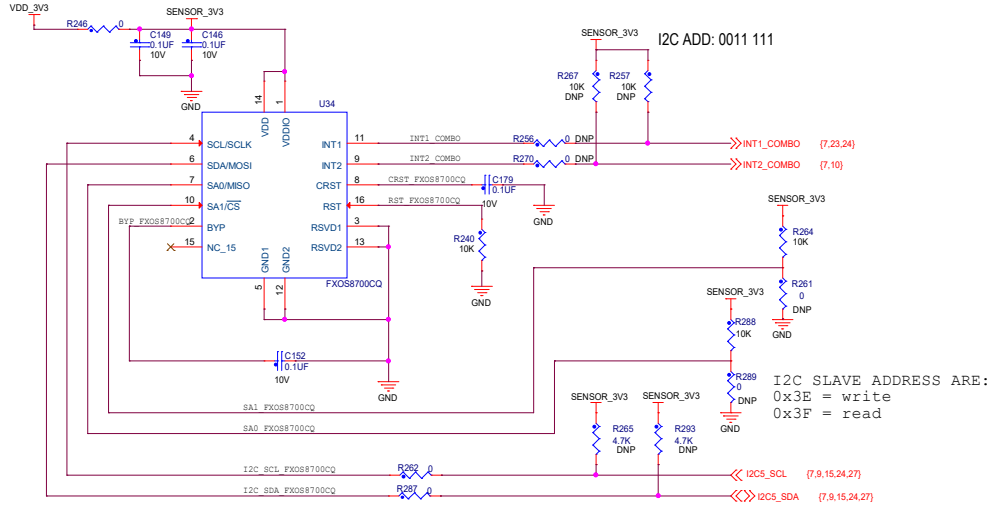
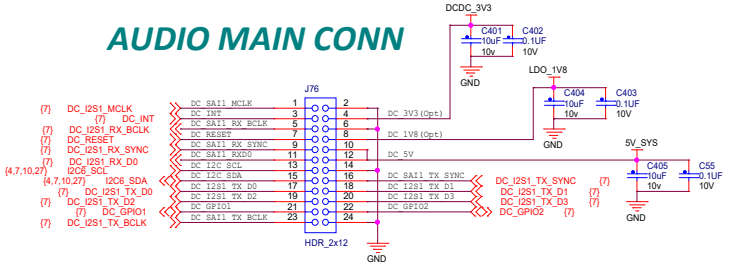
COMBO SENSOR



FXOS8700CQ Combo Sensor to include both Accelerometer and Magnetometer

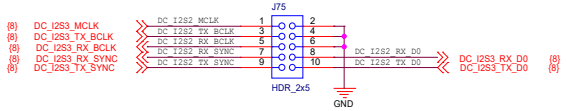
If Audio main conn (J76) is used, please mount resistors below, R2008,R2022,R2011,R2021,R2009,R2010,R2012,R2016,R1998,R2013,R2014, R2018,R2017,R2000

AUDIO MAIN CONN

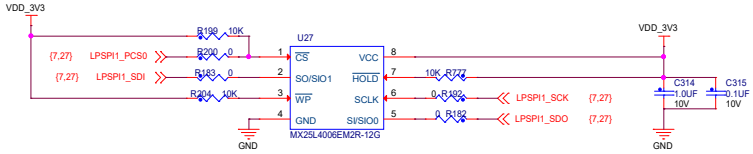


If Audio aux conn (J75) is used, please mount resistors below, R1996,R1994,R1991,R1990,R1995,R1992,R1993

AUDIO AUX CONN



LPSPI Flash(Secondary Boot)



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Drawing Title:	MIMXRT1170-PMIC		
Page Title:	MISC		
Size: C	Document Number: SCH-48118, PDF: SPF-48118		Rev: A
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