NXP Semiconductors
Design Reference Manual

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HVP-LLC Design Reference Manual

LLC fully digital resonant converter

1. Introduction

This document describes the LLC resonant converter reference design. It contains detailed information about the hardware and software and provides a control software example.

The high-voltage resonant converter board (also known as HVP-LLC) in combination with the HVP-KV46F150 controller card provides a solution for a 250-W power supply with input voltage of 390 V DC and output voltage of 12 V/21 A. This board uses GaN low-loss switches and a digitally-controlled synchronous rectifier, which enables to achieve efficiency of above 96 % in a wide range of loads. The photo of the system is shown in Figure 1. The platform consists of the controller card and the main board.

Contents

Figure 1. LLC board

WARNING

This board set operates in an environment that includes dangerous voltages that may result in electrical shock, fire hazard, or personal injury if not handled or applied properly. Use this board carefully and employ appropriate safeguards to avoid personal injury or property damage.

Only qualified persons familiar with the risks associated with handling high-voltage electrical systems and subsystems can use this evaluation board.

Use this evaluation board only in a laboratory environment. The evaluation board is not a finished end-product fit for general consumer use.

For safe operation, the input power for the high-voltage power stage must come from a current-limited laboratory power supply.

If an isolated power supply is not used, the power stage grounds and the oscilloscope grounds have different potentials, unless the oscilloscope is floating. Note that the probe grounds and floating oscilloscope are subject to dangerous voltages.

NOTE

Use a current-limited DC power supply with a current limit of 1 A to power this board.

Before moving the scope probes and making connections, it is recommended to power down the high-voltage supply.

Do not touch the EVM or components connected to the EVM when these components are powered.

Always wear safety glasses, use shields, do not wear ties and jewelry, and operate the development tool set only if you are trained in high-voltage laboratory techniques.

The power semiconductors and the transformer can reach temperatures high enough to cause burns.

When powering down, dangerous voltages are present until the power-on LED is off due to the residual voltage in the bus capacitors.

This board is an electro-static sensitive device. Handle it only at ESD workstations.

2. Theory

2.1. Resonant converter topologies

The demand to increase the power density of switched-mode power supplies pushes designers to use a higher switching frequency. A high switching frequency significantly increases switching losses at Pulse Width-Modulated (PWM) converters. It decreases the efficiency and some space (saved by using smaller passive components) is wasted by larger heating or forced cooling. Therefore, SMPS designers look for solutions to decrease switching losses.

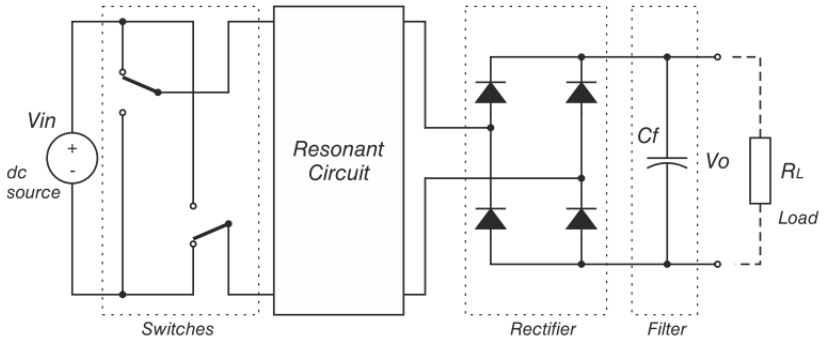

Figure 2. Resonant converter topology

One possible solution is to use resonant converter topologies. A resonant converter uses a resonant circuit in the conversion path. A typical structure of a resonant converter is shown in Figure 2. The switching network generates a square-wave voltage output with a 50 % duty cycle. This voltage pattern feeds the resonant tank. The resonant tank consists of a serial (or parallel) combination of the L and C passive components. There are several combinations of two or three L and C passive components used in the resonant tank. The type of the resonant tank and its connection to the load defines the resonant converter behavior. Due to the resonant tank, the semiconductor switches can operate at a zero voltage or a current-switching condition. This phenomenon significantly reduces switching losses and enables the converter to operate at high switching frequencies.

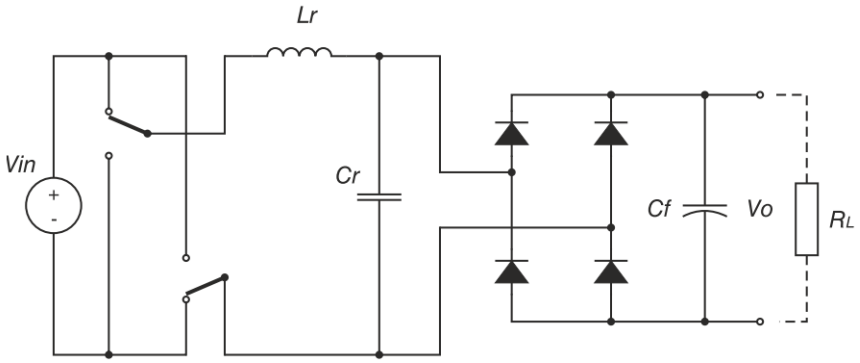

Figure 3. Parallel Resonant Converter topology (PRC)

The PRC (another well-known topology) is shown in Figure 3. The PRC topology uses the same resonant tank as the serial resonant converter (the serial connection of inductor L_r and capacitor C_r). The PRC topology differs in the load connection to the resonant tank. In this case, the load is connected in parallel to capacitor C_r. In this configuration, the voltage divider consists of the impedance of inductor (L_r) and the impedance of the parallel combination of capacitor C_r and load R_L. This means that both parts (the top and bottom impedances) of the voltage divider are frequency-dependent. At a direct current or low switching, the output voltage of the parallel resonant converter is equal to the input voltages. When increasing the switching frequency, the output voltage also increases due to the characteristics of the resonant tank. The maximum output voltage is achieved at a resonant frequency, where the output voltage is Q times higher than the input voltage. Q is the quality factor of the resonant tank. Over the resonant frequency, the output voltage falls, because the inductor impedance becomes more dominant over the capacitor impedance.

The PRC topology can control the output voltage even at no-load conditions. In this case, the load is composed only of the resonant tank. On the other hand, the permanent connection of the resonant tank to the switch network brings some drawbacks at a nominal operation. At a nominal load, the parallel converter operates close to the resonant frequency and the resonant tanks have the lowest impedance. This also causes high current to circulate through the resonant tank. The parallel converter also operates over the resonant frequency due to the ZVS conditions.

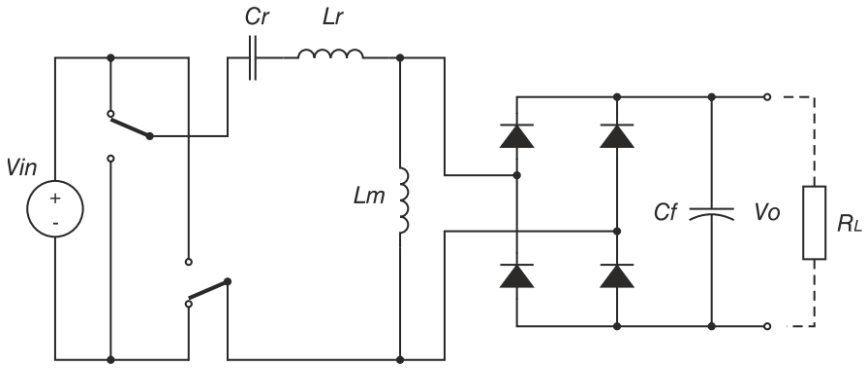

Figure 4. LLC resonant converter topology

Besides the two-part resonant tanks, there are almost 40 possibilities of the three-part resonant tanks. The most popular member of the three-part tanks is the LLC resonant converter. The resonant tank consists of inductors L_r and L_m and capacitor C_r (see Figure 4). The load is connected in parallel to inductor L_m. The LLC resonant converter solves all the drawbacks mentioned above. During no-load

conditions, the output voltage can still be controlled by a voltage drop over inductor L_m. At the resonant frequency, the current is limited by inductor L_m. Therefore, the current circulating through the resonant circuit can be kept at an acceptable level. Another advantage of the LLC resonant converter is that it can operate under the ZVS condition over the whole load range. The behavior of the LLC resonant converter is discussed in more detail in Section 2.2, "LLC converter description". The key features of all mentioned resonant converters are listed in Table 1.

Table 1. Resonant converters comparison

—	SRC	PRC	LLC
ZVS operation	Above f_r only	Above f_r only	Yes
Operation without load	No	Yes, but with high losses	Yes
Operation at f_r	No (close to f_r)	No (close to f_r)	Yes
Operation at wide input range	High losses	High losses	Yes

2.2. LLC converter description

The LLC resonant topology has many advantages when compared to the other resonant topologies described in Section 2.1, "Resonant converter topologies". The majority of switched mode power supplies use a transformer to provide galvanic isolation or input/output voltage adjustment. Using a transformer in the LLC resonant topology brings another advantage (see Figure 5).

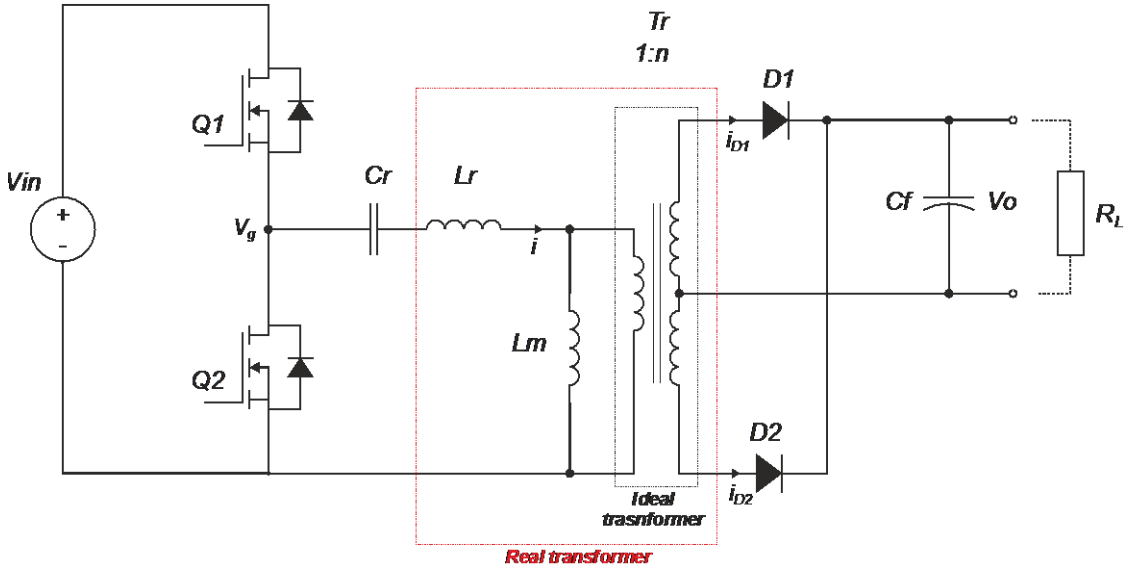

Figure 5. LLC resonant converter with transformer

The real transformer can be defined as an ideal transformer with the magnetizing and leakage inductances (L_m, L_r). These inductances can be used as elements of the resonant circuit. This eliminates the need for additional inductances for the resonant circuit of the LLC resonant converter. There are also techniques to integrate a parasitic capacitor into a transformer. Therefore, the components necessary for a resonant circuit are built into the transformer. The only drawback of this approach is the limited variability of the components' values.

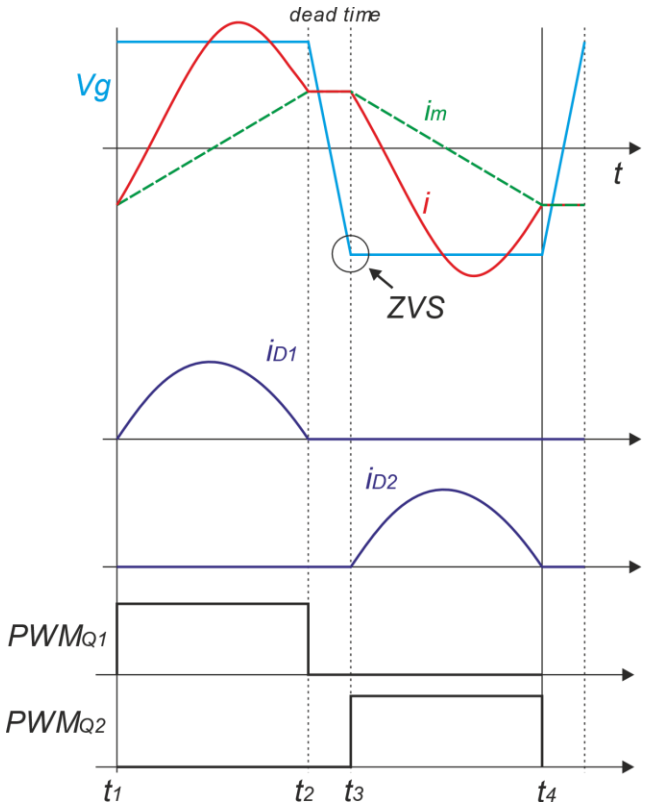

Figure 6. LLC resonant converter waveforms at resonant frequency

The typical waveforms of the LLC resonant converter are shown in Figure 6. The square-wave voltage V_g is generated by a half-bridge consisting of transistors Q1 and Q2. The transistors are switched in a complementary manner with a 50 % duty cycle. The magnetizing current starts to increase from its minimal value together with the load current. If the LLC converter operates at a resonant frequency, the load current achieves a zero value at the end of the Q1 PWM pulse. At this moment, the magnetizing current also reaches its maximum. After the transistor Q1 is switched off, the magnetizing current continues to flow through the internal output capacitance of transistor Q1. To ensure proper ZVS operation, the dead-time has to be long enough to allow to completely charge the internal MOSFET capacitance of transistor Q1 to the DC-bus voltage. At the end of the deadtime, the drain-source voltage of transistor Q2 equals zero. Therefore, transistor Q2 can be switched on during the ZVS condition. The second half period is similar to the first half period. After transistor Q2 switches on, the magnetizing current starts to fall. The load current flows in the opposite direction. At the end of the period, the load current reaches zero and the magnetizing current reaches its minimal value. The consequential dead-time ensures the ZVS condition for transistor Q1. After the drain to the source voltage of transistor Q1 is zero, the operation can start from the beginning. Figure 6 shows the LLC converter operation at a resonant frequency. At this frequency, the load current on both the primary and secondary parts reaches a zero value, so the switching losses are minimized as much as possible.

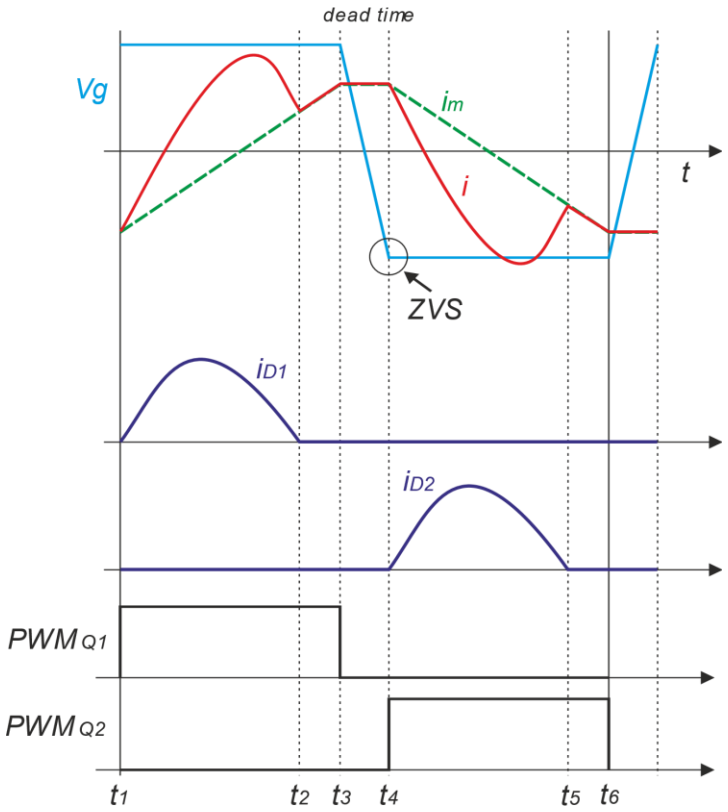

Figure 7. LLC resonant converter waveform below resonant frequency

The operation under the resonant frequency (Figure 7) is similar to the operation at the resonant frequency. In addition, there is an interval (t_2-t_3) where the load current is zero. In the last case (operation above the resonant frequency), the load current is forced to fall to zero at the end of the half-period. This causes increased reverse recovery losses (see Figure 8).

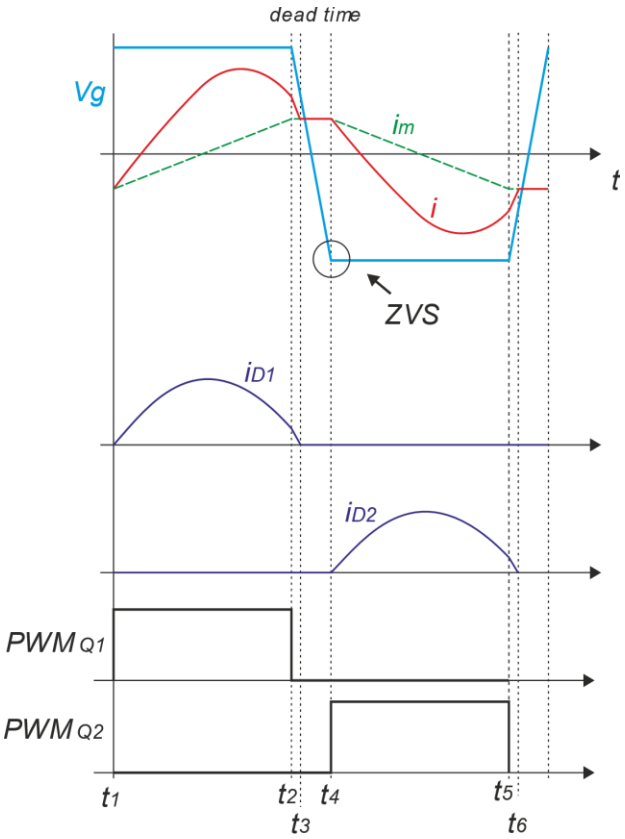

Figure 8. LLC resonant converter waveform above resonant frequency

To analyze the LLC resonant converter behavior, you can re-draw the circuit in Figure 5 to the equivalent circuit in Figure 9.

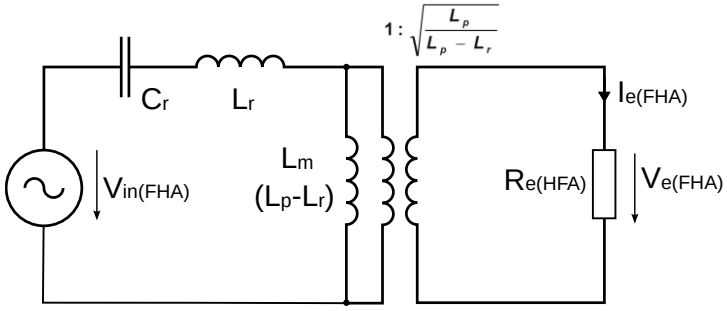

Figure 9. Equivalent circuit of LLC resonant converter

Assuming that the power is transferred mainly by a fundamental component of voltages and currents, the First Harmonic Approximation (FHA) approach can be used to analyze the LLC resonant converter behavior. Thus, the output quantities can be transformed from V_O, I_O, and R_O to $V_{e(FHA)}$, $I_{e(FHA)}$, and $R_{e(FHA)}$ using these equations:

$$V_{e(FHA)} = \frac{4V_O}{\pi} sin(\omega t) \quad \textit{Eq. 1}$$

$$I_{e(FHA)} = \frac{\pi I_O}{2\pi} sin(\omega t) \quad \textit{Eq. 2}$$

Eq. 3

$$R_{e(FHA)} = \frac{8V_O}{\pi^2 I_O} = \frac{8}{\pi^2} R_O$$

Considering the transformer ratio $M_{Tr} = \sqrt{\frac{L_p}{L_p - L_r}}$, the equivalent load resistant seen on the primary side can be expressed as:

Eq. 4

$$R_{e(FHA)} = \frac{8n^2 R_O}{\pi^2 M_{Tr}^2}$$

The output transfer function of the LLC resonant converter is expressed as:

Eq. 5

$$M = \frac{2nV_O}{V_{in}} = \left| \frac{\left(\frac{\omega}{\omega_0}\right)^2 (m-1) M_{Tr}}{\left(\frac{\omega^2}{\omega_p^2} - 1\right) + j\left(\frac{\omega}{\omega_0}\right)\left(\frac{\omega^2}{\omega_0^2} - 1\right)(m-1)Q_e} \right|$$

Where:

Eq. 6

$$Q_e = \sqrt{\frac{L_r}{C_r}} \frac{1}{R_{e(FHA)}}, \omega_0 = \frac{1}{\sqrt{L_r C_r}}, \omega_p = \frac{1}{\sqrt{L_p C_r}}$$

Figure 10 shows the output transfer function (gain) for different values of quality factor Q_e. The gain of the LLC resonant converter changes with the load. For the resonant frequency, the gain is constant, regardless of the load variation defined by the M_{Tr} ratio.

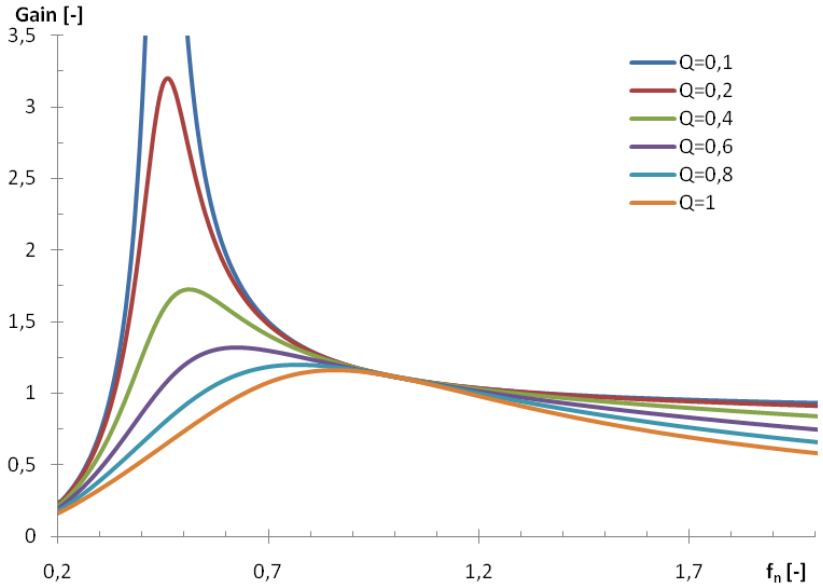

Figure 10. Output transfer function (gain) for LLC resonant converter

3. Hardware description

3.1. Main board

Here is the summary of the main board's key features:

- Input voltage: 330-390 V DC
- Output power: up to 250 W
- Output voltage: 12 V
- Output current: up to 21 A
- Switching frequency: 75-300 kHz
- GaN low-loss switches
- Passive cooling
- Digitally-controlled synchronous rectifier
- Reinforced galvanic isolation
- Over-current and over-voltage protection
- SM-bus interface and serial interface
- Analog sensing (output voltage, output current, resonant circuit current)
- Supports multiple MCU cards
- Load switch for step-response tuning

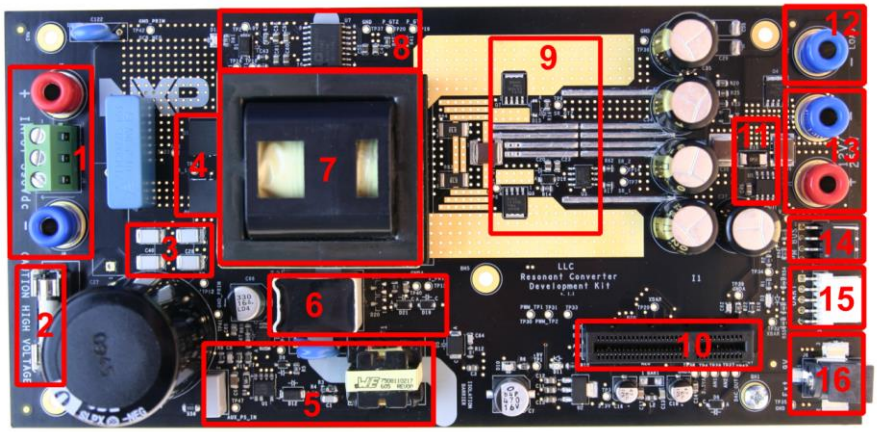

Figure 11. Main board description

In the above figure:

1. DC power input
2. Fuse
3. Resonant capacitors
4. Primary GaN switches
5. AUX power supply
6. Primary current-measurement circuit
7. Resonant transformer
8. Isolated gate drivers
9. Synchronous rectifier
10. Controller card interface
11. Output current-measurement circuit
12. Load switch
13. DC output
14. PM-bus
15. Serial interface

To connect the input voltage, use input terminals J4 or J8 and J9 on the primary side (number 1 in Figure 11). Connect a load to terminals J1 and J3 or J1 and J2 if the step response is evaluated (number 12 and 13 in Figure 11).

3.1.1. Electrical characteristics

The electrical characteristics in Table 2 apply to operation at 25 °C.

Table 2. Electrical characteristics

Characteristic	Symbol	Min	Typ	Max	Units
DC input voltage	V_{IN}	330	390	410	V
DC output voltage	V_{OUT}	11.9	12	12.1	V
Output current permanent	I_{OUT}	—	—	21	A
Output current peak (t_p < 1 s)	I_{OP}	—	—	30	A
Quiescent current	I_{CC}	—	4	7	mA
Minimum logic 1 input voltage	V_{IH}	2.0	—	—	V
Maximum logic 0 input voltage	V_{IL}	—	—	0.8	V
Analog input/output range	V_{ANA}	0	—	3.3	V
Primary current measurement sensitivity	I_{PRIM}	—	500	—	mV/A
Output current measurement offset	I_{OOF}	—	1.12	—	A
Output current measurement sensitivity	I_{OUT}	—	50	—	mV/A
Voltage measurement sensitivity	V_{OUT}	—	235.7	—	mV/V
Switching frequency	f_{SW}	75	—	300	kHz

3.1.2. Resonant circuit

The resonant circuit on this board consists of resonant capacitors C26, C28, C40, and C41 and the integrated leakage inductance of transformer T5. The leakage inductance is intentionally increased and the inductance value is standardized to get rid of the external resonant inductance. A ceramic capacitor with the C0G dielectric is used due to good thermal stability, low ESR, and very small footprint.

Transformer T3 is a part of the current-monitoring circuit which senses the current amplitude on the primary side. Although the T3 transformer is a part of the resonant circuit, its primary inductance is minimal. Therefore, the impact on the resonant circuit is also minimized.

The resonant circuit uses the split resonant capacitor topology. The resonant circuit frequency is computed as follows:

Eq. 7

$$f_R = \frac{1}{2\pi\sqrt{L_R . C_R}}$$

Considering the inductance of the transformer used L_R = 105 µH and the resonant capacitor C_R = 4 * 8,2 nF, the value of the resonant frequency is:

Eq. 8

$$f_R = \frac{1}{2\pi\sqrt{105.10^{-6} + 32,8.10^{-9}}} = 85\ kHz$$

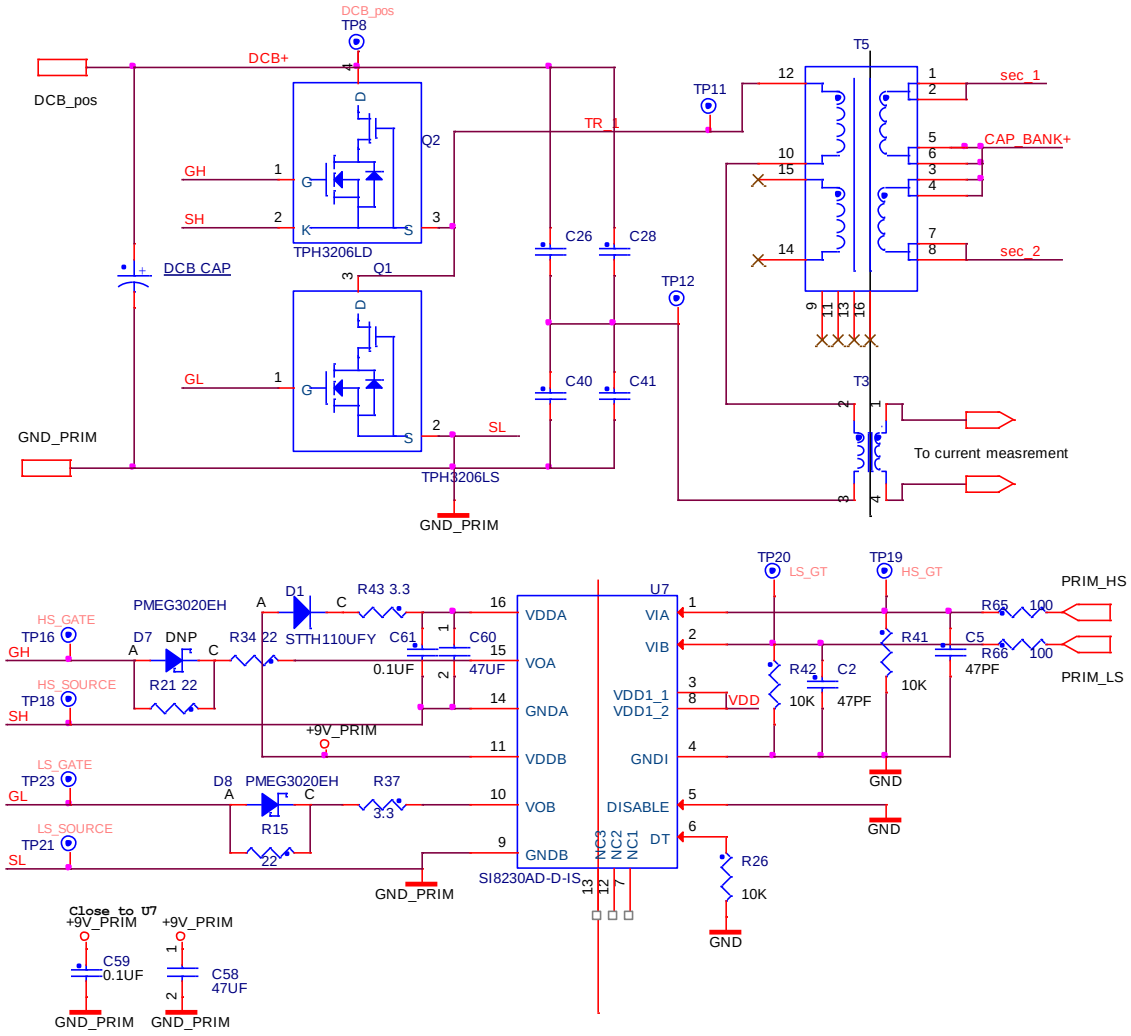

Figure 12. Resonant circuit detail

The GaN's pre-driver provides two isolated channels for Q2 and Q1 with dead-time insertion. Because the dead-time insertion is very critical for the GaN's half-bridge, keep in mind that the software is responsible for proper and reliable deadtime insertion to keep the converter in the soft switching mode.

3.1.3. Output voltage sensing

The output voltage sensing circuit consists of a low-impedance voltage divider in combination with an RC filter. The low-impedance divider reduces noise and improves ADC sampling. The voltage division ratio *r* is selected to scale the measured voltage to the MCU analog input range. The maximum measured voltage is V_{MAX} = 14 V and the MCU analog reference is V_{MCU} = 3.3 V. The signal for the voltage measurement is available at PTB0/ADCB_CH2.

$$r = \frac{V_{MAX}}{V_{MCU}} = \frac{14}{3.3} = 4.24 \qquad \textit{Eq. 9}$$

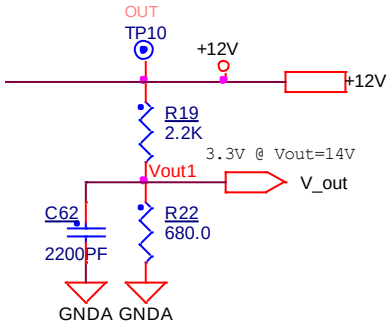

Figure 13. Voltage measurement circuit

3.1.4. Resonant current sensing

The main board also contains a circuit to monitor the current flowing through the resonant circuit on the primary side. The analog value of the primary current can be used for the inner current-control loop as well as the over-current protection function. The current-measurement circuit is isolated using a current-sense transformer. The maximum current that can be measured by this circuit is I_{PMAX} = 6.6 A, which corresponds to the output voltage V_{IPMAX} = 3.3 V. This signal is available at PTE29/ADCA_CH4.

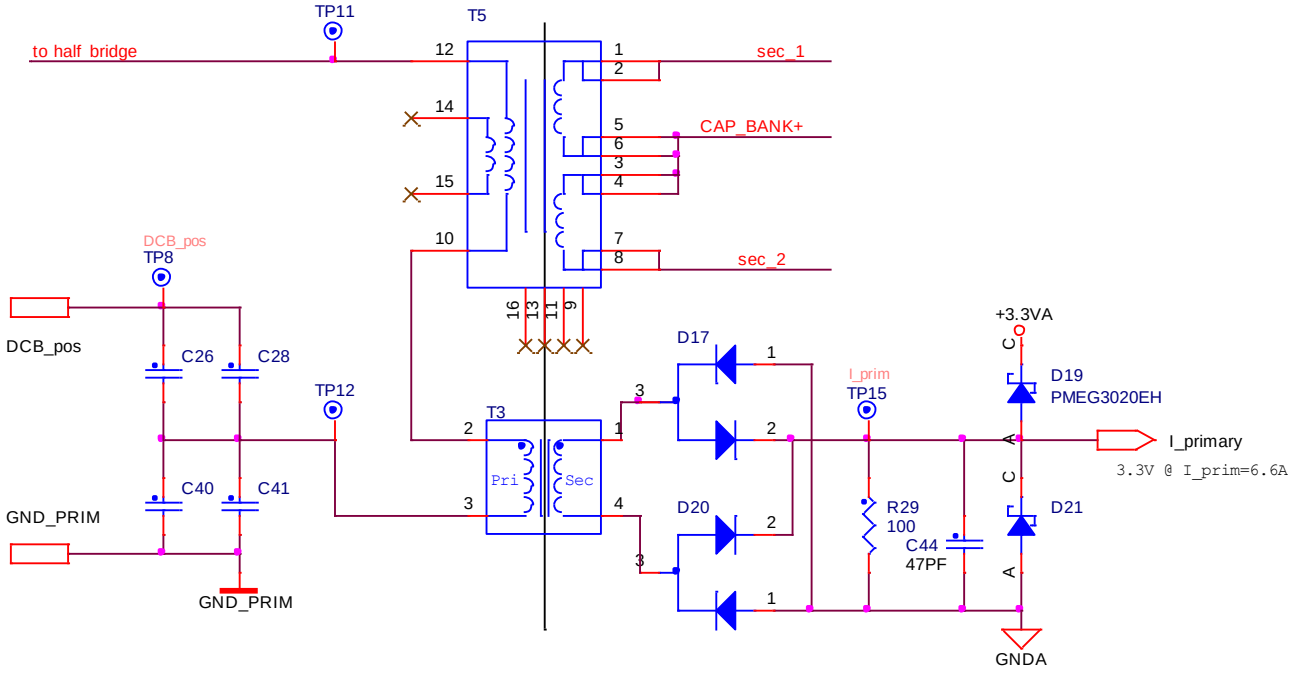

Figure 14. Resonant current-measurement circuit

3.1.5. Output current sensing

To ensure the output short circuit protection and output current monitoring, the main board is equipped with the output current-monitoring circuit. Because high current flows through the output, the circuit consists of a 0.5-mΩ current-sensing resistor and a high-side current-sensing amplifier with voltage gain a_V = 100. In this configuration, I_{SMAX} = 66 A corresponds to the output voltage of 3.3 V. This signal is available at ADCA_CH6D.

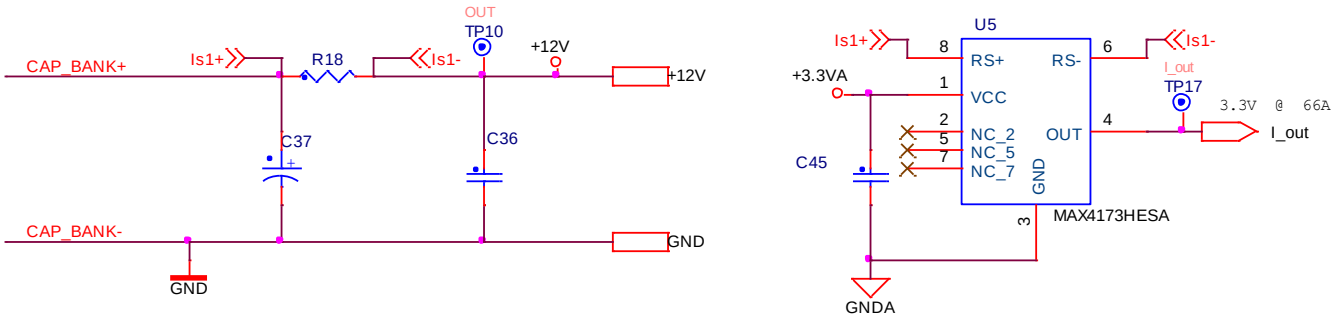

Figure 15. Output current-measurement circuit

3.1.6. Synchronous rectifier

When compared to a standard diode rectifier, the digitally-controlled synchronous rectifier significantly improves the converter efficiency. Because the output current flowing through the secondary side is higher than 20 A, the power loses can be reduced more than 15 times when compared to a standard diode rectifier. To minimize the silicon components' count, a full-wave rectifier and a transformer with a center tap are selected. The center tap of the transformer is connected to the positive node of the output DC-bus. In this configuration, both MOSFETs are N-type and they don't require a more complicated pre-driver with a bootstrap circuit.

The whole rectifier is fully controlled by the MCU which calculates the gate signals according to the converter operation mode. Therefore, the synchronous rectifier doesn't require any additional circuits to monitor the rectifier current direction or the current amplitude. This method significantly reduces the component count.

To demonstrate the high efficiency of this rectifier type, the board doesn't need an additional heat sink or an active cooling system. Even at a maximum output power, the PCB traces are sufficient to dissipate the MOSFET power losses.

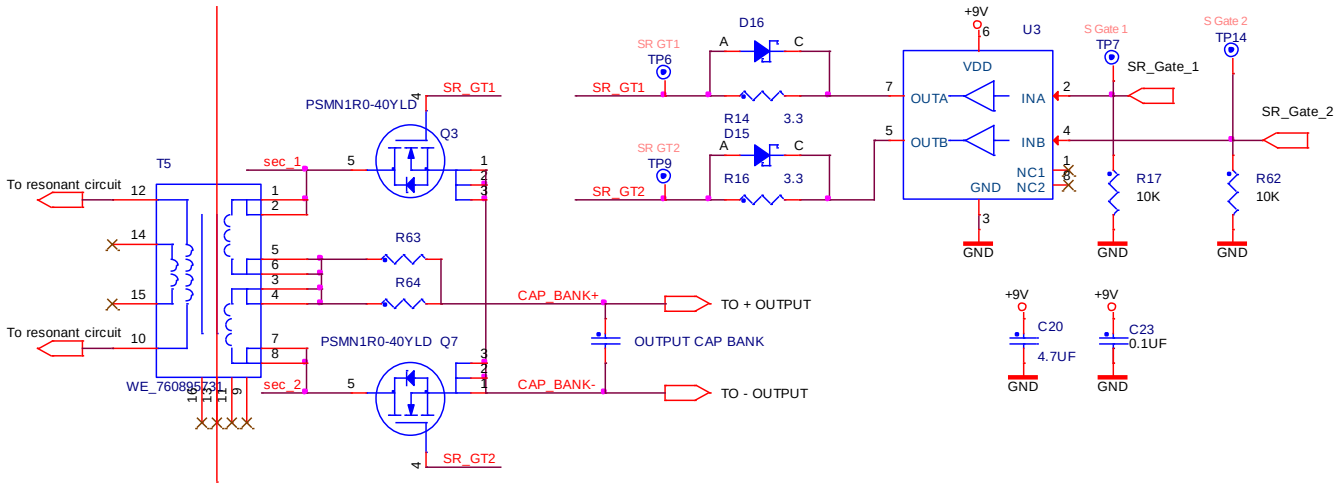

Figure 16. Synchronous rectifier

The zero resistors R72 and R73 can be replaced by a shunt resistor or a current probe for current evaluation through a synchronous rectifier. For more information about the SR control, see Section 4.5, "Synchronous rectifier control".

3.1.7. Auxiliary power supply

A small flyback power supply controlled by the TEA1721 device is used to power the main controller and MOSFET pre-drivers. TEA1721 is a small and low-cost Switched Mode Power Supply (SMPS) controller IC for low-power applications (up to 5 W) and operates directly from the rectified universal mains input. The device includes a high-voltage power switch (700 V) and is optimized for flyback converter topologies to provide high efficiency over the entire load range with very low power consumption in the no-load condition. It provides a circuit for starting up directly from the rectified mains voltage without any external bleeder circuits. The Burst mode frequency of 430 Hz enables the no-load power consumption to be below 10 mW at the high mains input.

The auxiliary power supply provides two supply voltages with a level of +9 V. One branch provides the voltage for the primary side and the second one for the secondary side. The voltage for the MCU is derived by a voltage regulator from the secondary-side +9 V branch.

When a USB cable is connected to the controller card, the voltage source from the controller card can affect the MCU voltage reference V_{REFH}. In this case, the output precision of the voltage measurement can be affected.

3.1.8. Fault protection

Both the secondary output and primary resonant currents can be measured by the ADC. In addition, these signals are also connected to the internal MCU analog comparators which can act as hardware protection in case of proper software configuration. For the secondary side, current protection CMP0 IN4 or CMP2 IN3 can be used. For the primary side, current protection CMP1 IN5 or CMP0 IN5 can be used. If the comparators' output signals are internally routed to the PWM fault signals, the PWM outputs are immediately turned off when an over-current condition occurs.

The board input is also protected by melting fuse F1. Always replace this fuse with the same value and the same characteristic as its default value. The default value is F1.6 A/250 V.

3.1.9. Load switch

To evaluate the converter step response, the main board is equipped with an additional software-controlled switch which can connect and disconnect the output load. In this case, the load can be connected between terminals J1 and J2. This switch can be controlled by the PTB16 port.

3.1.10. Test points and LEDs description

Table 3. Test points and LED description

Designator	Name	Description
TP 1	+9V	MOSFET driver supply at the secondary side
TP 2	+9V_PRIM	MOSFET driver supply at the primary side
TP 3	+3.3V	MCU power supply
TP 4	+3.3VA	Analog circuits' power supply
TP 6	SR_GT1	Q3 gate signal
TP 7	SR_1	Q3 control signal
TP 8	DCB_POS	DCB voltage at the primary side
TP 9	SR_GT2	Q7 gate signal
TP 10	V_OUT	Converter output voltage
TP 11	TR1	Voltage in the middle of the primary half-bridge
TP 12	TR2	Voltage at the resonant capacitors
TP 13	DAC_OUT	Test point for the DAC
TP 14	SR_2	Q7 control signal
TP 15	I_PRIM	Primary current in the resonant circuit
TP 16	GH	Q2 gate signal
TP 17	I_OUT	Converter output current
TP 18	SH	Q2 source signal
TP 19	HS_GT	Q2 control signal
TP 20	LS_GT	Q1 control signal
TP 21	SL	Q1 source signal
TP 22	GND_PRIM	GND at the primary side
TP 23	GL	Q1 gate signal
TP 24	GND_PRIM	GND at the primary side
TP 25	AUX_PS_IN	AUX flyback supply voltage
TP 26	AUX_PS_GND	GND at the primary side
TP 27	AN2	Analog test point n.2
TP 28	AN1	Analog test point n.1
TP 29	XBAR_TP1	XBAR test point n.1
TP 30	PWM_TP1	PWM test point n.1
TP 31	PWM_TP2	PWM test point n.2
TP 32	XBAR_TP2	XBAR test point n.2
TP 33	TP33	General test point
TP 34	TP34	General test point
TP 35	GND	Power ground
TP 36	GND	Power ground
TP 37	GND	Power ground

Table 3. Test points and LED description

Designator		Name	Description
TP	38	GNDA	Analog signal ground
TP	39	GNDA	Analog signal ground
TP	40	GNDA	Analog signal ground
D	3	User LED 1	User LED Red
D	4	User LED 2	User LED Green
D	10	+9V	Secondary +9 V power indicator (LED Yellow)
D	11	+3.3V	Secondary +3.3 V power indicator (LED Green)
D	13	+9V_PRIM	Primary +9 V power indicator (LED Yellow)

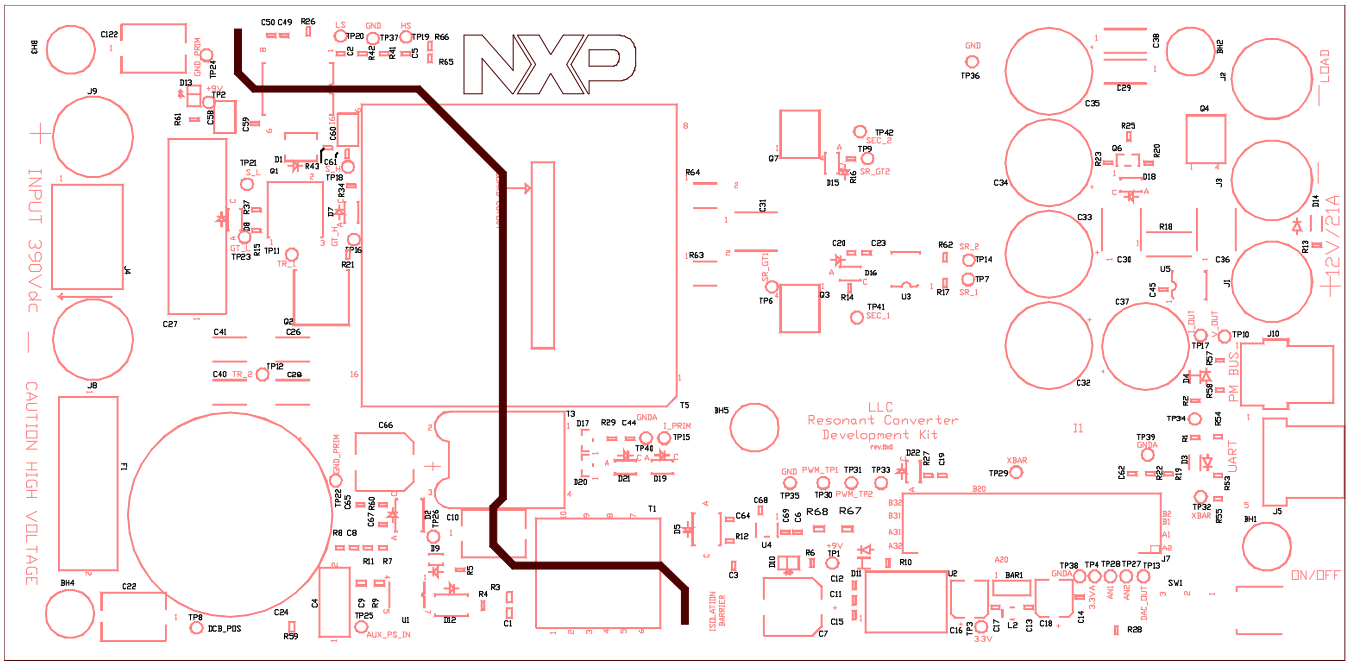

Figure 17. Test points' location

3.2. Bill of materials

Table 4. Bill of materials

Item	Quantity	ASSY_OPT	Reference	Value	Mfg part number
1	1	—	BAR1	ShortingBar1206	—
2	5	—	BH1,BH2,BH3,BH4,BH5	MOUNTING HOLE	—
3	1	—	C1	220 pF	C3216C0G2J221J060AA
4	2	—	C3,C65	0.1 µF	C0805C104K5RAC
5	1	—	C4	0.01 µF	BFC233920103
6	1	—	C7	470 µf	—
7	1	—	C8	10 pF	C0805C100J5GAC
8	1	—	C9	2.2 µF	C1206X7R500-225KSNE
9	3	—	C10,C22,C122	2200 pF	CD90ZU2GA222MYNKA

Table 4. Bill of materials

Item	Quantity	ASSY_OPT	Reference	Value	Mfg part number
10	9	—	C11,C12,C14,C15,C23,C45,C49,C59,C61	0.1 μF	GRM21BR71E104KA01L
11	2	—	C13,C17	0.01 μF	C0805X7R500-103KNE
12	2	—	C16,C18	47 μF	EEE0JA470SR
13	4	—	C20,C50,C58,C60	4.7 μF	0805X475K160CT
14	1	—	C24	330 μF	ESMQ451VSN331MR40S
15	4	—	C26,C28,C40,C41	8200 pF	C4532COG2J822J
16	1	—	C27	0.1 μF	B32653A0104J000
17	2	DNP	C29,C38	1000 pF	GA352QR7GF102KW01L
18	3	—	C30,C31,C36	15 μF	C5750X7S2A156M
19	5	—	C32,C33,C34,C35,C37	1000 μF	EEU-FM1E102
20	1	—	C43	22	RC0805FR-0722RL
21	1	DNP	C44	47 pF	C0805C0G500-470JNE
22	3	—	C62,C64,C67	2200 pF	MCCE222J2NOTF
23	1	—	C66	330 μF	EMZJ250ADA331MHA0G
24	1	—	D1	ES1J-LTP	ES1J-LTP
25	2	—	D2,D5	MBRS1100T3G	MBRS1100T3G
26	1	—	D3	RED	HSMH-C170
27	2	—	D4,D11	HSMG-C170	HSMG-C170
28	5	—	D6,D15,D16,D19,D21	PMEG3020EH	PMEG3020EH,115
29	1	—	D9	BAS316	BAS316,115
30	2	—	D10,D13	HSMY-C170	HSMY-C170
31	1	—	D12	MRA4007T3G	MRA4007T3G
32	2	—	D17,D20	BAT54S	BAT54S
33	1	—	F1	Fuse Holder	HTC-15M
34	2	—	J1,J9	A-2.109-R	A-2.109-R
35	3	—	J2,J3,J8	A-2.109	A-2.109-BL
36	1	—	J4	MC000049	MC000049
37	1	—	J5	HDR 1X5 RA	22-05-7058
38	1	—	J6	CON PWR 3	RASM722PX
39	1	—	J7	CONN PCI EXP 64	8-1612163-2
40	1	—	J10	HDR_1x4_RA	22053041
41	1	—	L2	1 μH	MLZ2012A1R0PT
42	1	—	Q2	TPH3206LD	TPH3206LD
43	3	—	Q3,Q4,Q7	PSMN1R0-40YLD	PSMN1R0-40YLDX
44	1	—	Q5	TPH3206LS	TPH3206LS
45	1	—	Q6	BC817-40LT1G	BC817-40LT1G
46	3	—	R1,R2,R10	330	CRCW0805330RJNEA
47	1	—	R3	100 k	RV1206JR-07100KL

Table 4. Bill of materials

Item	Quantity	ASSY_OPT	Reference	Value	Mfg part number
48	1	—	R4	470	CR0805-JW-471ELF
49	1	—	R5	10	RK73B2ATTD100J
50	2	—	R6,R61	2.67 k	ERJ6ENF2671V
51	1	—	R7	21 k	CR0805FX2102ELF
52	3	—	R8,R20,R23	4.7 k	CR0805-FX-4701ELF
53	1	—	R9	1.5	CRCW12061R50FKEA
54	1	DNP	R11	560 k	CR0805-FX-5603ELF
55	2	—	R12,R60	100	RC73L2D101JTF
56	2	—	R14,R16	3.3	CR0805-FX-3R30ELF
57	8	—	R17,R25,R41,R42,R53,R54,R55,R62	10 k	CR0805-8W-103JT
58	1	—	R18	TLR3A20DR0005FTDG	TLR3A20DR0005FTDG
59	1	—	R19	2.2 k	ERJ-6ENF2201V
60	1	—	R22	680	RC0805FR-07680RL
61	1	—	R29	100	CR0805-8W-1000FT
62	2	—	R34,R37	47	RC0805FR-0747RL
63	2	—	R57,R58	1.1 k	MCPWR05FTEW1101
64	1	—	R59	0	CRCW12060000Z0EA
65	2	—	R63,R64	WSL251200000ZEA9	WSL251200000ZEA9
67	1	—	T1	WE_7508110217	—
68	1	—	T3	CS4200V-01L	—
69	1	—	T5	WE_760895731	—
70	1	—	U1	TEA1721AT	TEA1721AT/N1,118
71	1	—	U2	NCP1117ST33T3G	NCP1117ST33T3G
72	1	—	U3	FAN3214T	FAN3214TMX
73	1	—	U5	MAX4173FESA	MAX4173FESA+
74	1	—	U7	ADUM4223ARWZ	ADUM4223ARWZ

3.3. HVP-KV46F150M controller card

The HVP-KV46F150M controller card is a part of the HVP and compatible with the HVP-LLC board.

This is the summary of the controller board's key features:

- KV46F256VLL15 MCU
- SWD isolation of up to 5 kV
- Programmable OpenSDA debug interface with multiple applications available, including:
  - Mass-storage device flash-programming interface
  - Debug interface for run-control debugging and compatibility with IDE tools
  - Data-logging application

- Compatible with CodeWarrior 10.x, IAR Embedded Workbench®, and Keil® IDEs
- Design optimized for low noise
- On-board isolated power supply providing safe debugging
- Controller card supporting standalone operation

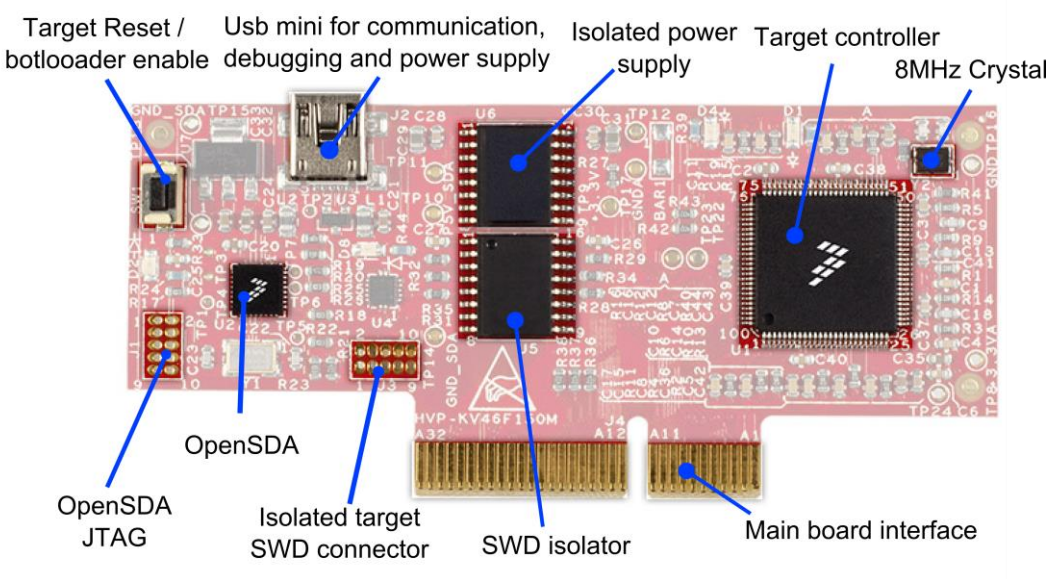

Figure 18. HVP-KV46F150M controller card

For more information, see *HVP-KV46F150M User's Guide* (document HVPKV46F150MUG).

3.3.1. MCU signal description

The interface between the main board and the controller card is done via a 64-pin PCI express connector. Because this interface is used on several development boards, not all signals are used or the functionality of pins can be different when compared to other boards. Table 5 describes the signal functionality of the HVP-KV46F150M controller card in combination with the HVP-LLC board. The functionality and signal routing for other cards may vary.

Table 5. Signal and pin assignment

—	Signal name	Port at HVP-KV46F150M	Pin at PCI EXP 64	Pin number	Functionality
Power supply	+3.3VA	VDDA, VREFH	A1	22,23	Analog circuits supply voltage
	+3.3V	VDD	B12	8,30,40,48,61,75, 89	MCU and digital part supply voltage
	GND	VSS	A13/A24/B13/ B32	9,29,41,49,60,74, 88	Digital ground
	GNDA	VSSA, VREFL	A11/B11	25,24	Analog ground
PWM signals	HS_GT	PTD1	A15	94	Control signal for the top GaN Switch Q2
	LS_GT	PTD0	A14	93	Control signal for the bottom GaN Switch Q1
	SR_Gate_1	PTD2	A16	95	Control signal for SR MOSFET Q3
	SR_Gate_2	PTD3	A17	96	Control signal for SR MOSFET Q7
Analog signals	V_out	PTB0/ADCB_CH2	A4	53	Output voltage
	I_out	ADCA_CH6D/CMP0_IN4/CMP2_IN3	B6	28	Output current
	I_prim	PTE29/ADCA_CH4/CMP1_IN5/CMP0_IN5	B3	26	Primary resonant current
General-purpose signals	TP27	PTE16/ADCA_CH0	A7	10	User-programmable test point for ADC
	TP28	PTE19/ADCB_CH1	B9	13	User-programmable test point for ADC
	TP29	PTE0/XBAROUT10/XBARIN11	B16	1	User-programmable test point for XBAR
	TP30	PTC1/FTM0_CH0/FLEXPWM_A3	A22	71	User-programmable test point for PWM
	TP31	PTC2/FTM0_CH1/FLEXPWM_B3	A23	72	User-programmable test point for PWM
	TP32	PTE1/XBAROUT11/XBARIN7	A25	2	User-programmable test point for XBAR
	TP33	PTB11	A29	59	User-programmable test point
	TP34	PTB10	A30	58	User-programmable test point
	TP43	PTB3	A9	56	User-programmable test point
	Load_SW	PTB16	B14	62	Load switch control signal
	user_led_1	PTB19	B20	65	User LED 1 RED (D3)
	user_led_2	PTB10	A30	58	User LED 2 GREEN (D4)
	I2C_SCL	PTC6/I2C0_SCL	A28/B21	78	I^2C interface
	I2C_SDA	PTC7/I2C0_SDA	A27/B22	79	I^2C interface
	TxD_EXT	PTD7/UART0_TX	B26	100	UART interface
	RxD_EXT	PTD6/UART0_RX	B27	99	UART interface
	PWR_ON	PTC13	B28	85	PWR Ok signal + power switch
	GPIO_SW	PTE1	A25	—	Input for the power switch

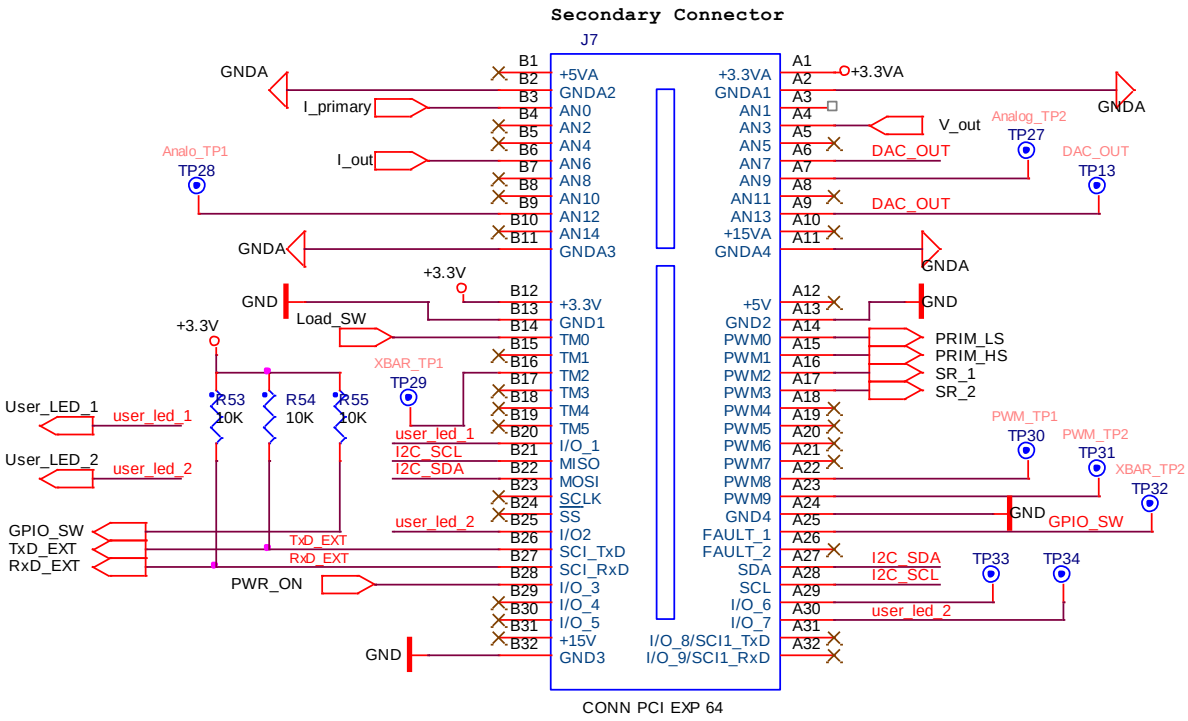

Figure 19. Signal arrangement of PCI EXP connector

3.4. Hardware concept

The hardware consists of a controller card and the main board. The main board is divided into two parts, isolated with reinforced isolation—the primary side and the secondary side. The primary side is designed to be supplied from a DC voltage supply or an external PFC stage and incorporates the GaN transistors' half-bridge, the resonant circuit, the AUX power supply, and the GaN driver circuit.

The secondary side incorporates the secondary side of the LLC resonant converter, the synchronous rectifier, the analog sensing circuitry, the communication between the host PC and the PM Bus, the drivers, and the MCU controller board.

The AUX power supply is powered directly from the DC-bus. It generates the desired voltages for both the primary and secondary sides and uses the flyback topology.

The illustration of the system architecture is shown in Figure 20.

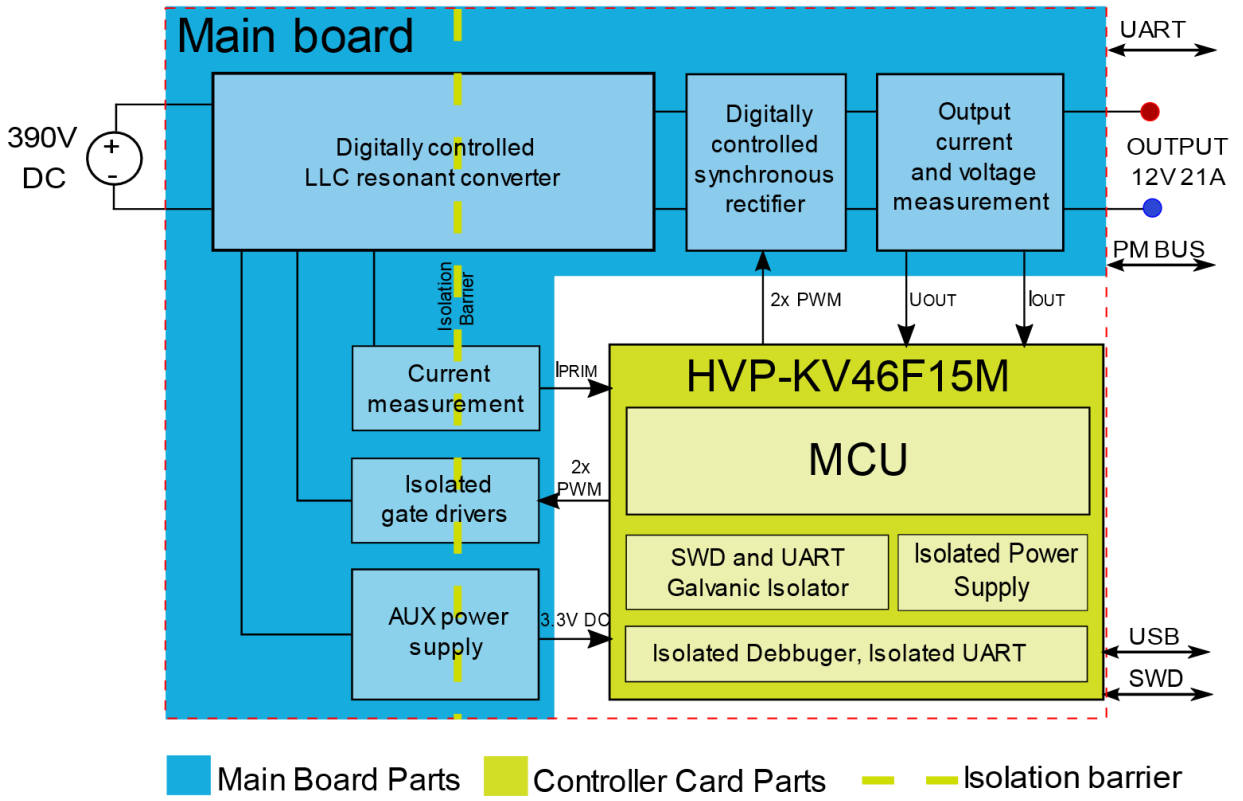

Figure 20. HVP-LLC converter block diagram

The control of the LLC resonant converter is executed by the KV46 MCU located on the secondary side of the switched-mode power supply. The MCU measures the output voltage and current. The ADCA_CH6D ADC input is also shared with the CMP0 built-in analog comparator whose output is internally connected to the fault input of the eFlexPWM module. Thus, the output current is compared with the maximum allowed current. In case of an overload condition, the LLC resonant converter is switched off and restarted after a pre-defined period of time. The difference between the output voltage and the required voltage is input into the PI controller. The voltage mode control is implemented using the PI controller. The output of the PI controller corresponds to the switching frequency of the LLC resonant converter. The PWM signals are generated by the SM0 and SM1 submodules of the eFlexPWM module based on the output of the PI controller. The signal connections between the LLC resonant converter circuit and the MCU are shown in Figure 21.

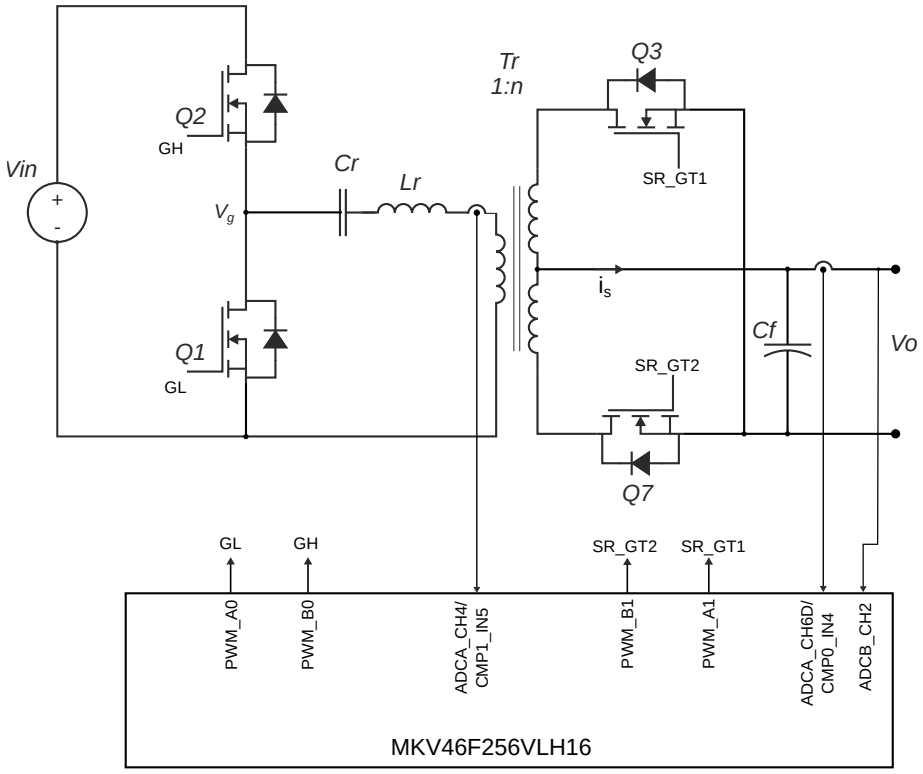

Figure 21. LLC resonant converter control diagram

3.5. LLC resonant converter hardware design

This section describes the design procedure for the LLC resonant converter. The inputs used for the calculations are as follows:

3.5.1. LLC resonant converter specification

- Output power (P_O): 250 W
- Output voltage (V_O): 12 V
- Diode voltage drop (V_F): 0.5 V
- Minimum DC-bus Voltage (V_{min}): 310 V
- Maximum DC-bus Voltage (V_{max}): 390 V
- Resonant switching frequency (f_O): 85 kHz
- Lp/Lr ratio (m): 4.8

3.5.2. Resonant network design

Most of the parameters are given by the power supply requirements. The first design parameter to select is the L_p/L_r ratio (*m*). According to the LLC resonant converter behavior analysis, the recommended value of *m* is in the range from 4 to 10. If using the leakage inductance of the transformer as a resonant inductance, there is a limited possibility of *m* selection because the L_p/L_r ratio is defined by the

mechanical construction of the transformer. Because a standard transformer was chosen, the L_p/L_r ratio is given by the transformer manufacturer. The required gain of the LLC resonant converter is calculated next. When *m* is defined, the minimum gain of the converter at a resonant frequency is expressed as:

Eq. 10

$$M_{min} = \sqrt{\frac{m}{m-1}} = \sqrt{\frac{4.8}{4.8-1}} = 1.124$$

For the minimum input voltage V_{min}, the maximum gain is expressed as:

Eq. 11

$$M_{max} = \frac{V_{max}}{V_{min}} M_{min} = \frac{390}{310} 1.124 = 1.414$$

Knowing the minimum and maximum gains, the transformer turns ratio can be calculated.

Eq. 12

$$n = \frac{N_p}{N_s} = \frac{V_{max}}{2(V_O + V_F)} M_{min} = \frac{390}{2 \cdot (12 + 0.5)} 1.124 = 17.5$$

The next step is to calculate the equivalent load resistance, which is needed for the resonant network calculation. It can be obtained as:

Eq. 13

$$R_{e(FHA)} = \frac{8n^2 V_O^2}{\pi^2 P_O} = \frac{8 \cdot 17.5^2 \cdot 12^2}{\pi^2 \cdot 250^2} = 144\,\Omega$$

The resonant circuit consists of resonant capacitor C_r and resonant inductor L_r. The resonant capacitor can be calculated as:

Eq. 14

$$C_r = \frac{1}{2\pi Q_e f_0 R_{e(FHA)}}$$

Quality factor Q_e depends also on C_r. Therefore, the behavior of the resonant converter must be analyzed for different values of Q_e. Using Eq. 6 and changing the quality factor Q_e value from 0.1 to 1 results in different gain characteristics of the LLC resonant converter. Considering the maximum gain only, the peak gain versus Qe graph can be drawn, as shown in Figure 18. Because the maximum required gain M_{max} is already known, the Q_e value can be obtained from the graph. To ensure safe LLC converter operation even in the worst conditions, the maximum gain must be increased by 10-20 %. Then, the maximum gain is equal to 1.7, considering a margin of 20 %. Quality factor Q_e can be read from the graph in Figure 22, which gives $Q_e = 0.395$.

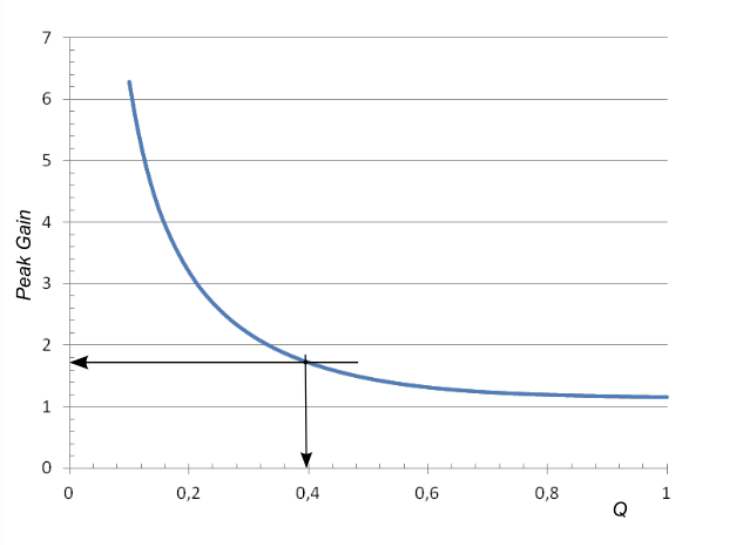

Figure 22. Peak gain versus Q

Resonant capacitor C_r can be calculated as:

$$C_r = \frac{1}{2\pi \cdot 0.395 \cdot 85 \cdot 10^3 \cdot 144} = 33\ nF \quad \textit{Eq. 15}$$

The second component of the resonant circuit is resonant inductor L_r. Its value can be obtained as:

$$L_r = \frac{1}{(2\pi f_0)^2 C_r} = \frac{1}{(2\pi \cdot 85 \cdot 10^3)^2 \cdot 33 \cdot 10^{-9}} = 106\ \mu H \quad \textit{Eq. 16}$$

Because the ratio between the primary transformer inductance and the resonant inductance (*m*) was defined at the start of the design, the primary winding inductance can be calculated as:

$$L_p = mL_r = 4.8 \cdot 106 = 509\ \mu H \quad \textit{Eq. 17}$$

4. Software

4.1. MCU overview

The Kinetis KV4x family of MCUs is a high-performance solution offering exceptional precision, sensing, and control for some of the most demanding applications in motor and power control. Built upon the Arm® Cortex®-M4 core running at 168 MHz with a DSP and a floating-point unit, it features advanced high-speed and high-accuracy peripherals, such as a high-resolution Pulse-Width Modulation (PWM) with a 312-ps resolution, dual 12-bit Analog-to-Digital Converters (ADCs) sampling at 4.1 Mega Samples Per Second (MSPS), a total of 30 PWM channels to support multi-motor systems, and dual FlexCAN modules. To maximize the execution performance, a 128-bit flash interface is used, providing best-in-class execution from the embedded flash memory. The Kinetis KV4x MCU family is supported by a comprehensive enablement suite from NXP and third-party resources, including reference designs, software libraries, and motor-configuration tools.

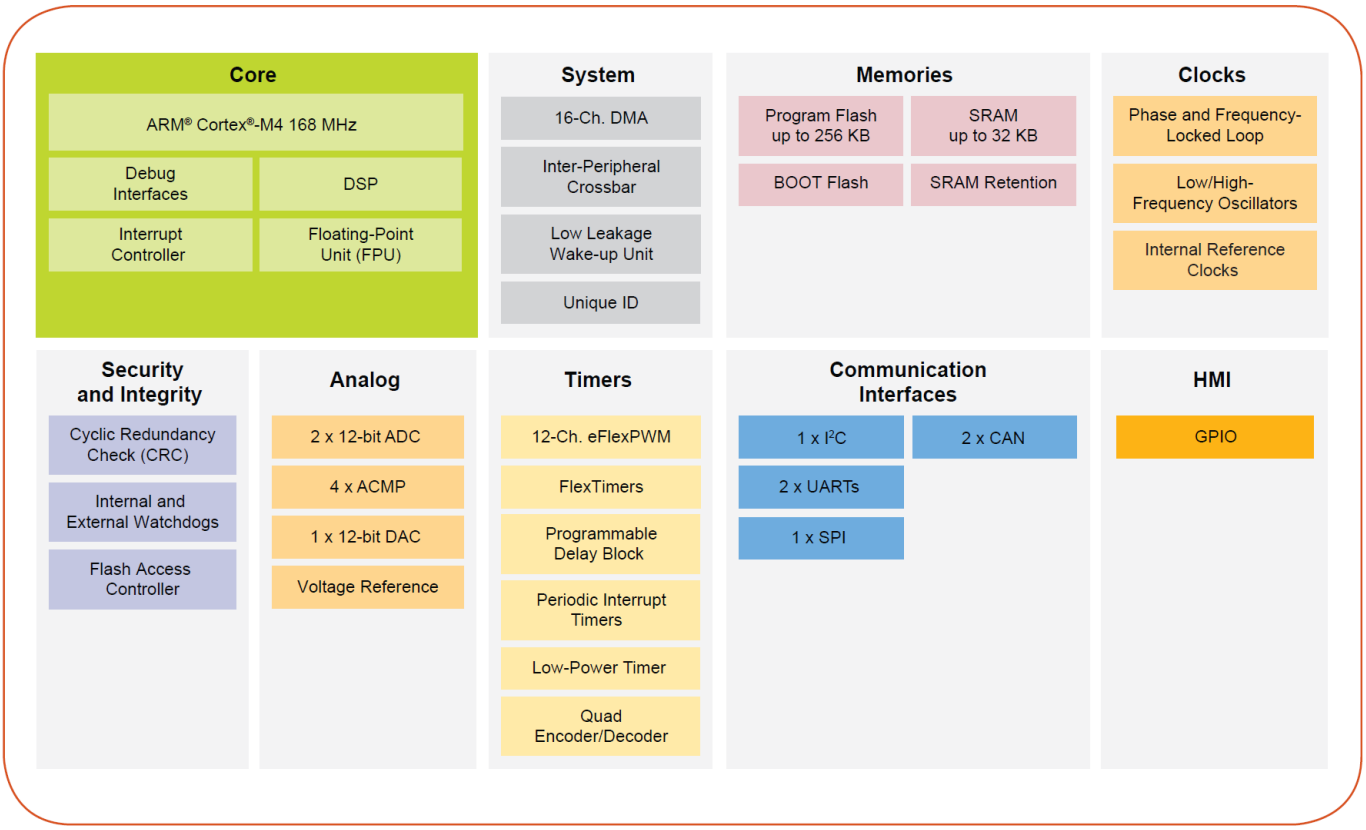

Figure 23. MCU overview

4.2. Peripheral usage

This reference design uses these peripherals:

- Pulse Width Modulator (eFlexPWM)
- 12-bit cyclic Analog-to-Digital Converter (ADC)
- Periodic Interrupt Timer (PIT)
- Analog Comparator (CMP)
- Inter-Peripheral Crossbar Switch (XBAR)
- Universal Asynchronous Receiver/Transmitter (UART)/FlexSCI
- I^2C

The detailed peripherals' functionality is described in the following sections.

4.2.1. Pulse Width Modulator (eFlexPWM)

The eFlexPWM has four PWM submodules and each one of them is set up to control a single half-bridge power stage, complementary channels, or, possibly, eight independent channels. It supports the generation of PWM signals to control electric motors and power-management applications. The eFlexPWM time reference is a 16-bit counter that can be used as an unsigned or signed counter.

The features of the enhanced PWM module include:

- The eFlexPWM module contains four PWM submodules, each of which is set up to control a single half-bridge power stage.
- 16 bits of resolution for the center, edge-aligned, and asymmetrical PWMs.
- Fractional delay for enhanced resolution of the PWM period and edge placement.
- PWM outputs that can operate as complementary pairs or independent channels.
- Ability to accept signed numbers for PWM generation.
- Independent control of both edges of each PWM output.
- Support for synchronization to external hardware or other PWMs.
- Double-buffered PWM registers.
- Integral reload rates from 1 to 16.
- Half-cycle reload capability.
- Multiple output trigger events can be generated per each PWM cycle via hardware.
- Support for double-switching PWM outputs.
- Fault inputs can be assigned to control multiple PWM outputs.
- Programmable filters for fault inputs.
- Independently-programmable PWM output polarity.
- Independent top and bottom deadtime insertion.
- Each complementary pair can operate with its own PWM frequency and deadtime values.
- Individual software control for each PWM output.
- All outputs can be programmed to change simultaneously via the FORCE_OUT event.
- The PWMX pin can optionally output a third PWM signal from each submodule.
- The channels not used for the PWM generation can be used for buffered output-compare functions.
- The channels not used for the PWM generation can be used for input-capture functions.
- Enhanced dual-edge capture functionality.
- The option to supply the source for each complementary PWM signal pair from any of the following:
  - Crossbar Switch (XBAR) module outputs.
  - External ADC input, taking into account the values set in the ADC high- and low-limit registers.

Two eFlexPWM submodules are used to generate PWM signals. The submodules are synchronized to achieve synchronous operation between the primary switches and the synchronous rectifier operation.

- Submodule 0: Setup
  - Used to drive the primary GaN low-loss switches.
  - Generate the center-align complementary PWM with automatic deadtime insertion.
  - Counter running in the unsigned mode, where INIT = 0.
  - Takes advantage of the nano-edge placement to achieve high PWM resolution.

  - Generate the output trigger in the center of the PWM pulse to trigger the ADC conversion.
- Submodule 1: Setup
  - Used to drive the secondary synchronous rectifier MOSFETs.
  - Generate two independent center-aligned PWMs.
  - Counter running in the unsigned mode, where INIT = 0.
  - Takes advantage of the nano-edge placement to achieve high PWM resolution.

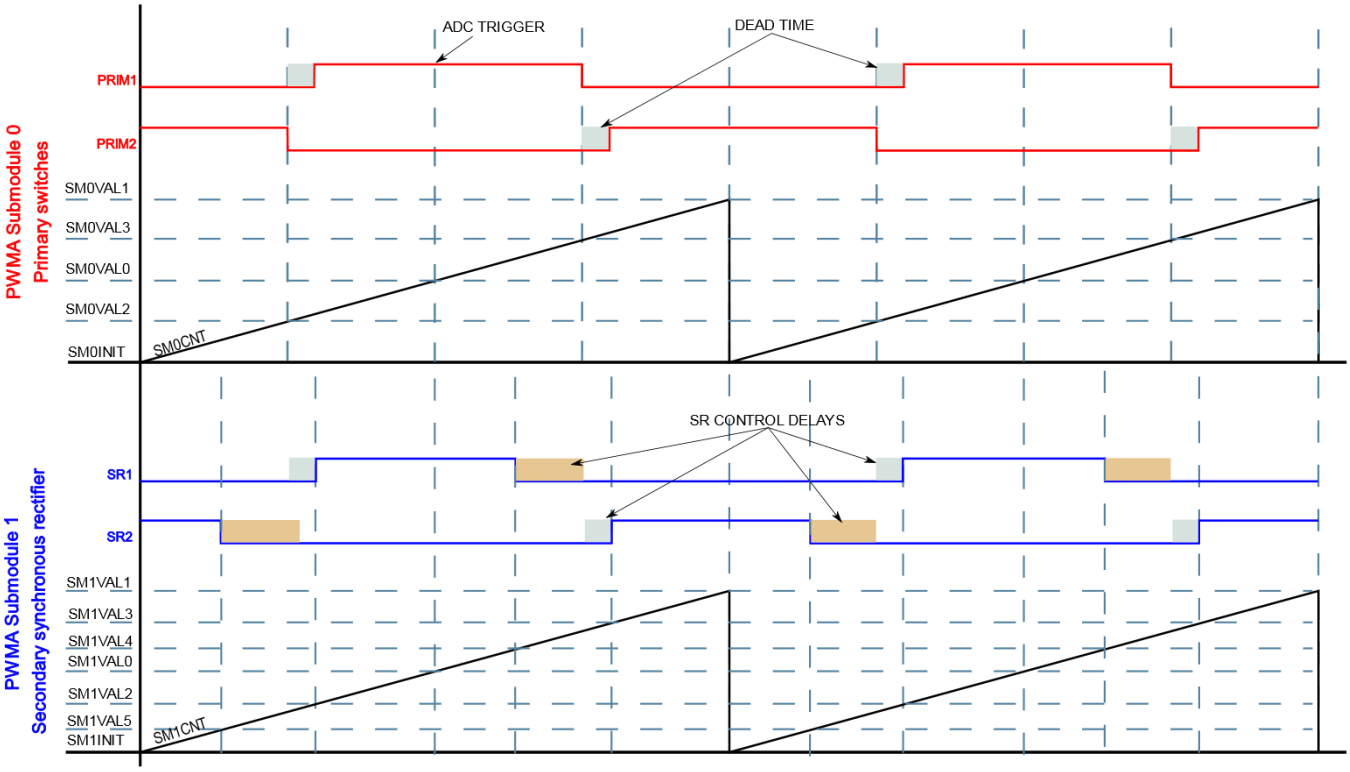

Figure 24. Primary and secondary PWM signals

4.2.2. 12-bit cyclic Analog-to-Digital Converter (ADC)

The ADC function consists of two separate ADCs, each having eight analog inputs and its own sample and hold circuit. A common digital control module configures and controls the functionality of the converters. The ADC features include:

- 12-bit resolution.
- Designed for a maximum ADC clock frequency of 25 MHz with a 40-ns period.
- Sampling rate of up to 8.83 million samples per second.
- Single conversion time of 8.5 ADC clock cycles (8.5 × 40 ns = 340 ns).
- Additional conversion time of 6 ADC clock cycles (6 × 40 ns = 240 ns).
- Eight conversions in 26.5 ADC clock cycles (26.5 × 40 ns = 1.060 µs) using the parallel mode.
- Can be synchronized to other peripherals that are connected to the internal Inter-Peripheral Crossbar module and PDB (such as the PWM) through the SYNC0/1 input signal.

- Sequentially scans and stores up to sixteen measurements.
- Scans and stores up to eight measurements, each on two ADC converters operating simultaneously and in parallel.
- The scan can pause and wait for a new SYNC input before continuing.
- Gains the input signal by x1, x2, or x4.
- Optional interrupts at end of scan when the out-of-range limit is exceeded or when there is a zero crossing.
- Optional DMA function to transfer the conversion data at the end of a scan or when a sample is ready to be read.
- Optional sample correction by subtracting a pre-programmed offset value.

In the LLC resonant converter software example, the ADC channels are assigned as follows:

- Output current—I_out—ADCA_CH6D.
- Resonant current—I_prim—ADCA_CH4.
- Output voltage—U_out—ADCB_CH2.

For the given channel assignment, this channel list is prepared:

Table 6. ADC channel list

—	0	1	2	3	4	5	6	7
ADCA	ADCA_CH6D	ADCA_CH4	X	X	X	X	X	X
ADCB	ADCB_CH2	X	X	X	X	X	X	X

4.2.3. Periodic Interrupt Timer (PIT)

The PIT is used to generate an interrupt every 200 μs. This interrupt is used for the slow loop execution. The biggest part of the control software includes a voltage-control loop, which is executed in this interrupt.

4.2.4. Analog Comparator (CMP)

Two CMPs are used for fault-protection purposes. The CMP acts as a fast hardware protection which can immediately turn off the PWM signals when normal operational conditions are exceeded, regardless of the software workflow. For more information about the CMP configuration, see Section 3.1.8, “Fault protection”.

4.2.5. Inter-Peripheral Crossbar Switch (XBAR)

This module implements an array of M N-input combinational mutexes. All mutexes share the same N inputs in the same order, but each mutex has its own independent select field. The intended application of this module is to provide a flexible crossbar switch function that enables any input (typically from external GPIO or internal module outputs) to connect to any input (typically to external GPIO or internal module inputs) under user control. This is used to enable user configuration of data paths between the internal modules and between the internal modules and GPIO.

In this example application, XBAR is used to route these signals:

- ADC triggers
- Over-current faults
- PWM FORCE signal
- Diagnostic signals

The above signals are routed to these outputs:

Table 7. XBAR signal routing

Signal purpose	XBARA input	XBARA output
ADC trigger	PWMA0_TRG0	XBARA_OUT12–ADCA_TRIG
Primary OC	CMP1_OUT	XBARA_OUT29–PWMA_FAULT0
Secondary OC	CMP0_OUT	XBARA_OUT30–PWMA_FAULT1
PWM synchronization	PWMA0_TRG1	XBARA_OUT33–PWMA_FORCE
TP29–GPIO	PWMA0_TRG0	XBARA_OUT10–XB_OUT10

4.2.6. GPIO pins

There are three GPIO outputs used to drive the status LEDs; one signal drives the output load terminal (GPIO B16), one signal confirms that the AUX power supply is running correctly, and one signal is used as the main ON/OFF switch (GPIO E1). The red LED D1 (located on the controller card) is used to indicate the run state and connects to GPIO B2. The green LED D4 (located on the main board) indicates the active state of the synchronous rectifier and connects to GPIO C16. The red LED D3 (located on the main board) indicates the fault state and connects to GPIO B19. The other GPIO pins used by the peripherals are set to the peripheral mode.

4.3. Software structure

The LLC converter software consists of two periodical interrupts and a background loop. The *ADCA_IRQHandler()* periodic interrupt is driven by the ADC converter. The period of this interrupt depends on the switching frequency. The second interrupt (*PIT0_IRQHandler ()*) is called every 200 μs by PIT 0. The background loop executes the application state machine and also handles FreeMASTER communication.

4.3.1. ADCA_IRQHandler()—fast control loop

The *ADCA_IRQHandler()* routine is called at the end of the ADC conversion. This ADC converts the output voltage and the primary and secondary currents of the LLC resonant converter. This routine is configured as the highest-priority interrupt. The ADC conversion starts in the middle of the first half of the PWM period, so the execution period of this routine is equal to the switching frequency of the LLC resonant converter. The interrupt routine stores the ADC converter results into the corresponding variables and executes the software over-current/over-voltage protections. If the output of the LLC resonant converter exceeds the allowed voltage/current limit, the PWM outputs are disabled.

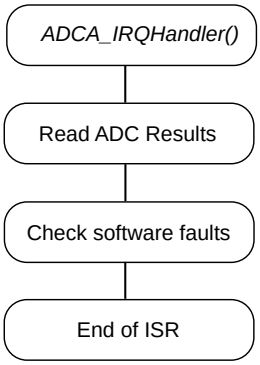

Figure 25. ADCA_IRQHandler() flowchart

4.3.2. PIT0_IRQHandler()—slow control loop

The *PIT0_IRQHandler()* routine is executed every 200 μs and manages the control loop and the software timer. The routine starts with the voltage control loop calculation for the LLC resonant converter. The output of the PI controller corresponds to the required PWM period. The PWM-compare registers of submodules 0 and 1 are updated with new values.

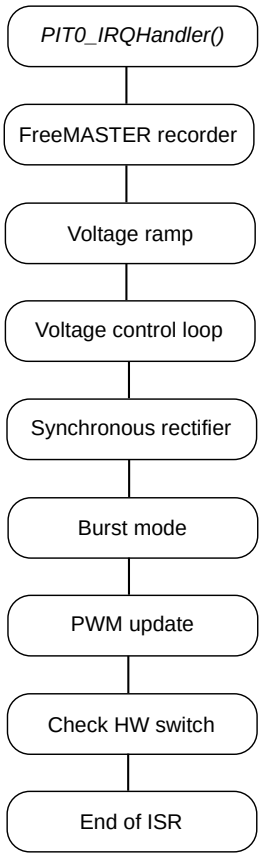

Figure 26. PIT0_IRQHandler() flowchart

4.3.3. Background loop

The software in the background loop runs in a never-ending loop. It includes the application state machine and communication with the PC (FreeMASTER).

4.3.4. Application state machine

After the reset, the MCU configures all peripherals and enters a never-ending loop, including the application state machine. The application state machine goes through the *AppInit* state into the *Stop* state. In the *Stop* state, the application state machine regularly checks the ON/OFF switch state. When the switch is ON and the AUX power supply is ready, the application state machine continues into the *AppStartLLC* state. If there is no fault condition during the startup of the LLC resonant converter, the application voltage control loop closes and the state machine continues into the *AppRun* state. In both the *AppStartLLC* and *AppRun* states, the application state machine checks the fault events. If a fault condition is detected, the application state machine enters the *AppError* state. The state machine states are indicated by the LED diodes. If the application state machine enters the *AppError* state, it waits for a pre-defined delay and then tries to start the converter again.

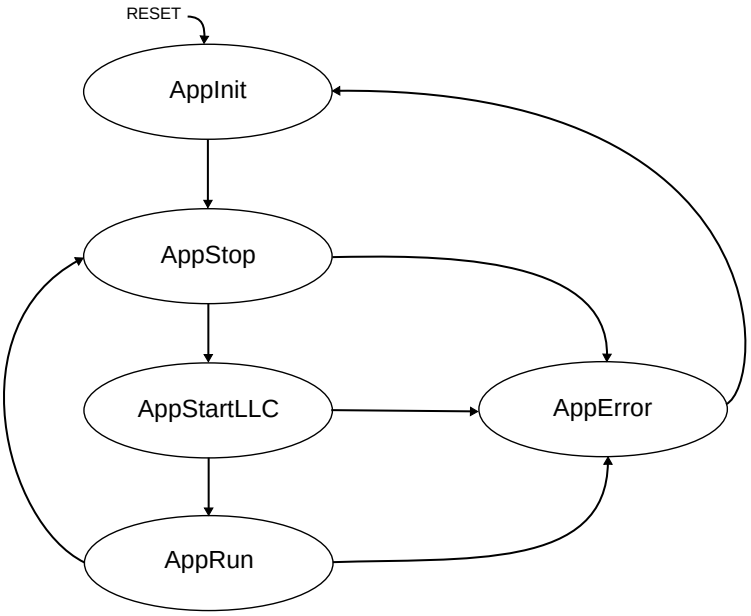

Figure 27. Application state machine

4.4. Startup

The converter soft-start startup is implemented in this design to enable a slow buildup of the output current and voltage. When the software recognizes a power-on request, the start-up sequence is initiated and the converter starts to execute the required start-up tasks. Firstly, the converter waits for a pre-defined delay to stabilize the input voltage. After this delay, all control variables are initialized to the start-up state, including the top frequency limit which is set to 203 kHz to achieve the smallest possible gain and a low amplitude of the inrush current. This frequency is also designed to keep the soft switching during the start-up sequence. Secondly, the bottom PWM signal is unmasked to pre-charge the

bootstrap circuits of the top-side pre-driver. This step is necessary for a proper operation of the high-side switch. When the bootstrap circuits are ready, the top PWM signal is enabled, which causes the converter output voltage to raise to a certain level. At this point, the deadtime ramping takes place to slowly ramp up the voltage to enter the entering point of the voltage ramp. It is very important to set up the dead-time ramp correctly to keep the converter in the soft-switching mode during startup. Otherwise, the primary switches can overload. When the dead-time ramping completes, the system enters the voltage close loop region where the PI controller controls the voltage according to the required voltage amplitude from the voltage ramp. The PWM frequency in this region varies from 75 kHz to 203 kHz. When the output voltage reaches 75 % of the required voltage, the upper frequency limit changes to 149 kHz. The PI controller follows the output ramp voltage until it is equal to the required voltage. Now, the start-up sequence is done and the converter continues with the normal operation (constant output voltage). The start-up sequence is shown in Figure 28.

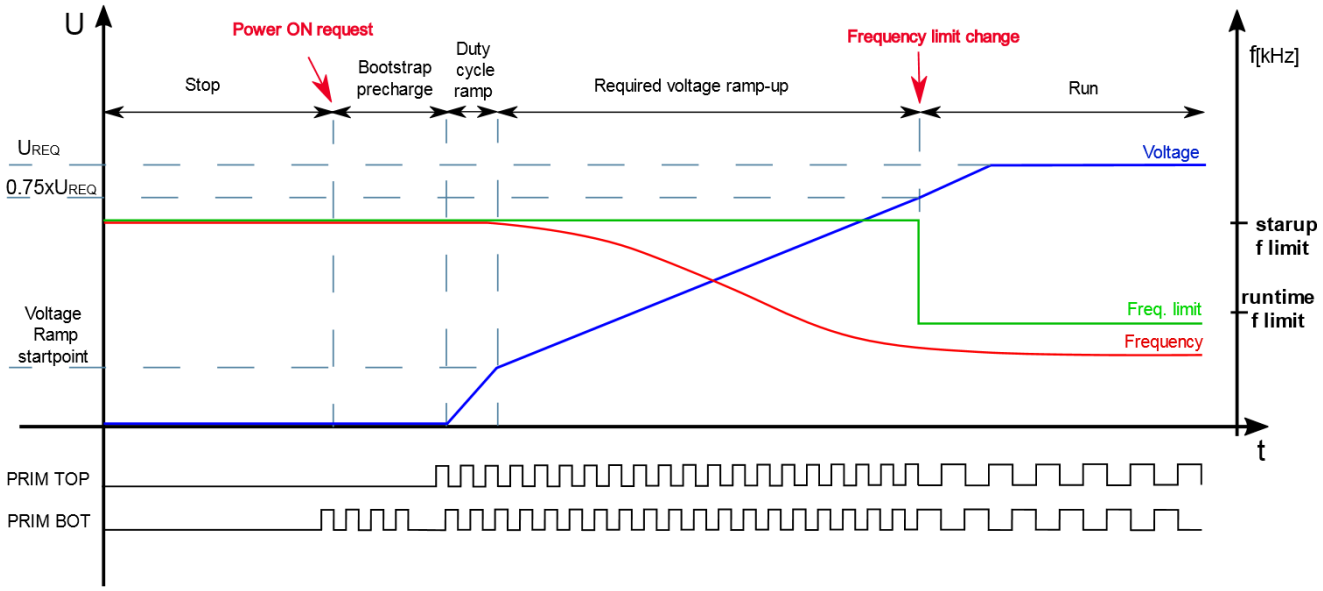

Figure 28. Start-up sequence

4.5. Synchronous rectifier control

The Synchronous Rectifier (SR) is an important part of this design. It helps to maintain good efficiency even at high output-current amplitudes. It consists of two low R_{DSON} MOSFETs and a gate drive circuit. Due to a fully digital control, there is no need for an analog comparator to sense the MOSFETs' voltage drop as with the traditional analog SR control. This simplifies the control circuit and provides a precise, highly-efficient, and low-complexity SR control solution. Because the primary switches and the SR are controlled from one MCU, it is easy to calculate and control the MOSFET switching instants.

The switching instants depend strongly on the converter operation mode. If the switching frequency is lower than the resonance frequency, the rectifier current falls to a zero value even before the primary switch is turned off. At the resonance frequency, the current reaches zero when the primary switch is turned off. The last case is the operation over the resonance frequency when the current must be turned off at the end of the period, even if the current has a non-zero value. In this region, higher commutation losses can be observed due to hard switching.

The current waveform at different modes is shown in Figure 24. The reference software uses a different PWM strategy for the primary and secondary (SR) switches. The rising edge of the SR PWM signal is aligned with the corresponding primary PWM signal, while the falling edge is always switched earlier than the primary PWM signal according to the actual switching frequency. The value of the off interval is interpolated using a look-up table, based on the actual switching frequency. The switching of PWM patterns and current shapes at various modes is shown in Figure 29.

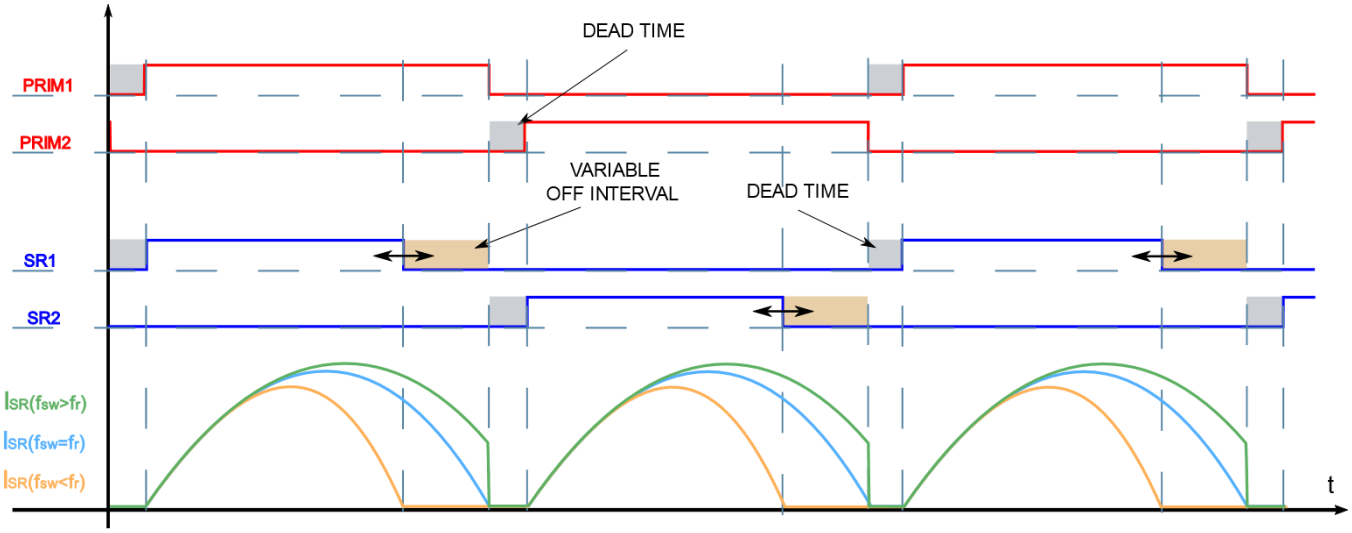

Figure 29. SR current and SR switching pattern

4.6. Burst mode

At a very light load, the PI controller may saturate at the frequency limit and is no longer able to keep the output voltage at the required value. Because the gain is already at the minimum value, another strategy of the output voltage control must be used. One possible solution is to use the burst mode. The burst mode can control the output voltage and also improve the converter light-load efficiency due to the switching losses reduction.

This design provides a constant-period burst mode, which is activated only at no-load or very-light-load conditions. To activate the burst mode, these conditions must be met:

- The voltage controller is saturated.
- The output voltage amplitude exceeds the required voltage value.

If both of the above conditions are met, the software disables the PWM outputs. When the output voltage drops below the required value again, the software enables the PWM outputs, charges the output capacitors, and then disables the PWM again. When the burst period ends, the software waits for the beginning of a new burst period and repeats the process again. In this design, a burst frequency of 100 Hz was selected, which means that one burst cycle takes 10 ms. This period ensures low voltage ripple and reasonable efficiency. To ensure a proper operation of the high-side switch, the bootstrap circuits are refreshed by several PWM pulses at the beginning of every burst period. The functionality of the burst mode and the transition to the normal mode is shown in Figure 30.

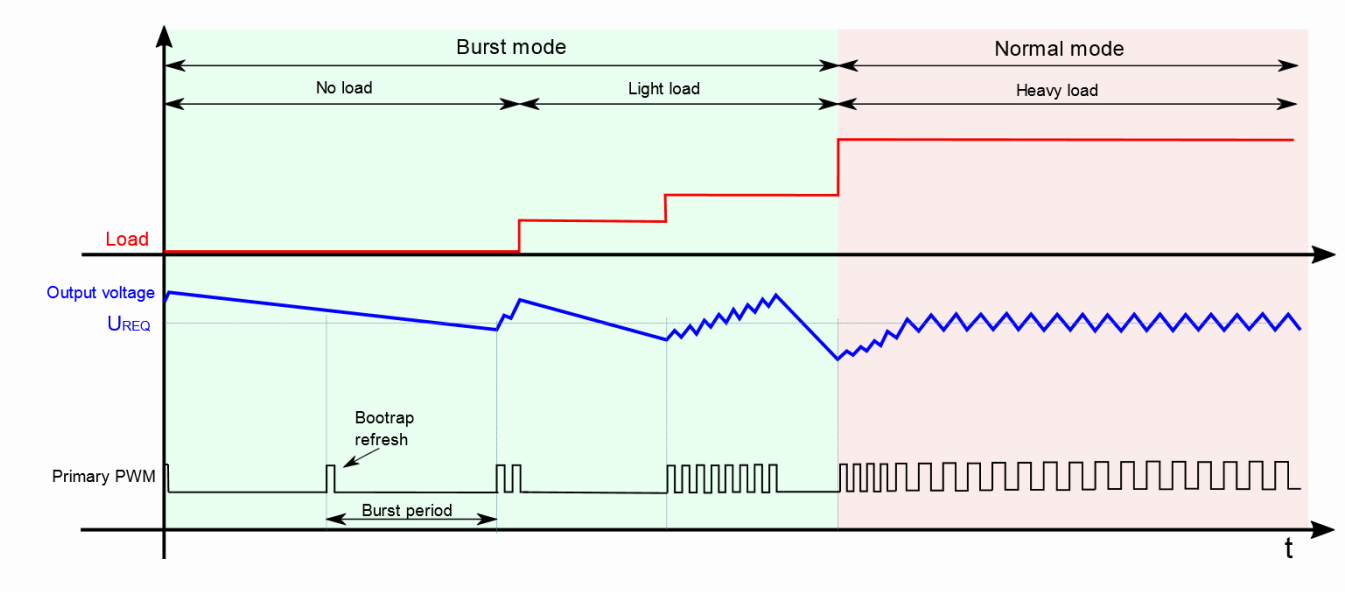

Figure 30. Burst mode

4.7. Fault protection

Both the secondary output and primary resonant currents are measured by the ADC. In addition, these signals are connected also to the internal MCU analog comparators which act as hardware protection. The software protection includes only the over-voltage protection.

The MCU constantly monitors the converter output current using the current-measurement circuit and the CMP1_IN4 comparator input. This comparator is the source of the FAULT 1 signal which is routed to the eFlexPWM module via XBAR. For the secondary side, the fault threshold is set to 33 A.

The MCU also constantly monitors the resonant circuit current using the isolated current-measurement circuit and the CMP0_IN5 comparator input. This comparator is the source of the FAULT 0 signal which is routed to the eFlexPWM module via XBAR. For the primary side, the fault threshold is set to 4.5 A.

For detailed information about the fault signal routing in XBAR, see Section 4.2.5, “Inter-Peripheral Crossbar Switch (XBAR)”.

The board input is also protected by melting fuse F1. Always replace this fuse with the same value and the same characteristic as its default values. The default value is F1.6 A/250 V.

4.8. Measurement and evaluation

4.8.1. Efficiency

Several efficiency measurements were made. Figure 31 shows the efficiency at the input voltage of 390 V. Figure 32 shows the efficiency at the input voltage of 330 V.

Table 8. Test results at input voltage of 390 V

Uin [V]	Iin [A]	Uout [V]	Iout [A]	Pin [W]	Pout [W]	ΔP [W]	η [%]	Load [%]
390	0.003	12.00	0.000	1.17	0.00	1.17	0.00	0.00
390	0.023	11.98	0.530	8.97	6.35	2.62	70.78	2.54
390	0.037	11.98	1.029	14.43	12.33	2.10	85.43	4.93
390	0.069	11.99	2.027	26.91	24.30	2.61	90.31	9.72
390	0.130	12.00	4.025	50.70	48.30	2.40	95.27	19.32
390	0.193	12.01	6.028	75.27	72.40	2.87	96.18	28.96
390	0.257	12.02	8.028	100.23	96.50	3.73	96.28	38.60
390	0.321	12.04	10.025	125.19	120.70	4.49	96.41	48.28
390	0.385	12.05	12.025	150.15	144.90	5.25	96.50	57.96
390	0.450	12.06	14.025	175.50	169.14	6.36	96.38	67.66
390	0.515	12.07	16.024	200.85	193.41	7.44	96.30	77.36
390	0.581	12.09	18.024	226.59	217.91	8.68	96.17	87.16
390	0.648	12.10	20.024	252.72	242.29	10.43	95.87	96.92
390	0.681	12.10	21.024	265.59	254.39	11.20	95.78	101.76

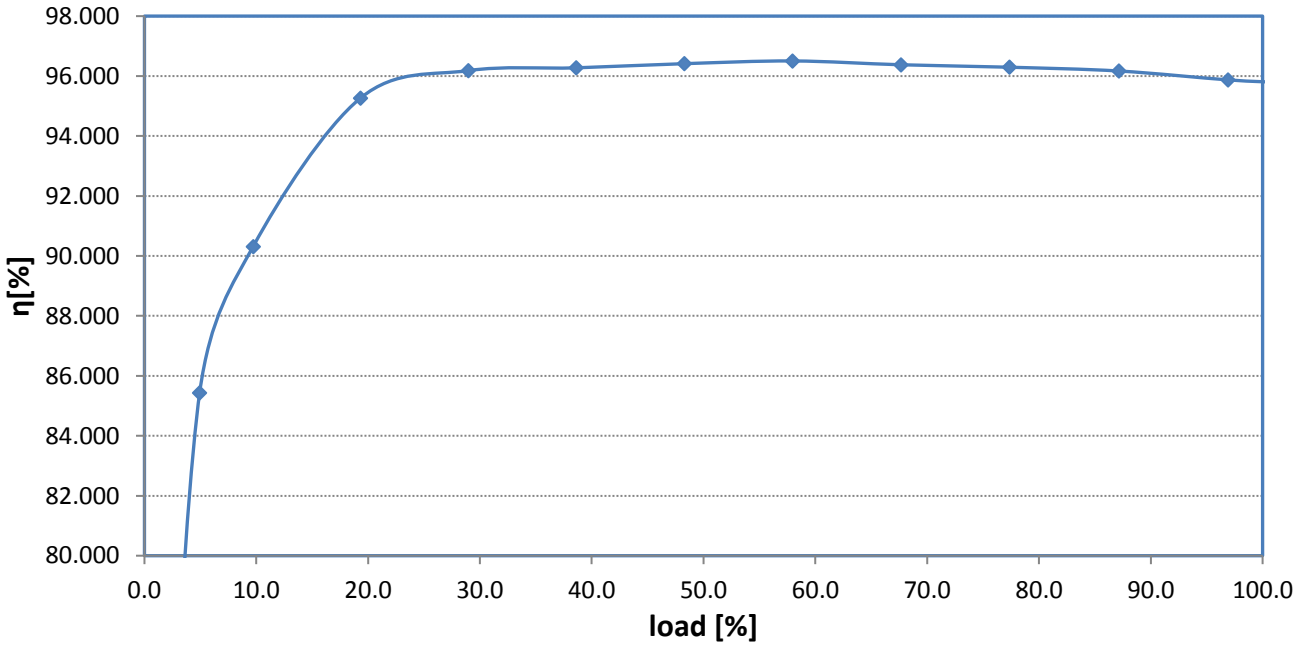

Figure 31. Efficiency at input voltage of 390 V

Table 9. Test results at input voltage of 330 V

Uin [V]	Iin [A]	Uout [V]	Iout [A]	Pin [W]	Pout [W]	ΔP [W]	η [%]	Load [%]
330	0.003	12.00	0.000	0.99	0.00	0.99	0.00	0.00
330	0.027	11.98	0.529	8.91	6.34	2.57	71.13	2.53
330	0.045	11.99	1.027	14.85	12.31	2.54	82.92	4.93
330	0.082	11.99	2.026	27.06	24.29	2.77	89.77	9.72
330	0.155	12.00	4.026	51.15	48.31	2.84	94.45	19.32
330	0.229	12.01	6.025	75.57	72.36	3.21	95.75	28.94
330	0.304	12.01	8.025	100.32	96.38	3.94	96.07	38.55
330	0.379	12.02	10.025	125.07	120.50	4.57	96.35	48.20
330	0.455	12.03	12.025	150.15	144.66	5.49	96.34	57.86
330	0.532	12.03	14.025	175.56	168.72	6.84	96.10	67.49
330	0.609	12.04	16.024	200.97	192.93	8.04	96.00	77.17
330	0.687	12.05	18.024	226.71	217.19	9.52	95.80	86.88
330	0.766	12.05	20.024	252.78	241.29	11.49	95.45	96.52
330	0.806	12.07	21.024	265.98	253.76	12.22	95.41	101.50

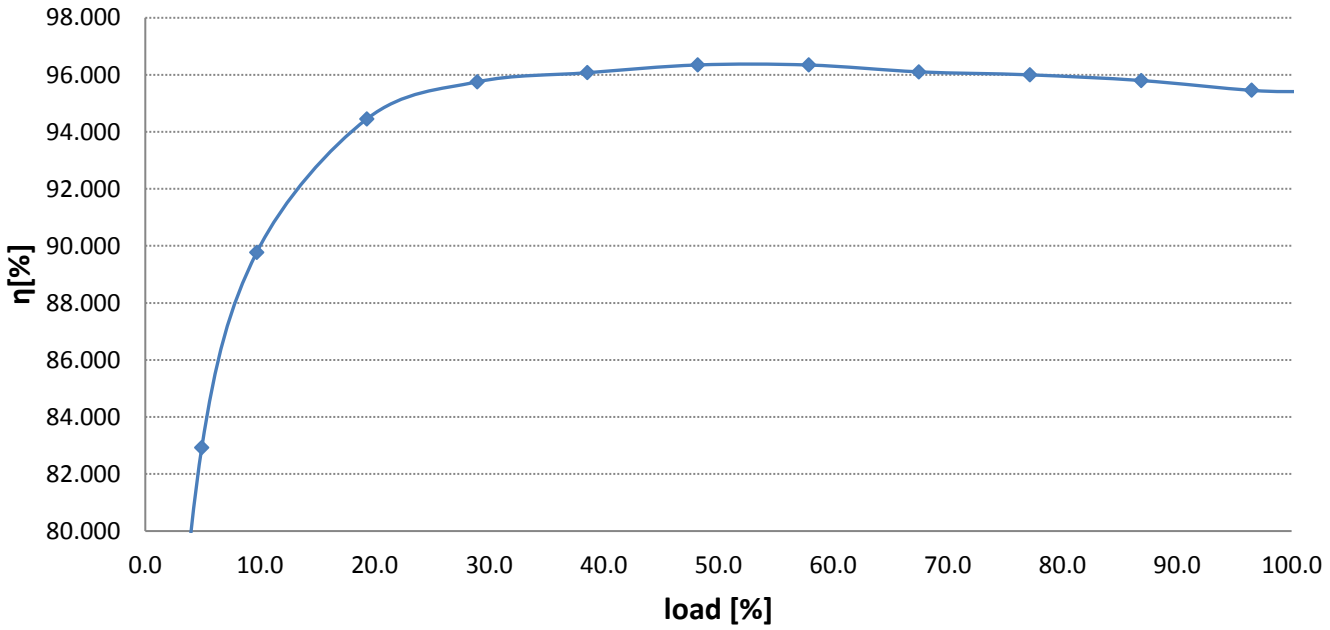

Figure 32. Efficiency at input voltage of 330 V

4.8.2. Thermal analysis

Thermal analysis helps to locate the places with the highest power losses. A photo was taken after 20 minutes of operation at a 100 % load, without a forced air flow, at the ambient temperature of 22 °C. Figure 33 shows that most of the heat is generated by the secondary winding of the transformer which dissipates a lot of heat also into the PCB. The hottest place reached a temperature of almost 80 °C.

This is caused by a high resistance of the secondary winding or a skin effect caused by the high switching frequency. This can be eliminated using a better-quality wire for the secondary winding.

The second most warm place on the PCB are the synchronous rectifier MOSFETs. On this board, only one MOSFET per transformer tap is used. To improve the SR efficiency, use a parallel combination of several MOSFETs.

A small amount of heat is dissipated also by the output current-sense resistors and by the AUX power supply. The primary GaN switches are cold due to operation in the soft-switching region.

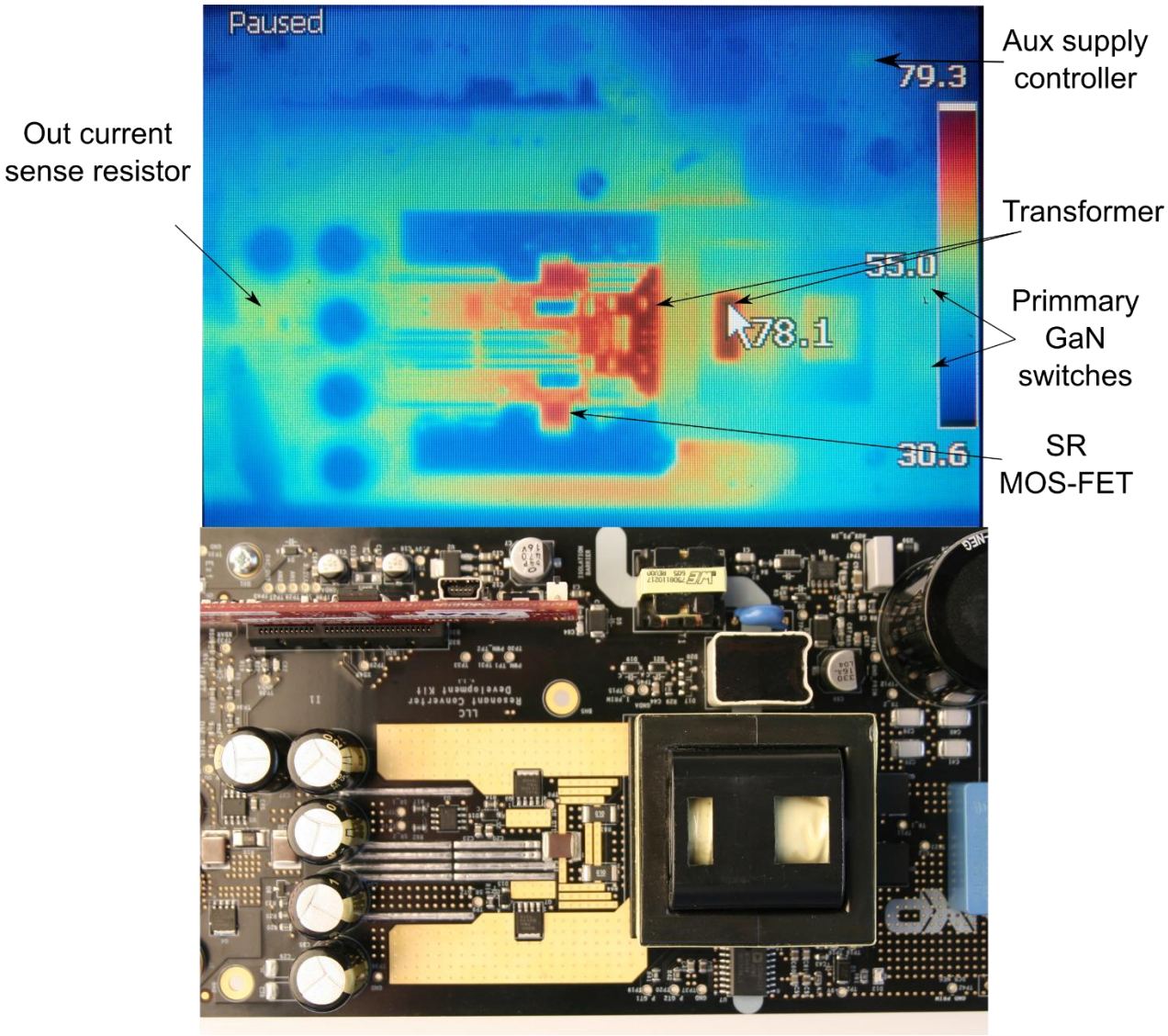

Figure 33. Thermal shot at maximum load

4.8.3. Voltage ripple

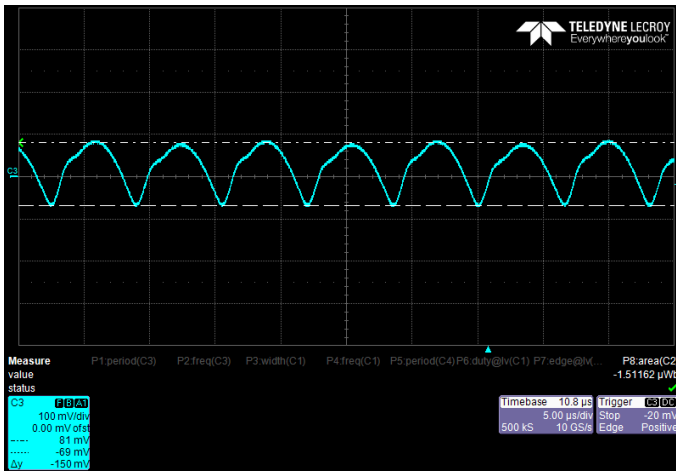

Figure 34. Output voltage ripple at input voltage of 330 V and load of 21 A

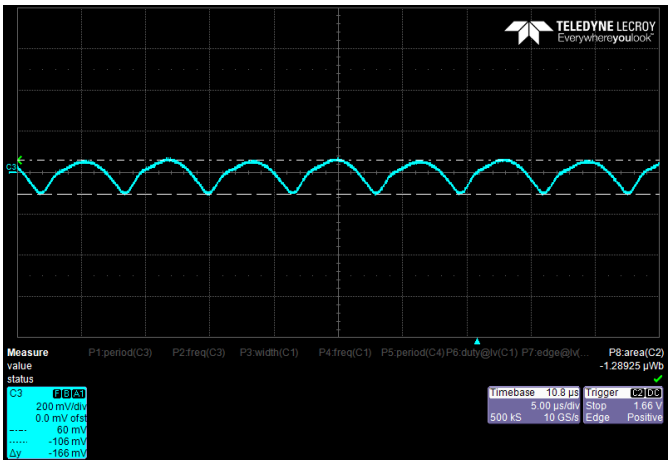

Figure 35. Output voltage ripple at input voltage of 330 V and load of 10 A

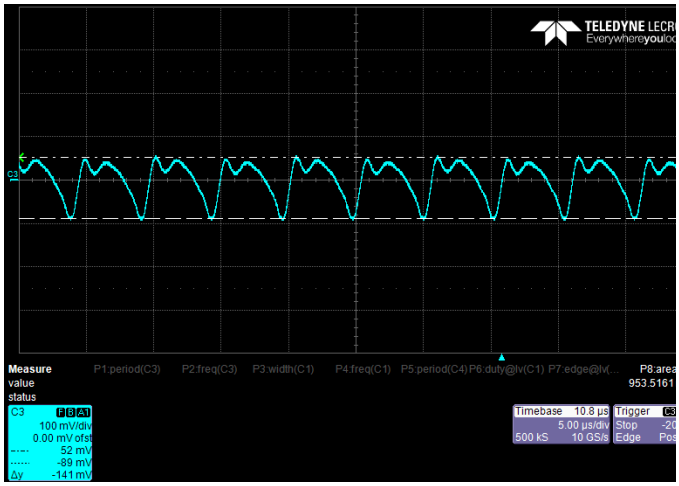

Figure 36. Output voltage ripple at input voltage of 390 V and load of 21 A

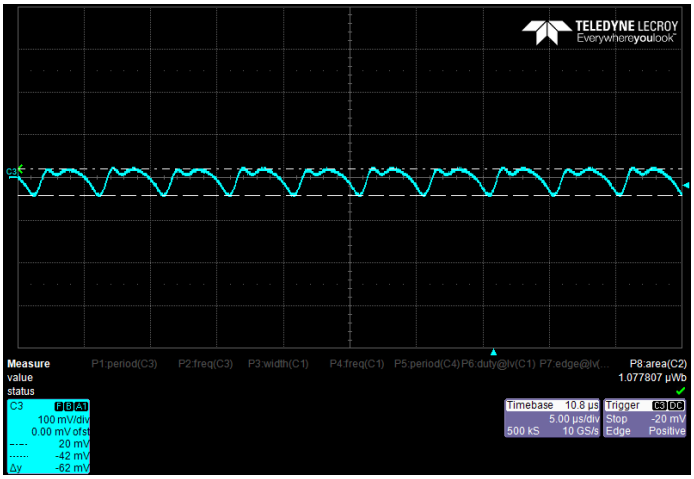

Figure 37. Output voltage ripple at input voltage of 390 V and load of 10 A

4.8.4. Step response

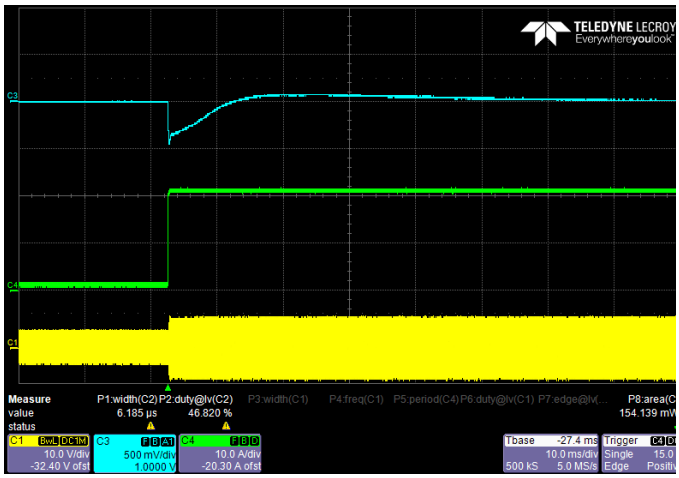

Figure 38. Load step from 5 % to 100 % at input voltage of 330 V (Yellow – primary current, Green – output current, Blue – output voltage (AC coupled))

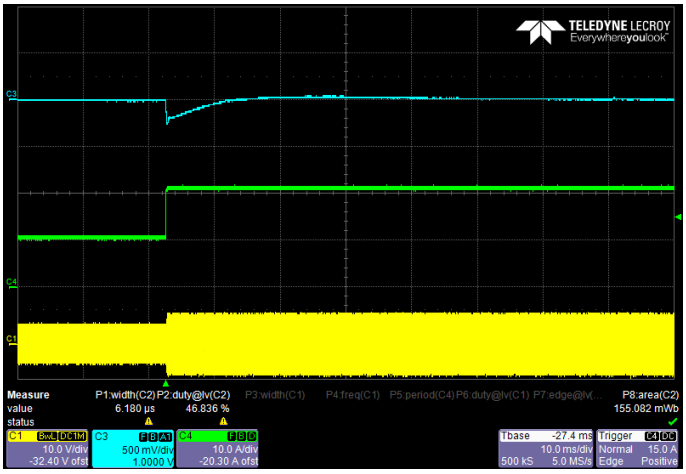

Figure 40. Load step from 50 % to 100 % at input voltage of 330 V (Yellow – primary current, Green – output current, Blue – output voltage (AC coupled))

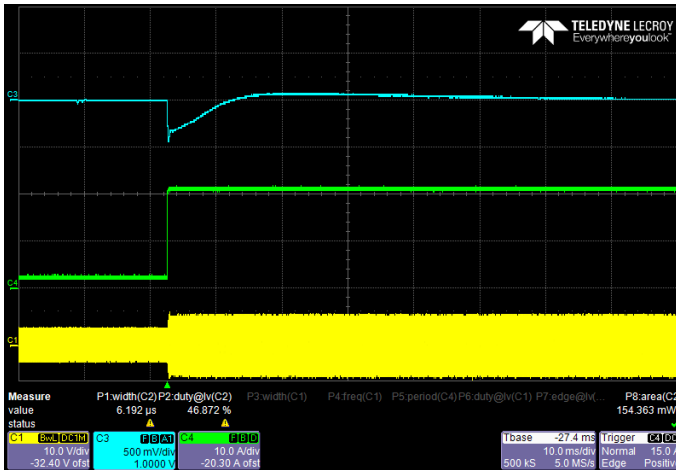

Figure 39. Load step from 10 % to 100 % at input voltage of 330 V (Yellow – primary current, Green – output current, Blue – output voltage (AC coupled))

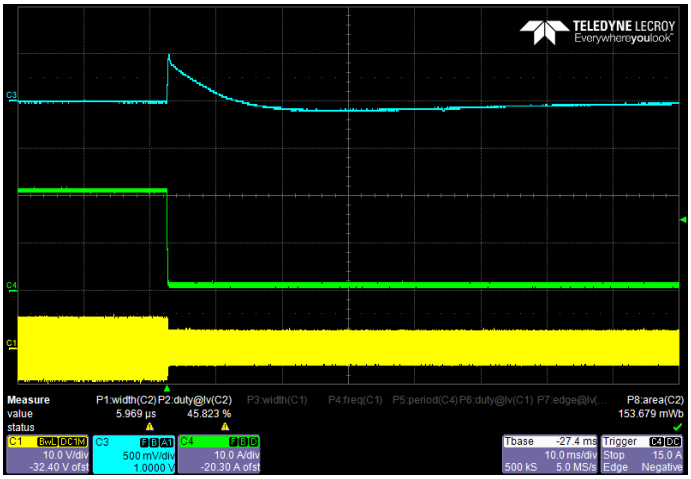

Figure 41. Load step from 100 % to 5 % at input voltage of 330 V (Yellow – primary current, Green – output current, Blue – output voltage (AC coupled))

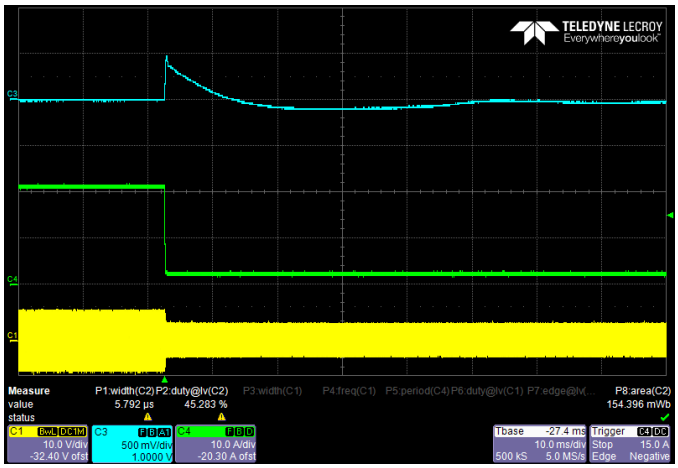

Figure 42. Load step from 100 % to 10 % at input voltage of 330 V (Yellow – primary current, Green – output current, Blue – output voltage (AC coupled))

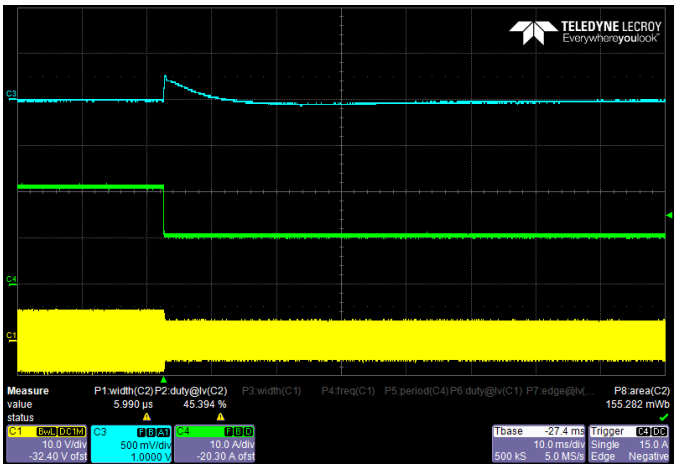

Figure 43. Load step from 100 % to 50 % at input voltage of 330 V (Yellow – primary current, Green – output current, Blue – output voltage (AC coupled))

4.8.5. Startup

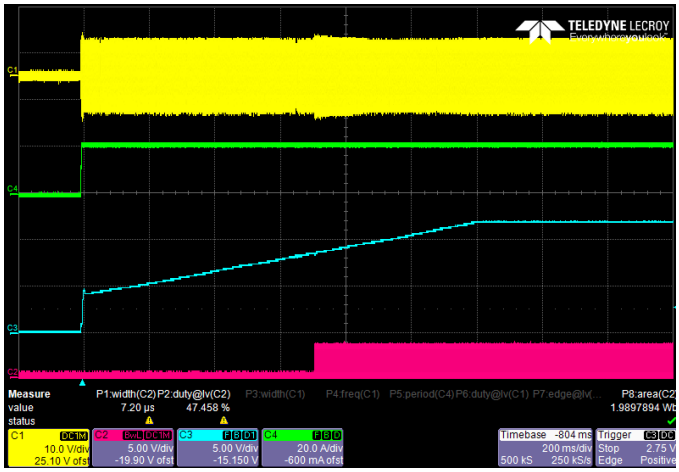

Figure 44. Full-load startup (Yellow – primary current, Green – output current, Blue – output voltage, Magenta – synchronous rectifier)

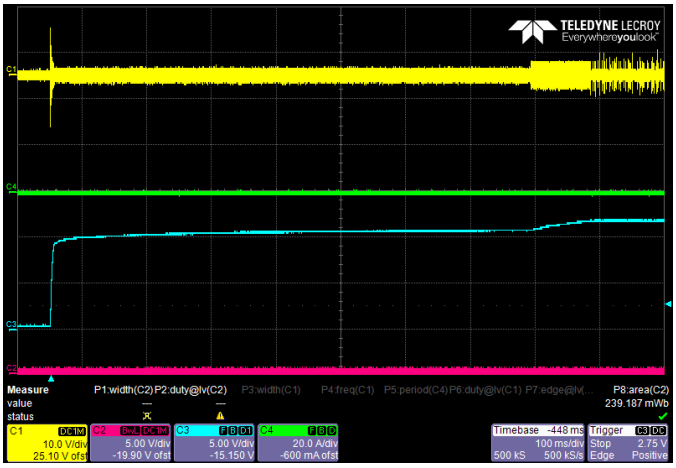

Figure 45. No-load startup (Yellow – primary current, Green – output current, Blue – output voltage, Magenta – synchronous rectifier)

4.8.6. Soft switching

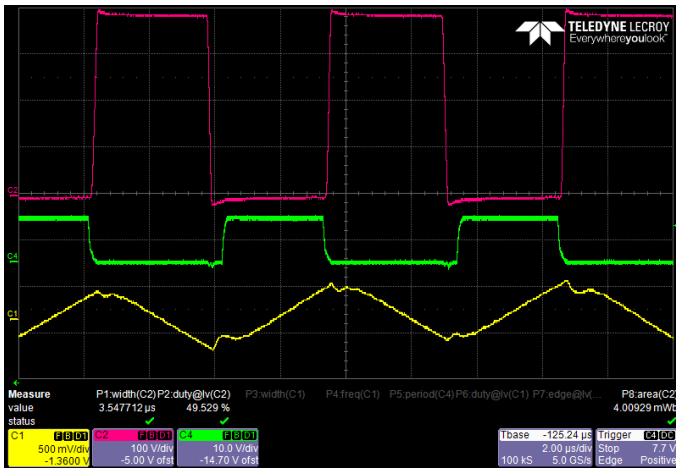

Figure 46. No-load operation at 390 V DC (Yellow – primary current, Green – Q1 U_{GS}, Magenta – Q1 U_{DS})

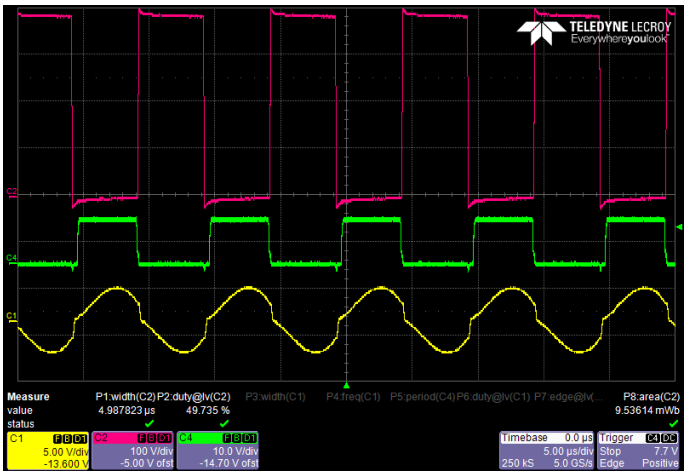

Figure 48. 50 % load operation at 390 V DC (Yellow – primary current, Green – Q1 U_{GS}, Magenta – Q1 U_{DS})

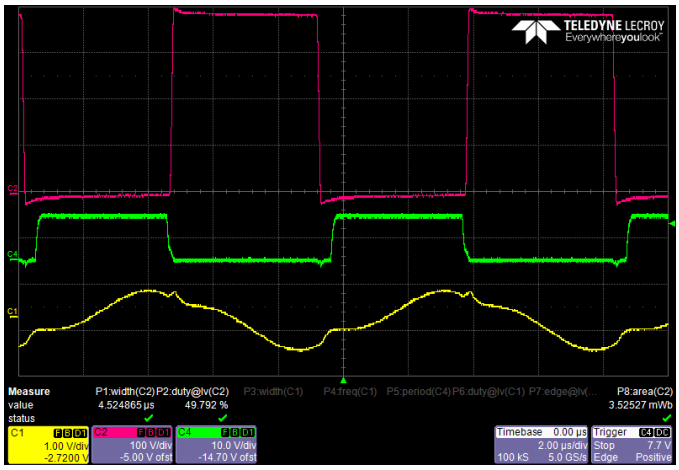

Figure 47. 5 % load operation at 390 V DC (Yellow – primary current, Green – Q1U_{GS}, Magenta – Q1 U_{DS})

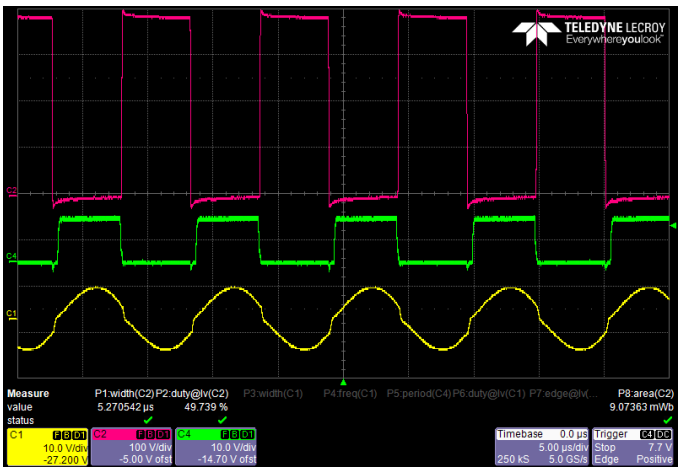

Figure 49. 100 % load operation at 390 V DC (Yellow – primary current, Green – Q1 U_{GS}, Magenta – Q1 U_{DS})

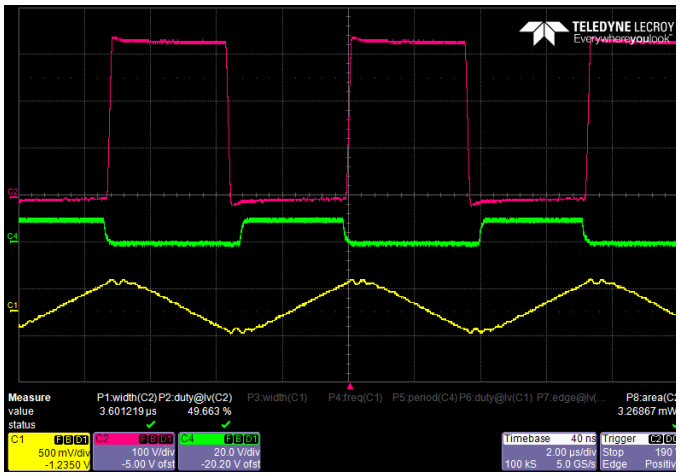

Figure 50. No-load operation at 330 V DC (Yellow – primary current, Green – Q1 U_{GS}, Magenta – Q1 U_{DS})

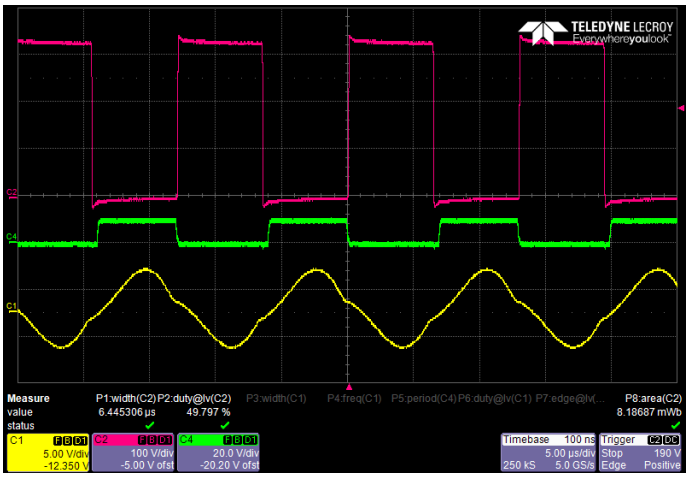

Figure 52. 50 % load operation at 330 V DC (Yellow – primary current, Green – Q1 U_{GS}, Magenta – Q1U_{DS})

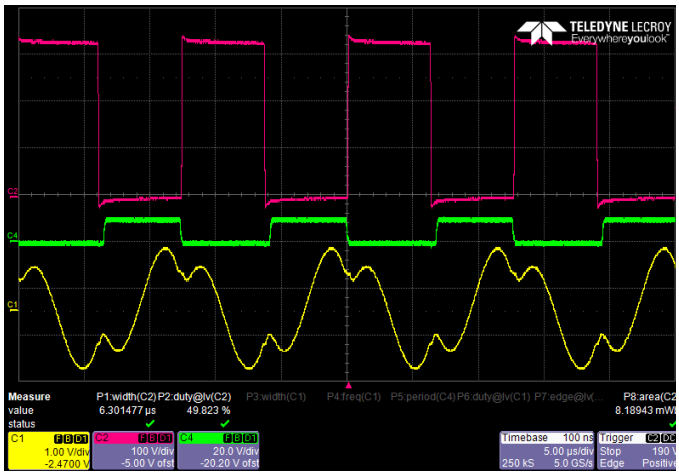

Figure 51. 5 % load operation at 330 V DC (Yellow – primary current, Green – Q1 U_{GS}, Magenta – Q1 U_{DS})

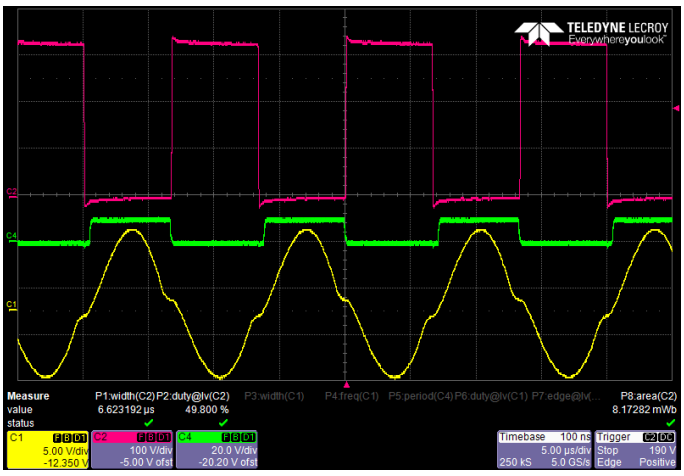

Figure 53. 100 % load operation at 330 V DC (Yellow – primary current, Green – Q1 U_{GS}, Magenta – Q1 U_{DS})

4.8.7. CPU load

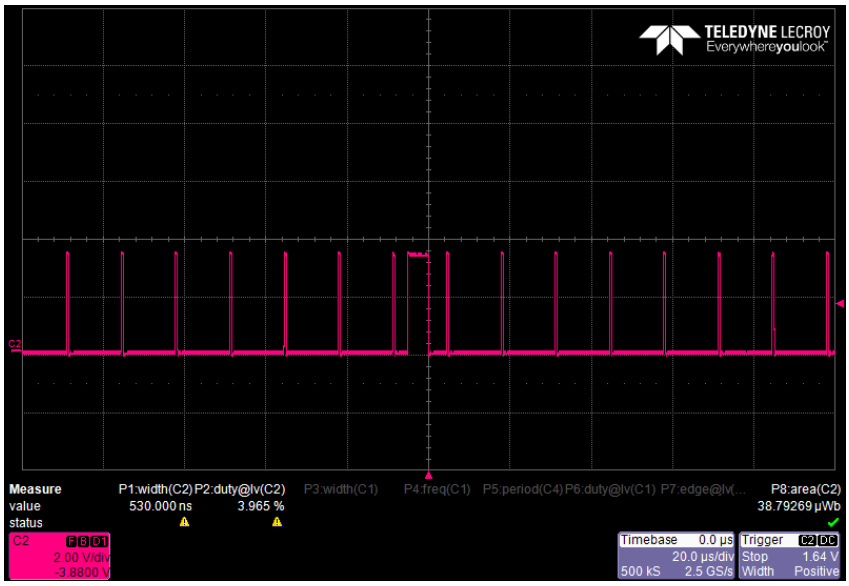

Figure 54. CPU load

- Average slow loop duration = 5 µs
- Average fast loop length duration = 500 ns
- Average CPU load at 168-MHz core clock – 12.5 %

4.9. Application configuration

The application is configured using the macros stored in the *LLC_appconfig.h* file. The description of constants is provided in Table 10.

Table 10. Application configuration

Group	Name	Description	Default value
Application scales and constants	I_IN_MAX	Maximal scale of primary resonant current measurement circuit	6.6
	I_OUT_MAX	Maximal scale of secondary output current measurement circuit	66.0
	U_OUT_MAX	Maximal scale of secondary output voltage measurement circuit	14
	U_OUT_REQUIRED	Required out voltage	FRAC16(0.857)
	U_OUT_OVERVOLTAGE	Secondary over-voltage fault threshold	FRAC16(0.97)
	PWM_PERIOD_LIMIT_HIGH	Maximal PWM period in timer cycles	1092
	PWM_DEAD_TIME	Deadtime in runtime	941
	PWM_DEAD_TIME_MAX	Max deadtime during startup	3000
	PWM_DEAD_TIME_HW	Deadtime added by ISO MOSFET pre-driver	806
Synchronous rectifier	SR_CURRENT_THRESHOLD_ON	Value of output current when SR is ON	FRAC16(0.02)
	SR_CURRENT_THRESHOLD_OFF	Value of output current when SR is OFF	FRAC16(0.01)
	SR_TURN_ON_DELAY	Time delay between on and off	10
	SR_CTRL_MIN_PERIOD_LIMIT	Maximal frequency for SR operation	FRAC16(0.64)
Voltage controller	U_KP_GAIN	Voltage controller P gain	ACC32(0.13)
	U_KI_GAIN	Voltage controller I gain	ACC32(0.03)
	U_CTRL_MAX_PERIOD_LIMIT	Maximal period	FRAC16(1.00)
	U_CTRL_MIN_STARTUP_PERIOD	Minimal period during startup	FRAC16(0.379)
	U_CTRL_MIN_PERIOD_LIMIT	Minimal period at runtime	FRAC16(0.516)
Startup voltage ramp	STARTUP_U_THRESHOLD	Startup voltage threshold	(U_OUT_REQUIRED*0.75)
	U_RAMP_UP	Voltage ramp rising edge	FRAC16 (0.0001)
	U_RAMP_DOWN	Voltage ramp falling edge	FRAC16 (0.0001)
	D_RAMP_UP	Deadtime ramp rising edge	FRAC16 (0.0003)
	D_RAMP_DOWN	Deadtime ramp falling edge	FRAC16 (0.0003)
	VOLTAGE_RAMP_STARTPOINT	Voltage ramp start point	FRAC16 (0.01)
	CONVERTER_ON_DELAY	Delay after powerup	15000
Burst mode	BURST_PERIOD	Burst mode period	50

5. Revision history

Table 11 summarizes the changes done to this document since the initial release.

Table 11. Revision history

Revision number	Date	Substantive changes
0	08/2017	Initial release

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