

6.4.7 VSNVS LDO/switch

VSNVS powers the low-power, SNVS/RTC domain on the processor. It derives its power from either V_{IN} , or coin cell, and cannot be disabled. When powered by both, V_{IN} takes precedence when above the appropriate comparator threshold. When powered by V_{IN} , VSNVS is an LDO capable of supplying seven voltages: 3.0, 1.8, 1.5, 1.3, 1.2, 1.1, and 1.0 V. The bits VSNVSVOLT[2:0] in register VSNVS_CONTROL determine the output voltage. When powered by coin cell, VSNVS is an LDO capable of supplying 1.8, 1.5, 1.3, 1.2, 1.1, or 1.0 V as shown in [Table 108](#). If the 3.0 V option is chosen with the coin cell, VSNVS tracks the coin cell voltage by means of a switch, whose maximum resistance is 100 Ω . In this case, the VSNVS voltage is simply the coin cell voltage minus the voltage drop across the switch, which is 40 mV at a rated maximum load current of 400 μ A.

The default setting of the VSNVSVOLT[2:0] is 110, or 3.0 V, unless programmed otherwise in OTP. However, when the coin cell is applied for the very first time, VSNVS outputs 1.0 V. Only when V_{IN} is applied thereafter does VSNVS transition to its default, or programmed value if different. Upon subsequent removal of V_{IN} , with the coin cell attached, VSNVS changes configuration from an LDO to a switch for the “110” setting, and remains as an LDO for the other settings, continuing to output the same voltages as when V_{IN} is applied, providing certain conditions are met as described in [Table 108](#).

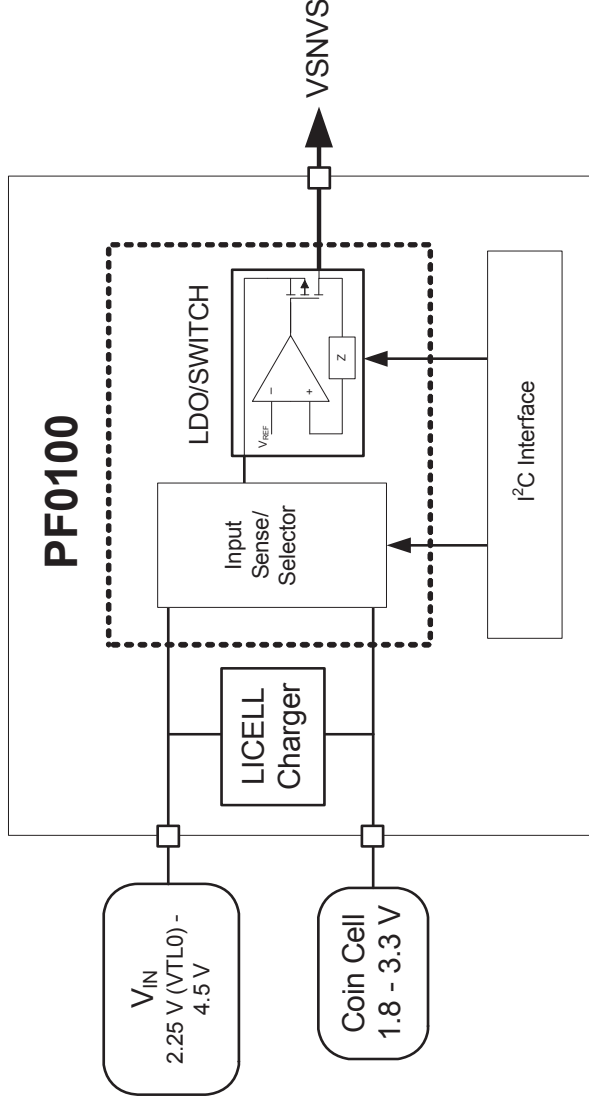


Figure 32. VSNVS supply switch architecture

[Table 108](#) provides a summary of the VSNVS operation at different input voltage V_{IN} and with or without coin cell connected to the system.