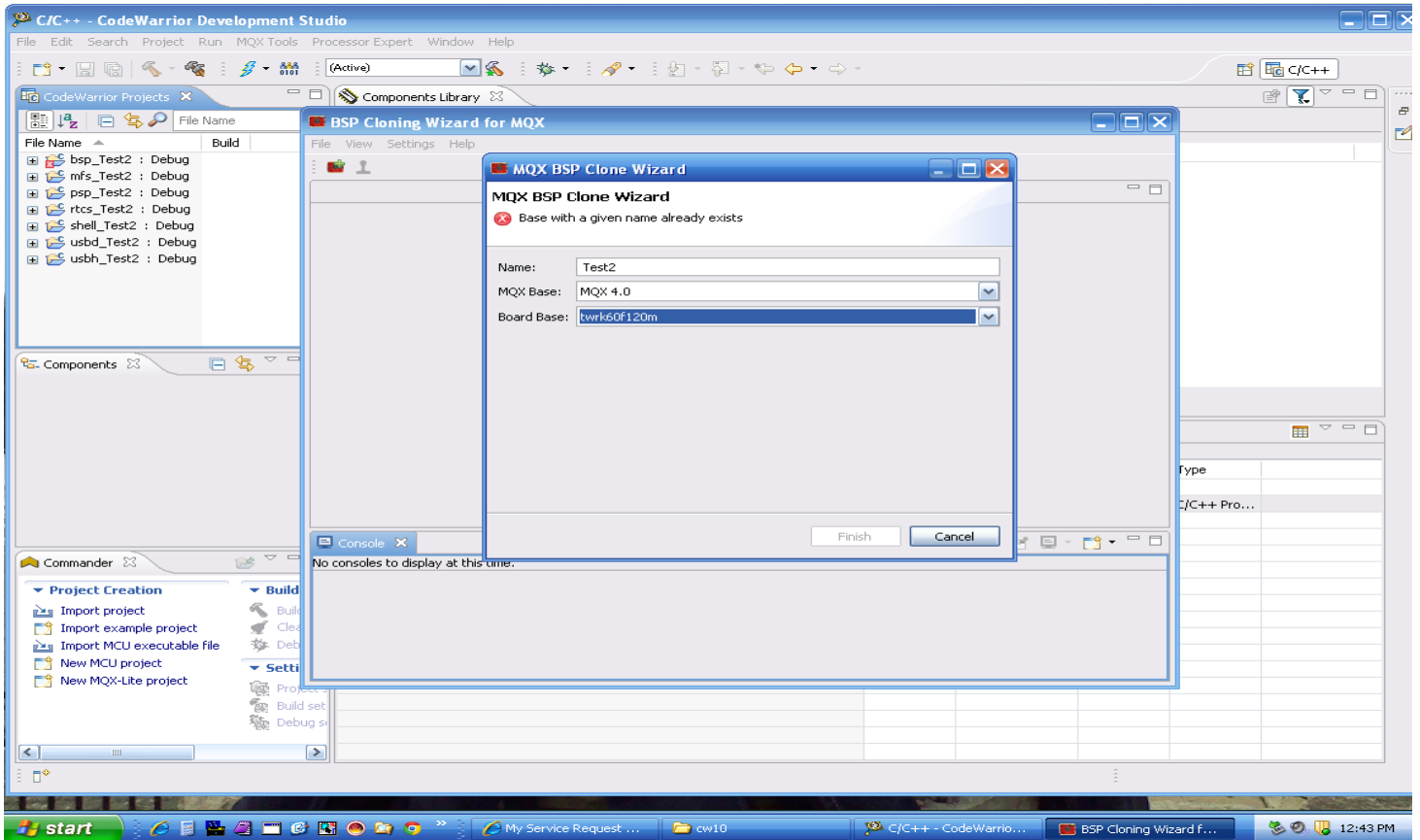


So I created a BSP called Test2 using the MQX BSP Clone Wizard.



As you can see I imported the BSP into my workspace. Since it was an exact clone the BSP compiled fine. I then followed the “How to Change Default Clock Settings in Kinetis BSP” guide. Doing the following...

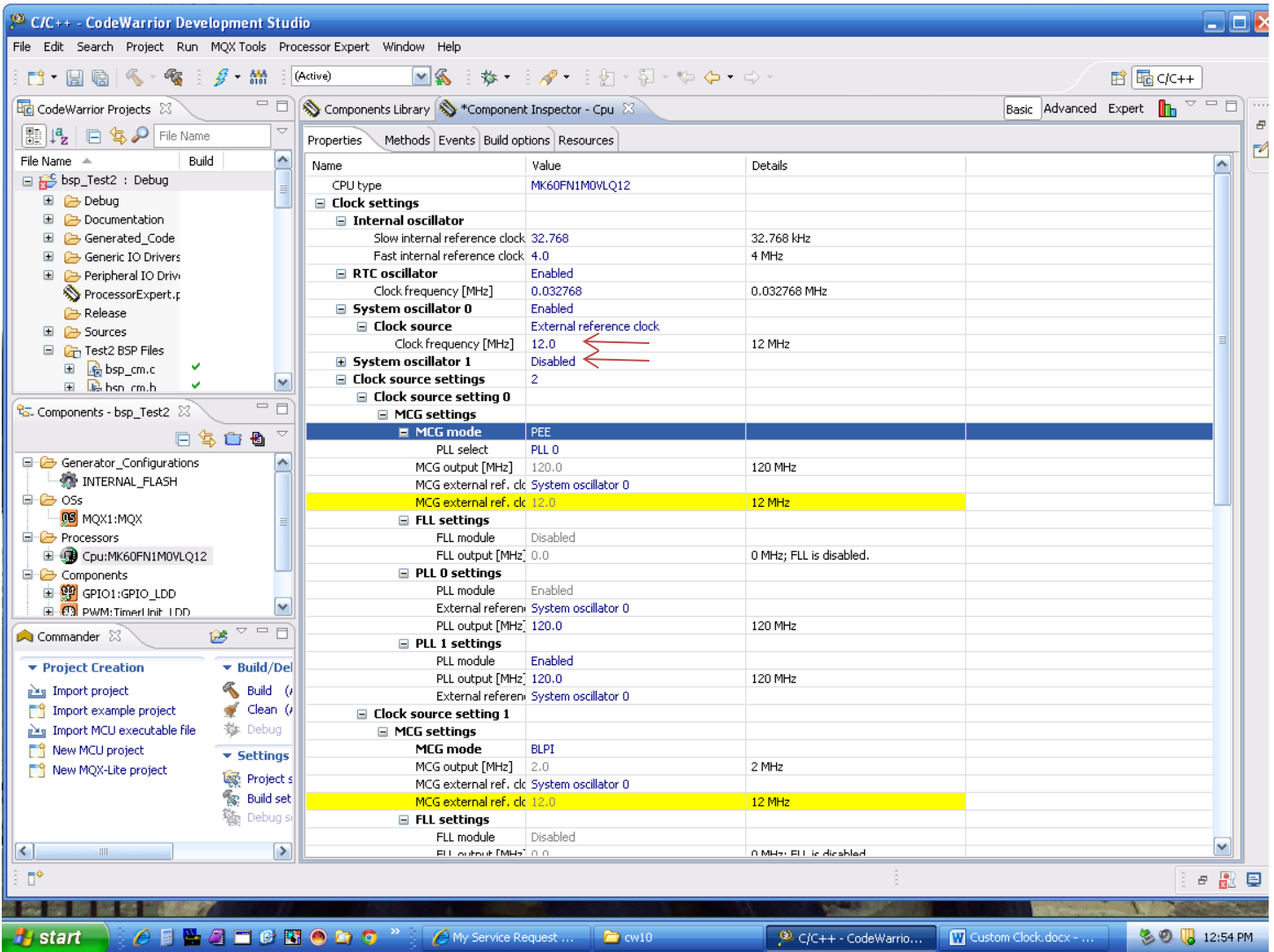
I opened the PE component inspector...

The screenshot shows the CodeWarrior Development Studio interface with the PE component inspector open. The main window displays a table of properties for the selected component (CPU type: MK60FN1M0VLQ12). The properties are organized into several sections:

Name	Value	Details
CPU type	MK60FN1M0VLQ12	
Internal oscillator		
Slow internal reference clock	32.768	32.768 kHz
Fast internal reference clock	4.0	4 MHz
RTC oscillator	Enabled	
Clock frequency [MHz]	0.032768	0.032768 MHz
System oscillator 0	Enabled	
Clock source	External reference clock	
Clock frequency [MHz]	50.0	50 MHz
System oscillator 1	Enabled	
Clock source	External crystal	
Clock frequency [MHz]	12.0	12 MHz
Clock source settings		
Clock source setting 0		
MCG settings		
MCG mode	PEE	
PLL select	PLL 0	
MCG output [MHz]	120.0	120 MHz
MCG external ref. clc	System oscillator 0	
MCG external ref. clc	50.0	50 MHz
FLL settings		
FLL module	Disabled	
FLL output [MHz]	0.0	0 MHz; FLL is disabled.
PLL 0 settings		
PLL module	Enabled	
External referenc	System oscillator 0	
PLL output [MHz]	120.0	120 MHz
PLL 1 settings		
PLL module	Enabled	
PLL output [MHz]	120.0	120 MHz
External referenc	System oscillator 0	
Clock source setting 1		
MCG settings		
MCG mode	BLPI	
MCG output [MHz]	2.0	2 MHz
MCG external ref. clc	System oscillator 0	
MCG external ref. clc	50.0	50 MHz
FLL settings		

The interface also shows a project tree on the left with 'Cpu:MK60FN1M0VLQ12' selected, and a 'Commander' window at the bottom left with project creation and build options.

I changed two settings...



I changed my clock setting from 50MHz to 12MHz and Disabled my "System Oscillator 1."

As you can see from the print screens no errors.

The screenshot displays the CodeWarrior Development Studio interface. The main window shows the Component Inspector for the CPU component, with the 'Resources' tab selected. The table below lists the properties and their values:

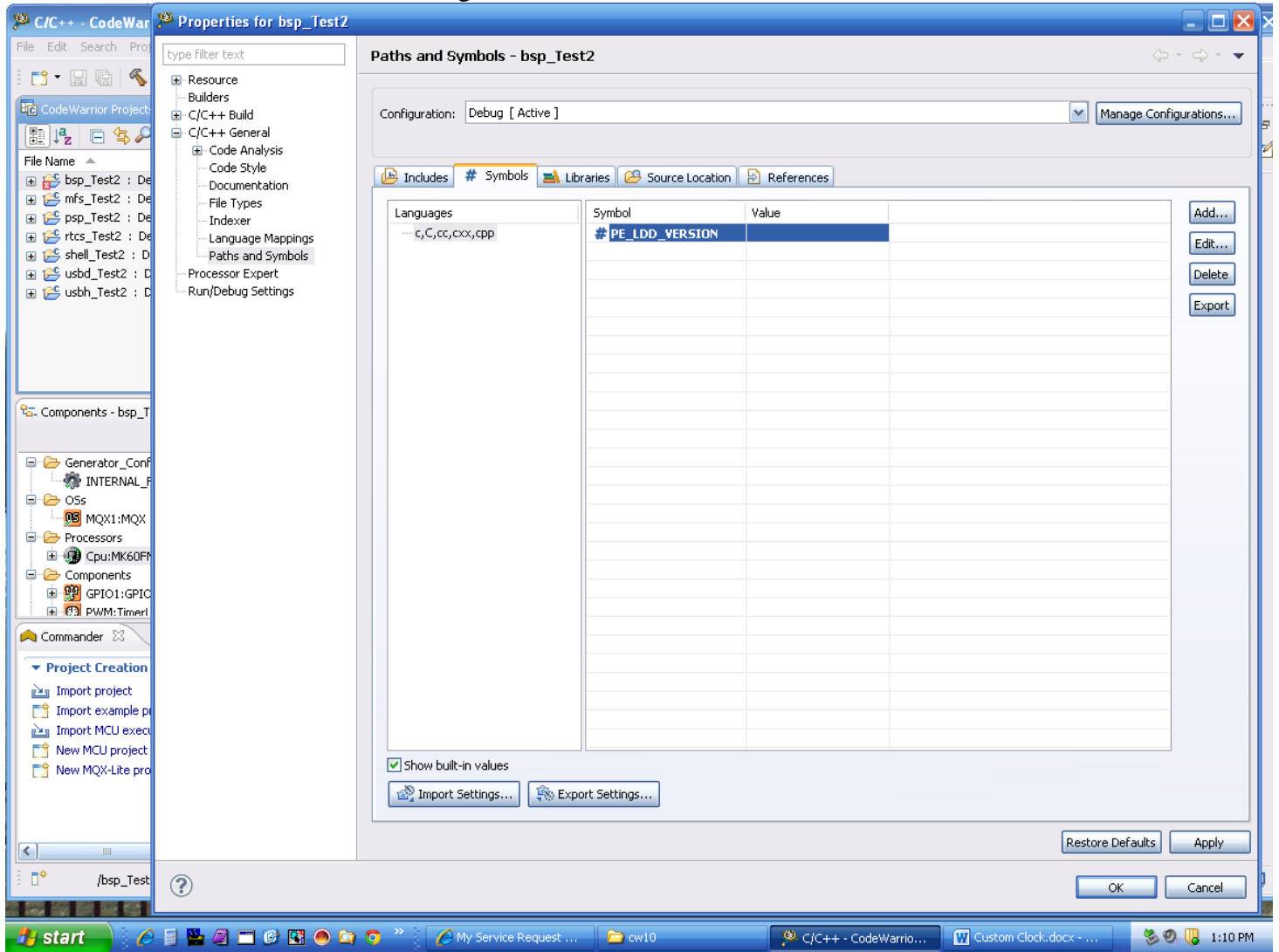
Name	Value	Details
FLL output [MHz]	0.0	0 MHz; FLL is disabled.
PLL 0 settings		
PLL module	Disabled	
External reference	System oscillator 0	
PLL output [MHz]	0.0	0 MHz; PLL is disabled
PLL 1 settings		
PLL module	Disabled	
PLL output [MHz]	0.0	0 MHz; PLL is disabled
External reference	System oscillator 0	
Initialization priority	minimal priority	15
Watchdog disable	yes	
CPU interrupts/resets		
External Bus	Disabled	
Clock configurations	3	
Clock configuration 0		
Clock source setting	configuration 0	
MCG mode	PEE	
System clocks		
Core clock	120.0	120 MHz
Bus clock	60.0	60 MHz
External bus clock	40.0	40 MHz
Flash clock	20.0	20 MHz
Clock configuration 1		
Clock source setting	configuration 0	
MCG mode	PEE	
System clocks		
Core clock	12.0	12 MHz
Bus clock	12.0	12 MHz
External bus clock	12.0	12 MHz
Flash clock	12.0	12 MHz
Clock configuration 2		
Clock source setting	configuration 1	
MCG mode	BLPI	
System clocks		
Core clock	2.0	2 MHz
Bus clock	2.0	2 MHz
External bus clock	2.0	2 MHz
Flash clock	0.5	0.5 MHz

Next I generate Processor Expert Code...

The screenshot shows the CodeWarrior Development Studio interface. The 'Process' context menu is open, and the 'Generate Processor Expert Code' option is highlighted. The background window, 'Component Inspector - Cpu', displays the following data:

Name	Value	Details
FLL output [MHz]	0.0	0 MHz; FLL is disabled.
PLL 0 settings		
PLL module	Disabled	
External reference	System oscillator 0	
PLL output [MHz]	0.0	0 MHz; PLL is disabled
PLL 1 settings		
PLL module	Disabled	
PLL output [MHz]	0.0	0 MHz; PLL is disabled
External reference	System oscillator 0	
priority	minimal priority	15
ble	yes	
ts/resets	Disabled	
ations	3	
figuration 0		
source setting	configuration 0	
G mode	PEE	
n clocks		
ie clock	120.0	120 MHz
i clock	60.0	60 MHz
ernal bus clock	40.0	40 MHz
sh clock	20.0	20 MHz
figuration 1		
source setting	configuration 0	
G mode	PEE	
n clocks		
ie clock	12.0	12 MHz
i clock	12.0	12 MHz
ernal bus clock	12.0	12 MHz
sh clock	12.0	12 MHz
figuration 2		
source setting	configuration 1	
G mode	BLPI	
n clocks		
ie clock	2.0	2 MHz
i clock	2.0	2 MHz
ernal bus clock	2.0	2 MHz
sh clock	0.5	0.5 MHz

I define PE_LDD_VERSION to use the generated code.



As I said before in the Service Request...

I didn't change anything in my BSP_CLOCK_CONFIGURATION enumeration because I'm not sure what to change in the bsp_cm.h.

```

109 /* CPU frequencies in clock configuration 2 */
110 #define CPU_CLOCK_CONFIG_2          0x02U /* Clock configuration 2 identifier */
111 #define CPU_CORE_CLK_HZ_CONFIG_2    2000000UL /* Core clock frequency in clock configuration 2 */
112 #define CPU_BUS_CLK_HZ_CONFIG_2     2000000UL /* Bus clock frequency in clock configuration 2 */
113 #define CPU_FLEXBUS_CLK_HZ_CONFIG_2 2000000UL /* Flexbus clock frequency in clock configuration 2 */
114 #define CPU_FLASH_CLK_HZ_CONFIG_2   500000UL /* FLASH clock frequency in clock configuration 2 */
115 #define CPU_USB_CLK_HZ_CONFIG_2     0UL /* USB clock frequency in clock configuration 2 */
116 #define CPU_PLL_FLL_CLK_HZ_CONFIG_2 2000000UL /* PLL/FLL clock frequency in clock configuration 2 */
117 #define CPU_MCGIR_CLK_HZ_CONFIG_2   2000000UL /* MCG internal reference clock frequency in clock configuration 2 */
118 #define CPU_OSCER_CLK_HZ_CONFIG_2   50000000UL /* System OSC external reference clock frequency in clock configuration 2 */
119 #define CPU_ERCLK32K_CLK_HZ_CONFIG_2 0UL /* External reference clock 32k frequency in clock configuration 2 */
120 #define CPU_MCGFF_CLK_HZ_CONFIG_2   16384UL /* MCG fixed frequency clock */
121
122 #endif /* PE_LDD_VERSION */
123
124
125 typedef enum {
126     BSP_CLOCK_CONFIGURATION_0 = 0, /* 120 MHz PEE */
127     BSP_CLOCK_CONFIGURATION_1, /* 12 MHz PEE */
128     BSP_CLOCK_CONFIGURATION_2, /* 2 MHz BLPI */
129     BSP_CLOCK_CONFIGURATIONS, /* Number of available clock configurations */
130     BSP_CLOCK_CONFIGURATION_DEFAULT = BSP_CLOCK_CONFIGURATION_0,
131     BSP_CLOCK_CONFIGURATION_120MHZ = BSP_CLOCK_CONFIGURATION_0,
132     BSP_CLOCK_CONFIGURATION_12MHZ = BSP_CLOCK_CONFIGURATION_1,
133     BSP_CLOCK_CONFIGURATION_2MHZ = BSP_CLOCK_CONFIGURATION_2,
134     BSP_CLOCK_CONFIGURATION_AUTOTRIM = BSP_CLOCK_CONFIGURATION_1
135 } BSP_CLOCK_CONFIGURATION;
136
137 #define Cpu_SetOperationMode_METHOD_ENABLED
138
139
140 #ifndef __cplusplus
141 extern "C" {
142 #endif
143
144
145 void _bsp_initialize_hardware
146 {
147     void

```

So I compile my BSP layer and now I have 6 errors.

