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Revision History

Rev	
X1	TWR-LS1021A draft revision for interposer(P1010 to LS1021A) and LS1021A/LS1020A silicon
A	TWR-LS1021A first release for interposer(P1010 to LS1021A) and LS1021A/LS1020A silicon
B	1. Add 96MHz clock to SYSCLK. 2. Connect 96MHz CLK to CLK12 by resistors. 3. Change OpenSDA power supply from USB port. 4. LVDD change to fixed 2.5V. 5. Add J19, J20 to select UART1 or LPUART1 to K20 MCU.
C1	1. R291 change to pullup. 2. Change R306 to DNP and R307 to be populated. 3. Change U33 to QFN package and place near J12. 4. Add C416 22pF near J12.4pin 5. Change R305 to 200ohm. 6. QSPI flash signal mux with NOR. 7. LVDD&L1VDD output support 2.5V/3.3V. Add Q1 to select LVDD&L1VDD voltage. 8. Add R398 external pullup for EVT0. 9. Change Asleep LED driven circuit. 10. Update MBED reset circuit 11. Add TP4 for PORESET 12. CPLD swap pins for layout
C2	1. De-populated C416. 2. Change R399 to 82Kohm. *Note: revC2 is equal to revC1+TDA5025+TDA5014
D	1. Use LTC3561 replace LTC3080 LDO for USB HUB 2. Add a cap location for QSPI D0
D1	1. Change C425(22pF) from DNP to populated.

TWR-LS1021A

Revisions

Rev	Description	Date	Approved
X1	Original Release	Nov 11, 2013	TOM SUN
A	Formal Release	Jan 16, 2014	TOM SUN
B	For revB Release	Mar 24, 2014	TOM SUN
C1	For revC1 Release	May 20, 2014	TOM SUN
C2	For revC2 Release	Jul 30, 2014	TOM SUN
D	For revD Release	Aug 28, 2014	TOM SUN
D1	For revD1 Release	Oct 24, 2014	TOM SUN

freescale™

Digital Networking Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: FCP: FIUO: PUBI: X

Designer: Paul Gan	Drawing Title: TWR-LS1021A	
Drawn by: Paul Gan	Page Title: COVER PAGE	
Approved: Tom Sun	Size C	Document Number SCH-28040 PDF: SPF-28040 Rev D1
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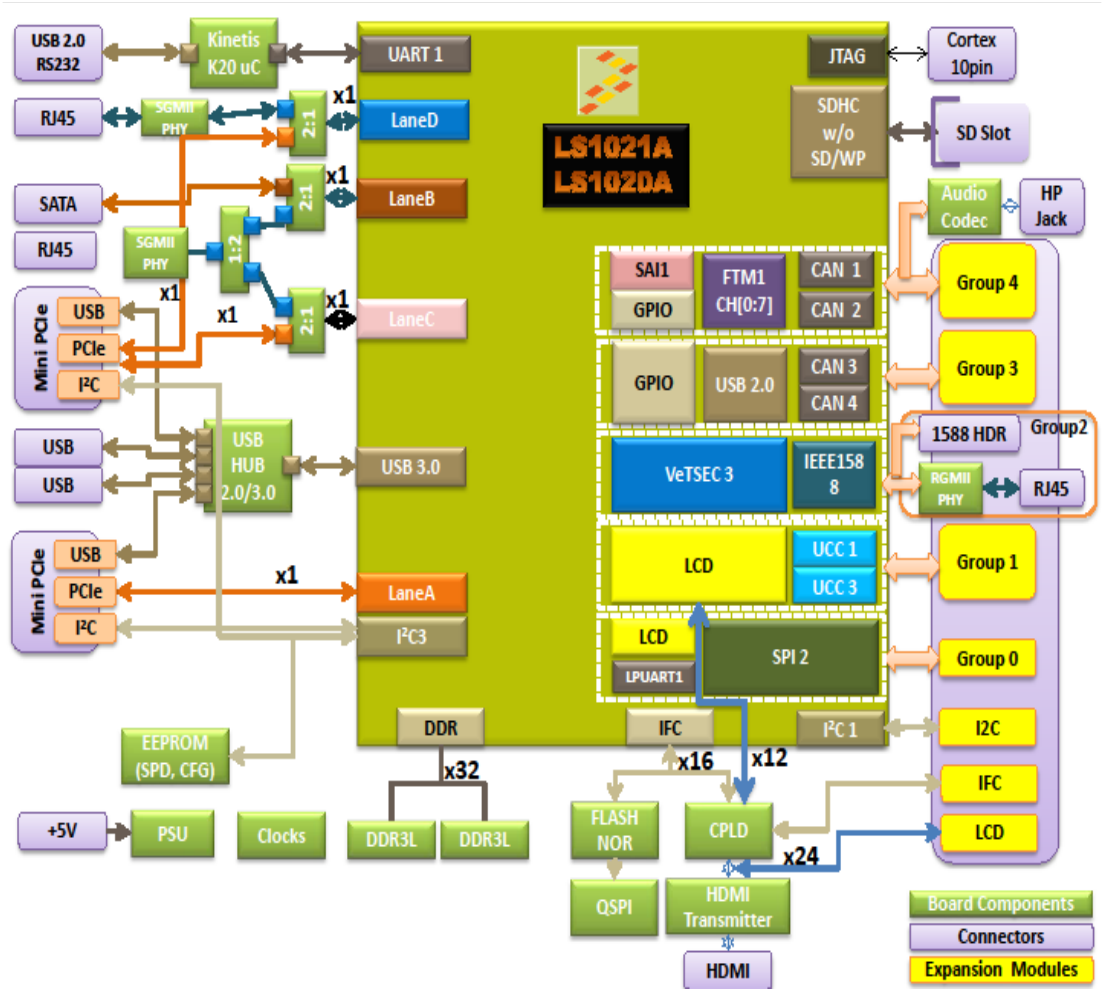
1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/8 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted Lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.



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ICAP Classification: FCP: ___ FIUO: PUBI: X

Drawing Title: TWR-LS1021A

Page Title: NOTES

Size	Document Number	Rev
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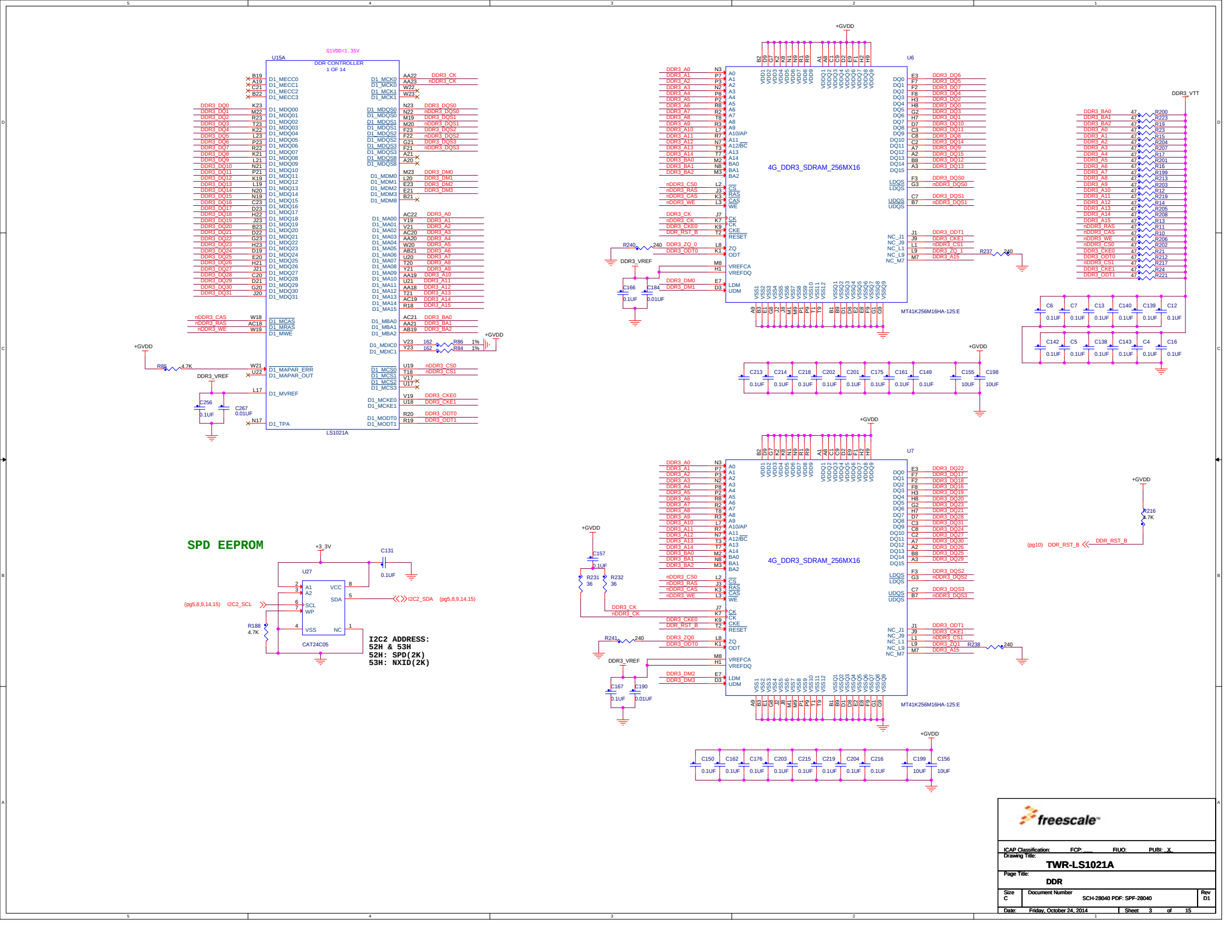
Date: Friday, October 24, 2014 Sheet 2 of 15


G1VDD=1.35V
U15A
DDR CONTROLLER
1 OF 14
LS1021A
D1_MECC0
D1_MECC1
D1_MECC2
D1_MECC3
D1_MDQ00
D1_MDQ01
D1_MDQ02
D1_MDQ03
D1_MDQ04
D1_MDQ05
D1_MDQ06
D1_MDQ07
D1_MDQ08
D1_MDQ09
D1_MDQ10
D1_MDQ11
D1_MDQ12
D1_MDQ13
D1_MDQ14
D1_MDQ15
D1_MDQ16
D1_MDQ17
D1_MDQ18
D1_MDQ19
D1_MDQ20
D1_MDQ21
D1_MDQ22
D1_MDQ23
D1_MDQ24
D1_MDQ25
D1_MDQ26
D1_MDQ27
D1_MDQ28
D1_MDQ29
D1_MDQ30
D1_MDQ31
D1_MCAS
D1_MRAS
D1_MWE
D1_MAPAR_ERR
D1_MAPAR_OUT
D1_MVREF
D1_TPA
D1_MCK0
D1_MCK1
D1_MDQS0
D1_MDQS1
D1_MDQS2
D1_MDQS3
D1_MDQS8
D1_MDM0
D1_MDM1
D1_MDM2
D1_MDM3
D1_MDM8
D1_MA00
D1_MA01
D1_MA02
D1_MA03
D1_MA04
D1_MA05
D1_MA06
D1_MA07
D1_MA08
D1_MA09
D1_MA10
D1_MA11
D1_MA12
D1_MA13
D1_MA14
D1_MA15
D1_MBA0
D1_MBA1
D1_MBA2
D1_MDIC0
D1_MDIC1
D1_MCS0
D1_MCS1
D1_MCS2
D1_MCS3
D1_MCKE0
D1_MCKE1
D1_MODT0
D1_MODT1
DDR3_CK
nDDR3_CK
DDR3_DQS0
nDDR3_DQS0
DDR3_DQS1
nDDR3_DQS1
DDR3_DM0
DDR3_DM1
DDR3_DQS2
nDDR3_DQS2
DDR3_DQS3
nDDR3_DQS3
DDR3_DM2
DDR3_DM3
DDR3_A0
DDR3_A1
DDR3_A2
DDR3_A3
DDR3_A4
DDR3_A5
DDR3_A6
DDR3_A7
DDR3_A8
DDR3_A9
DDR3_A10
DDR3_A11
DDR3_A12
DDR3_A13
DDR3_A14
DDR3_A15
DDR3_BA0
DDR3_BA1
DDR3_BA2
DDR3_CS0
nDDR3_CS1
DDR3_CKE0
DDR3_CKE1
DDR3_ODT0
DDR3_ODT1
nDDR3_CAS
nDDR3_RAS
nDDR3_WE
+GVDD
R85 4.7K
DDR3_VREF
C256 0.1UF
C267 0.01UF
R86 1%
R84 1%
SPD EEPROM
+3_3V
U27
C131 0.1UF
A1
A2
SCL
WP
VSS
VCC
SDA
NC
CAT24C05
R188 4.7K
(pg5,8,9,14,15) I2C2_SCL
I2C2_SDA (pg5,8,9,14,15)
I2C2 ADDRESS:
52H & 53H
52H: SPD(2K)
53H: NXID(2K)
U6
U7
4G_DDR3_SDRAM_256MX16
MT41K256M16HA-125:E
R240 240
R237 240
R238 240
R241 240
R232 36
R231 36
C157 0.1UF
C166 0.1UF
C184 0.01UF
C167 0.1UF
C190 0.01UF
C213 C214 C218 C202 C201 C175 C161 C149 0.1UF
C155 C198 10UF
C150 C162 C176 C203 C215 C219 C204 C216 0.1UF
C199 C156 10UF
DDR3_VTT
R200 R223 R19 R23 R15 R204 R207 R17 R201 R16 R199 R213 R203 R12 R219 R14 R205 R208 R13 R11 R10 R206 R202 R21 R212 R217 R24 R221 47
C6 C7 C13 C140 C139 C12 C142 C5 C138 C143 C4 C16 0.1UF
R216 4.7K
(pg10) DDR_RST_B
DDR_RST_B
freescale
ICAP Classification: FCP: ___ FIUO: PUBI: X
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Page Title: DDR
Size C
Document Number SCH-28040 PDF: SPF-28040
Rev D1
Date: Friday, October 24, 2014
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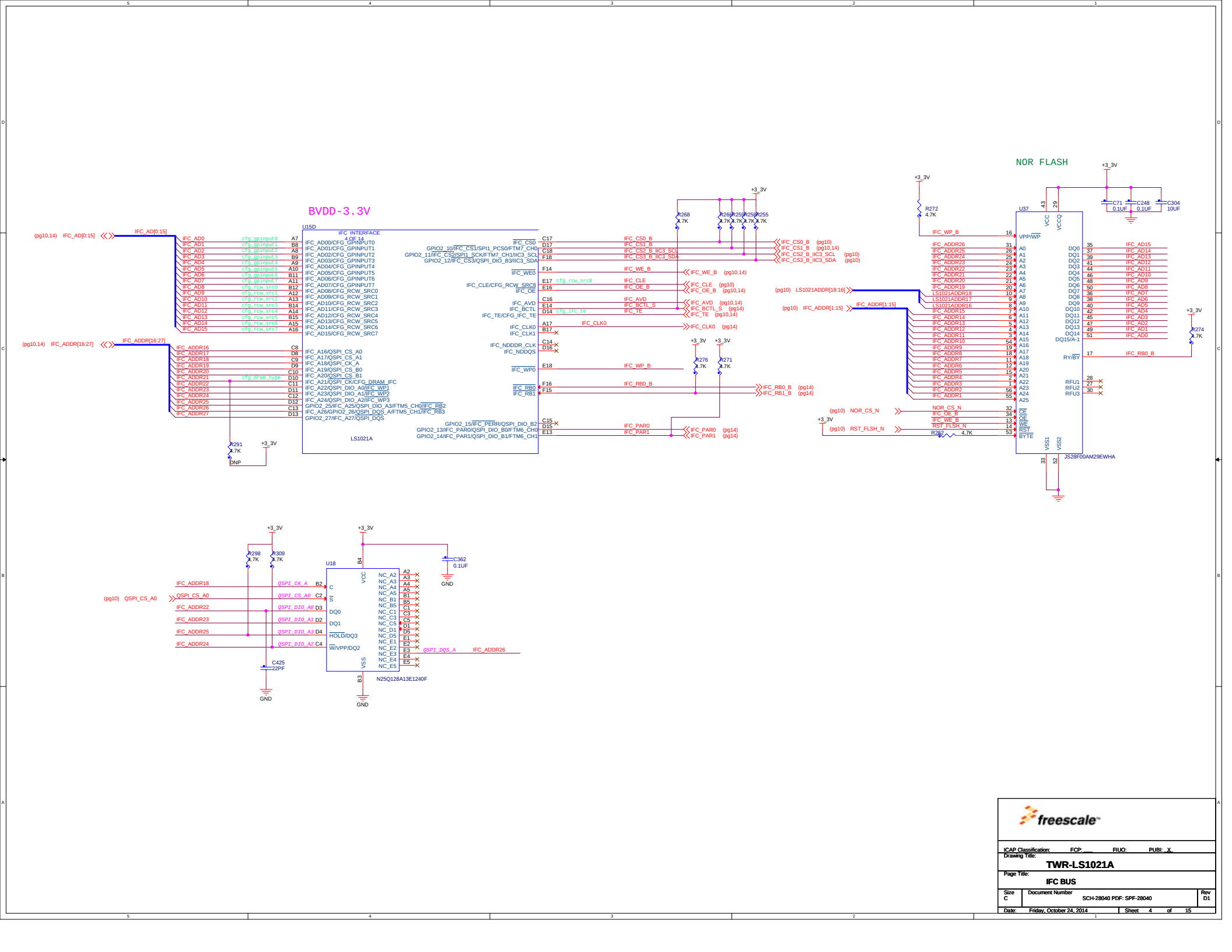

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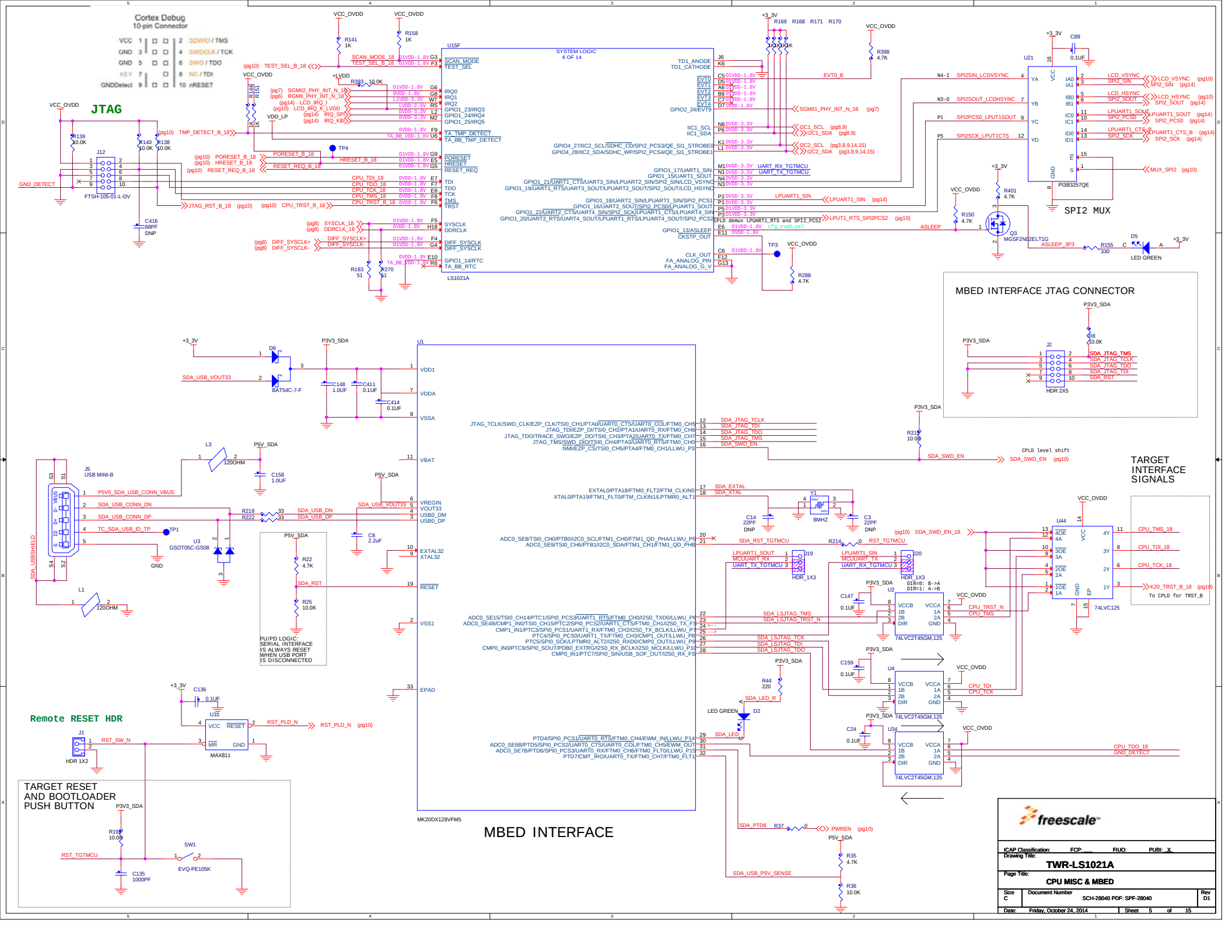
Rev: D1	
Date: Friday, October 24, 2014	Sheet 4 of 15


Cortex Debug
10-pin Connector
JTAG
MBED INTERFACE JTAG CONNECTOR
SPI2 MUX
TARGET INTERFACE SIGNALS
Remote RESET HDR
TARGET RESET AND BOOTLOADER PUSH BUTTON
MBED INTERFACE
PU/PD LOGIC: SERIAL INTERFACE IS ALWAYS RESET WHEN USB PORT IS DISCONNECTED
LS1021A
MK20DX128VFM5
freescale
ICAP Classification:
FCP:
FIUO:
PUBI: X
Drawing Title:
TWR-LS1021A
Page Title:
CPU MISC & MBED
Size C
Document Number
SCH-28040 PDF: SPF-28040
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Date: Friday, October 24, 2014
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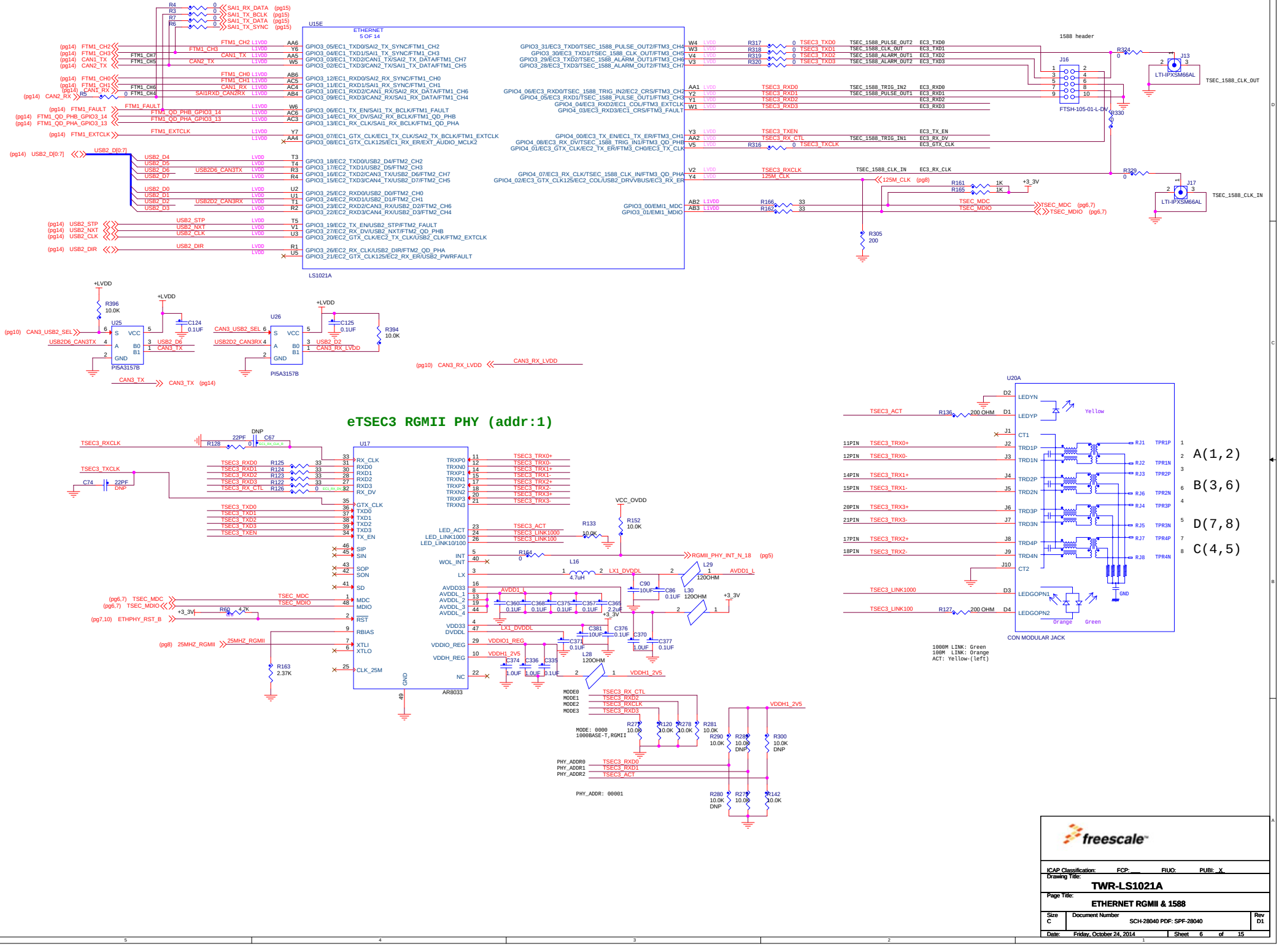
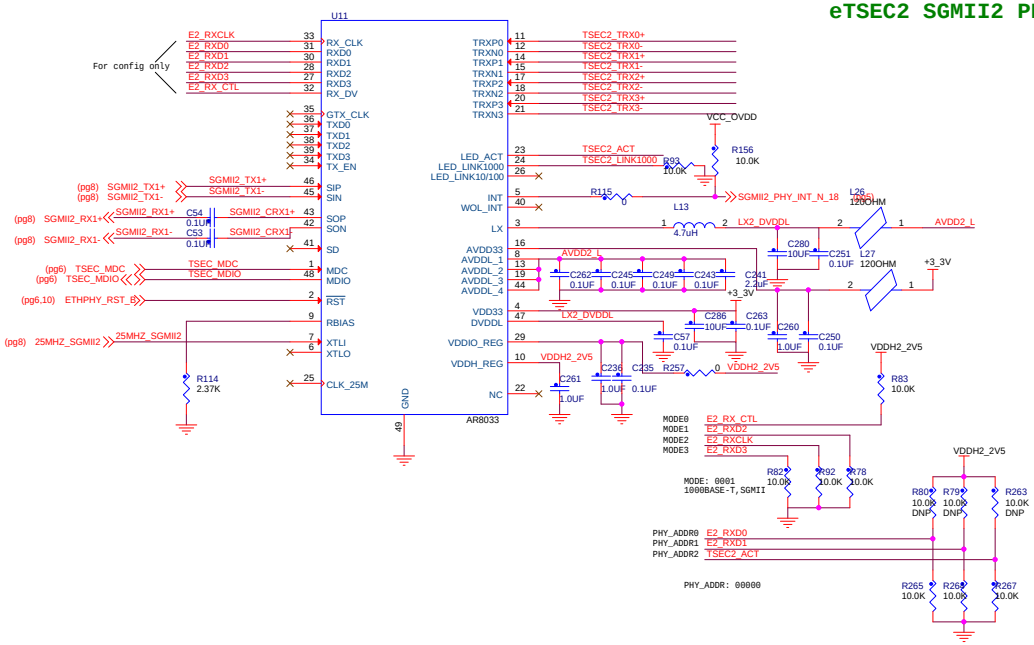
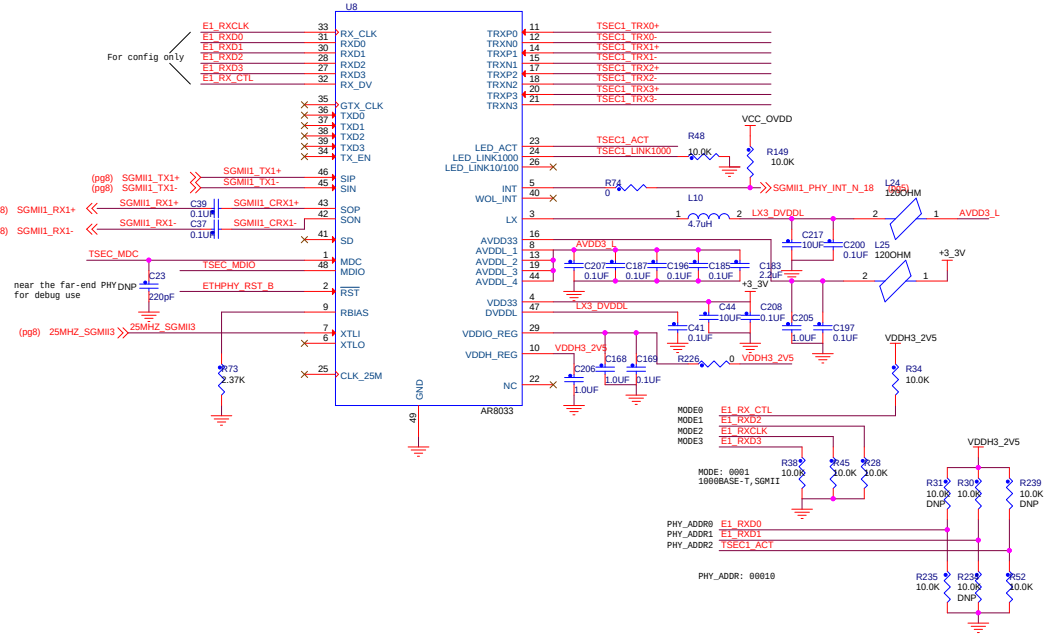

eTSEC3 RGMII PHY (addr:1)
U15E
ETHERNET
5 OF 14
LS1021A
U25
PI5A3157B
U26
PI5A3157B
U17
AR8033
U20A
CON MODULAR JACK
1588 header
A(1,2)
B(3,6)
D(7,8)
C(4,5)
1000M LINK: Green
100M LINK: Orange
ACT: Yellow-(left)
freescale
ICAP Classification:
FCP:
FIUO:
PUBI: X
Drawing Title:
TWR-LS1021A
Page Title:
ETHERNET RGMII & 1588
Size C
Document Number
SCH-28040 PDF: SPF-28040
Rev D1
Date: Friday, October 24, 2014
Sheet 6 of 15

eTSEC2 SGMII2 PHY (addr:0)



eTSEC1 SGMII1 PHY (addr:2)



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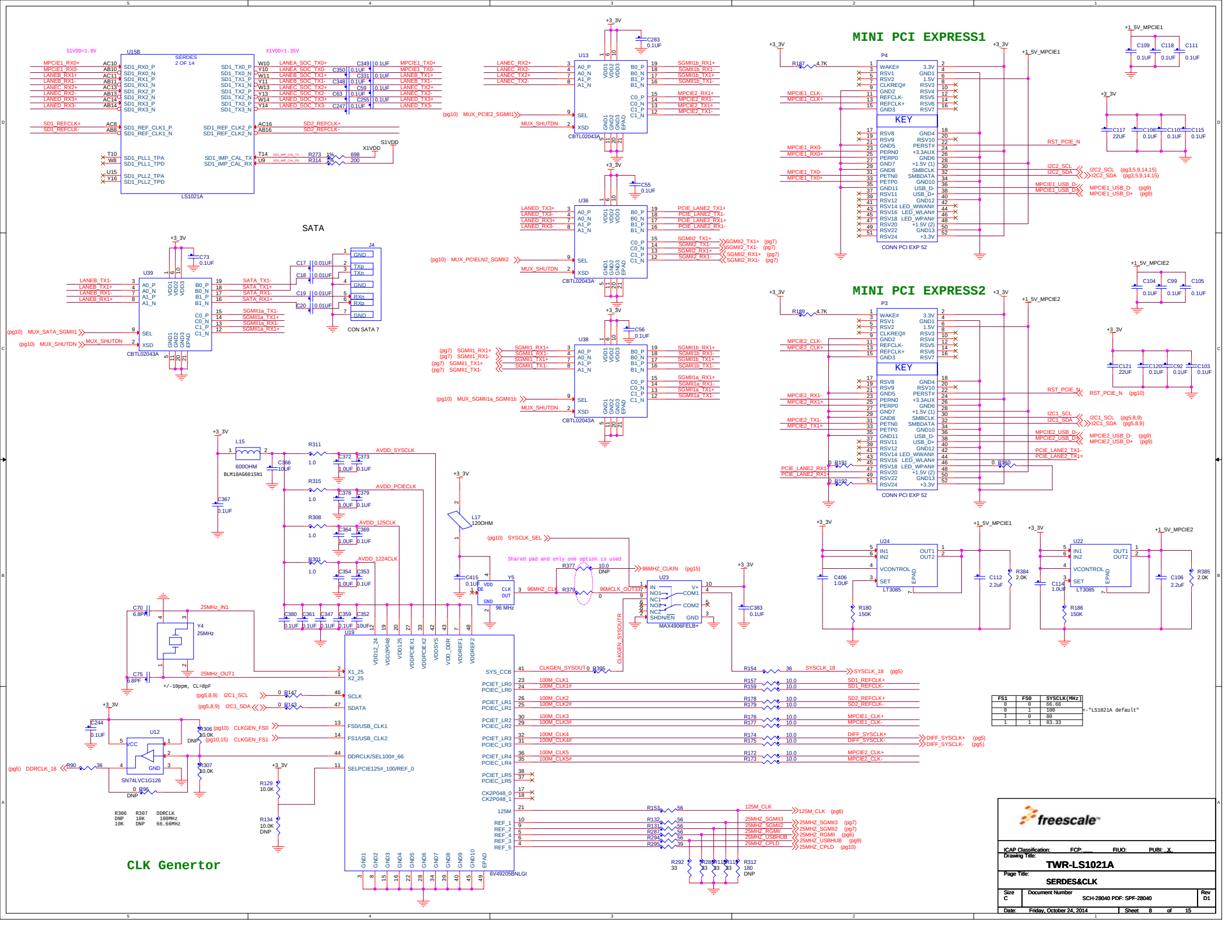
Page Title:	ETHERNET SGMII
Size: C	Document Number: SCH-28040 PDF: SPF-28040 Rev: D1
Date: Friday, October 24, 2014	Sheet 7 of 15


MINI PCI EXPRESS1
MINI PCI EXPRESS2
SATA
CLK Genertor
U15B
SERDES
2 OF 14
LS1021A
U13
U36
U39
U38
P4
P3
CONN PCI EXP 52
CON SATA 7
J4
U19
U12
U23
U24
U22
Y4
25MHz
Y5
96 MHz
L15
600OHM
BLM18AG601SN1
L17
120OHM
MAX4906FELB+
LT3085
SN74LVC1G126
6V49205BNLGI
CBTL02043A
S1VDD=1.0V
X1VDD=1.35V
S1VDD
X1VDD
+3_3V
+1_5V_MPCIE1
+1_5V_MPCIE2
AVDD_SYSCLK
AVDD_PCIECLK
AVDD_125CLK
AVDD_1224CLK
25MHz_IN1
25MHz_OUT1
+/-10ppm, CL=8pF
Shared pad and only one option is used
SYSCLK_SEL
CLKGEN_SYSOUTR
DDRCLK_18
I2C1_SCL
I2C1_SDA
CLKGEN_FS0
CLKGEN_FS1
SELPCIE125#_100/REF_0
DDRCLK/SEL100#_66
FS0/USB_CLK1
FS1/USB_CLK2
SCLK
SDATA
RST_PCIE_N
I2C2_SCL
I2C2_SDA
MPCIE1_USB_D-
MPCIE1_USB_D+
MPCIE2_USB_D-
MPCIE2_USB_D+
DIFF_SYSCLK+
DIFF_SYSCLK-
125M_CLK
25MHZ_SGMII3
25MHZ_SGMII2
25MHZ_RGMII
25MHZ_USBHUB
25MHZ_CPLD
SYSCLK_18
MUX_PCIE2_SGMII1
MUX_SHUTDN
MUX_PCIELN2_SGMII2
MUX_SATA_SGMII1
MUX_SGMII1a_SGMII1b
96MHZ_CLKIN
96MCLK_OUT337
CLKGEN_FS0
CLKGEN_FS1
FS1 FS0 SYSCLK(MHz)
0 0 66.66
0 1 100
1 0 80
1 1 83.33
<-"LS1021A default"
ICAP Classification:
FCP:
FIUO:
PUBI: X
Drawing Title:
TWR-LS1021A
Page Title:
SERDES&CLK
Size C
Document Number
SCH-28040 PDF: SPF-28040
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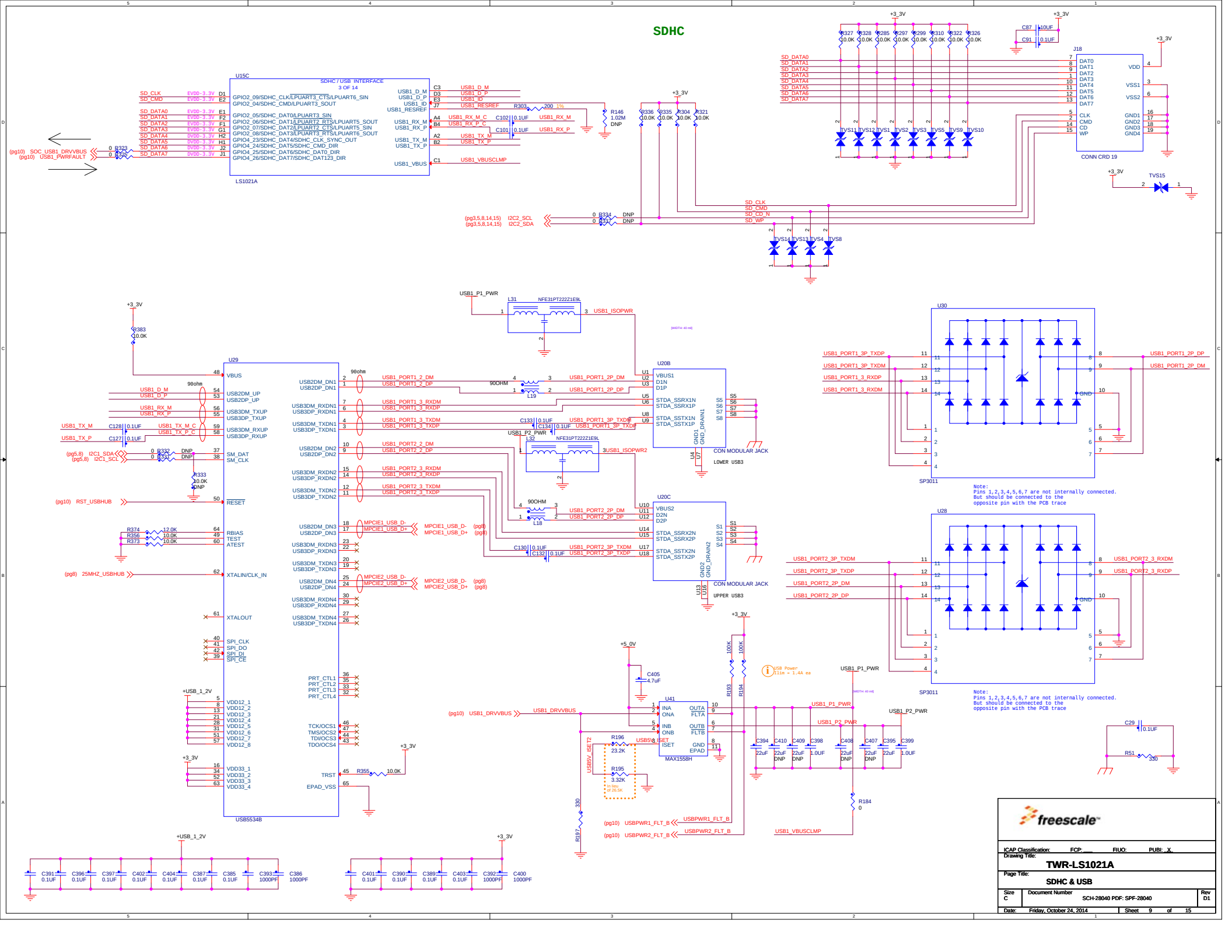
SDHC



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Drawing Title:	TWR-LS1021A
Page Title:	SDHC & USB
Size: C	Document Number: SCH-28040 PDF: SPF-28040
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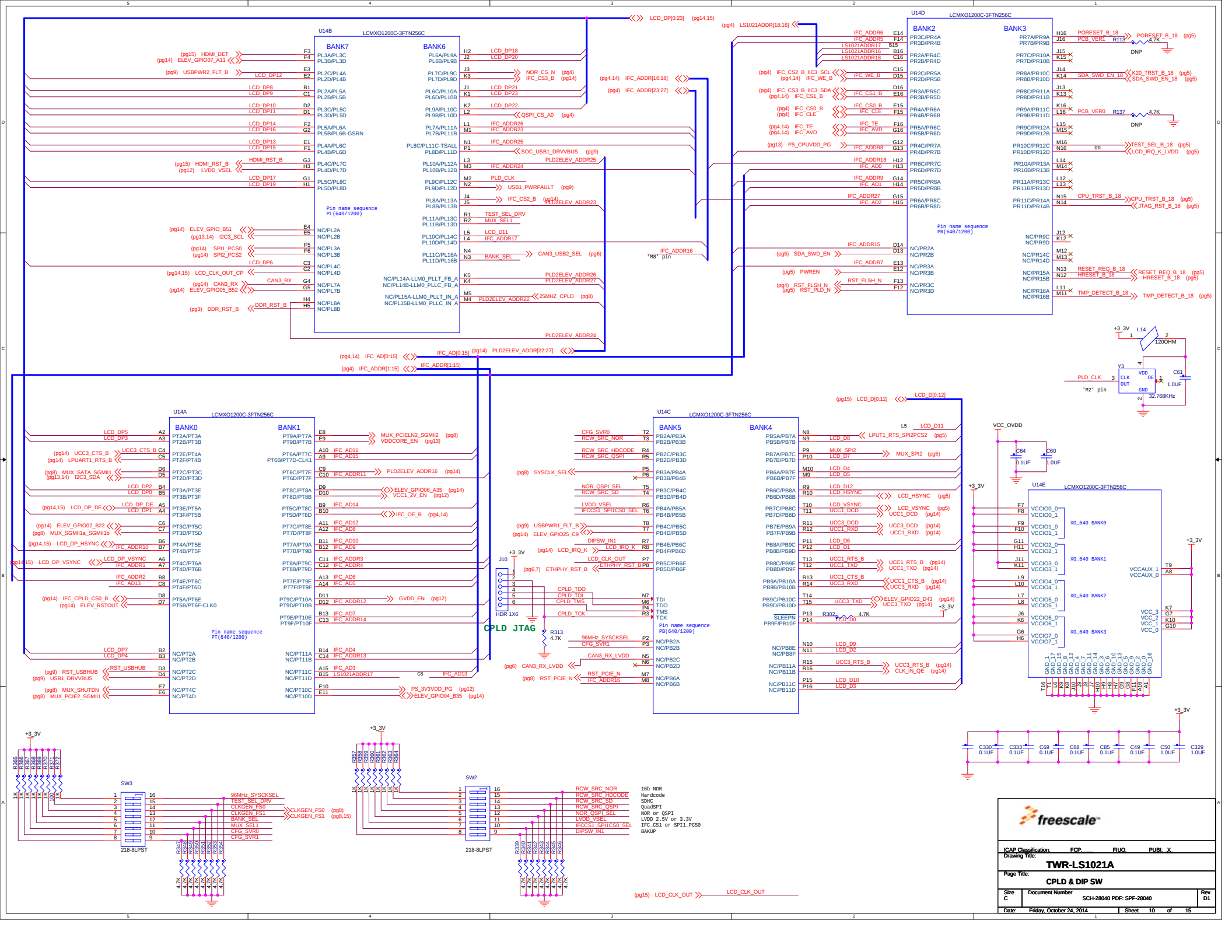
Date: Friday, October 24, 2014	Sheet 9 of 15


U14B
LCMXO1200C-3FTN256C
BANK7
BANK6
U14D
BANK2
BANK3
U14A
BANK0
BANK1
U14C
BANK5
BANK4
U14E
Pin name sequence PL(640/1200)
Pin name sequence PR(640/1200)
Pin name sequence PT(640/1200)
Pin name sequence PB(640/1200)
CPLD JTAG
HDR 1X6
SW3
SW2
218-8LPST
16b-NOR
Hardcode
SDHC
QuadSPI
NOR or QSPI
LVDD 2.5V or 3.3V
IFC_CS1 or SPI1_PCS0
BAKUP
freescale
ICAP Classification:
FCP:
FIUO:
PUBI:
Drawing Title:
TWR-LS1021A
Page Title:
CPLD & DIP SW
Size C
Document Number
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Date:
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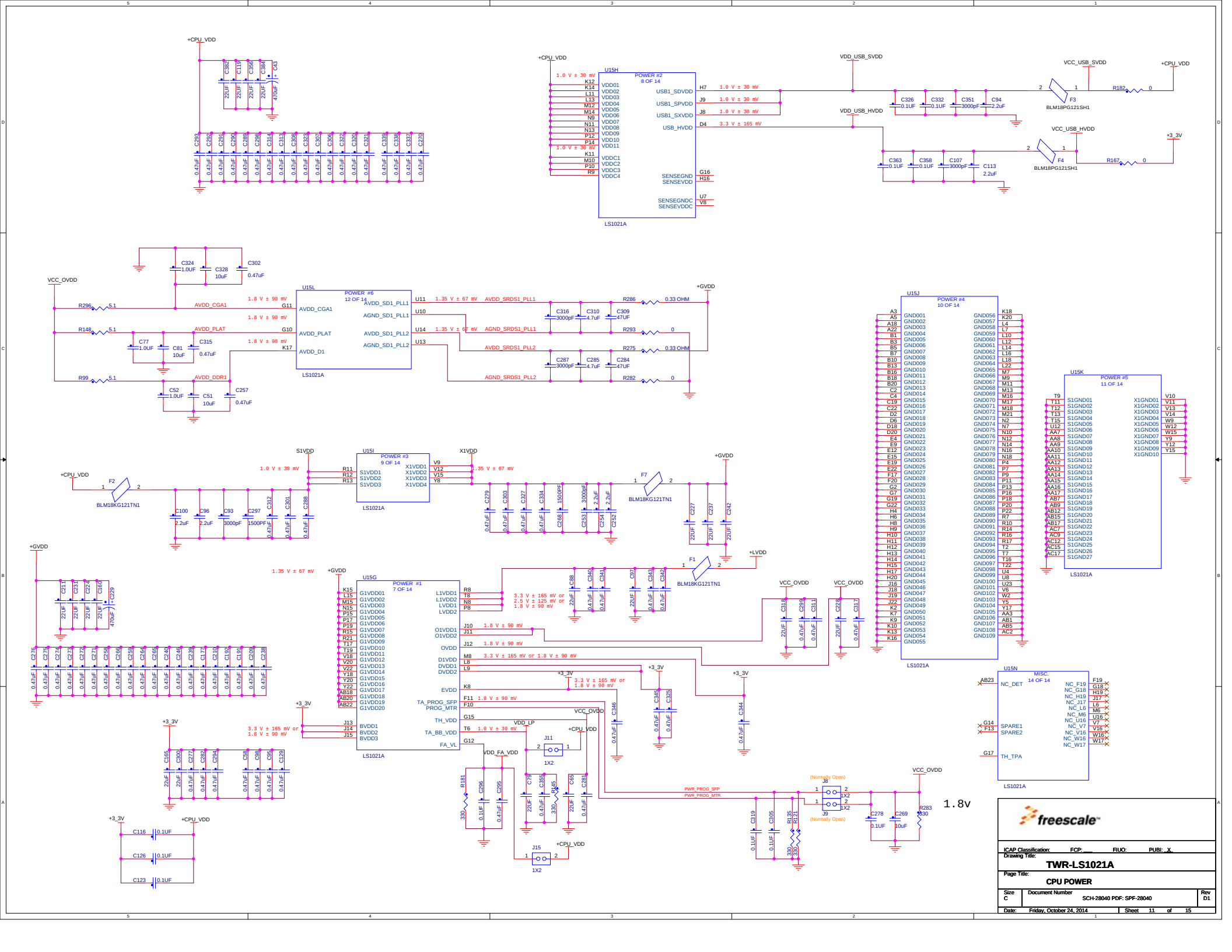

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Drawing Title:	TWR-LS1021A
Page Title:	CPU POWER
Size: C	Document Number: SCH-28040 PDF: SPF-28040
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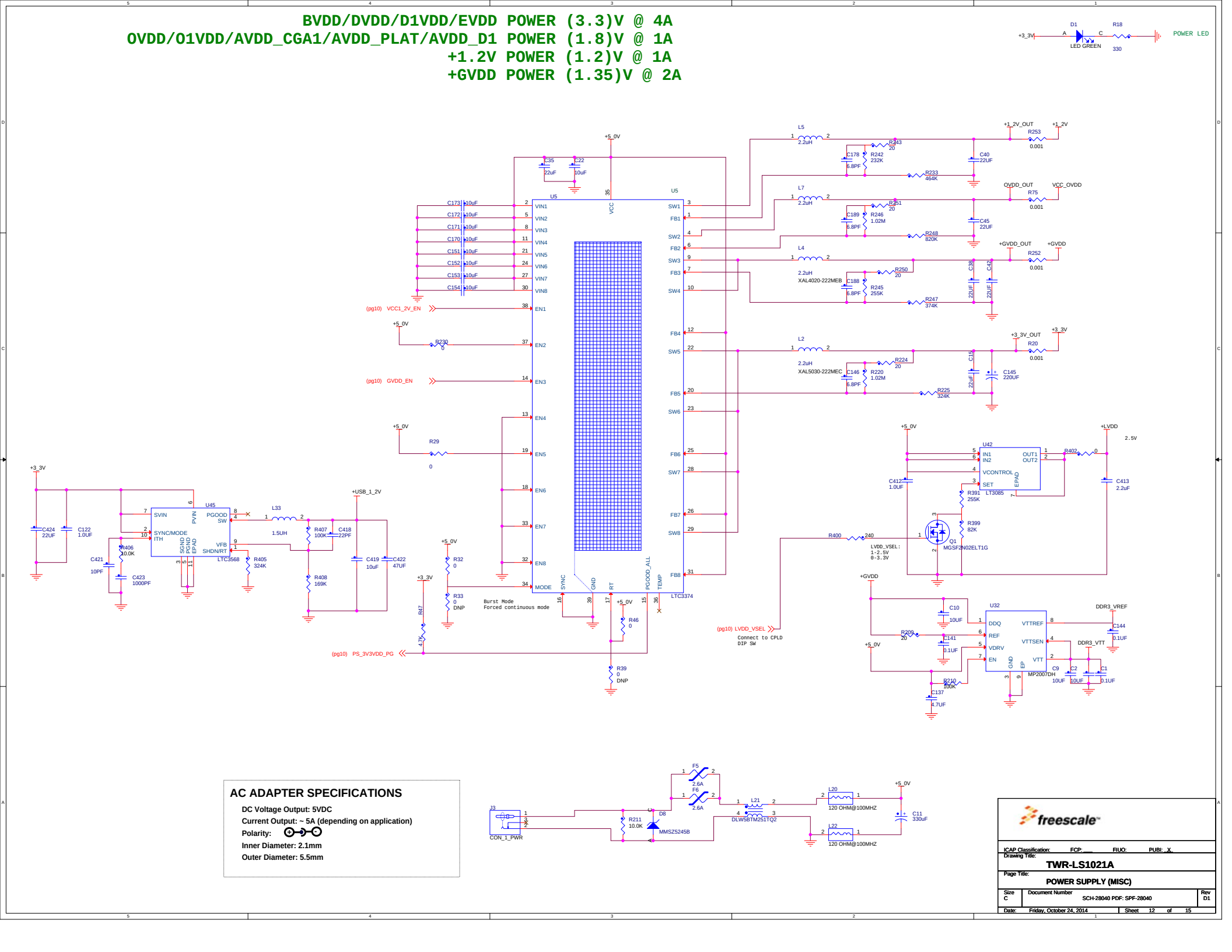
BVDD/DVDD/D1VDD/EVDD POWER (3.3)V @ 4A
OVDD/O1VDD/AVDD_CGA1/AVDD_PLAT/AVDD_D1 POWER (1.8)V @ 1A
+1.2V POWER (1.2)V @ 1A
+GVDD POWER (1.35)V @ 2A



AC ADAPTER SPECIFICATIONS

DC Voltage Output: 5VDC

Current Output: ~ 5A (depending on application)

Polarity:

Inner Diameter: 2.1mm

Outer Diameter: 5.5mm

freescale

ICAP Classification: FCP: ___ FIUO: PUBI: X

Drawing Title: **TWR-LS1021A**

Page Title: **POWER SUPPLY (MISC)**

Size	Document Number	Rev
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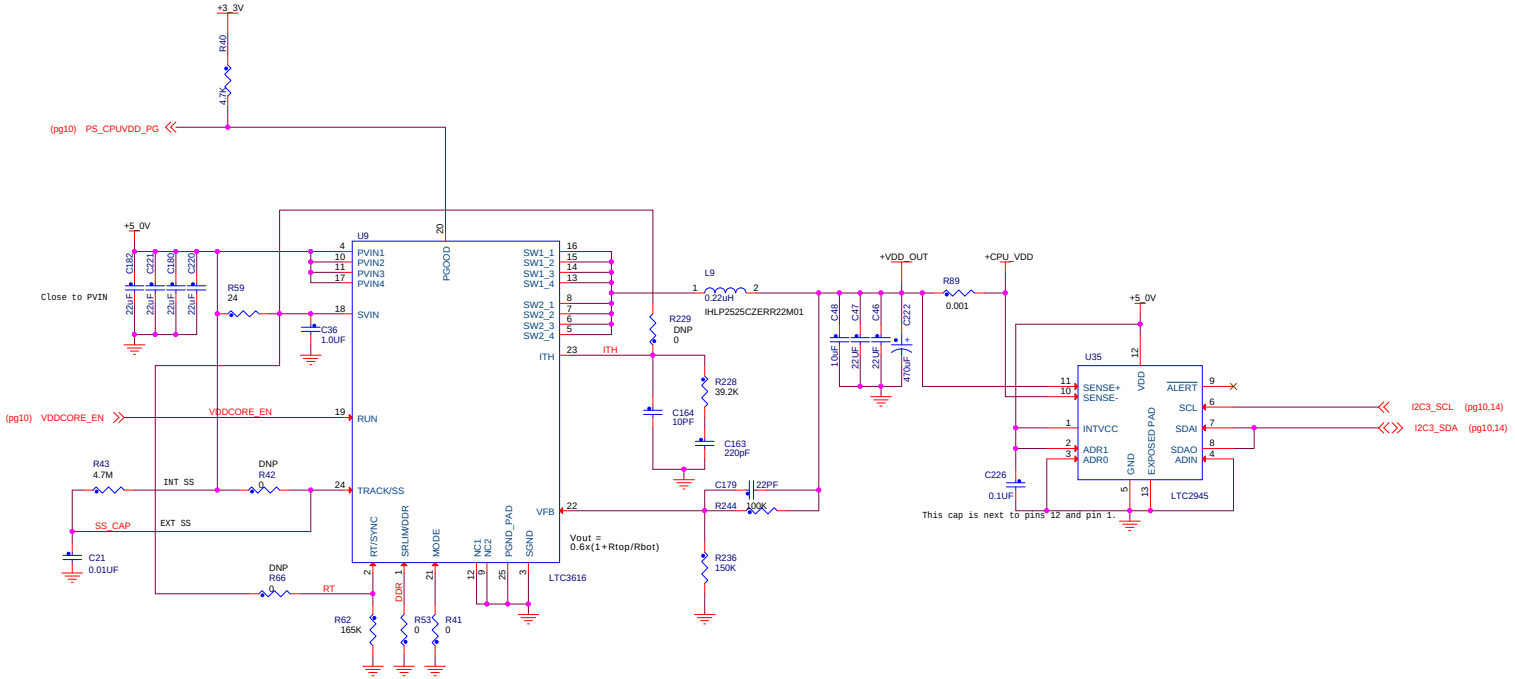
Date: Friday, October 24, 2014 Sheet 12 of 15

CPU_VDD POWER (1.0)V @ 5A



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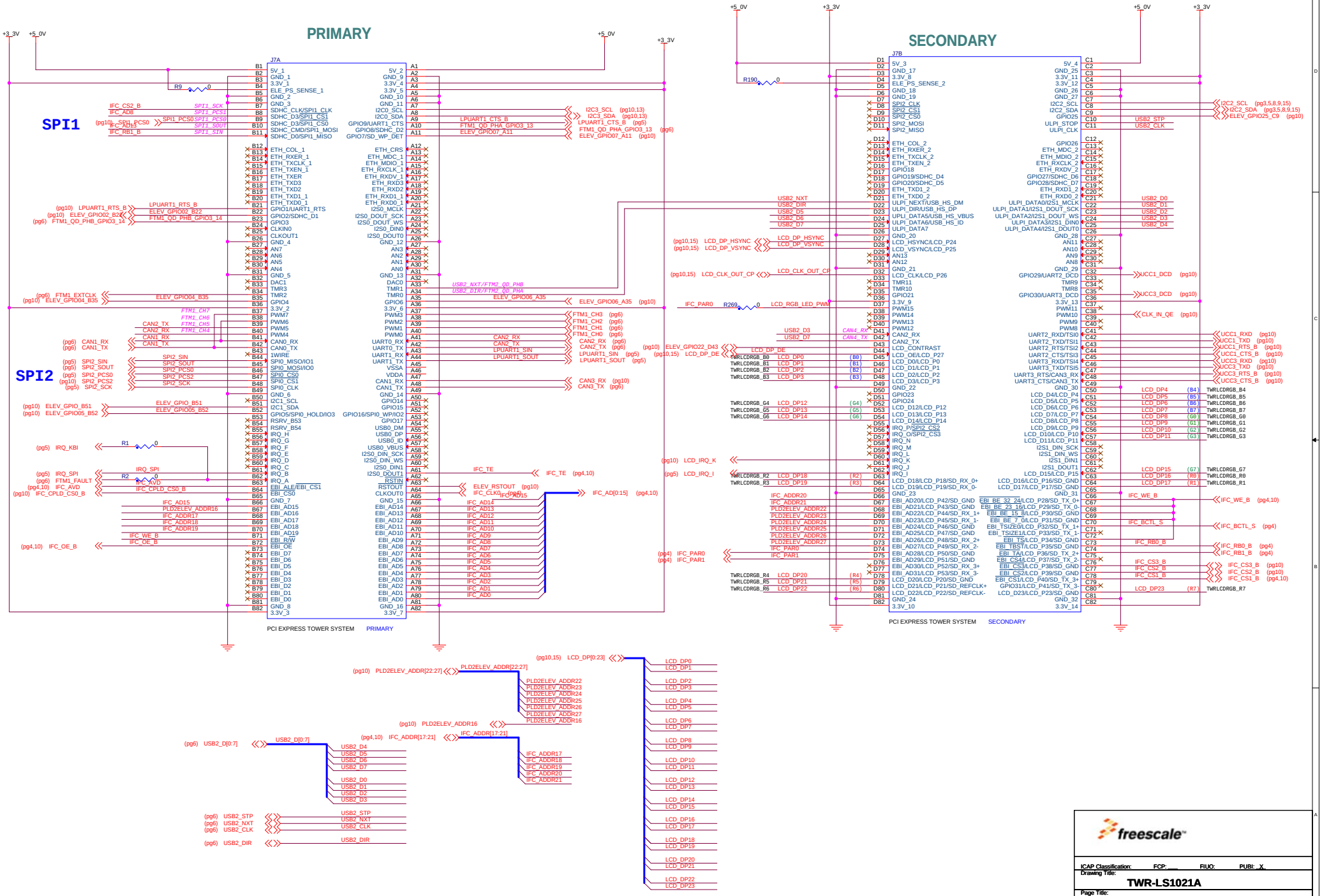
ICAP Classification: FCP: ___ FIUO: PUBI: X

Drawing Title: **TWR-LS1021A**

Page Title: **POWER SUPPLY (CORE)**

Size	Document Number	Rev
C	SCH-28040 PDF: SPF-28040	D1

Date: Friday, October 24, 2014 Sheet 13 of 15


PRIMARY
SECONDARY
SPI1
SPI2
J7A
J7B
PCI EXPRESS TOWER SYSTEM PRIMARY
PCI EXPRESS TOWER SYSTEM SECONDARY
+3_3V
+5_0V
R9 0
R190 0
R269 0
R1 0
R2 0
IFC_CS2_B
IFC_AD8
IFC_AD13
IFC_RB1_B
SPI1_SCK
SPI1_PCS1
SPI1_PCS0
SPI1_SOUT
SPI1_SIN
SDHC_CLK/SPI1_CLK
SDHC_D3/SPI1_CS1
SDHC_D3/SPI1_CS0
SDHC_CMD/SPI1_MOSI
SDHC_D0/SPI1_MISO
LPUART1_RTS_B
ELEV_GPIO02_B22
FTM1_QD_PHB_GPIO3_14
ELEV_GPIO04_B35
FTM1_CH7
FTM1_CH6
FTM1_CH5
FTM1_CH4
CAN2_TX
CAN2_RX
CAN1_RX
CAN1_TX
SPI2_SIN
SPI2_SOUT
SPI2_PCS0
SPI2_PCS2
SPI2_SCK
ELEV_GPIO_B51
ELEV_GPIO05_B52
IRQ_KBI
IRQ_SPI
IFC_FAULT
IFC_AVD
IFC_CPLD_CS0_B
IFC_AD15
PLD2ELEV_ADDR16
IFC_ADDR17
IFC_ADDR18
IFC_ADDR19
IFC_WE_B
IFC_OE_B
ETH_COL_1
ETH_RXER_1
ETH_TXCLK_1
ETH_TXEN_1
ETH_TXER
ETH_TXD3
ETH_TXD2
ETH_TXD1_1
ETH_TXD0_1
GPIO1/UART1_RTS
GPIO2/SDHC_D1
GPIO3
CLKIN0
CLKOUT1
GND_4
AN7
AN6
AN5
AN4
GND_5
DAC1
TMR3
TMR2
GPIO4
3.3V_2
PWM7
PWM6
PWM5
PWM4
CAN0_RX
CAN0_TX
WIRE
SPI0_MISO/IO1
SPI0_MOSI/IO0
SPI0_CS0
SPI0_CS1
SPI0_CLK
GND_6
I2C1_SCL
I2C1_SDA
GPIO5/SPI0_HOLD/IO3
RSRV_B53
RSRV_B54
IRQ_H
IRQ_G
IRQ_F
IRQ_E
IRQ_D
IRQ_C
IRQ_B
IRQ_A
EBI_ALE/EBI_CS1
EBI_CS0
GND_7
EBI_AD15
EBI_AD16
EBI_AD17
EBI_AD18
EBI_AD19
EBI_R/W
EBI_OE
EBI_D7
EBI_D6
EBI_D5
EBI_D4
EBI_D3
EBI_D2
EBI_D1
EBI_D0
GND_8
3.3V_3
5V_2
GND_9
3.3V_4
3.3V_5
GND_10
GND_11
I2C0_SCL
I2C0_SDA
GPIO9/UART1_CTS
GPIO8/SDHC_D2
GPIO7/SD_WP_DET
ETH_CRS
ETH_MDC_1
ETH_MDIO_1
ETH_RXCLK_1
ETH_RXDV_1
ETH_RXD3
ETH_RXD2
ETH_RXD1_1
ETH_RXD0_1
I2S0_MCLK
I2S0_DOUT_SCK
I2S0_DOUT_WS
I2S0_DIN0
I2S0_DOUT0
GND_12
AN3
AN2
AN1
AN0
GND_13
DAC0
TMR1
TMR0
GPIO6
3.3V_6
PWM3
PWM2
PWM1
PWM0
UART0_RX
UART0_TX
UART1_RX
UART1_TX
VSSA
VDDA
CAN1_RX
CAN1_TX
GND_14
GPIO14
GPIO15
GPIO16/SPI0_WP/IO2
GPIO17
USB0_DM
USB0_DP
USB0_ID
USB0_VBUS
I2S0_DIN_SCK
I2S0_DIN_WS
I2S0_DIN1
I2S0_DOUT1
RSTIN
RSTOUT
CLKOUT0
GND_15
EBI_AD14
EBI_AD13
EBI_AD12
EBI_AD11
EBI_AD10
EBI_AD9
EBI_AD8
EBI_AD7
EBI_AD6
EBI_AD5
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EBI_AD3
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TWRLCDRGB_G6
TWRLCDRGB_R2
TWRLCDRGB_R3
TWRLCDRGB_R4
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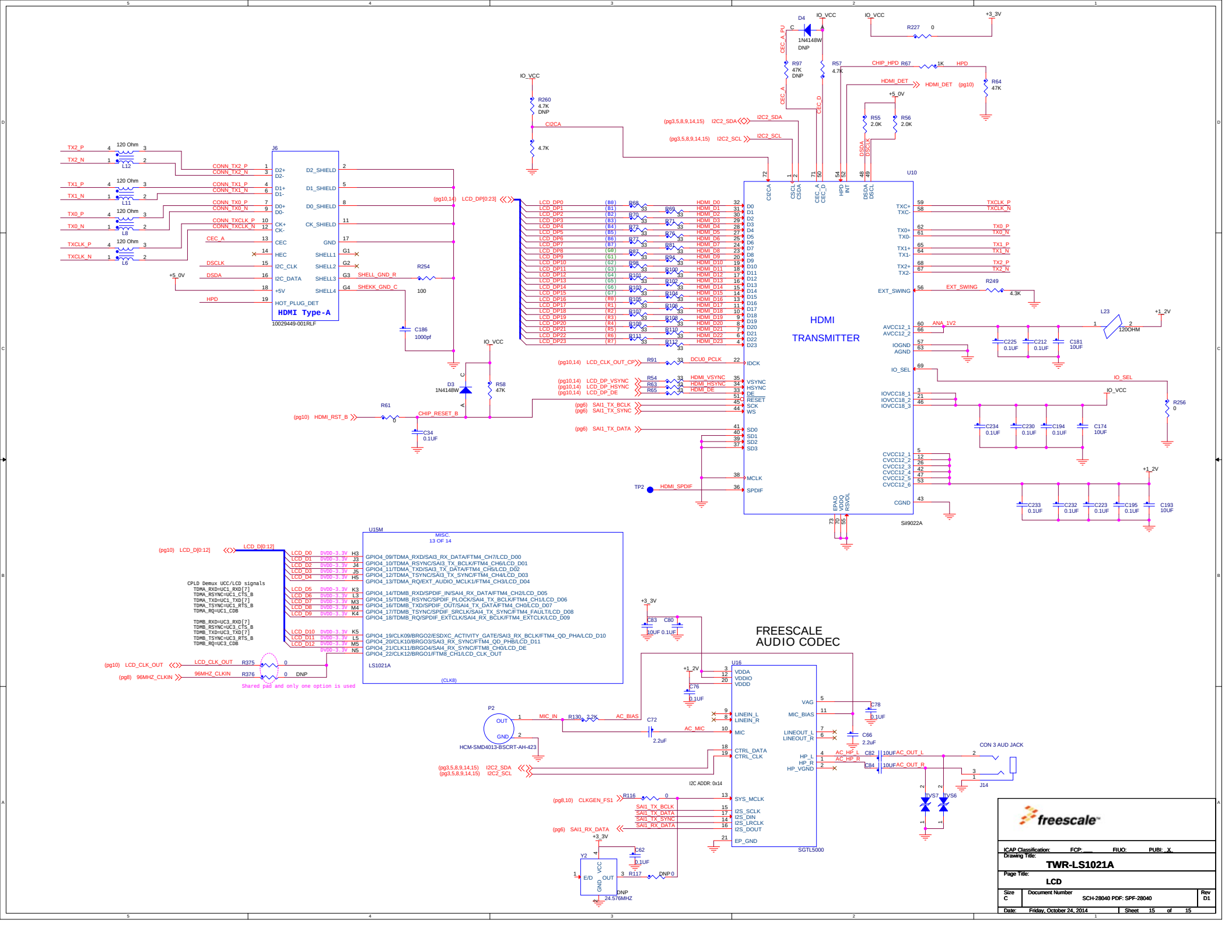
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