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QorIQ LS1046A Reference Design Board Getting Started Guide

Contents

1 Introduction

The LS1046A reference design board (RDB) is a high-performance computing, evaluation, and development platform based on the QorIQ LS1046A processor.

This document describes the LS1046ARDB hardware kit contents and different components of the board. It also explains how to configure and boot the board.

The LS1046ARDB functions with an integrated development environment (IDE), such as CodeWarrior Development Studio. For instructions on how to work with the CodeWarrior Development Studio IDE, see *CodeWarrior Development Studio for QorIQ LS series - ARM V8 ISA, Targeting Manual*, available at CodeWarrior for ARMv8 product summary page.

The list of items included in the LS1046ARDB hardware kit is provided in Hardware kit contents.

2 Related documentation

The table below lists and explains the additional documents that you can refer to, for more information about the LS1046ARDB. Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer or sales representative.

Table 1. Related documentation

Document	Description
QorIQ LS1046A Reference Design Board Reference Manual (LS1046ARDBRM)	Explains the LS1046ARDB interfaces and configuration. The LS1046ARDB documentation is available on the LS1046ARDB product summary page.
QorIQ LS1046A Reference Manual (LS1046ARM)	Provides a detailed description of the LS1046A multicore processor and its features, such as the memory map, serial interfaces, power supply, chip features, and clock information
QorIQ LS1046A Data Sheet	Contains information on LS1046A pin assignments, electrical characteristics, hardware design considerations, package information, and ordering information
QorIQ LS1046A BSP v0.4 document	Provides detailed information about QorIQ LS1046A BSP v0.4. It is available on the LS1046ARDB product summary page.
CodeWarrior TAP Probe User Guide (CWTAPUG)	Provides details of CodeWarrior® TAP, which enables target system debugging via a standard debug port (usually JTAG) while connected to a developer's workstation via Ethernet or USB. It is available at CodeWarrior TAP product summary page.
CodeWarrior Development Studio for QorIQ LS series - ARM V8 ISA, Targeting Manual (CWARMv8TM)	Explains how to use the CodeWarrior Development Studio for QorIQ LS series - ARM V8 ISA product. It is available at CodeWarrior for ARMv8 product summary page.

3 Hardware kit contents

The table below lists the items included in the LS1046ARDB hardware kit.

Table 2. Hardware kit contents

Item	Description
LS1046ARDB hardware assembly with enclosure	
Micro-USB 3.0 Micro-B male to Type A female cable	Converts the USB Micro-AB male port (port with the "USB2" silk on the chassis back panel) to USB Type A female port
Ethernet cable, straight through wiring, 6 ft min, RoHS compliant	Used to connect the board to network and get updated software for the board
USB 2.0 Type A to Micro-B cable	Used to provide a console connection at the chassis front panel
SATA3 data and power combo cable with 22 pins	Used to connect the board with SATA devices
12 V / 8.5 A AC-DC power adapter	An external 12 V DC power adapter to power the board
Universal supply AC power cable, 5 ft	Used to connect the power adapter with AC power supply
Universal AC input adapter	Used to convert the AC adapter plug to any type of standard plug
RJ45-to-DB9F cable	Used to provide a console connection at the chassis back panel
Finisar FTLX8571D3BCL SFP+ transceiver	Used to run the XFI2 function and insert the SFP+ module into the 10G SFP+ port
Thermal pad	Added on the bottom of the Wi-Fi card for thermal purposes
LS1046ARDB insert card	Provides quick link to the LS1046ARDB product summary page

Besides the hardware devices included in the hardware kit, you may optionally need the following hardware devices:

- CodeWarrior TAP: Used to debug the board

- Wi-Fi card
- SATA disk

4 Software requirements

The table below shows the software requirements to set up the LS1046ARDB.

Table 3. Software requirements

Requirement	Description
mbed Windows serial port driver	This driver is required to use the USB serial port on Windows. You can download it from https://developer.mbed.org/handbook/Windows-serial-configuration.
Serial terminal emulator	A serial terminal emulator, such as Tera Term, is required to control and monitor the LS1046ARDB from the serial console. You can download a serial terminal emulator from Internet.

5 LS1046ARDB chassis

The figure below shows the front panel of the LS1046ARDB chassis.

Figure 1. LS1046ARDB chassis front panel

The figure below shows the back panel of the LS1046ARDB chassis.

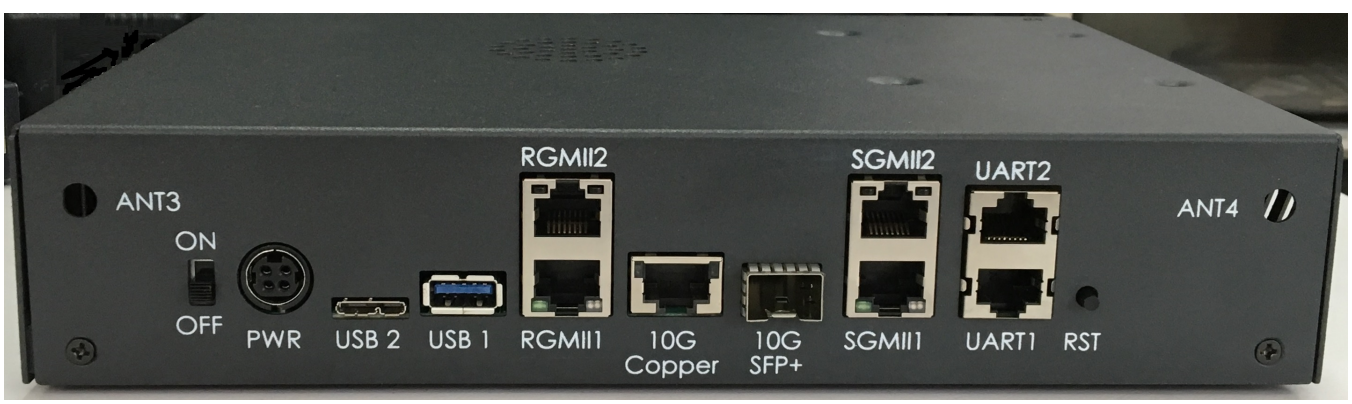


Figure 2. LS1046ARDB chassis back panel

6 Power and reset buttons

The table below describes the functions of the LS1046ARDB power and reset buttons.

Table 4. LS1046ARDB power and reset buttons

Push/slide button	Label	Function	Description
SW1	RESET	System reset	Press SW1 to reset the system, including the device and all attached peripherals.
SW2	PWR	Power cycle	Slide SW2 to turn the power on or off. **NOTE:** If J8 is shorted, to force power on, then SW2 will have no effect.

The figure below shows the locations of the power and reset buttons.

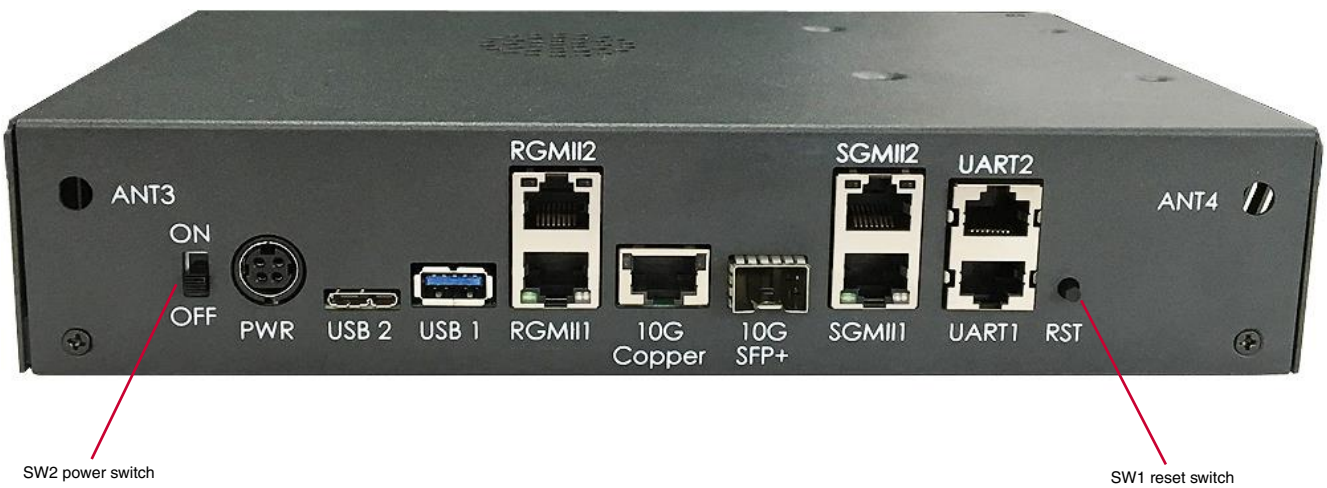


Figure 3. Power and reset button locations

7 Connectors, jumpers, and LED indicators

The following subsections describe the different components present on the LS1046ARDB. Note that some of these components are only visible after opening the chassis covers.

- Connectors
- Jumpers
- LED indicators

7.1 Connectors

The figure below shows the connectors available on the top view of the LS1046ARDB.

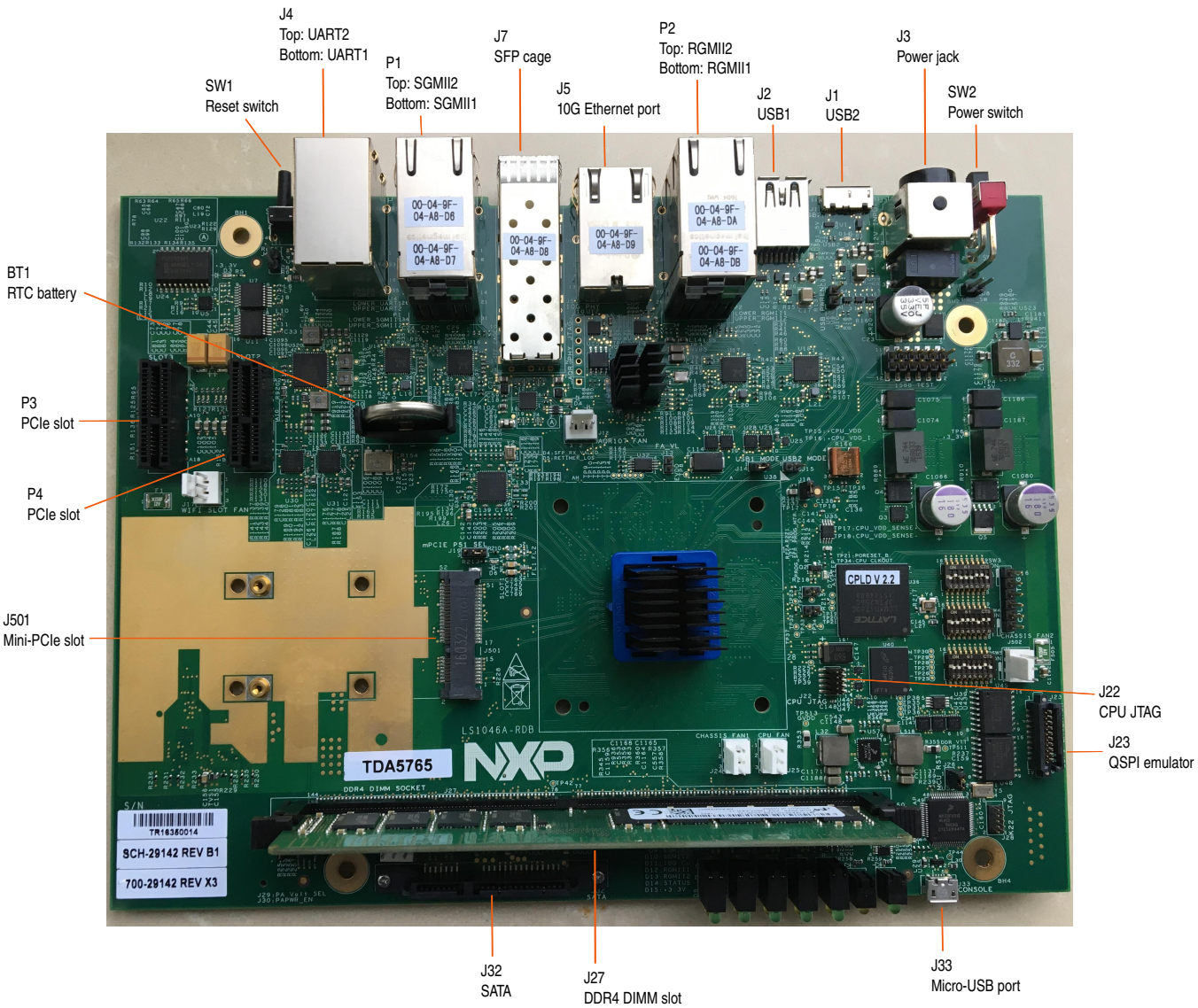


Figure 4. LS1046ARDB connectors (top view)

The figure below shows one connector available on the bottom view of the LS1046ARDB.

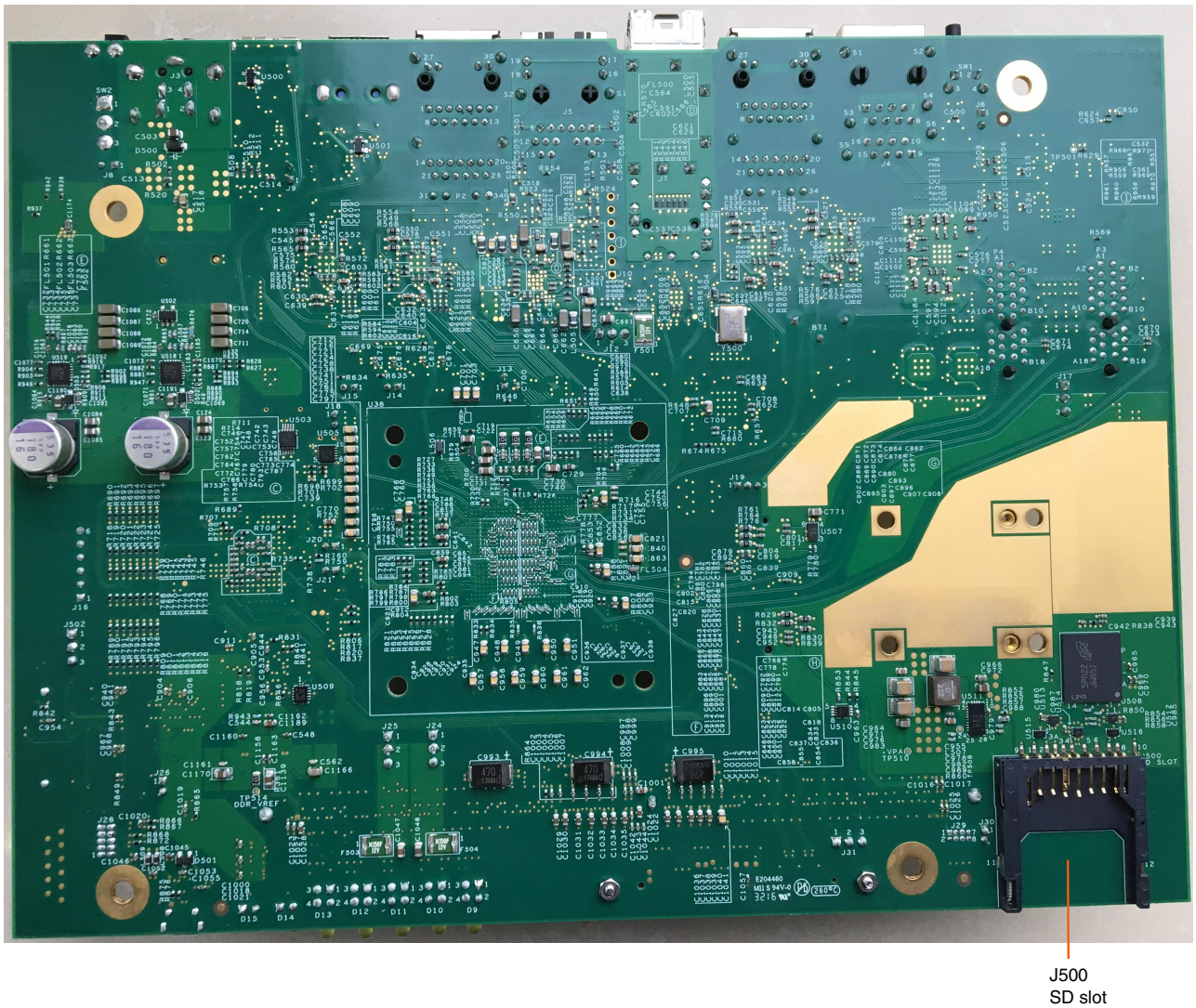


Figure 5. LS1046ARDB connectors (bottom view)

The table below lists the connectors available on the LS1046ARDB.

Table 5. LS1046ARDB connectors

Connector	Description	Connector type	Typical connection
BT1	RTC battery	3-pin battery holder	Connects to 3 V coin battery
J1	USB2	USB 3.0 Micro-AB connector	
J2	USB1	USB 3.0 Type A connector	
J3	12 V power jack	DC power jack	Connects to 12 V, 8 A power supply
J4	DUART	2x8-pin RJ45 connector • UART2: Top • UART1: Bottom	Connects to the RJ45-to-DB9F serial cable
J5	10G Ethernet port	19-pin RJ46 connector	Open
J7	SFP cage	2x10 pin connector	Install Finisar FTLX8571D3BCL SFP+ module available in the LS1046ARDB hardware kit.

Table continues on the next page...

Table 5. LS1046ARDB connectors (continued)

Connector	Description	Connector type	Typical connection
J22	CPU JTAG	2x5-pin ARM JTAG header	Connects to the CodeWarrior TAP
J23	QSPI emulator	2x10-pin connector	Open
J27	DDR4 DIMM slot	288-pin connector	Install DDR4 DIMM
J32	SATA	22-pin SATA connector	
J33	Debug USB (CMSIS DAP)	5-pin micro-USB 2.0 connector	Open
J500	SD slot		
J501	Mini-PCIe slot	52-pin mini-PCIe socket	Open
P1	10/100/1000M Ethernet ports	2x13-pin RJ45 connector • SGMII2: Top • SGMII1: Bottom	
P2	10/100/1000M Ethernet ports	2x13-pin RJ45 connector • RGMII2: Top • RGMII1: Bottom	Open
P3	PCIe slot	36-pin X1 PCIe socket	Open
P4	PCIe slot	36-pin X1 PCIe socket	Open
SW1	Reset key	4-pin reset switch	Open
SW2	DC power switch	3-pin ON/OFF switch	Turns power ON/OFF

7.2 Jumpers

The figure below shows the jumpers available on the LS1046ARDB.

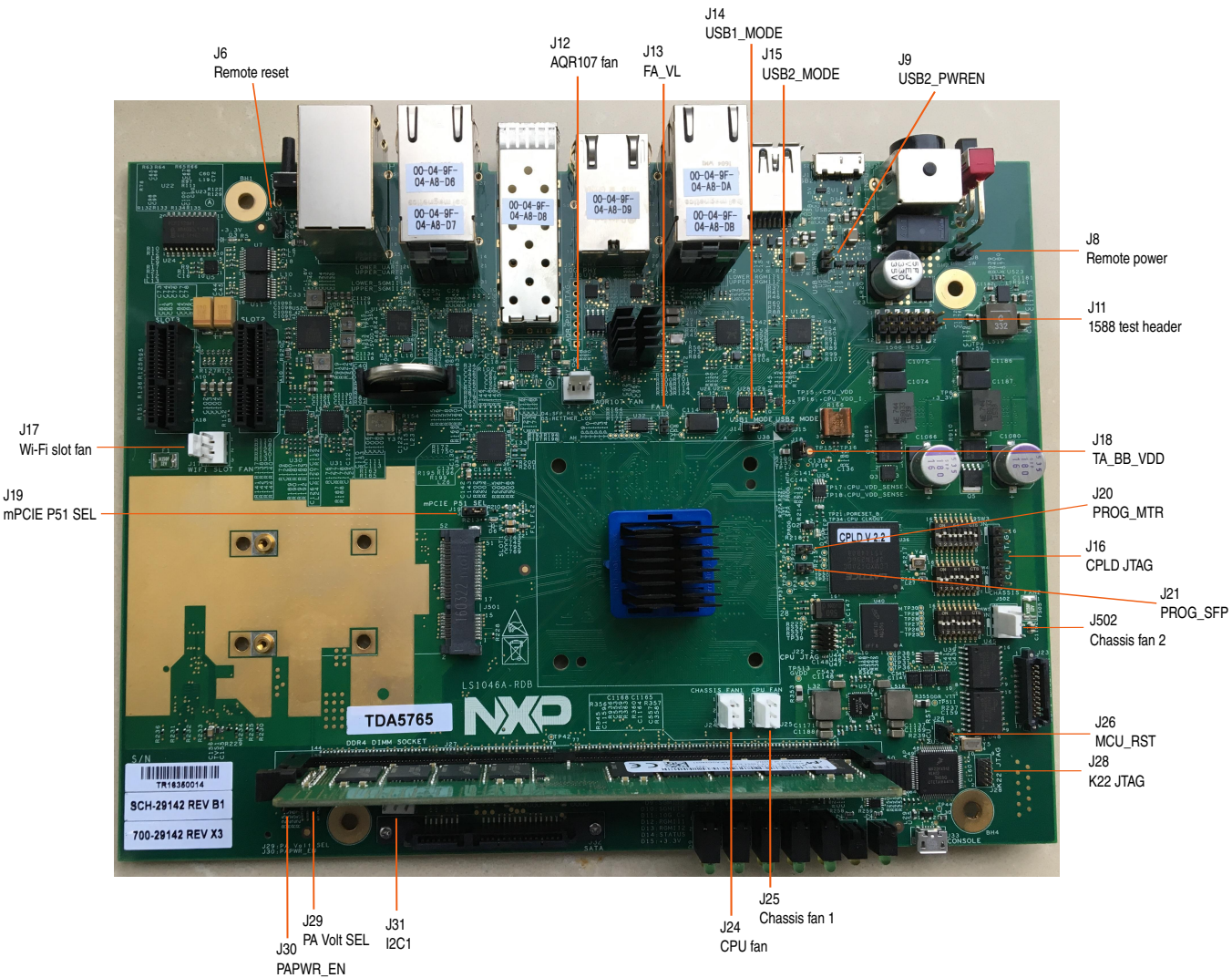


Figure 6. LS1046ARDB jumper locations

The table below shows the default factory settings for the LS1046ARDB jumpers.

Table 6. LS1046ARDB jumpers

Jumper	Type	Name/function	Description
J6	1X2-pin connector	Remote reset	• Open: No activity (default value) • Shorted: Resets the board
J8	1X2-pin connector	Remote power	• Open: Power switch is functional (default value) • Shorted: Power switch is disabled
J9	1X2-pin connector	USB2 power enable setting	• Open: USB2 power is controlled by the USB2_DRVVBUS signal (default value) • Shorted: USB2 power is controlled by the USB_DRVVBUS signal
J10	1X7-pin connector	AQR JTAG	Not available
J11	2X6-pin connector	1588 test header	• Open: No activity (default value) • Shorted: Connects to other devices for testing purposes

Table continues on the next page...

Table 6. LS1046ARDB jumpers (continued)

Jumper	Type	Name/function	Description
J12	1X3-pin connector	AQR107 fan	• Open: No activity (default value) • Shorted: Connects fan for thermal dissipation
J13	1X2-pin connector	FA_VL pin voltage setting	• Open: GND (default value) • Shorted: 1.0 V
J14	1X2-pin connector	USB1 mode setting	• Open: USB1 works in Device mode • Shorted: USB1 works in Host mode (default value)
J15	1X2-pin connector	USB2 mode setting	• Open: USB2 works in On-The-Go (OTG) mode (default value) • Shorted: USB2 works in Host mode
J16	1X6-pin connector	CPLD JTAG	Connects to the CPLD programmer
J17	1X3-pin connector	Wi-Fi slot fan	• Open: No activity (default value) • Shorted: Connects fan for thermal dissipation
J18	1X2-pin connector	TA_BB_VDD voltage setting	• Open: No supply for the TA_BB_VDD pin • Shorted: 1.0 V supply for TA_BB_VDD (default value)
J19	1X3-pin connector	Mini-PCIe pin 51 setting	Pins 1 and 2 are shorted; pin 3 is open **NOTE:** For some Wi-Fi cards, pin 51 of mini-PCIe is used to disable wireless input to active low. In this case, jumper pins 1 and 2 are shorted. For other Wi-Fi cards, pin 51 of mini-PCIe is used for power amplifier (PA) voltage. In this case, jumper pins 2 and 3 are shorted.
J20	1X2-pin connector	PROG_MTR voltage setting	• Open: GND (default value) • Shorted: 1.8 V
J21	1X2-pin connector	PROG_SFP voltage setting	• Open: GND (default value) • Shorted: 1.8 V
J24	1X3-pin connector	CPU fan	• Open: No activity (default value) • Shorted: Connects fan for thermal dissipation
J25	1X3-pin connector	Chassis fan 1	Connects to the chassis fan
J26	1X2-pin connector	MCU_RST	• Open: Disables reset function to MCU. It can avoid board reset when connected to Telnet. • Shorted: Reset key SW1 can enter Boot Loader mode to upgrade firmware (default value)
J28	2X5-pin connector	K22 JTAG	Connects to the JLINK emulation
J29	2X4-pin connector	PA voltage selection	PA voltage depends on the Wi-Fi card used: • 1-2 shorted: PA voltage is 5 V • 3-4 shorted: PA voltage is 4.5 V • 5-6 shorted: PA voltage is 3.5 V • 7-8 shorted: PA voltage is 3.3 V

Table continues on the next page...

Table 6. LS1046ARDB jumpers (continued)

Jumper	Type	Name/function	Description
J30	1X2-pin connector	Wi-Fi PA enable setting	• Open: Shuts down PA voltage • Shorted: Enables PA voltage (default value)
J31	1X3-pin connector	I2C1 jumper setting	• Open: No activity (default value) • Shorted: Connects to other I2C monitors
J502	1X3-pin connector	Chassis fan 2	Connects to the chassis fan

7.3 LED indicators

The figure below shows the light emitting diodes (LEDs) available on the LS1046ARDB.

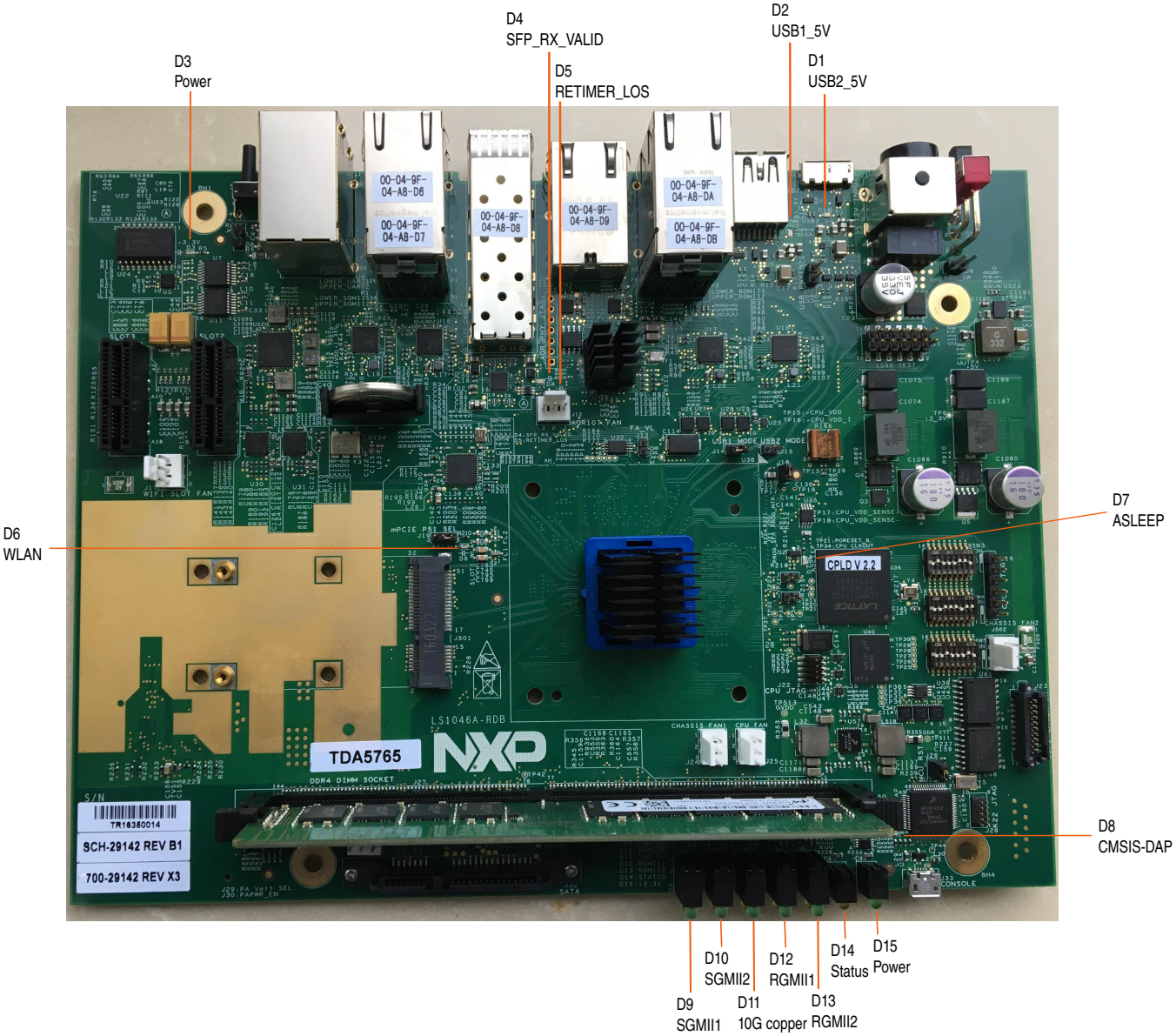


Figure 7. LS1046ARDB LED locations

The table below describes the LS1046ARDB LEDs.

Table 7. LS1046ARDB LEDs

LED	Color	Positioned on	Name	Description
D1	Green	PCB	USB2_5V	• OFF: USB2 power is OFF • ON: USB2 power is supplied
D2	Green	PCB	USB1_5V	• OFF: USB1 power is OFF • ON: USB1 power is supplied
D3	Green	PCB	Power LED (3.3 V)	• OFF: 3.3 V power is OFF • ON: 3.3 V power is supplied
D4	Green	PCB	SFP_RX_VALID	• ON: SFP receiving is operating normally • OFF: SFP receiving is reporting a loss-of-signal

Table continues on the next page...

Table 7. LS1046ARDB LEDs (continued)

LED	Color	Positioned on	Name	Description
D5	Green	PCB	RETIMER_LOS	• ON: XFI receive and transmit paths operating normally • OFF: XFI retimer is reporting a loss-of-signal
D6	Green	PCB	WLAN	This LED is defined by customer Wi-Fi card
D7	Green	PCB	ASLEEP	• ON: If the processor is not configured properly, or if the RCW contents are not correct • OFF: RCW is fetched
D8	Green	PCB	CMSIS-DAP	• ON: CMSIS-DAP firmware is loaded • OFF: CMSIS-DAP firmware is not loaded
D9	Yellow/green	Chassis	SGMII1	• Green: SGMII1 link • Yellow: SGMII1 activity
D10	Yellow/green	Chassis	SGMII2	• Green: SGMII2 link • Yellow: SGMII2 activity
D11	Yellow/green	Chassis	10G	• Green: AQR106 10G PHY link • Yellow: AQR106 10G PHY activity
D12	Yellow/green	Chassis	RGMII1	• Green: RGMII1 link • Yellow: RGMII1 activity
D13	Yellow/green	Chassis	RGMII2	• Green: RGMII2 link • Yellow: RGMII2 activity
D14	Yellow	Chassis	Status LED	Defined in the CPLD register
D15	Green	Chassis	Power LED	• OFF: 3.3 V power is OFF • ON: 3.3 V power is supplied

8 Switch configurations

The LS1046ARDB has three 8-bit dual inline package (DIP) switches, SW3, SW4, and SW5, which are shown in the figure below.

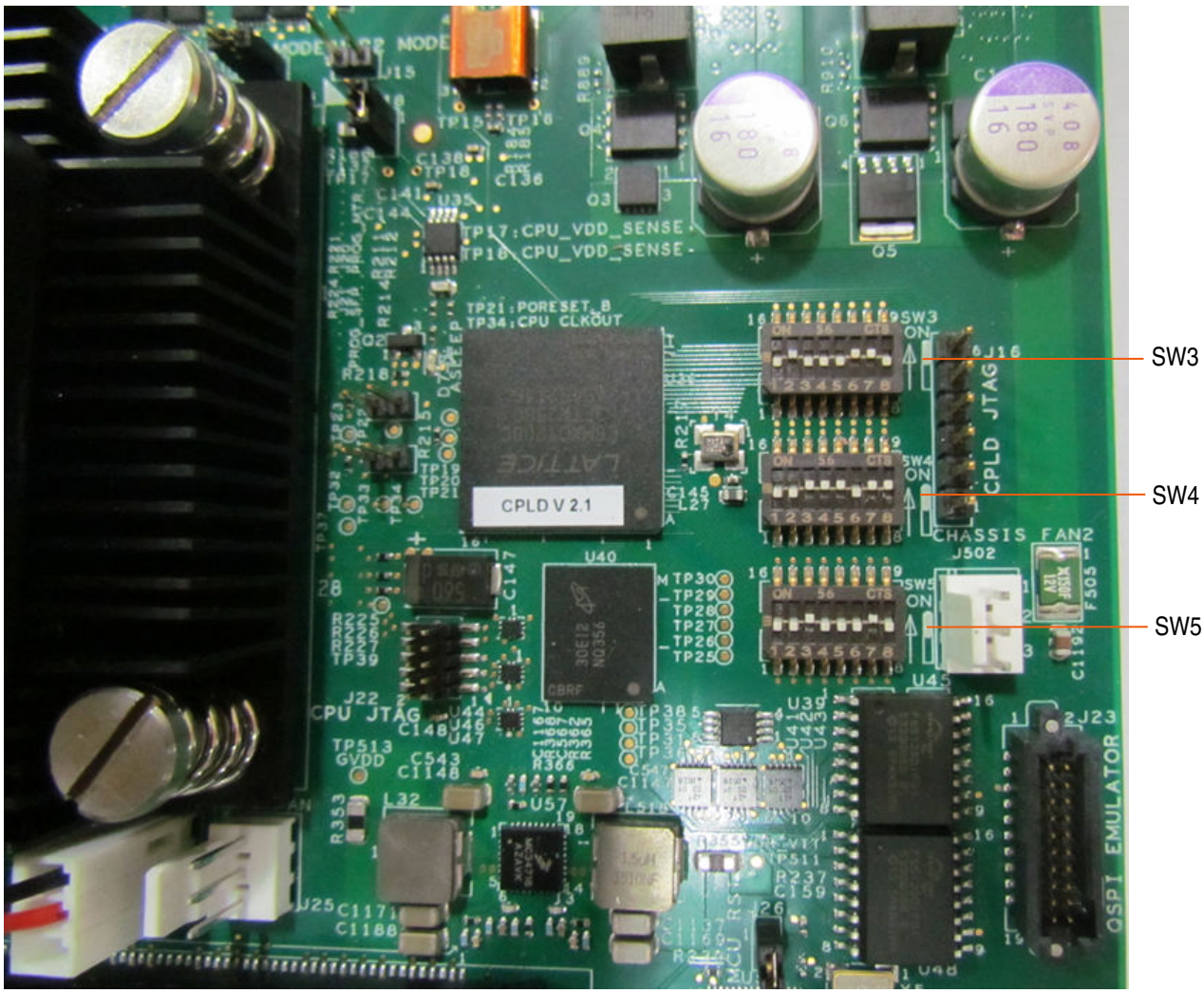


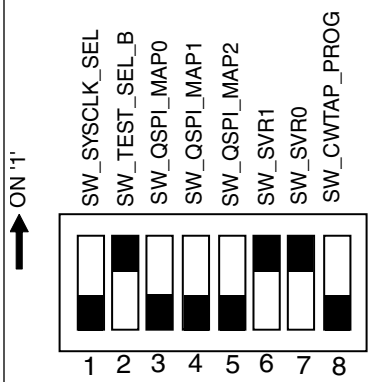
Figure 8. LS1046ARDB DIP switches

The LS1046ARDB DIP switches follow this convention:

- When a switch bit is up (ON), its value is 1
- When a switch bit is down (OFF), its value is 0

The table below describes the configuration settings for the LS1046ARDB DIP switches.

Table 8. DIP switch settings

<table>
<tr><th>Switch figure</th><th>Switch</th><th>Name</th><th>Description</th></tr>
<tr><td rowspan="8"> 
</td><td>SW3[1]</td><td>SYSCLK_SEL</td><td>Differential SYSCLK select
• 0: Differential SYSCLK (default value)
• 1: Single-end system clock</td></tr>
<tr><td>SW3[2]</td><td>CFG_TEST_SEL_B</td><td>TEST_SEL_B
• 0: Reserved
• 1: Enables all cores (default value)</td></tr>
<tr><td>SW3[3-5]</td><td>QSPI_MAP [0-2]</td><td><table><tr><th></th><th>QSPI_A_CS0</th><th>QSPI_A_CS1</th><th>Description</th></tr><tr><td>000</td><td>DEV#0</td><td>DEV#1</td><td>Normal (default value)</td></tr><tr><td>001</td><td>DEV#1</td><td>DEV#0</td><td>Swap</td></tr><tr><td>010</td><td>EMU</td><td>DEV#0</td><td>Prog#0</td></tr><tr><td>011</td><td>EMU</td><td>DEV#1</td><td>Prog#1</td></tr><tr><td>100</td><td>DEV#0</td><td>EMU</td><td>EMU Access</td></tr></table>Others: Reserved</td></tr>
<tr><td>SW3[6]</td><td>SW_SVR1</td><td rowspan="2">CFG_TEST_SEL_B + SW_SVR[0:1]
• 111: Reserved (default value)

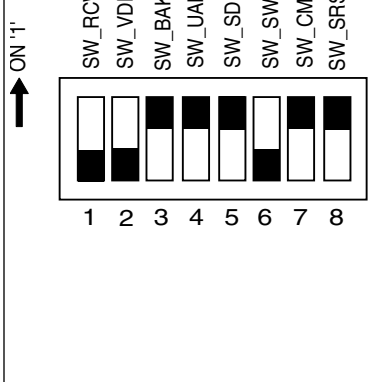
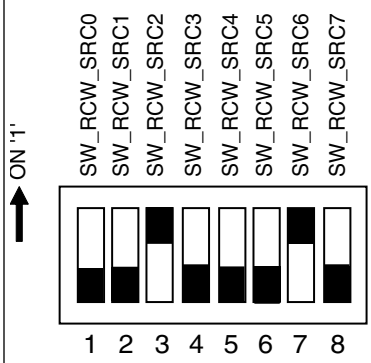
NOTE: The three bits, CFG_TEST_SEL_B, SW_SVR0, and SW_SVR1, are used together to determine the silicon personality (SVR).</td></tr>
<tr><td>SW3[7]</td><td>SW_SVR0</td></tr>
<tr><td>SW3[8]</td><td>CWTAP_PROG</td><td>• 0: JTAG header for LS1046A (default value)
• 1: JTAG header for CPLD programming</td></tr>
<tr><td rowspan="8"> 
</td><td>SW4[2]</td><td>VDD_VOLT_SEL</td><td>VDD_VOLT_SEL
• 0: VDD is 1.0 V (default value)
• 1: VDD is 0.9 V</td></tr>
<tr><td>SW4[3]</td><td>SW_BAKUP</td><td>BACKUP Bit
• 0: Reserved
• 1: Reserved (default value)</td></tr>
<tr><td>SW4[4]</td><td>UART_SEL</td><td>UART1 output select
• 0: RJ45
• 1: CMSIS-DAP (default value)</td></tr>
<tr><td>SW4[5]</td><td>SD1REFCLK_SEL</td><td>SD1 REFCLK select
• 0: 100 MHz
• 1: 156.25 MHz (default value)</td></tr>
<tr><td>SW4[6]</td><td colspan="2">Reserved</td></tr>
<tr><td>SW4[7]</td><td>CMSISDAP_EN</td><td>CMSISDAP_EN
• 0: Enable
• 1: Disable (default value)</td></tr>
<tr><td>SW4[8]</td><td>SW_RST_MODE</td><td>Software reset mode
• 0: Ignore RESET_REQ_B assertion
• 1: Trigger system reset on RESET_REQ_B assertion (default value)</td></tr>
</table>

Table continues on the next page...

Table 8. DIP switch settings (continued)

Switch figure	Switch	Name	Description
	SW5[1-8]	RCW_SRC[0-7]	RCW_SRC[0:8] select • 0010_0000_0: SDHC/eMMC • 0010_0010_0: QSPI (default value) • 0100_1XXX_X: Hard-coded RCW **NOTE:** The RCW_SRC field (9 bits) is spread over SW4 and SW5. **NOTE:** If you want to boot from eMMC, program a bootable image on the eMMC flash. When you boot from eMMC, you cannot insert an SD card. If you want to boot from an SD card, insert a bootable SD card. When an SD card is inserted, eMMC will be disabled.
	SW4[1]	RCW_SRC8	

9 Setting up CodeWarrior TAP

The CodeWarrior TAP allows you to debug and control of the LS1046ARDB system using the CodeWarrior IDE. For instructions on how to work with CodeWarrior IDE, see *CodeWarrior Development Studio for QorIQ LS series - ARM V8 ISA, Targeting Manual* (CWARMv8TM).

The LS1046ARDB hardware kit does not include a CodeWarrior TAP. To buy a CodeWarrior TAP, see the CodeWarrior TAP product summary page or contact your local NXP representative. Follow the instructions provided with the CodeWarrior package to set up the environment and attach the host (for example, USB or Ethernet).

To attach the CodeWarrior TAP to the LS1046ARDB, follow the steps below:

1. Install the 10-pin micro adapter provided with the CodeWarrior TAP (CWH-CTP-CTX10-YE).
2. Connect the 10-wire cable as shown in the figure below (both ends are keyed and can be installed on either side).

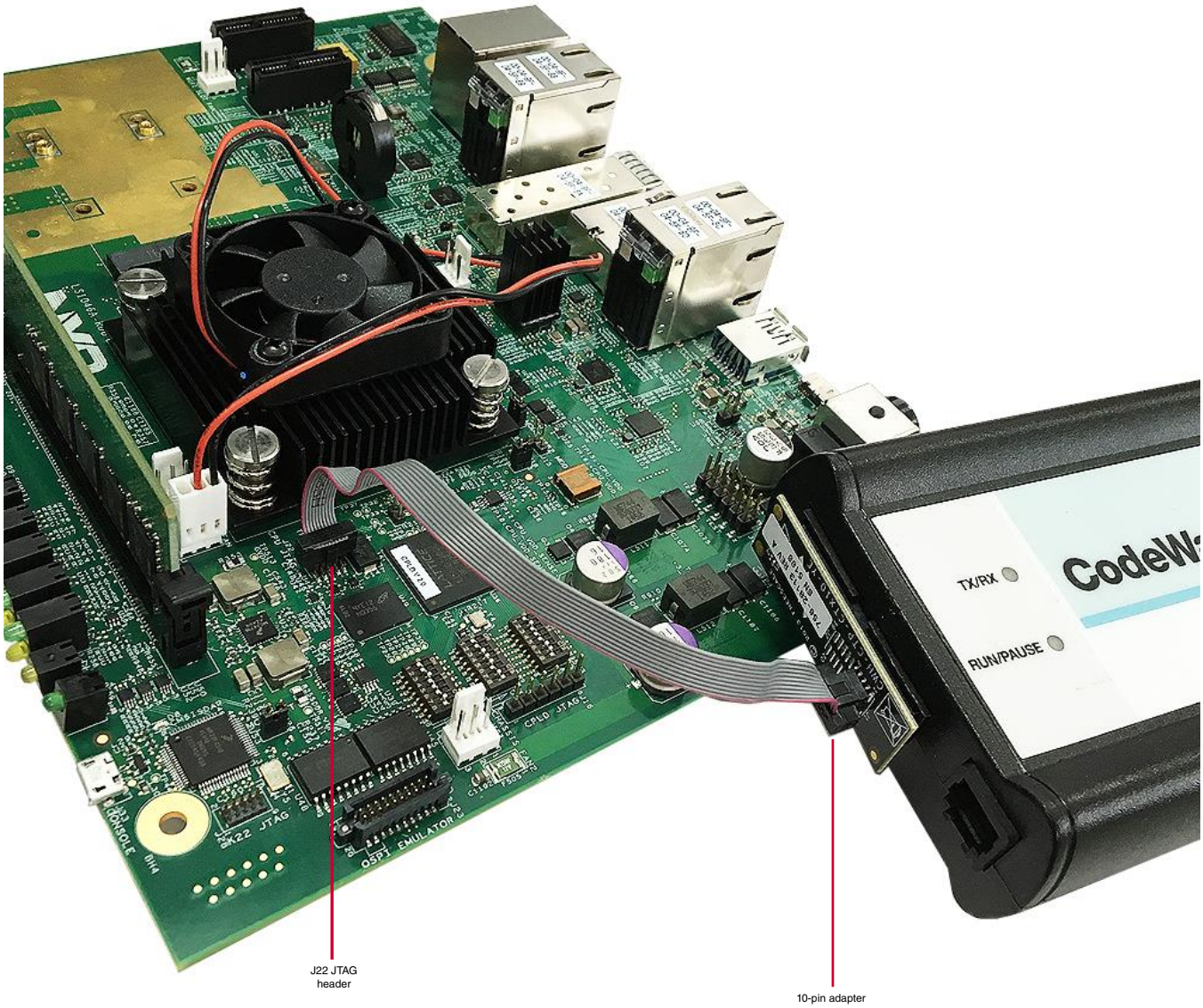


Figure 9. CodeWarrior installation

3. Install the free end of the cable to J22 on the LS1046ARDB. The red stripe should be aligned as shown in the figure above. The CodeWarrior TAP is now ready to be used.
4. Follow the instructions provided with the CodeWarrior package to complete the IDE setup.

10 Booting LS1046ARDB

Perform the following steps to boot the LS1046ARDB:

1. Download mbed Windows serial port driver to the host computer from https://developer.mbed.org/handbook/Windows-serial-configuration.
2. Download and install Tera Term on the host computer from Internet. After installation, a shortcut to the tool is created on the desktop of the host computer.

NOTE

This is a one-time activity. Skip this step if you have already installed the serial terminal emulator on the host computer.

3. Open chassis top cover and ensure that the board is configured for the default switch settings, as shown in the table below. See Switch configurations for details.

Table 9. Default switch settings

	1	2	3	4	5	6	7	8
SW3	0	1	0	0	0	1	1	0
SW4	0	0	1	1	1	0	1	1
SW5	0	0	1	0	0	0	1	0

4. Ensure that the power switch mounted on the wall is turned off.
5. Connect one end of the AC power cable to the wall mount power switch, using the universal adapter.
6. Connect other end of the AC power cable to the AC-DC power adapter.
7. Connect the power adapter cord connector to the power jack on the chassis back panel, by positioning the flat surface of the connector horizontally on the top side, as shown in the figure below.

Figure 10. Power connector position

8. Turn on the wall mount power switch.
9. Now, make a console connection between the board and host computer to see console output:
   - For Standalone mode (board setup with only one board):
     1. Ensure that SW4[4] is ON (default value).
     2. Using the USB 2.0 Type A to Micro-B cable provided with the hardware kit, connect the port with the "CONSOLE" silk on the chassis front panel to a USB port on the host computer, as shown in the figure

below. The D8 LED on the PCB turns ON. The host computer will automatically detect the USB device and will install the USB driver software.

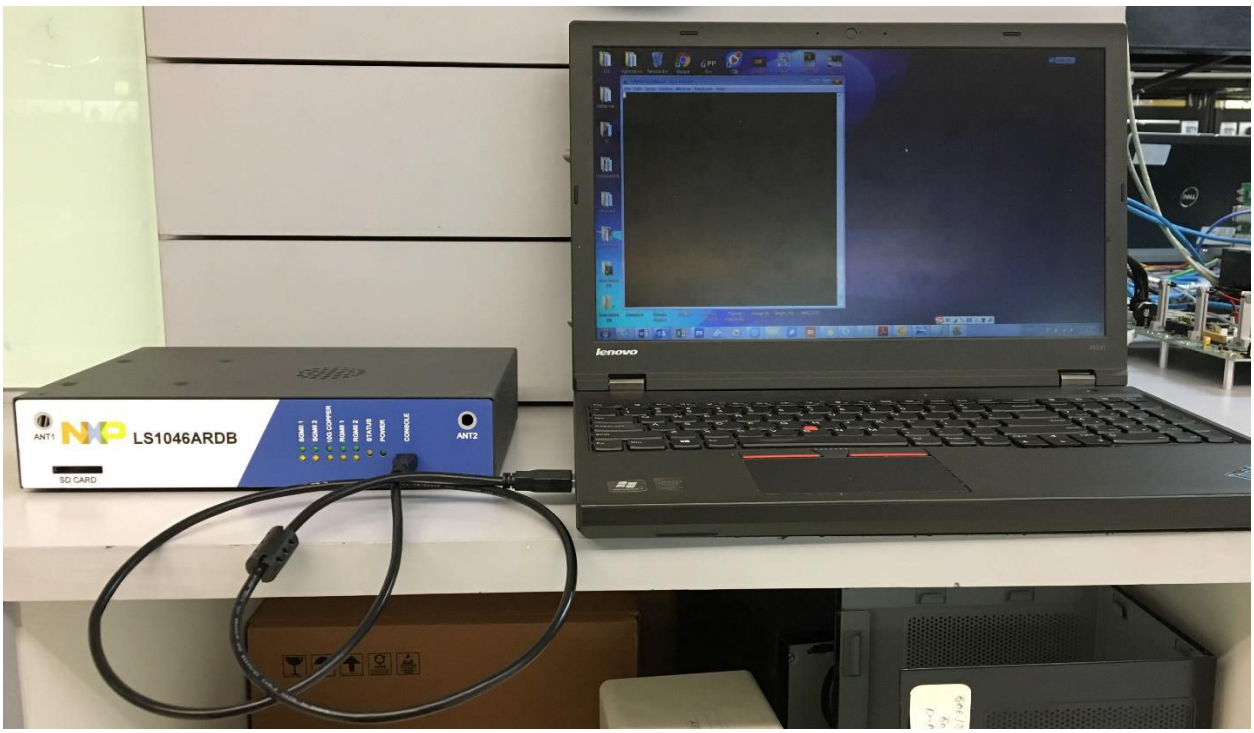


Figure 11. Console port connection using a USB cable

- For board farm:
  1. Turn SW4[4] to OFF.
  2. Using the RJ45-to-DB9F cable provided with the hardware kit, connect the port with the "UART1" silk on the chassis back panel to the host computer serial port, USB-to-DB9 convertor, or other devices, such as the CodeWarrior TAP, as shown in the figure below.

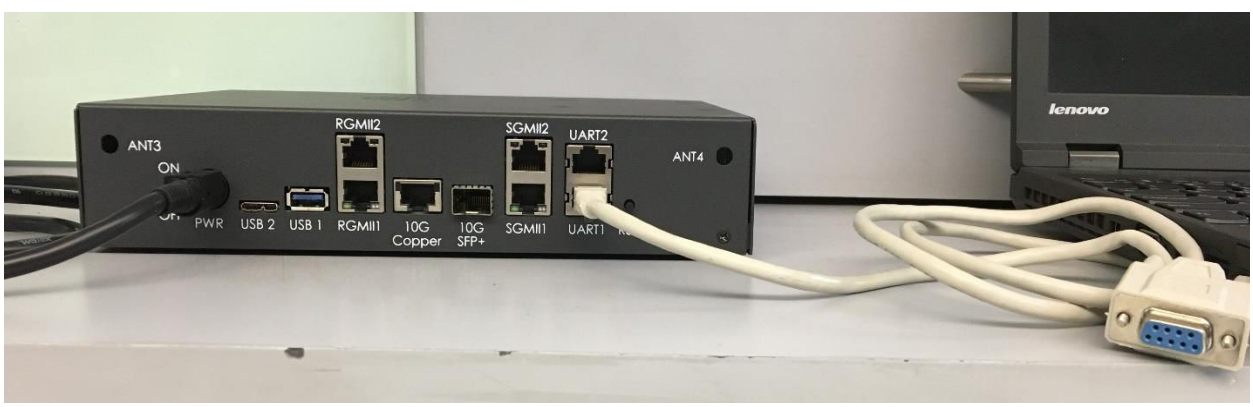


Figure 12. Console port connection using a RJ45-to-DB9F cable

Next steps in this section are based on the Standalone mode.

10. Install the mbed Windows serial port driver you downloaded earlier to the host computer.

NOTE

This is a one-time activity. Skip this step if you have already installed the mbed driver on the host computer.

11. Start and set up Tera Term:

a. Double-click the Tera Term shortcut. The Tera Term console appears, along with the **New connection** dialog.
b. On the **New connection** dialog, select the **Serial** option and ensure that **mbed Serial Port** is selected in the **Port** menu.
c. Click **OK** to close the **New connection** dialog.
d. Choose **Setup > Serial port** from the Tera Term console menu bar. The **Serial port setup** dialog appears.
e. On the **Serial port setup** dialog, configure the serial port of the host computer with the following settings:
    - Port: COM4
    - Baud rate: 115200
    - Data: 8 bit
    - Parity: none
    - Stop: 1 bit
    - Flow control: none
    - Transmit delay: 0 msec/char; 0 msec/line
f. Click **OK**.

12. Optionally, connect the CodeWarrior TAP to the LS1046ARDB. See Setting up CodeWarrior TAP for details.
13. Optionally, connect the Ethernet cable if you want to connect your board to the network, for example, for obtaining the latest board software and updating board images.
14. Turn on the power switch (SW2). The power LED (D3) on the printed circuit board (PCB) and the LED with "POWER" silk on the chassis front panel turn green. The board boots up and the console shows the U-Boot messages as illustrated below.

NOTE

The D7 (ASLEEP) LED on the PCB remains OFF if correct RCW is fetched.

```
U-Boot 2016.092.0+g2735535 (Jan 13 2017 - 21:39:10 +0800)

SoC:  LS1046AE Rev1.0 (0x87070010)
Clock Configuration:
       CPU0(A72):1800 MHz  CPU1(A72):1800 MHz  CPU2(A72):1800 MHz
       CPU3(A72):1800 MHz
       Bus:      700  MHz  DDR:      2100 MT/s  FMAN:     800  MHz
Reset Configuration Word (RCW):
       00000000: 0e150012 10000000 00000000 00000000
       00000010: 11335559 40005012 40025000 c1000000
       00000020: 00000000 00000000 00000000 00238800
       00000030: 20124000 00003101 00000096 00000001
Model: LS1046A RDB Board
Board: LS1046ARDB, boot from QSPI vBank 0
CPLD:  V2.2
PCBA:  V2.0
SERDES Reference Clocks:
SD1_CLK1 = 156.25MHZ, SD1_CLK2 = 100.00MHZ
I2C:   ready
DRAM:  Initializing DDR....using SPD
Detected UDIMM 18ASF1G72AZ-2G3B1
8 GiB (DDR4, 64-bit, CL=15, ECC on)
       DDR Chip-Select Interleaving Mode: CS0+CS1
SEC0: RNG instantiated
PPA Firmware: Version 0.2
Using SERDES1 Protocol: 4403 (0x1133)
Using SERDES2 Protocol: 21849 (0x5559)
NAND:  512 MiB
MMC:   FSL_SDHC: 0
SF: Detected S25FS512S with page size 256 Bytes, erase size 256 KiB, total 64 MiB
EEPROM: NXID v1
In:    serial
Out:   serial
Err:   serial
SATA link 0 timeout.
AHCI 0001.0301 32 slots 1 ports 6 Gbps 0x1 impl SATA mode
flags: 64bit ncq pm clo only pmp fbss pio slum part ccc apst
Found 0 device(s).
SCSI:  Net:   SF: Detected S25FS512S with page size 256 Bytes, erase size 256 KiB,
```

```
total 64 MiB
Fman1: Uploading microcode version 106.4.18
PCIe0: pcie@3400000 Root Complex: no link
PCIe1: pcie@3500000 Root Complex: no link
PCIe2: pcie@3600000 Root Complex: no link
FM1@DTSEC3 [PRIME], FM1@DTSEC4, FM1@DTSEC5, FM1@DTSEC6, FM1@TGEC1, FM1@TGEC2
Hit any key to stop autoboot:0
```

NOTE

The above U-Boot log is an example log. The actual log on the board may differ in compile time or in other ways.

11 Ethernet port mapping

The table below shows a mapping between the Ethernet port names printed on the chassis and the port names used in U-Boot and the Linux kernel.

Table 10. Ethernet port mapping

Port name on chassis	Port name in U-Boot	Port name in Linux kernel
RGMII1	FM1@DTSEC3	fm1-mac3
RGMII2	FM1@DTSEC4	fm1-mac4
SGMII1	FM1@DTSEC5	fm1-mac5
SGMII2	FM1@DTSEC6	fm1-mac6
10G Copper	FM1@TGEC1	fm1-mac9
10G SFP+	FM1@TGEC2	fm1-mac10

The figure below shows the Ethernet ports available on the LS1046ARDB chassis back panel.

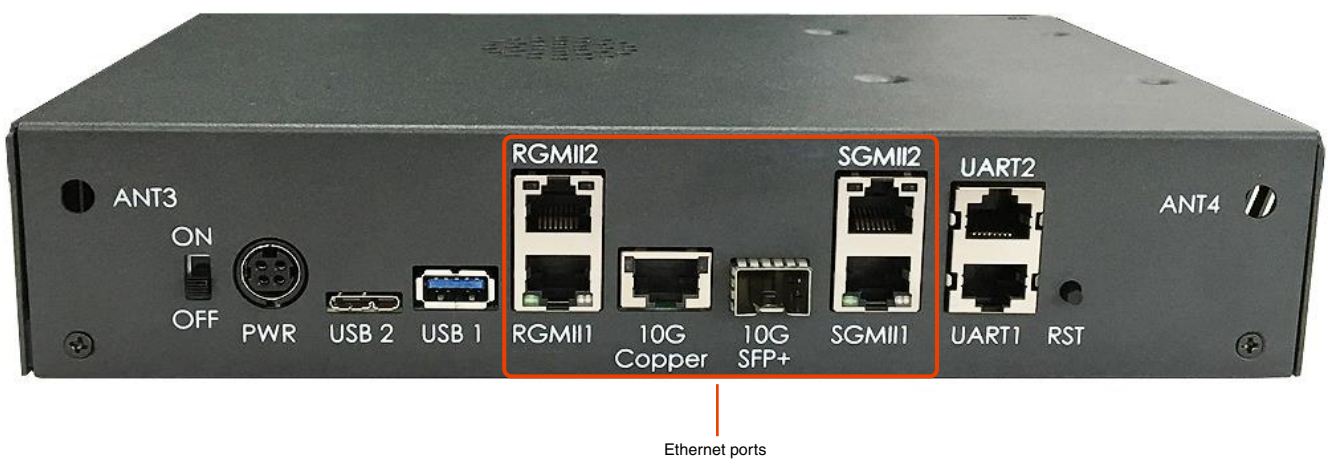


Figure 13. Ethernet ports on chassis

12 LS1046ARDB boot sources

The LS1046ARDB supports booting from the following three boot sources:

- QSPI bank 0
- QSPI bank 4
- SD card

The table below shows switch settings for the available boot sources.

Table 11. Switch settings for boot sources

Boot source	SW3[1:8]	SW4[1:8]	SW5[1:8]
QSPI bank 0 (default bank)	01000110	00111011	00100010
QSPI bank 4	01001110	00111011	00100010
SD card	01000110	00111011	00100000

You can change the current boot source for the board by either changing the switch settings manually on the board or overriding the current switch settings in software using CPLD commands. The table below describes CPLD commands that can be used to switch between the three boot sources.

Table 12. CPLD commands for switching between boot sources

CPLD command	Description
`cpld reset`	Resets the board to boot from the default bank (bank 0)
`cpld reset altbank`	Resets the board to boot from the alternative bank (bank 4)
`cpld reset sd`	Resets the board to boot from the SD card

NOTE

For detailed information on the system memory map and available booting options, see LSDK Knowledge Center.

13 LS1046ARDB operating configurations

The table below shows the default LS1046ARDB operating voltages.

Table 13. LS1046ARDB operating voltages

Supply voltages	Description	Voltage value
AVDD_CGA1, AVDD_CGA2, AVDD_PLAT, AVDD_D1	Supply voltages (core/platform/DDR) for PLLs	1.8 V
AVDD_SD1_PLL1, AVDD_SD1_PLL2, AVDD_SD2_PLL1, AVDD_SD2_PLL2	Supply voltages (filtered from XVDD) for SerDes PLLs 1 and 2	1.35 V
G1VDD voltage	I/O supply voltage for DDR DRAM	1.2 V
SVDD voltage	Core power supply for the SerDes transceivers	1.0 V or 0.9 V
XVDD voltage	Pad power supply for the SerDes transceivers	1.35 V

Table continues on the next page...

Table 13. LS1046ARDB operating voltages (continued)

Supply voltages	Description	Voltage value
OVDD voltage	General I/O supply: Used for GPIO1, GPIO2, DSPI, eSDHC[4:7], SYSCLK, DDRCLK, and IFC system control and power management, clocking, debug, and JTAG I/O	1.8 V
LVDD voltage	Ethernet supply voltage	1.8 V
DVDD voltage	Supply voltage for DUART, I2C, DMA, GPIO1, GPIO4, and USB control	3.3 V
EVDD voltage	Supply voltage for eSDHC[0:3]/CLK/CMD and GPIO2	3.3 V / 1.8 V
TVDD voltage	Supply voltage for Ethernet management interface 2 (EMI2) and GPIO4	2.5 V
2V5 voltage	AQR107 VDD_IO supply voltage	2.5 V
FA_VL voltage	Reserved for internal use	0 V / (1.0 V - optional)
PROG_MTR	Reserved for internal use	0 V / (1.8 V - optional)
PROG_SFP	Security fuse programming override supply	0 V / (1.8 V - optional)
TH_VDD	Thermal monitor unit supply	1.8 V
TA_BB_VDD voltage	Low power security monitor supply	1.0 V
VDD	Core and platform supply	1.0 V or 0.9 V
USB_SVDD1 and 2	USB PHY analog supply	1.0 V or 0.9 V
USB_SDVDD1 and 2	USB PHY digital supply	1.0 V or 0.9 V
USB_HVDD1 and 2	USB PHY transceiver supply	3.3 V
VPP voltage	DDR4 activating power supply	2.5 V
VREF (DDR VREF voltage)	DDR VREF voltage power supply	0.6 V
VTT1 (DDR4_VTT voltage)	DDR4 termination voltage power supply	0.6 V

The table below shows the default LS1046ARDB clock frequencies.

Table 14. LS1046ARDB clock frequencies

Clock	Description	Frequency
Core clock	Depends on RCW	1800 MHz
Platform clock	Depends on RCW	700 MHz
SYSCLK (differential or single-end SYSCLK)	System clock (default: Differential mode)	100 MHz
DDR CLK	DDR clock	100 MHz
RTC CLK	Real-time clock	32.768 kHz
SD1_REF_CLK1	SerDes1 reference clock 1	100 MHz
SD1_REF_CLK2	SerDes1 reference clock 2	100/156.25 MHz
SD2_REF_CLK1	SerDes2 reference clock 1	100 MHz
SD2_REF_CLK2	SerDes2 reference clock 2	100 MHz
25MHZ_EC1_RGMII	RGMII PHY RTL8211FS reference clock	25 MHz
25MHZ_EC2_RGMII	RGMII PHY RTL8211FS reference clock	25 MHz
25MHZ_EC3_SGMII	SGMII PHY RTL8211 reference clock	25 MHz

Table continues on the next page...

Table 14. LS1046ARDB clock frequencies (continued)

Clock	Description	Frequency
25MHZ_EC4_SGMII	SGMII PHY RTL8211 reference clock	25 MHz
PCIE1_CLK	PCIe slot 1 reference clock	100 MHz
PCIE2_CLK	PCIe slot 2 reference clock	100 MHz
MPCIE_CLK	Mini-PCIe reference clock	100 MHz
XGT1588_CLK	IEEE1588 reference clock for AQR PHY	100 MHz
XFI1_REFCLK	XFI reference clock	25 MHz

14 Revision history

The table below summarizes revisions to this document.

Table 15. Revision history

Revision	Date	Topic cross-reference	Change description
Rev. 3	08/2017		Removed obsolete SDK information and added reference to LSDK Knowledge Center
Rev. 2	03/2017	Jumpers	Added details of jumpers in Table 6
		Booting LS1046ARDB	Updated U-Boot log
		Flashing prebuilt SDK images on LS1046ARDB	Updated the section
		LS1046ARDB operating configurations	Updated core and platform frequencies in Table 14
Rev. 1	12/2016	Introduction	Updated the section
		Related documentation	Added new document references
		Jumpers	Updated details of the J19 jumper
		Setting up CodeWarrior TAP	Updated introductory text of the section
		Booting LS1046ARDB	Updated the section
		LS1046ARDB boot sources	Added as a new section
		Configuring U-Boot environment variables	Added as a new section
			Removed the "Programming a new U-Boot, RCW, and microcode" section and its subsections
		Flashing prebuilt SDK images on LS1046ARDB	Added as a new section
		Troubleshooting	Updated the section
Rev. 0	09/2016		Initial public release

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