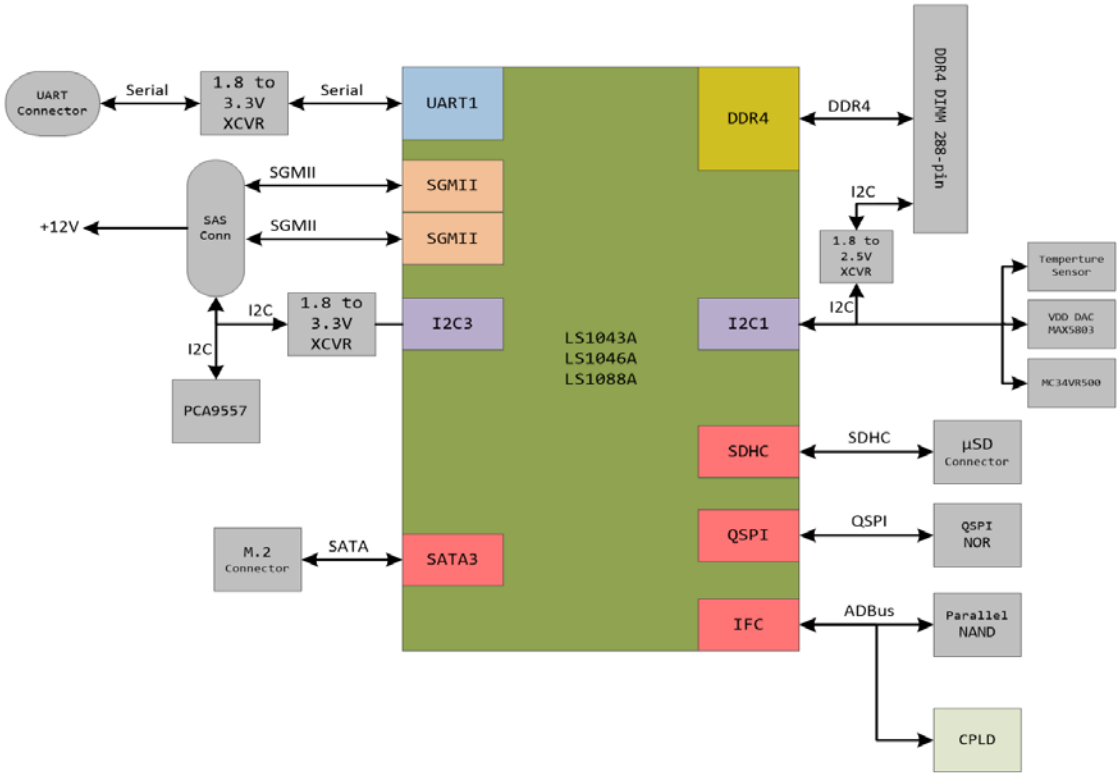
Background

We have designed a LS1046A based PCB with substantial similarity to the LS1046ARDB.



Similarly to the LS1046ARDB the CPLD drives the ~HRESET, ~PORESET, RCW source config, and others.

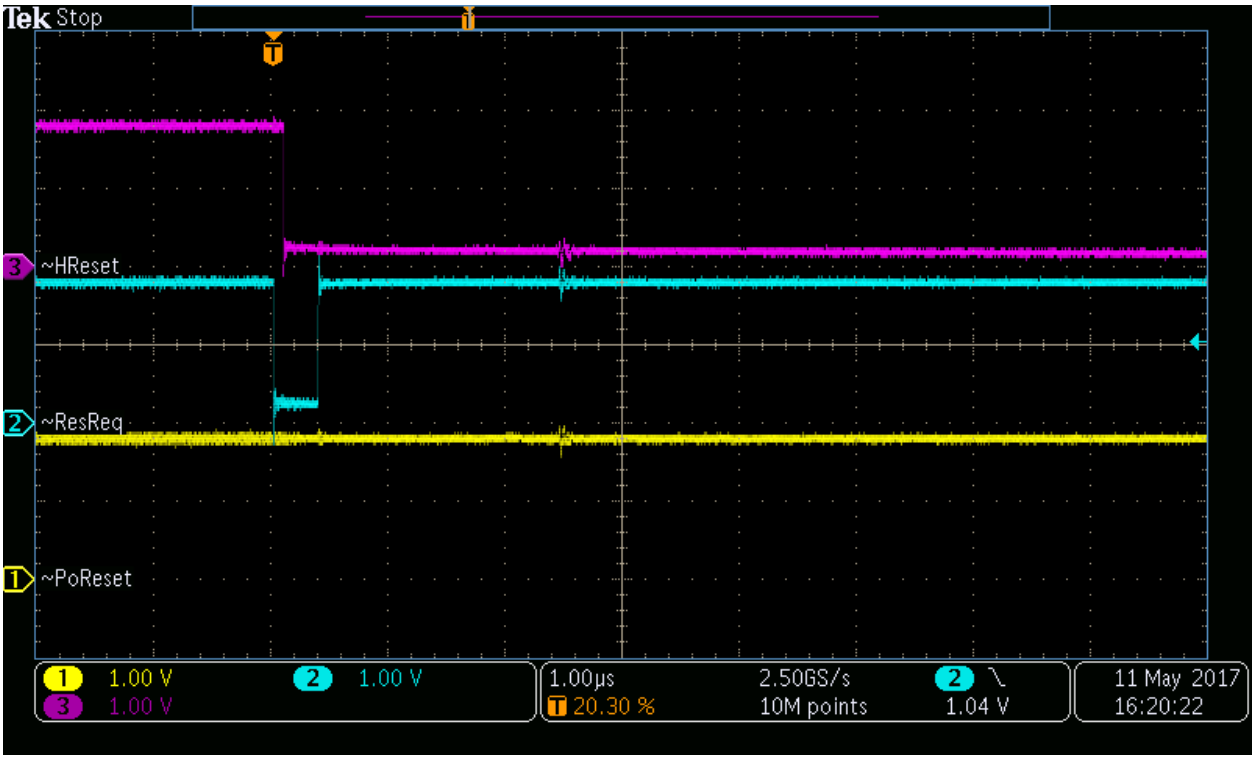
U-Boot displays some basic information below:

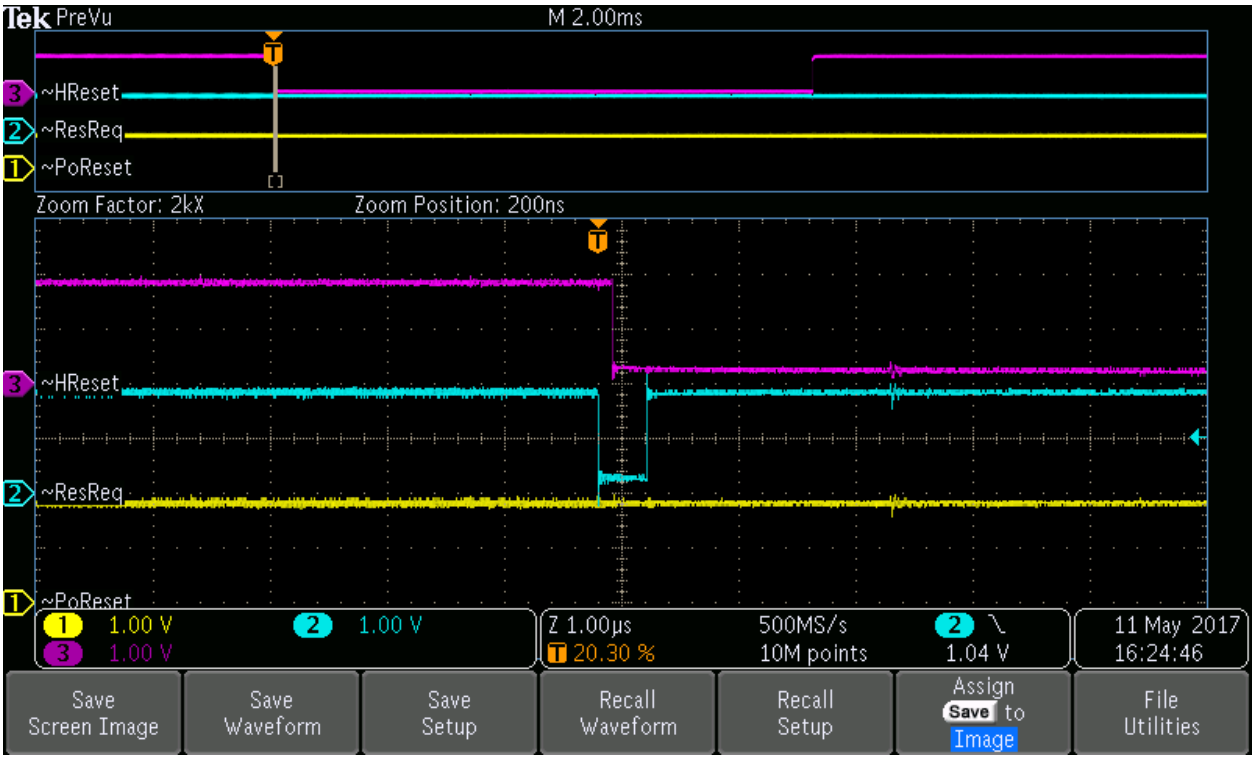
```
U-Boot 2017.01 (Mar 28 2017 - 18:26:49 -0700)

SoC:  LS1046AE Rev1.0 (0x87070010)
Clock Configuration:
       CPU0(A72):1600 MHz  CPU1(A72):1600 MHz  CPU2(A72):1600 MHz
       CPU3(A72):1600 MHz
       Bus:      600  MHz  DDR:      2100 MT/s  FMAN:     700  MHz
Reset Configuration Word (RCW):
       00000000: 0c150010 0e000000 00000000 00000000
       00000010: 33335559 f0005012 40025000 c1000000
       00000020: 00000000 00000000 00000000 0001e87e
       00000030: 20004000 24660101 00000096 00000001
Model: LS1046A RDB Board
Board: HAUTEMICA, boot from Invalid setting of SW5
CPLD:  V0.0
PCBA:  V0.0
SERDES Reference Clocks:
SD1_CLK1 = 100.00MHZ, SD1_CLK2 = 100.00MHZ
I2C:   ready
DRAM:  Initializing DDR....using SPD  :
```

Problem Encountered

Attempting to use the Hard Reset feature as defined in QorIQ LS1046A Reference Manual, Rev. D 11/2016 Section 4.4.2

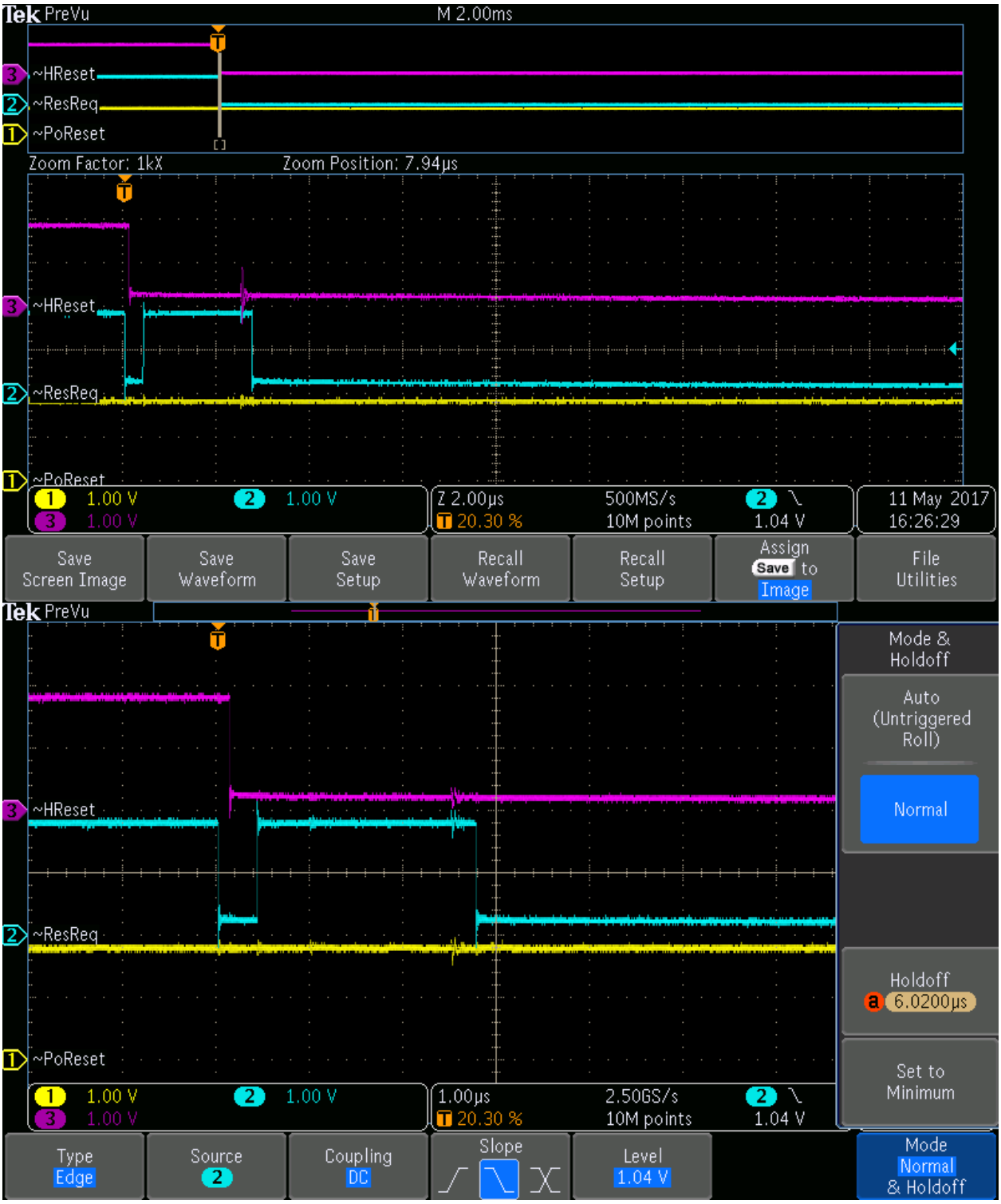
When booting from a SDHC device; asserting the ~HRESET in response to a ~RESET_REQ reboots effectively.





We see the ~RESET_REQ assert for 400nS and much later ~HRESET deassert at exit of Hard Boot.

When booting from QSPI there is some unexpected behavior.



In this case the ~RESET_REQ initially looks like before (SDHC case) but 2.36uS after deasserting it drives low again. This condition persists forever. We have tried masking all the ~RESET_REQ sources in the RSTRQMR1 but the failure is the same.