KEYSIGHT TECHNOLOGIES

Test Report

Overall Result: FAIL

Test Configuration Details	
Device Description	
Burst Triggering Method	DQS-DQ Phase Difference
LPDDR3	No
DDR3L	Yes
Test Mode	Compliance
Speed Grade	DDR3L-1600
Test Session Details	
Infiniium SW Version	05.50.0021
Infiniium Model Number	DSO90604A
Infiniium Serial Number	MY51500109
Application SW Version	2.44.9007
Debug Mode Used	No
Probe (Channel 1)	Model: 1134A Serial: US49491073 Head: E2678A/B Atten: Calibrated (2 DEC 2016 12:15:52), Using Cal Atten (1.0025E+001) Skew: Calibrated (2 DEC 2016 12:16:01), Using Cal Skew
Last Test Date	2016-12-02 15:39:04 UTC +01:00

Summary of Results

Test Statistics	
Failed	**2**
Passed	2
Total	4

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✗	1	1	VIH.CA(AC)	760.580000000 mV	**-6.1 %**	VALUE >= VrefCA_Volt+AcLevels_CA_Volt V
✗	1	1	VIH.CA(DC)	760.580000000 mV	**-0.8 %**	VrefCA_Volt+DcLevels_Volt V <= VALUE <= VDD_Volt V
✓	0	1	VIL.CA(AC)	223.840000000 mV	58.5 %	VALUE <= VrefCA_Volt-AcLevels_CA_Volt V
✓	0	1	VIL.CA(DC)	219.730000000 mV	37.6 %	0.000000000000 V <= VALUE <= VrefCA_Volt-DcLevels_Volt V

Report Detail

Next

✗VIH.CA(AC)

Reference: JEDEC Standard No. 79-3-1A.01, Table 4

Test Summary: **FAIL** Test Description: AC Input Logic High

Pass Limits: >= VrefCA_Volt+AcLevels_CA_Volt V **VIH.CA(AC)** 760.580000000 mV

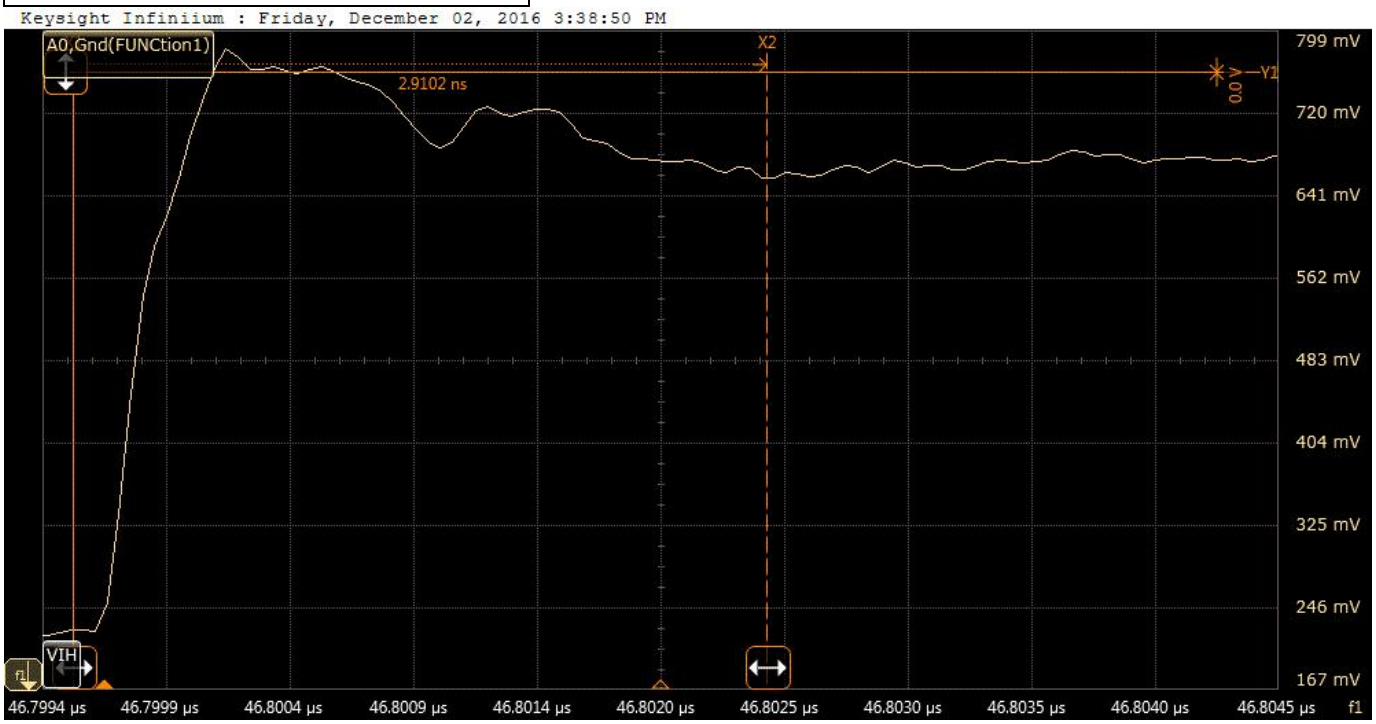
Result Details

Worst VIH (See image) **NumOfMeas** 10.000 **PUT** A0 **PUT Src** Channel 1 **Supporting Pin** N/A

Supporting Pin Src N/A **PassLimit Min (VrefCA_Volt+AcLevels_CA_Volt)** 810.000000000 mV

Trial 1

Trial 1: Worst VIH



Next

✗VIH.CA(DC)

Reference: JEDEC Standard No. 79-3-1A.01, Table 4

Test Summary: **FAIL** Test Description: DC Input Logic High

Pass Limits: [VrefCA_Volt+DcLevels_Volt V to VDD_Volt V] **VIH.CA(DC)** 760.580000000 mV

Result Details

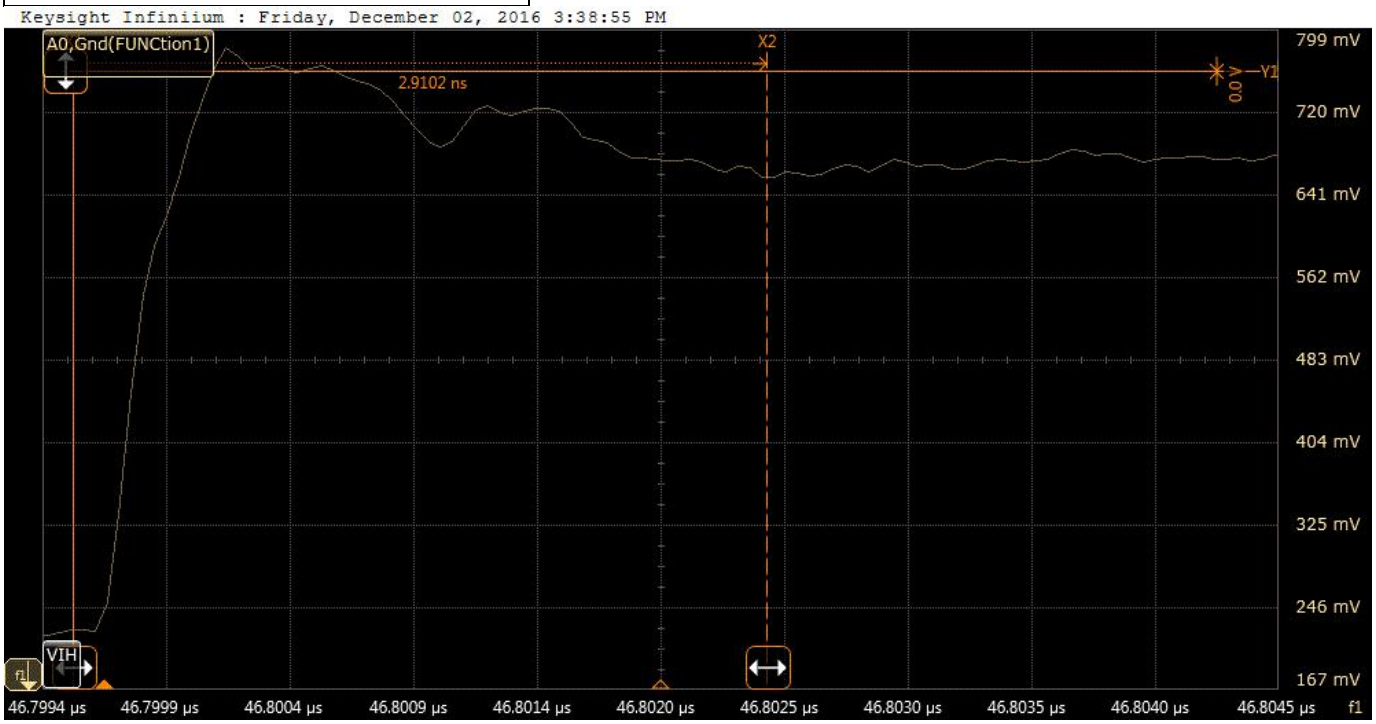
Worst VIH (See image) **NumOfMeas** 10.000 **PUT** A0 **PUT Src** Channel 1 **Supporting Pin** N/A

Supporting Pin Src N/A **PassLimit Min (VrefCA_Volt+DcLevels_Volt)** 765.000000000 mV

PassLimit Max (VDD_Volt) 1.350000000000 V

Trial 1

Trial 1: Worst VIH



Next

✓VIL.CA(AC)

Reference: JEDEC Standard No. 79-3-1A.01, Table 4

Test Summary: Pass | Test Description: AC Input Logic Low

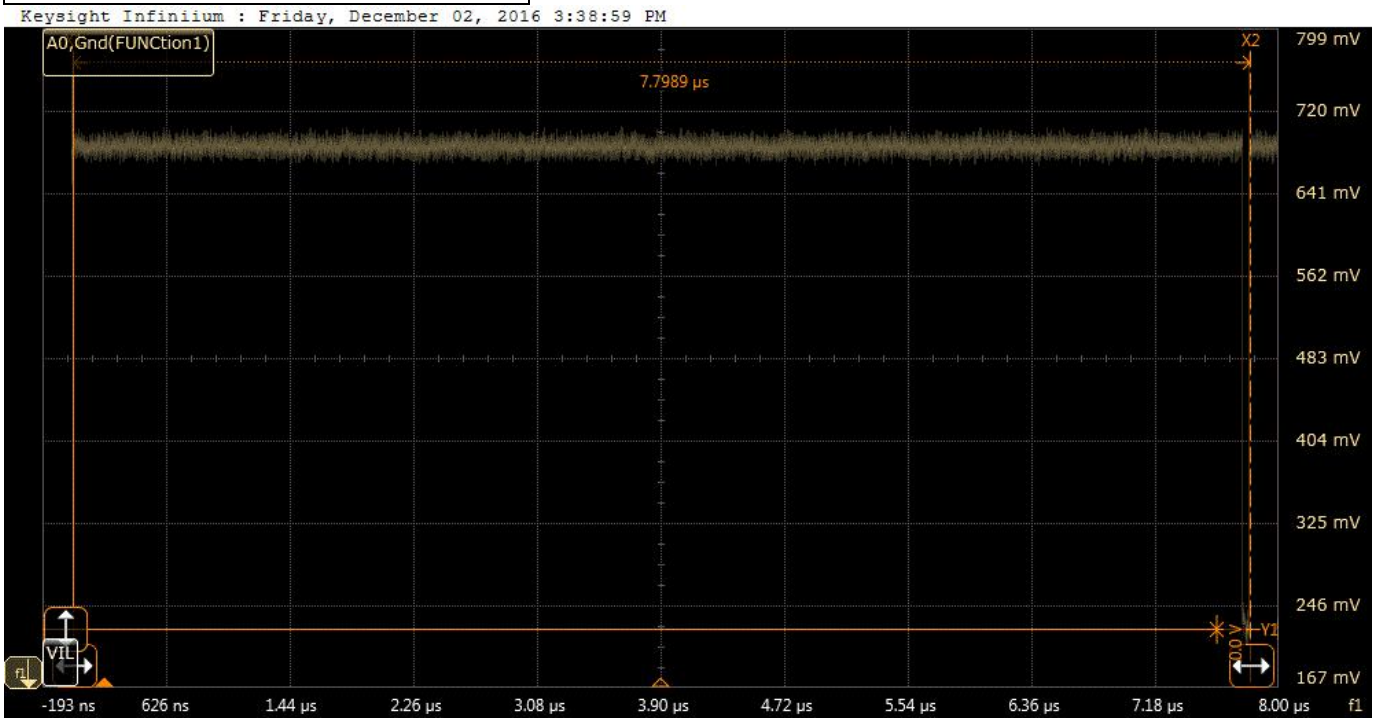
Pass Limits: <= VrefCA_Volt-AcLevels_CA_Volt V | **VIL.CA(AC)** 223.840000000 mV

Result Details

Worst VIL (See image) | **NumOfMeas** 10.000 | **PUT** A0 | **PUT Src** Channel 1 | **Supporting Pin** N/A | **Supporting Pin Src** N/A | **PassLimit Max (VrefCA_Volt-AcLevels_CA_Volt)** 540.000000000 mV

Trial 1

Trial 1: Worst VIL



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✓VIL.CA(DC)

Reference: JEDEC Standard No. 79-3-1A.01, Table 4

Test Summary: Pass | Test Description: DC Input Logic Low

Pass Limits: [0.000000000000 V to VrefCA_Volt-DcLevels_Volt V] | **VIL.CA(DC)** 219.730000000 mV

Result Details

Worst VIL	(See image)	**NumOfMeas**	10.000	**PUT**	A0	**PUT Src**	Channel 1	**Supporting Pin**	N/A
Supporting Pin Src	N/A	**PassLimit Max (VrefCA_Volt-DcLevels_Volt)**	585.000000000 mV						

Trial 1

Trial 1: Worst VIL