Freescale Semiconductor
Application Note

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LS1043A Design Checklist

1 About this document

This document provides recommendations for new designs based on the LS1043A/LS1023A, which is a cost-effective, power-efficient, and highly integrated system-on-chip (SoC) design that extends the reach of the NXP Value Performance line of QorIQ communications processors.

This document can also be used to debug newly-designed systems by highlighting those aspects of a design that merit special attention during initial system start-up.

NOTE

This document applies to the LS1043A and LS1023A. For a list of functionality differences, see the appendixes in *LS1043A/LS1023A QorIQ Integrated Multicore Communications Processor Reference Manual*.

Contents

2 Before you begin

Ensure you are familiar with the following NXP collateral before proceeding:

- LS1043A QorIQ Advanced Multicore Processor (LS1043A)
- LS1023A QorIQ Advanced Multicore Processor (LS1023A)

3 Simplifying the first phase of design

Before designing a system with the chip, it is recommended that the designer be familiar with the available documentation, software, models, and tools.

This figure shows the major functional units within the LS1043A chip.

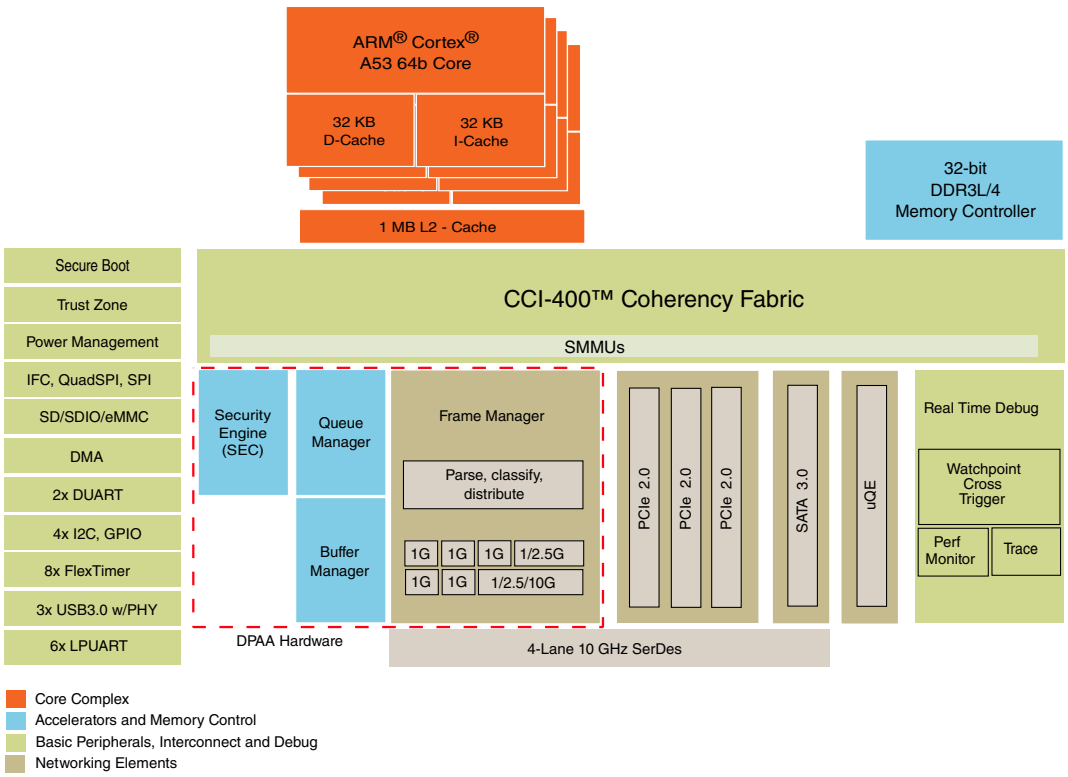

Figure 1. LS1043A block diagram

This figure shows the major functional units within the LS1023A chip.

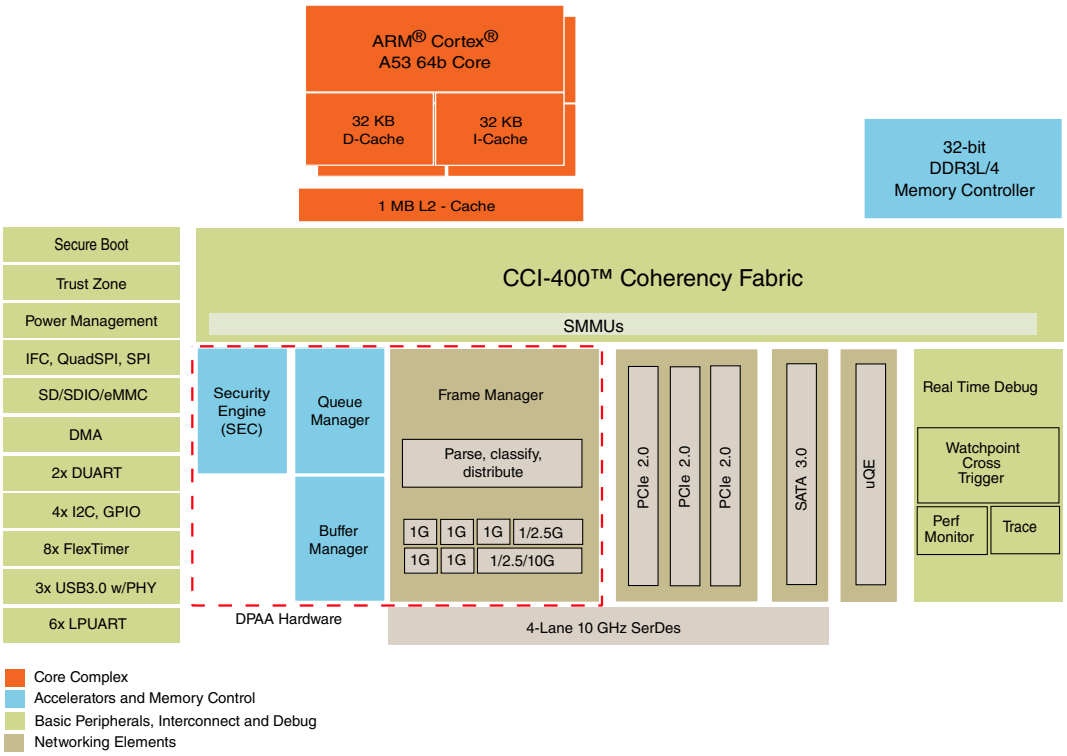

Figure 2. LS1023A block diagram

3.1 Recommended resources

This table lists helpful tools, training resources, and documentation, some of which may be available only under a non-disclosure agreement (NDA). Contact your local field applications engineer or sales representative to obtain a copy.

Table 1. Helpful tools and references

ID	Name	Location
	Related collateral	
LS1043ACE	LS1043A*Chip Errata* **NOTE:** This document describes the latest fixes and workarounds for the chip. It is strongly recommended that this document be thoroughly researched prior to starting a design with the chip.	Contact your NXP representative
LS1043A	*LS1043A/LS1023A QorIQ Integrated Multicore Processor Data Sheet*	Contact your NXP representative
QorIQ LS1043A - Fact Sheet	*LS1043A Fact Sheet*	Contact your NXP representative
LS1043ARM	*LS1043A/LS1023A Integrated Multicore Processor Family Reference Manual*	Contact your NXP representative
QorIQ LS1043A Product Brief	*LS1043A/LS1023A Product Brief*	

Table continues on the next page...

Table 1. Helpful tools and references (continued)

ID	Name	Location
AN5125	*Introduction to Device Trees - Application note*	
	Core Reference Manual	Contact your NXP representative
AN4871	*Assembly Handling and Thermal Solutions for Lidless Flip Chip Ball Grid Array Packages*	www.nxp.com
	QorIQ P1xxx series to LS1043A Migration Guide - Application Note	www.nxp.com
	Hardware and Layout Design Considerations for DDR4 SDRAM Memory Interfaces - Application Note	www.nxp.com
Software tools		
	CodeWarrior Development Software for ARM® v8 64-bit based QorIQ LS-Series Processors	www.nxp.com
	Software Development Kit for LS1043A	www.nxp.com
Hardware tools		
	CodeWarrior TAP	www.nxp.com
	QorIQ LS Processor Probe Tips for CodeWarrior TAP	www.nxp.com
	QorIQ LS1043A reference design board	www.nxp.com
Models		
IBIS	To ensure first path success, NXP strongly recommends using the IBIS models for board-level simulations, especially for SerDes and DDR characteristics.	Contact your NXP representative
BSDL	Use the BSDL files in board verification.	Contact your NXP representative
Flotherm	Use the Flotherm model for thermal simulation. Especially without forced cooling or constant airflow, a thermal simulation should not be skipped.	Contact your NXP representative
Available training		
-	Our third-party partners are part of an extensive alliance network. More information can be found at www.NXP.com/alliances.	www.nxp.com/alliances
-	Training materials from past Smart Network Developer's Forums and NXP Technology Forums (FTF) are also available at our website. These training modules are a valuable resource for understanding the chip.	www.nxp.com/alliances

3.2 Product revisions

This table lists the System Version Register (SVR) and ARM Core main ID register (TRCIDR1) values for the various chip silicon derivatives.

Table 2. Chip product revisions

Part	Device Revision	ARM® Cortex®-A53 MPCore Processor Revision	ARM Core Main ID Register	System Version Register Value	Note
LS1043A	1.0	r0p4	0x4100_0404h	0x8792_0110h	Without Security
LS1043AE	1.0	r0p4	0x4100_0404h	0x8792_0010h	With Security
LS1023AE	1.0	r0p4	0x4100_0404h	0x8792_0810h	Without Security
LS1023A	1.0	r0p4	0x4100_0404h	0x8792_0910h	With Security

4 Power design recommendations

4.1 Power pin recommendations

Table 3. Power and ground pin termination checklist

Signal name	Signal type	Used	Not used	Completed
AV_{DD}_CGA1	I	Power supply for cluster group A PLL 1 supply (1.8 V through a filter)	Must remain powered	
AV_{DD}_CGA2	I	Power supply for cluster group A PLL 2 supply (1.8 V through a filter)	Must remain powered	
AV_{DD}_D1	I	Power supply for DDR1 PLL (1.8 V through a filter)	Must remain powered	
AV_{DD}_PLAT	I	Power supply for Platform PLL (1.8 V through a filter)	Must remain powered	
AV_{DD}_SD1_PLL1	I	Power supply for SerDes1 PLL 1 (SerDes, filtered from X1VDD) (1.35 V)	Must remain powered (no need to filter from X1VDD)	
AV_{DD}_SD1_PLL2	I	Power supply for SerDes1 PLL 2 (SerDes, filtered from X1VDD) (1.35 V)	Must remain powered (no need to filter from X1VDD)	
V_{DD}	I	Core and platform supply voltage (1.0 V)		

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Table 3. Power and ground pin termination checklist (continued)

Signal name	Signal type	Used	Not used	Completed
$S1V_{DD}$	I	Core power supply for the SerDes logic transceiver	Must remain powered	
EV_{DD}	I	eSDHC[0-3]/CLK/CMD, GPIO2,LPUART2_CTS_B,LPUART2_RTS_B, LPUART3,LPUART5, LPUART6, FTM4_CH6/7,FTM4_EXTCLK/FAULT/QD_PHA/ QD_PHB (3.3 V / 1.8V)	Must remain powered	
DV_{DD}	I	DUART1/2, I2C, DMA, QE, LPUART1,LPUART2_SOUT/ SIN, LPUART4, GPIO1, GPIO4,GIC (IRQ 3/4/5/6/7/8/9/10), FTM 3/8, USB Control(DRVVBUS, PWRFAULT), FTM4_CH0/1/2/3/4/5 (3.3 V / 1.8 V)	Must remain powered	
$G1V_{DD}$	I	Power supply for the DDR3L/DDR4 (1.35 V / 1.2 V)	Must remain powered	
TV_{DD}	I	Ethernet management interface 2 (EMI2) (1.2 V / 1.8 V / 2.5 V)	Must remain powered	
LV_{DD}	I	Ethernet Interface 1/2, Ethernet management interface 1 (EMI1), TSEC_1588, GPIO1, GPIO3,FTM1/2, GIC (IRQ11) (2.5 V/1.8 V)	Must remain powered	
OV_{DD}	I	IFC, SPI, GIC (IRQ 0/1/2), Temper_Detect, System control and power management, SYSCLK,DDR_CLK, DIFF_SYSCLK, GPIO2, GPIO1,eSDHC[4-7]/VS/ DAT123_DIR/DAT0_DIR/CMD_DIR/SYNC), Debug, SYSCLK, JTAG, RTC, FTM5/6/7,POR signals (1.8 V)	Must remain powered	
X1VDD	I	Pad power supply for the SerDes transceiver (1.35 V)	Must remain powered	
TA_PROG_SFP	I	Should only be supplied 1.8V during secure boot programming. For normal operation, this pin needs to be tied to GND.		
PROG_MTR	I	Should only be supplied 1.8V during secure boot programming. For normal operation, this pin needs to be tied to GND.		
FA_VL	-	This pin must be pulled to GND	-	
TA_BB_VDD	-	Low power security monitor supply. This signal should be connected to 1.0 V always on supply.	This signal should be connected to 1.0 V switchable supply.	
TH_V_{DD}	I	Reserved. Thermal monitor unit supply (1.8 V)	Must remain powered	
USB_HV_{DD}	I	USB PHY Transceiver supply (3.3 V)	Must remain powered (No need to add filter)	

Table continues on the next page...

Table 3. Power and ground pin termination checklist (continued)

Signal name	Signal type	Used	Not used	Completed
USB_SDV_{DD}	I	Analog and Digital HS supply for USBPHY	Must remain powered (No need to add filter)	
USB_SV_{DD}	I	Analog and Digital SS supply for USBPHY	Must remain powered (No need to add filter)	
SENSEVDD	O	V_{DD} sense pin	Do not connect. This pins should be left floating.	
GND	I	Ground	Tie to GND	
SENSEGND	O	GND sense pin	Do not connect. This pins should be left floating.	
SD_GND	I	GND pin for SerDes and PLL supplies.	Tie to GND	

4.2 Power system-level recommendations

Table 4. Power design system-level checklist

Item	Completed
General	
Ensure that the ramp rate for all voltage supplies (including OV_{DD}, DV_{DD}, $G1V_{DD}$, $S1V_{DD}$, $X1V_{DD}$, LV_{DD}, EV_{DD}, TV_{DD}, OV_{DD} all core and platform VDD supplies, D1_MVREF and all AVDD supplies.) follows the recommendations as mentined in "Power-on ramp rate" table in datasheet.	
Ensure that VDD nominal voltage supply is set for 1.0 V with voltage tolerance of +/- 30 mV from the nominal VDD value. Ensure that all other power supplies have a voltage tolerance as specified in "**Recommended operating conditions** in datasheet.' [1]	
Ensure that power supply is selected based on MAXIMUM power dissipation.[1]	
Ensure the thermal design is based on THERMAL power dissipation.[1]	
Ensure the power-up sequence is within 75 ms.[1]	
Use large power planes to the extent possible.	
Ensure the PLL filter circuit is applied to AV_{DD}_PLAT, AV_{DD}_CGA1, AV_{DD}_CGA2, AV_{DD}_D1.	

Table continues on the next page...

Table 4. Power design system-level checklist (continued)

Item	Completed
If SerDes is enabled, ensure the PLL filter circuit is applied to the respective AV_{DD}_SD1_PLL1, AV_{DD}_SD1_PLL2. Otherwise, a filter is not required. Even if an entire SerDes module is not used, the power is still needed to the AV_{DD} pins. However, instead of using a filter, it needs to be connected to the XV_{DD} rail through a zero Ω resistor.	
Ensure the PLL filter circuits are placed as close to the respective AV_{DD}_SD1_PLL1, AV_{DD}_SD1_PLL2 pin as possible.	
Power supply decoupling	
Provide sufficiently-sized power planes for the respective power rail. Use separate planes if possible; split (shared) planes if necessary. If split planes are used, ensure that signals on adjacent layers do not cross splits. Avoid splitting ground planes at all costs.	
Place at least one decoupling capacitor of 0.1µF (SMT ceremic chip) at each V_{DD}, OV_{DD}, DV_{DD}, $G1V_{DD}$, $S1V_{DD}$, $X1V_{DD}$, LV_{DD}, EV_{DD}, and TV_{DD} pin of this chip	
It is recommended that the decoupling capacitors receive their power from separate V_{DD}, OV_{DD}, DV_{DD}, $G1V_{DD}$, $S1V_{DD}$, $X1V_{DD}$, LV_{DD}, EV_{DD}, and TV_{DD} and GND planes in the PCB, utilizing short traces to minimize inductance.	
Capacitors may be placed directly under the chip using a standard escape pattern, and others may surround the part.	
Ensure these capacitors have a value of at least 0.1µF. Recommended 0201.	
Only use ceramic surface-mount technology (SMT) capacitors to minimize lead inductance, preferably 0402 or 0603.	
Distribute several bulk storage capacitors around the PCB, feeding the V_{DD} and other planes (for example, DV_{DD}, EV_{DD}, LV_{DD}, and $G1V_{DD}$), to enable quick recharging of the smaller chip capacitors.	
Ensure the bulk capacitors have a low equivalent series-resistance (ESR) rating to ensure the quick response time necessary.	
Ensure the bulk capacitors are connected to the power and ground planes through two vias to minimize inductance.	
Ensure you work directly with your power regulator vendor for best values and types of bulk capacitors. The capacitors need to be selected to work well with the power supply to be able to handle the chip's power requirements. [2] Most regulators perform best with a mix of ceramic and very low ESR Tantalum type capacitors.	
As a guideline for customers and their power regulator vendors, Freescale recommends that these bulk capacitors be chosen to maintain the positive transient power surges to less than +50 mV (negative transient undershoot should comply with specification -30mV) for current steps of up to 2A with a slew rate of 1.5A/µs (10 A with a slew rate of 12A/µs).	
Additional power supply decoupling	
Use only SMT capacitors to minimize inductance.	
Connections from all capacitors to power and ground must be done with multiple vias to further reduce inductance.	
Ensure the board has at least one 0.1 µF SMT ceramic chip-capacitor as close as possible to each supply ball of the chip ($S1V_{DD}$, $X1V_{DD}$)	
Where the board has blind vias, ensure these capacitors are placed directly below the chip supply and ground connections. Where the board does not have blind vias, ensure these capacitors are placed in a ring around the chip as close to the supply and ground connections as possible.	
For all SerDes supplies: Ensure there is a 1-µF ceramic chip capacitor on each side of the chip.	

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Table 4. Power design system-level checklist (continued)

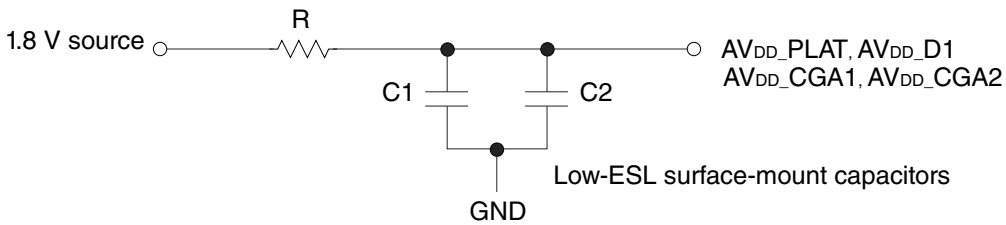
Item	Completed
For all SerDes supplies: Ensure there is a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor between the device and any SerDes voltage regulator.	
PLL power supply filtering[3]	
Provide independent filter circuits per PLL power supply, as illustrated in this figure.  • R = 5 Ω ± 5% • C1 = 10 µF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH • C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH • Low-ESL surface-mount capacitors **NOTE:** A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R, ESL ≤ 0.5 nH). **NOTE:** Voltage for AV_{DD} is defined at the input of the PLL supply filter and not the pin of AV_{DD}.	
Ensure filter circuits use surface mount capacitors with minimum effective series inductance (ESL).	
Place each circuit as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. **NOTE:** If done properly, it is possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 621 (or 780) FC-PBGA footprint, without the added inductance of vias. **NOTE:** It is recommended that an area fill or power plane split be provided to provide a low-impedance profile, which helps keep nearby crosstalk noise from inducing unwanted noise.	
Ensure each of the PLLs is provided with power through independent power supply pins (AV_{DD}_CGA1, AV_{DD}_CGA2, AV_{DD}_PLAT, AV_{DD}_D1, AV_{DD}_SD1_PLL1, and AV_{DD}_SD1_PLL2, respectively).	
For maximum effectiveness, ensure the filter circuit is placed as close as possible to the AV_{DD}_SD1_PLLn ball to ensure it filters out as much noise as possible.	
Ensure the ground connection is near the AV_{DD}_SD1_PLLn ball. The 0.003-µF capacitor is closest to the ball, followed by a 4.7-µF capacitor and 47-µF capacitor, and finally the 0.33-Ω resistor to the board supplyplane.	
To ensure stability of the internal clock, ensure the power supplied to the PLL is filtered using a circuit similar to the one shown in this figure. • AV_{DD}_SD1_PLL*n* should be a filtered version of $X1V_{DD}$. • Signals on the SerDes interface are fed from the $X1V_{DD}$ power plane. • It is recommended that an area fill or power plane split be provided for both AV_{DD} and AGND to provide a low-impedance profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Voltage for AV_{DD}_SD1_PLL*n* is defined at the PLL supply filter and not the pin of AV_{DD}_SD1_PLL*n*. • A 47 µF 0805 XR5 or XR7, 4.7 µF 0603, and 0.003 µF 0402 capacitor are recommended. The size and material type are important. A 0.33 Ω ± 1% resistor is recommended. • **Caution**: These filters are a necessary extension of the PLL circuitry and are compliant with the device specifications. Any deviation from the recommended filters is done at the user's risk.	

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Table 4. Power design system-level checklist (continued)

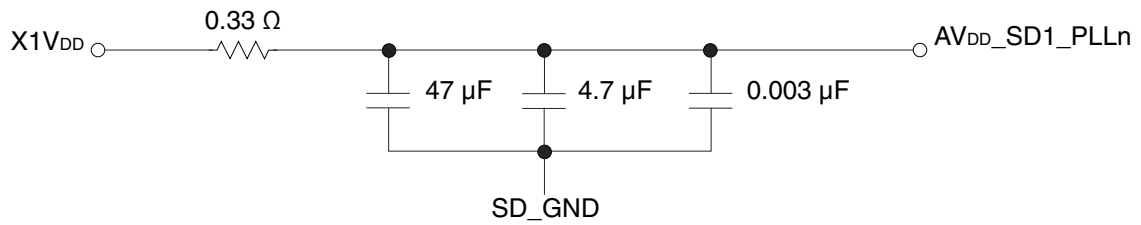
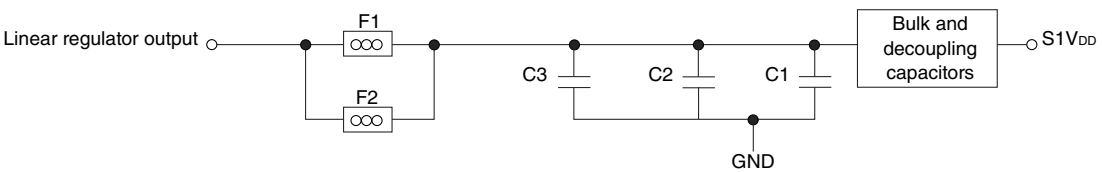
Item	Completed
 **Caution**: These filters are a necessary extension of the PLL circuitry and are compliant with the device specifications. Any deviation from the recommended filters is done at the user's risk.	
Ensure the capacitors are connected from AV_{DD}_SD1_PLLn to the ground plane.	
Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.	
Ensure AV_{DD}_SD1_PLLn is a filtered version of $X1V_{DD}$	
Ensure that signals on the SerDes interface are fed from the $X1V_{DD}$ power plane.	
$S1V_{DD}$ should be supplied by a linear regulator and needs a nominal voltage of 1.0V. An example solution for $S1V_{DD}$ filtering, where $S1V_{DD}$ is sourced from a linear regulator, is shown in the following figure. The component values in this example filter are system-dependent and are still under characterization, so component values may need adjustment based on the system or environment noise. Where: • C1 = 0.003 µF ± 10%, X5R, with ESL ≤ 0.5 nH • C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH • F1 and F2 = 120 Ω at 100 MHz 2A 25% 0603 Ferrite (for example, Murata BLM18KG121TN1) • Bulk and decoupling capacitors are added, as needed, per power supply design.  **NOTE:** See section "Power-on ramp rate" in the applicable chip data sheet for maximum SnV_{DD} power-up ramp rate. **NOTE:** There must be enough output capacitance or a soft-start feature to assure the ramp-rate requirement is met. **NOTE:** The ferrite beads should be placed in parallel to reduce voltage droop. **NOTE:** Besides a linear regulator, a low-noise-dedicated switching regulator can be used. 10 mVp-p, 50 kHz-500 MHz is the noise goal.	
$X1V_{DD}$ may be supplied by a linear regulator or sourced by a filtered $G1V_{DD}$. Systems may design-in both options to allow flexibility to address system noise dependencies. However, for initial system bring-up, the linear regulator option is highly recommended. An example solution for XnV_{DD} filtering, where XnV_{DD} is sourced from a linear regulator, is shown in the following figure. The component values in this example filter are system-dependent and are still under characterization, so component values may need adjustment based on the system or environment noise. Where: • C1 = 0.003 µF ± 10%, X5R, with ESL ≤ 0.5 nH • C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH • F1 and F2 = 120 Ω at 100 MHz 2A 25% 0603 Ferrite (for example, Murata BLM18KG121TN1) • Bulk and decoupling capacitors are added, as needed, per power supply design.	

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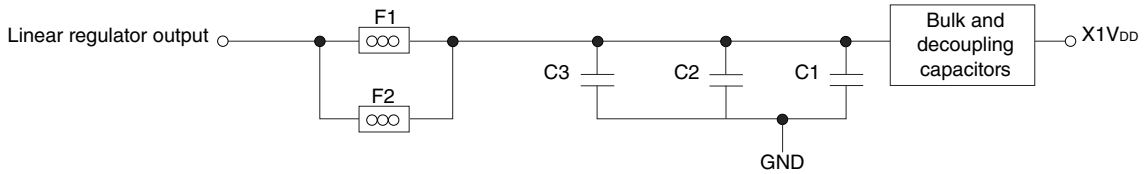
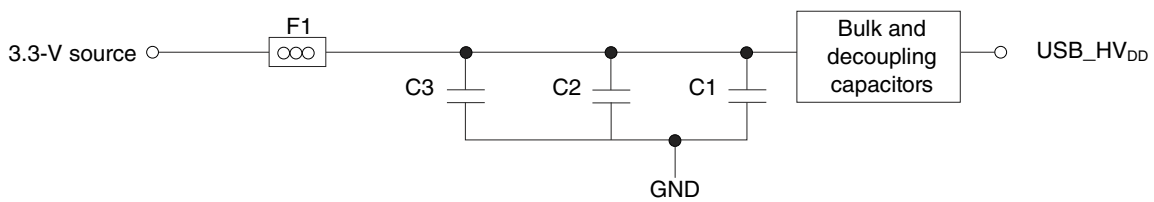
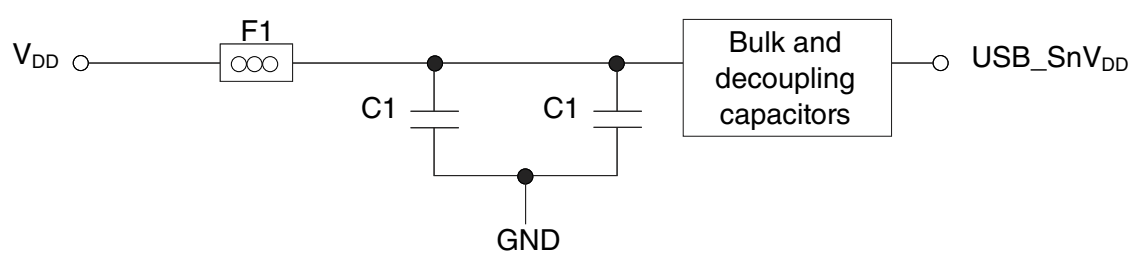
Table 4. Power design system-level checklist (continued)

Item	Completed
 **NOTE:** See section "Power-on ramp rate" in the applicable chip data sheet for maximum X*n*V_{DD} power-up ramp rate. **NOTE:** There must be enough output capacitance or a soft-start feature to assure the ramp-rate requirement is met. **NOTE:** The ferrite beads should be placed in parallel to reduce voltage droop. **NOTE:** Besides a linear regulator, a low-noise-dedicated switching regulator can be used. 10 mVp-p, 50 kHz-500 MHz is the noise goal.	
USB_HV_{DD} must be sourced by a filtered 3.3V voltage source using a star connection. An example solution for USB_HV_{DD} filtering, where USB_HV_{DD} is sourced from a 3.3V voltage source, is illustrated in the following figure. The component values in this example filter are system-dependent and are still under characterization, so component values may need adjustment based on the system or environment noise. Where: • C1 = 0.003 µF ± 10%, X5R, with ESL ≤ 0.5 nH • C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH • F1 = 120 Ω at 100 MHz 2A 25% 0603 Ferrite (for example, Murata BLM18KG121TN1) • Bulk and decoupling capacitors are added, as needed, per power supply design. 	
USB_SDV_{DD} must be sourced by a filtered V_{DD} using a star connection. An example solution for USB_SDV_{DD} filtering, where USB_SDV_{DD} is sourced from V_{DD}, is illustrated in the following figure. The component values in this example filter are system-dependent and are still under characterization, so component values may need adjustment based on the system or environment noise. Where: • C1 = 2.2 µF ± 20%, X5R, with low ESL (for example, Panasonic ECJ0EB0J225M) • F1 = 120 Ω at 100-MHz 2A 25% Ferrite (for example, Murata BLM18KG121TN1) • Bulk and decoupling capacitors are added, as needed, per power supply design 	
Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.	

1. See the applicable chip data sheet for more details.
2. Suggested bulk capacitors are 100-330 µF (AVX TPS tantalum or Sanyo OSCON).
3. The PLL power supply filter circuit filters noise in the PLLs' resonant frequency range from 500 kHz-10 MHz.

4.3 Power-on reset recommendations

Various chip functions are initialized by sampling certain signals during the assertion of PORESET_B. These power-on reset (POR) inputs are pulled either high or low during this period. While these pins are generally output pins during normal operation, they are treated as inputs while PORESET_B is asserted. When PORESET_B de-asserts, the configuration pins are sampled and latched into registers, and the pins then take on their normal output circuit characteristics.

Table 5. Power-on reset system-level checklist

Item	Completed
Ensure PORESET_B is asserted for a minimum of 1 ms.	
Ensure HRESET_B is asserted for a minimum of 32 SYSCLK cycles.	
In cases where a configuration pin has no default, use a 4.7 kΩ pull-up or pull-down resistor for appropriate configuration of the pin.	
Optional: An alternative to using pull-up and pull-down resistors to configure the POR pins is to use a PLD or similar device that drives the configuration signals to the chip when HRESET_B is asserted. The PLD must begin to drive these signals at least four SYSCLK cycles prior to the de-assertion of PORESET_B (PLL configuration inputs must meet a 100 µs set-up time to HRESET_B), hold their values for at least two SYSCLK cycles after the de-assertion of PORESET_B, and then release the pins to high impedance afterward for normal device operation **NOTE:** See the applicable chip data sheet for details about reset initialization timing specifications.	
Configuration settings	
Ensure the settings in Configuration signals sampled at reset are selected properly. **NOTE:** See the applicable chip reference manual for a more detailed description of each configuration option.	
Power sequencing	
The chip requires that its power rails be applied in a specific sequence in order to ensure proper device operation. Please refer to "QorIQ LS1043A, LS1023A Data Sheet" for details.	

4.3.1 Configuration signals sampled at reset

The signals that serve alternate functions as configuration input signals during system reset are summarized in this table.

Reset configuration signals are sampled at the negation of PORESET_B. However, there is a setup and hold time for these signals relative to the rising edge of PORESET_B, as described in the chip's data sheet document.

The reset configuration signals are multiplexed with other functional signals. The values on these signals during reset are interpreted to be logic one or zero, regardless of whether the functional signal name is defined as active-low. The reset configuration signals have internal pull-up resistors so that if the signals are not driven, the default value is high (a one), as shown in the table. Some signals must be driven high or low during the reset period. For details about all the signals that require external pull-up resistors, see the applicable device data sheet.

Table 6. LS1043A reset configuration signals

Configuration Type	Functional Pins	Comments
Reset configuration word (RCW) source inputs cfg_rcw_src[0:8]	IFC_AD[8:15] IFC_CLE	They must be set to one of the valid options. The 512 bit RCW word has all the necessary configuration information for the chip. If there is no valid RCW in the external memory, it can be programmed using the Code Warrior or other programmer. The JTAG configuration files can be used in the following situations: • target boards that do not have RCW already programmed • new board bring up • recovering boards with blank or damaged flash
IFC external transceiver enable polarity select (cfg_ifc_te)	IFC_TE	Default is "1"
DRAM type select (cfg_dram_type)	IFC_A[21]	Default is DDR3L. This reset configutation pin selects the porper I/O voltage: DDR3L=1.35V or DDR4=1.2V. Ensure the selection value that matches the DDR type used on board.
General-purpose input (cfg_gpinput[0:7])	IFC_AD[0:7]	Default "1111 1111", values can be application defined
"Single Oscillator Source" clock select. This field selects between SYSCLK (Single ended) and DIFF_SYSCLK/ DIFF_SYSCLK_B (differential) inputs. (cfg_eng_use0)	IFC_WE0_B	0=DIFF_SYSCLK/ DIFF_SYSCLK_B(differential) 1=SYSCLK (single ended) Default selection is single ended SYSCLK; "1"
"Single Oscillator Source" clock. This field indicates whether on-chip LVDS termination for differential clock is enabled or disabled. configuration (cfg_eng_use1)	IFC_OE_B	0 = Disabled (MUST make sure that External termination pads of DIFF_SYSCLK/DIFF_SYSCLK_B have proper termination) 1 = Enabled (default) Default is "1". It is recommened to keep provision for optional pull-down resistor on board.
"Single Oscillator Source" clock configuration (cfg_eng_use2)	IFC_WP0_B	Default is "1". Reserved. It is recommened to keep provision for optional pull-down resistor on board.

NOTE

1. The hardcoded RCW can be used as an alternative method for initial board bring up when there is no valid RCW in the external memory. For more information, see the hardcoded RCW table below.

This table shows the some basic hardcoded RCW values. For details please refer to LS1043A Reference Manual.

Table 7. Hardcoded RCW values

Harcoded RCW		
cfg_rcw_src[0:8]	9'b0_1001_1010 (0x9A)	9'b0_1001_1110 (0x9E)
SYSCLK (MHz)	66	100
DDRCLK (MHz)	100	100
PLL configuration		
SYS_PLL_RAT	4:1	3:1
RCW[2:6]	5'd4	5'd3
MEM_PLL_RAT	13:1	13:1
RCW[10:15]	6'd13	6'd13
CGA_PLL1_RAT	18:1	12:1
RCW[26:31]	6'd18	6'd12
CGA_PLL2_RAT	15:1	10:1
RCW[34:39]	6'd15	6'd10
C1_PLL_SEL	CGA_PLL1 / 1	CGA_PLL1 / 1

If a new board is using a blank flash and flash is the source of RCW, then the all 0xff value from flash for RCW will put the device in an unknown state.

There are two methods to work around this problem:

1. Put switches on cfg_rcw_src signals to choose hardcoded RCW(0x9A, 0x9E).

2. Use CodeWarrior tool from Freescale to override RCW."

5 Interface recommendations

5.1 DDR controller recommendations

LS1043A/LS1023A supports DDR3L(1.35V) and DDR4(1.2V) SDRAM

The memory interface controls main memory accesses. The interface supports 32 bit data access.

5.1.1 DDR controller pin termination recommendations

Table 8. DDR controller pin termination checklist

Signal Name[1]		I/O type	Used	Not used	Completed
DDR3L Signal	**DDR4 Signal**				
D1_MA[13:00]	D1_MA[13:00]	O	Must be properly terminated to VTT	These pins can be left unconnected.	
D1_MA[14]	D1_MBG1				
D1_MA[15]	D1_MACT_B				

Table continues on the next page...

Table 8. DDR controller pin termination checklist (continued)

Signal Name[1]		I/O type	Used	Not used	Completed
DDR3L Signal	DDR4 Signal				
D1_MBA[0:1] D1_MBA[2]	D1_MBA[0:1] D1_MBG0	O	Must be properly terminated to VTT	These pins can be left unconnected.	
D1_MCK[0:1]/D1_MCK[0:1]_B		O	These pins must be properly terminated.	These pins may be left unconnected.	
D1_MCKE[0:1]		O	Must be properly terminated to VTT These pins are actively driven during reset instead of being released to high impedance.	These pins can be left unconnected.	
D1_MCS[0:3]_B		O	Must be properly terminated to VTT	These pins can be left unconnected.	
D1_MDIC[0:1]		I/O	• These pins are used for automatic calibration of the DDR3L/DDR4 IOs. The MDIC[0:1] pins must be connected to 162Ω precision 1% resistors. • MDIC[0] is grounded through a 162Ω precision 1% resistor and MDIC[1] is connected to GV_{DD} through a 162Ω precision 1% resistor. • For either full- or half-driver strength calibration of DDR IOs, use the same MDIC resistor value of 162 Ω. • The memory controller register setting can be used to determine if automatic calibration is done to full- or half-drive strength.	These pins can be left unconnected.	
D1_MDM[0:3], D1_MDM[8]		O	-	These pins can be left unconnected.	
D1_MDQ[0:32]		I/O	-	These pins can be left unconnected.	
D1_MDQS[0:3]/D1_MDQS[0:3]_B, D1_MDQS[8]/D1_MDQS[8]_B		I/O	-	These pins can be left unconnected.	
D1_MECC[0:3]		I/O	-	These pins can be left unconnected.	
D1_MAPAR_ERR_B	D1_MALERT_B	O	This pin is an open drain output from registered DIMMs. Ensure that a 2-10 kΩ pull-up to $G1V_{DD}$ is present on this pin.	This pin should be pulled up.	

Table continues on the next page...

Table 8. DDR controller pin termination checklist (continued)

Signal Name[1]		I/O type	Used	Not used	Completed
DDR3L Signal	DDR4 Signal				
D1_MAPAR		O	If the controller supports the optional MAPAR and MAPAR_ERR signals, ensure that they are hooked up as follows: • MAPAR_OUT (from the controller) => PAR_IN (at the RDIMM) • ERR_OUT (from the RDIMM) => MAPAR_ERR (at the controller)	This pin can be left unconnected.	
D1_MODT[0:1]		O	Ensure the MODT signals are connected correctly. Two dual ranked DIMMs topology is not supported on LS1043A. For a single, dual-ranked DIMM, consider the following connections • MODT(0), MCS(0), MCKE(0) • MODT(1), MCS(1), MCKE(1) For quad-ranked DIMMS, it is recommended to obtain a data sheet from the memory supplier to confirm required signals. But in general, each controller needs MCS(0:3), MODT(0:1), and MCKE(0:1) connected to the one quad-ranked DIMM. These pins are actively driven during reset instead of being released to high impedance.	These pins can be left unconnected.	
D1_MRAS_B		O	Must be properly terminated to VTT	This pin can be left unconnected.	
D1_MCAS_B		O	Must be properly terminated to VTT	This pin can be left unconnected.	
D1_MWE_B		O	Must be properly terminated to VTT	This pin can be left unconnected.	
D1_MVREF	DDR4 Vref is provided internally, the external vref signal needs to be grounded when using DDR4 SDRAM	I	DDR reference voltage: 0.49 x GV_{DD} to 0.51 x $G1V_{DD}$. D1_MVREF can be generated using a divider from $G1V_{DD}$ as MVREF. Another option is to use supplies that generate $G1V_{DD}$, VTT, and D1_MVREF voltage. These methods help reduce differences between	This pin must be connected to GND.	

Table 8. DDR controller pin termination checklist

Signal Name[1]		I/O type	Used	Not used	Completed
DDR3L Signal	DDR4 Signal				
			$G1V_{DD}$ and MVREF. D1_MVREF generated from a separate regulator is not recommended, because D1_MVREF does not track $G1V_{DD}$ as closely.		

1. DDR3L signals are muxed with DDR4 signals and shown in this table

5.1.2 DDR system-level recommendations

Table 9. DDR system-level checklist

Item	Completed
General	
DDR3L /DDR4 mode selection is through por-config signal cfg_dram_type. Ensure that the pin is configured correctly as per the DDR mode. Setting DDR4 mode while applying GVdd=1.35V can lead to damage of IO's.	
Data Bus inversion (DBI) signals are muxed on Data Mask (D1_MDM) signals and are optional function for DDR4. Only one function can be used at a time.	
PORESET_B assertion should also reset SDRAM Memory.	

NOTE

1. Stacked memory for DDR4 are not supported
2. DDR4 RDIMM are not supported.
3. For devices with 4 ECC pins, ensure to connect one of the ECC pins to the Prime DQ of ECC DRAM.

5.2 IFC pin termination recommendations

Table 10. IFC pin termination checklist

Signal name	I/O type	Used	Not used	Completed
IFC_A[16:20]	O	These pins must not be pulled down during power-on reset. It may be pulled up, driven high, or if there are no externally connected devices, left in tristate. If these pins are connected to a device that pulls down during reset, an external pull-up is required to drive these pins to a safe state during reset.		
IFC_A[21]	O	This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. The pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		

Table continues on the next page...

Table 10. IFC pin termination checklist (continued)

Signal name	I/O type	Used	Not used	Completed
IFC_A[22:27]	I/O	Connect as needed.	These pins can be left unconnected.	
IFC_AD[0:15]	I/O	These pins are reset configuration pins. They have a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. These pull-ups are designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		
IFC_PAR[0:1]	I/O	Connect as needed.	These pins can be left unconnected.	
IFC_CS[0:3]_B	O	Recommend weak pull-up resistors (2–10 kΩ) be placed on these pins to OV_{DD}.	These pins can be left unconnected.	
IFC_WE[0]_B	O	These pins are reset configuration pins, they have a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. The internal pull-ups are designed such that it can be overpowered by an external 4.7 kΩ resistor. However, It is recommended to keep a provision for optional pull-up and pull-down resistor on board.		
IFC_OE_B	O			
IFC_WP[0]_B	O			
IFC_PERR_B	O	Connect as needed.	These pins can be left unconnected.	
IFC_BCTL	O	Connect as needed.	This pin can be left unconnected.	
IFC_TE	O	This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		
IFC_NDDQS	I/O	Connect as needed.	This pin can be left unconnected.	
IFC_AVD	O	This pin must not be pulled down during power-on reset. It may be pulled up, driven high, or if there are no externally connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.		
IFC_CLE	O	This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		
IFC_RB[0:1]_B	I	These pins should be pulled high through a 1 kΩ resistor to OV_{DD}.	These pins should be pulled high through a 1 kΩ resistor.	

Table continues on the next page...

Table 10. IFC pin termination checklist (continued)

Signal name	I/O type	Used	Not used	Completed
IFC_CLK[0:1]	O	Connect as needed.	This pin can be left unconnected.	
IFC_NDDDR_CLK	O	Connect as needed	This pin can be left unconnected.	

NOTE

IFC interface is on OVDD power domain which is 1.8V only

For functional connection diagram, refer chip reference manual.

5.3 DUART pin termination recommendations

Table 11. DUART pin termination checklist

Signal name	I/O type	Used	Not used	Completed
UART1_SOUT	O	The functionality of these pins isdetermined by the UART_BASEand UART_EXT fields in the resetconfiguration word(RCW[UART_BASE],RCW[UART_EXT]).	These pins can be left unconnected.	
UART1_RTS_B	O			
UART1_SIN	I		Program as GPIO and output.	
UART1_CTS_B	I		This pin should be pulled high through a 2-10 kΩ resistor to DV_{DD} or else programmed as GPIO and output	
UART2_SOUT	O		This pin can be left unconnected.	
UART2_RTS_B	O			
UART2_SIN	I		Program as GPIO and output.	
UART2_CTS_B	I		This pin should be pulled high through a 2-10 kΩ resistor to DV_{DD} or else programmed as GPIO and output	
UART3_SOUT	O		This pin can be left unconnected.	
UART3_SIN	I		Program as GPIO and output.	
UART4_SOUT	O		This pin can be left unconnected.	
UART4_SIN	I		Programas GPIO and output.	

5.4 LPUART pin termination recommendations

Table 12. LPUART pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
LPUART[1:3]_CTS_B	I	The functionality of LPUART1_CTS_B is determined by the UART_BASE and	Program as GPIOs and outputs.	

Table continues on the next page...

Table 12. LPUART pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
		UART_EXT fields in the reset configuration word (RCW[UART_BASE], RCW[UART_EXT]). The functionality of LPUART[2:3]_CTS_B is determined by the SDHC_BASE and SDHC_EXT fields in the reset configuration word (RCW[SDHC_BASE], RCW[SDHC_EXT]).		
LPUART[1:3]_RTS_B	O	The functionality of LPUART1_RTS_B is determined by the UART_BASE and UART_EXT fields in the reset configuration word (RCW[UART_BASE], RCW[UART_EXT]). The functionality of LPUART[2:3]_RTS_B is determined by the SDHC_BASE and SDHC_EXT fields in the reset configuration word (RCW[SDHC_BASE], RCW[SDHC_EXT]).	Program as GPIOs and outputs.	
LPUART[1:6]_SIN	I	The functionality of LPUART[1:2]_SIN and LPUART[4]_SIN is determined by the UART_BASE and UART_EXT fields in the reset configuration word (RCW[UART_BASE], RCW[UART_EXT]). The functionality of LPUART[5:6]_SIN and LPUART[3]_SIN is determined by the SDHC_BASE and SDHC_EXT fields in the reset configuration word (RCW[SDHC_BASE], RCW[SDHC_EXT]).	Program as GPIOs and outputs.	
LPUART[1:6]_SOUT	O	The functionality of LPUART[1:2]_SOUT and LPUART[4]_SOUT is determined by the UART_BASE and UART_EXT fields in the reset configuration word (RCW[UART_BASE], RCW[UART_EXT]). The functionality of LPUART[5:6]_SOUT and LPUART[3]_SOUT is determined by the SDHC_BASE and SDHC_EXT fields in the reset	Program as GPIOs and outputs.	

Table 12. LPUART pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
		configuration word (RCW[SDHC_BASE], RCW[SDHC_EXT]).		

5.5 I2C pin termination recommendations

Table 13. I2C pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
IIC1_SDA	I/O	Tie these open-drain signals high through a nominal 1 kΩ resistor to DV_{DD}. Optimum pull-up value depends on the capacitive loading of external devices and required operating speed.	These pins should be pulled high through a 2-10 kΩ resistor to DV_{DD}.	
IIC1_SCL	I/O			
IIC2_SDA	I/O	The functionality of this signal is determined by the IIC2_EXT and IIC2_BASE field in the reset configuration word (RCW[IIC2_EXT]) and (RCW[IIC2_BASE]). Recommendthat a weak pull-up resistor (1 kΩ)be placed on this pin to theres pective power supply.This pin is an open-drain signal.	If I2C2 is not used, all pins can be programmed as GPIO's and output.	
IIC2_SCL	I/O			
IIC3_SDA	I/O	The functionality of this signal is determined by the SCFG_RCWPMUXCR0 register. Recommend that a weak pull-up resistor (1 kΩ)be placed on this pin to theres pective power supply.This pin is an open-drain signal.	If I2C3 is not used, all pins can be programmed as GPIO's and output.	
IIC3_SCL	I/O			
IIC4_SDA	I/O	The functionality of this signal is determined by the SCFG_RCWPMUXCR0 register. Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to theres pective power supply.This pin is an open-drain signal.	If I2C4 is not used, all pins can be programmed as GPIO's and output.	
IIC4_SCL	I/O			

5.6 eSDHC recommendations

The LS1043A/LS1023A eSDHC interface supports a large variety of devices

- SDXC cards Upto 2TB space, with UHS-I speed grade
- UHS-I (Ultra high speed grade) SDR12, SDR25, SDR50, SDR104, DDR50 are supported
- UHS-I cards work on 1.8V signaling

- On board dual voltage regulators are needed to support UHS-I cards because card initialization happens at 3.3V and regular operations happen at 1.8V. SD controller provides a signal to control the voltage regulator, controlled via SDHC_VS bit
- eMMC 4.5 is supported (HS200, DDR)

Table 14. Supported SD card Modes

Mode	1 bit support		4 bit support		8 bit support
	LS1043A/ LS1023A	SD (3.0)	LS1043A/ LS1023A	SD (3.0)	
DS (Default Speed)	Yes	Yes	Yes	Yes	Neither Supported By SD standards nor by LS1043A/LS1023A
HS (High Speed)	Yes	Yes	Yes	Yes	
SDR12	No	No	Yes	Yes	
SDR25	No	No	Yes	Yes	
SDR50	No	No	Yes	Yes	
SDR104	No	No	Yes	Yes	
DDR50	No	No	Yes	Yes	

Table 15. Supported MMC/eMMC Modes

Mode	1 bit support		4 bit support		8 bit support	
	LS1043A/ LS1023A	eMMC(4.5)	LS1043A/ LS1023A	eMMC(4.5)	LS1043A/ LS1023A	eMMC(4.5)
DS (Default Speed)	Yes	Yes	Yes	Yes	Yes	Yes
HS(High Speed)	Yes	Yes	Yes	Yes	Yes	Yes
HS200	No	No	Yes	Yes	Yes	Yes
DDR	No	No	Yes	Yes	No	Yes

5.6.1 eSDHC pin termination recommendations

Table 16. eSDHC pin termination checklist

Signal name	I/O type	Used	Not used	Completed
SDHC_CMD	I/O	This pin should be pulled high through a 10-100 kΩ resistor to EV_{DD}. The functionality is determined by the SDHC_BASE field in the reset configuration word (RCW[SDHC_BASE]).	Program as GPIO and output.	
SDHC_CLK	O	The functionality is determined by the SDHC_BASE field in the reset configuration word (RCW[SDHC_BASE]).		
SDHC_DATA[0]	I/O	These pins should be pulled high through a 10-100 kΩ resistor to EV_{DD}.	Program as GPIO and output.	

Table continues on the next page...

Table 16. eSDHC pin termination checklist (continued)

Signal name	I/O type	Used	Not used	Completed
SDHC_DATA[1:3]	I/O	The functionality is determined by the SDHC_BASE field in the reset configuration word (RCW[SDHC_BASE]).	Unused pins should be pulled high through a 10-100 kΩ resistor to EV_{DD}.	
SDHC_DATA[4:7]	I/O	These pins should be pulled high through 10-100 kΩ resistors to OV_{DD}. The functionality is determined by the SPI_BASE field in the reset configuration word (RCW[SPI_BASE]).	Program as GPIO's and output.	
SDHC_CD_B	I	These pins should be pulled high through 10-100 kΩ resistors to DV_{DD}. The functionality is determined by the SDHC field in the reset configuration word (RCW[IIC2_EXT]).	These pins should be pulled high through a 10-100 kΩ resistor to DV_{DD} or Program as GPIO's and output.	
SDHC_WP	I			
SDHC_CMD_DIR	O	These pins should be pulled high through 10-100 kΩ resistors to OV_{DD}. The functionality is determined by the SPI_EXT field in the reset configuration word (RCW[SPI_EXT]). **NOTE:** DIR signals are used as direction controls of external voltage translator	Pins can be programmed for other functions or GPIO and output.	
SDHC_DAT0_DIR	O			
SDHC_DAT123_DIR	O			
SDHC_VS	O	These pins should be pulled high through 10-100 kΩ resistors to OV_{DD}. The functionality isdetermined by theSPI_BASE field andSPI_EXT field in thereset configuration word(RCW[SPI_BASE] andRCW[SPI_EXT]). **NOTE:** External voltage select, to change voltage of external regulator	Can be left floating or programmed for other function.	
SDHC_CLK_SYNC_IN	I	The functionality isdetermined by theSPI_BASE field andSPI_EXT field in thereset configuration word(RCW[SPI_BASE] andRCW[SPI_EXT]).	If signal is not used, pin can be programmed as output for other functions or pulled down using a weak resistor.	
SDHC_CLK_SYNC_OUT	O	The functionality isdetermined by theSPI_BASE field andSPI_EXT field in thereset configuration word(RCW[SPI_BASE] andRCW[SPI_EXT]).	Can be left floating or programmed for other function.	

NOTE

1. Separate DIR signals are implemented to support card interrupt on DAT1 in single bit mode.
2. SDHC_CLK_SYNC_OUT to SDHC_CLK_SYNC_IN connection is required in SDR50 and DDR50 mode only.

3. In SDR50 and DDR50 mode all the input signals are sampled with respect to SDHC_CLK_SYNC_IN
4. SDHC_CLK_SYNC_OUT and SDHC_CLK_SYNC_IN should be routed as close as possible to card, with minimum skew with respect to SD_CLK.
5. When using 8-bit MMC/eMMC configuration, EVDD and OVDD should be set at same voltage

5.6.2 eSDHC system-level recommendations

Table 17. eSDHC system-level checklist

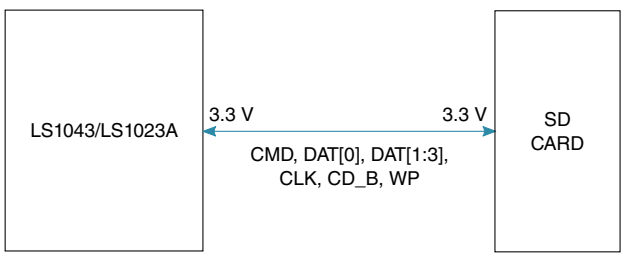
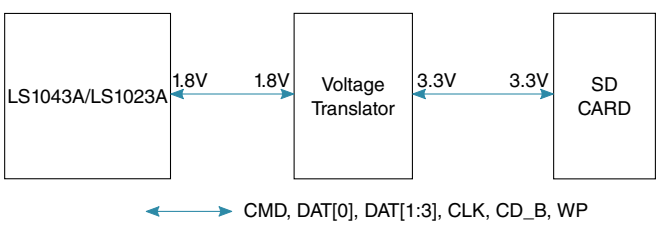
Item	Completed
SD Card interfacing (8 bit is not supported)	
SD Card Connections (DS and HS mode) EVDD configured for 3.3V  **Figure 3. DS and HS modes**	
SD Card Connections (DS and HS modes with voltage translator) EVDD configured for 1.8V  **Figure 4. DS and HS modes**	
SD Card Connections (SDR12, 25, 50, 104 and DDR50 Modes without voltage translator) UHS-I modes, work on 1.8V signalling. SYNC_OUT, SYNC_IN connections are required in SDR50, DDR50 modes only **NOTE:** Resistor R=10K is needed when RCW loading is required to be done from SD card	

Table continues on the next page...

Table 17. eSDHC system-level checklist (continued)

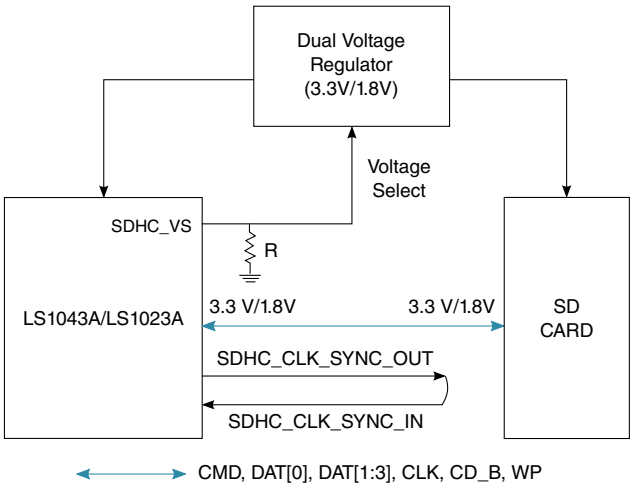
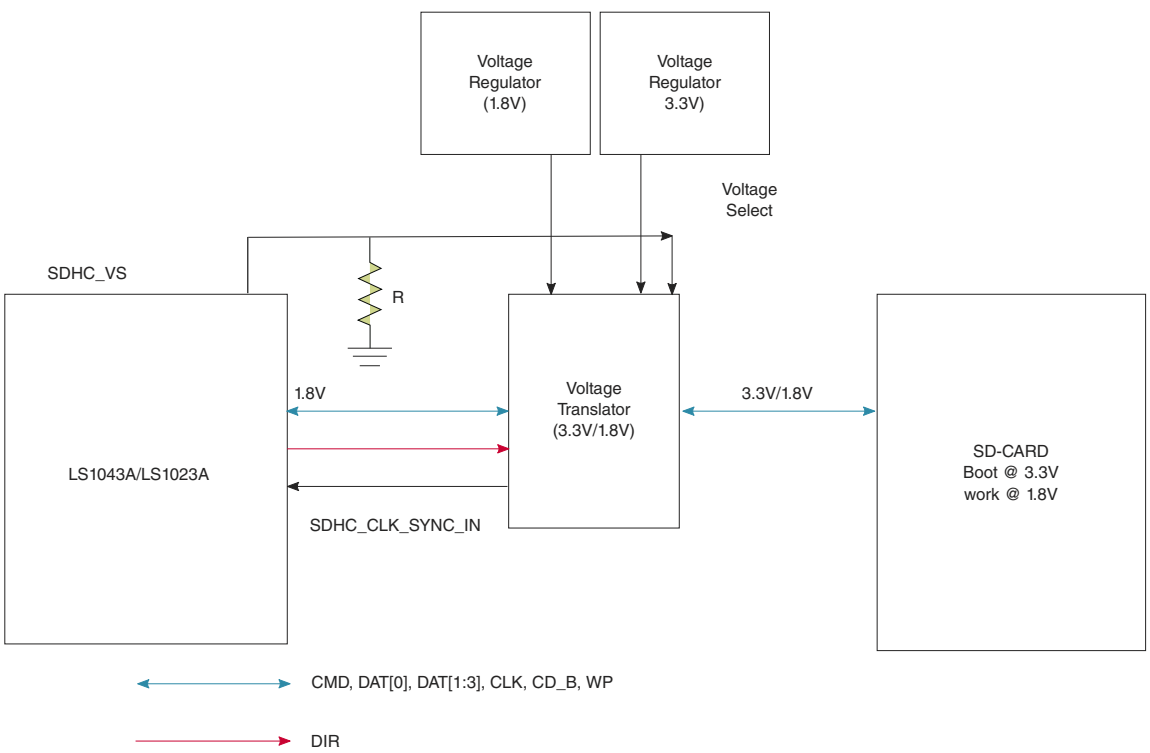
Item	Completed
 **Figure 5. SDR12, 25, 50, 104 and DDR50 modes**	
SD Card Connections (SDR12, 25, 50, 104 and DDR50 Modes with voltage translator) UHS-I modes, work on 1.8V signalling. SYNC_IN connections are required in SDR50, DDR50 modes only **NOTE:** Resistor R=10K is needed when RCW loading is required to be done from SD card. .  **Figure 6. SDR12, 25, 50, 104 and DDR50 modes**	
eMMC Interfacing	

Table continues on the next page...

Table 17. eSDHC system-level checklist (continued)

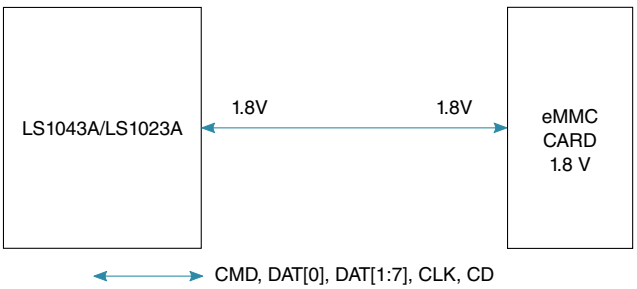
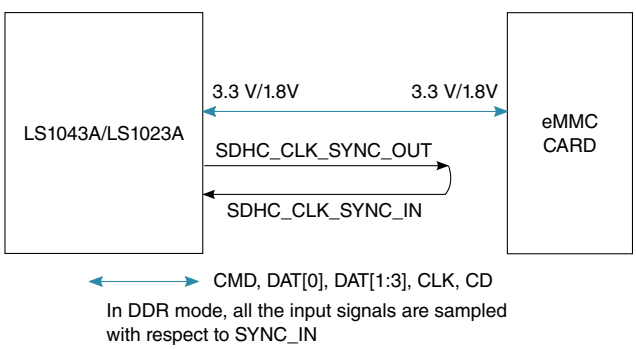
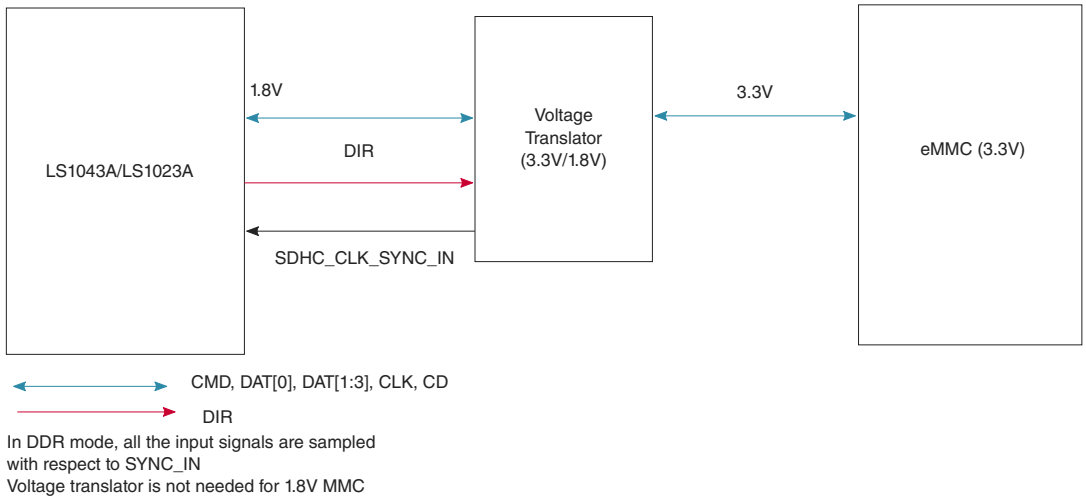
Item	Completed
eMMC Card Connections (DS, HS, HS200 Modes) @ 1.8 V Card 8-bit eMMC requires EVDD and OVDD configured at same voltage. Switch to 1.8 V operation  **Figure 7. DS, HS, HS200 modes for eMMC (1.8 v)** **NOTE:** 1. Voltage translator requirment depends upon the chosen eMMC voltage and OVDD/EVDD voltage configuration 2. HS200 mode is 1.8V only mode as per eMMC 4.5 specification	
eMMC Card Connection in DDR mode 8 bit operation cannot be supported due to pin multiplexing constraints DDR mode supports both 3.3 V and 1.8 V operation as per eMMC 4.4 specification Different AC timings are supported at 3.3 V/1.8 V, refer device data sheet for details  **Figure 8. DDR mode without voltage translator**	

Table 17. eSDHC system-level checklist

Item	Completed
 **Figure 9. DDR mode with voltage translator**	

5.7 Global Interrupt Controller (GIC) recommendations

Note that the GIC pins in LS1043/LS1023A are distributed over several voltage domains. Some GIC signals can be used to generate interrupt for wake up from deep sleep mode.

5.7.1 GIC pin termination recommendations

Table 18. GIC pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
IRQ[0:2]	I	Ensure these pins are driven in the non-asserted state.	These pins should be tied high through a 2-10 kΩ resistor to OV_{DD}.	
IRQ[3:10]	I	The functionality is determined bythe IRQ_BASE and IRQ_EXT field inthe reset configuration word(RCW[IRQ_BASE] andRCW[IRQ_EXT]).	These pins should be pulled high through a 2-10 kΩ resistor to DV_{DD} or else programmed as GPIO's and output.	
IRQ[11]	I	The functionality is determined bythe IRQ_BASE and IRQ_EXT field inthe reset configuration word(RCW[IRQ_BASE] andRCW[IRQ_EXT]).	These pins should be pulled high through a 2-10 kΩ resistor to LV_{DD} else programmed as GPIO's and output.	
IRQ_OUT_B	O	The functionality of this signal is determined by the IRQ_OUT field in the reset configuration word (RCW[IRQ_OUT]).	If unused it may be left floating.	

Table 18. GIC pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
		Tie this open-drain signal high through a weak pull-up resistor (2-10 kΩ) to OV_{DD}.		

5.8 Trust pin termination recommendations

Table 19. Trust pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
TA_BB_TMP_DETECT_B	I	If a tamper sensor is used, it must maintain the signal at the specified voltage (1.0V) until a tamper is detected. A 1 kΩ pull-down resistor is strongly recommended. If trust is used without tamper sensors tie high.	Tie this pin to ground (GND). This forces the SecMon to enter the non-secure state.	
TA_TMP_DETECT_B	I	If a tamper sensor is used, it must maintain the signal at the specified voltage (OVDD) until a tamper is detected. A 1 kΩ pull-down resistor is strongly recommended. If trust is used without temper sensors tie high.	Tie this pin to ground (GND). This forces the SecMon to enter the non-secure state.	
TA_BB_RTC	I	Pull low through a 2-10kΩ resistor to GND.	Pull low through a 2-10kΩ resistor to GND.	

5.9 Power Management pin termination recommendations

Table 20. Power Management pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
ASLEEP	O	This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. The internal pull-up resistor value for applicable IFC pins is ~33kΩ. This pull-up is designed such that it can be over powered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed. The functionality of this signal is determined by the ASLEEP field in the reset configuration word (RCW[ASLEEP]).		

5.10 Debug and reserved pin recommendations

5.10.1 Debug and reserved pin termination recommendations

Table 21. Debug and test pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
SCAN_MODE_B	I	This is a test signal for factory use only and must be pulled up (100 Ω-1 kΩ) to OV_{DD} for normal device operation.		
TEST_SEL_B	I	This pin must be pulled to OVDD through a 100-ohm to 1k-ohm resistor for a 4 core LS1043A and tied to ground for a 2 core LS1023A device.		
EVT_B[0:4]	I/O	These pins have a weak (~20KΩ) internal pull-up P_FET that is always enabled.	Pull high through a 2-10kΩ resistor to OVDD.	
EVT_B[5:8]	I/O	The functionality of these signals is determined by the IIC3 and IIC4 field in the SCFG_RCWPMUXCR0 register	EVT[5:8] can be programmed as GPIO outputs through SCFG_RCWPMUXCR0 bits and left floating	
EVT_B[9]	I/O	This pin should be pulled high through a 2-10 kΩ resistor to OVDD. The functionality of this signal is determined by the IRQ_OUT field in the reset configuration word (RCW[IRQ_OUT]).	EVT_B[9] can be programmed as output through RCW[IRQ_OUT] bit and left floating (naveenm)	
JTAG_BSR_VSEL	I	Depending upon the requirement, this pin should either be pulled up to OVDD (through a 2 - 4.7 kΩ resistor) OR should an pulled down to ground (through 4.7 kΩ resistor).		
TBSCAN_EN_B	I	Depending upon the requirement, this pin should either be pulled up to OVDD (through a 2 - 4.7 kΩ resistor) OR should an pulled down to ground (through 4.7 kΩ resistor).		
CKSTP_OUT_B	O	This pin is an open drain signal and should be pulled high through a 2-10 kΩ resistor to OVDD.		
FA_VL	-	Reserved. This pin must be pulled to ground (GND).		
PROG_MTR	-	Reserved. This pin must be pulled to ground (GND).		
FA_ANALOG_G_V	-	Reserved. This pin must be pulled to ground (GND).		
FA_ANALOG_PIN	-	Reserved. This pin must be pulled to ground (GND).		
TH_TPA	-	Do not connect. This pin should be left floating.		
TD1_ANODE	-	Connect as required.	Tie to GND if not used.	
TD1_CATHODE	-	Connect as required.	Tie to GND if not used.	

NOTE

1. JTAG standard allows the BSR mode to be entered anytime during the functioning of the chip OR even prior to PORESET de-assertion of the chip. If BSR mode is entered duing the normal functioning of the chip, the pads have already been configured for appropriate voltage levels. If BSR mode is entered even prior to PORESET, the pads may have not been configured to adjust to applied voltages, therefore it becomes necessary to put the pads in safe mode (auto mode).

JTAG_BSR_VSEL is sampled at the de-assertion of TRST_B, if this pad is set to OVDD then pads are put to “auto mode”. An auto-mode is the state which prepares and protects pads against any overvoltage damage. For example if the pad is configured to work at 1.8/2.5V and the applied voltage is 3.3V then there is a chance that pads undergoes stress. When in Auto-Mode, the pads can be subjected to maximum allowable voltage without damage/stress. .

2. TBSCAN_EN=0 means only FSL TAP connected to JTAG interface; TBSCAN_EN=1 means FSL TAP in series with DAP.

5.11 Analog Signals pin termination recommendations

Table 22. Analog Signals pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
D1_MVREF	IO	DDR reference voltage: 0.49 x GVDD to 0.51 x G1VDD. D1_MVREF can be generated using a divider from GVDD as MVREF. Another option is to use supplies that generate GVDD, VTT, and D1_MVREF voltage. These methods help reduce differences between GVDD and MVREF. D1_MVREF generated from a separate regulator is not recommended, because D1_MVREF does not track GVDD as closely.	-	
D1_TPA	IO	Do not connect. These pins should be left floating.		

5.12 SerDes pin termination recommendations

Table 23. SerDes pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
SD1_IMP_CAL_RX	I	Tie to S1VDD through a 200 Ω 1% resistor.	If the SerDes interface is entirely unused, the unused pin must be left unconnected.	
SD1_IMP_CAL_TX	I	Tie to X1VDD through a 698 Ω 1% resistor.	If the SerDes interface is entirely unused, the unused pin must be left unconnected.	
SD1_PLL1_TPA	O	Provide a test point if possible. These pins should be left floating		
SD1_PLL1_TPD	O	Provide a test point if possible. These pins should be left floating		
SD1_PLL2_TPA	O	Provide a test point if possible. These pins should be left floating		
SD1_PLL2_TPD	O	Provide a test point if possible. These pins should be left floating		

Table continues on the next page...

Table 23. SerDes pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
SD1_REF_CLK1_P SD1_REF_CLK1_N	I	Ensure clocks are driven from anappropriate clock source, as per the default allocation with the RCW settings. PLL1 can support 100, 125 and 156.25 MHz. In addition to PCIe, SATA, SGMII, QSGMII which require 100/125 MHz, it can also support XFI. 2.5 G SGMII required 125 MHz or 156.25 MHz, therefore can be supported only by PLL1 if 156.25 MHz is chosen.	If the SerDes lanes are unused, connect to SD_GND, where *1* corresponds to the unused SerDes lanes.	
SD1_REF_CLK2_N SD1_REF_CLK2_P	I	Ensure clocks are driven from anappropriate clock source, as per the default allocation with the RCW settings. PLL2 supports only 100 and 125 MHz frequency therefore has support limited to PCIe SGMII and QSGMII.	If the SerDes lanes are unused, connect to SD_GND,	
SD1_RX[0:3]_N	I	Ensure pins are correctly terminated for the interface type used.	If the SerDes interface is entirely or partly unused, the unused pins must be connected to SD_GND.	
SD1_RX[0:3]_P	I	Ensure pins are correctly terminated for the interface type used.	If the SerDes interface is entirely or partly unused, the unused pins must be connected to SD_GND.	
SD1_TX[0:3]_N	O	Ensure pins are correctly terminated for the interface type used.	If SerDes interface is entirely or partly unused, the unused pins must be left unconnected.	
SD1_TX[0:3]_P	O	Ensure pins are correctly terminated for the interface type used.	If SerDes interface is entirely or partly unused, the unused pins must be left unconnected.	

NOTE

1. In the RCW configuration field SRDS_PLL_PD_S1, the respective bits for each unused PLL must be set to power it down. The SerDes module is disabled when both of its PLLs are turned off.

2. After POR, if an entire SerDes module is unused, it must be powered down by clearing the SDEN fields of its corresponding PLL1 and PLL2 reset control registers (SRDSxPLLaRSTCTL).

3.Unused lanes must be powered down by clearing the RRST_B and TRST_B fields and setting the RX_PD and TX_PD fields in the corresponding lane's general control register (SRDSxLNmGCR0).

4. A spread-spectrum reference clock is permitted for PCI Express. However, if any other high-speed interface, such as SGMII or SATA, is used concurrently on the same SerDes bank, spread-spectrum clocking is not permitted.

5. **Select the optimal setting for the SerDes channel Rx Equalization Boost bit suitable for a particular end product system board**

Description:

For certain high speed SerDes protocols, the Rx Equalization Boost bits for all the SerDes lanes in use are initialized with a default value of 1b by the RCW. In reality, although the default 1b setting does overlap with the 0b setting in terms of Rx Equalization boost effect, the 0b setting works better for short and normal SerDes channels, while the 1b setting works better for high loss channels.

For end product system with non-high loss SerDes channels (lanes), using the default 1b setting of the Rx Equalization Boost bit may adversely enhance the return loss due to some discontinuities possibly presented in the channel. This may further causes more reflection. Therefore, unless the channel is high loss, to ensure the channel's health and better performance, the 0b setting of Rx Equalization Boost bit should be used for all the lanes, instead of the default 1b setting.

The following high speed SerDes protocols are related to this issue. If a protocol supports more than one speed, only the speed(s) listed below is affected.

- SATA 6 Gbaud
- XFI 10.3125 Gbaud

Since the channel characteristics is board and layout dependent, NXP cannot quantify the actual channel loss introduced during board design, layout and fabrication of all end product systems for our customers. Customers should always perform board level simulation and also use other appropriate tool (for example, NXP's SerDes Validation Tool) and/or instrument to determine whether the SerDes channels (lanes) are in high loss condition and then adopt the best setting suitable for their end product and application. Instead of quantifying a SerDes channel as high or non-high loss, a more practical way is to try both the 1b and 0b settings and find out which setting yields better signal integrity for the customer's particular end product system or board.

Once determined that the channels are in non-high loss condition, the Rx Equalization Boost bit for all the lanes in use should be set to 0b during the Pre-boot Initialization (PBI) stage.

Since the Rx Equalization Boost bit is defined in different SerDes registers depending on the SerDes protocols in use, it is important to select the appropriate SerDes register with the correct offset and value as described below when implementing the register write in PBI. The SerDes registers involved are defined on a per lane basis. Therefore, PBI register write must be implemented for all the lanes utilized for the affected SerDes protocols and speeds.

- For SATA 6 Gbaud:
  - Perform a PBI write to each lane's LNaSSCR1 register with a value of 0x0050_2880, which sets this lane's Rx Equalization Boost bit, LNaSSCR1 [RXEQ_BST_1] to 0b.
- For XFI 10.3125 Gbaud:
  - Perform a PBI write to each lane's LNaRECR0 register with a value of 0x0000_045F, which sets this lane's Rx Equalization Boost bit, LNaRECR0 [RXEQ_BST] to 0b.

5.13 USB PHY pin termination recommendations

Table 24. USB 1/2/3 PHY pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
USB[1/2/3]_D_P	IO	USB PHY Data Plus	Do not connect. These pins should be left floating.	
USB[1/2/3]_D_M	IO	USB PHY Data Minus	Do not connect.These pins should be left floating.	
USB[1/2/3]_VBUS	I	USB1 power supply pin. A charge pump external to the USB 3.0 PHY must provide power to this pin. The nominal voltage for this pin is 5 V.	Do not connect.These pins should be left floating.	
USB[1/2/3]_ID	I	USB PHY ID Detect	Pull low through a 1kΩ resistor to GND.	
USB[1/2/3]_TX_P	O	USB PHY 3.0 Transmit Data (positive)	Do not connect.These pins should be left floating.	
USB[1/2/3]_TX_M	O	USB PHY 3.0 Transmit Data (negative)	Do not connect.These pins should be left floating.	
USB[1/2/3]_RX_P	I	USB PHY 3.0 Receive Data (positive)	Connect to ground (GND)	
USB[1/2/3]_RX_M	I	USB PHY 3.0 Receive Data (negative)	Connect to ground (GND)	
USB[1/2/3]_RESREF	IO	Attach a 200-Ω 1% 100-ppm/C precision resistor-to-ground on the board.	Do not connect.These pins should be left floating.	
USB_DRVVBUS	O	VBUS power enable. For example, if an external hub is used, it can handle this signal. The functionality of the USB_DRVVBUS signal is determined by the RCW[USB_DRVVBUS] field in the reset configuration word. The register SCFG_USBDRVVBUS_SELCR selects which of the three controllers drives USB_DRVVBUS.	Do not connect.These pins should be left floating.	
USB_PWRFAULT	I	Indicates that a VBUS fault has occurred. For example, if an external hub is used, it can handle this signal. The functionality of the USB_PWRFAULT signal is determined by the RCW[PWRFAULT] field in the reset configuration word. The register SCFG_USBPWRFAULT_SELCR selects which of the three controllers drives USB_PWRFAULT.	Pull low through a 1kΩ resistor to GND.	
USB2_DRVVBUS	O	VBUS power enable. For example, if an external hub is used, it can handle this signal. The functionality of the USB2_DRVVBUS signal is determined by Extended RCW	Do not connect.These pins should be left floating.	

Table continues on the next page...

Table 24. USB 1/2/3 PHY pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
		PinMux Control Register**(SCFG_RCWPMUXCR0)** in bitfield IIC3_SCL. The register SCFG_USBDRVVBUS_SELCR selects which of the three controllers drives USB_DRVVBUS.		
USB2_PWRFAULT	I	Indicates that a VBUS fault has occurred. For example, if an external hub is used, it can handle this signal. The functionality of the USB_PWRFAULT signal is determined by by Extended RCW PinMux Control Register**(SCFG_RCWPMUXCR0)** in bitfield IIC3_SDA. The register SCFG_USBPWRFAULT_SELCR selects which of the three controllers drives USB_PWRFAULT.	Pull low through a 1kΩ resistor to GND.	
USB3_DRVVBUS	O	VBUS power enable. For example, if an external hub is used, it can handle this signal. The functionality of the USB_DRVVBUS signal is determined by by Extended RCW PinMux Control Register**(SCFG_RCWPMUXCR0)** in bitfield IIC4_SCL. The register SCFG_USBDRVVBUS_SELCR selects which of the three controllers drives USB_DRVVBUS.	Do not connect.These pins should be left floating.	
USB3_PWRFAULT	I	Indicates that a VBUS fault has occurred. For example, if an external hub is used, it can handle this signal. The functionality of the USB_PWRFAULT signal is determined by by Extended RCW PinMux Control Register**(SCFG_RCWPMUXCR0)** in bitfield IIC4_SDA. The register SCFG_USBPWRFAULT_SELCR selects which of the three controllers drives USB_PWRFAULT.	Pull low through a 1kΩ resistor to GND.	

NOTE

USB3.0 PLLs can receive clock either from SYSCLK or DIFF_SYSCLK/ DIFF_SYSCLK_B. Ensure that clock selected has 100 MHz frequency.

5.13.1 USB1 PHY connections

This section describes the hardware connections required for the USB PHY.

This figure shows the VBUS interface for the chip.

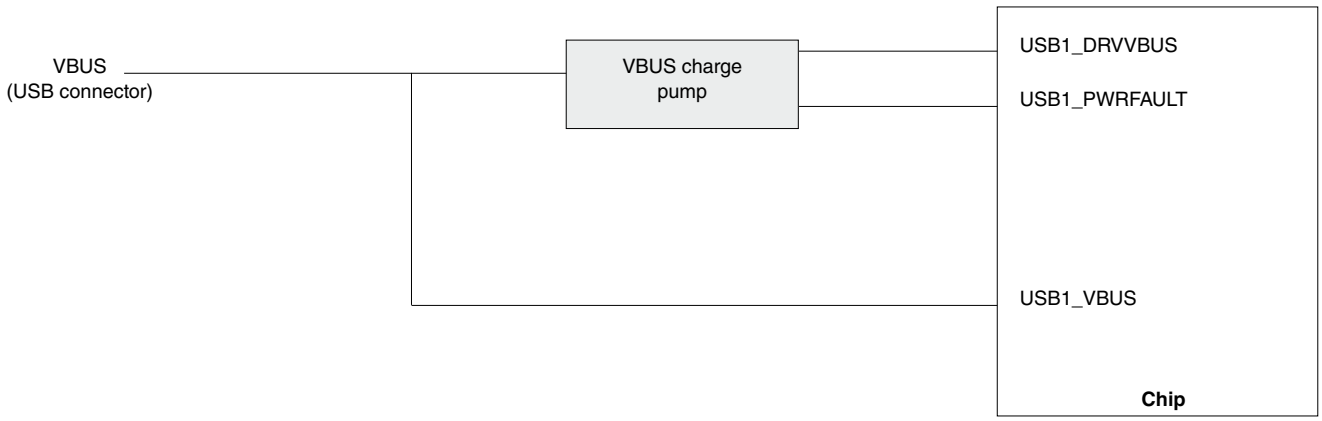


Figure 10. USB1 PHY VBUS interface

5.14 Ethernet Management Interface 1/2 pin termination recommendations

Table 25. Ethernet Management Interface (EMI1/2) pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
EMI1_MDC	O	The functionality of these signals is determined by the EM1 field in the reset configuration word (RCW[EM1]). (To configure as open drain signal, write EMI1_CMODE in reset configuration word)	Must be pulled down through 2-10K resistance to GND OR can be configured as a GPIO and output.	
EMI1_MDIO	IO	The functionality of these signals is determined by the EM1 field in the reset configuration word (RCW[EM1]). (To configure as open drain signal, write EMI1_DMODE in reset configuration word). This pin should be pulled high through a 2-10kΩ resistor to LVDD.	This pin should be tied low through a 2-10kΩ resistor to ground (GND), or this may be configured as a a GPIO and output.	
EMI2_MDC	O	The functionality of these signals is determined by the EM2 field in the reset configuration word (RCW[EM2]).	Must be pulled down through 2-10K resistance to GND OR can be configured as a GPIO and output.	

Table continues on the next page...

Table 25. Ethernet Management Interface (EMI1/2) pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
		(To configure as open drain signal, write EMI1_CMODE in reset configuration word)		
EMI2_MDIO	IO	The functionality of these signals is determined by the EM2 field in the reset configuration word (RCW[EM2]). (To configure as open drain signal, write EMI2_DMODE in reset configuration word). This pin should be pulled high through a 2-10kΩ resistor to TVDD.	This pin should be tied low through a 2-10kΩ resistor to ground (GND), or this may be configured as a a GPIO and output.	

NOTE

To meet MDIO to MDC hold time requirement (tMDDXKH) as mentioned in LS1043A datasheet, an external delay on MDIO line may be required on board.

Depending upon the MDC->MDIO output delay spec of PHY, an appropriate delay must be adjusted to meet the hold requirement of LS1043A.

5.14.1 Ethernet controller pin termination recommendations

The LS1043A/LS1023A supports two Ethernet Controllers (EC) which can connect to Ethernet PHYs using RGMII protocols. Both, EC1 and EC2 operated using LVDD supply which supports 1.8V /2.5V operation.

Table 26. Ethernet controller pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
EC1 in RGMII mode				
EC1_TXD[0:3], EC1_TX_EN	O	The functionality of these signals is determined by the EC1 field in the reset configuration word (RCW[EC1]). FMAN-MAC3 is connected to EC1 interface when RGMII is selected through RCW[EC1] field	These pins can be configured as GPIO's and outputs.	
EC1_GTX_CLK	O			
EC1_RXD[0:3]	I		These pins can be configured as GPIO's and outputs.	
EC1_RX_DV	I			
EC1_RX_CLK	I			
EC1_GTX_CLK125	I			
EC2 in RGMII mode				
EC2_TXD[0:3], EC2_TX_EN	O	The functionality of these signals is determined by the EC2 field in the reset configuration word (RCW[EC2]). FMAN-MAC4 is connected to EC2 interface when RGMII is selected through RCW[EC2] field	These pins can be configured as GPIO's and outputs.	
EC2_GTX_CLK	I			
EC2_RXD[0:3]	I		These pins can be configured as GPIO's and outputs.	
EC2_RX_DV	I			
EC2_RX_CLK	I			

Table continues on the next page...

Table 26. Ethernet controller pin termination checklist (continued)

Signal Name	I/O type	Used	Not used	Completed
EC2_GTX_CLK125	I			

5.15 QUICC Engine recommendations

QUICC Engine Block in LS1043/LS1023 supports two TDM/HDLC interfaces.

The functionality of these signals is determined by the QE-TDMA and QE-TDMB fields in the reset configuration word.

QUICC Engine supports 3.3V and 1.8V operation only

5.15.1 QUICC Engine pin termination recommendations

Table 27. QUICC Engine pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
QE Clock Signals				
BRGO[1 & 4]	O	The functionality of BRGO1 and BRGO4 signals is determined by the IIC3_SDA and IIC3_SCL respectively in **SCFG_RCWPMUXCR0** register. Similarly CLK12 and CLK11 signals is determined by the IIC3_SDA and IIC3_SCL respectively in **SCFG_RCWPMUXCR0** register.	Program as GPIOs and as output.	
CLK[11:12]	I			
BRGO[2:3]	O	The functionality of this signal is determined by the RCW[IIC2_EXT] fields in reset configuration word. RCW[QE_CLK_OVRRIDE] field in reset configuration word provides options to select other combinations of BRGs and CLKs. Please refer to reference manual for more details.	Program as GPIOs and as output.	
CLK[9:10]	I			
UCC1 signals				
UC1_CDB_RXER	I	The functionality of these signals is determined by the RCW[IRQ_EXT] field in the reset configuration word except for UC1_CDB_RXER which is determined by the IIC4_SCL bitfield in register **SCFG_RCWPMUXCR0**	If UCC1 is not used, all the pins can be programmed as GPIO's and outputs.	
UC1_CTSB_RXDV	I			
UC1_RXD7	I			
UC1_TXD7	O			
UC1_RTSB_TXEN	O			
UCC3 signals				

Table continues on the next page...

Table 27. QUICC Engine pin termination checklist (continued)

Signal Name	I/O type	Used	Not used	Completed
UC3_CDB_RXER	I	The functionality of these signals is determined by the RCW[IRQ_EXT] field in the reset configuration word except for UC3_CDB_RXER which is determined by the IIC4_SDA bitfield in register **SCFG_RCWPMUXCR0**	If UCC3 is not used, all the pins can be programmed as GPIO's and outputs.	
UC3_CTSB_RXDV	I			
UC3_RXD7	I			
UC3_TXD7	O			
UC3_RTSB_TXEN	O			
TDMA signals				
TDMA_TXD	O	The functionality of these signals is determined by the RCW[IRQ_EXT] field in the reset configuration word except for TDMA_RQ which is determined by the IIC4_SCL bitfield in register **SCFG_RCWPMUXCR0**	If TDMA is not used, all the pins can be programmed as GPIO's and outputs.	
TDMA_TSYNC	I			
TDMA_RQ	O			
TDMA_RSYNC	I			
TDMA_RXD	I			
TDMB signals				
TDMB_TXD	O	The functionality of these signals is determined by the RCW[IRQ_EXT] field in the reset configuration word except for TDMB_RQ which is determined by the IIC4_SDA bitfield in register **SCFG_RCWPMUXCR0**	If TDMB is not used, all the pins can be programmed as GPIO's and outputs.	
TDMB_TSYNC	I			
TDMB_RQ	O			
TDMB_RSYNC	I			
TDMB_RXD	I			
Strobe signals				
QE_SI1_STROBE[0:1]	O	The functionality of these signals is determined by the RCW[IIC2_EXT] field in the reset configuration word.	If Strobes are not used, all the pins can be programmed as GPIO's and outputs.	

5.16 QSPI pin termination recommendations

Table 28. QSPI pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
QSPI_A_SCK	O	The functionality of these signals is determined by the RCW[IFC_GRP_F_EXT] bits of reset configuration word.	Pin can be left unconnected.	
QSPI_B_SCK	O	The functionality of these signals is determined by the RCW[IFC_GRP_F_EXT] bits of reset configuration word.	Pin can be left unconnected	
QSPI_A_CS[0:1]	O	The functionality of these signals is determined by the RCW[IFC_GRP_F_EXT] bits of reset configuration word.	Pin can be left unconnected	

Table continues on the next page...

Table 28. QSPI pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
QSPI_B_CS[0:1]	O	The functionality of these signals is determined by the RCW[IFC_GRP_F_EXT] bits of reset configuration word.	Pin can be left unconnected	
QSPI_A_DATA[0:2]	IO	The functionality of these signals is determined by the RCW[IFC_GRP_F_EXT] bits of reset configuration word.	If this pin is not used, it should be programmed as GPIO and output.	
QSPI_A_DATA[3]	IO	The functionality of these signals is determined by the RCW[IFC_GRP_A_EXT] bits of reset configuration word.	If this pin is not used, it should be programmed as GPIO and output.	
QSPI_B_DATA[0:2]	IO	The functionality of these signals is determined by the RCW[IFC_GRP_D_EXT] bits of reset configuration word.	If this pin is not used, it should be programmed as GPIO and output.	
QSPI_B_DATA[3]	IO	The functionality of these signals is determined by the RCW[IFC_GRP_E1_EXT] bits of reset configuration word.	If this pin is not used, it should be programmed as GPIO and output.	

5.17 SPI recommendations

The LS1043A/LS1023A serial peripheral interface (SPI) pins are powered from OVDD supply, which supports 1.8V only.

5.17.1 SPI pin termination recommendations

Table 29. SPI pin termination checklist

Signal name	I/O type	Used	Not used	Completed
SPI_MISO	I	The functionality of this signal is determined by the SPI_BASE and SPI_EXT field in the reset configuration (RCW[SPI_EXT]).	This pin should be pulled high through a 2-10 kΩ resistor to OV_{DD}.	
SPI_MOSI	I/O	The functionality of this signal is determined by the SPI_BASE and SPI_EXT field in the reset configuration (RCW[SPI_EXT]).	This pin should be pulled high through a 2-10 kΩ resistor to OV_{DD}.	
SPI_CLK	O	The functionality of this signal is determined by the SPI_BASE and SPI_EXT field in the reset configuration (RCW[SPI_EXT]).	This pin may be left unconnected.	
SPI_CS[0:3]_B	O	The functionality of this signal is determined by the SPI_BASE field in the reset configuration (RCW[SPI_BASE]).	These pins may be left unconnected.	

5.18 General Purpose Input/Output pin termination recommendations

Table 30. General Purpose Input/Output pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
GPIO1_13	IO	The functionality of this signal is determined by the RCW[ASLEEP] field in the reset configuration word.	For all GPIOx pins: When programmed as outputs, no termination is required.	
GPIO1_14	IO	The functionality of this signal is determined by the RCW[RTC] field in the reset configuration word.		
GPIO1_[15:22]	IO	The functionality of these signals is determined by the RCW[UART_BASE] & RCW[UART_EXT] field in the reset configuration word.		
GPIO1_[23:31]	IO	The functionality of these signals is determined by the RCW[IRQ_EXT] and RCW[IRQ_BASE] fields in the reset configuration word.		
GPIO2_[0:3]	IO	The functionality of these signals is determined by the RCW[SPI_BASE] fields in the reset configuration word.	For all GPIOx pins: When programmed as outputs, no termination is required.	
GPIO2_[4:9]	IO	The functionality of these signals is determined by the RCW[SDHC_BASE] fields in the reset configuration word.	For all GPIOx pins: When programmed as outputs, no termination is required.	
GPIO2_[10:12]	IO	The functionality of these signals is determined by the RCW[IFC_GRP_E1_BASE] field in the reset configuration word.	For all GPIOx pins: When programmed as outputs, no termination is required.	
GPIO2_[13:15]	IO	The functionality of these signals is determined by the RCW[IFC_GRP_D_BASE] fields in the reset configuration word.		
GPIO2_[25:27]	IO	The functionality of these signals is determined by the RCW[IFC_GRP_A_BASE] field in the reset configuration word.		
GPIO3_[0:1]	IO	The functionality of these signals is determined by the RCW[EM1] field in the reset configuration word.	For all GPIOx pins: When programmed as outputs, no termination is required.	

Table continues on the next page...

Table 30. General Purpose Input/Output pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
GPIO3_[2:14]	IO	The functionality of these signals is determined by the RCW[EC1] field in the reset configuration word.		
GPIO3_[15:27]	IO	The functionality of these signals is determined by the RCW[EC2] field in the reset configuration word.		
GPIO4_[0:1]	IO	The functionality of these signals is determined by the RCW[EM2] field in the reset configuration word.	For all GPIOx pins: When programmed as outputs, no termination is required.	
GPIO4_[2:3]	IO	The functionality of these signals is determined by the RCW[IIC2_EXT] field in the reset configuration word.		
GPIO4_[10:11]	IO	The functionality of these signals is determined by the IIC3_SCL and IIC3_SDA fields in **SCFG_RCWPMUXCR0** respectively.		
GPIO4_[12:13]	IO	The functionality of these signals is determined by the IIC4_SCL and IIC4_SDA fields in **SCFG_RCWPMUXCR0** respectively.		
GPIO4_[29]	IO	The functionality of these signals is determined by the RCW[USB_DRVVBUS] field in the reset configuration word.		
GPIO4_[30]	IO	The functionality of these signals is determined by the RCW[USB_PWRFAULT] fields in the reset configuration word.	For all GPIOx pins: When programmed as outputs, no termination is required.	

5.19 FTM1 pin termination recommendations

Table 31. FTM1 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM1_CH[0:7]	IO	The functionality of this signal is determined by the EC1 field in the reset configuration (RCW[EC1]).	Program as GPIOs and as outputs.	
FTM1_EXTCLK	I	The functionality of this signal is determined by the EC1 field in the reset configuration (RCW[EC1]).	Program as GPIOs and as outputs.	

Table continues on the next page...

Table 31. FTM1 pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
FTM1_FAULT	I	The functionality of this signal is determined by the EC1 field in the reset configuration (RCW[EC1]).	Program as GPIOs and as outputs.	
FTM1_QD_PHA	I	The functionality of this signal is determined by the EC1 field in the reset configuration (RCW[EC1]).	Program as GPIOs and as outputs.	
FTM1_QD_PHB	I	The functionality of this signal is determined by the EC1 field in the reset configuration (RCW[EC1]).	Program as GPIOs and as outputs.	

5.20 FTM2 pin termination recommendations

Table 32. FTM2 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM2_CH[0:7]	IO	The functionality of this signal is determined by the EC2 field in the reset configuration (RCW[EC2]).	Program as a GPIO and as an output.	
FTM2_EXTCLK	I	The functionality of this signal is determined by the EC2 field in the reset configuration (RCW[EC2]).	Program as a GPIO and as an output.	
FTM2_FAULT	I	The functionality of this signal is determined by the EC2 field in the reset configuration (RCW[EC2]).	Program as a GPIO and as an output.	
FTM2_QD_PHA	I	The functionality of this signal is determined by the EC2 field in the reset configuration (RCW[EC2]).	Program as a GPIO and as an output.	
FTM2_QD_PHB	I	The functionality of this signal is determined by the EC2 field in the reset configuration (RCW[EC2]).	Program as a GPIO and as an output.	

5.21 FTM3 pin termination recommendations

Table 33. FTM3 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM3_CH[0:7]	IO	The functionality of these signals is determined by the IRQ_BASE and IRQ_EXT fields in the reset configuration word (RCW[IRQ_BASE] and RCW[IRQ_EXT]).	Program as a GPIO and as an output.	

Table continues on the next page...

Table 33. FTM3 pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
FTM3_EXTCLK	I	The functionality of these signals is determined by the IIC4_SDA bitfield in register **SCFG_RCWPMUXCR0**	Program as a GPIO and as an output.	
FTM3_FAULT	I	The functionality of these signals is determined by the IIC4_SCL bitfield in register **SCFG_RCWPMUXCR0**	Program as a GPIO and as an output.	
FTM3_QD_PHA	I	The functionality of these signals is determined by the IIC2_EXT fields in the reset configuration word (RCW[IIC2_EXT]).	Program as a GPIO and as an output.	
FTM3_QD_PHB	I	The functionality of these signals is determined by the IIC2_EXT fields in the reset configuration word (RCW[IIC2_EXT]).	Program as a GPIO and as an output.	

5.22 FTM4 pin termination recommendations

Table 34. FTM4 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM4_CH[0:7]	IO	he functionality of FTM4_CH[0-5] signals is determined by the UART_EXT fields in the reset configuration word (RCW[UART_EXT]). The functionality of FTM4_CH6 and FTM4_CH7 signals is determined by the SDHC_EXT fields in the reset configuration word (RCW[SDHC_EXT]).	Program as a GPIO and as an output.	
FTM4_EXTCLK	I	The functionality of these signals is determined by the SDHC_EXT fields in the reset configuration word (RCW[SDHC_EXT]).	Program as a GPIO and as an output.	
FTM4_FAULT	I	The functionality of these signals is determined by the SDHC_EXT fields in the reset configuration word (RCW[SDHC_EXT]).	Program as a GPIO and as an output.	
FTM4_QD_PHA	I	The functionality of these signals is determined by the SDHC_EXT fields in the reset configuration word (RCW[SDHC_EXT]).	Program as a GPIO and as an output.	
FTM4_QD_PHB	I	The functionality of these signals is determined by the SDHC_EXT fields in the reset configuration word (RCW[SDHC_EXT]).	Program as a GPIO and as an output.	

5.23 FTM5 pin termination recommendations

Table 35. FTM5 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM5_CH[0:1]	IO	The functionality of these signals is determined by the IFC_GRP_A_EXT fields in the reset configuration word (RCW[IFC_GRP_A_EXT]).	Program as a GPIO and as an output.	
FTM5_EXTCLK	I	The functionality of these signals is determined by the IFC_GRP_A_EXT fields in the reset configuration word (RCW[IFC_GRP_A_EXT]).	Program as a GPIO and as an output.	

5.24 FTM6 pin termination recommendations

Table 36. FTM6 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM6_CH[0:1]	IO	The functionality of these signals is determined by the IFC_GRP_D_EXT fields in the reset configuration word (RCW[IFC_GRP_D_EXT]).	Program as a GPIO and as an output.	
FTM6_EXTCLK	I	The functionality of these signals is determined by the IFC_GRP_D_EXT fields in the reset configuration word (RCW[IFC_GRP_D_EXT]).	Program as a GPIO and as an output.	

5.25 FTM7 pin termination recommendations

Table 37. FTM7 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM7_CH[0:1]	IO	The functionality of these signals is determined by the IFC_GRP_E1_EXT fields in the reset configuration word (RCW[IFC_GRP_E1_EXT]).	Program as a GPIO and as an output.	

Table continues on the next page...

Table 37. FTM7 pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
FTM7_EXTCLK	I	The functionality of these signals is determined by the IFC_GRP_E1_EXT fields in the reset configuration word (RCW[IFC_GRP_E1_EXT]).	Program as a GPIO and as an output.	

5.26 FTM8 pin termination recommendations

Table 38. FTM8 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM8_CH[0:1]	IO	The functionality of these signals is determined by the IIC3_SCL and IIC3_SDA bitfields respectively in register **SCFG_RCWPMUXCR0**	Program as a GPIO and as an output.	

5.27 IEEE1588 recommendations

5.27.1 IEEE 1588 pin termination recommendations

Table 39. IEEE 1588 pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
TSEC_1588_CLK_IN	I	Connect to external high-precisiontimer reference input. The functionality of these signals is determined by the EC2 field in the reset configuration word (RCW[EC2]).	Program as GPIO's and output.	
TSEC_1588_ALARM_OUT1	O	The functionality of these signals is determined by the EC2 field in the reset configuration word (RCW[EC2]).	Program as GPIO's and output.	
TSEC_1588_ALARM_OUT2	O	The functionality of these signals is determined by the EC2 field in the reset configuration word (RCW[EC2]).	Program as GPIO's and output.	
TSEC_1588_CLK_OUT	O	The functionality of these signals is determined by the EC2 field in the	Program as GPIO's and output.	

Table continues on the next page...

Table 39. IEEE 1588 pin termination checklist (continued)

Signal Name	I/O type	Used	Not used	Completed
		reset configuration word (RCW[EC2]).		
TSEC_1588_PULSE_OUT1	O	The functionality of these signals is determined by the EC2 field in the reset configuration word (RCW[EC2]).	Program as GPIO's and output.	
TSEC_1588_PULSE_OUT2	O	The functionality of these signals is determined by the EC2 field in the reset configuration word (RCW[EC2]).	Program as GPIO's and output.	
TSEC_1588_TRIG_IN1	I	The functionality of these signals is determined by the EC2 field in the reset configuration word (RCW[EC2]).	Program as GPIO's and output.	
TSEC_1588_TRIG_IN2	I	The functionality of these signals is determined by the EC2 field in the reset configuration word (RCW[EC2]).	Program as GPIO's and output.	

NOTE

1. When configured for IEEE1588, the EC2 pins those are not available for IEEE1588, are configured for GPIO. All IEEE 1588 pins are referenced to LV_{DD}.

5.28 System control pin termination recommendations

Table 40. System Control pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
PORESET_B	I	This pin is required to be asserted as per the applicable chip data sheet, in relation to minimum assertion time and during power-up/power-down. It is an input-only pin and must be asserted to sample power on configuration pins.		
HRESET_B	I/O	This pin is an open drain signal and should be pulled high through a 2-10 kΩ resistor to OV_{DD}.		
RESET_REQ_B	O	Must not be pulled down during power-on reset.	This pin should be pulled high through a 2-10 kΩ resistor to OV_{DD} and must not be pulled down during power-on reset.	

NOTE

1. If on-board programming of NOR and NAND boot flash, QSPI boot flash, or SD card is needed, then maintain an option (may be via a jumper) that keeps PORESET_B and RESET_REQ_B disconnected from each other. Booting from a blank NAND flash or SPI flash causes boot error, which in turn causes assertion of RESET_REQ_B. When RESET_REQ_B is connected with PORESET_B, the device goes in a recurring reset loop and does not provide enough time for JTAG to take control of the device and perform any operation.

2. For RCW override, RESET_REQ_B should be disconnected from PORESET_B or HRESET_B. An option on board is required.

5.29 JTAG pin termination recommendations

Table 41. JTAG pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
TCK	I	Connect to pin 4 of the ARM Cortex 10-pin header. This pin requires a 2-10kΩ resistor to OV_{DD}.		
TDI	I	Connect to pin 8 of the ARM Cortex 10-pin header. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.	May be left unconnected.	
TDO	O	Connect to pin 6 of the ARM Cortex 10-pin header. This output is actively driven during reset rather than being tri-stated during reset.	May be left unconnected.	
TMS	I	Connect to pin 2 of the ARM Cortex 10-pin header. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.	May be left unconnected.	
TRST_B	I	This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled. Connect as shown in Figure 11.	Tie TRST_B to PORESET_B through a 0 kΩ resistor.	

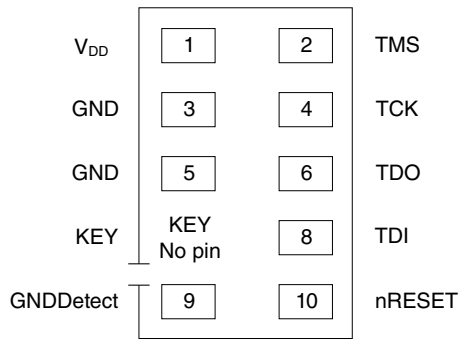
5.29.1 JTAG system-level recommendations

Table 42. JTAG system-level checklist

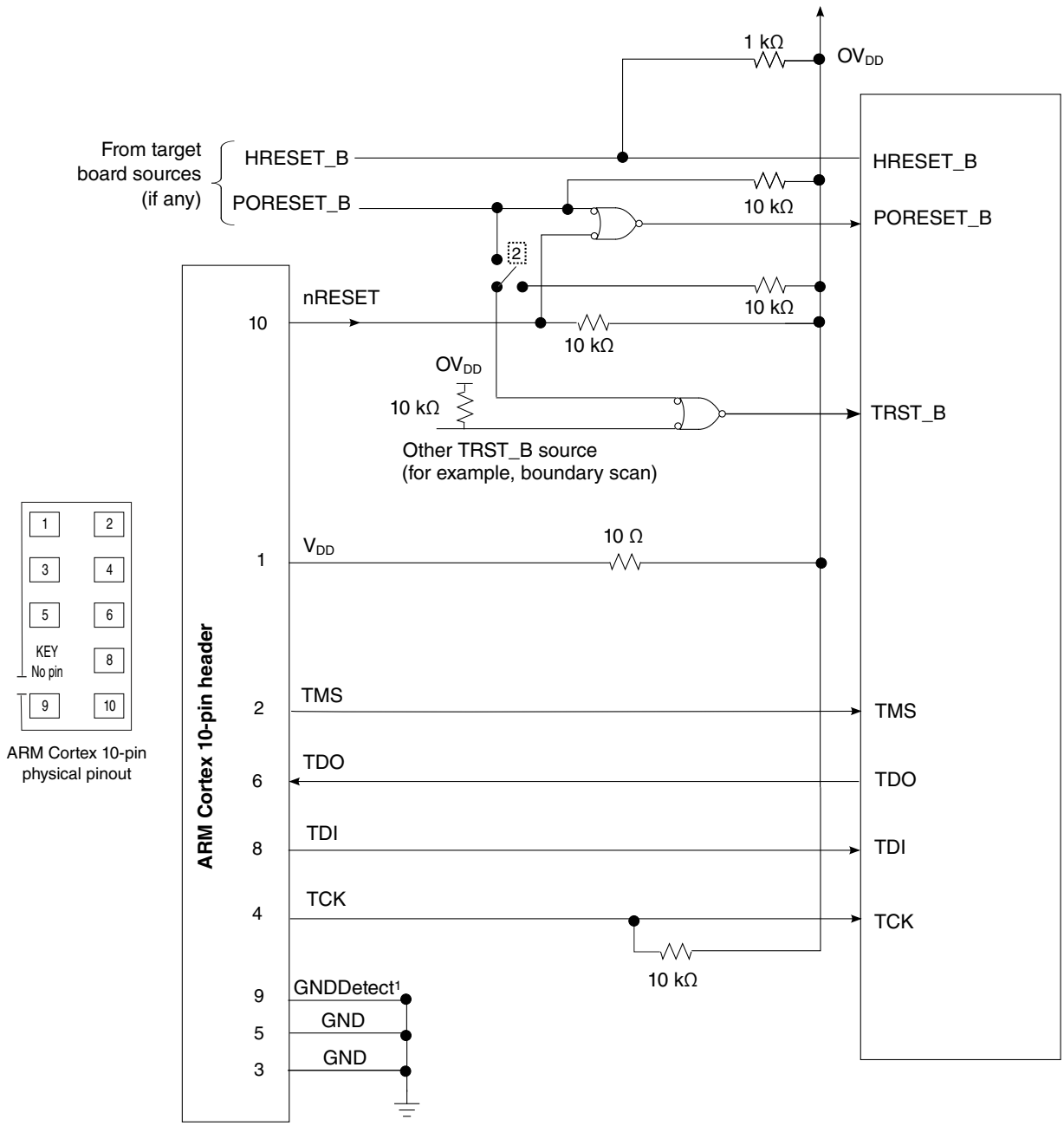
Item	Completed
ARM®Cortex® 10-pin header signal interface to JTAG port	
Configure the group of system control pins as shown in Figure 11. **NOTE:** These pins must be maintained at a valid deasserted state under normal operating conditions, because most have asynchronous behavior and spurious assertion gives unpredictable results.	
The JTAG port of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The ARM Cortex 10-pin header connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The ARM Cortex 10-pin header interface requires the ability to independently assert PORESET_B in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the nRESET signals must be merged into these signals with logic.	
Boundary-scan testing	
Ensure that TRST_B is asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation.	

Table continues on the next page...

Table 42. JTAG system-level checklist (continued)

Item	Completed
Follow the arrangement shown in Figure 11 to allow the ARM Cortex 10-pin header to assert PORESET_B independently while ensuring that the target can drive PORESET_B as well.	
The ARM® Cortex® 10-pin interface has a standard header, shown in the following figure. The connector typically has pin 7 removed as a connector key. The signal placement recommended in this figure is common to all known emulators.  **NOTE:** The ARM Cortex 10-pin header adds many benefits such as breakpoints, watch points, register and memory examination/modification, and other standard debugger features. An inexpensive option is to leave the ARM Cortex 10-pin header unpopulated until needed.	

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 11. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions, as most have asynchronous behavior and spurious assertion gives unpredictable results.



Note:
1. GNDDetect is an optional board feature. Check with 3rd-party tool vendor.
2. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, ensure this switch is closed.

Figure 11. JTAG interface connection

5.30 Clock pin termination recommendations

Table 43. Clock pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
EC1_GTX_CLK	O	The functionality of this signal is determined by the EC1 field in the reset configuration word (RCW[EC1]). LS1043A has a duty cycle reshaper inside RGMII block. This allows GTX clock from RGMII PHY to be used.	Program as a GPIO and as an output.	
EC1_GTX_CLK125	I			
EC2_GTX_CLK	O	The functionality of this signal is determined by the EC2 field in the reset configuration word (RCW[EC2]). LS1043A has a duty cycle reshaper inside RGMII block. This allows GTX clock from RGMII PHY to be used.	Program as a GPIO and as an output.	
EC2_GTX_CLK125	I			
SYSCLK	I	This is the single-ended primary clock input to the chip. It supports a 64.0 MHz to 100.0 MHz clock range. Note that 64MHz SYSCLK reference frequency is specifically for Profibus support on QUICC Engine.	This pin should be pulled low through a 2-10kΩ resistor to GND.[1]	
DIFF_SYSCLK	I	These pins are the differential primary clock input to the chip. These pins support 100MHz only. When used, these pins should be connected to a 100MHz differential clock generator.	These pins should be pulled low through a 2-10kΩ resistor to GND, or they can be left floating.[3]	
DIFF_SYSCLK_B	I			
RTC	I	The functionality of this signal is determined by the RTC field in the reset configuration word (RCW[RTC]).	Pull low through a 2-10kΩ resistor to GND, or program pin as a GPIO and output.	
DDRCLK	I	The reference clock for the DDR controller supports a 64 MHz to 100 MHz input clock range.	This pin should be pulled low through a 2-10kΩ resistor to GND.[2, 4]	

NOTE

1. In the "Single Oscillator Source" reference clock mode supported by LS1043A, DIFF_SYSCLK/DIFF_SYSCLK_B (differential) clock inputs are used as primary clock inputs and SYSCLK is unused. Power-on-configuration signal cfg_eng_use0 selects between SYSCLK (single ended) and DIFF_SYSCLK/DIFF_SYSCLK_B (differential) clock inputs.
2. In the "Single Oscillator Source" reference clock mode, DIFF_SYSCLK/ DIFF_SYSCLK_B clock inputs can be selected to feed the DDR PLL. RCW bits [DDR_REFCLK_SEL] are used for this selection and DDRCLK is unused.

3. When SYSCLK is chosen as the primary clock input to the chip, these pins are unused.
4. The options for RCW bits 186-187 (DDR_REFCLK_SEL, DDR reference clock selection) are as follows:

   00 The DDRCLK pin provides the reference clock to the DDR PLL

   10 DIFF_SYSCLK/DIFF_SYSCLK_B provides the reference clock to the DDR PLL

5.31 Single Source Clocking

The chip supports the single source clocking options with single, two, and more reference clocks.

5.32 "Single Oscillator Source" Reference Clock Mode

In this mode, single onboard oscillator can provide the reference clock (100MHz) to the following PLLs:

- Platform PLL
- Core PLLs
- USB PLL
- DDR PLL
- SerDes PLLs

The reset configuration field identifies whether the SYSCLK (single-ended) or DIFF_SYSCLK (differential) is selected as the clock input to the chip.

The RCW[DDR_REFCLK_SEL] bit is used to select clock input (DIFF_SYSCLK or DDRCLK) to the DDR PLL.

The following figure shows the system view of single oscillator source clocking. In this figure, the on-board oscillator generates three differential clock outputs. The first differential output is used to provide the clock to system clock associated PLLs and DDR PLL. However, the second and third differential outputs are used to provide clocks to SerDes PLLs.

A multiplexer between system clock and USBCLK is used to provide the USB PHY reference clock to the USB PLL. And, multiplexer between DIFF_SYSCLK/DIFF_SYSCLK_B inputs and DDRCLK is used to provide reference clock to the DDR PLL.

The duty cycle reshaper reshapes the 125 MHz EC*n*_GTX_CLK125 which is fed into frame manager for transmission as EC*n*_GTX_CLK.

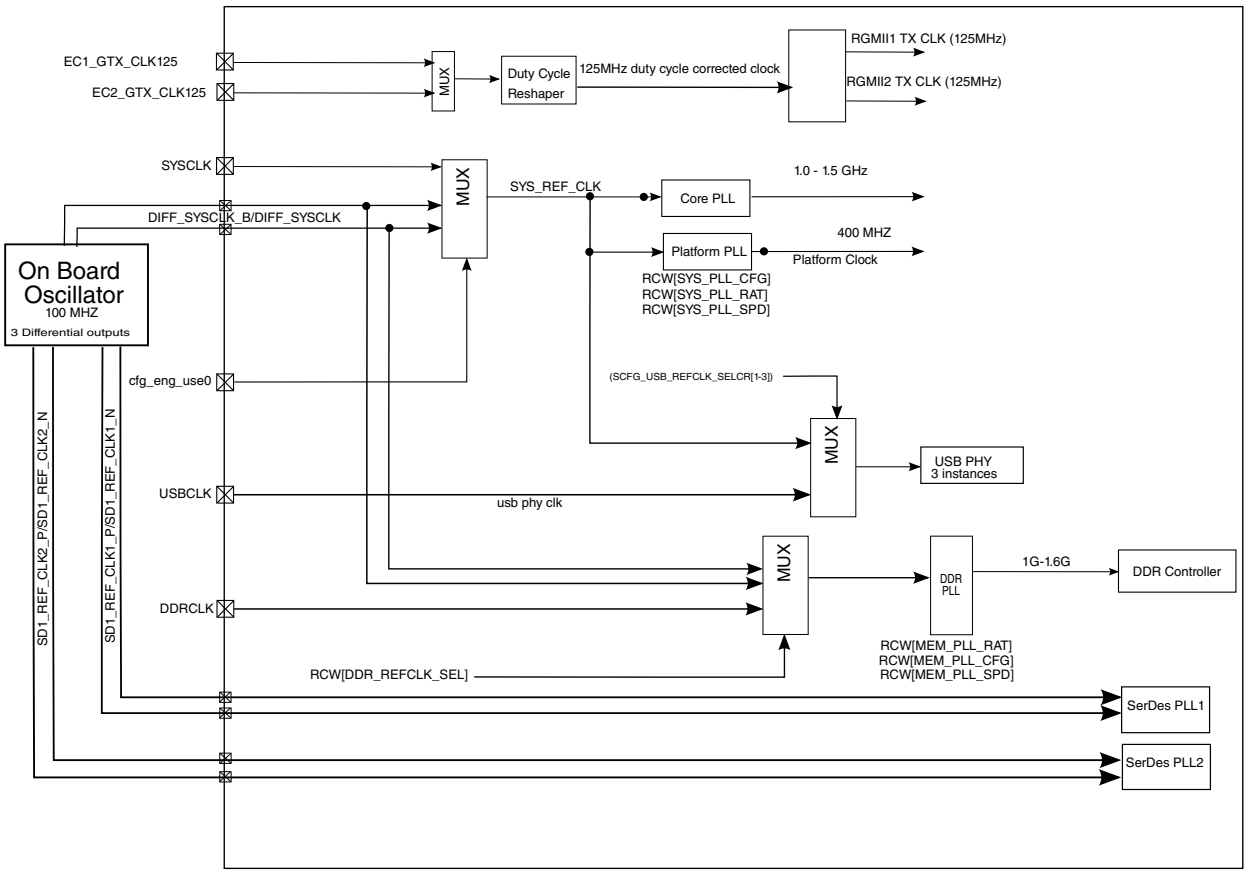


Figure 12. Single Oscillator Source Clocking

5.33 "Single Oscillator Source" clock select

The single oscillator source clock select input, described in this table, selects between SYSCLK (single ended) and DIFF_SYSCLK/DIFF_SYSCLK_B (differential) inputs.

Table 44. Single oscillator source clock select

Functional signals	Reset configuration name	Value (binary)	Options
IFC_WE0_B Default (1)	cfg_eng_use0	0	DIFF_SYSCLK/DIFF_SYSCLK_B (differential)
		1	SYSCLK (single ended)
IFC_OE_B Default (1)	cfg_eng_use1 On-chip LVDS termination must NOT be enabled when external (off-chip) termination are active.	0	On-chip LVDS termination disabled
		1	On-chip LVDS termination enabled
IFC_WP_B[0]	cfg_eng_use2	Reserved	Reserved

5.34 DIFF_SYSCLK/DIFF_SYSCLK_B system-level recommendations

Table 45. DIFF_SYSCLK/DIFF_SYSCLK_B system-level checklist

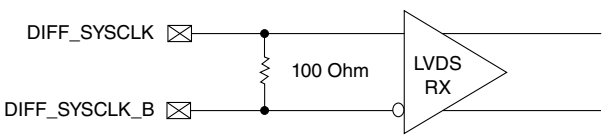
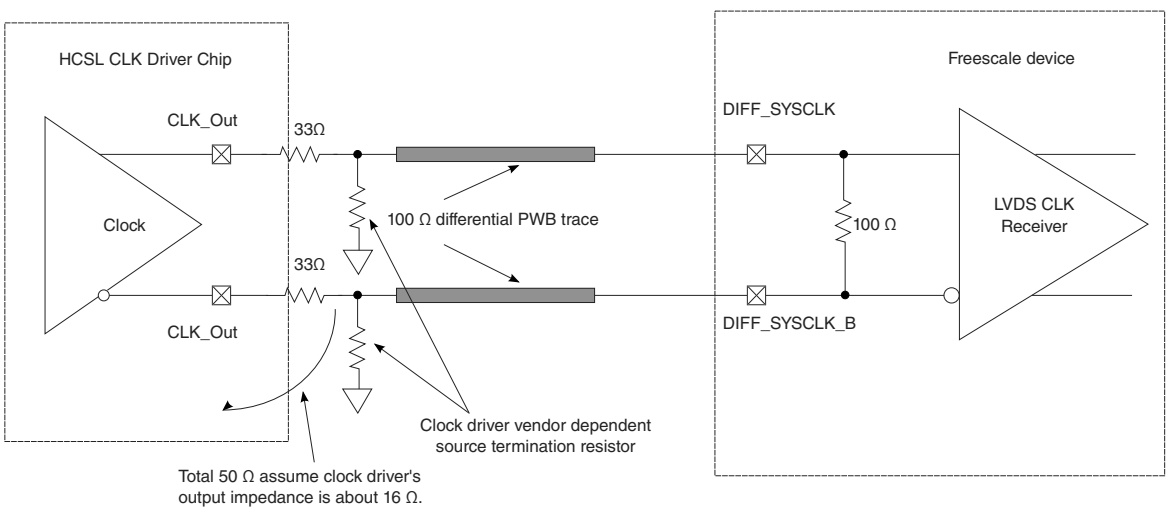
Item	Completed
DIFF_SYSCLK/DIFF_SYSCLK_B can be selected to provide primary clock to the chip. Although it is a Low Voltage Differential Signaling (LVDS) type clock driver but it has AC/DC characteristics identical to the SerDes reference clock inputs which are High-Speed Current Steering Logic (HCSL)-compatible. This eases system design as same clock driver can be used to provide the various differential clock inputs required by the chip  **Figure 13. LVDS receiver**	
Interfacing DIFF_SYSCLK/DIFF_SYSCLK_B with other Differential Signalling levels	
Connection with HCSL Clock driver  **Figure 14. Interfacing with HCSL clock driver (Reference only)**	
Connection with LVDS Clock driver	

Table continues on the next page...

Table 45. DIFF_SYSCLK/DIFF_SYSCLK_B system-level checklist (continued)

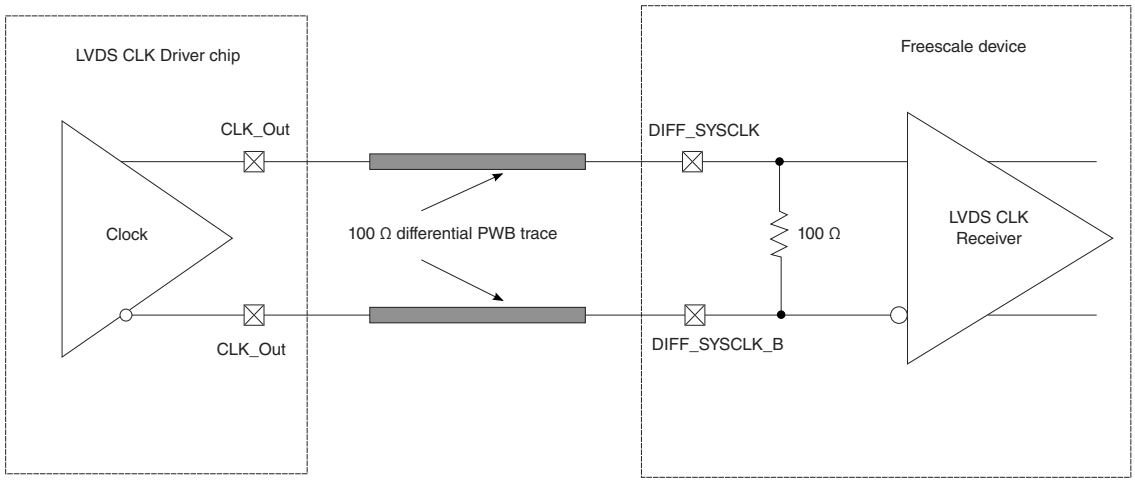
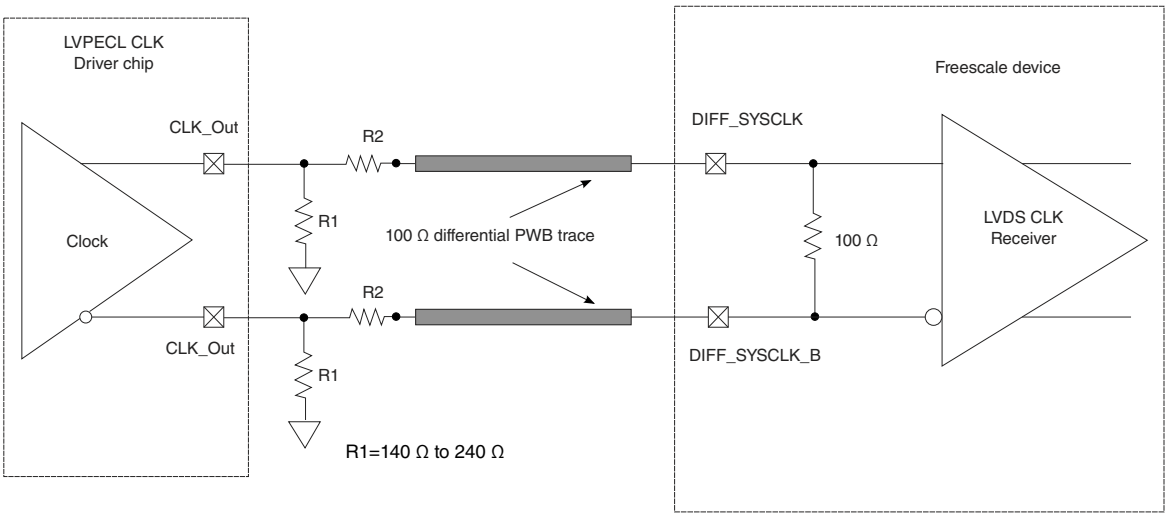
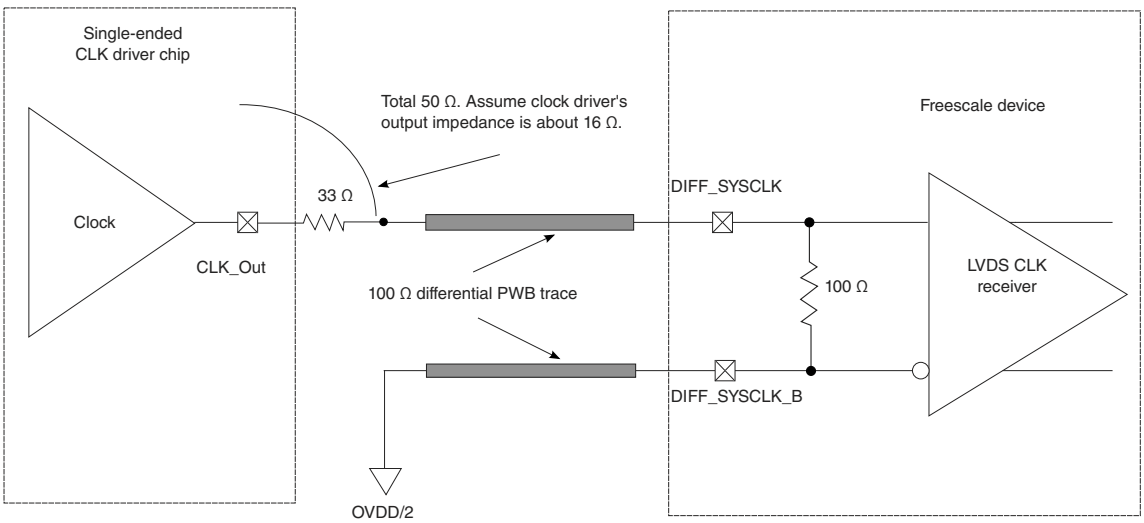
Item	Completed
 **Figure 15. Interfacing with LVDS clock driver (Reference only)**	
Connection with LVPECL Clock driver  **Figure 16. Interfacing with LVPECL clock driver (Reference only)**	
Single-Ended Connection with Clock driver The DIFF_SYSCLK_B should be terminated to OVDD/2	

Table 45. DIFF_SYSCLK/DIFF_SYSCLK_B system-level checklist

Item	Completed
 **Figure 17. Single ended connection (Reference only)**	

5.35 System clocking

This section describes the PLL configuration of the chip.

5.35.1 PLL characteristics

Characteristics of the chip's PLLs include the following:

- Core cluster CGA PLL1 generates a clock for all the cores and/or FMAN, from the externally supplied SYSCLK or LVDS generated (single ended) input.
- Core cluster CGA PLL2 generates a clock for all the cores and/or FMAN & eSDHC, from the externally supplied SYSCLK or LVDS generated (single ended) input.
- The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Platform to SYSCLK PLL ratio.
- The DDR block PLL generates an asynchronous DDR clock from the externally supplied DDRCLK input.
- The 4 lane SerDes blocks has two PLLs which generate a clock from their respective externally supplied SD1_REF_CLK*n*_P/SD1_REF_CLK*n*_N inputs. The frequency ratio is selected using the SerDes PLL RCW configuration bits as described in Valid Reference Clocks and PLL Configurations for SerDes Protocols .

5.35.2 Clock ranges

This table provides the clocking specifications for the processor core, platform, memory, and integrated flash controller.

Table 46. Processor, platform, and memory clocking specifications @ 1.0 V

Characteristic	Maximum processor core frequency								Unit	Notes
	1000 MHz		1200 MHz		1400 MHz		1600 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
Core cluster group PLL frequency	1000	1000	1000	1200	1000	1400	1000	1600	MHz	1
Platform clock frequency	256	300	256	300	256	300	256	400	MHz	1
Memory Bus Clock Frequency (DDR3L)	500	800	500	800	500	800	500	800	MHz	1, 2, 3
Memory Bus Clock Frequency (DDR4)	650	800	650	800	650	800	650	800	MHz	1, 3
IFC clock frequency	-	100	-	100	-	100	-	100	MHz	4
FMan	350	500	350	500	350	500	350	500	MHz	

1. **Caution:**The platform clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.

2. The memory bus clock speed is half the DDR3L/DDR4 data rate. DDR3L memory bus clock frequency is limited to min = 1000 MT/s whereas DDR4 memory bus clock frequency is limited to min = 1300 MT/s.

3. The memory bus clock speed is dictated by its own PLL.

4. The integrated flash controller (IFC) clock speed on IFC_CLK[0:1] is determined by the IFC module input clock (platform clock / 2) divided by the IFC ratio programmed in CCR[CLKDIV]. See the chip reference manual for more information.

5. The minimum platform frequency should meet the requirements in Minimum platform frequency requirements for high-speed interfaces.

5.35.2.1 DDR clock ranges

The DDR memory controller can run only in asynchronous mode, where the memory bus is clocked with the clock provided on the DDRCLK input pin, which has its own dedicated PLL.

This table provides the clocking specifications for the memory bus.

Table 47. Memory bus clocking specifications @ 1.0 V

Characteristic	Min Freq.(MHz)	Max Freq.(MHz)	Min Data Rate (MT/s)	Max Data Rate (MT/s)	Notes
Memory bus clock frequency and Data Rate for DDR3L	500	800	1000	1600	1, 2, 3
Memory bus clock frequency and Data Rate for DDR4	650	800	1300	1600	1, 2, 3

Notes:

1. **Caution:** The platform clock to SYSCLK ratio and core to platform clock ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform frequency do not exceed their respective maximum or minimum operating frequencies. See Platform to SYSCLK PLL ratio, and Core cluster to SYSCLK PLL ratio, and DDR controller PLL ratios, for ratio settings.

Table 47. Memory bus clocking specifications @ 1.0 V

Characteristic	Min Freq.(MHz)	Max Freq.(MHz)	Min Data Rate (MT/s)	Max Data Rate (MT/s)	Notes
2. The memory bus clock refers to the chip's memory controllers' Dn_MCK[0:3] and Dn_MCK[0:3]_B output clocks, running at half of the DDR data rate. 3. The memory bus clock speed is dictated by its own PLL. See DDR controller PLL ratios.					

5.35.3 Platform to SYSCLK PLL ratio

This table lists the allowed platform clock to SYSCLK ratios.

Because the DDR operates asynchronously, the memory-bus clock-frequency is decoupled from the platform bus frequency.

For all valid platform frequencies supported on this chip, set the RCW Configuration field SYS_PLL_CFG = 0b00.

Table 48. Platform to SYSCLK PLL ratios @ 1.0 V

Binary Value of SYS_PLL_RAT	Platform:SYSCLK Ratio
0_0011	3:1
0_0100	4:1
0_0101	5:1
0_0110	6:1
All Others	Reserved

5.35.4 Core cluster to SYSCLK PLL ratio

The clock ratio between SYSCLK and each of the core cluster PLLs is determined by the binary value of the RCW Configuration field CG*m*_PLL*n*_RAT. This table describes the supported ratios. For all valid core cluster frequencies supported on this chip, set the RCW Configuration field CG*n*_PLL_CFG = 0b00.

This table below lists the supported asynchronous core cluster to SYSCLK ratios.

Table 49. Core cluster PLL to SYSCLK ratios @ 1.0 V

Binary value of CG*m*_PLL*n*_RAT	Core cluster:SYSCLK Ratio
00_1010	10:1
00_1011	11:1
00_1100	12:1
00_1101	13:1
00_1110	14:1
00_1111	15:1
01_0000	16:1
01_0001	17:1
01_0010	18:1

Table continues on the next page...

Table 49. Core cluster PLL to SYSCLK ratios @ 1.0 V (continued)

Binary value of CG*m*_PLL*n*_RAT	Core cluster:SYSCLK Ratio
01_0011	19:1
01_0100	20:1
01_0101	21:1
01_0110	22:1
01_0111	23:1
01_1000	24:1
01_1001	25:1
All others	Reserved

5.35.5 Core complex PLL select

The clock frequency of each core is determined by the binary value of the RCW Configuration field C*1*_PLL_SEL. The tables describe the selections available for each core, where each individual core can select a frequency from their respective tables.

NOTE

There is a restriction that requires that the frequency provided to the ARM A53 core after any dividers must always be greater than half of the platform frequency. Special care must be used when selecting the /2 outputs of a cluster PLL in which this restriction is observed.

Table 50. Core PLL select

Binary Value of C*1*_PLL_SEL	Core cluster ratio
0000	CGA PLL1 /1
0001	CGA PLL1 /2
0100	CGA PLL2 /1
0101	CGA PLL2 /2

5.35.6 DDR controller PLL ratios

DDR memory controller operates asynchronous to the platform.

In asynchronous DDR mode, the DDR data rate to DDRCLK ratios supported are listed in the following table. This ratio is determined by the binary value of the RCW Configuration field MEM_PLL_RAT (bits 10-15).

The RCW Configuration field MEM_PLL_CFG (bits 8-9) must be set to MEM_PLL_CFG = 0b00 for all valid DDR PLL reference clock frequencies supported on this chip.

Table 51. DDR clock ratio @ 1.0 V

Binary value of MEM_PLL_RAT	DDR data-rate:DDRCLK ratio	Maximum supported DDR data-rate (MT/s)
00_1010	10:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
00_1011	11:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
00_1100	12:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
00_1101	13:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
00_1110	14:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
00_1111	15:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0000	16:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0001	17:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0010	18:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0011	19:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0100	20:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0101	21:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0110	22:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0111	23:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_1000	24:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
All Others	Reserved	-

5.35.7 Valid Reference Clocks and PLL Configurations for SerDes Protocols

Each supported SerDes protocol allows for a finite set of valid SerDes-related RCW fields and reference clock frequencies.

The clock ratio between each SerDes PLLs and their respective externally supplied SD1_REF_CLKn_P/SD1_REF_CLKn_N inputs is determined by a set of RCW Configuration fields-SRDS_PRTCL_S1, SRDS_PLL_REF_CLK_SEL_S1, and SRDS_DIV_* as shown in this table.

Table 52. Valid SerDes RCW Encodings and Reference Clocks

SerDes protocol (given lane)	Valid reference clock frequency	Valid setting for SRDS_PRTCL_S1	Valid setting for SRDS_PLL_REF_CLK_SEL_S1		Valid setting for SRDS_DIV_*_Sn
			PLL1	PLL2	
High Speed Serial interface					
PCI Express 2.5 Gbps (doesn't negotiate upwards)	100 MHz	Any PCIe	0: 100 MHz	0: 100 MHz	10: 2.5G
	125 MHz		1: 125 MHz	1: 125 MHz	
PCI Express 5 Gbps (can negotiate up to 5 Gbps)	100 MHz	Any PCIe	0: 100 MHz	0: 100 MHz	01: 5G
	125 MHz		1: 125 MHz	1: 125 MHz	
SATA (1.5, 3, 6 Gbps)	100 MHz	Any SATA	0: 100 MHz	-	Don't Care
	125 MHz		1: 125 MHz	-	
Networking interfaces					
SGMII (1.25 Gbps)	100 MHz	SGMII @ 1.25 Gbps	0: 100 MHz	0: 100 MHz	Don't Care
	125 MHz		1: 125 MHz	1: 125 MHz	
2.5 G SGMII (3.125 Gbps)	125 Mhz	SGMII @ 3.125 Gbps	0: 125 MHz	-	Don't Care
	156.25 MHz		1: 156.25 MHz	-	
QSGMII (5 Gbps)	100 MHz	Any QSGMII	0: 100 MHz	0: 100 MHz	Don't Care
	125 MHz		1: 125 MHz	1: 125 MHz	
XFI (10.3125 Gbps)	156.25 Mhz		1: 156.25 MHz	-	-
				-	
Notes: 1) A spread-spectrum reference clock is permitted for PCI Express. However, if any other high speed interface such as SGMII, QSGMII, SATA, or Debug is used concurrently on the same SerDes bank, spread-spectrum clocking is not permitted. 2) SerDes lanes configured as SATA initially operate at 3.0Gbps. 1.5Gbps operation may later be enabled through the SATA IP itself. It is possible for software to set each SATA at different rates.					

5.35.8 Frequency options

This section discusses interface frequency options.

5.35.8.1 SYSCLK and core cluster frequency options

This table shows the expected frequency options for SYSCLK and core cluster frequencies.

Table 53. SYSCLK and core cluster frequency @ 1.0 V[1]

Core cluster: SYSCLK Ratio	SYSCLK (MHz)		
	64.00	66.67	100.00
	Core cluster Frequency - (MHz)[1]		
10:1			1000

Table continues on the next page...

Table 53. SYSCLK and core cluster frequency @ 1.0 V[1] (continued)

Core cluster: SYSCLK Ratio	SYSCLK (MHz)		
	64.00	66.67	100.00
	Core cluster Frequency - (MHz)[1]		
11:1			1100
12:1			1200
13:1			1300
14:1			1400
15:1		1000	1500
16:1	1024	1067	1600
17:1	1088	1133	
18:1	1152	1200	
19:1	1216	1267	
20:1	1280	1333	
21:1	1344	1400	
22:1	1408	1467	
23:1	1472	1533	
24:1	1536	1600	
25:1	1600		

Notes:

1. Core cluster output is the operating frequency of the core.
2. Core cluster frequency values are shown rounded up to the nearest whole number (decimal place accuracy removed)
3. When using Single Source clocking only 100MHz input is available.

5.35.8.2 SYSCLK and platform frequency options

This table shows the expected frequency options for SYSCLK and platform frequencies.

Table 54. SYSCLK and platform frequency options @ 1.0 V

Platform: SYSCLK Ratio	SYSCLK (MHz)		
	64.00	66.67	100.00
	Platform Frequency (MHz)[1]		
3:1			300
4:1	256	267	400
5:1	320	333	
6:1	384	400	

Notes:

1. Platform frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed)
2. When using Single source clocking, only 100MHz options are valid

5.35.8.3 DDRCLK and DDR data rate frequency options

This table shows the expected frequency options for DDRCLK and DDR data rate frequencies.

Table 55. DDRCLK and DDR data rate frequency options @ 1.0 V

DDR data rate: DDRCLK Ratio	DDRCLK (MHz)		
	64.00	66.67	100.00
	DDR Data Rate (MT/s)[1]		
10:1			1000
11:1			1100
12:1			1200
13:1			1300
14:1			1400
15:1		1000	1500
16:1	1024	1067	1600
17:1	1088	1133	
18:1	1152	1200	
19:1	1216	1266	
20:1	1280	1333	
21:1	1344	1400	
22:1	1408	1466	
23:1	1472	1533	
24:1	1536	1600	

Notes:

1. DDR data rate values are shown rounded up to the nearest whole number (decimal place accuracy removed)
2. When using Single Source clocking, only 100MHz options are available.
3. Minimum Frequency supported by DDR4 is 1300MT/s. DDR3 supports a minimum of 1000MT/s.

5.35.8.4 SYSCLK and eSDHC high speed modes frequency options

This table shows the frequency multiplier options for SYSCLK when eSDHC operates in High Speed modes (>=52 MHz). For low frequency options CGA PLL2 is bypassed and eSDHC receives platform clock directly.

Table 56. SYSCLK multiplier/frequency options when eSDHC operates in High Speed mode (clocked by CGA PLL2 / 1)

Core cluster: SYSCLK Ratio	SYSCLK (MHz)		
	64.00	66.67	100.00
	Resultant Frequency (MHz)[1]		
12:1			1200
18:1	1152	1200	

Notes:

1. Resultant frequency values are shown rounded up to the nearest whole number (decimal place accuracy removed)
2. For Low speed operation, eSDHC is clocked from Platform PLL and does not use CGA PLL2.

5.35.8.5 Minimum platform frequency requirements for high-speed interfaces

The platform clock frequency must be considered for proper operation of high-speed interfaces as described below:.For proper PCI Express operation, the platform clock frequency must be greater than or equal to:

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{16}$$

Figure 18. Gen 1 PEX minimum platform frequency

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

Figure 19. Gen 2 PEX minimum platform frequency

See section "Link Width," in the chip reference manual for PCI Express interface width details. Note that "PCI Express link width" in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection. It refers to the widest port in use, not the combined width of the number ports in use.

6 Thermal

This section discusses the thermal model and management of the chip.

6.1 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local Freescale sales office.

6.2 Temperature diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A). These devices feature series resistance cancellation using 3 current measurements, where up to 1.5kΩ of resistance can be automatically cancelled from the temperature result, allowing noise filtering and a more accurate reading.

The following are the specifications of the chip's on-board temperature diode:

Operating range: 10 - 230μA

Ideality factor over 13.5 - 220 μA; Temperature range 80°C - 105°C: n = 1.004 ± 0.008

6.3 Thermal management information

This section provides thermal management information for the flip-chip, plastic-ball, grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design-the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in Figure 20. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 15 pounds force (65 Newton).

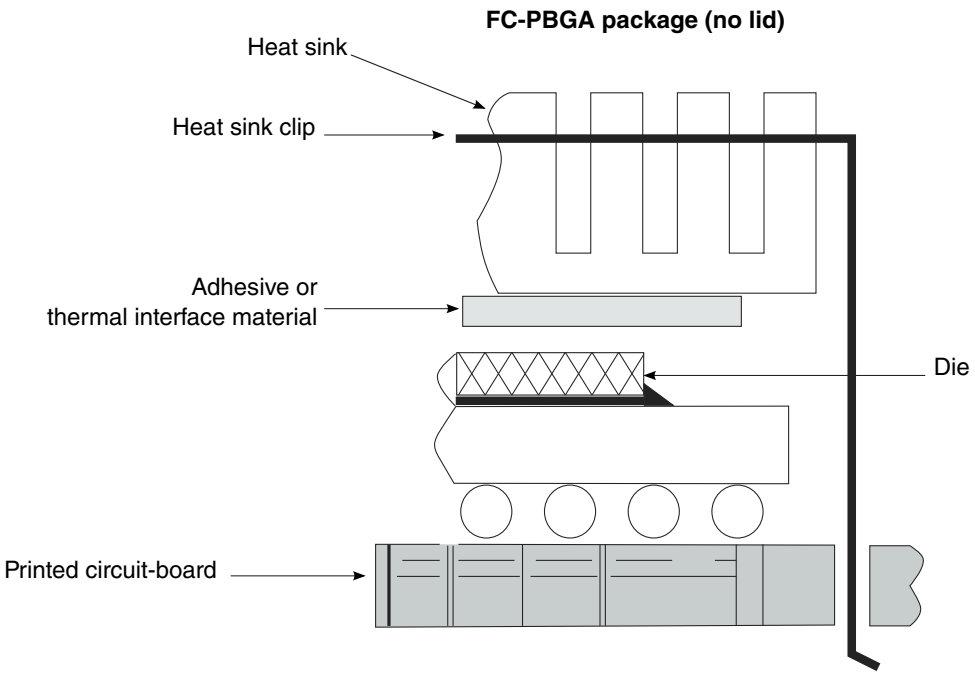


Figure 20. Package exploded, cross-sectional view-FC-PBGA (no lid)

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

6.3.1 Internal package conduction resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

This figure shows the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

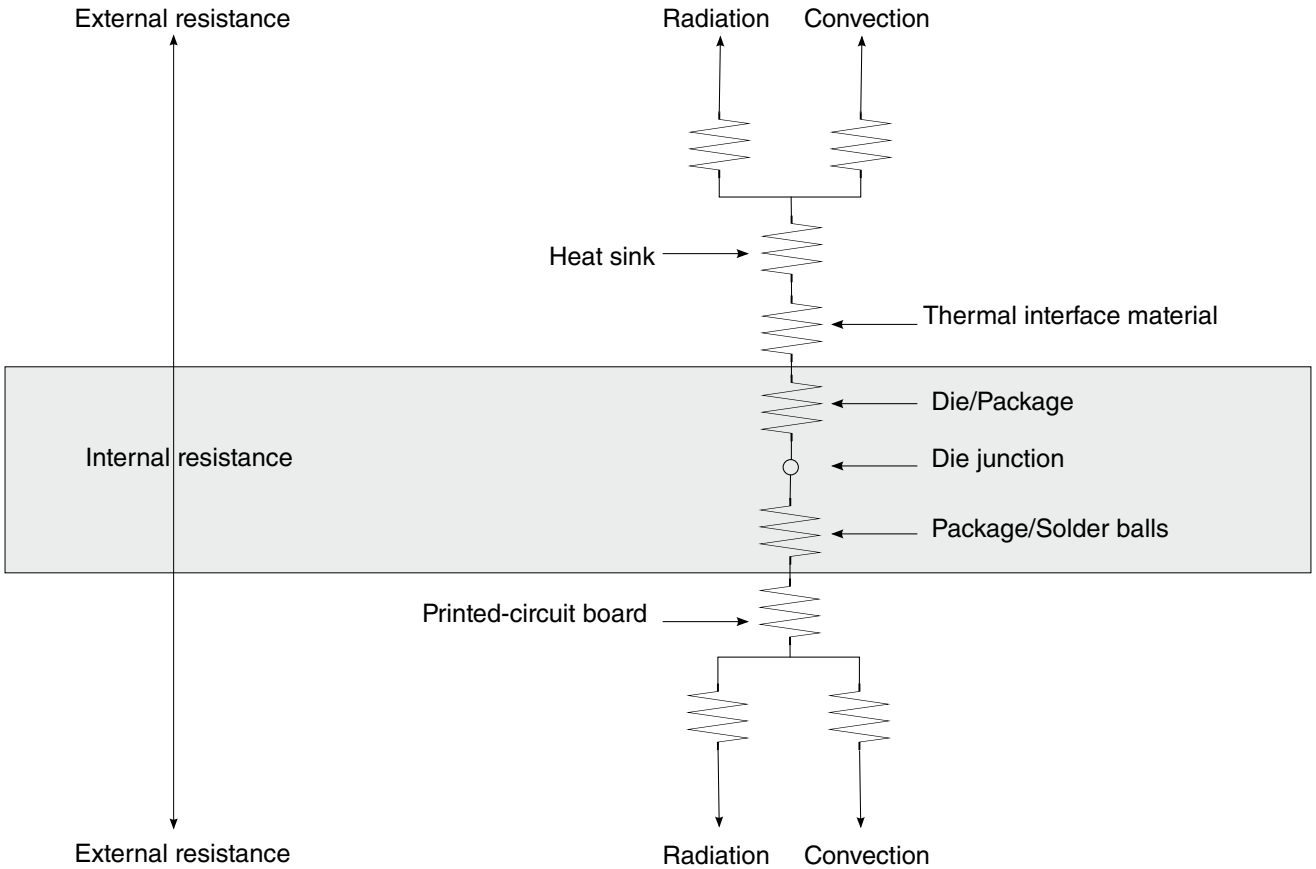


Figure 21. Package with heat sink mounted to a printed-circuit board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

6.3.2 Thermal interface materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 20).

The system board designer can choose among several types of commercially available thermal interface materials.

7 Revision history

This table summarizes changes to this document.

Table 57. Revision history

Revision	Date	Change
0	03/2016	Initial release

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number AN5012
Revision 0, 03/2016

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