PRODUCT BULLETIN

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ISSUE DATE:	07-Jun-2016
NOTIFICATION:	17145
TITLE:	Release New Errata and Update to Erratum A-008822 Workaround for the LS1020/21/22 Family of Devices
EFFECTIVE DATE:	08-Jun-2016

DEVICE(S)

MPN
LS1020ASE7HNA
LS1020ASE7HNB
LS1020ASE7KNA
LS1020ASE7KQA
LS1020ASE7KQB
LS1020ASN7HNA
LS1020ASN7HNB
LS1020ASN7KNA
LS1020ASN7KQA
LS1020ASN7KQB
LS1020AXE7HNA
LS1020AXE7HNB
LS1020AXE7KNA
LS1020AXE7KQA
LS1020AXE7KQB
LS1020AXN7HNA
LS1020AXN7HNB
LS1020AXN7KNA
LS1020AXN7KQA
LS1020AXN7KQB
LS1021ASE7HNA
LS1021ASE7HNB
LS1021ASE7KNA
LS1021ASE7KQA
LS1021ASE7KQB
LS1021ASE7XHNA
LS1021ASE7XHNB
LS1021ASE7XKQA
LS1021ASE7XKQB
LS1021ASE7XMQB
LS1021ASEX7XHNA
LS1021ASEX7XKQA
LS1021ASN7HNA
LS1021ASN7HNB
LS1021ASN7KNA

LS1021ASN7KQA
LS1021ASN7KQB
LS1021ASN7XHNB
LS1021ASN7XKQB
LS1021ASN7XMQB
LS1021AXE7HNA
LS1021AXE7HNB
LS1021AXE7KNA
LS1021AXE7KQA
LS1021AXE7KQB
LS1021AXE7XHNA
LS1021AXE7XKQA
LS1021AXN7HNA
LS1021AXN7HNB
LS1021AXN7KNA
LS1021AXN7KQA
LS1021AXN7KQB
LS1022ASE7EKA
LS1022ASE7EKB
LS1022ASE7XEKA
LS1022ASEX7XEKA
LS1022ASN7EKA
LS1022ASN7EKB
LS1022AXE7EKA
LS1022AXE7EKB
LS1022AXE7XEKA
LS1022AXN7EKA
LS1022AXN7EKB
PLS1020ASE7KNA
PLS1021ASE7KNA
PLS1021ASN7XKNA
PLS1021ASN7XKQA
PLS1022ASE7EKA
PS1020ASE7HNA
PS1020ASE7HNB
PS1020ASE7KQA
PS1020ASE7KQB
PS1020ASN7HNA
PS1020ASN7HNB
PS1020ASN7KQA
PS1020ASN7KQB
PS1020AXE7KQA
PS1020AXE7KQB
PS1020AXN7KQA
PS1020AXN7KQB
PS1021ASE7HNA
PS1021ASE7HNB
PS1021ASE7KQA
PS1021ASE7KQB
PS1021ASE7XHNA
PS1021ASE7XKQA
PS1021ASN7HNA
PS1021ASN7HNB
PS1021ASN7KQA

PS1021ASN7KQB
PS1021AXE7KQA
PS1021AXE7KQB
PS1021AXE7XHNA
PS1021AXE7XKQA
PS1021AXN7KQA
PS1021AXN7KQB
PS1022ASE7EKA
PS1022ASE7EKB
PS1022ASE7XEKA
PS1022ASN7EKA
PS1022ASN7EKB
PS1022AXE7XEKA
PS1022AXN7EKA
PS1022AXN7EKB
PSLS1020ASN7KNA
SLS1021ASE7XKNA
SLS1021ASE7XKQA

AFFECTED CHANGE CATEGORIES

- ERRATA

DESCRIPTION OF CHANGE

This notification is for the release of the following new errata: **IFC A-009241, USB A-010127, USB A-010129, USB A-010131, USB A-010151, QSPI A-009283, GIC A-010111, SATA A-010240 & PCI-e A-010315.** In addition **PCI-e A-008822** erratum workaround is updated.
A-009241: Unaligned write transactions to IFC may result in corruption of data
Affects: IFC
Description: 16 byte unaligned write from system bus to IFC may result in extra unintended writes on external IFC interface that can corrupt data on external flash.
Impact: Data corruption on external flash may happen in case of unaligned writes to IFC memory space.
Workaround: Following are the workarounds:
For write transactions from core, IFC interface memories (including IFC SRAM) should be configured as “device type" memory in MMU.
For write transactions from non-core masters (like system DMA), the address should be 16 byte aligned and the data size should be multiple of 16 bytes.

A-010127: Hot Reset Failure During U1/U2 Entry for USB 3.0
Affects: USB
Description: When the xHCI driver issues Port Reset (PORTSC.PR = 1) after the link partners have already exchanged LGO_Ux, LAU, and LPMA link commands for U1/U2 entry, the USB 3.0 controller incorrectly enters the Recovery state to perform a Hot Reset (TS2 ordered sets and TS1/TS2 handshake) instead of entering into U1/U2. The window for internally transitioning to U1/U2 after LAU and LPMA link commands is 16 mac3_clk (128 ns). This problem occurs only when the xHCI driver programs PORTSC.PR = 1 during the 128 ns window.
Impact: The impact is delay for the USB 3.0 controller to receive Warm Reset from the xHCI driver.
Workaround: No workaround is required. If a Hot Reset fails because of a TS1/TS2 handshake timeout, a downstream port transitions to SS.Inactive, which generates a PORTSC.PLC interrupt to the xHCI driver. The xHCI driver then programs a Warm Reset to the controller.

A-010129: USB 2.0 reset not driven while port is in the Resume State
Affects: USB
Description: This issue is applicable only to USB 2.0 ports in Host mode and assumes that PORTSC.PLS = 1111b. If the xHCI driver resets the USB 2.0 port by programming PORTSC.PR=1, then the USB controller does not drive reset and does not generate an interrupt (PORTSC.PRC=1) while it is in USB 2.0 Resume State.

Impact: The following are impacts for this erratum:
• The USB 2.0 port cannot be reset.
• The xHCI driver does not receive a port status change event interrupt (PORTSC.PRC=1).
Workaround: The xHCI driver should not program a USB 2.0 reset (PORTSC.PR=1) while in resume. When the xHCI driver is ready to program a USB 2.0 reset, check the PORTSC.PLS bit. Only program PORTSC.PR=1 when PORTSC.PLS is not set to 1111b.

A-010131: U3 request gets dropped when controller tries U1-to-U2 entry
Affects: USB
Description: This erratum is applicable for the USB 3.0 Super Speed host mode operation. When the U2 timer expires while in U1 mode, the USB 3.0 controller completes a U1->U2 entry operation lasting three mac3_clk (24 ns). If the xHCI driver issues a U3 request during this operation, the controller drops this request.
Impact: The controller ignores the request when the xHCI driver programs the U3 entry (PORTSC.PLS= U3). The occurrence of this issue is rare because of the 24 ns window.
Workaround: The xHCI driver must include following steps:
1. Before initiating U3 entry, save PORTPMSC
2. Disable U2 entry by programming PORTPMSC[U2 Timeout] = h'FF
3. After U3 entry, re-enable U2 timer by programming PORTPMSC with the value saved in Step 1

A-010151: Unreliable receiver detection in low power P3 mode
Affects: USB
Description: The USB 3.0 controller enables the Receiver (Rx) Detection feature in low power mode 3 (P3 mode). However, USB 3.0 PHY does not reliably support receiver detection in P3 mode. Therefore, some USB 3.0 devices are not detected reliably in Super Speed mode.
This erratum does not cause a compliance issue, because the receiver detection in P3 mode is beyond the PHY Interface for PCI Express and USB 3.0 (PIPE) specification which only requires receiver detection in power mode 2 (P2 mode).
Impact: Some USB3.0 devices may not be detected reliably in Super Speed mode.
Workaround: Set GUSB3PIPECTL[DisRxDetP3]=1 to configure USB3.0 in P2 mode for RX Detection.

A-009283: QuadSPI: Illegal accesses to SPI flash memory can result in a system hang
Affects: QSPI
Description: Under normal circumstances you can program the QuadSPI_LUTn using a read instruction so that the software reads data correctly from flash memory through the AMBA-AHB system bus (AHB). However, when programming the QuadSPI_LUTn as a non-read sequence, the flash memory does not send back any data and the system may hang, which requires a reset to recover. This is considered illegal programming. There is no time-out mechanism to recover from this scenario.
Impact: The system must be reset for illegal programming
Workaround:
Use a watch dog timer of 1 second. The start of this timer can be triggered before a read through AHB. If it expires, the system needs to be reset (set DCFG_CCSR_RSTCR[RESET_REQ]). The timer must be cleared when QuadSPI_SR[BUSY]=0

A-010111: Non-core master can only access Generic Interrupt Controller (GIC) banked registers of core 0
Affects: GIC
Description: An ARM GIC, "per core banked GIC register" has the same address but one copy for each individual core. During normal operation, a core specific register is accessed from each core by driving its unique core-ID attribute in addition to the address. When accessing these registers from non-core masters like debugger interface, the unique core-ID attribute is not implemented correctly. Therefore, only Core0 specific registers are accessible from non-core masters. Non-Core0 per core banked GIC registers cannot be retrieved.
Impact: The non-Core0 "per core banked GIC registers" cannot be retrieved by non-core masters. For example, the debugger cannot access "per core banked GIC registers" belong to cores other than Core 0.
Workaround: None. Use core software to access "non-core 0 per core banked GIC registers".

A-010240: SATA interface in BIST-L mode fails
Affects: SATA
Description: The SATA interface fails in BIST-L mode (high CRC errors) during the receiver jitter tolerance test (RSG).
Impact: SATA interface fails in BIST-L mode operation which results in SATA compliance test failure.
Workaround: None

A-010315: Read access to an unselected PCI Express controller's space causes core(s) and platform to hang
Affects: PCI-e
Description: Read access to an unselected PCI Express controller's space causes core(s) and platform to hang. An unselected PCI Express controller is any PCI Express controller that is not selected by a specific SRDS_PRTCL_Sn option in RCW.
Impact: The core(s) and platform hang when reading an unselected PCI Express controller's space.
Workaround: First, prevent access to any unselected PCI Express controller by implementing the workaround procedure below such that any future unanticipated access will result in an exception. Then, configure the exception handler to identify and block such accesses to prevent the core(s) and platform from hanging.
To prevent access to any unselected PCI Express controller, write all zeros to the corresponding PCI Express controller bit fields in the related Configuration Security Level (CSL) register of Central Security Unit (CSU).
For example, if PCI Express controller 1 is unselected, perform the following:
1. While preserving other bit fields, write all zeros to CSU_CSL3[24:16]. This prevents access to the register space of PCI Express controller 1.
2. While preserving other bit fields, write all zeros to the CSU_CSL0[8:0]. This prevents the access to the I/O and memory space of PCI Express controller 1.
For normal boot: The workaround can be implemented in either PBI code or U-Boot. For UBoot, the workaround should be implemented at the early stage of the boot code to avoid potential impact.
For secure boot: Because the CSU access is prohibited during PBI phase, implement the workaround in external secure boot code (ESBC) immediately after the PBI stage is complete (similar to the U-Boot implementation of normal boot process).

Workaround update to **A-008822**: Change the default AXI system error response behavior for PCI Express outbound non-posted requests
Affects: PCIe
Description: By default, when the PCI Express controller experiences an erroneous completion from an external completer for its outbound non-posted request, it always sends an OKAY response to the device's internal AXI slave system interface. This is desirable for outbound configure transactions to prevent an unnecessary error response from propagating through higher-level system hierarchy, because erroneous completion is a commonly expected behavior during PCI Express bus scan.
However, such default system error response behavior cannot be used for other types of outbound non-posted requests. For example, the outbound memory read transaction requires an actual ERROR response when experiencing erroneous completion from an external completer, like UR completion or completion timeout.
Impact: The device's higher level system hierarchy cannot detect the error condition when the PCI Express controller experiences an erroneous completion from the external completer for its outbound non-posted request. This is not the case for configure transactions.
Workaround: Write to the PCI Express controller's configure space offset 8D0h with 0000_0001h during the pre-boot initialization (PBI) process.

REASON FOR CHANGE
Alert customers of errata release.

ANTICIPATED IMPACT OF PRODUCT CHANGE(FORM, FIT, FUNCTION, OR RELIABILITY)
No impact to product form, fit, function or reliability.

NOTE:

THE CHANGE(S) SPECIFIED IN THIS NOTIFICATION WILL BE IMPLEMENTED ON THE EFFECTIVE DATE LISTED ABOVE. To request further data or inquire about the notification, please enter a Support Case. Be aware that after you select this link to enter your request, you must choose the topic "Product Change Notification" once on the Salesforce page.
For sample inquiries - please go to www.nxp.com

QUALIFICATION STATUS: N/A

QUALIFICATION PLAN:

N/A

RELIABILITY DATA SUMMARY:

N/A

ELECTRICAL CHARACTERISTIC SUMMARY:

N/A

CHANGED PART IDENTIFICATION:

N/A

ATTACHMENT(S):

External attachment(s) for this notification can be viewed at:
17145_PB_17145.pdf
