NXP Semiconductors
Application Note

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QorIQ LS1028A Design Checklist

1 About this document

This document provides recommendations for new designs based on the LS1028A, which is a cost-effective, power-efficient, and highly integrated system-onchip (SoC) design that extends the reach of the NXP Value Performance line of QorIQ communications processors.

This document can also be used to debug newly-designed systems by highlighting those aspects of a design that merit special attention during initial system start-up.

NOTE

This document applies to the LS1028A, LS1018A, LS1027A and LS1017A devices. For a list of functionality differences, see the appendices in *QorIQ LS1028A Reference Manual* (document LS1028ARM).

Contents

2 Before you begin

Ensure you are familiar with the following NXP collateral before proceeding:

- *QorIQ LS1028A Data Sheet*
- *QorIQ LS1027A Data Sheet*

3 Simplifying the first phase of design

Before designing a system with the chip, it is recommended that the designer be familiar with the available documentation, software, models, and tools.

This figure shows the major functional units within the LS1028A chip.

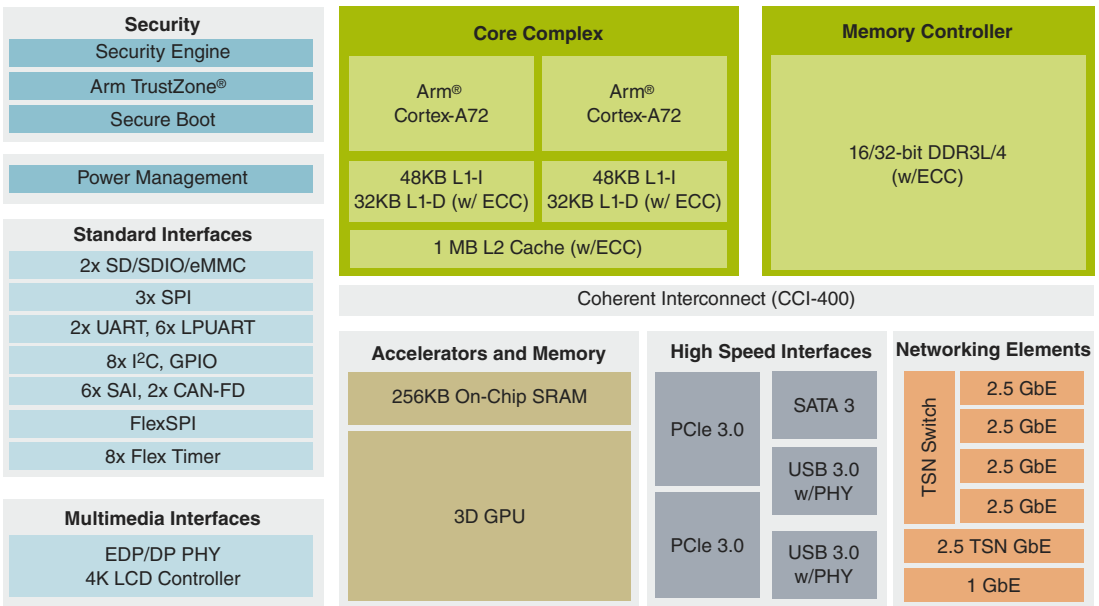

Figure 1. LS1028A block diagram

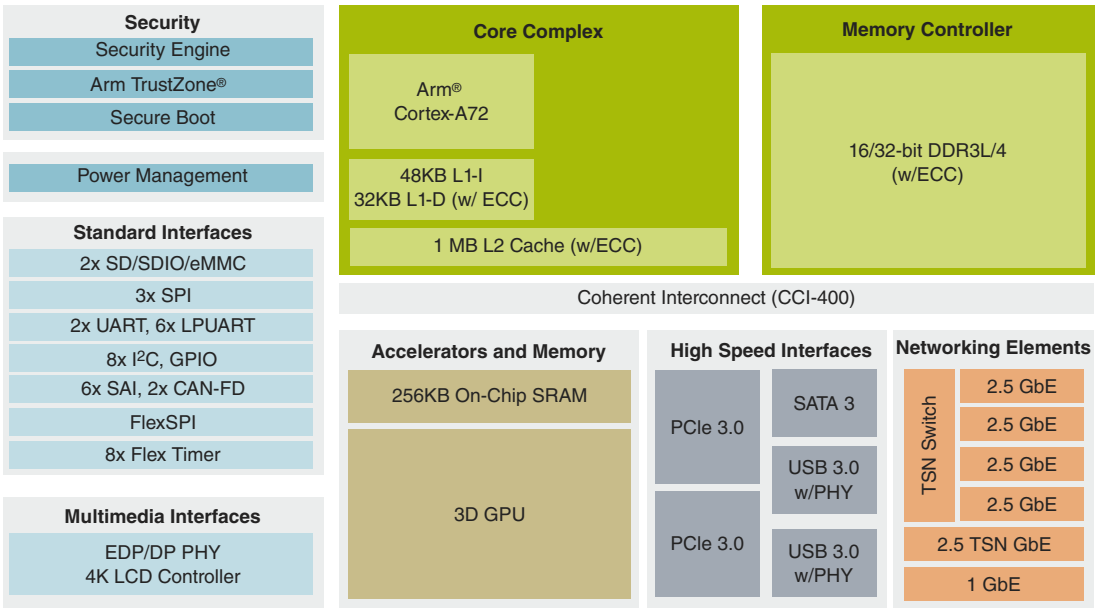

Figure 2. LS1018A block diagram

This figure shows the major functional units within the LS1027A chip.

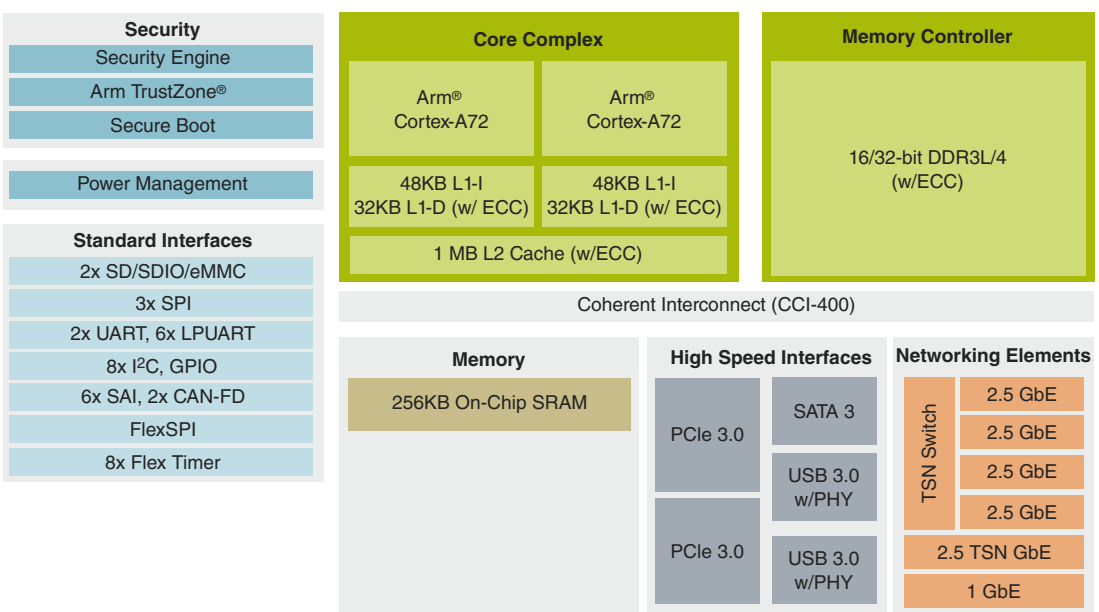

Figure 3. LS1027A block diagram

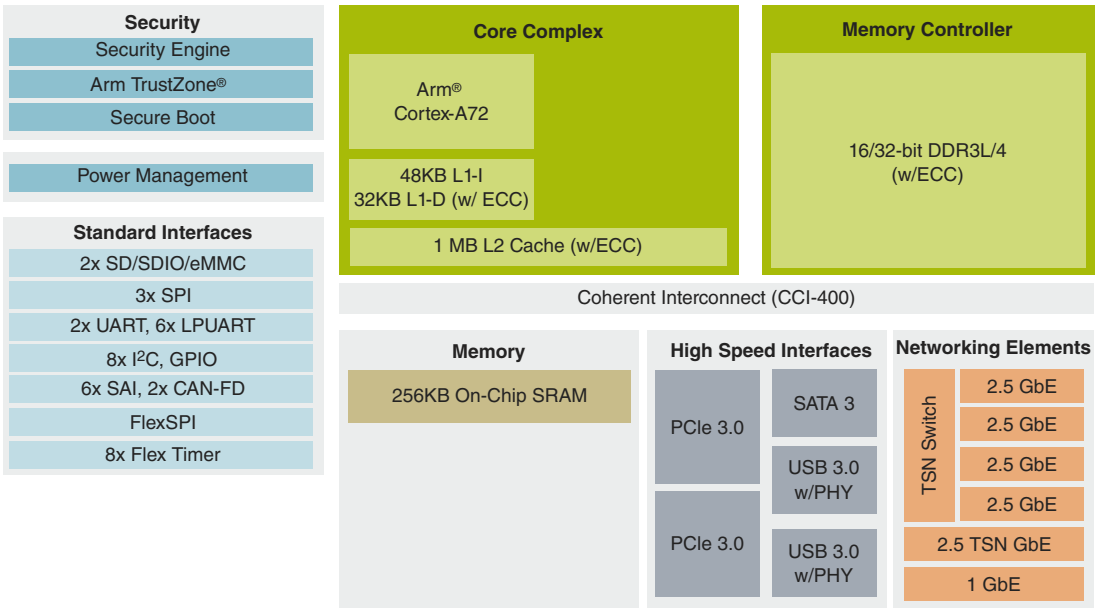

Figure 4. LS1017A block diagram

3.1 Recommended resources

This table lists helpful tools, training resources, and documentation, some of which may be available only under a non-disclosure agreement (NDA). Contact your local field applications engineer or sales representative to obtain a copy.

Table 1. Helpful tools and references

ID	Name	Location
Related collateral		
LS1028A	*QorIQ LS1028A Data Sheet*	www.nxp.com
LS1027A	*QorIQ LS1027A Data Sheet*	www.nxp.com
LS1028ARM	*QorIQ LS1028A Reference Manual*	www.nxp.com
LS1028ACE	*QorIQ LS1028A Chip Errata*	Contact your NXP representative
AN5125	*Introduction to Device Trees - Application note*	
cortex_a72_mpcore_trm_100095_0003_06_en	*Arm® Cortex®-A72 MPCore Processor - Technical Reference Manual*	Attached with LS1028ARM
AN4871	*Assembly Handling and Thermal Solutions for Lidless Flip Chip Ball Grid Array Packages*	www.nxp.com
AN4311	*SerDes Reference Clock Interfacing and HSSI Measurements Recommendations*	www.nxp.com
AN4290	*Configuring the Data Path Acceleration Architecture (DPAA)*	
AN4039	*PowerQUICC DDR3 SDRAM Controller Register Setting Considerations*	www.nxp.com

Table continues on the next page...

Table 1. Helpful tools and references (continued)

ID	Name	Location
AN3940	*Hardware and Layout Design Considerations for DDR3 SDRAM Memory Interfaces*	
AN5097	*Hardware and Layout Design Considerations for DDR4 SDRAM Memory Interfaces*	
AN3939	*DDR Interleaving for QorIQ Processors*	
AN2919	*Determining the I^2C Frequency Divider Ratio for SCL*	
Software tools		
	CodeWarrior Development Software for Arm® v8 64-bit based QorIQ LS-Series Processors	www.nxp.com
	Software Development Kit for LS1028A	www.nxp.com
Hardware tools		
	CodeWarrior TAP	www.nxp.com
	QorIQ LS Processor Probe Tips for CodeWarrior TAP	www.nxp.com
	QorIQ LS1028A reference design board	www.nxp.com
Models		
IBIS	To ensure first path success, NXP strongly recommends using the IBIS models for board level simulations, especially for SerDes and DDR characteristics.	Contact your NXP representative
BSDL	Use the BSDL files in board verification.	
Flotherm	Use the Flotherm model for thermal simulation. Especially without forced cooling or constant airflow, a thermal simulation should not be skipped.	
Available training		
-	Our third-party partners are part of an extensive alliance network. More information can be found at www.nxp.com/alliances.	www.nxp.com/alliances
-	Training materials from past Smart Network Developer's Forums and NXP Technology Forums (FTF) are also available at our website. These training modules are a valuable resource for understanding the chip.	

NOTE

Design requirements in the device hardware specification supersede requirements mentioned in design checklist and design requirements mentioned in design checklist supersede the design/implementation of the NXP reference design (RDB) system.

3.2 Product revisions

This table lists the system version register (SVR) and Arm core main ID register (TRCIDR1) values for the various chip silicon derivatives.

Table 2. Chip product revisions

Part	Device revision	Arm® Cortex®-A72 MPCore processor revision	Arm core main ID register	System version register value	TEST_SEL_B	cfg_svr[0]	Note
LS1028AN	1.0	r0p2	0x410F_D081h	0x870B_0110h	1	1	Without security
LS1028AE	1.0	r0p2	0x410F_D081h	0x870B_0010h	1	1	With security
LS1027AN	1.0	r0p2	0x410F_D081h	0x870B_0510h	0	1	Without security
LS1027AE	1.0	r0p2	0x410F_D081h	0x870B_0410h	0	1	With security
LS1018AN	1.0	r0p2	0x410F_D081h	0x870B_2110h	1	0	Without security
LS1018AE	1.0	r0p2	0x410F_D081h	0x870B_2010h	1	0	With security
LS1017AN	1.0	r0p2	0x410F_D081h	0x870B_2510h	0	0	Without security
LS1017AE	1.0	r0p2	0x410F_D081h	0x870B_2410h	0	0	With security

4 Power design recommendations

4.1 Power pin recommendations

Table 3. Power and ground pin termination checklist

Signal name	Used		Not used	Completed
OV_{DD}	General I/O supply SPI2/3, FlexSPI, SDHC2, DUART, LPUART, Temper_Detect, System control, GPIO1/2/3, I2C, Ethernet interface, Ethernet management interface (EMI), TSEC_1588, Debug, JTAG, POR signals, DFT, USB_PWRFAULT, USB_DRVVBUS, SAI3/4/5/6, Flextimer, CAN	1.8 V	Must remain powered	
EV_{DD}	eSDHC supply - switchable eSDHC1, GPIO1_DAT[16:21], SPI1, SAI1, SAI2	1.8/3.3 V dynamically switchable	Must remain powered	
$G1V_{DD}$	DDR3L/DDR4 supply	1.35V / 1.2 V	Must remain powered	
SV_{DD}	SerDes core logic and receiver supply, DIFF_SYSCLK_P/N	0.9/1.0 V	Must remain powered	
XV_{DD}	SerDes transmitter supply	1.35 V	Must remain powered	
PROG_MTR	This pin must be connected or pulled down via a resistor to ground (GND).			

Table continues on the next page...

Table 3. Power and ground pin termination checklist (continued)

Signal name	Used		Not used	Completed
TA_PROG_SFP	SFP fuse programming override supply	Should only be supplied 1.8 V during secure boot programming. For normal operation, this pin needs to be pulled down through a resistor.		
TH_V_{DD}	Thermal Monitor Unit supply	1.8 V	Must remain powered	
V_{DD}	Supply for cores and platform	0.9/1.0 V	Must remain powered	
TA_BB_V_{DD}	Battery Backed Low power security monitor supply	0.9/1.0 V	Must remain powered	
AV_{DD}_CGA1	CPU cluster group A PLL1 supply	1.8 V (independent supplies derived from board 1.8 V)	Must remain powered	
AV_{DD}_CGA2	CPU cluster group A PLL2 supply	1.8 V (independent supplies derived from board 1.8 V)	Must remain powered	
AV_{DD}_PLAT	Platform PLL supply	1.8 V (independent supplies derived from board 1.8 V)	Must remain powered	
AV_{DD}_D1	DDR PLL supply	1.8 V (independent supplies derived from board 1.8 V)	Must remain powered	
AV_{DD}_SD1_PLL1	SerDes1 PLL 1 supply	1.35 V (filtered off of XV_{DD} supply)	Must remain powered (no need to filter from XV_{DD})	
AV_{DD}_SD1_PLL2	SerDes1 PLL 2 supply	1.35 V (filtered off of XV_{DD} supply)	Must remain powered (no need to filter from XV_{DD})	
$SENSEV_{DD}$	V_{DD} sense pin	Sense pin, Must be connected to regulator feedback		
USB_HV_{DD}[3]	USB PHY Transceiver supply	3.3 V	Tie to GND	
USB_SDV_{DD}[3]	Analog and Digital HS supply for USBPHY	0.9/1.0 V	Tie to GND	
USB_SV_{DD}[3]	Analog and Digital SS supply for USBPHY	0.9/1.0 V	Tie to GND	
DP_OV_{DD}[2]	PMA common I/O supply	1.8V	The pins are RSVD in LS1027A	
DP_SV_{DD}[2]	PMA transmit supply	0.9/1.0 V	The pins are RSVD in LS1027A	
DP_AV_{DD}[2]	PMA common core supply	0.9/1.0 V	The pins are RSVD in LS1027A	
AV_{DD}_PIXEL[2]	Pixel clock PLL analog supply	1.8 V	The pins are RSVD in LS1027A	
PIXEL_DV_{DD}[2]	Pixel clock PLL digital supply	0.9/1.0 V	The pins are RSVD in LS1027A	
GND	Core, platform and PLL ground	GND	Tie to GND	
SD_GND	SerDes core logic, transceiver and PLL ground	GND	Tie to GND	
SENSEGND	Ground sense pin	Connect to regulator feedback		

NOTE

1. For supported voltage/frequency options, see the orderable part list of *QorIQ LS1028A and LS1018A Multicore Communications Processors* at www.nxp.com.
2. RSVD pins in LS1027A should be NC
3. If all USB power supplies are connected to GND when USB is not used, the JTAG IEEE Std 1149.1-2001 Boundary Scan Register (BSR) will not shift contents between TDI and TDO. USB_SVDD must be powered in order for the USB BSR cells to shift. In this case, the USB boundary cells cannot observe or control USB pins. This affects the USB BSR cells during EXTEST, EXTEST_PULSE, EXTEST_TRAIN, CLAMP and SAMPLE. The only fails are related to USB IO's when USB_SVDD is powered on, and USB_SDVDD and USB_HVDD are powered off. If all USB power supplies are connected to GND, the other 1149.1 JTAG or DAP debug instructions will still operate.

4.2 Thermal Power

The following graphs provide the thermal VDD power for LS1028A, LS1018A, LS1027A and LS1017A. Thermal power numbers are based on worst-case processed device. Thermal power assumes Dhrystone running with activity factor of 80% (on all cores) for LS102x devices and 90% for LS101x devices and executing DMA on the platform at 100% activity factor. The thermal power is used for the thermal solution design. The graphs use the Arm A72 speed as label. Please refer to Maximum VDD Power and IO Power for A72/Platform/DDR speed combinations.

Total power dissipation is the sum of the VDD power and IO power and must be used for the thermal solution design.

Total thermal power = VDD thermal power + IO thermal power

The power is measured when the device runs at the speed combinations given in Table 5.

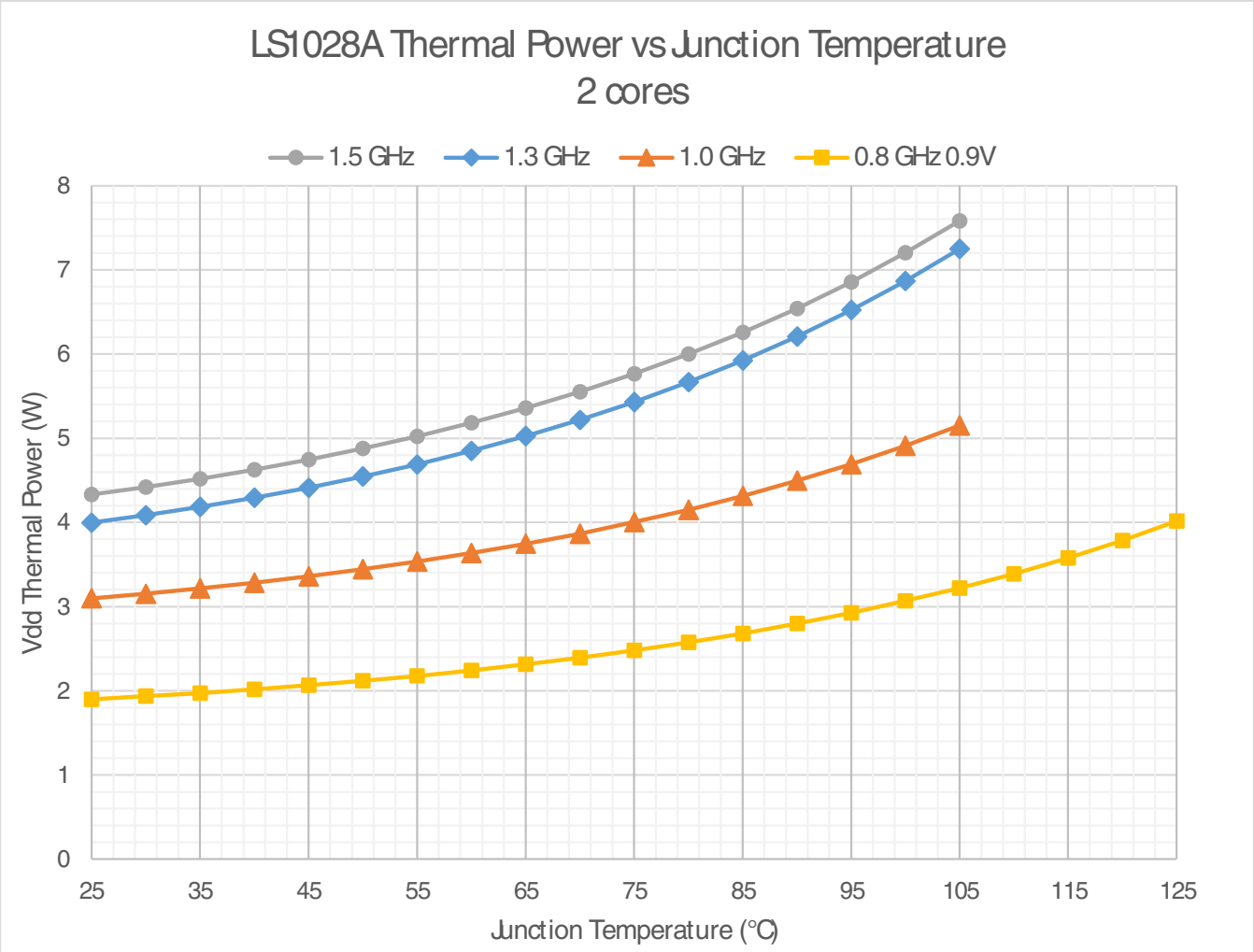

Figure 5. LS1028A Thermal VDD Power vs Junction Temperature

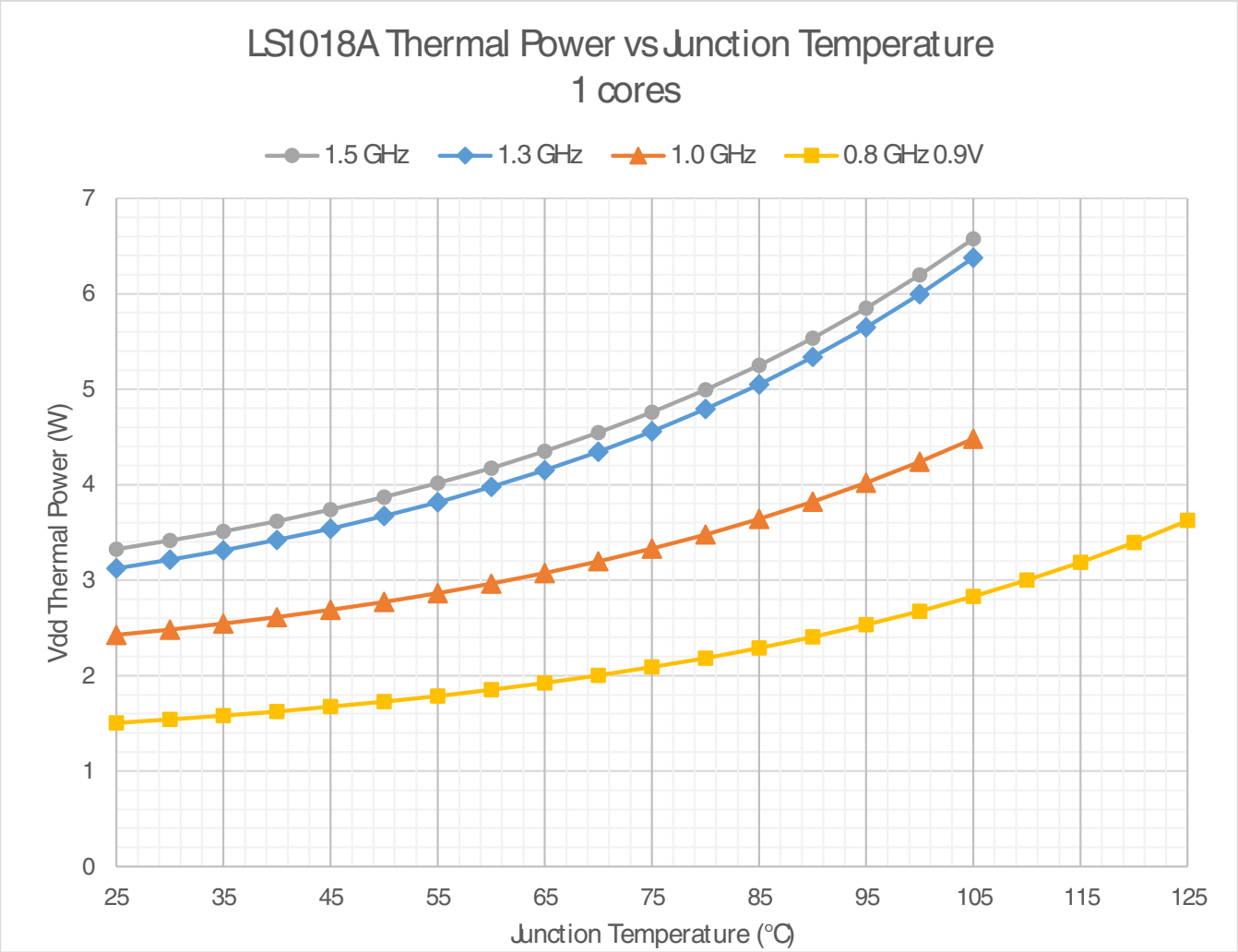

Figure 6. LS1018A Thermal VDD Power vs Junction Temperature

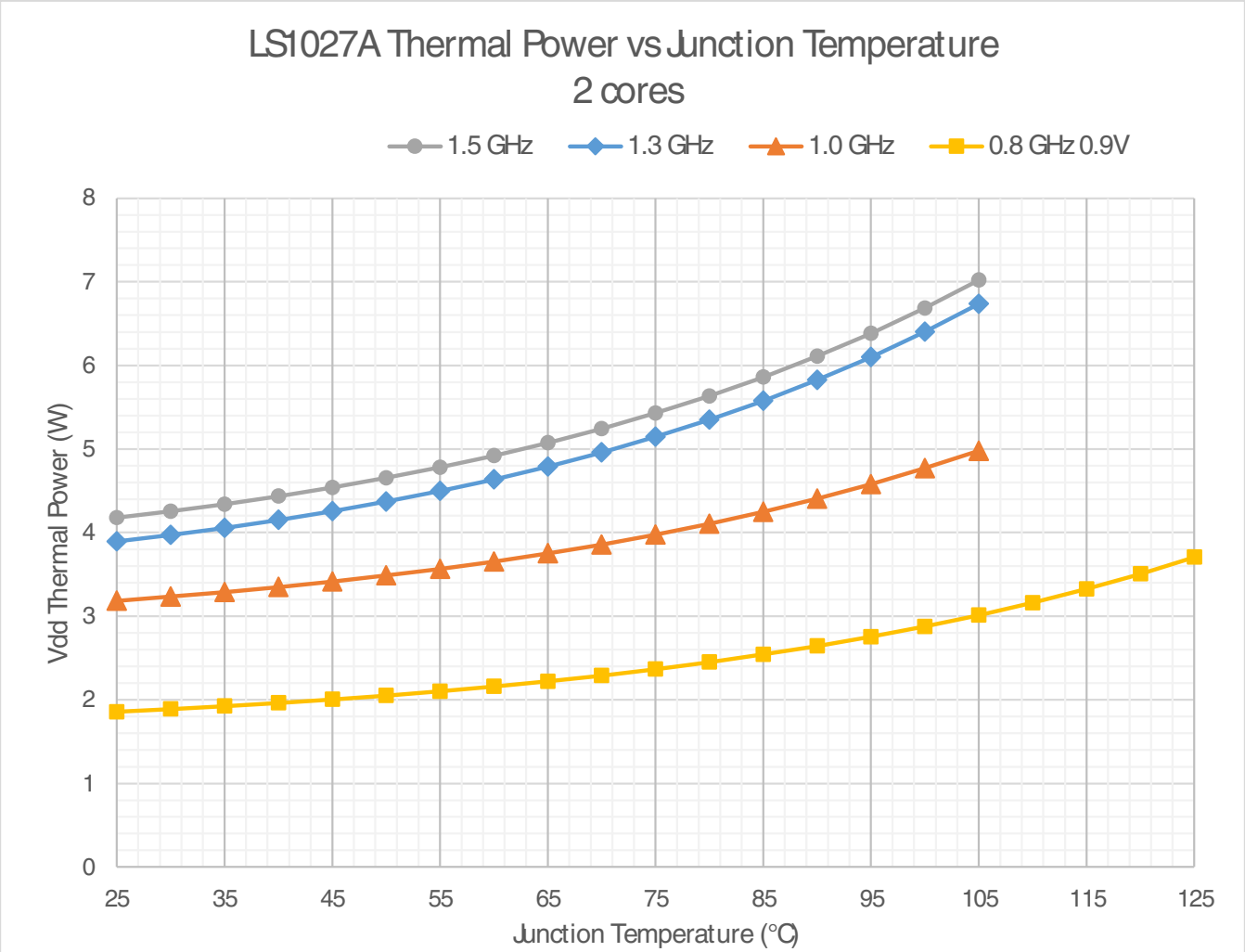

Figure 7. LS1027A Thermal VDD Power vs Junction Temperature

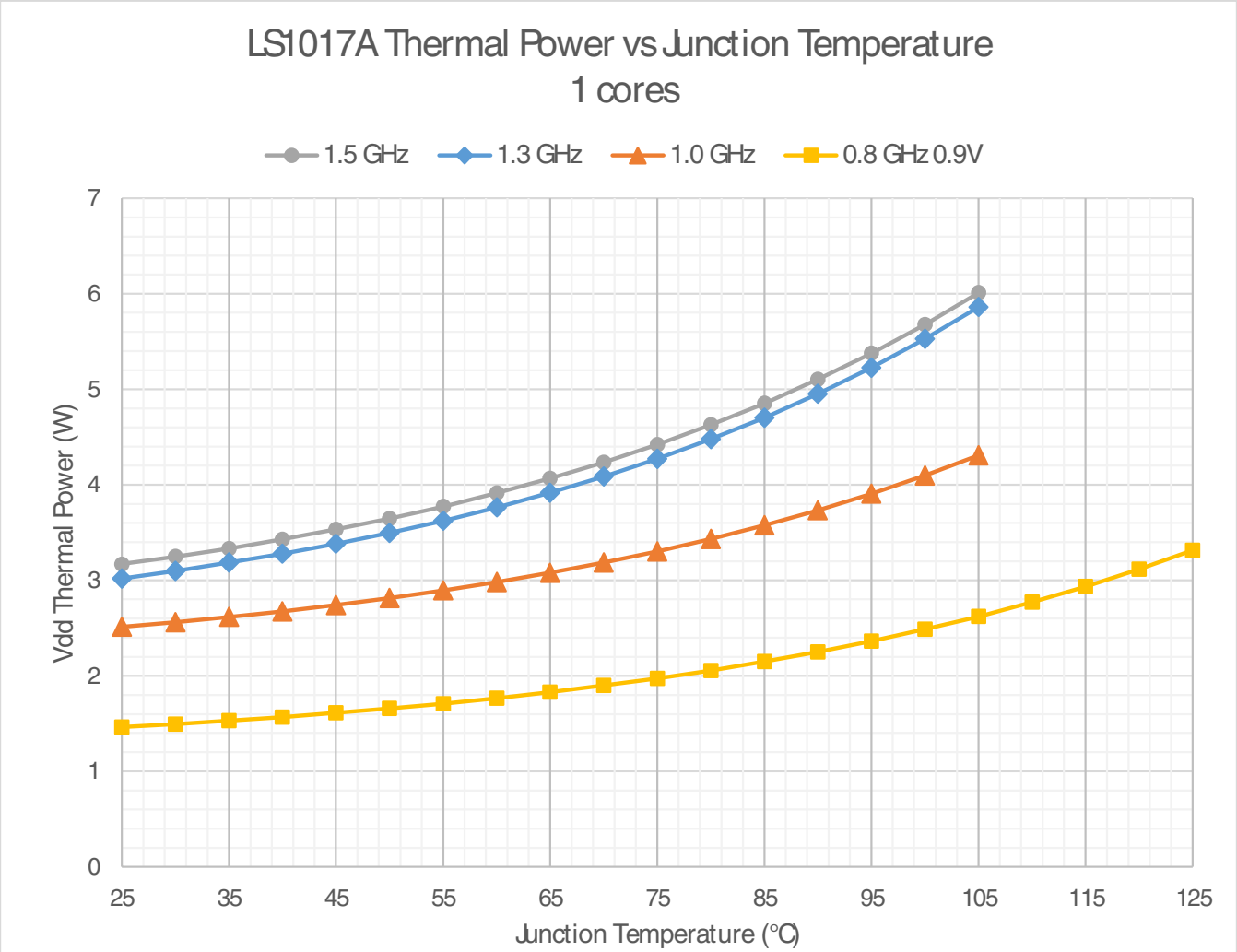

Figure 8. LS1017A Thermal VDD Power vs Junction Temperature

Table 4. I/O Thermal Power Dissipation at 105°C

Interface	I/O Power Supplies	Parameters	Thermal Power	Unit	Notes
DDRC (32-bit) I/O	G1VDD 1.35V	1600 MT/s	630	mW	1
DDRC (32-bit) I/O	G1VDD 1.2V	1600 MT/s	600	mW	1
Notes:					
1. Thermal DDR power numbers are based on one 2-rank DIMM with 40% utilization.					

4.3 Maximum VDD Power and IO Power

The power is measured when the device runs at the following speed combinations. In the graph, the speed is labeled with A72 speed only for the simpilicity.

Table 5. LS1028A/LS1018A/LS1027A/LS1017A Speed Combination

Core frequency (MHz)	Platform frequency(MHz)	DDR data rate (MT/s)	GPU and LCD controller frequency (MHz)[1]
1500	400	1600	700
1300	400	1600	650
1000	400	1600	500
800	300	1300	400

NOTE: 1. Only applicable for LS1028A and LS1018A only.

The following graphs provides the maximum VDD power for LS1028A, LS1018A, LS1027A and LS1017A. Maximum power are based on worst-case processed device. It assumes Dhrystone running with activity factor at 100% (on all cores) and worst case activity on the platform. The maximum power is used for the regulator design sizing. The maximum VDD power shown is expected to be sufficient for most applications.

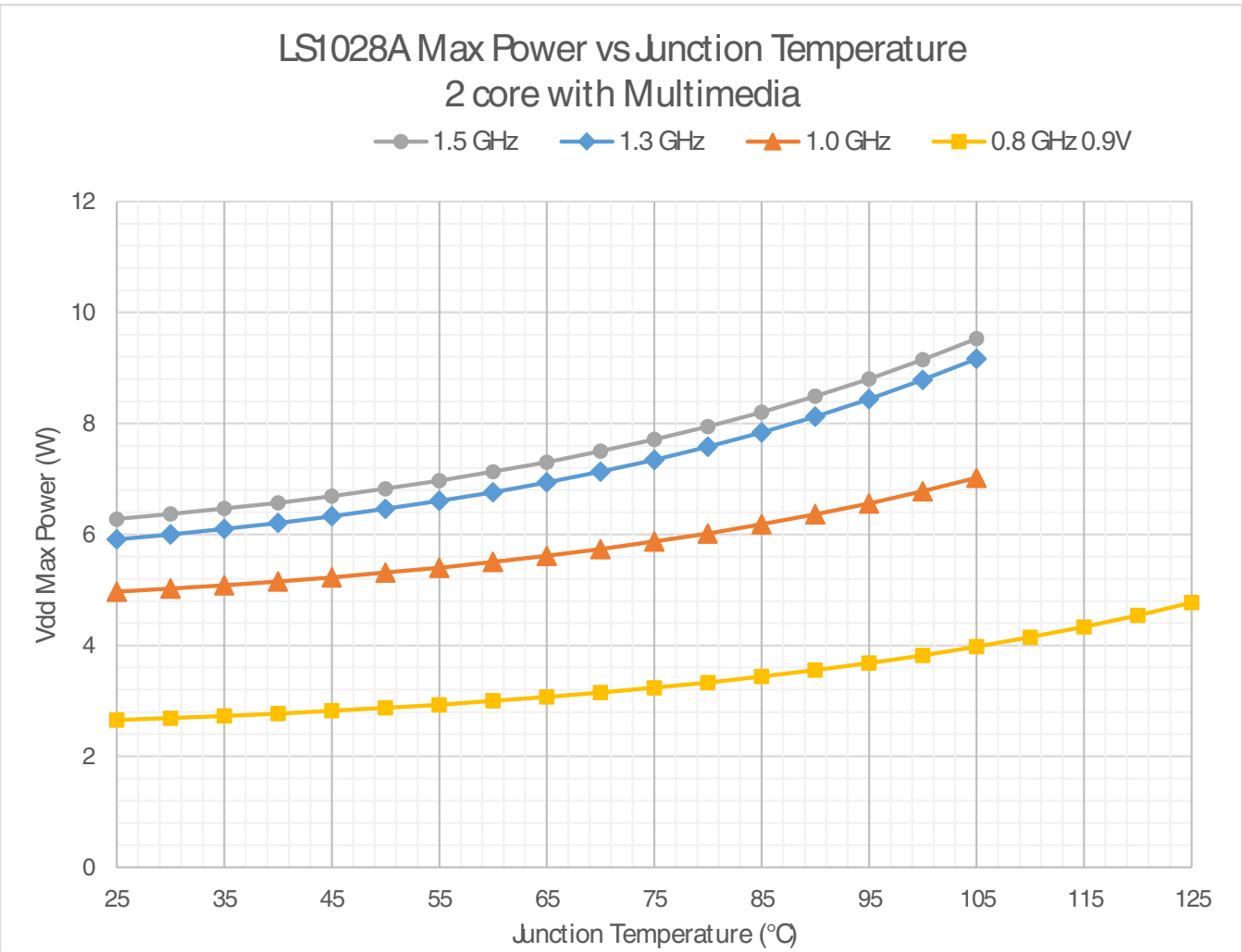

Figure 9. LS1028A Maximum VDD Power vs Junction Temperature

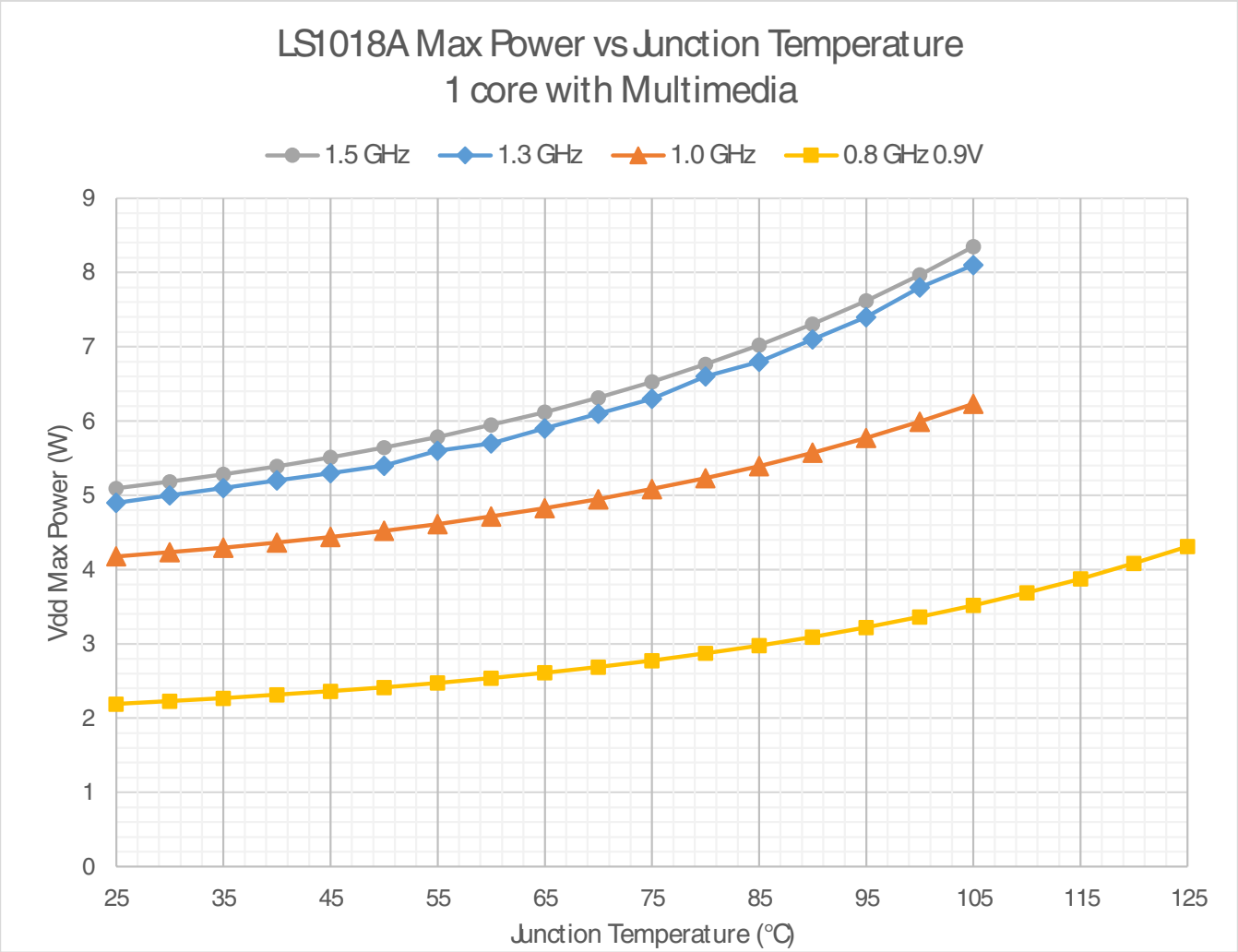

Figure 10. LS1018A Maximum VDD Power vs Junction Temperature

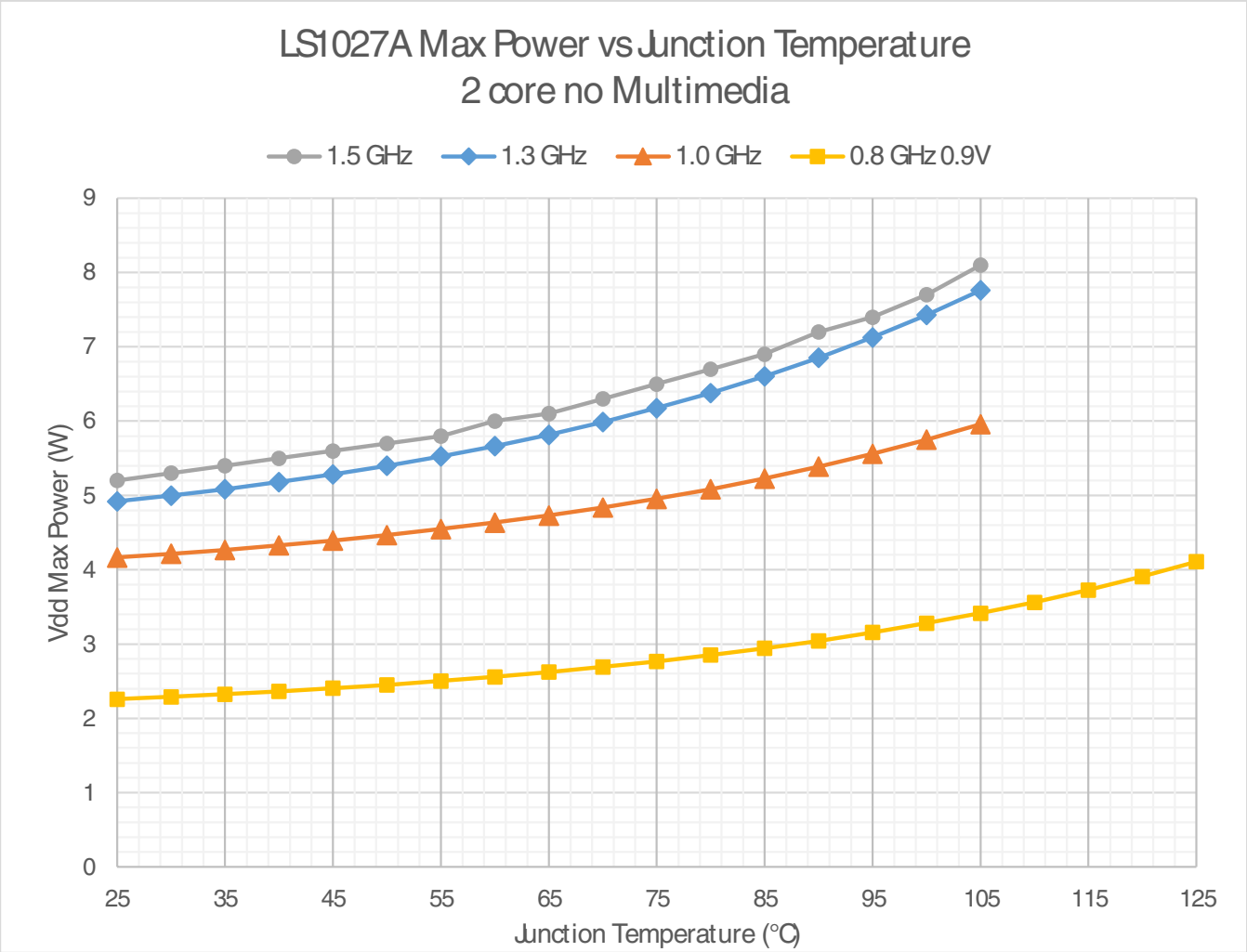

Figure 11. LS1027A Maximum VDD Power vs Junction Temperature

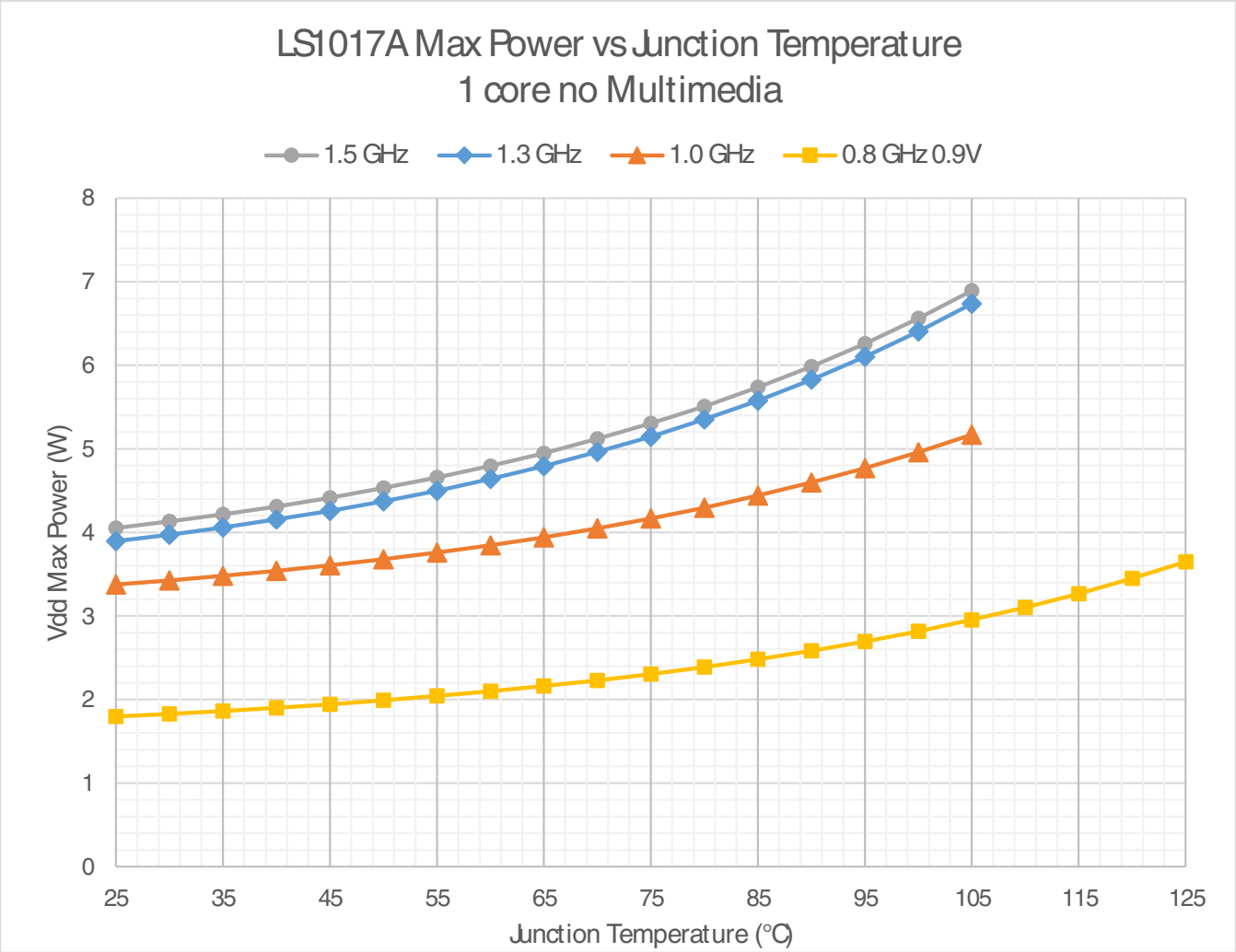

Figure 12. LS1017A Maximum VDD Power vs Junction Temperature

The following table shows the estimated maximum power on the I/O power supplies and the AV_{DD} and AV_{DD}_SD*n*_PLL*n* supplies for the chip's PLLs at allowable voltage levels.

Table 6. IO power supply estimated values

Interface	I/O Power Supplies	Parameters	Maximum Power	Unit	Notes
GPIO	OVDD 1.8V	x8	3	mW	1
Pixel clock PLL analog supply	AVDD_PIXEL 1.8V		9	mW	1
Pixel clock PLL digital supply	PIXEL_DVDD 1.0V		10	mW	1
eDP PHY	DP_OVDD 1.8V	DP(5.4Gbps)	9.2	mW	1
	DP_SVDD & DP_AVDD 1.0V		100	mW	1
	DP_OVDD 1.8V	eDP(5.4Gbps)	9.2	mW	1
	DP_SVDD & DP_AVDD 1.0V		83	mW	1

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Table 6. IO power supply estimated values (continued)

Interface	I/O Power Supplies	Parameters	Maximum Power	Unit	Notes
System Control	OVDD 1.8V		16	mW	1
Flextimer	OVDD 1.8V		18	mW	1
JTAG + DFT	OVDD 1.8V		10	mW	1
CAN	OVDD 1.8V		4	mW	1
EC1	OVDD 1.8V	RGMII	17	mW	1
EMI	OVDD 1.8V		2	mW	1
SAI	OVDD 1.8V		34	mW	1
TA_PROG_SFP	PROG_SFP		173	mW	1
TH_VDD	TH_VDD	1.8V	18	mW	1
IEEE1588	OVDD 1.8V		10	mW	1
FlexSPI	OVDD 1.8V	.	33	mW	1
DSPI	OVDD 1.8V	.	29	mW	1
eSDHC1	EVDD 1.8V	.	31	mW	1
eSDHC1	EVDD 3.3V	.	19	mW	1
eSDHC2	OVDD 1.8V	.	64	mW	1
I2C	OVDD 1.8 V	—	4	mW	1
DUART	OVDD 1.8 V	—	5	mW	1
DDRC (32-bit) I/O	G1VDD 1.35 V	1600 MT/s	1250	mW	1, 2
DDRC (32-bit) I/O	G1VDD 1.2 V	1600 MT/s	1100	mW	1, 2
USB PHY	USB_HVDD	1 x Super Speed port	51	mW	1, 4
	USB_SDVDD		0.1	mW	
(per PHY)	USB_SVDD		50	mW	
USB PHY	USB_HVDD	1 x High Speed port	87	mW	
	USB_SDVDD		5.5	mW	
(per PHY)	USB_SVDD		1	mW	
SerDes, 1.35 XVDD, 1.0 V SVDD	SVDD 1.0 V	Fi = Lane data rate in Gbps N = Total number of lanes used ni = number of lanes running at Fi rate	P_ SVDD = 155.047 + 16.766 * N + 3.287 * (Sum(ni * Fi)) ± 15 mW	mW	5
SerDes, 1.35 XVDD, 1.0 V SVDD	XVDD 1.35 V	Fi = Lane data rate in Gbps N = Total number of lanes used ni = number of lanes running at Fi rate	P_ XVDD = 53.256 + 50.685 * N + 0.683 * (Sum(ni * Fi)) ± 15 mW	mW	5
PLL Supply (core, platform, DDR)	AVDD_CGA1, AVDD_CGA2, AVDD_PLAT, AVDD_D1 (1.8V)	—	32 for each	mW	1

Table continues on the next page...

Table 6. IO power supply estimated values (continued)

Interface	I/O Power Supplies	Parameters	Maximum Power	Unit	Notes
PLL Supply (SerDes)	AVDD_SD1_PLL1, AVDD_SD1_PLL2 (1.35 V)	—	28 for each	mW	1

Notes:

1. The maximum values are dependent on actual use case such as what application, external components used, environmental conditions such as temperature, voltage and frequency. This is not intended to be the maximum guaranteed power. Expect different results depending on the use case. The maximum values are estimated and they are based on simulations at 105°C junction temperature.

2. Maximum DDR power numbers are based on one 2-rank DIMM with 100% utilization.

3. The total power numbers of XVDD is dependent on customer application use case. This table lists some typical SerDes configurations for the device. To get the XVDD power numbers, the user should add the combined lanes to match to the total SerDes Lanes used, not simply multiply the power numbers by the number of lanes.

4. USB Power supply pins are shared between two USB controllers

5. The total power numbers of XVDD and SVDD depend on the customer's application usecase. Power formulas assume 105° C junction temperature. If one PLL is used, then subtract 26 mW from the resulting P_ SVDD. The following examples show how to use the formulas in estimating P_ SVDD and P_ XVDD for different SerDes usecases.

Example 1: Worst case: SERDES (0x13CC) 10G SXGMII+ 10G-QXGMII + PCIe x2 Gen3; the SerDes maximum powers are expected to be:

P_ SVDD = 155.047 + 16.766 * 4 + 3.287 *(2*10.3125 + 2*8) ± 15 mW = 343 mW ± 15 mW

P_ XVDD = 53.256 + 50.685 * 4 + 0.683 * (2*10.3125 + 2*8) ± 15 mW = 281 mW ± 15 mW

Example 2: On a SerDes block running PCIe at 8 Gbps on four lanes, the SerDes maximum powers are expected to be:

P_ SVDD = 155.047 + 16.766 * 4 + 3.287 * (4 * 8) ± 15 mW - (28 mW "because one PLL is used") = 299 ± 15 mW

P_ XVDD = 53.256 + 50.685 * 8 + 0.683 *(8 * 5) ± 15 mW = 278 mW ± 15 mW

4.4 Power number for Typical Use Case

The following tables are use case power for the LS1028A, LS1018A, LS1027A and LS1017A.

Table 7. Typical use case power at 65^0C

SoC	Core (MHz)	Platform (MHz)	DDR (MT/s)	GPU and LCD ontroller frequency (MHz)	VDD (V)	VDD power (W)	Notes
LS1028A	1500	400	1600	700	1.0	6.9	1,2
	1300	400	1600	650	1.0	6.6	1,2
	1000	400	1600	500	1.0	5.4	1,2
	800	300	1300	400	0.9	4.1	1,2
LS1018A	1500	400	1600	700	1.0	5.8	1,3
	1300	400	1600	650	1.0	5.7	1,3

Table continues on the next page...

Table 7. Typical use case power at 65^{0}C (continued)

SoC	Core (MHz)	Platform (MHz)	DDR (MT/s)	GPU and LCD ontroller frequency (MHz)	VDD (V)	VDD power (W)	Notes
	1000	400	1600	500	1.0	4.8	1,3
	800	300	1300	400	0.9	3.6	1,3
LS1027A	1500	400	1600	NA	1.0	5.7	1,2
	1300	400	1600	NA	1.0	5.4	1,2
	1000	400	1600	NA	1.0	4.4	1,2
	800	300	1300	NA	0.9	3.5	1,2
LS1017A	1500	400	1600	NA	1.0	4.7	1,3
	1300	400	1600	NA	1.0	4.6	1,3
	1000	400	1600	NA	1.0	3.7	1,3
	800	300	1300	NA	0.9	2.9	1,3

Notes:

1. Nominal processed device.
2. Typical power assumes Dhrystone running with activity factor of 80% (on all cores) and executing DMA on the platform at 100% activity factor.
3. Typical power assumes Dhrystone running with activity factor of 90% on core and executing DMA on the platform at 100% activity factor.

4.5 Power system-level recommendations

Table 8. Power design system-level checklist

Item	Completed
General	
Ensure to meet all of the requirements in the data sheet, including power sequencing, power down requirements, THERMAL and MAXIMUM power dissipation, I/O power dissipation, and power on ramp rate.	
Ensure the PLL filter circuit is applied to AV_{DD}_PLAT, AV_{DD}_CGA1, AV_{DD}_CGA2, AV_{DD}_D1. See the "PLL power supply filtering" section of this table.	
If SerDes is enabled, ensure the PLL filter circuit is applied to the respective AV_{DD}_SD*m*_PLL*n* pins. Otherwise, a filter is not required. Even if an entire SerDes module is not used, the power is still needed to the AV_{DD} pins. However, instead of using a filter, it needs to be connected to the XV_{DD} rail through a 0 Ω resistor. See the "PLL power supply filtering" section of this table.	
Ensure the PLL filter circuits are placed as close to the respective AV_{DD}_SD*m*_PLL*n* pin as possible. If possible, a small cap for the filter should be placed directly at the pin. If no small cap for the filter is available, consider at least a standard decoupling cap, such as 0.1 µF.	
General Power supply decoupling	
Because of large address and data buses and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the system, and the device itself, so this requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer	

Table continues on the next page...

Table 8. Power design system-level checklist (continued)

Item	Completed
place at least one decoupling capacitor at each V_{DD}, TA_BB_V_{DD}, OV_{DD}, EV_{DD}, $G1V_{DD}$, SV_{DD}, and XV_{DD} pin of the device. These decoupling capacitors should receive their power from separate V_{DD}, TA_BB_V_{DD}, OV_{DD}, EV_{DD}, $G1V_{DD}$, SV_{DD}, XV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part. These capacitors typically should have a value of approximately 0.1 µF. However, larger values available in the given package, such as 10 µF for 0402 (supports 1.0 mm pitched parts) or 4.7 µF for 0201 (supports 0.8 mm pitched parts), may be used to provide both decoupling and intermediate capacitance for the power supply design. For example, a system may have 0.1 µF at the pin, but also needs 22 µF intermediate capacitance outside the package. Given routing escape density, it may be more beneficial to remove the 22 µF caps and replace the 0.1 µF with 4.7 µF to 10 µF 0201/0402. Thus, it allows more room for routing to escape as an option. It is best to have one decoupling capacitor at each pin location. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes for 1 mm pitched parts and 0201 for 0.8 mm pitched parts. As presented in the "Core and platform supply voltage filtering" section of this table, it is recommended that there be several medium and large sized bulk storage capacitors distributed around the PCB, feeding the V_{DD} and other planes (for example, EV_{DD}, $G1V_{DD}$, and so on), to enable quick recharging of the smaller chip capacitors.	
Provide sufficiently-sized power planes for the respective power rail. Use separate planes if possible; split (shared) planes if necessary. If split planes are used, ensure that signals on adjacent layers do not cross splits. Avoid splitting ground planes at all costs.	
Ensure the bulk capacitors have a low ESR rating to ensure the quick response time necessary.	
Ensure the bulk capacitors are connected to the power and ground planes through two vias, as necessary, to minimize inductance.	
Ensure you work directly with your power regulator vendor for best values and types of bulk capacitors. The capacitors need to be selected to work well with the power supply to be able to handle the chip's power requirements. Most regulators perform best with a mix of ceramic and other low ESR types, such as OSCON, POS, and other types of capacitor technologies.	
Core and platform supply voltage filtering	
The V_{DD} supply is normally derived from a high current switching power supply, which can regulate its output voltage very accurately despite changes in current demand from the chip within the regulator's relatively low bandwidth. Several bulk capacitors must be distributed around the PCB to supply transient current demand above the bandwidth of the voltage regulator. Bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the necessary response time. They should also be connected to the power and ground planes through two vias at each side, if necessary, to minimize inductance. However, customers should work directly with their power regulator vendor for best values and types of bulk capacitors. Most power supply designs work well with small ceramic caps at each pin, as discussed in the "General power supply decoupling" section of this table. But also nearby the SoC should be intermediate caps, such as 22 µF ceramic and larger 330 to 560 µF POS type caps, as an example. As a guideline for customers and their power regulator vendors, NXP recommends that these bulk capacitors should be chosen to maintain the positive transient power surges to less than V_{DD} + 50 mV (negative transient undershoot should comply with specification of VDD - 30 mV) for current steps of up to 50% to 100% rise and 100% to 50% of max current (based on maximum power in the data sheet) with a slew rate of 7 A/us. These bulk decoupling capacitors will ideally supply a stable voltage for current transients into the MHz range. See the "General power supply decoupling" section of this table for further decoupling recommendations.	
PLL supply filtering (core, platform, DDR, filtered from 1.8 V source)	
All PLLs are provided with power through independent power supply pins (AV_{DD}_PLAT, AV_{DD}_CGA1/2, and AV_{DD}_D1 voltages must be derived directly from a 1.8 V voltage source, such as OV_{DD}, through a low frequency filter. The recommended solution for this type of PLL filtering is to provide independent filter circuits per PLL power supply, one for each of the AV_{DD} pins. By providing independent filters to each PLL,	

Table continues on the next page...

Table 8. Power design system-level checklist (continued)

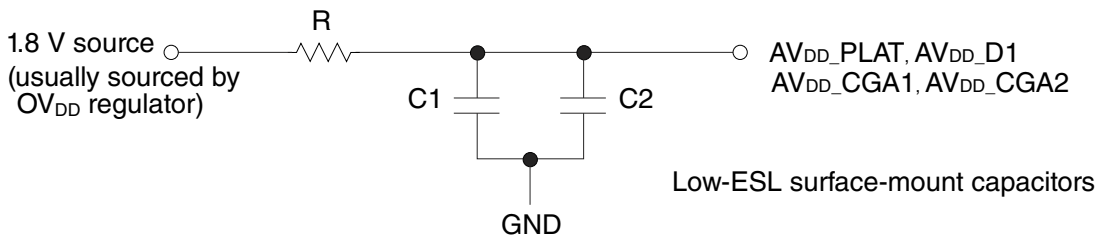
Item	Completed
the opportunity to cause noise injection from one PLL to the other is reduced. This circuit is intended to filter noise in the PLL's resonant frequency range from a 500 kHz to 10 MHz range. Provide independent filter circuits per PLL power supply, as illustrated in the following figure. Where • R = 5 Ω ± 5% • C1 = 10 µF ± 10%, 0603 or smaller, X5R or better (X7R or C0G are fine), with ESL ≤ 0.5 nH • C2 = 1.0 µF ± 10%, 0402 or 0201, X5R, with ESL ≤ 0.5 nH • Low-ESL surface-mount capacitors  Note the following: • Each AV_{DD} pin must have its own independent filter circuit. • Voltage for AV_{DD} is defined at the input of the PLL supply filter and not the pin of AV_{DD}. • If done properly, it is possible to route directly from the capacitors to the AV_{DD} pins, without the added inductance of vias. • It is recommended that an area fill or power plane split be provided for a low-impedance profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Place each circuit as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. • Placement should be such that the smaller capacitors are nearest to the AV_{DD} pin. If routing permits, the smallest cap would be best located at the pin of AV_{DD}. • **Caution:** These filters are a necessary extension of the PLL circuitry and are compliant with the device specifications. Any deviation from the recommended filters is done at the user's risk.	
PLL supply filtering (SerDes, filtered from XV_{DD})	
The AV_{DD}_SD*m*_PLL*n* signals provide power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, ensure the power supplied to the PLL is filtered using a circuit similar to the one shown in the following figure. The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, one for each side of the AV_{DD} pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced. Note the following: • Each AV_{DD} must have its own independent filter circuit. • AV_{DD}_SD*m*_PLL*n* should be a filtered version of XV_{DD}. • Voltage for AV_{DD} is defined at the pin of AV_{DD}. This is in contrast to the requirement, for example for the core PLL filter such as AV_{DD}_CGA*n*, which is measured at the input of the filter. • Placement should be such that the smaller capacitors are nearest to the AV_{DD} pin. If routing permits, the smallest cap would be best located at the pin of AV_{DD}. • It is recommended that an area fill or power plane split be provided for a low-impedance profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • A 47 µF 0805 XR5 or XR7, 4.7 µF 0603 or smaller, and 0.0033 µF 0402 or 0.0033 µF 0201 capacitor are recommended. The size and material type are important. A 0.33 Ω ± 1% resistor is recommended. • **Caution**: These filters are a necessary extension of the PLL circuitry and are compliant with the device specifications. Any deviation from the recommended filters is done at the user's risk.	

Table continues on the next page...

Table 8. Power design system-level checklist (continued)

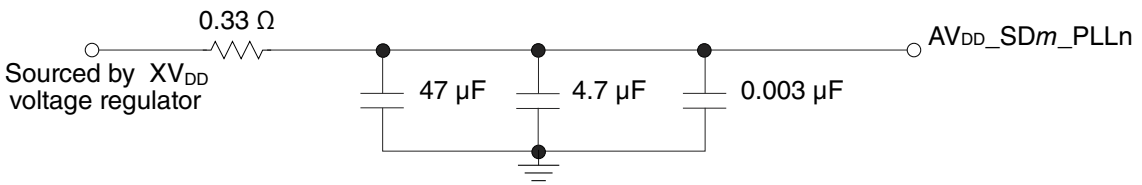
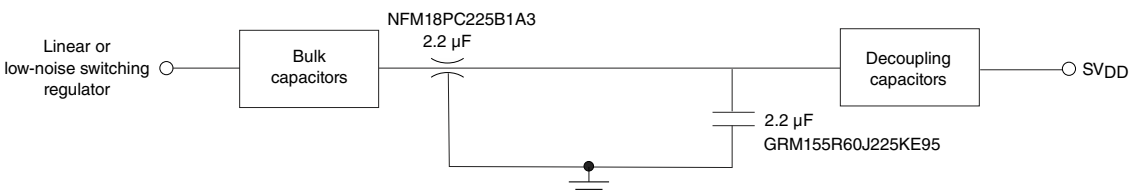
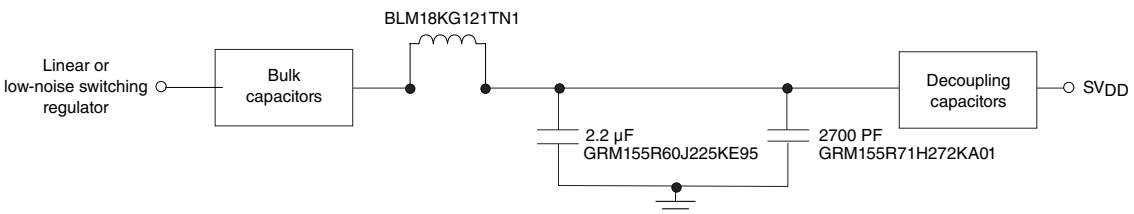
Item	Completed
	
SerDes power supply filtering	
The ferrite beads should be placed in parallel to reduce voltage droop. For the linear or low-noise switching regulator, 10 mVp-p, 50 kHz to 500 MHz is the noise goal. All traces should be kept short, wide, and direct. Use small area fill, if possible. The goal is to lower the impedance of this net, thus lowering the noise. SV_{DD} may be supplied by linear or low noise switching regulator or sourced by a filtered V_{DD}. Two example solutions for SV_{DD} filtering, where SV_{DD} is sourced from linear or low noise switching regulator, are illustrated in Figure 13 and Figure 14. Users can choose either one as they see best fit their needs, but the primary NFM type filter has two advantages: lower DC droop and easier layout than the ferrite bead solution.  **Figure 13. Primary SV_{DD} power supply filter circuit**  **Figure 14. Alternate SV_{DD} power supply filter circuit** Note the following: • See "Power-on ramp rate," in the data sheet for maximum SV_{DD} power-up ramp rate. • It is recommended that an area fill or power plane split be provided for a low-impedence profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Place each circuit as close as possible to the specific set of pins being supplied to minimize noise coupled from nearby circuits. • Located at each pin should have a decouple capacitor, such as 0.1 µF.	
XV_{DD} may be supplied by a linear or low noise switching regulator or sourced by a filtered G1VDD. Two example solutions for XV_{DD} filtering, where XV_{DD} is sourced from a linear or low noise switching regulator, are illustrated in Figure 15 and Figure 16. Users can choose either one as they see best fit their needs, but the primary NFM type filter has two advantages: lower DC droop and easier layout than the ferrite bead solution	

Table continues on the next page...

Table 8. Power design system-level checklist (continued)

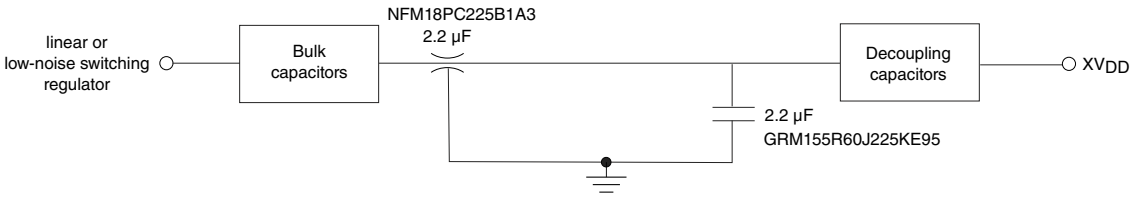
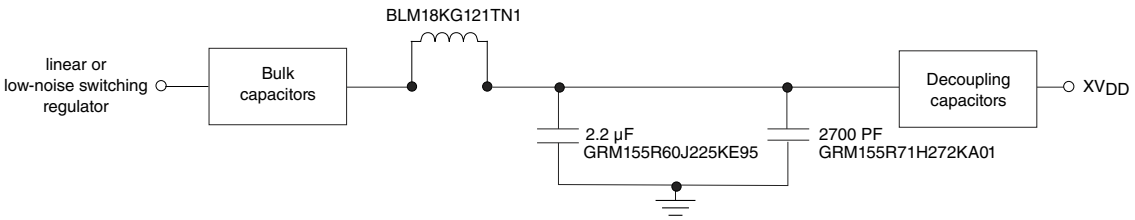
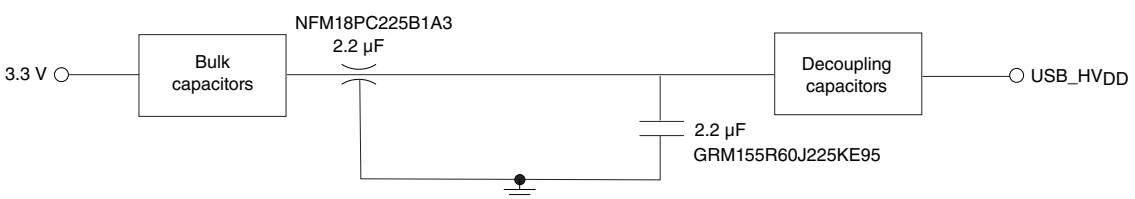
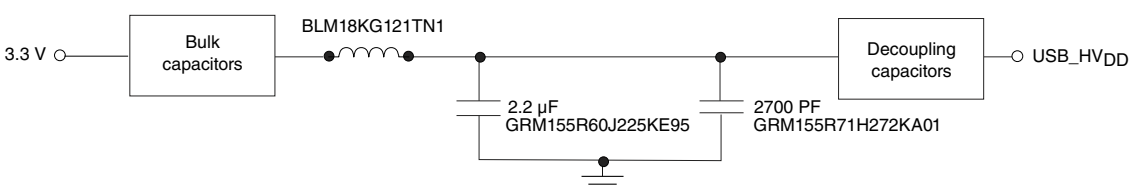
Item	Completed
 **Figure 15. Primary XV_{DD} power supply filter circuit**  **Figure 16. Alternte XV_{DD} power supply filter circuit** Note the following: • See "Power-on ramp rate," in the data sheet for maximum XV_{DD} power-up ramp rate. • It is recommended that an area fill or power plane split be provided for a low-impedance profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Place each circuit as close as possible to the specific set of pins being supplied to minimize noise coupled from nearby circuits. • Located at each pin should have a decouple capacitor, such as 0.1 µF.	
USB_HV_{DD} may be supplied by a linear or low noise switching regulator, which may be the system-wide 3.3 V power supply. Two example solutions for USB_HV_{DD} filtering, where USB_HV_{DD} is sourced from a linear or low noise switching regulator, are illustrated in Figure 17 and Figure 18. Users can choose either one as they see best fit their needs, but the primary NFM type filter has two advantages: lower DC droop and easier layout than the ferrite bead solution.  **Figure 17. Primary USB_HV_{DD} power supply filter circuit**  **Figure 18. Alternate USB_HV_{DD} power supply filter circuit**	

Table continues on the next page...

Table 8. Power design system-level checklist (continued)

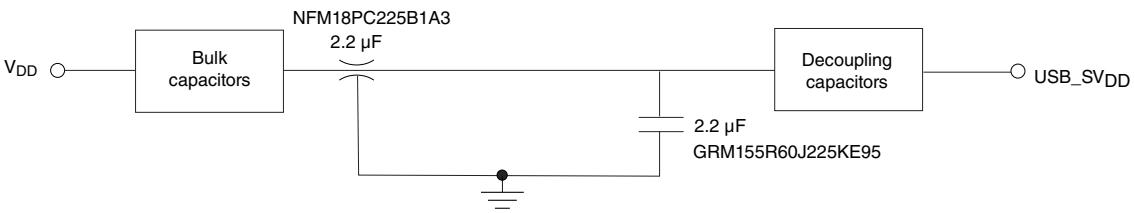
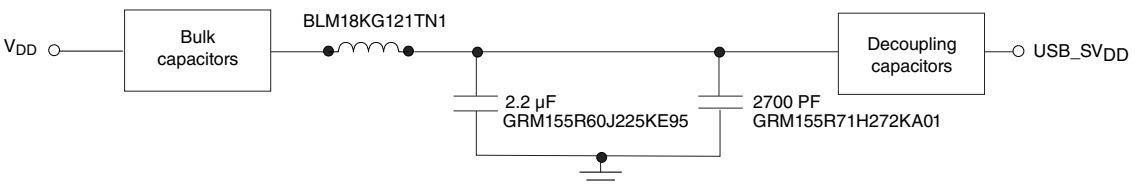
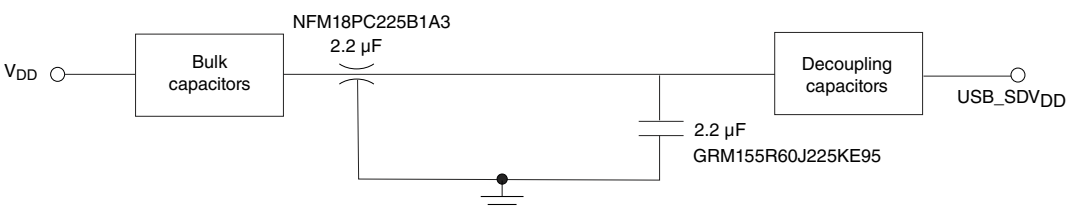
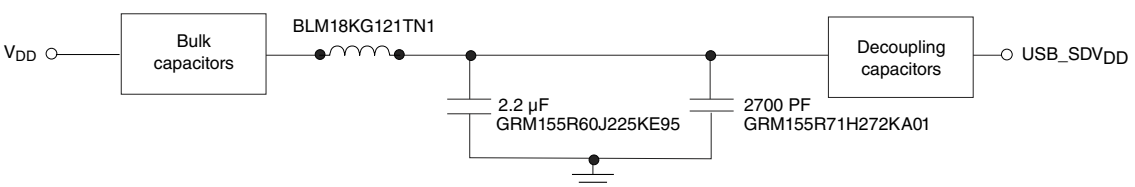
Item	Completed
Note the following: • It is recommended that an area fill or power plane split be provided for a low-impedence profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Place each circuit as close as possible to the specific set of pins being supplied to minimize noise coupled from nearby circuits. • Located at each pin should have a decouple capacitor, such as 0.1 µF.	
USB_SV_{DD} and USB_SDV_{DD} are to be filtered from the V_{DD} power supply. Two example solutions for USB_SV_{DD} and USB_SDV_{DD} filtering, where USB_SV_{DD} and USB_SDV_{DD} are sourced from a filtered version of V_{DD}, are illustrated in Figure 19, Figure 20, Figure 21 and Figure 22. Users can choose either one as they see best fit their needs, but the primary NFM type filter has two advantages: lower DC droop and easier layout than the ferrite bead solution.  **Figure 19. Primary USB_SV_{DD} power supply filter circuit**  **Figure 20. Alternate USB_SV_{DD} power supply filter circuit**  **Figure 21. Primary USB_SDV_{DD} power supply filter circuit**  **Figure 22. Alternate USB_SDV_{DD} power supply filter circuit** Note the following:	

Table continues on the next page...

Table 8. Power design system-level checklist (continued)

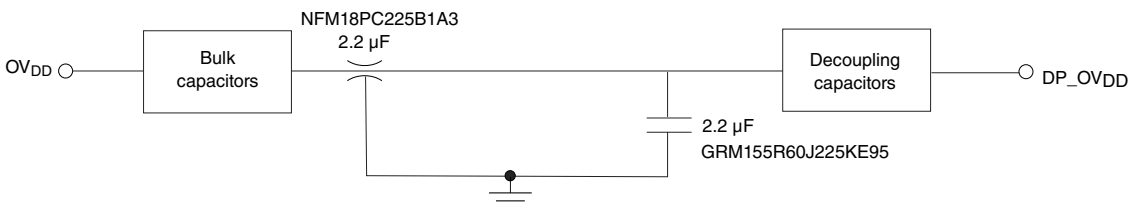
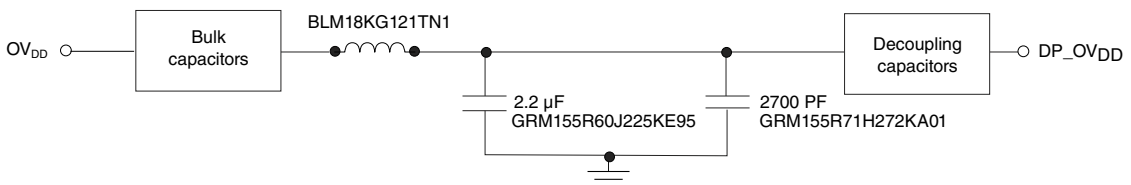
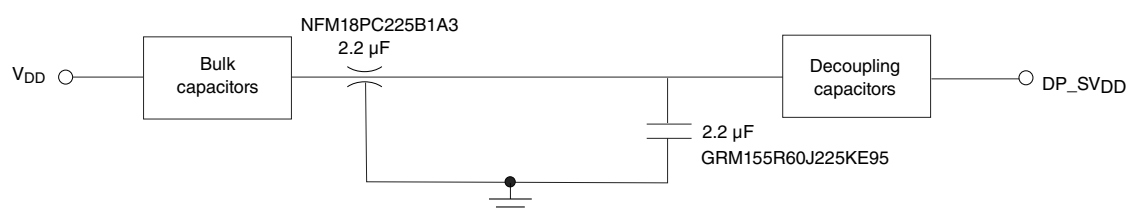
Item	Completed
• It is recommended that an area fill or power plane split be provided for a low-impedence profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Place each circuit as close as possible to the specific set of pins being supplied to minimize noise coupled from nearby circuits. • Located at each pin should have a decouple capacitor, such as 0.1 µF.	
DP_OV_{DD} may be supplied by a linear or low noise switching regulator, which may be the system-wide 1.8 V power supply. Two example solutions for DP_OV_{DD} filtering, where DP_OV_{DD} is sourced from a linear or low noise switching regulator, are illustrated in Figure 23 and Figure 24. Users can choose either one as they see best fit their needs, but the primary NFM type filter has two advantages: lower DC droop and easier layout than the ferrite bead solution.  **Figure 23. Primary DP_OV_{DD} power supply filter circuit**  **Figure 24. Alternate DP_OV_{DD} power supply filter circuit** Note the following: • It is recommended that an area fill or power plane split be provided for a low-impedence profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Place each circuit as close as possible to the specific set of pins being supplied to minimize noise coupled from nearby circuits. • Located at each pin should have a decouple capacitor, such as 0.1 µF.	
DP_SV_{DD} is to be filtered from the V_{DD} power supply. Two example solutions for DP_SV_{DD} filtering, where DP_SV_{DD} is sourced from a filtered version of V_{DD}, are illustrated in Figure 25 and Figure 26. Users can choose either one as they see best fit their needs, but the primary NFM type filter has two advantages: lower DC droop and easier layout than the ferrite bead solution.  **Figure 25. Primary DP_SV_{DD} power supply filter circuit**	

Table continues on the next page...

Table 8. Power design system-level checklist (continued)

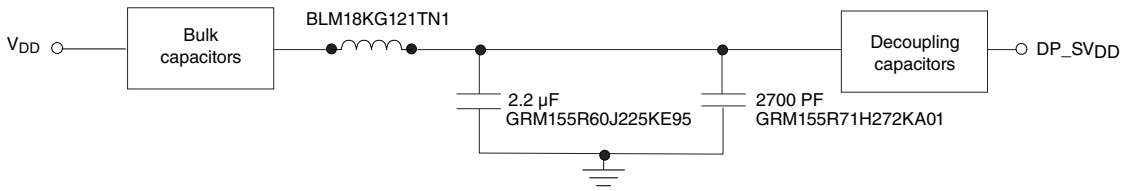
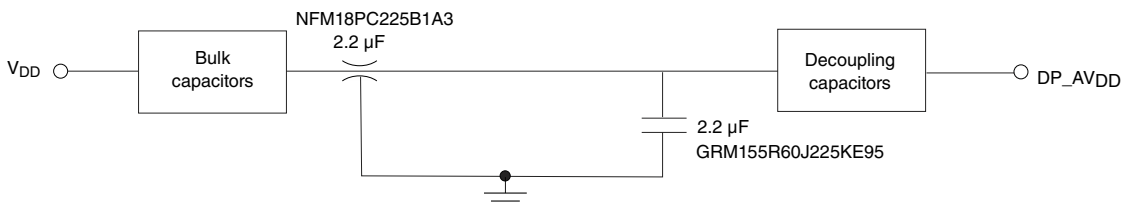
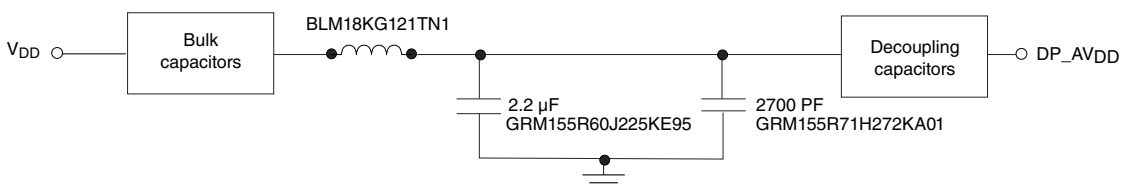
Item	Completed
 **Figure 26. Alternate DP_SV_{DD} power supply filter circuit** Note the following: • It is recommended that an area fill or power plane split be provided for a low-impedence profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Place each circuit as close as possible to the specific set of pins being supplied to minimize noise coupled from nearby circuits. • Located at each pin should have a decouple capacitor, such as 0.1 µF.	
DP_AV_{DD} is to be filtered from the V_{DD} power supply. Two example solutions for DP_AV_{DD} filtering, where DP_AV_{DD} is sourced from a filtered version of V_{DD}, are illustrated in Figure 27 and Figure 28. Users can choose either one as they see best fit their needs, but the primary NFM type filter has two advantages: lower DC droop and easier layout than the ferrite bead solution.  **Figure 27. Primary DP_AV_{DD} power supply filter circuit**  **Figure 28. Alternate DP_AV_{DD} power supply filter circuit** Note the following: • It is recommended that an area fill or power plane split be provided for a low-impedence profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Place each circuit as close as possible to the specific set of pins being supplied to minimize noise coupled from nearby circuits. • Located at each pin should have a decouple capacitor, such as 0.1 µF.	
AV_{DD}_PIXEL may be supplied by a linear or low noise switching regulator, which may be the system-wide 1.8 V power supply. Example solution for AV_{DD}_PIXEL filtering, where AV_{DD}_PIXEL is sourced from a filtered version of OV_{DD}, is illustrated in Figure 29.	

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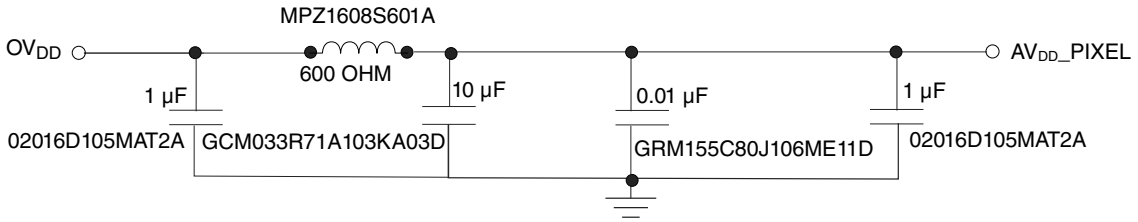
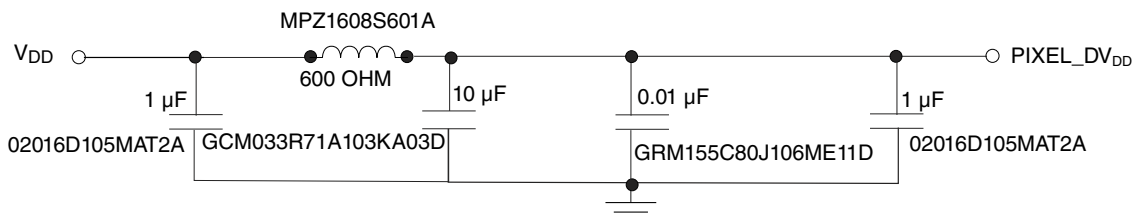
Table 8. Power design system-level checklist (continued)

Item	Completed
 **Figure 29. AV_{DD}_PIXEL power supply filter circuit** Note the following: • It is recommended that an area fill or power plane split be provided for a low-impedence profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Place each circuit as close as possible to the specific set of pins being supplied to minimize noise coupled from nearby circuits. • Located at each pin should have a decouple capacitor, such as 0.1 µF.	
PIXEL_DV_{DD} is to be filtered from the V_{DD} power supply. Example solutions for PIXEL_DV_{DD} filtering, where PIXEL_DV_{DD} is sourced from a filtered version of V_{DD}, are illustrated in Figure 30.  **Figure 30. PIXEL_DV_{DD} power supply filter circuit** Note the following: • It is recommended that an area fill or power plane split be provided for a low-impedence profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Place each circuit as close as possible to the specific set of pins being supplied to minimize noise coupled from nearby circuits. • Located at each pin should have a decouple capacitor, such as 0.1 µF.	

4.6 Power-on reset recommendations

Various chip functions are initialized by sampling certain signals during the assertion of PORESET_B. These power-on reset (POR) inputs are pulled either high or low during this period. While these pins are generally output pins during normal operation, they are treated as inputs while PORESET_B is asserted. When PORESET_B de-asserts, the configuration pins are sampled and latched into registers, and the pins then take on their normal output circuit characteristics.

Table 9. Power-on reset system-level checklist

Item	Completed
Ensure PORESET_B is asserted for a minimum of 1 ms after V_{DD} ramps up.	
Due to Gen A-050124, HRESET_B cannot be used to reset the chip. However the signal can be used as output if required.	
In cases where a configuration pin has no default, use a 4.7 kΩ pull-up or pull-down resistor for appropriate configuration of the pin.	
Optional: An alternative to using pull-up and pull-down resistors to configure the POR pins is to use a PLD or similar device that drives the configuration signals to the chip when PORESET_B is asserted. The PLD must begin to drive these signals at least four SYSCLK cycles prior to the de-assertion of PORESET_B, hold their values for at least two SYSCLK cycles after the de-assertion of PORESET_B, and then release the pins to high impedance afterward for normal device operation **NOTE:** See the applicable chip data sheet for details about reset initialization timing specifications.	
Configuration settings	
Ensure the settings in the Configuration Signals Sampled at Reset chapter of the reference manual are selected properly. **NOTE:** See the applicable chip reference manual for a more detailed description of each configuration option.	

4.6.1 Configuration signals sampled at reset

The signals that serve alternate functions as configuration input signals during system reset are summarized in this table.

Reset configuration signals are sampled at the negation of PORESET_B. However, there is a setup and hold time for these signals relative to the rising edge of PORESET_B, as described in the *QorlQ LS1028A Data Sheet* (document LS1028A).

The reset configuration signals are multiplexed with other functional signals. The values on these signals during reset are interpreted to be logic one or zero, regardless of whether the functional signal name is defined as active-low. The reset configuration signals have internal pull-up resistors so that if the signals are not driven, the default value is high (a one), as shown in the table below. Some signals must be driven high or low during the reset period. For details about all the signals that require external pull-up resistors, see the applicable device data sheet.

Following pins must NOT be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any externally connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.

- XSPI1_A_CS1_B /GPIO2_DAT20 /FTM8_CH0 /cfg_svr1
- XSPI1_A_SCK /GPIO2_DAT22 /FTM8_CH2 /cfg_eng_use0
- RESET_REQ_B /GPIO2_DAT08

Table 10. LS1028A reset configuration signals

Configuration Type	Functional Pins	Comments
Reset configuration word (RCW) source inputs cfg_rcw_src[0:3]	UART2_SOUT, UART1_SOUT, ASLEEP, CLK_OUT	They must be set to one of the valid RCW source input option. The 1024-bit RCW data has all the necessary configuration information for the chip. If there is no valid RCW in the external memory, it can be programmed using the Code Warrior or other programmer. The JTAG configuration

Table continues on the next page...

Table 10. LS1028A reset configuration signals (continued)

Configuration Type	Functional Pins	Comments
		files (CWInstallDir \CW4NET_v2019.01\CW_ARMv8\Config\) can be used in the following situations: • target boards that do not have RCW already programmed • new board bring up • recovering boards with blank or damaged flash
DRAM type select (cfg_dram_type)	EMI1_MDC	The reset configuration pin selects the proper IO voltage. • 1=DDR3L (1.35V) • 0=DDR4 (1.2 V)
General-purpose input (cfg_gpinput[0:3], cfg_gpinput[4:7])	SDHC1_DAT[0:3], SDHC2_DAT[0:3]	Default "1111 1111", values can be application defined
cfg_svr[0]	XSPI_A_CS0_B, XSPI_A_CS1_B	Keep pull up/down option on board. Table 2

4.6.2 Hard-coded RCW

The hard-coded RCW can be used as an alternative method for the initial board bring-up when there is no valid RCW in the external memory.

If a new board is using a blank flash and flash is the source of RCW, then all 0xff value from flash for RCW will put the device in an unknown state.

There are two methods to workaround this problem:

1. Put the switches on cfg_rcw_src signals to select hard-coded RCW (CFG_RCW_SRC[0:3] = 0x0/0x1/0x2/0x3).
2. Use the CodeWarrior tool from NXP to override RCW.

NOTE

- It is recommended to disconnect RESET_REQ_B from PORESET_B when using hard-coded RCW as any different board configuration may push the chip to an endless reset loop. For more information, see the hard-coded RCW options listed in *QorIQ LS1028A Reference Manual* (document LS1028ARM).

5 Interface recommendations

5.1 DDR controller recommendations

The memory interface controls main memory accesses. The LS1028A/LS1027A device supports 32-bit DDR3L (1.35 V) and DDR4 (1.2 V) SDRAM with ECC.

5.1.1 DDR controller pin termination recommendations

Table 11. DDR controller pin termination checklist

Signal name[1]		I/O type	Used	Not used	Completed
DDR3L signal	DDR4 signal				
D1_MA[13:0] D1_MA[14] D1_MA[15]	D1_MA[13:0] D1_MBG1 D1_MACT_B	O	Must be properly terminated to VTT	These pins can be left unconnected.	
D1_MBA[0:1] D1_MBA[2]	D1_MBA[0:1] D1_MBG0	O	Must be properly terminated to VTT	These pins can be left unconnected.	
D1_MCK[0:1]/D1_MCK[0:1]_B		O	These pins must be properly terminated.	These pins may be left unconnected.	
D1_MCKE[0:1]		O	Must be properly terminated to VTT These pins are actively driven during reset instead of being released to high impedance.	These pins can be left unconnected.	
D1_MCS[0:3]_B		O	Must be properly terminated to VTT	These pins can be left unconnected.	
D1_MDIC[0:1]		I/O	• These pins are used for automatic calibration of the DDR3L/DDR4 IOs. The MDIC[0:1] pins must be connected to 162 Ω precision 1% resistors. • MDIC[0] is grounded through a 162 Ω precision 1% resistor and MDIC[1] is connected to GV_{DD} through a 162 Ω precision 1% resistor. • For either full- or half-driver strength calibration of DDR IOs, use the same MDIC resistor value of 162 Ω. • The memory controller register setting can be used to determine if automatic calibration is done to full- or half-drive strength.	These pins can be left unconnected.	
D1_MDM[0:3], D1_MDM[8]		O	-	These pins can be left unconnected.	
D1_MDQ[0:31]		I/O	-	These pins can be left unconnected.	
D1_MDQS[0:3]/D1_MDQS[0:3]_B, D1_MDQS[8]/D1_MDQS[8]_B		I/O	-	These pins can be left unconnected.	
D1_MECC[0:3]		I/O	-	These pins can be left unconnected.	
D1_MAPAR_ERR_B	D1_MALERT_B	I	Recommend that a weak pullup resistor (2-10 kΩ) for SDRAM DDR4/DDR3L to $G1V_{DD}$.	This pin should be pulled up.	

Table continues on the next page...

Table 11. DDR controller pin termination checklist (continued)

Signal name[1]		I/O type	Used	Not used	Completed
DDR3L signal	DDR4 signal				
			When using discrete DRAM, the MALERT_B pin needs a strong pull-up resistor (50-100 Ω) to $G1V_{DD}$.		
D1_MPAR		O	-	This pin can be left unconnected.	
D1_MODT[0:1]		O	Ensure the MODT signals are connected correctly. Two dual ranked DIMMs topology is not supported. For a single, dual-ranked DIMM, consider the following connections • MODT(0), MCS(0), MCKE(0) • MODT(1), MCS(1), MCKE(1) For quad-ranked DIMMS, it is recommended to obtain a data sheet from the memory supplier to confirm required signals. But in general, each controller needs MCS(0:3), MODT(0:1), and MCKE(0:1) connected to the one quad-ranked DIMM. These pins are actively driven during reset instead of being released to high impedance.	These pins can be left unconnected.	
D1_MRAS_B		O	Must be properly terminated to VTT	This pin can be left unconnected.	
D1_MCAS_B		O	Must be properly terminated to VTT	This pin can be left unconnected.	
D1_MWE_B		O	Must be properly terminated to VTT	This pin can be left unconnected.	
D1_MVREF	DDR4 Vref is provided internally, the external vref signal needs to be grounded when using DDR4 SDRAM	I/O	DDR reference voltage: 0.49 x $G1V_{DD}$ to 0.51 x $G1V_{DD}$. D1_MVREF can be generated using a divider from $G1V_{DD}$ as MVREF. Another option is to use supplies that generate $G1V_{DD}$, VTT, and D1_MVREF voltage. These methods help reduce differences between $G1V_{DD}$ and MVREF. D1_MVREF generated from a separate regulator is not recommended, because D1_MVREF does not track $G1V_{DD}$ as closely.	This pin must be connected to GND.	

NOTE

1. DDR3L signals are muxed with DDR4 signals and shown in this table.
2. For DDR4, bit and byte swapping rules and layout guidelines, see the application note Hardware and Layout Design Considerations for DDR4 SDRAM Memory Interfaces (document AN5097).
3. When DDR4 Discrete is soldered on the board and two chip selects are used, and the second chip select is bit swizzling (meaning bits mapping from CS0 is additionally swapped in CS1 by swapping DQ0 with DQ1, DQ2 with DQ3, DQ4 with DQ5, and DQ6 with DQ7), then bit map orders of 0x10 (2 1 3 0) and 0x30 (6 5 7 4) are not allowed.

5.1.2 DDR system-level recommendations

Table 12. DDR system-level checklist

Item	Completed
General	
DDR3L /DDR4 mode selection is through por-config signal cfg_dram_type. Ensure that the pin is configured correctly as per the DDR mode. Setting DDR4 mode while applying GV_{DD}=1.35 V can lead to damage of IO's.	
Data Bus inversion (DBI) signals are muxed on Data Mask (D1_MDM) signals and are optional function for DDR4. Only one function can be used at a time.	
HRESET can be used to reset unbuffered DIMM (UDIMM, SoDIMM) or discrete DRAM.	

NOTE

- Stacked memory for DDR4 are not supported
- For devices with four ECC pins, ensure to connect one of the ECC pins to the Prime DQ of ECC DRAM.
- DDR3L/ DDR4 RDIMM is not supported

5.2 Controller Area Network (CAN) pin termination recommendations

Table 13. CAN interface pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
CAN1_RX	I	The functionality is determined by the RCW[IIC3_PMUX] field.	If CAN1 is not used, it can be programmed as GPIO outputs and left unconnected.	
CAN1_TX	O			
CAN2_RX	I	The functionality is determined by the RCW[IIC4_PMUX] field.	If CAN2 is not used, it can be programmed as GPIO output and left unconnected.	
CAN2_TX	O			

5.3 DUART pin termination recommendations

Table 14. DUART pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
UART1_SIN	I	The functionality of these pins is determined by the RCW[UART1_SOUTSIN_PMUX] field	If UART1 is not used, it can be programmed as GPIO outputs and left unconnected.	
UART1_SOUT	O			
UART2_SIN	I	The functionality of these pins is determined by the RCW[UART2_SOUTSIN_PMUX] field	If UART2 is not used, it can be programmed as GPIO outputs and left unconnected.	
UART2_SOUT	O			

5.4 LPUART pin termination recommendations

Table 15. LPUART pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
LPUART1_SIN LPUART1_SOUT	I O	The functionality of these pins is determined by the RCW[IIC3_PMUX] field	If LUART1 is not used, it can be programmed as GPIO outputs and left unconnected. Else input needs to be pulled high through a 2-10 kΩ resistor to OVDD and output can be left unconnected.	
LPUART1_CTS_B LPUART1_RTS_B	I O	The functionality of these pins is determined by the RCW[IIC4_PMUX] field	If these pins are not used, they can be programmed as GPIO outputs and left unconnected. Else input needs to be pulled high through a 2-10 kΩ resistor to OVDD and output can be left unconnected.	
LPUART2_SIN LPUART2_SOUT LPUART2_CTS_B LPUART2_RTS_B	I O I O	The functionality of these pins is determined by the (RCW[XSPI1_A_DATA74_PMUX]) fields	If these pins are not used, they can be programmed as GPIO outputs and left unconnected. Else input needs to be pulled high through a 2-10 kΩ resistor to OVDD and output can be left unconnected.	
LPUART3_SIN LPUART3_SOUT LPUART3_CTS_B LPUART3_RTS_B	I O I O	The functionality of these pins is determined by the RCW[XSPI1_A_DATA30_PMUX]) fields	If these pins are not used, they can be programmed as GPIO outputs and left unconnected. Else input needs to be pulled high through a 2-10 kΩ resistor to OVDD and output can be left unconnected.	
LPUART4_SIN LPUART4_SOUT LPUART4_CTS_B	I O I	The functionality of these pins is determined RCW[SDHC2_DAT74_PMUX]) fields	If these pins are not used, they can be programmed as GPIO outputs and left unconnected. Else input needs to be pulled high	

Table continues on the next page...

Table 15. LPUART pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
LPUART4_RTS_B	O		through a 2-10 kΩ resistor to OVDD and output can be left unconnected.	
LPUART5_SIN LPUART5_SOUT LPUART5_CTS_B LPUART5_RTS_B	I O I O	The functionality of these pins is determined RCW[SDHC2_BASE_PMUX]) fields	If these pins are not used, they can be programmed as GPIO outputs and left unconnected. Else input needs to be pulled high through a 2-10 kΩ resistor to OVDD and output can be left unconnected.	
LPUART6_SOUT	O	The functionality of these pins is determined RCW[UART1_SOUTSIN_PMUX]) fields	If these pins are not used, they can be programmed as GPIO outputs and left unconnected. Else input needs to be pulled high through a 2-10 kΩ resistor to OVDD and output can be left unconnected.	
LPUART6_SIN	I			
LPUART6_RTS_B	O	The functionality of these pins is determined RCW[UART2_SOUTSIN_PMUX]) fields		
LPUART6_CTS_B	I			

1. LPUART6_SOUT cannot be used in single wire mode. It is an output only pin.

5.5 I2C pin termination recommendations

Table 16. I2C pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
IIC1_SCL	IO	The functionality is determined by the (RCW[IIC1_PMUX]) field. Tie these open-drain signals high through a nominal 1 kΩ resistor to OVDD. Optimum pull-up value depends on the capacitive loading of external devices and required operating speed.	If IIC1 is not used, it can be programmed as GPIO outputs and left unconnected.	
IIC1_SDA	IO			
IIC2_SCL	IO	The functionality of this signal is determined by the (RCW[IIC2_PMUX]) field Tie these open-drain signals high through a nominal 1 kΩ resistor to OVDD. Optimum pull-up value depends on the capacitive loading of external devices and required operating speed.	If IIC2 is not used, it can be programmed as GPIO outputs and left unconnected	
IIC2_SDA	IO			
IIC3_SCL	IO	The functionality of this signal is determined by the (RCW[IIC3_PMUX]) field Tie these open-drain signals high through a nominal 1 kΩ resistor to OVDD. Optimum pull-up value	If IIC3 is not used, it can be programmed as GPIO outputs and left unconnected	
IIC3_SDA	IO			

Table continues on the next page...

Table 16. I2C pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
		depends on the capacitive loading of external devices and required operating speed.		
IIC4_SCL	IO	The functionality of this signal is determined by the (RCW[IIC4_PMUX]) field Tie these open-drain signals high through a nominal 1 kΩ resistor to OVDD. Optimum pull-up value depends on the capacitive loading of external devices and required operating speed.	If IIC4 is not used, it can be programmed as GPIO outputs and left unconnected	
IIC4_SDA	IO			
IIC5_SCL	IO	The functionality of this signal is determined by the (RCW[IIC5_PMUX]) field Tie these open-drain signals high through a nominal 1 kΩ resistor to OVDD. Optimum pull-up value depends on the capacitive loading of external devices and required operating speed.	If IIC5 is not used, it can be programmed as GPIO outputs and left unconnected	
IIC5_SDA	IO			
IIC6_SCL	IO	The functionality of this signal is determined by the (RCW[IIC6_PMUX]) field Tie these open-drain signals high through a nominal 1 kΩ resistor to OVDD. Optimum pull-up value depends on the capacitive loading of external devices and required operating speed.	If IIC6 is not used, it can be programmed as GPIO outputs and left unconnected	
IIC6_SDA	IO			
IIC7_SCL	IO	The functionality of this signal is determined by the (RCW[SDHC2_DAT74_PMUX]) field	If IIC7 and IIC8 are not used, it can be programmed as GPIO outputs and left unconnected	
IIC7_SDA	IO			
IIC8_SCL	IO			
IIC8_SDA	IO			

5.6 FlexSPI pin termination recommendations

Table 17. FlexSPI pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
XSPI1_A_SCK	O	The functionality of these signals is determined by the RCW[XSP1_A_BASE_PMUX] field.	Pins maybe left unconnected. If XSPI1_A_DQS is not used, it should be programmed as GPIO output and left as no-connect.	
XSPI1_A_CS[0:1]_B	O			
XSPI1_A_DQS	I/O			

Table continues on the next page...

Table 17. FlexSPI pin termination checklist (continued)

Signal Name	I/O type	Used	Not Used	Completed
		XSPI1_A_SCK and XSPI1_A_CS[1]_B pins must not be pulled down during power-on reset. It may be pulled up, driven high, or if there are no externally connected devices, left in tristate. If these pins are connected to a device that pulls down during reset, an external pull-up is required to drive these pins to a safe state during reset. XSPI1_A_CS[0]_B pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up PFET that is enabled only when the processor is in its reset state. The pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		
XSPI1_A_DATA[0:3]	I/O	The functionality of this signal is determined by the RCW[XSPI1_A_DATA_30_PMUX] field.	If these pins are not used, they should be programmed as GPIO outputs and leave as no-connect.	
XSPI1_A_DATA[4:7]	I/O	The functionality of this signal is determined by the RCW[XSPI1_A_DATA_74_PMUX] field.	If these pins are not used, they should be programmed as GPIO outputs and leave as no-connect.	
XSPI1_B_SCK XSPI1_B_CS[1]_B XSPI1_B_DQS	O O I/O	The functionality of these signals is determined by the RCW[SDHC2_BASE_PMUX] field.	Pins maybe left unconnected. If XSPI1_B_DQS is not used, it should be programmed as GPIO output and left as no-connect.	
XSPI1_B_DATA[0:3]	I/O	The functionality of this signal is determined by the RCW[SDHC2_BASE_PMUX] field.	If these pins are not used, they should be programmed as GPIO outputs and leave as no-connect.	
XSPI1_B_DATA[4:7]	I/O	XSPI data The functionality of this signal is determined by the RCW[SDHC2_DAT74_PMUX] field.	If these pins are not used, they should be programmed as GPIO outputs and leave as no-connect.	

NOTE

Refer AN4375 to calculate maximum achievable FlexSPI interface frequency on a system.

5.7 SPI pin termination recommendations

Table 18. SPI1 interface pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
SPI1_PCS[0:3]	O	If used as a SPI signal, pull up 10 to 100 kΩ to OV_{DD}. The functionality is determined by the RCW[SDHC1_BASE_PMUX] fields	If SPI is unused, program as GPIO outputs or alternate function. Else input needs to be pulled high through a 2-10 kΩ resistor to OVDD and outputs can be left unconnected	
SPI1_SCK	O	The functionality is determined by the RCW[SDHC1_BASE_PMUX] fields.		
SPI1_SIN	I			
SPI1_SOUT	O			

Table 19. SPI2 interface pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
SPI2_PCS[0:3]	O	If used as a SPI signal, pull up 10 to 100 kΩ to OV_{DD}. The functionality of this signal is determined by the RCW[SDHC2_BASE_PMUX] fields.	If SPI is unused, program as GPIO outputs or alternate function. Else input needs to be pulled high through a 2-10 kΩ resistor to OVDD and outputs can be left unconnected	
SPI2_SCK	O	The functionality of this signal is determined by the RCW[SDHC2_BASE_PMUX] fields.		
SPI2_SIN	I			
SPI2_SOUT	O			

Table 20. SPI3 interface pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
SPI3_PCS0	O	If used as a SPI signal, pull up 10 to 100 kΩ to OV_{DD}. The functionality of this signal is determined by the RCW[SPI3_PMUX] fields.	May be left unconnected.	
SPI3_PCS1	O	If used as a SPI signal, pull up 10 to 100 kΩ to OV_{DD}. The functionality of this signal is determined by the RCW[USB_PWRFAULT_PMUX] fields.		
SPI3_PCS2	O	If used as a SPI signal, pull up 10 to 100 kΩ to OV_{DD}. The functionality of this signal is determined by the RCW[USB_DRVBUS_PMUX] fields.		
SPI3_SCK	O	The functionality of this signal is determined by the RCW[SPI3_PMUX] fields.	If SPI is unused, program as GPIO outputs or alternate function. Else input needs to be pulled high	
SPI3_SIN	I			

Table continues on the next page...

Table 20. SPI3 interface pin termination checklist (continued)

Signal Name	I/O type	Used	Not Used	Completed
SPI3_SOUT	O		through a 2-10 kΩ resistor to OVDD and outputs can be left unconnected	

NOTE

Refer AN4375 to calculate maximum achievable SPI interface frequency on a system.

5.8 eSDHC recommendations

LS1028A supports two eSDHC interfaces.

- eSDHC1: Supported primarily for SD cards. This is on the EVDD interface. It always boots at 3.3V, but can dynamically switch to 1.8V controlled by the SDHC1_VSEL output pin.
- eSDHC2: Supported for 1.8V SDIO and 1.8V eMMC. This is on the 1.8V OVDD voltage domain. It does not support SD cards, as it has no card detect or write protect pins.

Modes	eSDHC1- 4 bit EVDD=3.3/1.8V	eSDHC2- 4 bit OVDD =1.8V	eSDHC2-8 bit OVDD=1.8V	comment
SDcard/SDIO card/embedded SDIO				
SD card in Default(25MHz)/High speed (50MHz)	Y	N	N	Cards are supported on eSDHC1 interface only due to availability of CD and WP pins. Only eMMC and eSDIO i.e. soldered down devices supported on eSDHC2 interface.
SDIO card in Default(25MHz)/High speed (50MHz)	Y	N	N	
SD memory/IO card SDR50	Y	N	N	SDR50 is 1.8V only, starts at DS/HS@3.3V and later switches to SDR50@1.8V.
SD memory/IO card DDR50	Y	N	N	DDR50 is 1.8V only, starts at DS/HS@3.3V and later switches to DDR50@1.8V
SD memory/IO card SDR104	Y	N	N	SDR104 is 1.8V only, starts at DS/HS@3.3V and later switches to SDR104@1.8V.
eSDIO SDR50	Y	Y	N	eSDIO devices available at 1.8V also
eSDIO DDR50	Y	Y	N	eSDIO devices available at 1.8V also
eSDIO SDR104	Y	Y	N	eSDIO devices available at 1.8V also

Table continues on the next page...

embedded MMC				
eMMC in Default(20MHz)/High speed (52MHz)	Y	Y	Y	
eMMC DDR	Y	Y (1.8V only)	Y	4 bit supported at both 1.8 and 3.3V 8 bit supported at 1.8V only
eMMC HS200	Y	Y	Y	HS200 is 1.8V only
eMMC HS400	N	N	Y	HS400 is 8 bit only mode, cannot be supported on eSDHC1

5.8.1 eSDHC pin termination recommendations

Table 21. eSDHC1 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
SDHC1_CMD	IO	The functionality is determined by the RCW[SDHC1_BASE_PMUX] field	Program as a GPIO and output.	
SDHC1_DAT[0:3]	IO	These pins should be pulled high through a 10-100 kΩ resistor to EVDD. The functionality is determined by the RCW[SDHC1_BASE_PMUX] field	Unused pins should be pulled high through a 10-100 kΩ resistor to EVDD or program as GPIOs and output.	
SDHC1_CLK	O	The functionality is determined by the RCW[SDHC1_BASE_PMUX] field	Program as GPIO and output.	
SDHC1_CD_B	I	The functionality is determined by the RCW[IIC2_PMUX] field	These pins should be pulled high through a 10-100 kΩ resistor to OVDD or programmed as GPIOs and output.	
SDHC1_WP	I	The functionality is determined by the RCW[IIC2_PMUX] field	These pins should be pulled high through a 10-100 kΩ resistor to OVDD or programmed as GPIOs and output.	
SDHC1_VSEL	O	The functionality is determined by the RCW[SDHC1_BASE_PMUX] field	These pins should be pulled high through a 10-100 kΩ resistor to O2VDD or programmed as GPIOs and output.	
SDHC1_CLK_SYNC_IN	I	The functionality is determined by the RCW[IIC5_PMUX] field	Program as GPIO and output.	
SDHC1_CLK_SYNC_OUT	O	The functionality is determined by the RCW[IIC5_PMUX] field	Program as GPIO and output or left unconnected.	

1. SDHC_CLK_SYNC_OUT to SDHC_CLK_SYNC_IN connection is required in SDR50 and DDR50 mode, all the input signals are sampled with respect to SDHC_CLK_SYNC_IN

2. Sampling clock should be at least 6 times SD_CLK when using modes that requires tuning
3. SDHC_CLK_SYNC_OUT and SDHC_CLK_SYNC_IN should be routed as close as possible to the card, with minimum skew with respect to SD_CLK.
4. As per the SD specification, a power cycle is required to reset the SD card working on UHS-I speed mode. Board design needs to provide some mechanism to power cycle the SD card during every reset.

Table 22. eSDHC2 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
SDHC2_CMD	IO	These pins should be pulled high through a 10-100 kΩ resistor to OVDD. The functionality is determined by the RCW[SDHC2_BASE_PMUX] field	These pins should be pulled high through a 10-100 kΩ resistor to OVDD or Program as a GPIO and output.	
SDHC2_DAT[0:3]	IO	These pins should be pulled high through a 10-100 kΩ resistor to OVDD. The functionality is determined by the RCW[SDHC2_BASE_PMUX] field	Unused pins should be pulled high through a 10-100 kΩ resistor to OVDD or program as GPIOs and output.	
SDHC2_DAT[4:7]	IO	These pins should be pulled high through a 10-100 kΩ resistor to OVDD. The functionality is determined by the RCW[SDHC2_DAT74_PMUX] field	Unused pins should be pulled high through a 10-100 kΩ resistor to OVDD or program as GPIOs and output.	
SDHC2_DS (eMMC HS400 mode)	IO	These pins should be pulled high through a 10-100 kΩ resistor to OVDD. The functionality is determined by the RCW[SDHC2_BASE_PMUX] field	Unused pins should be pulled high through a 10-100 kΩ resistor to OVDD or program as GPIOs and output.	
SDHC2_CLK	O	The functionality is determined by the RCW[SDHC2_BASE_PMUX] field	Program as GPIO and output.	
SDHC2_CLK_SYNC_IN	I	The functionality is determined by the RCW[IIC6_PMUX] field	Program as GPIO and output.	
SDHC2_CLK_SYNC_OUT	O	The functionality is determined by the RCW[IIC6_PMUX] field	Program as GPIO and output or left unconnected.	

1. SDHC_CLK_SYNC_OUT to SDHC_CLK_SYNC_IN connection is required in SDR50 and DDR mode, all the input signals are sampled with respect to SDHC_CLK_SYNC_IN
2. SDHC_CLK_SYNC_OUT and SDHC_CLK_SYNC_IN should be routed as close as possible to the device, with minimum skew with respect to SD_CLK.
3. Sampling clock should be at least 6 times SD_CLK when using modes that requires tuning

5.8.2 eSDHC system-level recommendations

Table 23. eSDHC system-level checklist

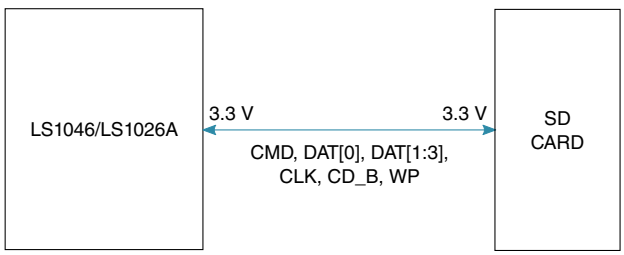
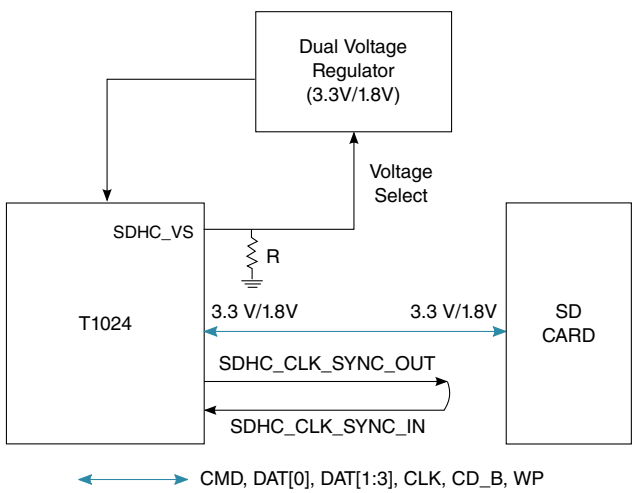
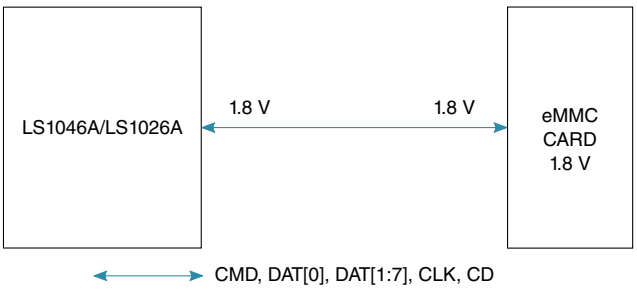
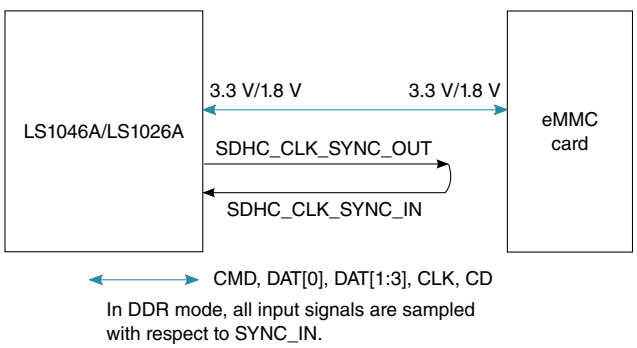
Item	Completed
SD Card interfacing (8-bit is not supported)	
SD Card Connections (DS and HS mode) EVDD configured for 3.3 V  **Figure 31. DS and HS modes**	
SD Card Connections (SDR12, 25, 50, 104, and DDR50 modes) UHS-I modes, work on 1.8 V signalling. The SYNC_OUT, SYNC_IN connections are required in SDR50 and DDR50 modes only. **NOTE:** Resistor R=10 K is needed when RCW loading is required to be done from SD card.  **Figure 32. SDR12, 25, 50, 104, and DDR50 modes**	
eMMC Interfacing	
eMMC Card Connections (DS, HS, HS200 Modes) at 1.8 V card The 8-bit eMMC interface requires EVDD and OVDD configured at 1.8V	

Table continues on the next page...

Table 23. eSDHC system-level checklist (continued)

Item	Completed
 **Figure 33. DS, HS, and HS200 modes for eMMC (1.8 V)** **NOTE:** • HS200 mode is 1.8 V only mode as per eMMC 4.5 specification	
eMMC Card Connection in DDR mode The 8-bit operation cannot be supported due to RCW selection constraints. The DDR mode supports both 3.3 V and 1.8 V operation as per eMMC 4.4 specification.  **Figure 34. DDR mode**	

5.9 Synchronous Audio Interface (SAI)/Integrated Interchip Sound (I^2S) recommendations

LS1028A supports six Synchronous Audio Interfaces (SAI) which support simplex operation.

When using all 6 SAI instances, LS1028A can support either 4 RX and 2 TX, or 2 Rx and 4 TX SAI instances, there is no way to support 3 RX and 3 TX instances

Multiple SAI instances are not synchronized within the SoC

5.9.1 SAI pin termination recommendations

Table 24. SAI1 and SAI2 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
SAI1_RX_BCLK SAI2_RX_BCLK	IO	The functionality of this signal is determined by the RCW[SDHC1_BASE_PMUX]=0b100 field	If SAI1 and SAI2 are unused, program as GPIO outputs. Else input needs to be pulled high through a 2-10 kΩ resistor to OVDD and outputs can be left unconnected	
SAI1_RX_DATA SAI2_RX_DATA	I			
SAI1_RX_SYNC SAI2_RX_SYNC	IO			
SAI1_TX_BCLK or SAI2_TX_BCLK	IO	The functionality of this signal is determined by the RCW[SDHC1_BASE_PMUX]=0b011 field		
SAI1_TX_DATA SAI2_TX_DATA	I			
SAI1_TX_SYNC SAI2_TX_SYNC	IO			

Table 25. SAI3 and SAI6 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
SAI3_RX_BCLK SAI6_RX_BCLK	IO	The functionality of this signal is determined by the RCW[EC1_SAI3_6_PMUX]=0b011 field	If SAI3 and SAI6 are unused, program as GPIO outputs. Else input needs to be pulled high through a 2-10 kΩ resistor to OVDD and outputs can be left unconnected	
SAI3_RX_DATA SAI6_RX_DATA	I			
SAI3_RX_SYNC SAI6_RX_SYNC	IO			
SAI3_TX_BCLK or SAI6_TX_BCLK	IO	The functionality of this signal is determined by the RCW[EC1_SAI3_6_PMUX]=0b010 field		
SAI3_TX_DATA SAI6_TX_DATA	I			
SAI3_TX_SYNC SAI6_TX_SYNC	IO			

Table 26. SAI4 and SAI5 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
SAI4_RX_BCLK SAI5_RX_BCLK	IO	The functionality of this signal is determined by the RCW[EC1_SAI4_5_PMUX]=0b011 field	If SAI4 and SAI5 are unused, program as GPIO outputs. Else input needs to be pulled high through a 2-10 kΩ resistor to OVDD and outputs can be left unconnected	
SAI4_RX_DATA SAI5_RX_DATA	I			
SAI4_RX_SYNC	IO			

Table continues on the next page...

Table 26. SAI4 and SAI5 pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
SAI5_RX_SYNC				
SAI4_TX_BCLK or SAI5_TX_BCLK	IO	The functionality of this signal is determined by the RCW[EC1_SAI4_5_PMUX]=0b010 field		
SAI4_TX_DATA SAI5_TX_DATA	I			
SAI4_TX_SYNC SAI5_TX_SYNC	IO			

5.10 Trust pin termination recommendations

Table 27. Trust pin termination checklist

Signal name	IO type	Used	Not used	Completed
TA_BB_TMP_DETECT_B	I	If a tamper sensor is used, it must maintain the signal at the specified voltage (1.0 V) until a tamper is detected. A 1 kΩ pull-down resistor is strongly recommended.	This pin should be pulled high through a 2-10 kΩ resistor to VDD (1.0 V).	
TA_TMP_DETECT_B	I	If a tamper sensor is used, it must maintain the signal at the specified voltage (OVDD) until a tamper is detected. A 1 kΩ pull-down resistor is strongly recommended.	This pin should be pulled high through a 2-10 kΩ resistor to OVDD.	

5.11 System Control pin termination recommendations

Table 28. System Control pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
PORESET_B	I	This pin is required to be asserted as per the applicable chip data sheet, in relation to minimum assertion time and during power-up/power-down. It is an input-only pin and must be asserted to sample power on configuration pins.		
HRESET_B	I/O	This pin is an open drain signal and should be pulled high through a 2-10 kΩ resistor to OV_{DD}. It is recommended to use a test point on this signal for debug purposes.		
RESET_REQ_B	O	Must not be pulled down during power-on reset.	This pin should be pulled high through a 2-10 kΩ resistor to OV_{DD} and must not be pulled down during power-on reset.	

NOTE

1. If on-board programming of FlexSPI NAND boot flash, FlexSPI NOR boot flash, I2C, or SD card is needed, then maintain an option (may be via a jumper) that keeps PORESET_B and RESET_REQ_B disconnected from each other. Booting from a blank NAND flash or SPI flash causes boot error, which in turn causes assertion of RESET_REQ_B. When RESET_REQ_B is connected with PORESET_B, the device goes in a recurring reset loop and does not provide enough time for JTAG to take control of the device and perform any operation.
2. When booting from I2C, refer LS1028A CE document for I2C A-010650.
3. For RCW override, RESET_REQ_B should be disconnected from PORESET_B or HRESET_B. An option on board is required.

5.12 Power Management pin termination recommendations

Table 29. Power Management pin termination checklist

Signal name	IO type	Used	Not used	Completed
ASLEEP	O	The functionality of this signal is determined by the ASLEEP field in the reset configuration word (RCW[ASLEEP_PMUX]).	Can be left floating as it is an output, alternately it may be programmed as GPO. It is recommended to have a test pin on this signal for debug.	

5.13 Debug and reserved pin termination recommendations

Table 30. Debug and test pin termination checklist

Signal name	I/O type	Used	Not used	Completed
SCAN_MODE_B	I	This is a test signal for factory use only and must be pulled up (100 Ω - 1 kΩ) to OV_{DD} for normal device operation.		
TEST_SEL_B	I	This pin must be pulled to OV_{DD} through a 100 Ω to 1 kΩ resistor for a LS1028A device and tied to the ground for a LS1027A device.		
EVT_B[1:2]	I/O	The functionality of these signals is determined by the RCW[IIC5_PMUX] field.	If this pin is not used, it should be programmed as GPIO output and left unconnected.	
EVT0_B, EVT3_B	I/O	The functionality of these signals is determined by the RCW[IIC6_PMUX] field.		
EVT4_B	I/O	The functionality of this signal is determined by the RCW[CLK_OUT_PMUX] field.		
EVT_B[5:6]	I/O	The functionality of these signals is determined by the RCW[IIC3_PMUX] field.		
EVT_B[7:8]	I/O	The functionality of these signals is determined by the RCW[IIC4_PMUX] field.		

Table continues on the next page...

Table 30. Debug and test pin termination checklist (continued)

Signal name	I/O type	Used	Not used	Completed
EVT_B[9]	I/O	The functionality of this signal is determined by the RCW[ASLEEP_PMUX] field.		
TBSCAN_EN_B[1]	I	It is advised that boards are built with the ability to pull up and pull down this pin. • For normal debug operation, this pin must be pulled high to OV_{DD} through 4.7 kΩ resistor. • For boundary scan operation, this pin must be pulled low to GND through 4.7 kΩ resistor.		
FA_VL	-	Reserved. This pin must be pulled to ground (GND).		
PROG_MTR	-	Reserved. This pin must be pulled to ground (GND).		
FA_ANALOG_PIN	-	This pin must be pulled to ground (GND).		
TD1_ANODE	-	Connect as required.	Tie to GND if not used.	
TD1_CATHODE	-	Connect as required.	Tie to GND if not used.	
FA_ANALOG_G_V	IO	This pin must be pulled to ground (GND).		

NOTE

1. TBSCAN_EN_B is an IEEE 1149.1 JTAG Compliance Enable pin.
   - 0:To be compliant to the 1149.1 specification for boundary scan functions. The JTAG compliant state is documented in the BSDL.
   - 1: JTAG connects to DAP controller for the Arm core debug.

5.14 SerDes pin termination recommendations

Table 31. SerDes pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
SD1_IMP_CAL_RX	I	Tie to SV_{DD} through a 200 Ω 1% resistor.	If the SerDes interface is entirely unused, this pin must be left unconnected.	
SD1_IMP_CAL_TX	I	Tie to XV_{DD} through a 698 Ω 1% resistor.		
SD1_REF_CLK1_P SD1_REF_CLK1_N	I	Ensure clocks are driven from an appropriate clock source, as per the protocol selected by the RCW settings.	If the PLL is unused, pull down to GND.	
SD1_REF_CLK2_N SD1_REF_CLK2_P	I			
SD1_RX[0:3]_N	I	Ensure pins are correctly terminated for the interface type used.	If the SerDes interface is entirely or partly unused, the unused pins must be pulled down to GND.	
SD1_RX[0:3]_P	I			
SD1_TX[0:3]_N	O	Ensure pins are correctly terminated for the interface type used.	If SerDes interface is entirely or partly unused, the unused pins must be left unconnected.	
SD1_TX[0:3]_P	O			

NOTE

1. In the RCW configuration field SRDS_PLL_PD_S1, the respective bits for each unused PLL must be set to power it down. The SerDes module is disabled when both of its PLLs are turned off.
2. After Power on Reset, if an entire SerDes module is unused, it must be powered down by clearing the SDEN fields of its corresponding PLL1 and PLL2 reset control registers (SRDSxPLLaRSTCTL).
3. Unused lanes must be powered down by clearing the RRST_B and TRST_B fields and setting the RX_PD and TX_PD fields in the corresponding lane's general control register (SRDSxLNmGCR0).
4. A spread-spectrum reference clock is permitted for PCI Express. However, if any other high-speed interface, such as SGMII or SATA, is used concurrently on the same SerDes PLL, spread-spectrum clocking is not permitted.
5. PCIe Gen 3 cannot be used if SATA is also being used on the same SerDes.
6. When LS1028A is used as an EP on motherboards, it is recommended to use the PCIe express clock from the PCIe slot as SerDes reference clock. This ensures that +/- 300ppm reference clock tolerance is met at both ends. This clocking architecture also supports spread spectrum clocking as per PCIe base specification.
7. As per PCIe base specification 3.0, both ends of link should enter LTSSM Detect state within 20 ms of the end of Fundamental Reset.
8. If SerDes lanes are routed to a backplane slot or a PCIe connector, SerDes pins can be left unterminated even if the link partner card is not present. If some SerDes lanes are a no-connect, pull down their receiver pins to GND. Then, if the SerDes block is powered, refer to the RM's Unused Lanes section for directions on how to power them down. To power down a SerDes lane, configure the General Control 0 register during the PBI phase. If the whole SerDes block is already powered down, there is no need to individually power down a lane.

5.14.1 Optimal setting for the SerDes channel Rx Equalization Boost bit

Select the optimal setting for the SerDes channel Rx Equalization Boost bit suitable for a particular end product system board.

For certain high speed SerDes protocols, the Rx Equalization Boost bits for all the SerDes lanes in use are initialized with a default value of 1b by the RCW. In reality, although the default 1b setting does overlap with the 0b setting in terms of Rx Equalization boost effect, the 0b setting works better for short and normal SerDes channels, while the 1b setting works better for high loss channels.

For end product system with non-high loss SerDes channels (lanes), using the default 1b setting of the Rx Equalization Boost bit may adversely enhance the return loss due to some discontinuities possibly presented in the channel. This may further causes more reflection. Therefore, unless the channel is high loss, to ensure the channel's health and better performance, the 0b setting of Rx Equalization Boost bit should be used for all the lanes, instead of the default 1b setting.

The following high speed SerDes protocols are related to this issue. If a protocol supports more than one speed, only the speed(s) listed below is affected.

- PCI Express Gen3 (8.0 GT/s)
- SATA 6 Gbaud

Since the channel characteristics is board and layout dependent, NXP cannot quantify the actual channel loss introduced during board design, layout and fabrication of all end product systems for our customers. Customers should always perform board level simulation and also use other appropriate tool (for example, NXP's SerDes Validation Tool) and/or instrument to determine whether the SerDes channels (lanes) are in high loss condition and then adopt the best setting suitable for their end

product and application. Instead of quantifying a SerDes channel as high or non-high loss, a more practical way is to try both the 1b and 0b settings and find out which setting yields better signal integrity for the customer's particular end product system or board.

Once determined that the channels are in non-high loss condition, the Rx Equalization Boost bit for all the lanes in use should be set to 0b during the Pre-boot Initialization (PBI) stage.

Since the Rx Equalization Boost bit is defined in different SerDes registers depending on the SerDes protocols in use, it is important to select the appropriate SerDes register with the correct offset and value as described below when implementing the register write in PBI. The SerDes registers involved are defined on a per lane basis. Therefore, PBI register write must be implemented for all the lanes utilized for the affected SerDes protocols and speeds.

- For PCI Express Gen3 (8.0 GT/s):

  Perform a PBI write to each lane's LNaSSCR1 register with a value of 0x9849_db00, which sets this lane's Rx Equalization Boost bit, LNaSSCR1 [RXEQ_BST_1] to 0b.

  Note that the RATIO_PST1Q_1 and AMP_RED_1 bit fields of the LNaSSCR1 register are read-only and directly driven by the PCI Express controller core hardware based on the Gen3 link training equalization negotiation result. Therefore, it is normal to observe values of the above bit fields different from lane to lane.

- For SATA 6 Gbaud:

  Perform a PBI write to each lane's LNaSSCR1 register with a value of 0x0050_2880, which sets this lane's Rx Equalization Boost bit, LNaSSCR1 [RXEQ_BST_1] to 0b.

- For USXGMII 10.3125 Gbaud:

  Perform a PBI write to each lane's LNaRECR0 register with a value of 0x0000_045F, which sets this lane's Rx Equalization Boost bit, LNaRECR0 [RXEQ_BST] to 0b.

5.15 USB PHY 1 and PHY 2 pin termination recommendations

Table 32. USB 1/2 PHY pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
USB[1/2]_D_P	IO	USB PHY Data Plus	Do not connect. These pins should be left floating.	
USB[1/2]_D_M	IO	USB PHY Data Minus	Do not connect.These pins should be left floating.	
USB[1/2]_VBUS	I	USB1 power supply pin. A charge pump external to the USB 3.0 PHY must provide power to this pin. The nominal voltage for this pin is 5 V.	Do not connect.These pins should be left floating.	
USB[1/2]_ID	I	USB PHY ID Detect	Pull low through a 1kΩ resistor to GND.	
USB[1/2]_TX_P	O	USB PHY 3.0 Transmit Data (positive)	Do not connect.These pins should be left floating.	
USB[1/2]_TX_M	O	USB PHY 3.0 Transmit Data (negative)	Do not connect.These pins should be left floating.	
USB[1/2]_RX_P	I	USB PHY 3.0 Receive Data (positive)	Connect to ground (GND)	
USB[1/2]_RX_M	I	USB PHY 3.0 Receive Data (negative)	Connect to ground (GND)	

Table continues on the next page...

Table 32. USB 1/2 PHY pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
USB[1/2]_RESREF	IO	Attach a 200-Ω 1% 100-ppm/ ^{0}C precision resistor-to-ground on the board.	Do not connect.These pins should be left floating.	
USB_DRVVBUS	O	VBUS power enable. For example, if an external hub is used, it can handle this signal. The functionality of the USB_DRVVBUS signal is determined by the RCW[USB_DRVVBUS_PMUX] field in the reset configuration word.	Do not connect.These pins can be left floating.	
USB_PWRFAULT	I	Indicates that a VBUS fault has occurred. For example, if an external hub is used, it can handle this signal. The functionality of the USB_PWRFAULT signal is determined by the RCW[USB_PWRFAULT_PMUX] field in the reset configuration word.	Pull low through a 1kΩ resistor to GND.	
USB2_DRVVBUS	O	VBUS power enable. For example, if an external hub is used, it can handle this signal. The functionality of the USB2_DRVVBUS signal is determined by RCW[IIC6_PMUX] field in the reset configuration word.	Do not connect.These pins can be left floating.	
USB2_PWRFAULT	I	Indicates that a VBUS fault has occurred. For example, if an external hub is used, it can handle this signal. The functionality of the USB2_PWRFAULT signal is determined by the RCW[IIC6_PMUX] field in the reset configuration word.	Pull low through a 1kΩ resistor to GND.	

NOTE

USB[1/2]_VBUS: The permissible voltage range is 0 - 5.25V.

USB[1/2]_ID: The permissible voltage range for input signal is 0 - 1.8V.

5.15.1 USB1 PHY connections

This section describes the hardware connections required for the USB PHY.

This figure shows the VBUS interface for the chip.

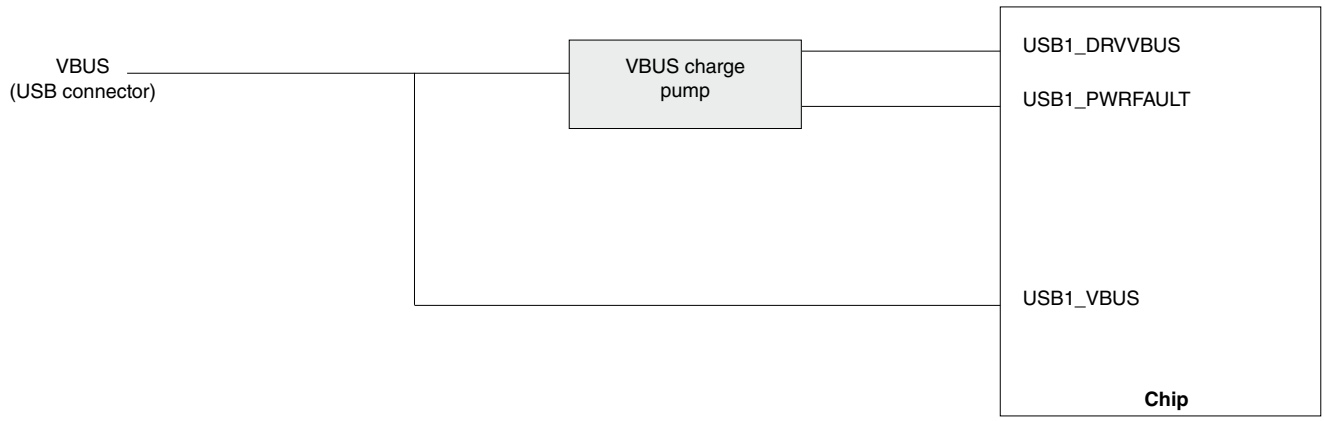


Figure 35. USB1 PHY VBUS interface

5.16 IEEE1722 pin termination recommendations

Table 33. IEEE 1722 pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
EC1_1722_DAT[0]	IO	The functionality of this pin is determined by the RCW[GTX_CLK125_P MUX] field.	Program as GPIO output and left unconnected.	
EC1_1722_DAT[1]	IO	The functionality of this pin is determined by the RCW[EC1_SAI4_5_P MUX] field.		
EC1_1722_DAT[2]	IO	The functionality of these pins is determined by the RCW[SPI3_PMUX] field.		
EC1_1722_DAT[3]	IO			

NOTE

The 1722 pins can be configured for various functions, refer PTCMRa[TMODE]

5.17 IEEE1588 pin termination recommendations

Table 34. IEEE 1588 pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
EC1_1588_CLK_IN	I	For EC1_1588_CLK_IN, connect to external high-precisiontimer reference input.	Program as a GPIO output and left unconnected.	
EC1_1588_CLK_OUT	O			
EC1_1588_PULSE_OUT2	O			
EC1_1588_TRIG_IN1	I			

Table continues on the next page...

Table 34. IEEE 1588 pin termination checklist (continued)

Signal Name	I/O type	Used	Not used	Completed
		The functionality of these pins is determined by the RCW[EC1_SAI3_6_PMUX] field.		
EC1_1588_ALARM_OUT1	O	The functionality of these pins is determined by the RCW[EC1_SAI4_5_PMUX] field.	Program as a GPIO output and left unconnected.	
EC1_1588_PULSE_OUT1	O			
SWITCH_1588_DAT[0:1]	IO			
EC1_1588_ALARM_OUT2	O	The functionality of these pins is determined by the RCW[SPI3_PMUX] field.	Program as a GPIO output and left unconnected.	
EC1_1588_TRIG_IN2	I			
SWITCH_1588_DAT[2:3]	IO			

NOTE

When configured for IEEE 1588, the EC1 pins are not available.

5.18 Ethernet Management Interface 1 pin termination recommendations

Table 35. Ethernet Management Interface (EMI1) pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
EMI1_MDC	O	EMI1_MDC will be actively driven and pull up resistors are not required.	This pin can be left unconnected.	
EMI1_MDIO	IO	EMI1_MDIO will be actively driven. A pull up resistors might still be required as the peripherals on EMI bus might have their EMI1_MDIO pins configured as open-drain. The value of pull-up resistor depends on total input impedance of all the peripherals connected.	This pin can be left unconnected.	

NOTE

- Non-monotonic edges of MDC may result MDIO getting stuck in busy condition. It is recommended to simulate board design using IBIS model to ensure clean waveform of MDC. Also it'll help to have a place holder for series termination and a capacitor as close as possible to MDC pin of LS1028A. User can get the appropriate value based on actual board measurements.

5.19 Ethernet Controller (RGMII) 1 pin termination recommendations

Table 36. Ethernet controller pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
EC1 in RGMII mode				
EC1_TXD[0:1]	O	The functionality of these pins is determined by RCW[EC1_SAI3_6_PMUX] field.	Program as a GPIO output and left unconnected.	
EC1_RXD[0:1]	I			
EC1_RX_DV	I			
EC1_RX_CLK	I			
EC1_TXD[2:3]	O	The functionality of these pins is determined by RCW[EC1_SAI4_5_PMUX] field.	Program as a GPIO output and left unconnected.	
EC1_TX_EN[1]	O			
EC1_GTX_CLK	O			
EC1_RXD[3:2]	I			
EC1_GTX_CLK125	I	The functionality of this pin is determined by RCW[GTX_CLK125_PMUX] field.	Program as a GPIO output and left unconnected.	

NOTE

1. This pin requires an external 1-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.

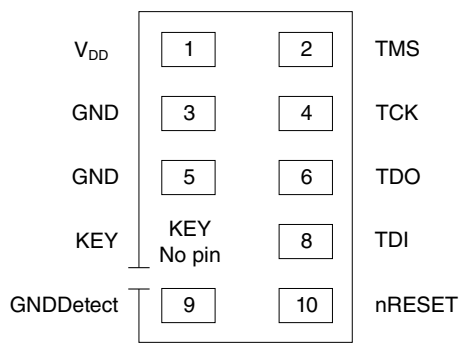
5.20 JTAG pin termination recommendations

Table 37. JTAG pin termination checklist

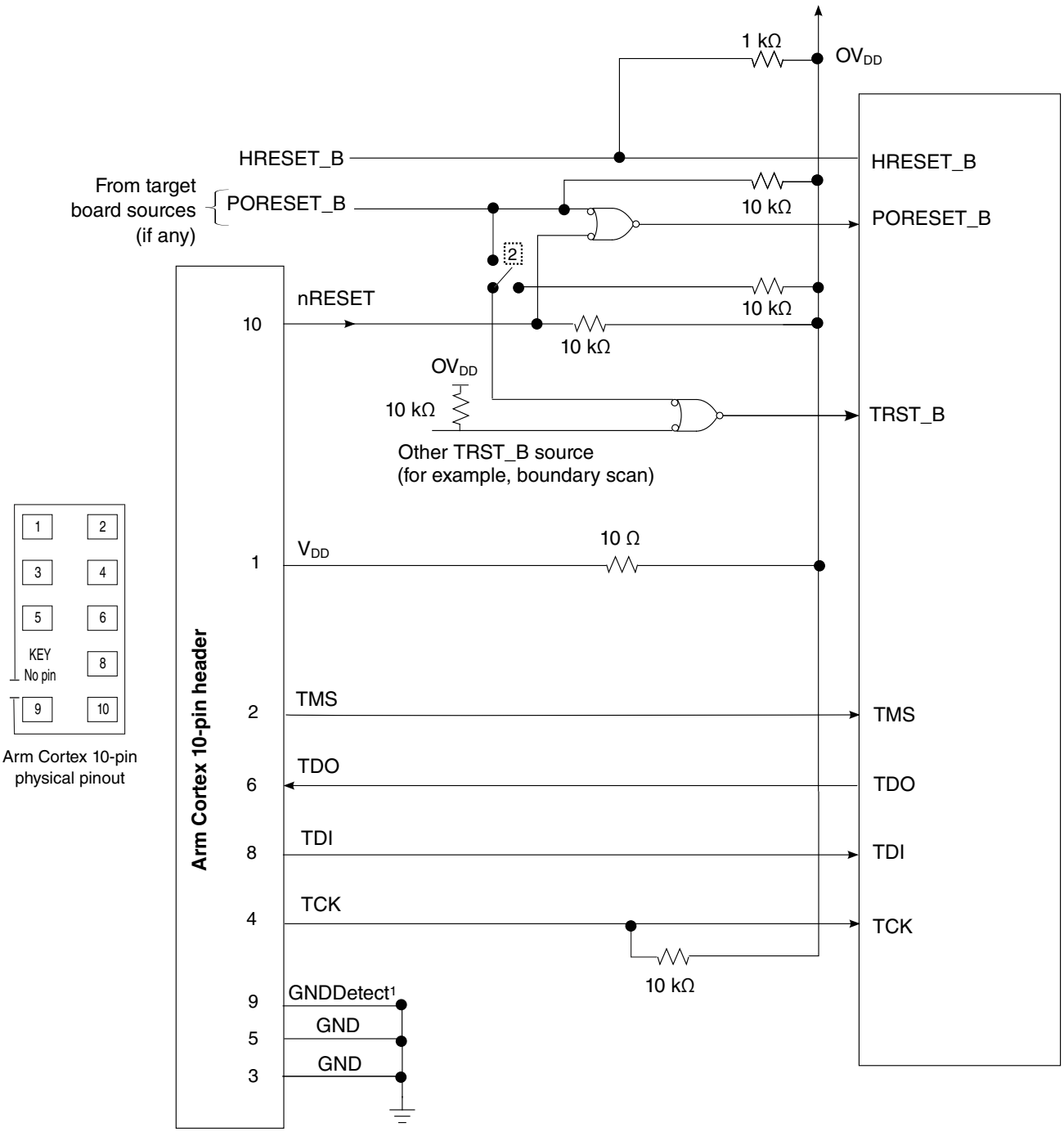
Signal Name	IO type	Used	Not Used	Completed
TCK	I	Connect to pin 4 of the Arm Cortex 10-pin header. This pin requires a 2-10 kΩ resistor to OV_{DD}.		
TDI	I	Connect to pin 8 of the Arm Cortex 10-pin header. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.	May be left unconnected.	
TDO	O	Connect to pin 6 of the Arm Cortex 10-pin header. This output is actively driven during reset rather than being tri-stated during reset.	May be left unconnected.	
TMS	I	Connect to pin 2 of the Arm Cortex 10-pin header. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.	May be left unconnected.	
TRST_B	I	This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled. Connect as shown in Figure 36.	Tie TRST_B to PORESET_B through a 0 kΩ resistor.	

5.20.1 JTAG system-level recommendations

Table 38. JTAG system-level checklist

Item	Completed
Arm®Cortex® 10-pin header signal interface to JTAG port	
Configure the group of system control pins as shown in Figure 36. **NOTE:** These pins must be maintained at a valid deasserted state under normal operating conditions, because most have asynchronous behavior and spurious assertion gives unpredictable results.	
The JTAG port of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The Arm Cortex 10-pin header connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The Arm Cortex 10-pin header interface requires the ability to independently assert PORESET_B in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the nRESET signals must be merged into these signals with logic.	
Boundary-scan testing	
Ensure that TRST_B is asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation.	
Follow the arrangement shown in Figure 36 to allow the Arm Cortex 10-pin header to assert PORESET_B independently while ensuring that the target can drive PORESET_B as well.	
The Arm® Cortex® 10-pin interface has a standard header, shown in the following figure. The connector typically has pin 7 removed as a connector key. The signal placement recommended in this figure is common to all known emulators.  **NOTE:** The Arm Cortex 10-pin header adds many benefits such as breakpoints, watch points, register and memory examination/modification, and other standard debugger features. An inexpensive option is to leave the Arm Cortex 10-pin header unpopulated until needed.	

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 36. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions, as most have asynchronous behavior and spurious assertion gives unpredictable results.



Note:
1. GNDDetect is an optional board feature. Check with 3rd-party tool vendor.
2. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, ensure this switch is closed.

Figure 36. JTAG interface connection

5.21 Clock pin termination recommendations

Table 39. Clock pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
EC1_GTX_CLK	O	The functionality of this pin is determined by RCW[EC1_SAI4_5_PMUX] field.	Program as a GPIO output and left unconnected.	
EC1_GTX_CLK125	I	The functionality of this pin is determined by RCW[GTX_CLK125_PMUX] field. LS1028A has a duty cycle reshaper inside RGMII block. This allows GTX clock from RGMII PHY to be used.		
DIFF_SYSCLK_P	I	These pins are the differential primary clock input to the chip. These pins support 100 MHz only. These pins should be connected to a 100 MHz differential clock generator.		
DIFF_SYSCLK_N	I			

5.22 Display Unit Interface recommendations

LS1028A supports a eDP and DP controller with PHY

5.22.1 Display Interface Unit pin termination recommendations

Table 40. Display interface pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
DP_HPD	I	These pin should be pulled down through 1 MΩ resistor to GND.		
DP_LANE_P[0:3]	O	All lanes should be decoupled with 100nF.	May be left unconnected.	
DP_LANE_N[0:3]	O	All lanes should be decoupled with 100nF.	May be left unconnected.	
DP_AUX_P	IO	All lanes should be decoupled with 100nF. These pin should be pulled down through 100 kΩ resistor to GND.	Pull low through a 2-10kΩ resistor to GND.	
DP_AUX_N	IO	All lane should be decoupled with 100nF. These pin should be pulled high through 100 kΩ resistor to USB_HVDD.	Pull low through a 2-10kΩ resistor to GND.	
DP_REXT	I	Connect 500 ohm, 1% resistance to GND.		
DP_REFCLK_P	I	27MHz HCSL differential clock plus should be given. Input clock must be ac coupled.	Pull low through a 2-10kΩ resistor to GND.	

Table continues on the next page...

Table 40. Display interface pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
DP_REFCLK_N	I	27MHz HCSL differential clock minus should be given. Input clock must be ac coupled.	Pull low through a 2-10kΩ resistor to GND.	

5.23 FlexTimer recommendations

The FlexTimer module implements the following parameter settings in the chip:

Table 41. FlexTimer parameter settings

FlexTimer parameters	FTM1	FTM2	FTM3	FTM4	FTM5	FTM6	FTM7	FTM8
Number of channels available at device I/O level	8	3	3	3	3	3	3	3
Quadrature decoding support	Yes	No	No	No	No	No	No	No
EXT_CLK support	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Fixed frequency clock support	Internally generated secure clock							
System clock support	Platform clock/2							
Stop mode support	Yes. Refers to the LPM20 low power mode of the chip.							

5.23.1 FTM1 pin termination recommendations

Table 42. FTM1 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM1_CH[0]	IO	The functionality of this pin is determined by the RCW[IIC2_PMUX] field.	Program as a GPIO output and left unconnected.	
FTM1_CH[1]	O	The functionality of this pin is determined by the RCW[CLK_OUT_PMUX] field.	Program as a **GPIO output only** and left unconnected.	
FTM1_CH[2]	IO	The functionality of these pins is determined by the RCW[EC1_SAI4_5_PMUX] field.	If these pins are not used, they can be programmed as GPIO outputs and left unconnected. Else input needs to be pulled low through a 2-10kΩ resistor to GND.	
FTM1_CH[3]	IO			
FTM1_CH[6]	IO			
FTM1_CH[7]	IO			
FTM1_EXTCLK	I			
FTM1_FAULT	I			

Table continues on the next page...

Table 42. FTM1 pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
FTM1_CH[4]	IO	The functionality of these pins is determined by the RCW[EC1_SAI3_6_PMUX] field.	If these pins are not used, they can be programmed as GPIO outputs and left unconnected. Else input needs to be pulled low through a 2-10kΩ resistor to GND.	
FTM1_CH[5]	IO			
FTM1_QD_PHA	I			
FTM1_QD_PHB	I			

5.23.2 FTM2 pin termination recommendations

Table 43. FTM2 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM2_CH[0]	IO	The functionality of this pin is determined by the RCW[IIC2_PMUX] field.	Program as a GPIO output and left unconnected.	
FTM2_CH[1]	IO	The functionality of these pins is determined by the RCW[XSPI1_A_DATA74_PMUX] field.	If these pins are not used, they can be programmed as GPIO outputs and left unconnected. Else input needs to be pulled low through a 2-10kΩ resistor to GND.	
FTM2_CH[2]	IO			
FTM2_EXTCLK	I			

5.23.3 FTM3 pin termination recommendations

Table 44. FTM3 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM3_CH[0:2]	IO	The functionality of these pins is determined by the RCW[XSPI1_A_DATA30_PMUX] field.	If these pins are not used, they can be programmed as GPIO outputs and left unconnected. Else input needs to be pulled low through a 2-10kΩ resistor to GND.	
FTM3_EXTCLK	I			

5.23.4 FTM4 pin termination recommendations

Table 45. FTM4 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM4_CH[0:2]	IO	The functionality of these pins is determined by the RCW[SDHC2_DAT74_PMUX] field.	If these pins are not used, they can be programmed as GPIO outputs and left unconnected. Else input needs to be pulled low through a 2-10kΩ resistor to GND.	
FTM4_EXTCLK	I			

5.23.5 FTM5 pin termination recommendations

Table 46. FTM5 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM5_CH[0:1]	IO	The functionality of these pins is determined by the RCW[SDHC2_BASE_ PMUX] field.	If these pins are not used, they can be programmed as GPIO outputs and left unconnected. Else input needs to be pulled low through a 2-10kΩ resistor to GND.	
FTM5_CH[2]	I			
FTM5_EXTCLK	I			

5.23.6 FTM6 pin termination recommendations

Table 47. FTM6 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM6_CH[0]	O	The functionality of these pins is determined by the RCW[UART1_SOUTSIN_PMUX] field.	If these pins are not used, it can be programmed as GPIO output and left unconnected. Else input need to be pulled low through a 2-10kΩ resistor to GND.	
FTM6_EXTCLK	I			
FTM6_CH[1]	O	The functionality of these pins is determined by the RCW[UART2_SOUTSIN_PMUX] field.	Program as a GPIO output and left unconnected.	
FTM6_CH[2]	IO			

5.23.7 FTM7 pin termination recommendations

Table 48. FTM7 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM7_CH[0]	IO	The functionality of these pins is determined by the RCW[IIC3_PMUX] field.	If this pin is not used, it can be programmed as GPIO output and left unconnected. Else input need to be pulled low through a 2-10kΩ resistor to GND.	
FTM7_EXTCLK	I			
FTM7_CH[1]	O	The functionality of these pins is determined by the RCW[IIC4_PMUX] field.	Program as a GPIO and as an output.	
FTM7_CH[2]	IO			

5.23.8 FTM8 pin termination recommendations

Table 49. FTM8 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM8_CH[0:2]	O	The functionality of these pins is determined by the RCW[XSPI1_A_BASE_PMUX] field.	Program as a GPIO output and left unconnected. Else input need to be pulled low through a 2-10kΩ resistor to GND.	
FTM8_EXTCLK	I			

5.24 General Purpose Input/Output pin recommendations

Table 50. General Purpose Input/Output pin checklist

Signal Name	IO type	Completed
GPIO1_DAT[2:3]	IO	
GPIO1_DAT[6]	IO	
GPIO1_DAT[7]	O	
GPIO1_DAT[10]	IO	
GPIO1_DAT[11]	O	
GPIO1_DAT[15:31]	IO	
GPIO2_DAT[6:8]	O	
GPIO2_DAT[9:19]	IO	
GPIO2_DAT[20:22]	O	
GPIO2_DAT[23:31]	IO	
GPIO3_DAT[0:18]	IO	

NOTE

- When GPIOx pin is not used, program it as an output and left unconnected.
- Any GPIO configured as an input, can optionally generate an interrupt upon detection of an edge.
- Since LS1028A does not support any external IRQs GPIOs can be used to interface with devices which generate edge based interrupts. To support devices which generate level interrupts, Software ISR should be designed accordingly.
- When an individual GPIO port's direction is set to input (GPIO_GPDIR[DRn=0]), the associated input enable must be set (GPIOxGPIE[IEn]=1) to propagate the port value to the GPIO Data Register.
- GPIO1_DAT[7], GPIO1_DAT[11], GPIO2_DAT[6:8] and GPIO2_DAT[20:22] are **output only**.

5.25 eSDHC and FlexSPI interface frequency calculations

This section describes the settings to be used for maximising the frequency of SDHC and FlexSPI for different speed bins of LS1028A. Other selections and frequencies are also possible, please refer Reference Mnaual for the details

This table describes the eSDHC interface frequency calculations.

Table 51. eSDHC interface frequency calculations

Core frequency (MHz)	Platform frequency (MHz)	DDR data rate (MT/s)	eSDHC										Notes
							eSDHC1[5]		eSDHC2				
							HS200 or SDR104		HS200 or SDR104		HS400		
			CGA_PLL2 (MHz)	HWA_DIV[1]	Peripheral clock (MHz)[1]	BASE_CLK (MHz)[2]	SDHC1_DIV[3, 4]	SDHC1_CLK (MHz)	SDHC2_DIV[3, 4]	SDHC2_CLK (MHz)	SDHC2_DIV[3, 4]	SDHC2_CLK (MHz)	
1500	400	1600	1200	1	1200	600	3	200	4	150	4	150	6
1300	400	1600	1200	1	1200	600	3	200	4	150	4	150	
1000	400	1600	1200	1	1200	600	3	200	3	200	4	150	
800	300	1300	1000	1	1000	500	3	167	3	167	4	125	7

Notes:

1. Selection through RCW[HWA_CGA_M2_CLK_SEL] field.
2. Base clock can be selected by programming ESDHCCTL[PCS]. It selects between platform clock and peripheral clock / 2
3. Minimum value for SDHC_DIV can be 3 and 4 for HS200/SDR104 and HS400 modes respectively.
4. Refer SYSCTL_ESDHCCTL_CRS_0 in LS1028A RM for details.
5. HS400 mode is not supported on eSDHC1 interface.
6. GPU & LCDC can run at a maximum of 700MHz which requires CGA PLL2 to be configured for 1400MHz. In that case eSDHC will need to source clock from CGA PLL1(1500MHz).
7. Supported at VDD=0.9V

This table describes FlexSPI interface frequency calculations.

Table 52. FlexSPI interface frequency calculations

Core frequency (MHz)	Platform frequency (MHz)	DDR data rate (MT/s)	FlexSPI										Notes
							SDR Mode			DDR Mode			
			CGA_PLL selection[1]	CGA PLL Frequency (MHz)	HWA_DIV[1]	SFCK[2] (MHz)	SER CLK DIV[3]	Serial Root Clock (MHz)	XSPI_SCK	SER CLK DIV[3]	Serial Root Clock (MHz)	XSPI_SCK[4]	
1500	400	1600	1	1500	3	500	5	100	100	2	250	125	
1300	400	1600	2	1200	3	400	4	100	100	2	200	100	5
			1	1300	3	433	5	86.6	86.6	2	217	108	
			2	1000	2	500	5	100	100	2	250	125	

Table continues on the next page...

Table 52. FlexSPI interface frequency calculations (continued)

Core frequency (MHz)	Platform frequency (MHz)	DDR data rate (MT/s)	FlexSPI										Notes
							SDR Mode			DDR Mode			
			CGA_PLL selection[1]	CGA PLL Frequency (MHz)	HWA_DIV[1]	SFCK[2] (MHz)	SER CLK DIV[3]	Serial Root Clock (MHz)	XSPI_SCK	SER CLK DIV[3]	Serial Root Clock (MHz)	XSPI_SCK[4]	
1000	400	1600	1	1000	2	500	5	100	100	2	250	125	
800	300	1300	2	1000	2	500	5	100	100	2	250	125	6

Notes:

1. Selection through RCW[HWA_CGA_M1_CLK_SEL] field.
2. Clock from HWA_CGA_MUX1.
3. Refer MCR0 in LS1028A RM for details.
4. In DDR mode, FlexSPI adds an extra /2 divisor between Serial Root Clock and XSPI_SCK.
5. Choose one of 3 combinations as per the other interface (e.g. eSDHC, GPU) requirements of the system.
6. Supported at VDD=0.9V

6 Thermal recommendations

This section lists the thermal model and management of the chip.

6.1 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local NXP sales office.

6.2 Thermal system-level recommendations

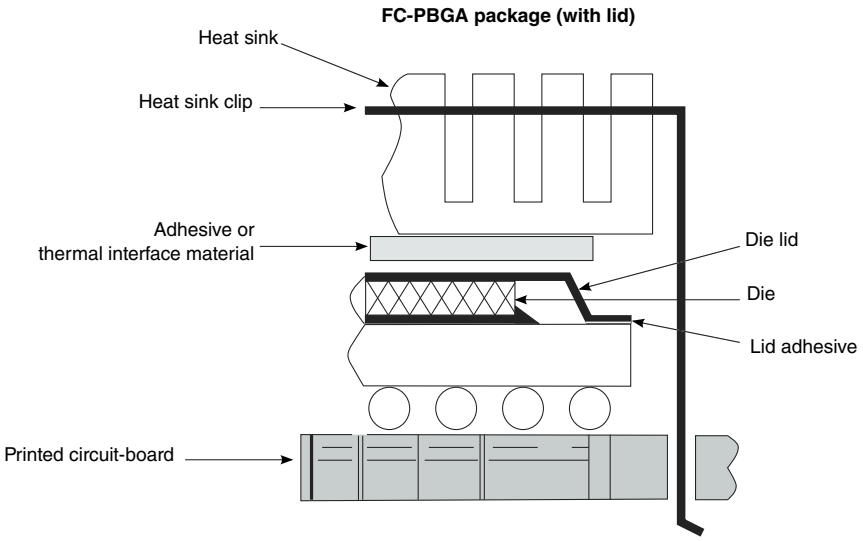
Proper thermal control design is primarily dependent on the system level design-the heat sink, airflow and thermal interface material.

Table 53. Thermal system-level checklist

Item	Completed
Use the recommended thermal model. Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local NXP sales office.	
Use this recommended board attachment method to the heat sink:[1]	

Table continues on the next page...

Table 53. Thermal system-level checklist (continued)

Item	Completed
The processor heat sink must be connected to GND at one point for EMC performance. GND here specifies processor ground.  **Figure 37. Cross-sectional view of FC PBGA with lid**	
Ensure the heat sink is attached to the printed-circuit board with the spring force centered over the package.[2]	
Ensure the spring force does not exceed 15 pounds force (65 Newtons).	
A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance.[3]	
Ensure the method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board.	
A thermal simulation is required to determine the performance in the application.[4]	

Notes:

1. The system board designer can choose among several types of commercially available heat sinks to determine the appropriate one to place on the device. Ultimately, the final selection of an appropriate heat sink depends on factors such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

2. The performance of the thermal interface materials improves with increased contact pressure; the thermal interface vendor generally provides a performance characteristic to guide improved performance.

3. The system board designer can choose among several types of commercially available thermal interface materials.

4. A Flotherm model of the part is available.

7 Revision history

This table summarizes changes to this document.

Table 54. Revision history

Revision	Date	Change
0	12/2019	Initial public release

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Document Number AN12028
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