AN12750

Enabling 10GBase-KR on QorIQ Platforms

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Document information

Information	Content
Keywords	AN12750, 10GBase, QorIQ, 10GBase-KR, QorIQ Platforms
Abstract	This application note describes 10GBase-KR link training to get optimal training parameters and the procedure to validate it.

1 Introduction to 10GBase-KR

10GBase-KR is a high-speed standard designed for backplane Ethernet applications. It is defined in *Clause 72* of *IEEE Std 802.3*. 10GBase-KR standard has a transmission bit rate of 10.3125 Gbit/s with 64B/66B line coding. Similar to other IEEE backplane Ethernet standards, 10GBase-KR also does the auto-negotiation. In addition, the 10GBase-KR standard allows link training to overcome the signal integrity challenges related to 10 Gbit/s. With the help of link training, link partners can set their electrical parameters that are optimal for channel characteristics.

The purpose of this document is to enable the backplane system at 10 Gbit/s on a system design with QorIQ family of devices. This document describes 10GBase-KR link training to get optimal training parameters and the procedure to validate it.

Note: *All the experiments and measurements shown in the document are based on LS1046A. Similar guidelines can be followed for other QorIQ devices.*

2 Link training

Auto-negotiation is vital for all Ethernet transmission having speed more than 10 Gbit/s. It is the initial stage of the physical link layer bring-up. The function of auto-negotiation is to enable link partners that share a backplane connection. It automatically chooses the suitable mode of operation which is common to both partners.

Moreover, to overcome the signal integrity challenges for optimal transmission, the second stage for link establishment is known as link training. It allows the transmitter and receiver of both link partners to optimize their parameters via data exchange. These parameters may vary for different channel losses. The process involves the transmission and reception of test frames between link partners until optimal settings are set with minimum Bit Error Rate (BER). Clock/Data Recovery (CDR) is locked with optimal settings.

Link training starts with either a default initialization value or custom value. Refer to the section, Section 5.4. Link training is successful when optimal settings of PRE cursor, POSTQ cursor, and ADAPT equalizations are set. The sections below provide more information on these equalization parameters. Updated parameters should be compliant with the requirements mentioned in **Table 72–7—Transmitter output waveform requirements related to coefficient update** and **Table 72–8—Transmitter output waveform requirements related to coefficient status** of *IEEE Std 802.3*.

3 Important parameters, registers, and bits for link optimization

Lossy channels distort the bit waveform at the receiver. It makes it difficult to sample the bit correctly. Transmitter and receiver work together during link initialization to adaptively tune transmit equalization on both ends of the link. Transmit and receive equalization help to distribute the energy of bit in such a way that a clean eye can be received to sample the bit correctly. The following sections describe the parameters, registers, and bits that can be used to perform link optimization.

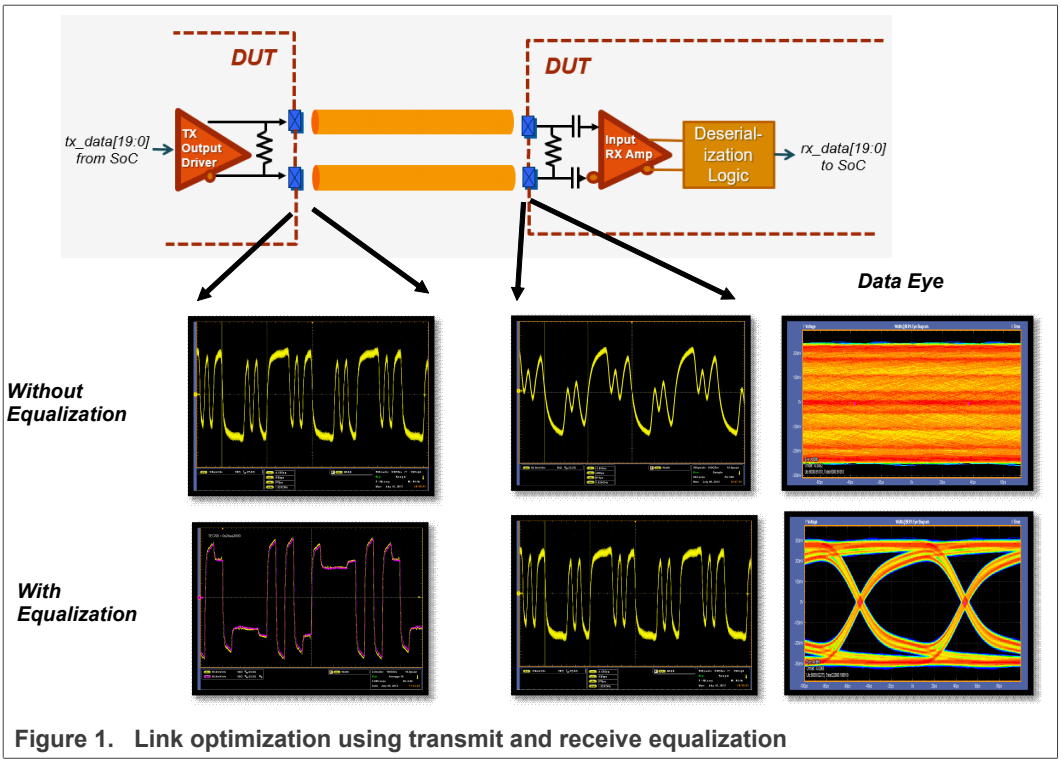


Figure 1. Link optimization using transmit and receive equalization

3.1 Transmitter side

This section describes the equalization parameters at the transmitter side. In 3-tap equalization used in 10GBase-KR, a bit signal is divided into three parts: precursor, main cursor, and postcursor. These cursors should be selected in a way that the receiver is able to recover the bitstream after the lossy channel.

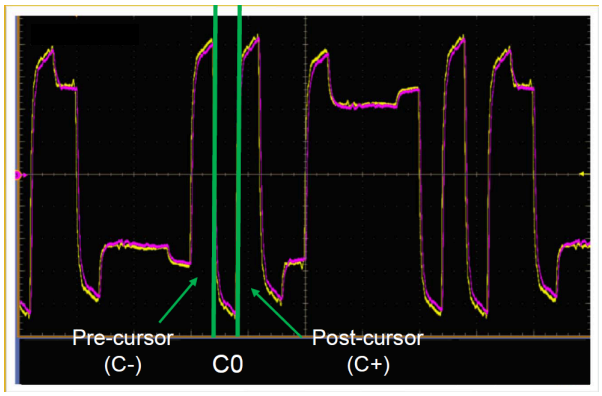


Figure 2. 3-Tap equalization signal: Pre, Main, and Post cursors

These transmit equalization parameters are used in *Clause 72 of IEEE Std 802.3*. The following table shows the nomenclature used for cursors.

Table 1. 10GBase-KR Nomenclature

Coefficients	Cursors
C(-1)	Precursor

Table 1. 10GBase-KR Nomenclature*...continued*

Coefficients	Cursors
C(0)	Main cursor
C(+1)	Postcursor

During link training, fixed-length training frames are continuously exchanged between the link device and its partner. Each frame has octets of frame maker, coefficient update, status report, and training pattern.

1. **Frame Marker (4 Octets)**: It is a 32-bit 0xFFFF_0000 pattern.
2. **Control Channel (32 Octets)**: Differential Manchester encoding is used for control channel signaling.
   - **Coefficient update**: Receiver transmits coefficient update to the transmitter of link partner for modifying cursors.
     a. Preset control: Coefficient set equalization to off. C(-1),C(+1)=0, C(0)=MAX
     b. Initialization control: Initialize coefficients
     c. Coefficient control for C(-1), C(0), C(+1): Increment, Decrement, Hold
   - **Status report**: Transmitter reports its status to link partner.
     a. Receiver ready: Status for link training completion
     b. Coefficient status for C(-1), C(0), C(+1): Maximum, Minimum, updated and not updated
3. **Training pattern (512 Octets)**: IEEE Std 802.3 recommends PRBS11 sequence. However the Linux backplane PHY driver for LS1046A uses PRBS31 sequence.

Before link training starts, coefficients must be initialized in such a way to maintain Precursor and Postcursor ratios as defined in 10GBase-KR specifications. Equalization ratios for Precursor (R_{pre}) and Postcursor (R_{post}) can be calculated from the waveform shown in the figure below. All scope shots shown in the document are run at 2.5 Gbit/s and are meant for references only. Refer **72.7.1.11 Transmitter output waveform requirements** from *IEEE Std 802.3* for details on transmitter output waveform requirements.

- $R_{pre} = V_3/V_2$
- $R_{post} = V_1/V_2$

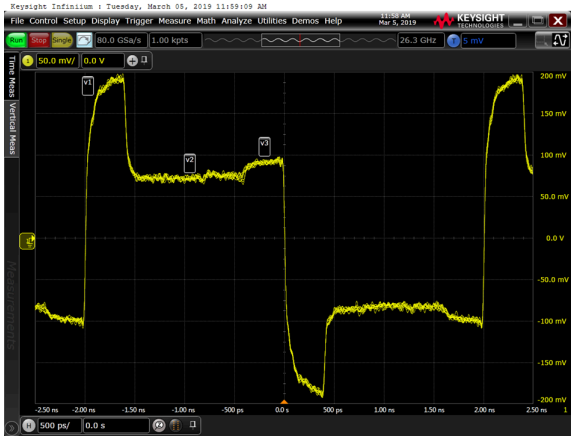


Figure 3. Pre and Post-equalization ratios

With initial parameters, coefficients get updated until optimal equalization parameters are achieved. The table below shows the cursor effects on the transmitter output waveform by incrementing/decrementing one parameter and holding other parameters. Any coefficient updates must satisfy the requirements given in **Table 72–7—Transmitter output waveform requirements related to coefficient update** and **Table 72–8—Transmitter output waveform requirements related to coefficient status** of *IEEE Std 802.3*.

Table 2. Cursor effects on waveform

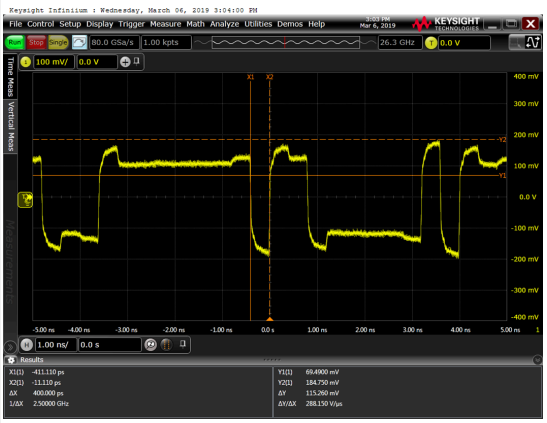
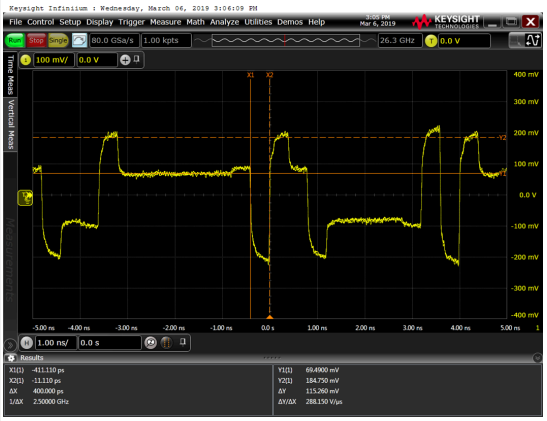
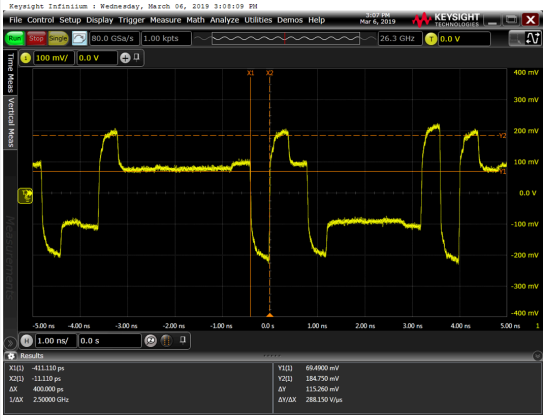
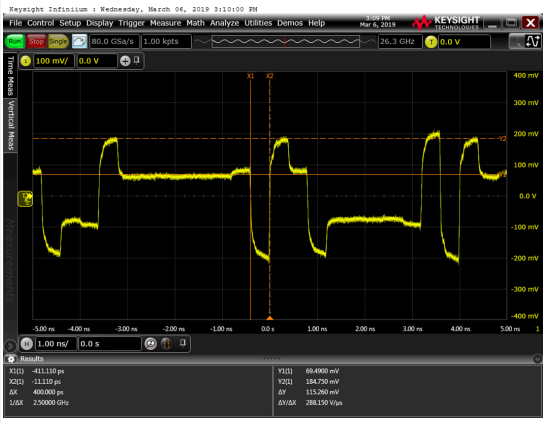
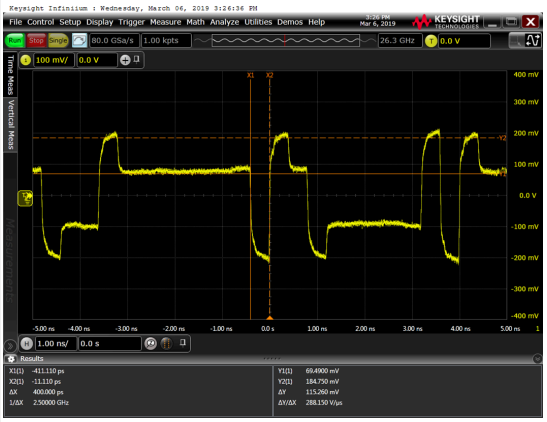
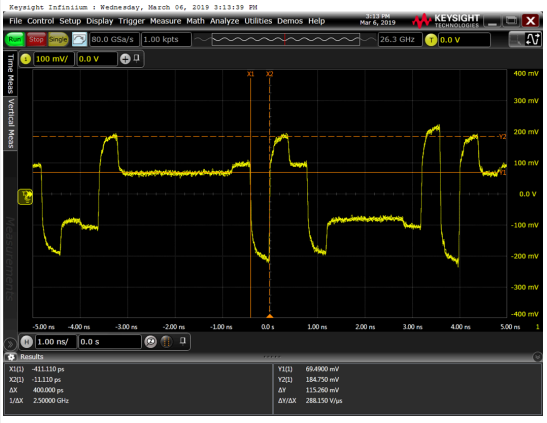
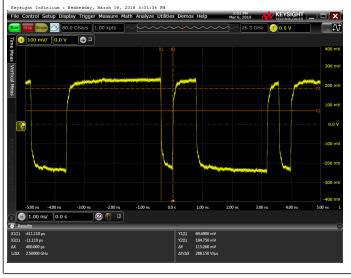
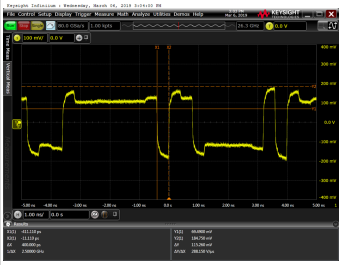
Coefficient Update			Waveform
C(+1)	C(0)	C(-1)	
Increment	Hold	Hold	
Decrement	Hold	Hold	
Hold	Increment	Hold	

Table 2. Cursor effects on waveform*...continued*

Coefficient Update			Waveform
C(+1)	C(0)	C(-1)	
Hold	Decrement	Hold	
Hold	Hold	Increment	
Hold	Hold	Decrement	

The figures below show the waveform with no equalization (PRESET), with initial 3-Tap equalization (before link training), and with optimal 3-Tap equalization (after link training):

PRESET Waveform (no equalization)	Waveform with initial equalization	Waveform with optimal equalization
		

SerDes module of QorIQ platform manages the transmit equalization parameters. Initial parameters are set through Transmit Equalization Control Register - Lane *m* (LN*m*TECR0). Transmit equalization includes the following parameters:

- TEQ_TYPE - Amount/Type of Transmit Equalization
- SGN_PREQ - Precursor sign
- RATIO_PREQ - Ratio of full swing transition bit to pre-cursor
- SGN_POST1Q - Post q Sign
- RATIO_PST1Q - Ratio of full swing transition bit to first post-cursor.
- ADPT_EQ - Transmitter Adjustments
- AMP_RED - Overall TX Amplitude Reduction

Transmit Equalization Control Register settings for 10GBase-KR:

1. **Tap equalization (TEQ_TYPE)** = 3-Tap equalization
2. **Adaptive equalization (ADPT_EQ)**= The total number of sources available as 48 by setting ADPT_EQ as 6'b11_0000.
3. **Overall TX Amplitude Reduction (AMP_RED)**

Table 3. Amplitude reduction for transmitter

Value	Adjust swing of TX signal
00_0000 (d0)	1.000 X full swing
10_0000 (d32)	1.100 X full swing

4. **Precursor**

Table 4. Pre Cursor Ratio (RATIO_PREQ)

Value	Equalization
0000 (d0)	No equalization
0001 (d1)	1.04 X relative amplitude
0010 (d2)	1.09 X relative amplitude
0011 (d3)	1.14 X relative amplitude
0100 (d4)	1.20 X relative amplitude
0101 (d5)	1.26 X relative amplitude
0110 (d6)	1.33 X relative amplitude
0111 (d7)	1.40 X relative amplitude
1000 (d8)	1.50 X relative amplitude
1001 (d9)	1.60 X relative amplitude

Table 4. Pre Cursor Ratio (RATIO_PREQ)*...continued*

Value	Equalization
1010 (d10)	1.71 X relative amplitude
1011 (d11)	1.84 X relative amplitude
1100 (d12)	2.00 X relative amplitude

Table 5. Pre Cursor Sign (SGN_PREQ)

Value	Sign
0	Negative Sign (close eye)
1	Positive Sign (open eye)

5. **Postcursor**

Table 6. Post Cursor Ratio (RATIO_PST1Q)

Value	Equalization
00000 (d0)	No equalization
00001 (d1)	1.04 X relative amplitude
00010 (d2)	1.09 X relative amplitude
00011 (d3)	1.14 X relative amplitude
00100 (d4)	1.20 X relative amplitude
00101 (d5)	1.26 X relative amplitude
00110 (d6)	1.33 X relative amplitude
00111 (d7)	1.40 X relative amplitude
01000 (d8)	1.50 X relative amplitude
01001 (d9)	1.60 X relative amplitude
01010 (d10)	1.71 X relative amplitude
01011 (d11)	1.84 X relative amplitude
01100 (d12)	2.00 X relative amplitude
01101 (d13)	2.18 X relative amplitude
01110 (d14)	2.40 X relative amplitude
01111 (d15)	2.66 X relative amplitude
10000 (d16)	3.00 X relative amplitude

Table 7. Post Cursor Sign (SGN_POST1Q)

Value	Sign
0	Negative Sign (close eye)
1	Positive Sign (open eye)

For details, refer SerDes High-Speed I/O Implementation.

All transmitter parameters should satisfy the following conditions for 10GBase-KR. These equations satisfy the constraints for coefficients mentioned in *Clause 72 of IEEE Std 802.3*.

1. 6'd26 ≤ RATIO_PREQ + ADPT_EQ + RATIO_PST1Q ≤ 6'd48
2. 4'b0000 ≤ RATIO_PREQ ≤ 4'b1000
3. 5'b0_0000 ≤ RATIO_PST1Q ≤ 5'b1_0000
4. 6'b01_1010≤ ADPT_EQ ≤ 6'b11_0000
5. RATIO_PST1Q ≥ RATIO_PREQ
6. $\frac{\text{ADPT\_EQ + RATIO\_PREQ + RATIO\_PST1Q}}{\text{ADPT\_EQ - RATIO\_PREQ - RATIO\_PST1Q}} < 4.25$

3.2 Receiver side

NXP SerDes 10G receiver circuit uses adaptive equalization. It finds best values for its RX Equalization parameters. For more information, refer LS1046ARM. (See Section 9.)

3.3 Additional information

To determine whether the SerDes channels (lanes) are in high loss condition, customers should always perform board-level simulation. In addition, use other appropriate tools (for example, SerDes Validation Tool from NXP) and/or instruments. Then adopt the best setting suitable for their end product and application. Refer to the below sections for more information regarding link optimization.

3.3.1 Transmit amplitude boost

Setting AMP_RED as 6'b10_0000 (d32) increases the overall amplitude by 1.100 X Full Swing when the channel is tending to maximum loss limit. For LS1046A, the maximum loss limit is 17 dB. These settings may be used to improve the loss margin.

3.3.2 RX equalization boost

For end-product system with low loss SerDes channels (lanes), using the default 1b setting of the RX Equalization Boost bit may adversely enhance the return loss due to some discontinuities possibly presented in the channel. This may further cause more reflection. Therefore, unless the channel is high loss, to ensure the channel's health and better performance, the 0b setting of RX Equalization Boost bit should be used for all the lanes, instead of the default 1b setting.

4 Simulation of 10GBase-KR channel

NXP provides IBIS-AMI models and users are encouraged to simulate their channel. Contact your local FAE (Field Application Engineer) or local NXP representative for details.

This section shows some simulation results with 10GBase-KR channels.

Table 8. Simulation results with 10GBase-KR channels on LS1046A

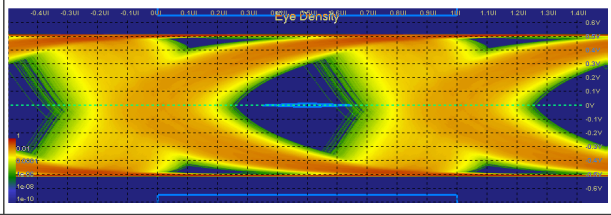
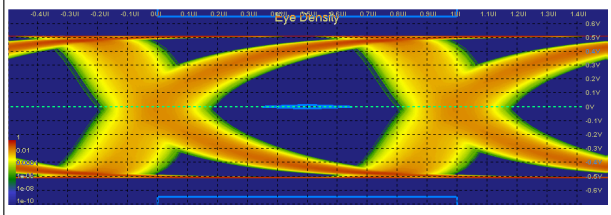
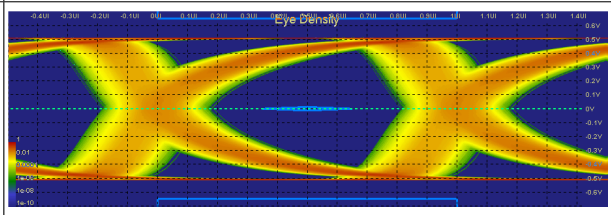
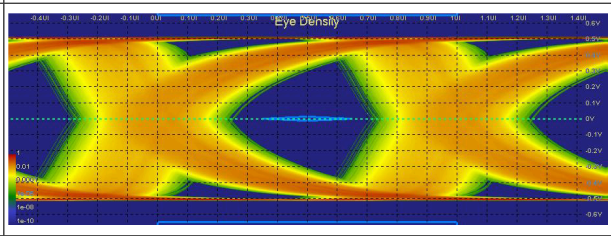
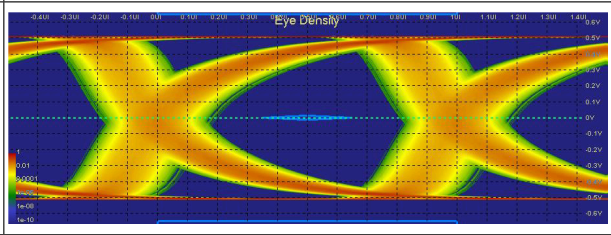
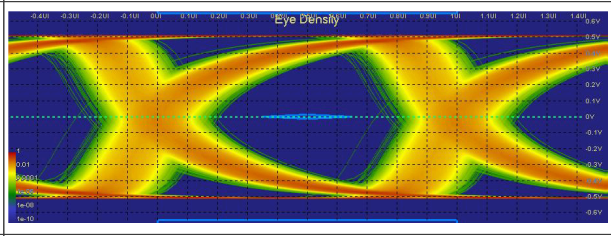
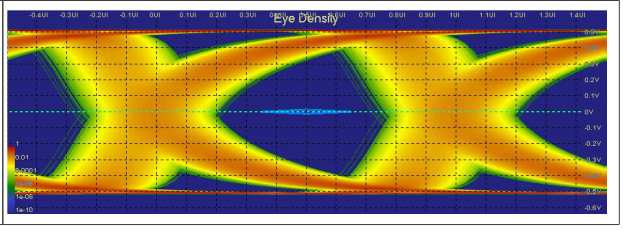
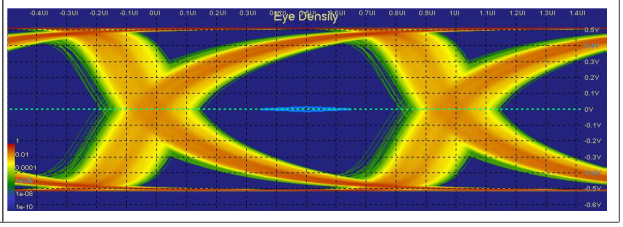
Insertion loss at the Nyquist frequency	Settings		Eye diagram
	PREQ	POST1Q	
-5 dB	3	12	
-5 dB	0	2	
-5 dB	0	0	
-9 dB	3	12	
-9 dB	0	2	
-9 dB	0	0	
-16 dB	3	12	

Table 8. Simulation results with 10GBase-KR channels on LS1046A...*continued*

Insertion loss at the Nyquist frequency	Settings		Eye diagram
	PREQ	POST1Q	
-16 dB	0	0	

5 Test setup for 10GBase-KR

This section provides the steps to enable 10GBase-KR setup on LS1046A boards back-to-back backplane connection. Similar steps are also applicable for other SoCs such as T2080 and LX2160A based boards.

5.1 LS1046A block diagram

The figure below shows two LS1046A boards connected back-to-back using backplane.

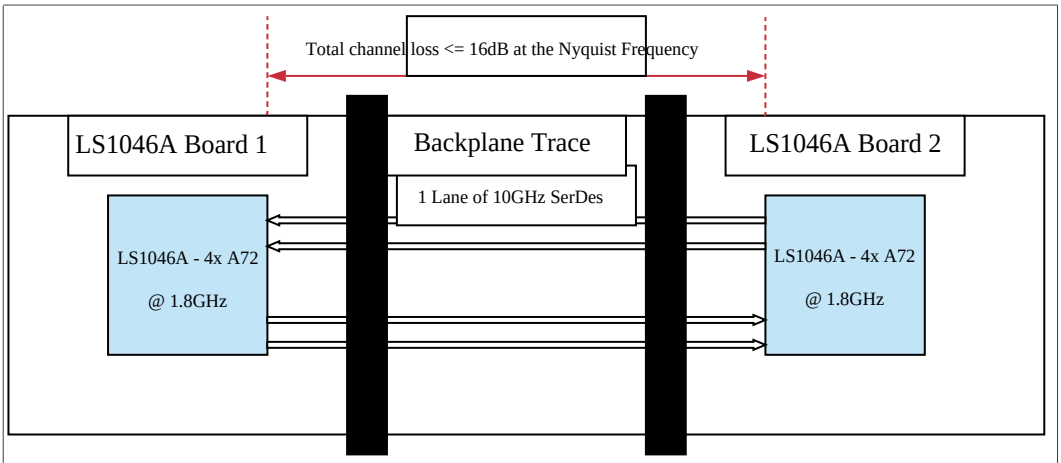


Figure 4. Backplane connection of two LS1046A boards

5.2 LS1046A RCW configuration

The below section provides steps to configure the RCW (Reset Configuration Word) on LS1046A. Refer to LS1046ARM for the SerDes protocol. (See Section 9.) Choose any valid SerDes1 option that supports XFI on one of the lanes. For example, the table below shows the configuration settings when 0x1133 SerDes1 protocol is chosen.

Table 9. Example of XFI protocol supported on SerDes1

SRDS_PRTCL_S1 RCW[128-143] (in hex)	D SD1_RX0_P/N SD1_TX0_P/N	C SD1_RX1_P/N SD1_TX1_P/N	B SD1_RX2_P/N SD1_TX2_P/N	A SD1_RX3_P/N SD1_TX3_P/N	PLL Mapping
1133	XFI.9	XFI.10	SGMII.5	SGMII.6	2211

Note: *For SerDes2, any supported protocol from LS1046ARM can be selected based on the customer requirement.*

Set the following RCW configurations:

1. SRDS_PRTCL_S1=0x1133
2. SRDS_PLL_REF_CLK_SEL_S1=0b01 (100 MHz for PLL1, 156.25 MHz for PLL2)
3. SRDS_PLL_PD_S1=0b00
4. SRDS_REFCLK_SEL_S1=0b0

5.3 U-Boot setup

All default SerDes settings are for XFI protocol. The following settings need to be modified for 10GBase-KR:

- LNmTECR0[TEQ_TYPE]
- LNmTECR0[SGN_PREQ]
- LNmTECR0[RATIO_PREQ]
- LNmTECR0[RATIO_PST1Q]
- LNmTECR0[ADPT_EQ]
- LNmTECR0[AMP_RED]

Transmit Equalization Control Register (LNmTECR0) is per lane. *m* represents the SerDes Lane. Above parameters will be updated only for those XFI SerDes lanes which need to configure as 10GBase-KR. For details on LNmTECR0 parameters, refer to Section 3.1.

Below is the U-Boot command to reconfigure LNmTECR0:

```
mw.l <LNmTECR0_address> <LNmTECR0_hex_value>
```

As per the chosen SerDes protocol on LS1046A, XFI.9 is on Lane D of SerDes1 with LNmTECR0 at offset 0x8D8:

```
mw.l 0x1ea08d8 0x0020ad24
```

Note: *LNmTECR0 is in big endian format in LS1046A.*

Table 10. LNmTECR0 register fields

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RSVD		TEQ_ TYPE		RSVD	SGN_ PREQ	RATIO_PREQ				SGN_ POST1Q	RATIO_PST1Q				
0	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**0**	**1**
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
RSVD		ADPT_EQ						RSVD		AMP_RED					
0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Table 11. 10GBASE-KR default values for LNmTECR0

Field	Description
TEQ_TYPE	2b10 - 3 Levels of TX Equalization (+1 pre-cursor and +1 post-cursor)

Table 11. 10GBASE-KR default values for LNmTECR0*...continued*

Field	Description
SGN_PREQ	1b1 - Positive Sign (open eye)
RATIO_PREQ	4b0010 - 1.09 X relative amplitude
SGN_POST1Q	1b1 - Positive Sign (open eye)
RATIO_PST1Q	5b0_1101 – 2.18 X relative amplitude
ADPT_EQ	6b10_0000 - Transmitter Adjustments (32 sources)
AMP_RED	6b00_0000 - 1.000 X Full Swing

Refer to the section ***Enabling backplane PHY driver*** of ***AN12572*** for reconfiguring LNmTECR0 in Linux. (See Section 9.)

5.4 LS1046A 10GBase-KR initialization settings

This section describes the initialization settings for 10GBase-KR to be implemented on LS1046A. The default transmit equalization settings are shown in the Table 11.

Other suggested initialization settings for different channel loss values are shown in the table below.

Table 12. Channel loss

-5 dB channel loss at the Nyquist frequency						
Type	**PreCursor sign**	**PreCursor ratio**	**PostCursor sign**	**PostCursor ratio**	**Adaptive equalization**	**Amplitude reduction**
0x2	0x1	0x2	0x1	0x2	0x20	0x0
0x2	0x1	0x2	0x1	0x7	0x20	0x0
0x2	0x1	0x2	0x1	0x9	0x20	0x0
-11 dB channel loss at the Nyquist frequency						
Type	**PreCursor sign**	**PreCursor ratio**	**PostCursor sign**	**PostCursor ratio**	**Adaptive equalization**	**Amplitude reduction**
0x2	0x1	0x4	0x1	0x8	0x20	0x0
0x2	0x1	0x2	0x1	0xB	0x20	0x0
0x2	0x1	0x3	0x1	0xC	0x20	0x0
-13 dB channel loss at the Nyquist frequency						
Type	**PreCursor sign**	**PreCursor ratio**	**PostCursor sign**	**PostCursor ratio**	**Adaptive equalization**	**Amplitude reduction**
0x2	0x1	0x2	0x1	0xA	0x20	0x0
0x2	0x1	0x6	0x1	0xA	0x20	0x0
0x2	0x1	0x5	0x1	0xB	0x20	0x0
-16 dB channel loss at the Nyquist frequency						
Type	**PreCursor sign**	**PreCursor ratio**	**PostCursor sign**	**PostCursor ratio**	**Adaptive equalization**	**Amplitude reduction**
0x2	0x1	0x5	0x1	0xD	0x1E	0x0

Table 12. Channel loss*...continued*

0x2	0x1	0x4	0x1	0xB	0x1D	0x0
0x2	0x1	0x6	0x1	0xB	0x1D	0x0

Note: *The SerDes receiver interface of LS1046A for 10GBase-KR can only support up to 17 dB of channel loss. Refer* ***A-004985: SerDes receiver high-speed data path is short in gain*** *in LS1046A Chip Errata for details. (See Section 9.)*

6 Verifying the equalization parameters using SerDes Validation Tool

NXP provides the QCVS SerDes validation tool as part of CodeWarrior Development Studio for Network Applications. The tool helps in testing of transmitter and receiver of SerDes with customized equalization parameters. Refer to *AN5119* for information about SerDesConfiguration and Validation Tool. (See Section 9.) This document details the procedure for setting Transmitter and Receiver parameters, sending BIST patterns and seeing CDR lock and bit error at the receiver.

6.1 LS1046A boards – back to back setup

This section describes the procedure to test optimal settings on LS1046A back to back setup. See Figure 4. Here, SerDes1 Lane D is used.

1. Open QCVS tool on CodeWarrior separately for both boards.
2. Set Board 1 configuration.

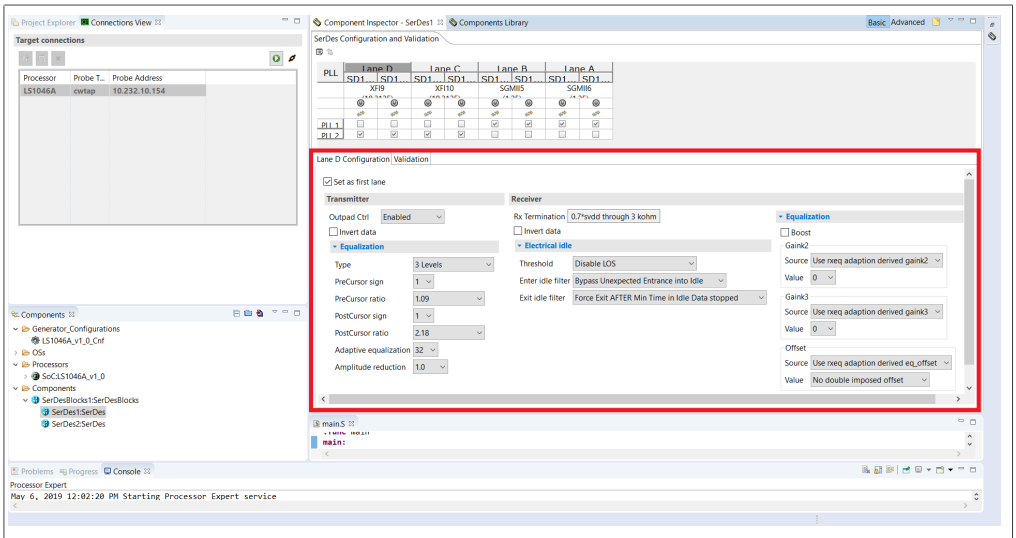


Figure 5. Board 1 configuration

3. Set Board 2 configuration.

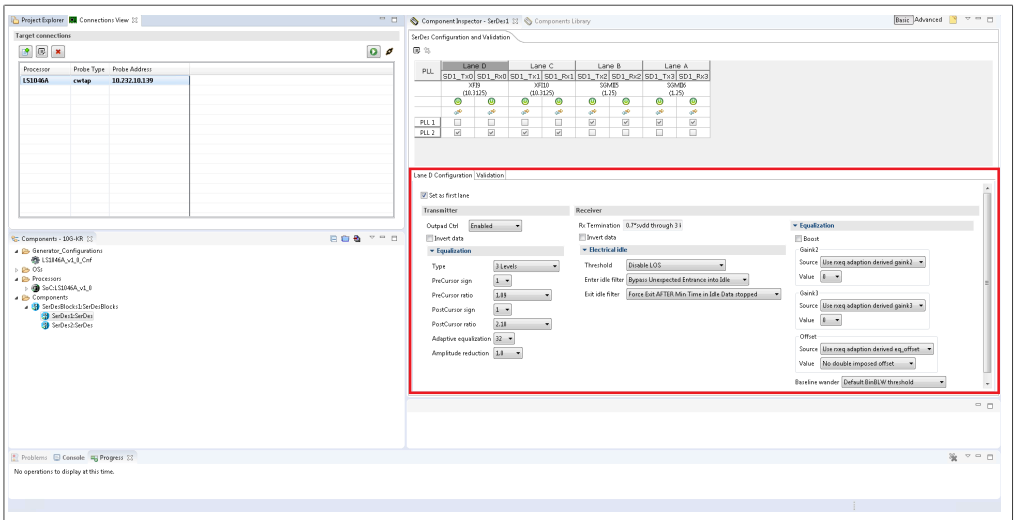


Figure 6. Board 2 configuration

4. To transmit from Board 1, start PSSPR pattern.

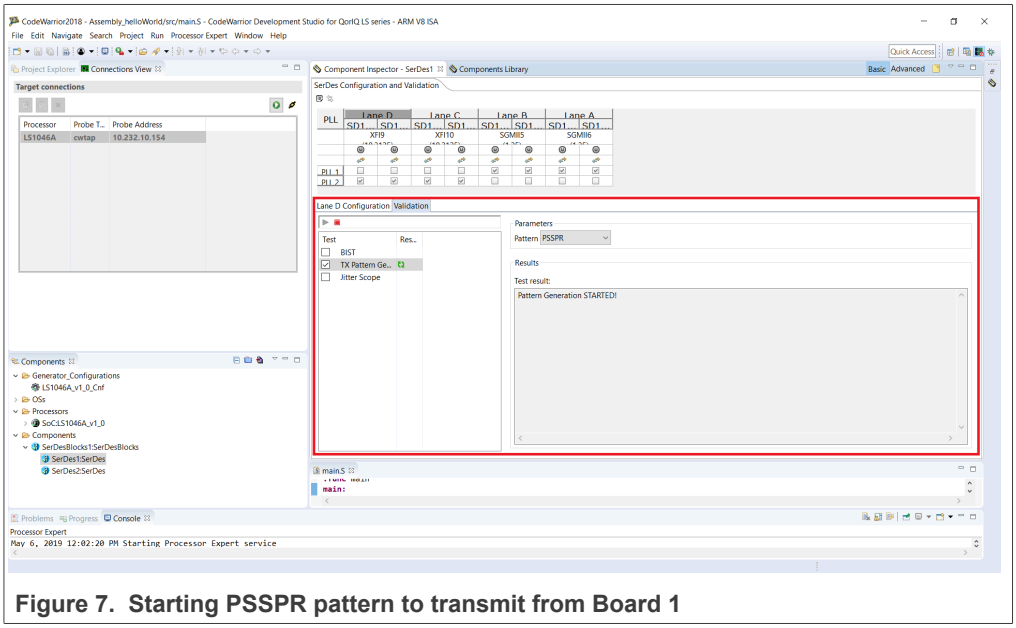


Figure 7. Starting PSSPR pattern to transmit from Board 1

5. Run BIST test on Board 2 to see CDR lock and BIST error count. With acceptable BER, optimal settings for equalization parameters can be determined.

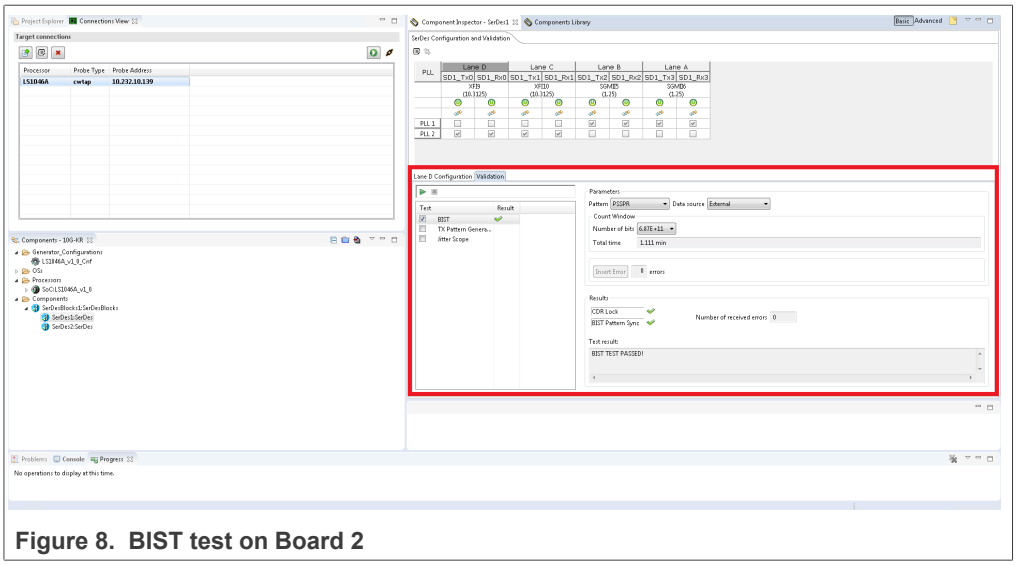


Figure 8. BIST test on Board 2

7 Testing 10GBase-KR channel

This section describes the various steps for testing channel robustness for 10GBase-KR channel.

7.1 Forward error correction (FEC)

Transmitting data on the lossy channel might introduce errors. Enabling FEC can help fixing errors at the Physical Coding Sublayer (PCS).

On LS1046A, you can enable FEC through XFI AN Advertisement 2 (XFI_AN_ADVERT2) register.

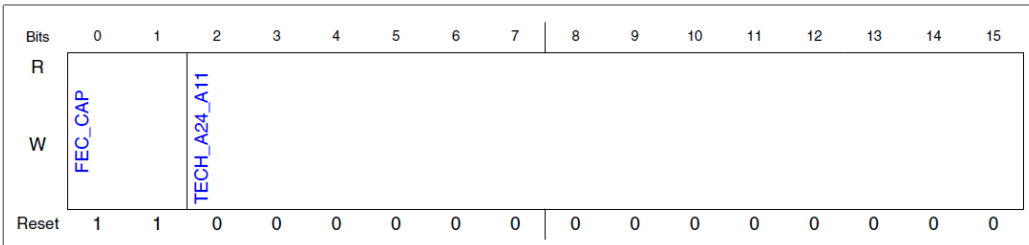


Figure 9. XFI AN Advertisement 2 (XFI_AN_ADVERT2)

FEC Capability (FEC_CAP [0:1])

00b - Device is not capable of or requesting FEC.

11b - Device is capable of and requesting FEC support.

7.2 Netperf

Netperf is a benchmark tool for measuring performance numbers of the network. For details, refer https://linux.die.net/man/1/netperf.

Use netperf to attain maximum 10 Gbit/s performance on 10G Ethernet link. Here, `netperf_test_client.sh` and `netperf_test_server.sh` run on LS1046A boards.

1. On client side, run the below command:

```
$ bash +x netperf_test_client.sh -b 10g -f common -p tcp -t
 RR_FFSSPPPH_1133_5559
```

2. On server side, run the below command:

```
$bash +x netperf_test_server.sh -b 10g -f common -t
 RR_FFSSPPPH_1133_5559
```

The general purpose of the netperf test is to create streams for each core. For example, LS1046A has four cores. So the script configures four IP addresses for single 10G interfaces. Then starts four netperf servers to listen on those four IP addresses as shown by the following commands:

```
$netserver -L 1.0.0.1
$netserver -L 2.0.0.1
$netserver -L 3.0.0.1
$netserver -L 4.0.0.1
Starting netserver with host '4.0.0.1' port '12865' and family
 AF_UNSPEC
Starting netserver with host '1.0.0.1' port '12865' and family
 AF_UNSPEC
Starting netserver with host '2.0.0.1' port '12865' and family
 AF_UNSPEC
Starting netserver with host '3.0.0.1' port '12865' and family
 AF_UNSPEC
```

On the client side, the steps are similar as on the server side. The script also configures four IP addresses for single 10G interface. Then start the four netperf sessions to test with bidirectional traffic (TCP_STREAM and TCP_MAERTS) for testing.

```
$netperf -Cc -H 1.0.0.1 -l 60 -t TCP_STREAM -T 0,0 -P 0 -B
 "outbound" &
$netperf -Cc -H 2.0.0.1 -l 60 -t TCP_MAERTS -T 1,1 -P 0 -B
 "inbound" &
$netperf -Cc -H 3.0.0.1 -l 60 -t TCP_STREAM -T 2,2 -P 0 -B
 "outbound" &
$netperf -Cc -H 4.0.0.1 -l 60 -t TCP_MAERTS -T 3,3 -P 0 -B
 "inbound" &
```

Results:

```
===start!===
===frame size is default===
=======Start Date: Thu Apr 26 14:17:53 UTC 2018=======
It is tcp STREAM connect to 4.0.0.1 bind to cpu 0 !!
It is tcp MAERTS connect to 1.0.0.1 bind to cpu 1 !!
It is tcp STREAM connect to 2.0.0.1 bind to cpu 2 !!
It is tcp MAERTS connect to 3.0.0.1 bind to cpu 3 !!
87380 16384 16384 60.00 1097.61 79.24 79.15 23.658 23.629
 outbound
87380 16384 0 60.00 5203.84 79.25 79.15 4.990 4.984 inbound
87380 16384 16384 60.00 5246.56 79.24 79.15 4.949 4.944
 outbound
```

```
87380 16384 0 60.00 952.96 79.21 79.13 27.237 27.209 inbound
===frame size is default===
===inbound===
6.1568Gbps
===outbound===
6.34417Gbps
===sum is===
12.501Gbps
===frame size is default===
=======End Date: Thu Apr 26 14:18:53 UTC 2018=======
===end!===
```

7.3 Ethtool

Ethtool is the utility of Linux for controlling network drivers and hardware. For details, refer https://linux.die.net/man/8/ethtool.

After running a network benchmark performance tool, information on packets and errors can be seen through using the following command:

```
ethtool -S <network-device>
```

Following is the display log:

```
root@ls1046ardb:~# ethtool -S fm1-mac9
```

Below is the NIC statistics:

```
interrupts [CPU 0]: 8930
interrupts [CPU 1]: 8930
interrupts [CPU 2]: 8931
interrupts [CPU 3]: 8931
interrupts [TOTAL]: 35722
rx packets [CPU 0]: 5364
rx packets [CPU 1]: 3565
rx packets [CPU 2]: 5367
rx packets [CPU 3]: 3569
rx packets [TOTAL]: 17865
tx packets [CPU 0]: 5321
tx packets [CPU 1]: 1708
tx packets [CPU 2]: 5717
tx packets [CPU 3]: 5111
tx packets [TOTAL]: 17857
tx recycled [CPU 0]: 0
tx recycled [CPU 1]: 0
tx recycled [CPU 2]: 0
tx recycled [CPU 3]: 0
tx recycled [TOTAL]: 0
tx confirm [CPU 0]: 3566
tx confirm [CPU 1]: 5365
tx confirm [CPU 2]: 3564
tx confirm [CPU 3]: 5362
tx confirm [TOTAL]: 17857
tx S/G [CPU 0]: 0
tx S/G [CPU 1]: 0
tx S/G [CPU 2]: 0
tx S/G [CPU 3]: 0
tx S/G [TOTAL]: 0
```

```
rx S/G [CPU 0]: 0
rx S/G [CPU 1]: 0
rx S/G [CPU 2]: 0
rx S/G [CPU 3]: 0
rx S/G [TOTAL]: 0
tx error [CPU 0]: 0
tx error [CPU 1]: 0
tx error [CPU 2]: 0
tx error [CPU 3]: 0
tx error [TOTAL]: 0
rx error [CPU 0]: 0
rx error [CPU 1]: 0
rx error [CPU 2]: 0
rx error [CPU 3]: 0
rx error [TOTAL]: 0
bp count [CPU 0]: 84
bp count [CPU 1]: 91
bp count [CPU 2]: 81
bp count [CPU 3]: 87
bp count [TOTAL]: 343
rx dma error: 0
rx frame physical error: 0
rx frame size error: 0
rx header error: 0
rx csum error: 0
qman cg_tdrop: 0
qman wred: 0
qman error cond: 0
qman early window: 0
qman late window: 0
qman fq tdrop: 0
qman fq retired: 0
qman orp disabled: 0
congestion time (ms): 0
entered congestion: 0
congested (0/1): 0
```

8 T2080 10GBase-KR initialization settings

This section describes the initialization settings for 10GBase-KR to be implemented on T2080. The default transmit equalization settings are shown in Table 11.

Other suggested initialization settings for different channel loss values are shown in the Table 13.

Table 13. Transmit equalization parameters at different channel loss

-7 dB channel loss at the Nyquist frequency						
Type	**PreCursor sign**	**PreCursor ratio**	**PostCursor sign**	**PostCursor ratio**	**Adaptive equalization**	**Amplitude reduction**
0x2	0x1	0x2	0x1	0x7	0x20	0x0
0x2	0x1	0x1	0x1	0x5	0x22	0x0
0x2	0x1	0x2	0x1	0x6	0x1A	0x0
-9 dB channel loss at the Nyquist frequency						

Table 13. Transmit equalization parameters at different channel loss...*continued*

Type	PreCursor sign	PreCursor ratio	PostCursor sign	PostCursor ratio	Adaptive equalization	Amplitude reduction
0x2	0x1	0x2	0x1	0x8	0x1A	0x0
0x2	0x1	0x2	0x1	0x6	0x20	0x0
0x2	0x1	0x2	0x1	0x4	0x22	0x0
-11 dB channel loss at the Nyquist frequency						
Type	**PreCursor sign**	**PreCursor ratio**	**PostCursor sign**	**PostCursor ratio**	**Adaptive equalization**	**Amplitude reduction**
0x2	0x1	0x3	0x1	0x5	0x1A	0x0
0x2	0x1	0x2	0x1	0x8	0x1C	0x0
0x2	0x1	0x2	0x1	0xB	0x20	0x0
-15 dB channel loss at the Nyquist frequency						
Type	**PreCursor sign**	**PreCursor ratio**	**PostCursor sign**	**PostCursor ratio**	**Adaptive equalization**	**Amplitude reduction**
0x2	0x1	0x4	0x1	0x6	0x1A	0x0
0x2	0x1	0x1	0x1	0x8	0x1D	0x0
0x2	0x1	0x3	0x1	0x7	0x20	0x0

9 References

The table below lists additional resources that can be referred for additional information.

Table 14. Reference documentation and tools

ID	Name of related collateral/ information to refer	Location
IEEE Std 802.3	IEEE Standard for Ethernet (*Clause 72.* Physical Medium Dependent sublayer and baseband medium, type 10GBASE-KR)	standards.ieee.org
LS1046ARM	QorIQ LS1046A Reference Manual	www.nxp.com
AN5252	LS1046A Design Checklist	www.nxp.com
LS1046A CE	LS1046A Chip Errata	Contact your FAE / local NXP representative
AN12572	Ethernet Backplane Driver Support Application Note	www.nxp.com
AN5119	SerDes Configuration and Validation Tool Companion Application Note	www.nxp.com
	High-Speed SERDES Modeling for the PCB and System Environment	www.nxp.com
	QCVS SerDes Tool User Guide	www.nxp.com
	QCVS Getting Started Guide	www.nxp.com

10 Revision history

The table below summarizes the revisions to this document.

Revision history

Revision	Date	Change description
Rev. 0	06/2020	Initial public release.
Rev. 1	07/2022	Added Section 8.

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