CAUTION

The processor's minimum and maximum SYSCLK and core/platform/DDR frequencies must not be exceeded, regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/platform/DDR frequency should use only down-spreading to avoid violating the stated limits.

3.7.3 Real-time clock timing (RTC)

The real-time clock timing (RTC) input is sampled by the platform clock. The output of the sampling latch is then used as an input to the Watchdog, Flextimer, 1588 Timer and snvs unit; there is no need for jitter specification. The minimum period of the RTC signal should be greater than or equal to 16x the period of the platform clock with a 50% duty cycle. There is no minimum RTC frequency; RTC may be pulled to ground, if not needed.

3.7.4 Gigabit Ethernet reference clock timing

This table provides the Ethernet gigabit reference clock DC electrical characteristics with LV_{DD} = 2.5 V / 1.8 V.

Table 17. EC*n*_GTX_CLK125 DC electrical characteristics (LV_{DD} = 2.5 V / 1.8 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	—	—	V	2
Input low voltage	V_{IL}	—	—	0.2 x LV_{DD}	V	2
Input capacitance	C_{IN}	—	—	6	pF	—
Input current (V_{IN} = 0 V or V_{IN} = LV_{DD})	I_{IN}	—	—	± 50	μA	3

Notes:

1. For recommended operating conditions, see Table 4.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max V_{IN} values found in Table 4.
3. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 4.

This table provides the Ethernet gigabit reference clock AC timing specifications.

Table 18. EC*n*_GTX_CLK125 AC timing specifications [1]

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC*n*_GTX_CLK125 frequency	f_{G125}	125 - 100 ppm	125	125 + 100 ppm	MHz	—
EC*n*_GTX_CLK125 cycle time	t_{G125}	--	8	--	ns	—
EC*n*_GTX_CLK125 rise and fall time	t_{G125R}/t_{G125F}	—	—	0.75	ns	2
EC*n*_GTX_CLK125 duty cycle 1000Base-T for RGMII	t_{G125H}/t_{G125}	40	—	60	%	3

Notes:

1. At recommended operating conditions with LV_{DD} = 1.8 V ± 90mV / 2.5 V ± 125 mV. See Table 4.
2. Rise times are measured from 20% of LV_{DD} to 80% of LV_{DD}. Fall times are measured from 80% of LV_{DD} to 20% of LV_{DD}.
3. EC*n*_GTX_CLK125 is used to generate the GTX clock for the Ethernet transmitter. See RGMII AC timing specifications for duty cycle for the 10Base-T and 100Base-T reference clocks.

3.7.5 DDR clock (DDRCLK)

This section provides the DDRCLK DC electrical characteristics and AC timing specifications.

3.7.5.1 DDRCLK DC electrical characteristics

This table provides the DDRCLK DC electrical characteristics.

Table 19. DDRCLK DC electrical characteristics[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	—	—	V	1
Input low voltage	V_{IL}	—	—	0.3 x OV_{DD}	V	1
Input capacitance	C_{IN}	—	7	12	pF	—
Input current (V_{IN}= 0V or V_{IN} = OV_{DD})	I_{IN}	—	—	± 50	μA	2

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 4.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 4.
3. At recommended operating conditions with OV_{DD} = 1.8 V. See Table 4.

3.7.5.2 DDRCLK AC timing specifications

This table provides the DDRCLK AC timing specifications.