## Table of Contents



## Revision History

| Rev | |
|---|---|
| X1 | Draft revision for interposer(LS1043A) and LS1046A |
| A | Formal release revA board for interposer (LS1043A) and LS1046A. |
| B | 1. Changed low cost power solution.<br>2. Update the power jack(J3) symbol and correct the connection.<br>3. Update miniPCIe(J501) connector.<br>4. Change U20 to AQR107.<br>5. R237 changed to 1.5Kohm.<br>6. R953 added on 2V1 EN pin.<br>7. Updated R650 to 4.7Kohm, R655 to 1.5Kohm.<br>8. Add J502 for the 2nd chassis fan power.<br>9. Swap J24 and J25 silkscreen.<br>10. Changed R936 to 27.4Kohm.<br>11. Removed R515, R516 and R519 PD at CMS of 10G RJ45(J5).<br>12. Changed C818, C777, C862 and C878 to 3300PF.<br>13. Changed C756, C744, C838, C832, C732, C735, and C737 to 150-79454.<br>14. Changed Q5 to PSMN2R4-30YLD.<br>15. Added R954 and C1193 for 10G RJ45 CMS channel.<br>16. Updated S1VDD&X1VDD net name to SVDD and XVDD.<br>17. As AQR107 ES1 errata, add some PU/PD resistors, R972-R961, R963-R957. |
| B1 | 1. Changed R676 to 18.2K, C1185 to 1nF.<br>2. R69 changed to DNP and R70 changed to populated.<br>3. Add a note on page14. Need disconnect I2C1 bus to J7.<br>4. Update U520 to V8 part number to match with real board. |
| B2 | 1. Changed CPU to LS1046ASE8T1A<br>2. Changed U20 to AQR107-B0-EG-Y. |
| BX1 | 1. Changed U20 to AQR113C-B0-C.<br>2. Changed U15 from MX25V4006EM1I-13G to AT45DB041E-SSHN2B-B<br>3. Removed XGT1588_CLK_P/N, not used for AQR113C<br>4. Connected AQR113C SMB_CLK/DAT to I2C1 with 0ohm and DNP<br>5. Changed U520 from MC34VR500V8ES to MC34VR500VCES, SW1 output change from 0.85V to 0.7V<br>6. Added LT3065 (U524) to supply AQR113C 1.8V VDD_IO<br>7. Changed R552 from 60.4K to 40.2K to change U12 output from 1.2V to 1.0V<br>8. Changed R550 from 150K to 140K to change U13 output from 2.1V to 2.0V<br>9. Changed TVDD supply from 2.5V to 1.8V<br>10. Changed EMI2_MDC/MDIO pull-up from 2.5V to 1.8V<br>11. Added 0ohm DNP to disconnect I2C1 interface from J7 to incorporate errata<br>12. Replaced obsolete eMMC U508 MTFC4GACAAAM-1M WT with MTFC4GACAJCN-1M WT<br>13. Replaced obsolete NAND U40 MT29F4G08ABBEAH4:E with MT29F4G08ABBFAH4-IT:F<br>14. Replaced obsolete load switch U3, U6 NX5P2190UKZ with NX5P3090UK<br>15. Replaced obsolete CLK Buffer U30, U31 831724AKILFT with 9DML0441AKILF<br>16. Replaced obsolete EEPROM U32 CAT24C05YI-GT3 with CAT24C04WI-G<br>17. Replaced obsolete OSC Y500 FN2500152 with ASV-25.000MHZ-EJ-T<br>18. Populated R754, DNP R758 to update PCB revision |
| C | Final release with updates in BX1 revision |

## Revisions

| Rev | Description | Date | Approved |
|---|---|---|---|
| X1 | Original Release | Dec 23, 2015 | Tom Sun |
| A | Formal Release | Mar 4, 2016 | Matt Carlson |
| B | Changed power solution | Apr 28, 2016 | Tom Sun |
| B1 | Update as bringup | Aug 8, 2016 | Tom Sun |
| B2 | Change CPU to 1.8GHz on LS1046ARDB-PB board. | Feb 24, 2017 | Tom Sun |
| BX1 | Change 10G PHY from AQR107 to AQR113C Replace obsolete parts | Jan 7, 2021 | Paul Gan |
| C | Rev C final Release | Mar 19, 2021 | Paul Gan |



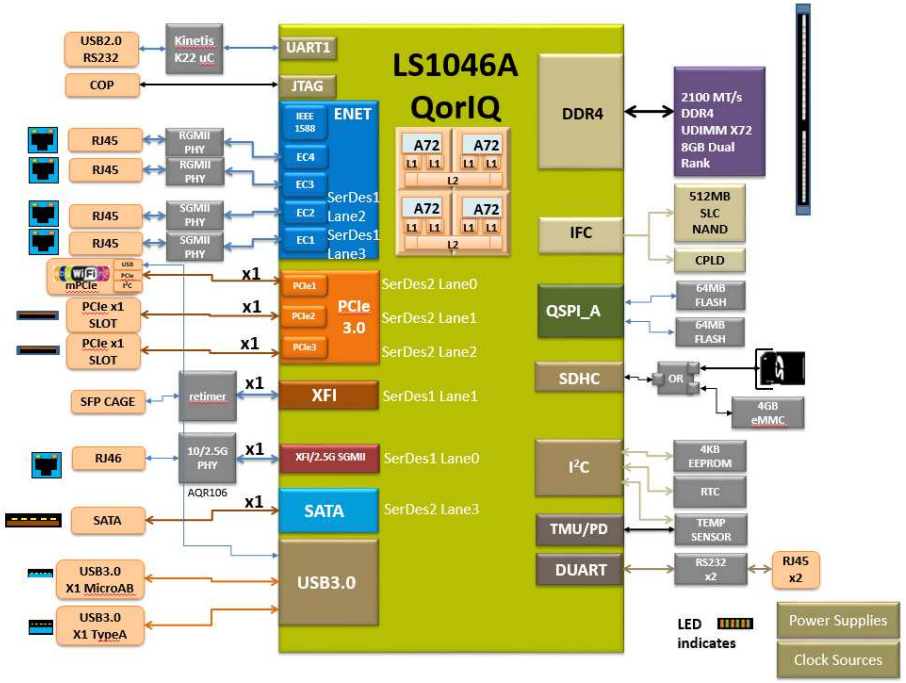
# LS1046ARDB-PB

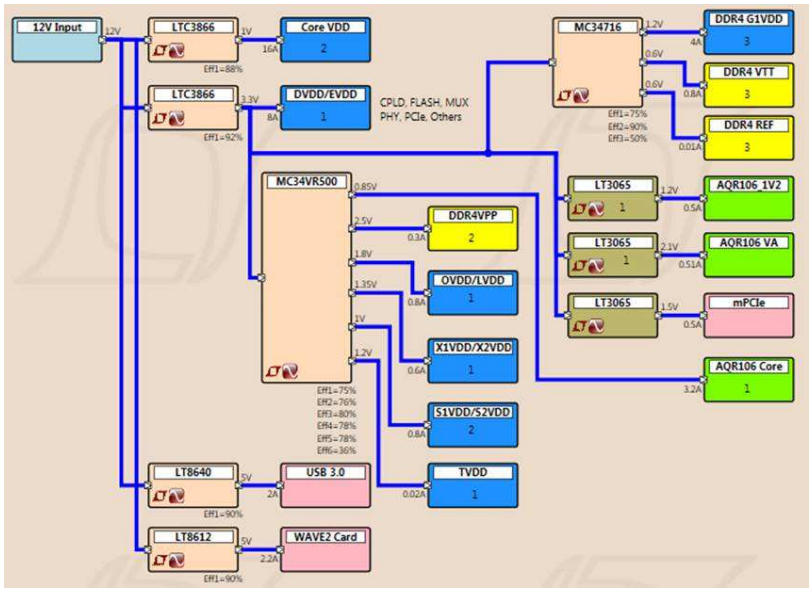

Digital Networking Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598




Classification: Public

| | | | |
|---|---|---|---|
| Designer: Paul Gan | Drawing Title: LS1046ARDB-PB | | |
| Drawn by: Paul Gan | Page Title: COVER PAGE | | |
| Approved: Tom Sun | Size C | Document Number SCH-29142 PDF: SPF-29142 | Rev C |
| | Date: Friday, March 19, 2021 | Sheet 1 of 24 | |




## Default Switch Setting

| *REF DES* | *SWITCH(DEFAULT)* | *PAGE NAME* |
|---|---|---|
| SW5 | 1~8: 00100010 | PAGE18-CPLD & DIP SW |
| SW4 | 1~8: 00111011 | PAGE18-CPLD & DIP SW |
| SW3 | 1~8: 01000110 | PAGE18-CPLD & DIP SW |
| SW2 | OFF | PAGE21-PS (5V&PA&MISC) |

## Default Jumper Setting

| *REF DES* | *JUMPER(DEFAULT)* | *PAGE NAME* |
|---|---|---|
| J26 | 1-2 | PAGE06-CMSIS-DAP |
| J14 | 1-2 | PAGE24-USB |
| J19 | 1-2 | PAGE15-SERDES &PCIE&SATA |
| J18 | 1-2 | PAGE20-CPU POWER (VDD&GND&NC) |
| J30 | 1-2 | PAGE21-PS (5V&PA&MISC) |
| J29 | 7-8 | PAGE21-PS (5V&PA&MISC) |

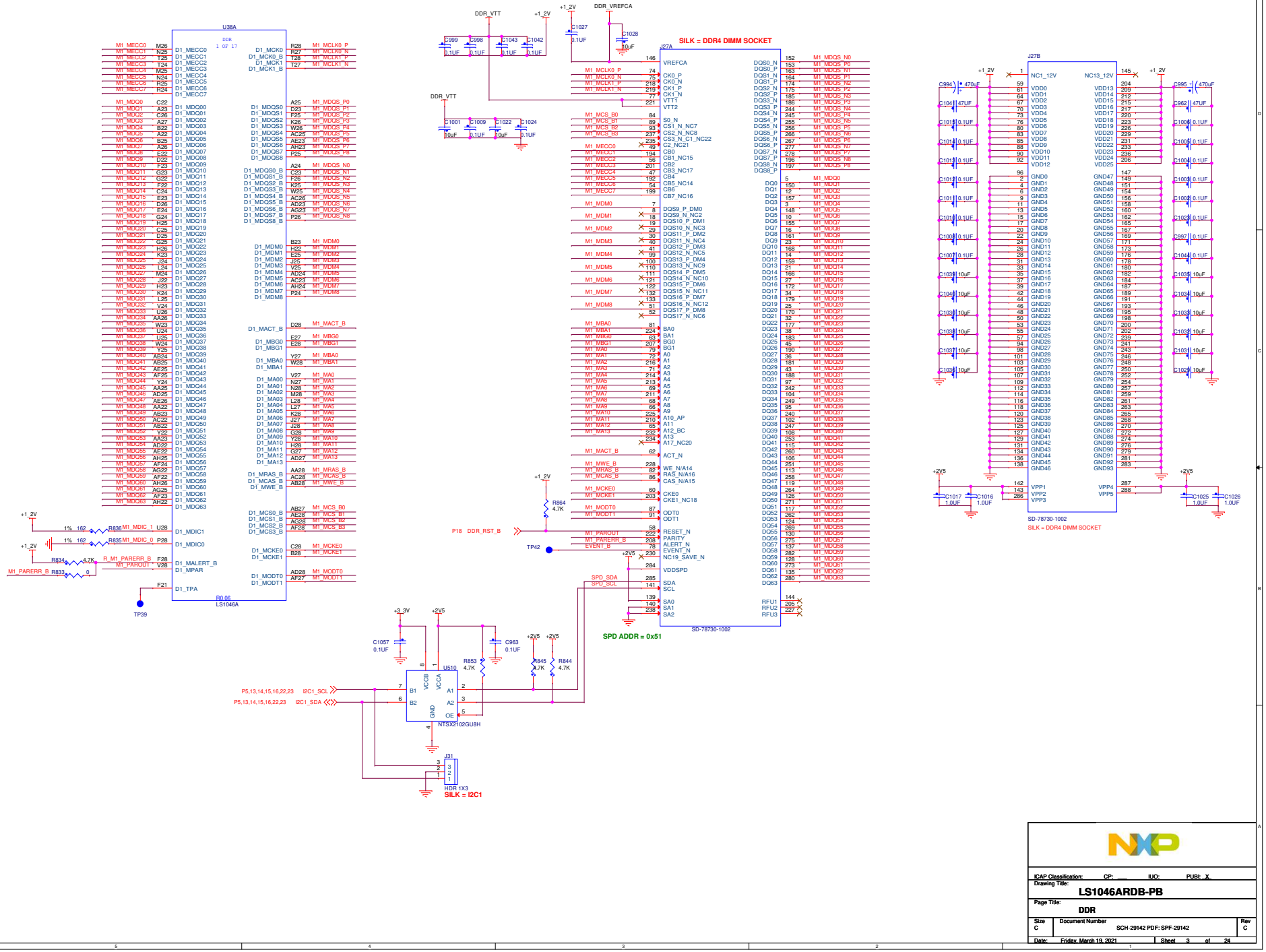
ICAP Classification: CP: ___ IUO: PUBL X

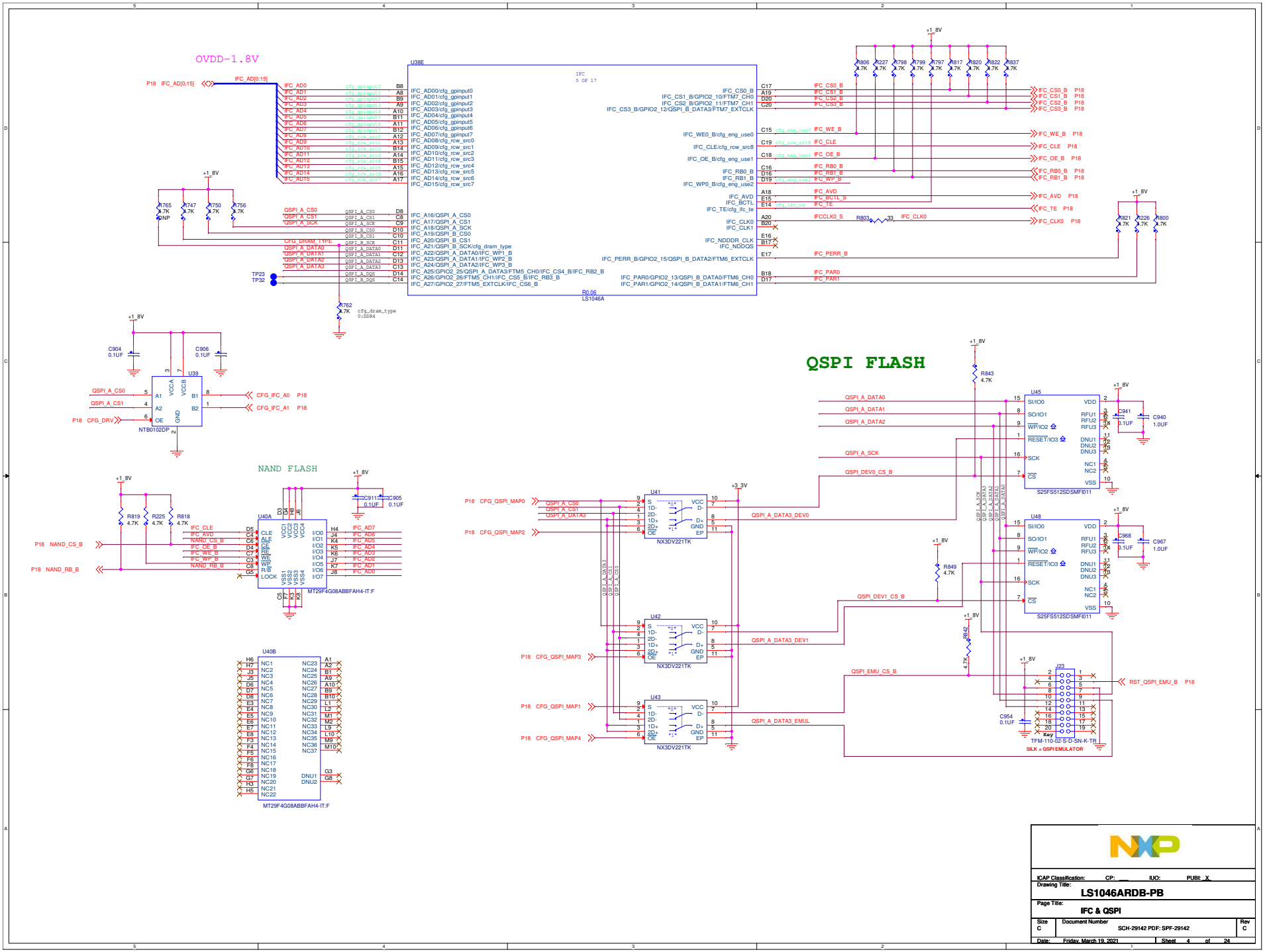
Drawing Title: **LS1046ARDB-PB**

Page Title: **NOTES**

| Size | Document Number | Rev |
|---|---|---|
| C | SCH-29142 PDF: SPF-29142 | C |

Date: Friday, March 19, 2021 Sheet 2 of 24


U38A
DDR
1 OF 17
SILK = DDR4 DIMM SOCKET
J27A
SD-78730-1002
SPD ADDR = 0x51
J27B
SD-78730-1002
SILK = DDR4 DIMM SOCKET
U10
NTSX2102GU8H
J31
HDR 1X3
SILK = I2C1
TP39
TP42
R0.06
LS1046A
ICAP Classification:
CP:
IUO:
PUBI: X
Drawing Title:
LS1046ARDB-PB
Page Title:
DDR
Size
C
Document Number
SCH-29142 PDF: SPF-29142
Rev
C
Date:
Friday, March 19, 2021
Sheet
3
of
24

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|---|---|---|---|
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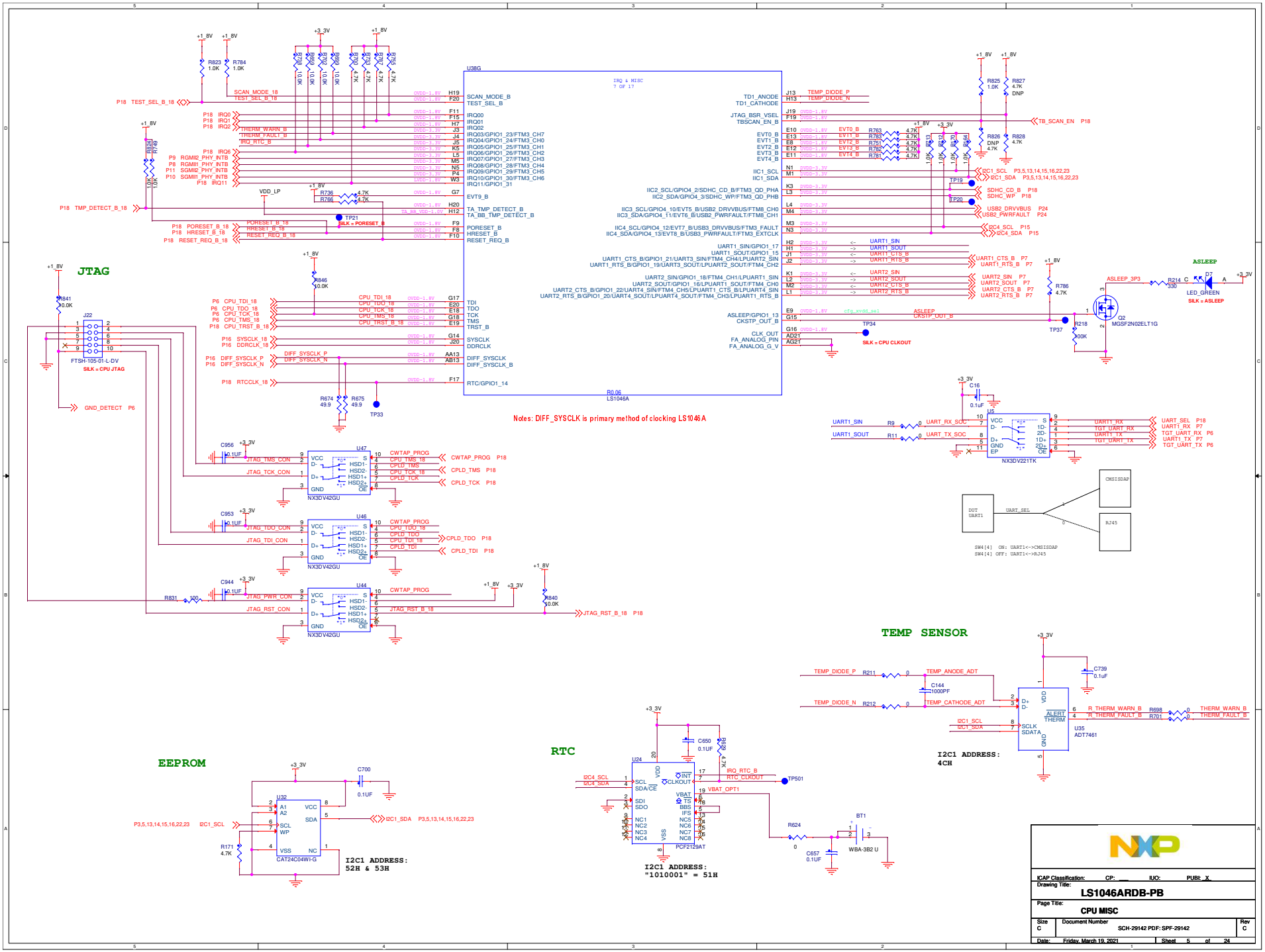
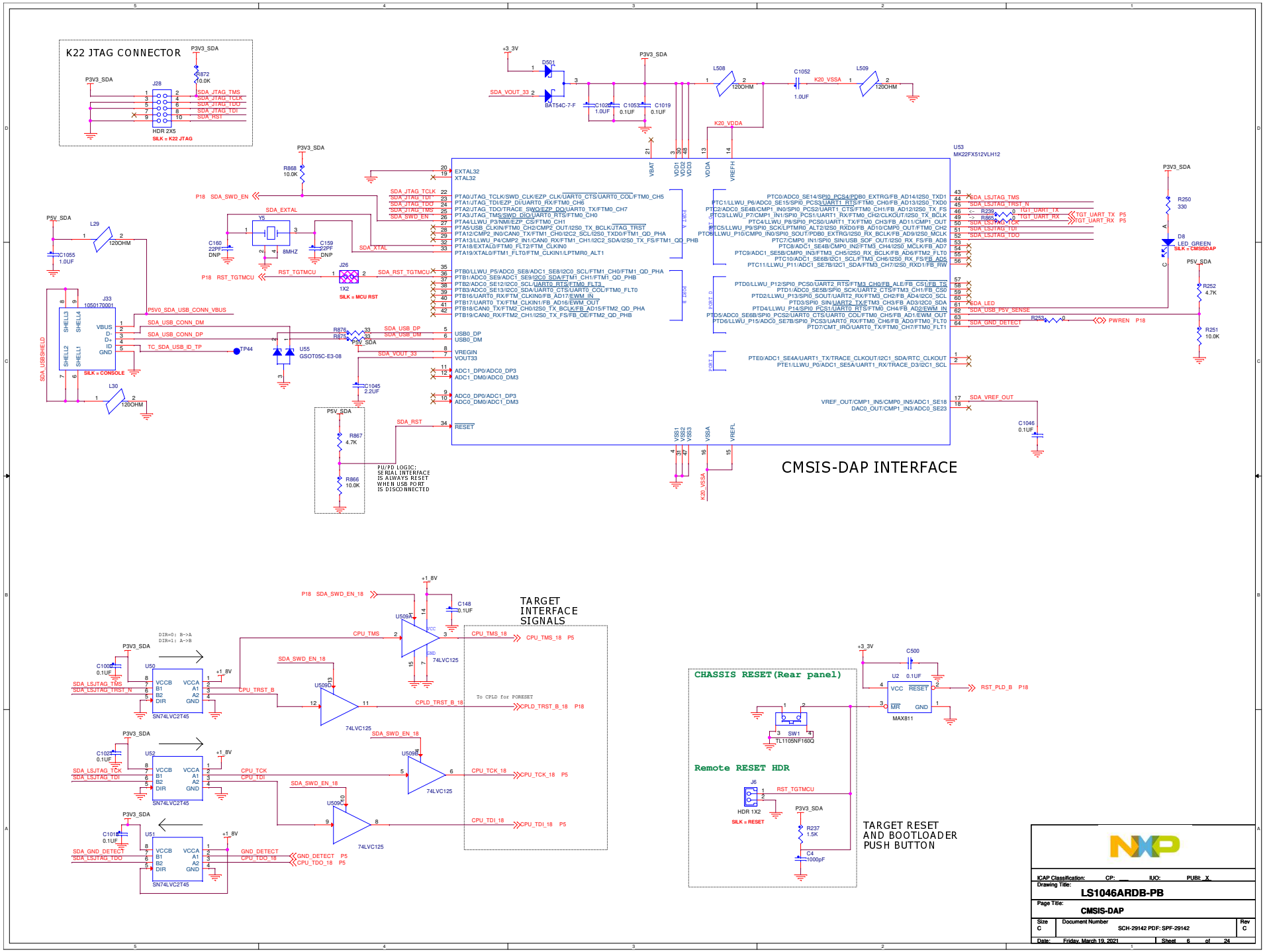
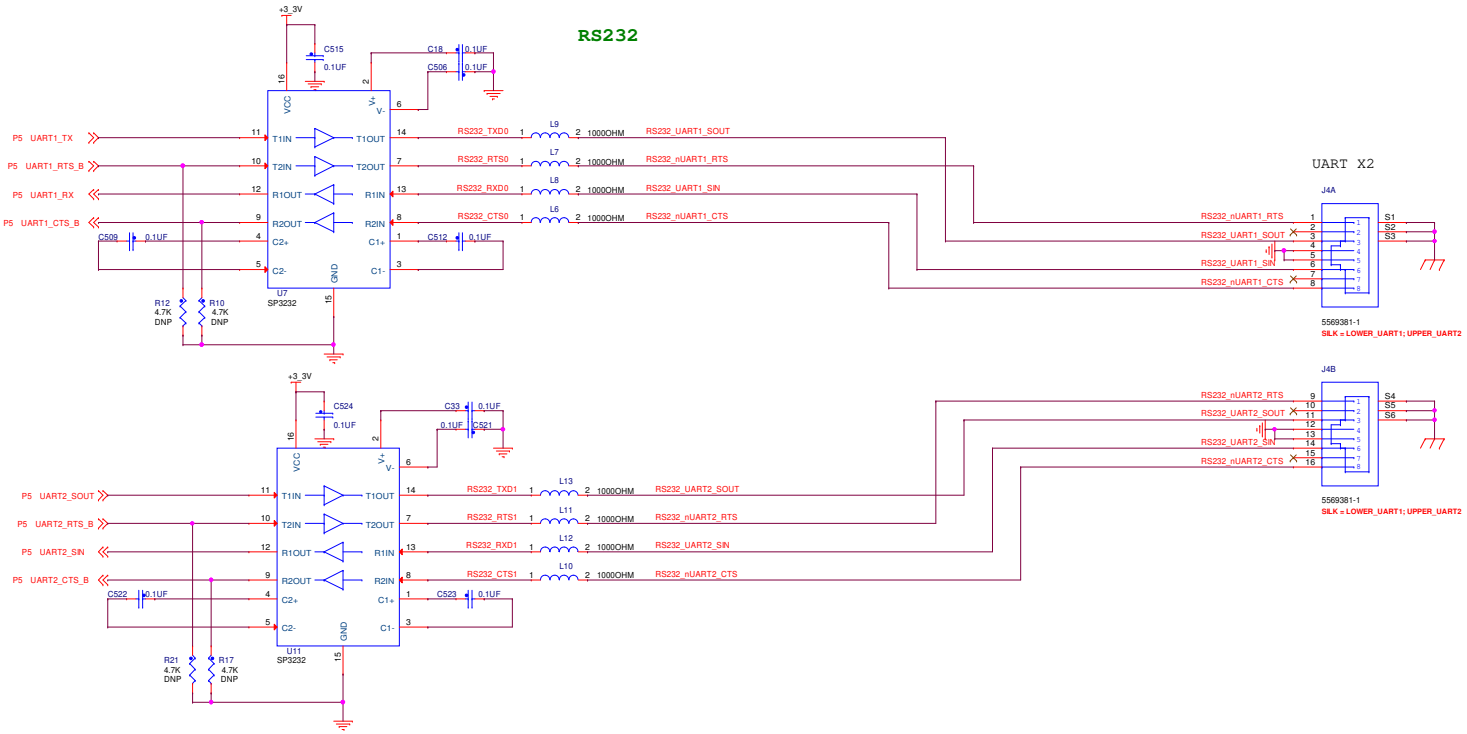
| Drawing Title: | LS1046ARDB-PB | | |
| Page Title: | IFC & QSPI | | |
| Size: C | Document Number: SCH-29142 PDF: SPF-29142 | | Rev: C |
| Date: Friday, March 19, 2021 | | Sheet 4 of 24 | |


JTAG
EEPROM
RTC
TEMP SENSOR
U38G
LS1046A
Notes: DIFF_SYSCLK is primary method of clocking LS1046A
SILK = CPU JTAG
SILK = PORESET_B
SILK = CPU CLKOUT
SILK = ASLEEP
I2C1 ADDRESS: 52H & 53H
I2C1 ADDRESS: "1010001" = 51H
I2C1 ADDRESS: 4CH
LS1046ARDB-PB
CPU MISC
SCH-29142 PDF: SPF-29142
Friday, March 19, 2021


K22 JTAG CONNECTOR
CMSIS-DAP INTERFACE
TARGET INTERFACE SIGNALS
CHASSIS RESET(Rear panel)
Remote RESET HDR
TARGET RESET AND BOOTLOADER PUSH BUTTON
LS1046ARDB-PB
CMSIS-DAP
SCH-29142 PDF: SPF-29142
Friday, March 19, 2021

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|---|---|---|
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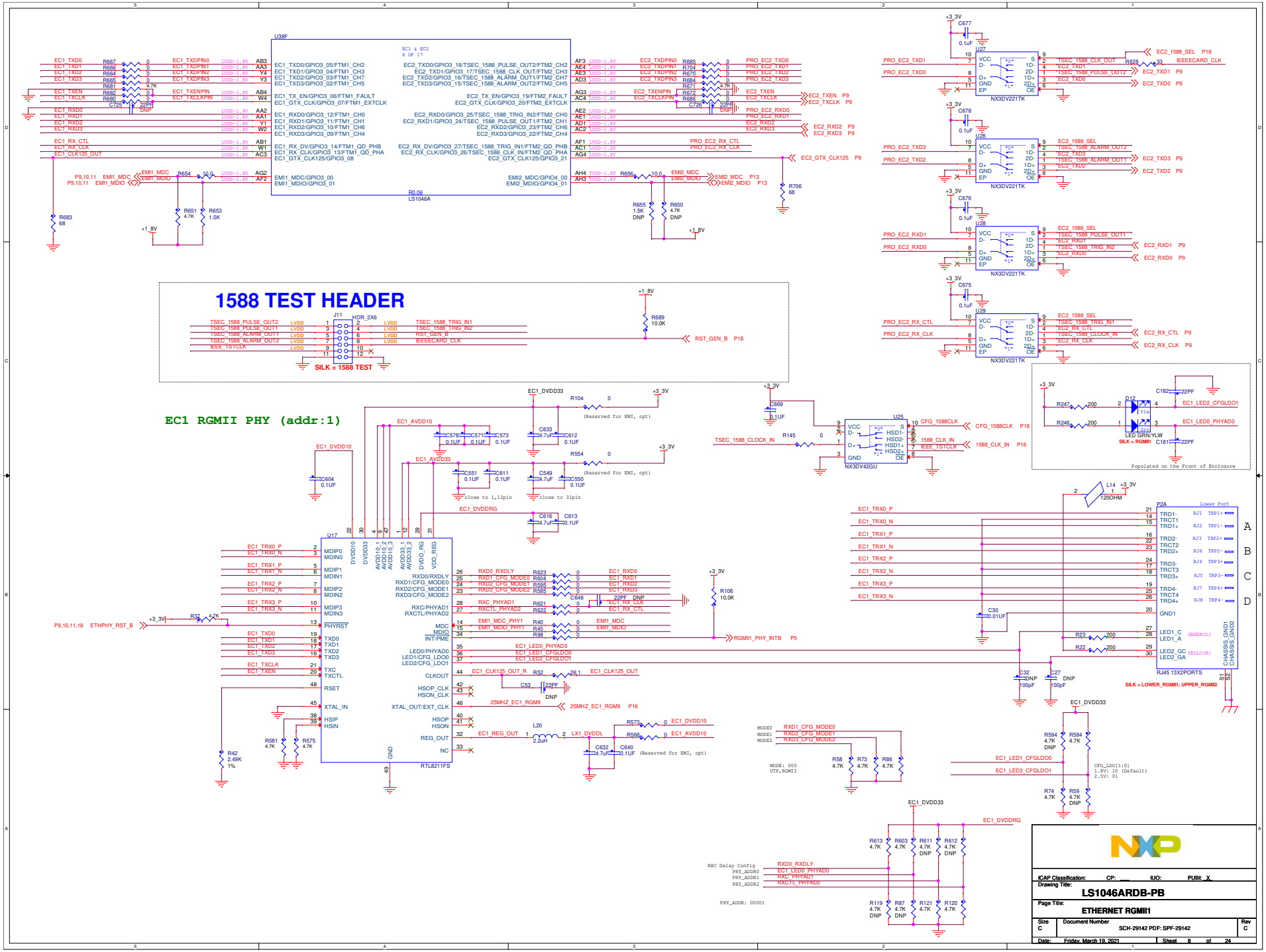
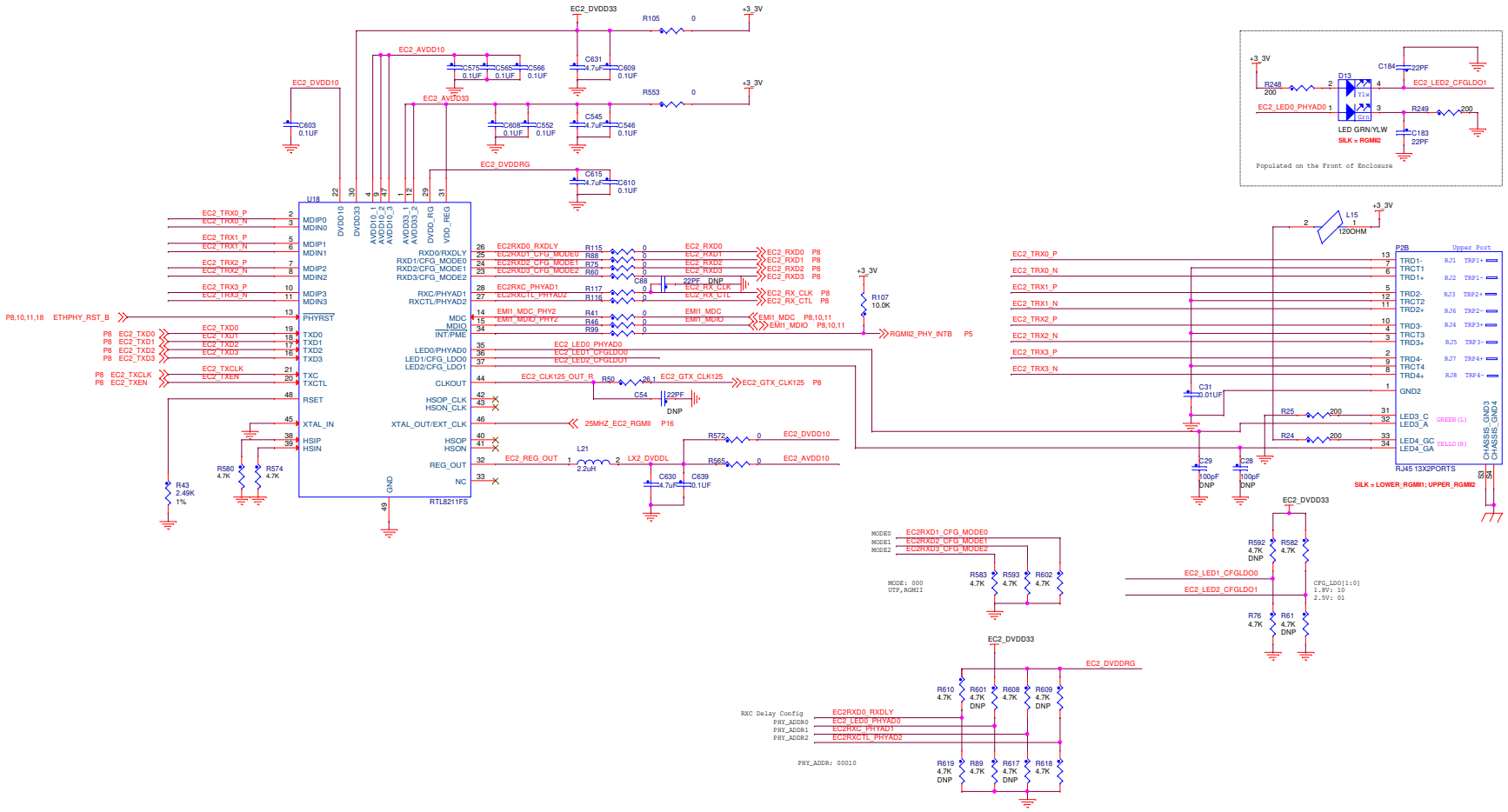
| Drawing Title: | LS1046ARDB-PB | |
| Page Title: | UART | |
| Size: C | Document Number: SCH-29142 PDF: SPF-29142 | Rev: C |
| Date: Friday, March 19, 2021 | Sheet 7 of 24 | |


1588 TEST HEADER
SILK = 1588 TEST
EC1 RGMII PHY (addr:1)
LS1046ARDB-PB
ETHERNET RGMII1
SCH-29142 PDF: SPF-29142
Friday, March 19, 2021
Sheet 8 of 24

# EC2 RGMII PHY (addr:2)

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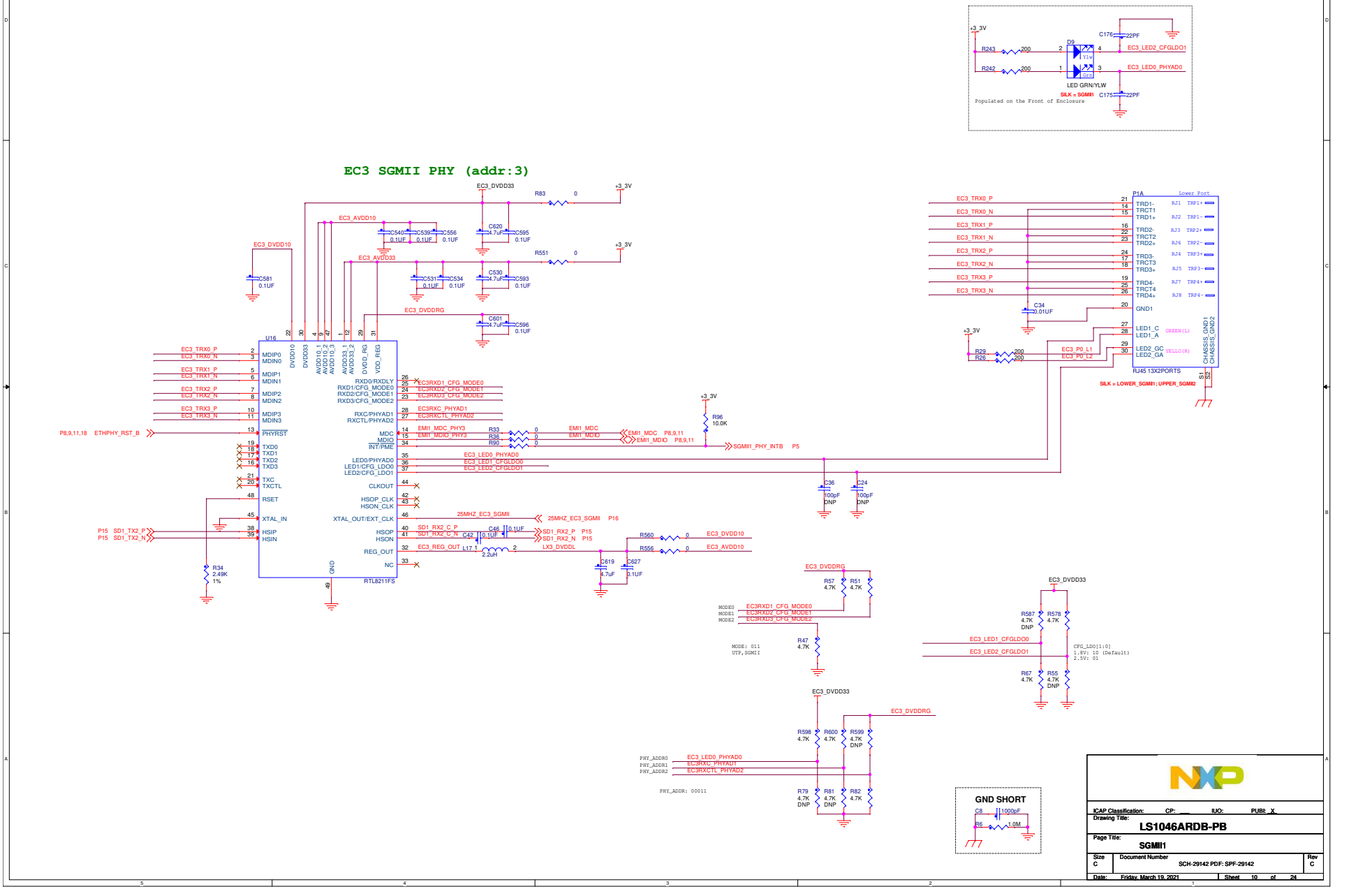
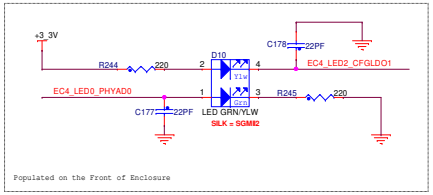
|---|---|---|---|
| ICAP Classification: | CP: ___ | IUO: | PUBL: X |
| Drawing Title: | LS1046ARDB-PB | | |
| Page Title: | ETHERNET RGMII2 | | |
| Size: C | Document Number: SCH-29142 PDF: SPF-29142 | | Rev: C |
| Date: Friday, March 19, 2021 | | Sheet 9 of 24 | |

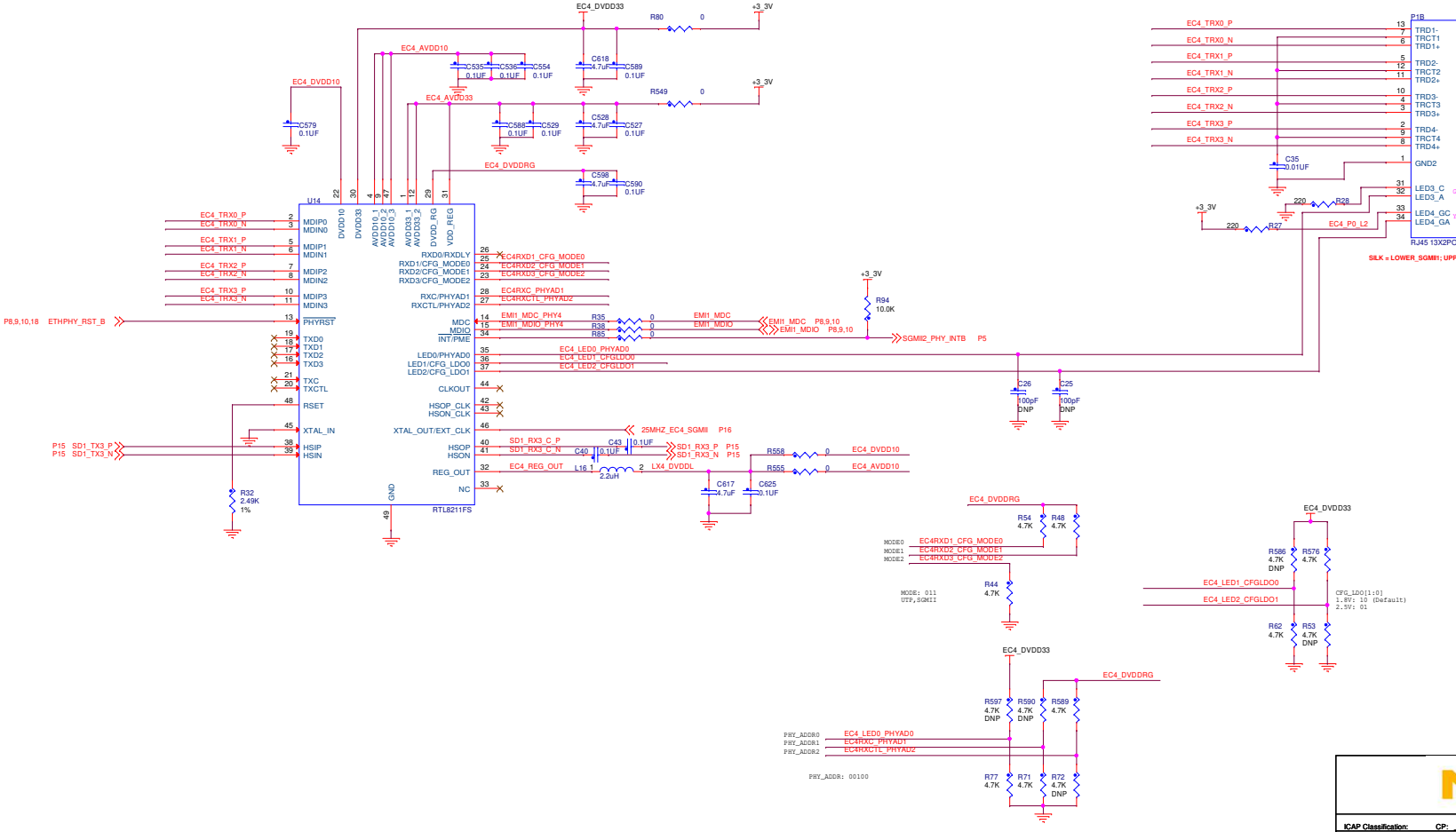
# SGMII1 PHY ETHERNET



# SGMII2 PHY ETHERNET




## EC4 SGMII PHY (addr:4)

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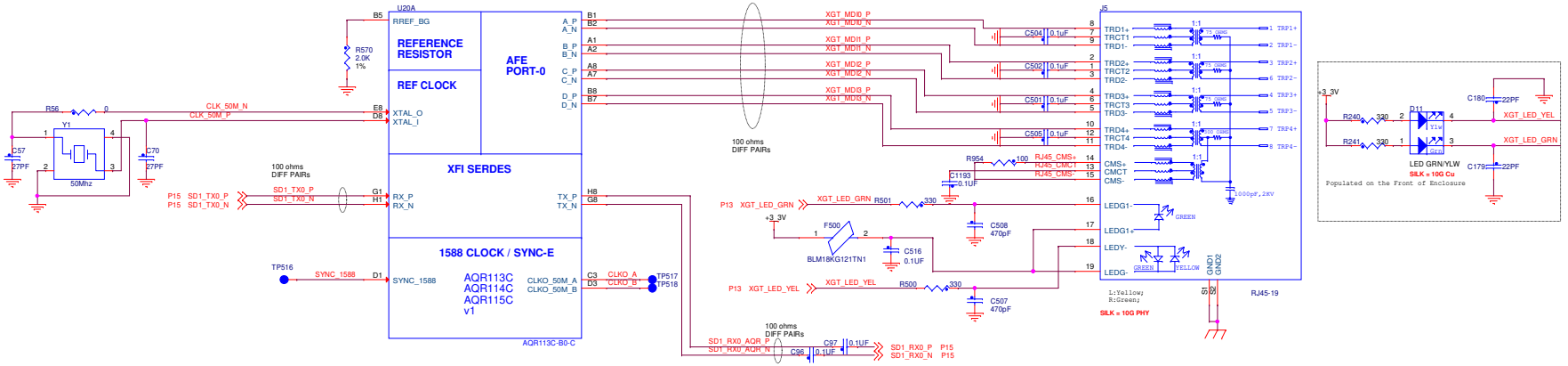
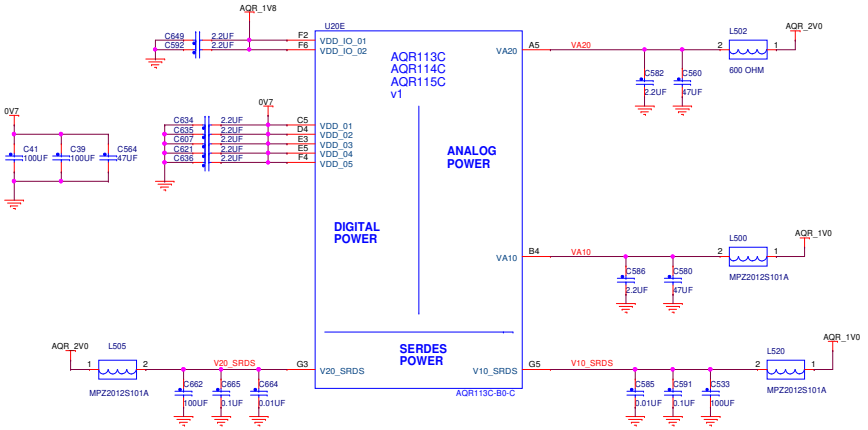
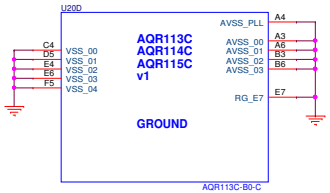
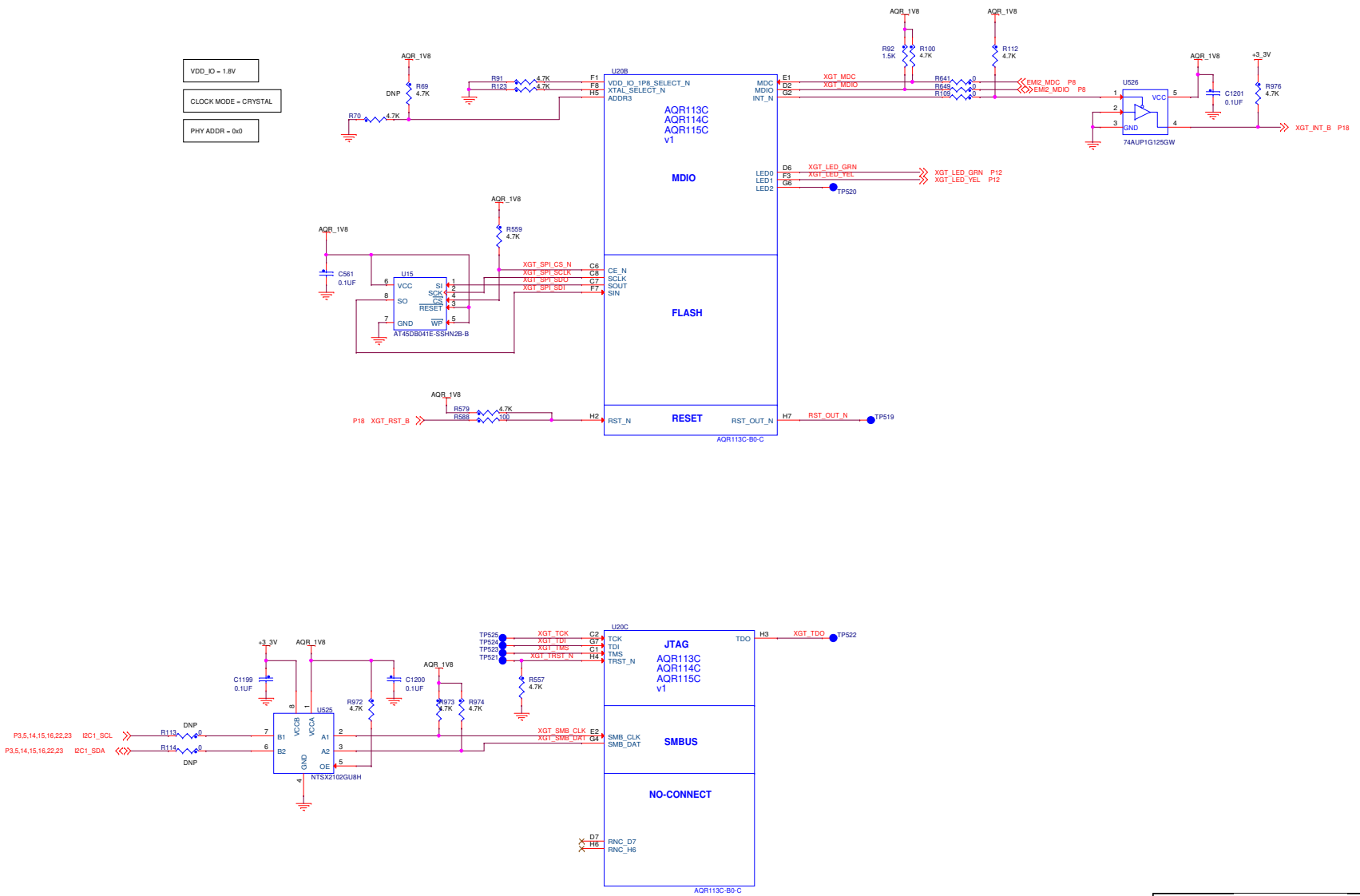
|---|---|---|---|
| ICAP Classification: | CP: ___ | IUO: | PUBI: X |
| Drawing Title: | LS1046ARDB-PB | | |
| Page Title: | SGMII2 | | |
| Size: C | Document Number: SCH-29142 PDF: SPF-29142 | | Rev: C |
| Date: Friday, March 19, 2021 | Sheet 11 of 24 | | |




| | | | |
|---|---|---|---|
| ICAP Classification: | CP: ___ | IUO: | PUBL: X |
| Drawing Title: | LS1046ARDB-PB | | |
| Page Title: | ETHERNET PHY AQR113C_1 | | |
| Size: C | Document Number: SCH-29142 PDF: SPF-29142 | | Rev: C |
| Date: Friday, March 19, 2021 | Sheet 12 of 24 | | |




| | |
|---|---|
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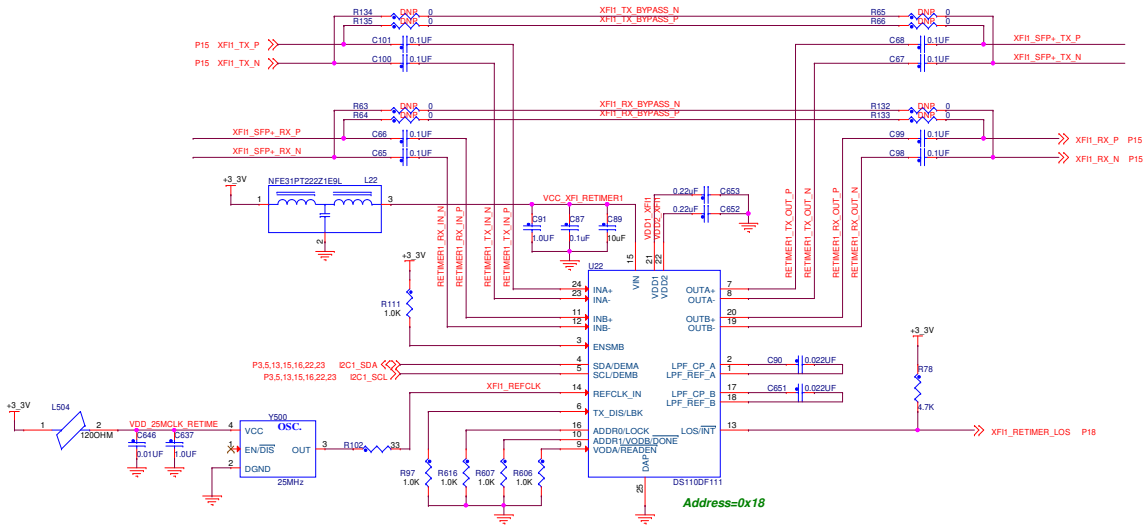
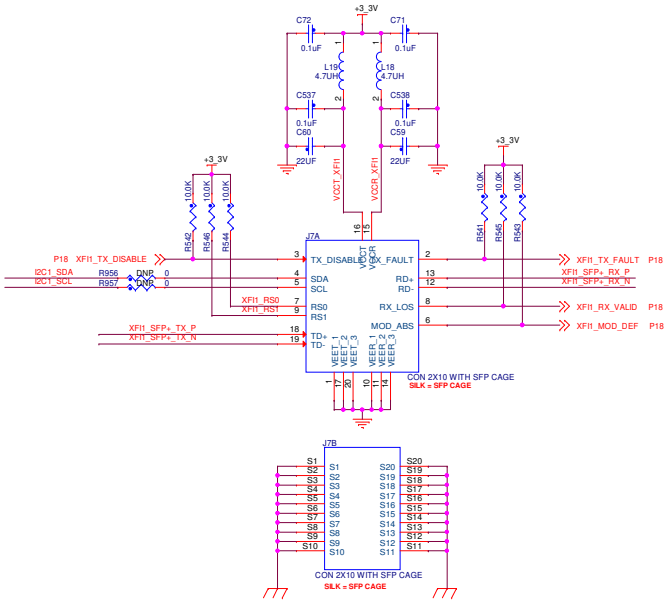
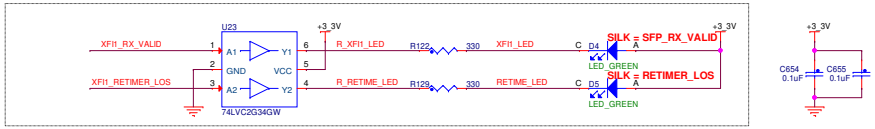
| Page Title: | ETHERNET PHY AQR113C_2 |
| Size: C | Document Number: SCH-29142 PDF: SPF-29142 Rev: C |
| Date: Friday, March 19, 2021 | Sheet 13 of 24 |

# XFI1 RETIMER




**Note:**
**I2C bus(I2C1_SDA, I2C1_SCL) is disconnected to J7 by 0ohm. FINISAR module FTLX851D3BCL also use 0x51 address. It's confilct with SPD address on I2C1 bus.**




| | |
|---|---|
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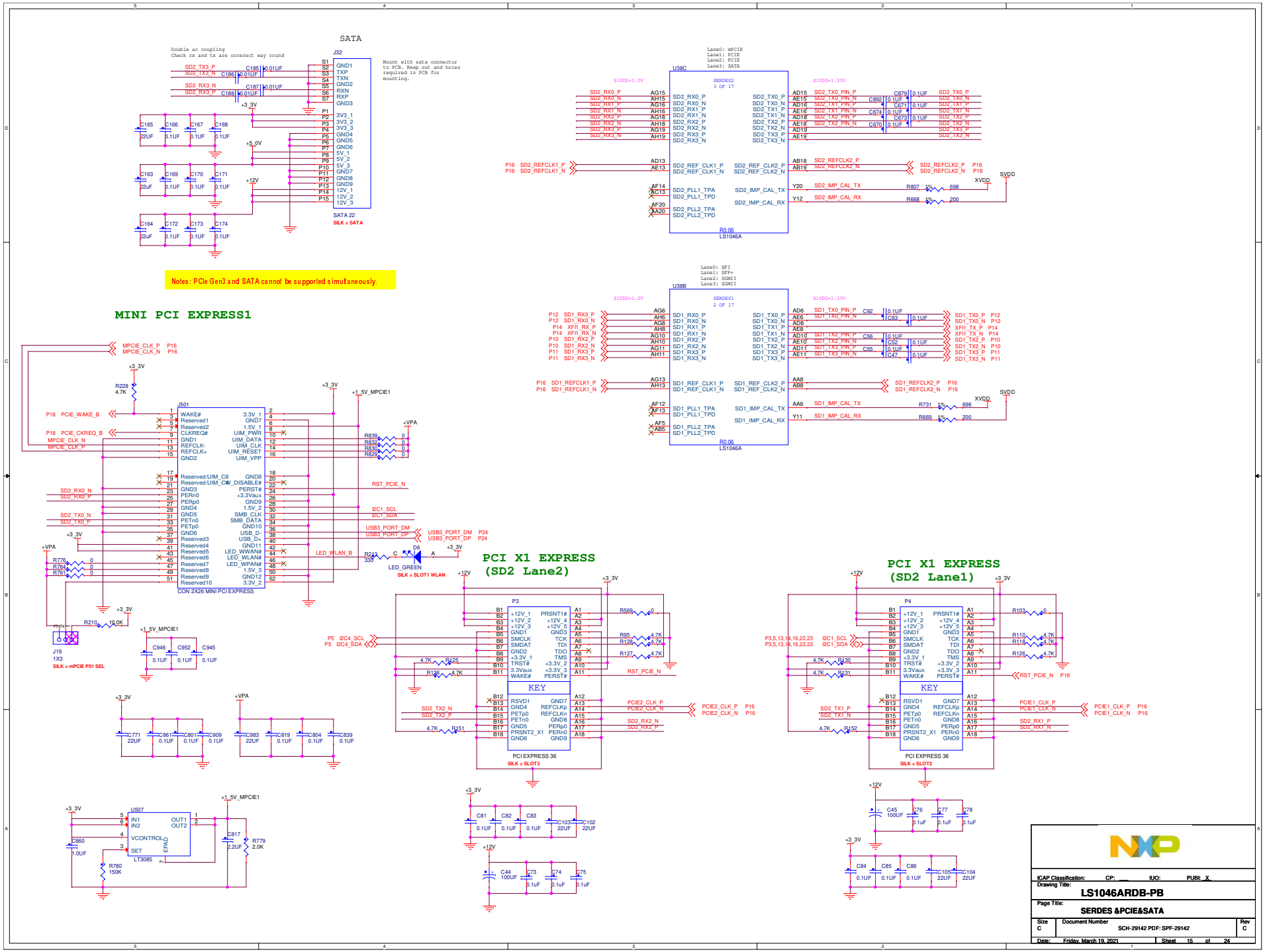
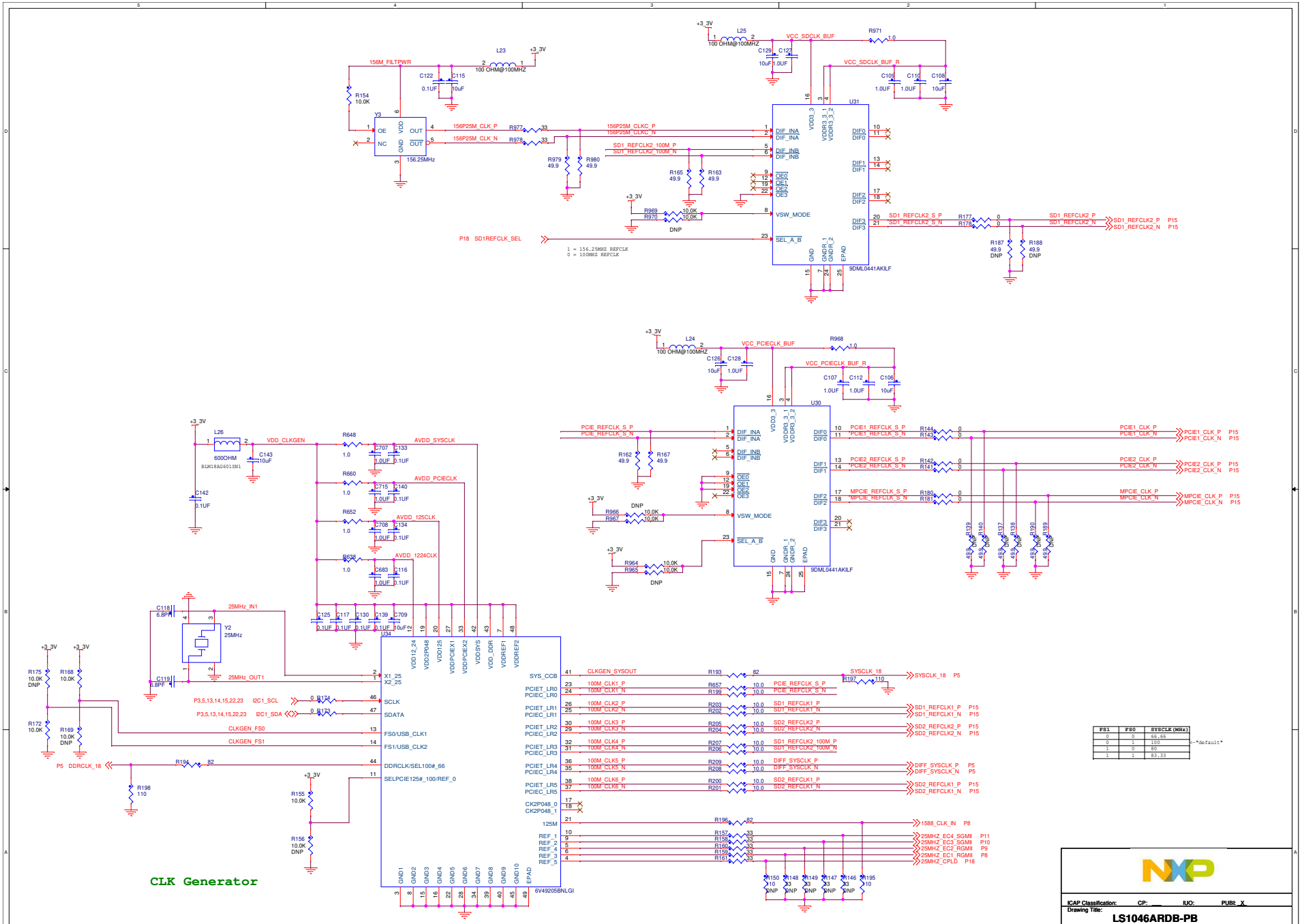
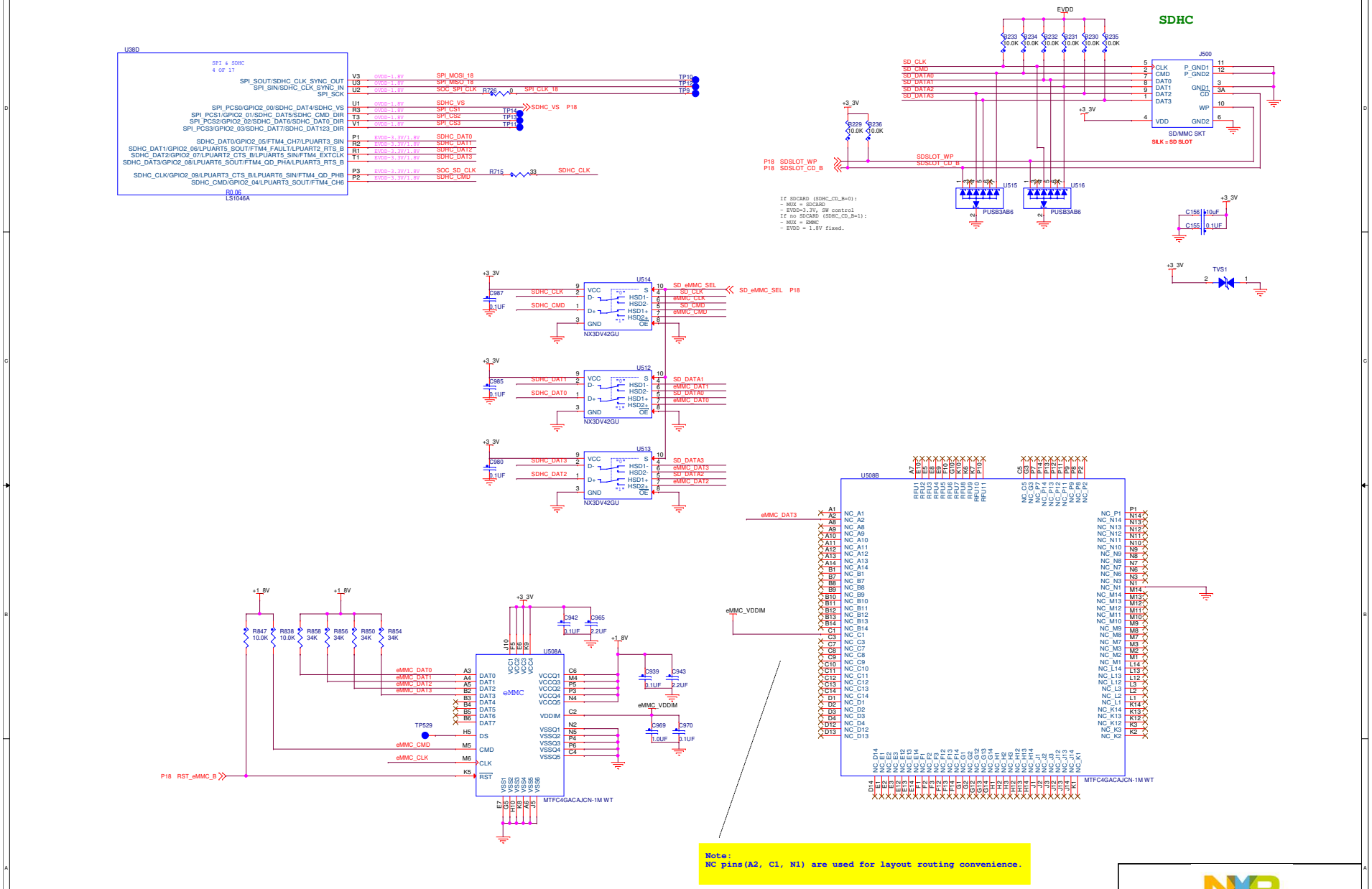
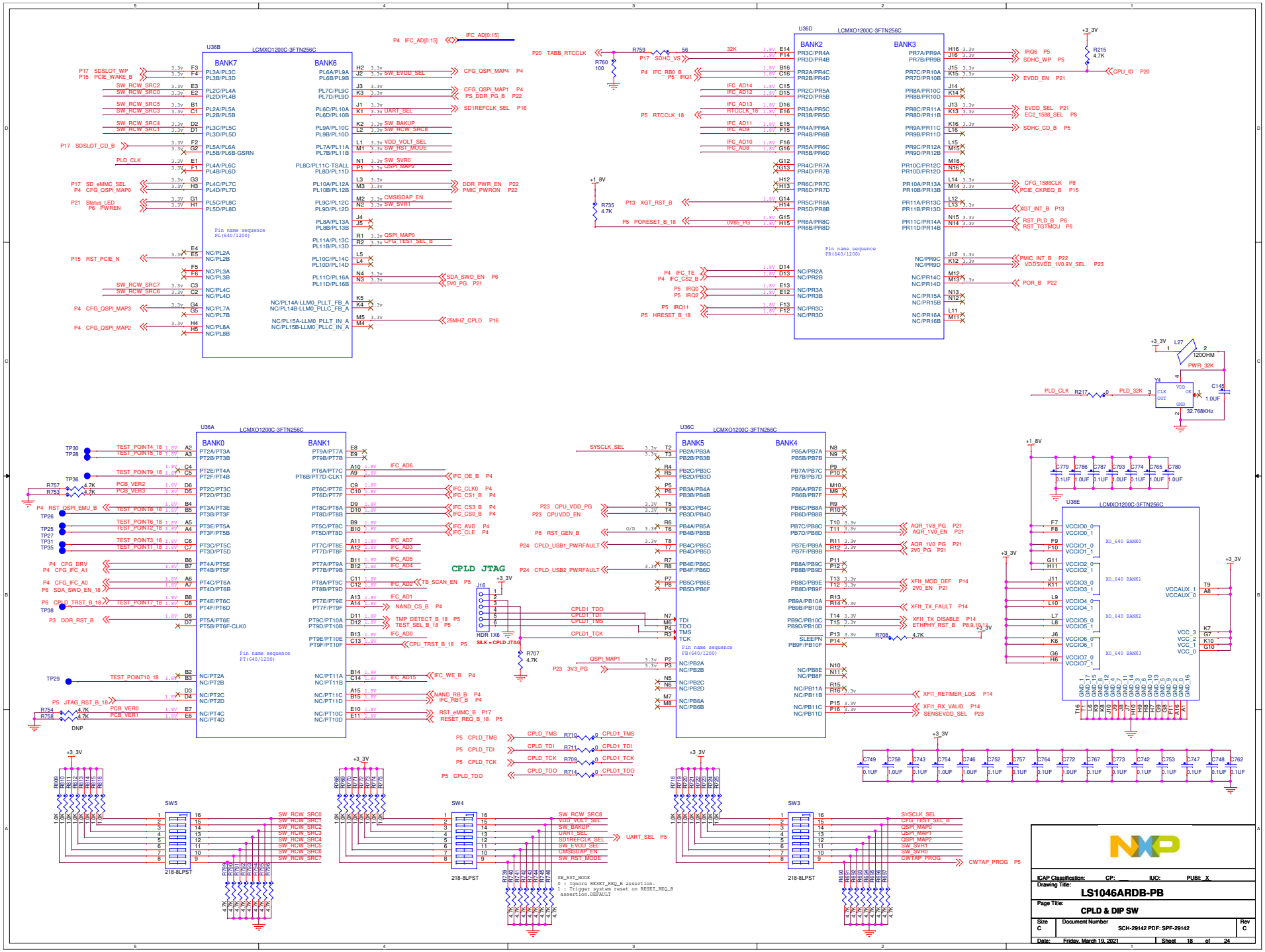
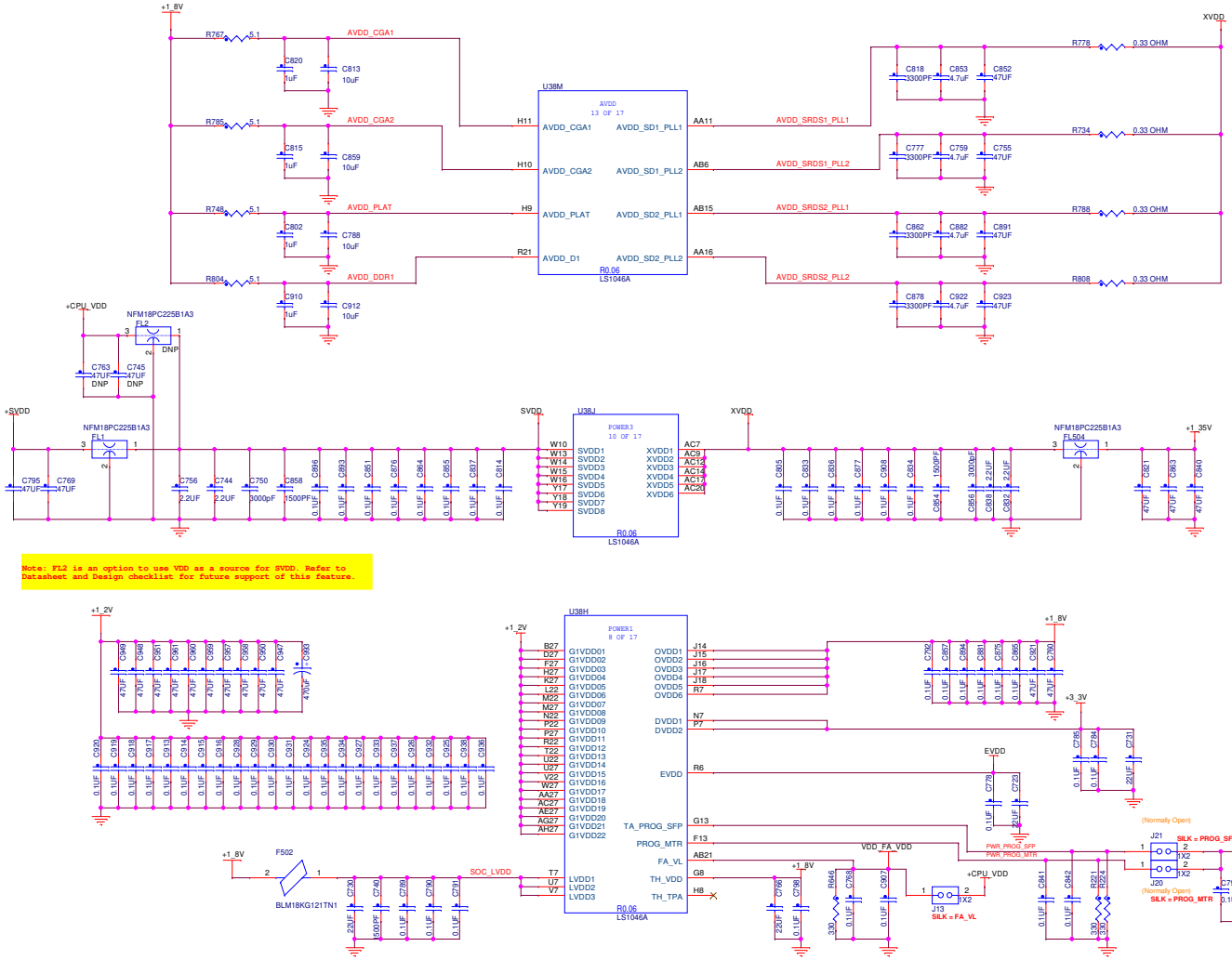
| Drawing Title: | LS1046ARDB-PB |
| Page Title: | ETHERNET 10G SFP+ |
| Size: C | Document Number: SCH-29142 PDF: SPF-29142 Rev: C |
| Date: Friday, March 19, 2021 | Sheet 14 of 24 |


SATA
Double ac coupling
Check rx and tx are corerect way round
J32
Mount with sata connector to PCB. Keep out and holes required in PCB for mounting.
SATA 22
SILK = SATA
Lane0: mPCIE
Lane1: PCIE
Lane2: PCIE
Lane3: SATA
U38C
SERDES2
3 OF 17
LS1046A
Notes: PCIe Gen3 and SATA cannot be supported simultaneously.
MINI PCI EXPRESS1
CON 2X26 MINI PCI EXPRESS
SILK = mPCIE P51 SEL
Lane0: XFI
Lane1: SFP+
Lane2: SGMII
Lane3: SGMII
U38B
SERDES1
2 OF 17
PCI X1 EXPRESS
(SD2 Lane2)
PCI EXPRESS 36
SILK = SLOT3
SILK = SLOT1 WLAN
PCI X1 EXPRESS
(SD2 Lane1)
SILK = SLOT2
U507
LT3085
ICAP Classification:
CP:
IUO:
PUBL: X
Drawing Title:
LS1046ARDB-PB
Page Title:
SERDES &PCIE&SATA
Size
C
Document Number
SCH-29142 PDF: SPF-29142
Rev
C
Date:
Friday, March 19, 2021
Sheet
15
of
24

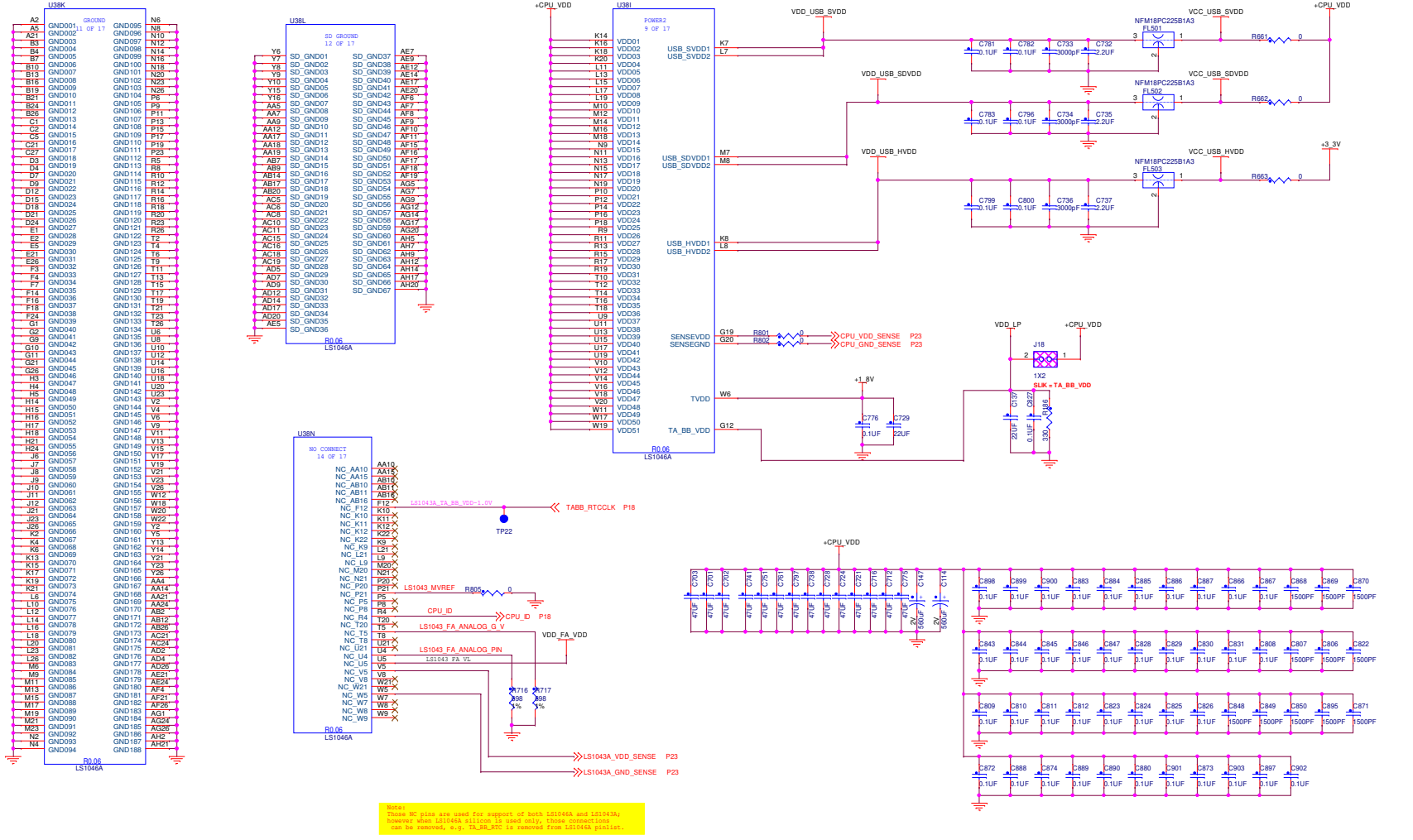

CLK Generator
9DML0441AKILF
6V49205BNLGI
LS1046ARDB-PB
CLOCK
SCH-29142 PDF: SPF-29142
Friday, March 19, 2021
Sheet 16 of 24
FS1 FS0 SYSCLK (MHz)
0 0 66.66
0 1 100 <-"default"
1 0 80
1 1 83.33

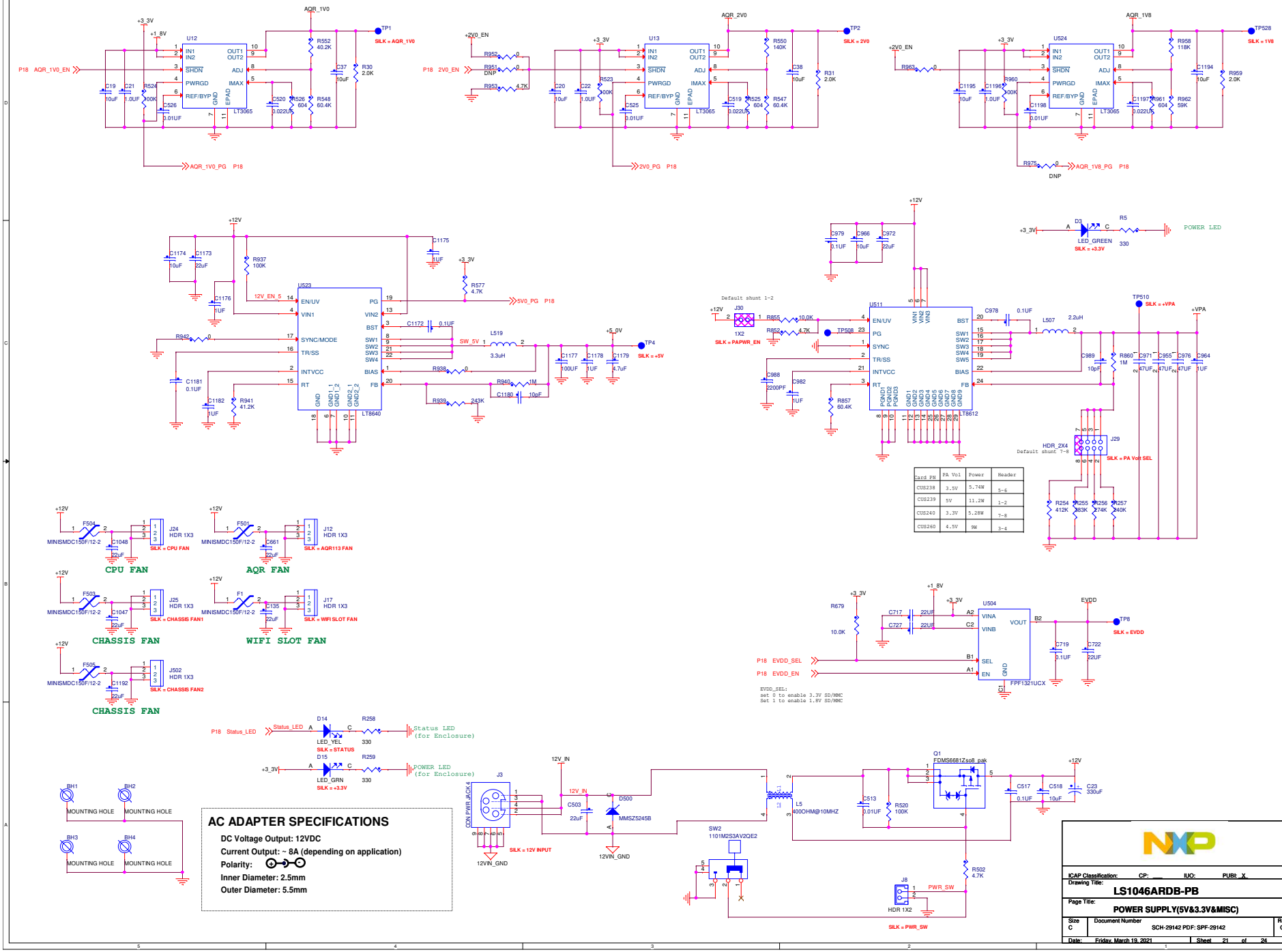

SDHC
U38D
SPI & SDHC
4 OF 17
SPI_SOUT/SDHC_CLK_SYNC_OUT
SPI_SIN/SDHC_CLK_SYNC_IN
SPI_SCK
SPI_PCS0/GPIO2_00/SDHC_DAT4/SDHC_VS
SPI_PCS1/GPIO2_01/SDHC_DAT5/SDHC_CMD_DIR
SPI_PCS2/GPIO2_02/SDHC_DAT6/SDHC_DAT0_DIR
SPI_PCS3/GPIO2_03/SDHC_DAT7/SDHC_DAT123_DIR
SDHC_DAT0/GPIO2_05/FTM4_CH7/LPUART3_SIN
SDHC_DAT1/GPIO2_06/LPUART5_SOUT/FTM4_FAULT/LPUART2_RTS_B
SDHC_DAT2/GPIO2_07/LPUART2_CTS_B/LPUART5_SIN/FTM4_EXTCLK
SDHC_DAT3/GPIO2_08/LPUART6_SOUT/FTM4_QD_PHA/LPUART3_RTS_B
SDHC_CLK/GPIO2_09/LPUART3_CTS_B/LPUART6_SIN/FTM4_QD_PHB
SDHC_CMD/GPIO2_04/LPUART3_SOUT/FTM4_CH6
R0.06
LS1046A
SPI_MOSI_18
SPI_MISO_18
SOC_SPI_CLK
SPI_CLK_18
R726
SDHC_VS
SDHC_VS P18
SPI_CS1
SPI_CS2
SPI_CS3
SDHC_DAT0
SDHC_DAT1
SDHC_DAT2
SDHC_DAT3
SOC_SD_CLK
SDHC_CMD
R715
SDHC_CLK
EVDD
SD_CLK
SD_CMD
SD_DATA0
SD_DATA1
SD_DATA2
SD_DATA3
J500
SD/MMC SKT
SILK = SD SLOT
SDSLOT_WP
SDSLOT_CD_B
P18 SDSLOT_WP
P18 SDSLOT_CD_B
U515
U516
PUSB3AB6
If SDCARD (SDHC_CD_B=0):
- MUX = SDCARD
- EVDD=3.3V, SW control
If no SDCARD (SDHC_CD_B=1):
- MUX = EMMC
- EVDD = 1.8V fixed.
C156 10uF
C155 0.1UF
TVS1
U514
U512
U513
NX3DV42GU
SD_eMMC_SEL
SD_eMMC_SEL P18
SD_DATA1
SD_DATA3
eMMC_CLK
eMMC_CMD
eMMC_DAT0
eMMC_DAT1
eMMC_DAT2
eMMC_DAT3
U508A
U508B
eMMC
MTFC4GACAJCN-1M WT
eMMC_VDDIM
TP529
RST_eMMC_B
P18 RST_eMMC_B
Note:
NC pins(A2, C1, N1) are used for layout routing convenience.
ICAP Classification:
CP:
IUO:
PUBL: X
Drawing Title:
LS1046ARDB-PB
Page Title:
SDHC & SPI & eMMC
Size
C
Document Number
SCH-29142 PDF: SPF-29142
Rev
C
Date:
Friday, March 19, 2021
Sheet
17
of
24

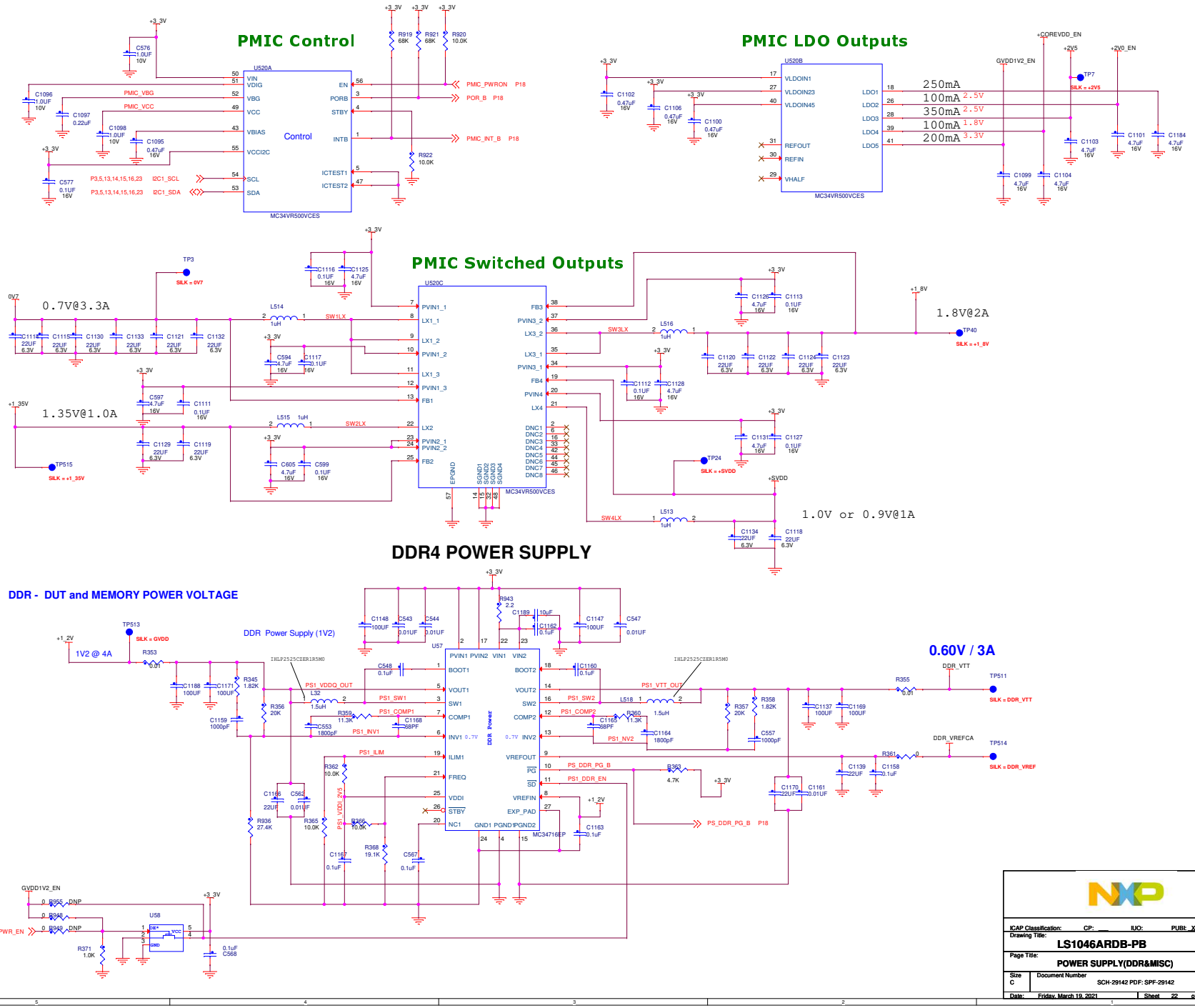

U36B
LCMXO1200C-3FTN256C
BANK7
BANK6
U36D
BANK2
BANK3
U36A
BANK0
BANK1
U36C
BANK5
BANK4
U36E
CPLD JTAG
SW5
SW4
SW3
218-8LPST
LS1046ARDB-PB
CPLD & DIP SW
SCH-29142 PDF: SPF-29142
Friday, March 19, 2021
Sheet 18 of 24




| | | |
|---|---|---|
| ICAP Classification: | CP: ___ IUO: | PUBI: X |
| Drawing Title: | LS1046ARDB-PB | |
| Page Title: | CPU POWER(MISC) | |
| Size: C | Document Number: SCH-29142 PDF: SPF-29142 | Rev: C |
| Date: Friday, March 19, 2021 | Sheet 19 of 24 | |


U38K
GROUND
1 OF 17
U38L
SD GROUND
12 OF 17
U38I
POWER2
9 OF 17
U38N
NO CONNECT
14 OF 17
R0.06
LS1046A
+CPU_VDD
VDD_USB_SVDD
VDD_USB_SDVDD
VDD_USB_HVDD
VCC_USB_SVDD
VCC_USB_SDVDD
VCC_USB_HVDD
NFM18PC225B1A3
FL501
FL502
FL503
+3_3V
+1_8V
VDD_LP
J18
1X2
SLK=TA_BB_VDD
CPU_VDD_SENSE P23
CPU_GND_SENSE P23
TABB_RTCCLK P18
TP22
LS1043_MVREF
CPU_ID
CPU_ID P18
LS1043_FA_ANALOG_G_V
LS1043_FA_ANALOG_PIN
LS1043_FA_VL
VDD_FA_VDD
LS1043A_VDD_SENSE P23
LS1043A_GND_SENSE P23
Note:
Those NC pins are used for support of both LS1046A and LS1043A;
however when LS1046A silicon is used only, those connections
can be removed, e.g. TA_BB_RTC is removed from LS1046A pinlist.
ICAP Classification:
CP:
IUO:
PUBL: X
Drawing Title:
LS1046ARDB-PB
Page Title:
CPU POWER(VDD&GND&NC)
Size
C
Document Number
SCH-29142 PDF: SPF-29142
Rev
C
Date:
Friday, March 19, 2021
Sheet
20
of
24


AQR_1V0
TP1
SILK = AQR_1V0
U12
LT3065
AQR_1V0_EN P18
AQR_1V0_PG P18
AQR_2V0
TP2
SILK = 2V0
U13
+2V0_EN
2V0_EN P18
2V0_PG P18
AQR_1V8
TP528
SILK = 1V8
U524
AQR_1V8_PG P18
DNP
+12V
U523
LT8640
12V_EN_5
5V0_PG P18
SW_5V
TP4
SILK = +5V
+5_0V
U511
LT8612
Default shunt 1-2
SILK = PAPWR_EN
TP510
SILK = +VPA
+VPA
HDR_2X4
Default shunt 7-8
J29
SILK = PA Volt SEL
Card PN | PA Vol | Power | Header
CUS238 | 3.5V | 5.74W | 5-6
CUS239 | 5V | 11.2W | 1-2
CUS240 | 3.3V | 5.28W | 7-8
CUS260 | 4.5V | 9W | 3-4
POWER LED
LED_GREEN
SILK = +3.3V
CPU FAN
AQR FAN
CHASSIS FAN
WIFI SLOT FAN
CHASSIS FAN
MINISMDC150F/12-2
SILK = CPU FAN
SILK = AQR113 FAN
SILK = CHASSIS FAN1
SILK = WIFI SLOT FAN
SILK = CHASSIS FAN2
HDR 1X3
U504
FPF1321UCX
EVDD
TP8
SILK = EVDD
P18 EVDD_SEL
P18 EVDD_EN
EVDD_SEL:
set 0 to enable 3.3V SD/MMC
Set 1 to enable 1.8V SD/MMC
P18 Status_LED
Status LED
(for Enclosure)
POWER LED
(for Enclosure)
LED_YEL
LED_GRN
SILK = STATUS
SILK = +3.3V
BH1
BH2
BH3
BH4
MOUNTING HOLE
AC ADAPTER SPECIFICATIONS
DC Voltage Output: 12VDC
Current Output: ~ 8A (depending on application)
Polarity:
Inner Diameter: 2.5mm
Outer Diameter: 5.5mm
J3
DCN_PWR_JACK_4
12V_IN
12VIN_GND
SILK = 12V INPUT
D500
MMSZ5245B
SW2
1101M2S3AV2QE2
L5
400OHM@10MHZ
Q1
FDMS6681Zs08_pak
J8
HDR 1X2
PWR_SW
SILK = PWR_SW
NXP
ICAP Classification: CP: ___ IUO: PUBL: X
Drawing Title:
LS1046ARDB-PB
Page Title:
POWER SUPPLY(5V&3.3V&MISC)
Size C
Document Number
SCH-29142 PDF: SPF-29142
Rev C
Date: Friday, March 19, 2021
Sheet 21 of 24


PMIC Control
PMIC LDO Outputs
PMIC Switched Outputs
DDR4 POWER SUPPLY
DDR - DUT and MEMORY POWER VOLTAGE
DDR Power Supply (1V2)
0.7V@3.3A
1.35V@1.0A
1.8V@2A
1.0V or 0.9V@1A
0.60V / 3A
1V2 @ 4A
250mA
100mA 2.5V
350mA 2.5V
100mA 1.8V
200mA 3.3V
MC34VR500VCES
MC34716EP
LS1046ARDB-PB
POWER SUPPLY(DDR&MISC)
SCH-29142 PDF: SPF-29142
Friday, March 19, 2021

# VDD POWER (1.0V@20A)

VOUT:
OPT1(0.9V): Rt=60.4Kohm; Rb=121Kohm
OPT2(1.0V): Rt=60.4Kohm; Rb=90.9Kohm

U518 LTC3866

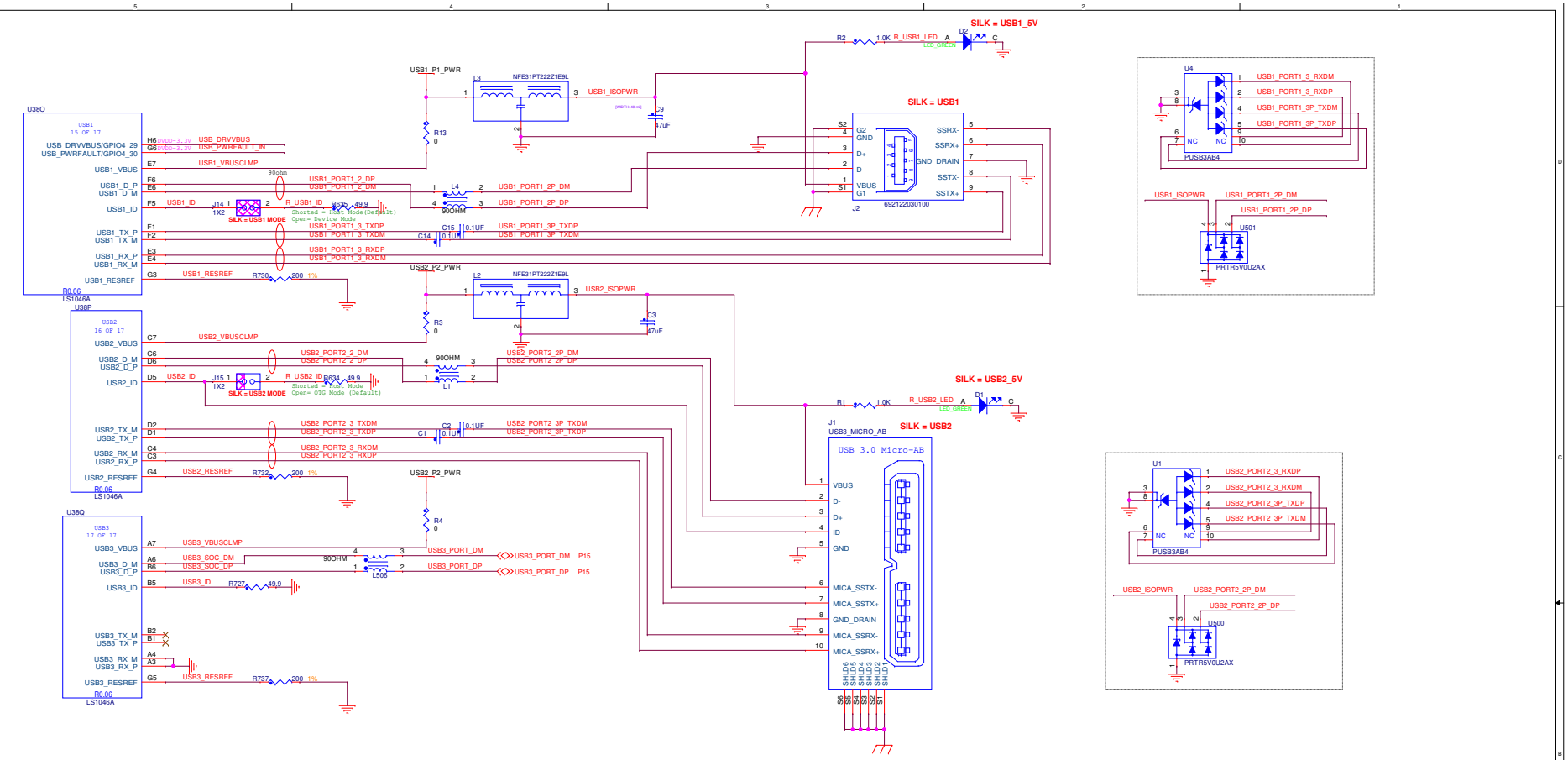
VDD&SVDD Vout:
Enable(Low Level): 1.0V;
Disable(High level):0.9V

# 3.3V POWER (3.3V@15A)

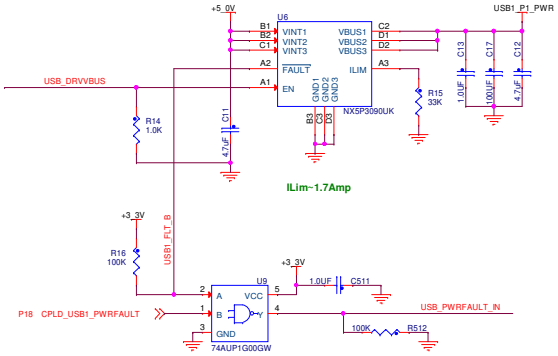
U519 LTC3866

Note:
It is permissible to omit this analog mux so to improve the regulator circuit stability and lower cost providing the sense lines are routed to both sets of sense pair pins for support of both LS1046A and LS1043A; however little or no stub as a daisy chain topology is a must.

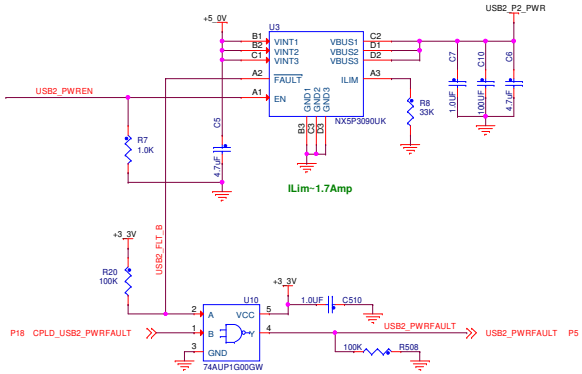
| | |
|---|---|
| ICAP Classification: | CP: ___ IUO: PUBL: X |
| Drawing Title: | LS1046ARDB-PB |
| Page Title: | VDD & SVDD |
| Size: C | Document Number: SCH-29142 PDF: SPF-29142 Rev: C |
| Date: Friday, March 19, 2021 | Sheet 23 of 24 |



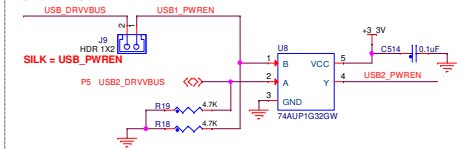

# USB1 POWER



# USB2 POWER



Install Jumper J9 to control all USB_PWREN signals through USB1_DRVVBUS



| | |
|---|---|
| ICAP Classification: | CP: ___ IUO: PUBL: X |
| Drawing Title: | LS1046ARDB-PB |
| Page Title: | USB |
| Size: C | Document Number: SCH-29142 PDF: SPF-29142 Rev: C |
| Date: Friday, March 19, 2021 | Sheet 24 of 24 |