Figure 1. LX2160ARDB chassis

The figure below shows the back panel of the LX2160ARDB chassis.

Figure 2. Chassis back panel

The figure below shows the onboard connectors of the LX2160ARDB.

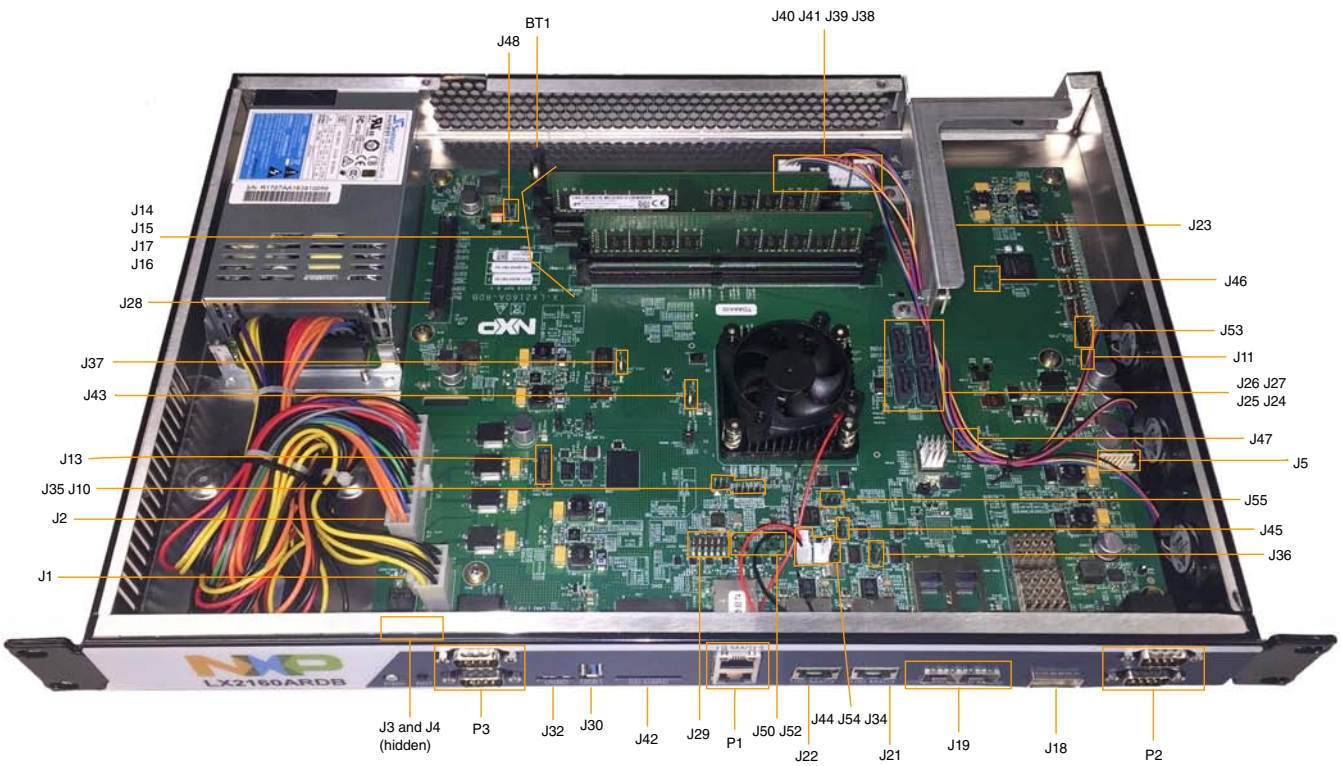

Figure 3. Connectors

The figure below shows the jumpers, LEDs, and DIP switches available on the LX2160ARDB.

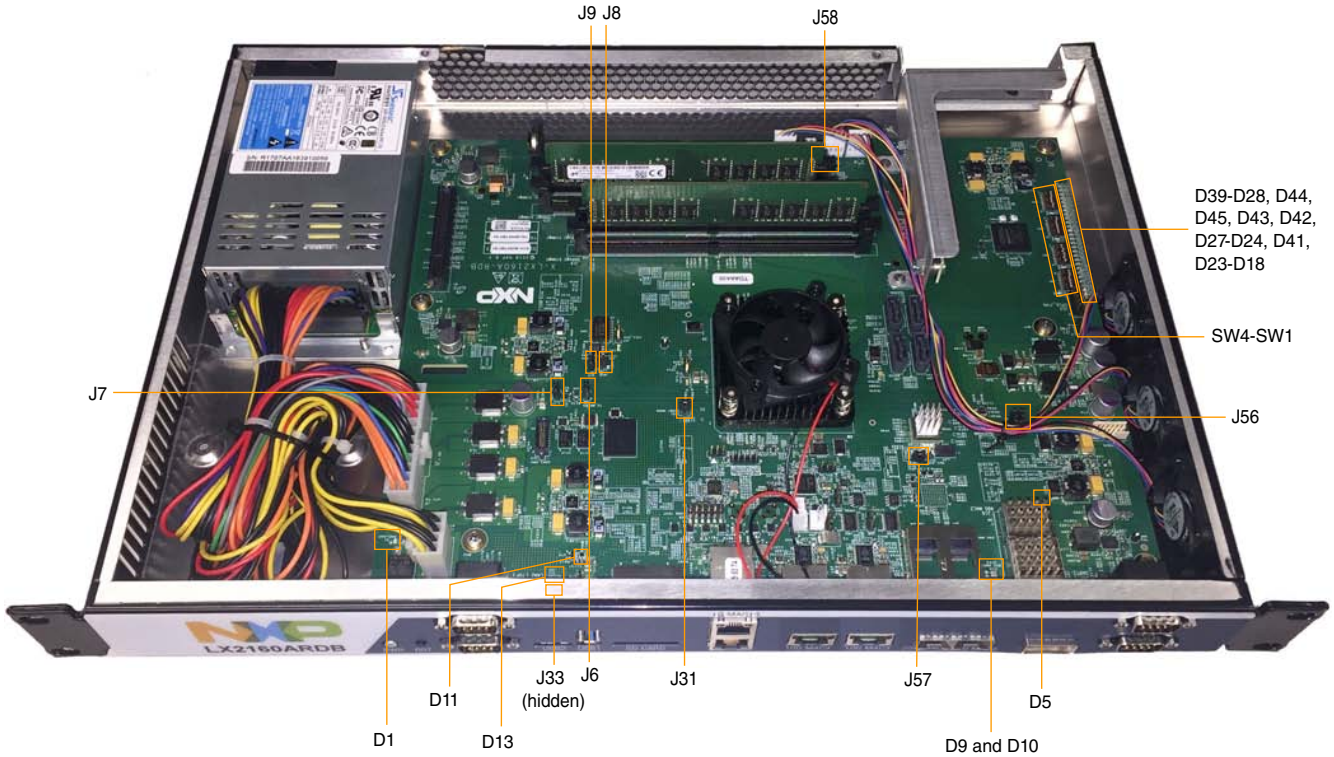

Figure 4. Jumpers, LEDs, and DIP switches

The figure below shows a closer look of the DIP switches.

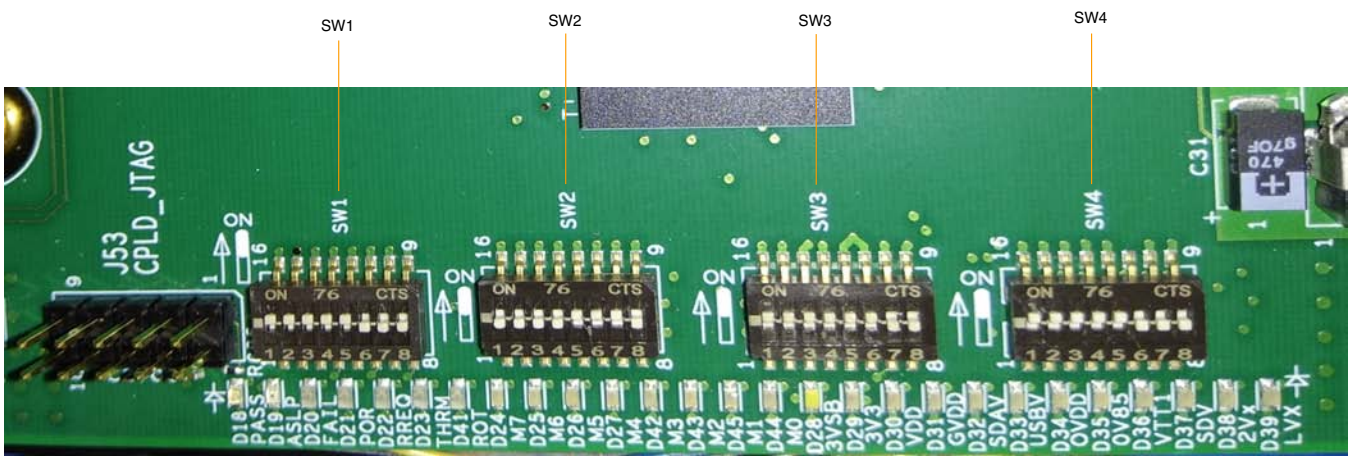

Figure 5. DIP switches

5 Power and reset buttons

The power and reset buttons are present on the front panel of the LX2160ARDB chassis (see Figure 1). Both power and reset buttons are push buttons. The table below describes the power and reset buttons.

Table 5. Power and reset buttons

Identifier	Label	Function	Description
SW5	PWR	Power cycle	Press SW5 to turn the power on or off
SW7	RST	System reset	Press SW7 to reset the system, including the device and all the attached peripherals

You cannot switch off the board completely when the SW_AUTO_ON switch (SW4[2]) is set to ON/1. In this mode, pressing the power switch turns the power off briefly, then it immediately turns back on. To turn off power, set the SW_AUTO_ON switch to OFF/0 or disconnect the AC power.

6 Connectors

The LX2160ARDB has numerous onboard connectors (see Figure 3). The table below describes the LX2160ARDB connectors.

Table 6. LX2160ARDB connectors

Connector	Description	Connector type	Typical connection
BT1	RTC battery	3-pin battery holder	Connects to 3 V standby CR2032 lithium coin cell battery
J1	12 V ATX power supply	2x4-pin ATX 12 V connector	Connects to the ATX power supply; both connections are required
J2	Main ATX power supply	2x12-pin ATX connector	
J3	Remote power	1x2-pin header	Connects to remote power switch
J4	Remote reset	1x2-pin header	Connects to remote reset switch
J5	VDD_DEBUG	2x6-pin header	Connects to Linear Technology PMBus monitoring tool (not included in the hardware kit)
J47	VDD measurement	1x2-pin connector	Allows remote measurement of VDD
J48	GVDD measurement	1x2-pin connector	Allows remote measurement of GVDD
J11	Arm JTAG	2x5-pin Arm JTAG header	Connects to CodeWarrior TAP using a 10-pin cable
J53	CPLD JTAG	2x5-pin header	Connects to JTAG interface for CPLD programming
J18	40G MAC2: 40 Gbit Ethernet	QSFP+ cage	Accepts one zQSFP+ transceiver (optical or copper) (not included in the hardware kit)
J19	25G MAC5/6: 25 Gbit Ethernet	SFP cage (2)	Accepts two SFP+ transceivers (optical or copper) (not included in the hardware kit)
J21	10G MAC3: 10 Gbit USXGMII	RJ45-19 connector	Connects to external RJ45 Ethernet cable
J22	10G MAC4: 10 Gbit USXGMII	RJ45-19 connector	Connects to external RJ45 Ethernet cable
P1	1G MAC17/18: 1 Gbit RGMII • 1G MAC17 (bottom) • 1G MAC18 (top)	RJ45 connector (2)	Connects to external RJ45 Ethernet cable

Table continues on the next page...

Table 6. LX2160ARDB connectors (continued)

Connector	Description	Connector type	Typical connection
J45	40G interface programming	1x3-pin connector	Provides direct access to CS4223 data EEPROM for programming purposes
P2	UART1 (bottom) UART2 (top)	DB9 connector (2)	Connects to external RS-232 cable
P3	CAN1 (bottom) CAN2 (top)	DB9 connector (2)	Connects to external CAN adapter cable
J23	PCI Express slot #1	PCIe Gen 4 x4 connector	Connector for Gen 1/2/3/4 PCIe cards, or right-angle/low-profile chassis adapter accepting Gen 1/2 cards
J28	PCI Express slot #2	PCIe Gen 4 x8 connector	Connector for Gen 1/2/3/4 PCIe cards
J24	SATA1	SATA-3 header	Connector for user-supplied SATA disk
J25	SATA2	SATA-3 header	Connector for user-supplied SATA disk
J26	SATA3	SATA-3 header	Connector for user-supplied SATA disk
J27	SATA4	SATA-3 header	Connector for user-supplied SATA disk
J30	USB1 (Host mode by default)	USB 3.0 Type-A connector	Connects to USB-compatible device
J32	USB2 (OTG mode by default)	USB 3.0 Micro-AB connector	Connects to USB-compatible device
J42	SD card slot	SD card receptacle	Provides access to an SDHC/SDXC card
J13	QSPI emulator	2x10-pin connector	Connects to DediProg EM100Pro QSPI emulator using a sideband cable (ISP-ADP-intel-B)
J46	QSPI emulator reset	1x2-pin connector	Allows system reset to be triggered by DediProg EM100Pro emulator using the ISP-ADP-intel-B cable
J34	I2C1	1x3-pin header	Provides remote access to I2C1 bus
J36	I2C1_CH0	1x3-pin header	Provides remote access to I2C1 channel 0 segment
J55	I2C1_CH1	1x3-pin header	Provides remote access to I2C1 channel 1 segment
J37	I2C1_CH3	1x3-pin header	Provides remote access to I2C1 channel 3 segment
J35	I2C5	1x3-pin header	Provides remote access to I2C5 bus
J43	I2C6	1x3-pin header	Provides remote access to I2C6 bus
J10	GPIO/event access	1x5-pin header	Provides access to GPIO/event pins
J38	Fan #1 (placed near bottom of PCB)	1x4 connector	Provides PWM-controlled 12 V power for cooling fans
J39	Fan #2 (placed near bottom of PCB)	1x4 connector	
J41	Fan #4 (placed near bottom of PCB)	1x4 connector	
J40	Fan #3 (placed near bottom of PCB)	1x4 connector	

Table continues on the next page...

Table 6. LX2160ARDB connectors (continued)

Connector	Description	Connector type	Typical connection
J44	Fan #5 (placed near top of PCB)	1x4 connector	
J54	Heatsink fan (placed near Fan #5)	1x3 connector	
J29	1588 test	2x6-pin header	Provides access to IEEE 1588 pins
J50	SMA #1	Subminiature version A (SMA) coaxial connector	Provides access to recovered IEEE-1588 clock. J50 is not installed, by default.
J52	SMA #2	SMA coaxial connector	J52 is not installed, by default
J14	DDR4#1 DIMM#1	288-pin DDR4 UDIMM socket	Single/dual rank UDIMM inserted
J15	DDR4#1 DIMM#2	288-pin DDR4 UDIMM socket	Single/dual rank UDIMM (optional)
J17	DDR4#2 DIMM#1	288-pin DDR4 UDIMM socket	Single/dual rank UDIMM inserted
J16	DDR4#2 DIMM#2	288-pin DDR4 UDIMM socket	Single/dual rank UDIMM (optional)

7 Jumpers

Jumpers (or shorting headers) are used to select some options that either do not change often or involve power conduction. The LX2160ARDB jumpers are shown in Figure 4 and are described in the table below.

Table 7. LX2160ARDB jumpers

Jumper	Type	Name/function	Description
J6	1x2-pin connector	TA_BB_TMP_DETECT_B enable	Open: TA_BB_TMP_DETECT_B pin is grounded Shorted: TA_BB_TMP_DETECT_B pin is powered (default setting)
J7	1x2-pin connector	VBAT power for TA_BB_VDD enable	Not supported. Do not install J7. See *QorIQ LX2160A Reference Design Board Errata* for more details.
J8	1x2-pin connector	PROG_MTR voltage control (for NXP use only)	Open: PROG_MTR pin is powered off (default setting) Shorted: PROG_MTR pin is powered by OVDD (1.8 V)
J9	1x2-pin connector	TA_PROG_SFP voltage control (for NXP use only)	Open: TA_PROG_SFP pin is powered off (default setting) Shorted: TA_PROG_SFP pin is powered by OVDD (1.8 V)
J31	1x2-pin connector	USB1 mode setting	Open: USB1 works in Device mode Shorted: USB1 works in Host mode (default setting)

Table continues on the next page...

Table 7. LX2160ARDB jumpers (continued)

Jumper	Type	Name/function	Description
J33	1x2-pin connector	USB2 mode setting	Open: USB2 works in On-The-Go (OTG) mode (default setting) Shorted: USB2 works in Host mode
J56	2x3-pin connector	Inphi CS4223 GUI access	Normal: 1-2 short, 5-6 short (default setting) GUI mode: 1-2 open, 5-6 open
J57	1x2-pin connector	Inphi CS4223 GUI enable	Normal: Open (default setting) GUI mode: Short
J58	1x2-pin connector	Fan speed	Open: 100% speed Short: 50% speed (default setting)

NOTE

Most of these jumpers are installed during assembly, and they do not require any change.

8 LEDs

The LX2160ARDB has numerous onboard light-emitting diodes (LEDs), which can be used to monitor various system functions, such as power on, reset, board faults, and so on. The information collected from LEDs can be used for debugging purposes. The table below lists all the LEDs present on the LX2160ARDB.

Table 8. LX2160ARDB LEDs

Reference designator	LED color	LED name	Description (when LED is ON)
D1	Yellow	PRELOAD	The PSU-loading FET is active; it may be hot during power-up or shortly afterward. Avoid touching this area.
D18	Blue	PASS	The CPLD has completed power and reset sequencing and no errors are detected
D19	Yellow	ASLEEP	The processor has not exited Sleep mode, which generally indicates: • Improper RCW source selection • Boot memory does not contain a valid RCW/PBL • PLL multipliers in the RCW data are not compatible with the fixed SYSCLK, DDRCLK, or SDCLK values
D20	Red	FAIL	One of the following has happened: • A thermal over-temperature fault has occurred • One or more power supplies have not started • Software has set the register CTL[0] (FAIL) to indicate a software fault
D21	Red	PORST	The CPLD is asserting PORESET_B to the processor and is in the process of restarting the system
D22	Red	RST REQ	The processor is asserting RESET_REQ_B. This is typically due to the reasons described for the ASLEEP LED.
D23	Red	THERM	Thermal monitors have detected a thermal fault and have shut down the system

Table continues on the next page...

Table 8. LX2160ARDB LEDs (continued)

Reference designator	LED color	LED name	Description (when LED is ON)
			NOTE: Unless reprogrammed by user software, the thermal trip point is 85 °C.
D41	Red	ROTERR	The processor has been installed in the socket rotated 90, 180, or 270 degrees from the pin 1 orientation. The system and device power supplies have been shut down to protect the device.
D24	Green	M7	General status. See Multi-status LEDs for details.
D25	Green	M6	
D26	Green	M5	
D27	Green	M4	
D42	Green	M3	
D43	Green	M2	
D45	Green	M1	
D44	Green	M0	
D28	Green	3VSB	The ATX power supply is supplying 3.3 V “standby power” to the system. The system cannot power up unless this supply is provided.
D29	Green	3V3	3V3 ATX power supply is operating correctly
D30	Green	VDD	VDD (processor core) power supply is operating correctly
D31	Green	GVDD	GVDD (DDR4) power supply is operating correctly
D32	Green	SDAV	SD_AVDD power supply is operating correctly
D33	Green	USBV	USB_SVDD power supply is operating correctly
D34	Green	OVDD	OVDD power supply is operating correctly
D35	Green	0V85	0V85 power supply is operating correctly
D36	Green	VTT1	VTT1 power supply is operating correctly
D37	Green	SDV	SD_VDD power supply is operating correctly
D38	Green	2Vx	2V1 and 2V5 power supplies are operating correctly
D39	Green	LVX	0V9 and 1V2 power supplies are operating correctly
D5	Green	QSFP	A QSFP module is installed in the QSFP port
D9	Green	25GMAC5	An SFP module is installed in 25G MAC5 SFP port
D10	Green	25GMAC6	An SFP module is installed in 25G MAC6 SFP port
D11	Green	USB1_5V	5 V power is supplied to the USB #1 connector for external devices
D13	Green	USB2_5V	5 V power is supplied to the USB #2 connector for external devices

8.1 Multi-status LEDs

The board includes eight multi-status LEDs that indicate hardware activity; however, software can override these LEDs to use them for debugging purposes. The table below describes the functions of the multi-status LED arrays.

Table 9. LED array functions

LED	Startup (from power on to power-up complete + 2 seconds)	Normal (after 2 seconds)	User-defined (if register CTL[1] (LED) = 1)
M7	Power Sequencer state (see Table 10)	"Idle" pattern, a pattern shown to indicate that the FPGA has completed all startup activities	M[7:0] reflect contents of the LED register
M6			
M5			
M4		Off always	
M3	Reset Sequencer state (see Table 11)	Live I2C1_SCL activity	
M2		Live I2C remote activity	
M1		Same as M[3:2], except that short pulses are stretched to 500 ms for easier detection	
M0			

NOTE

The LX2160ARDB power up voltage sequence diagram (LX2160ARDB Reference Manual) lists the power supplies assigned to each tier.

Table 10. Power Sequencer state

State	LED: M[7:4]	Description
IDLE	1110 = 0xE	Waiting for power-on events (for example, switch)
WAIT_ATX	0000 = 0x0	Waiting for ATX PSU to report stable
EN_TIER1	0001 = 0x1	Enable tier 1 PSUs, wait for tier 1 power-good reports
EN_TIER2	0010 = 0x2	Enable tier 2 PSUs, wait for tier 2 power-good reports
EN_TIER3	0011 = 0x3	Enable tier 3 PSUs, wait for tier 3 power-good reports
EN_TIER4	0100 = 0x4	Enable tier 4 PSUs, wait for tier 4 power-good reports
WAIT_ALL	0110 = 0x6	Wait for all unmanaged PSUs to report power-good
PG_FAIL	0111 = 0x7	All power supplies were not stable within 1800*30 ns after the last power was enabled
STABLE	1000 = 0x8	Power sequencing complete. Wait for power-off events.
DISABLE	1101 = 0xD	Disable tiers 4..1 PSUs, in that order, with 1 ms delay
FAULT	1111 = 0xF	Fault occurred. Power supplies were shut down due to thermal faults or die rotation errors.

Table 11. Reset Sequencer state

State	LED: M[3:0]	Description
IDLE	0000 = 0x0	Waiting for initial reset events
RECONFIG	0010 = 0x2	Update configuration from registers
CLOCK_LOCK	0101 = 0x5	Wait for clock PLLs to stabilize
RELEASE_ALL	0110 = 0x6	Release all hardware resets except DUT
RELEASE_DUT	0111 = 0x7	Release DUT from reset
STABLE	1000 = 0x8	Reset sequencing complete. Wait for reset events.
RESET_REQ	1001 = 0x9	Start reset due to DUT RESET_REQ_B

Table continues on the next page...

Table 11. Reset Sequencer state (continued)

State	LED: M[3:0]	Description
PORESET	1010 = 0xA	Start reset due to JTAG_RST_B
RST_WATCH	1011 = 0xB	Start reset due to watchdog timeout
RST_BY_REG	1100 = 0xC	Start reset due to setting register bit RST_CTL[RST] = 1
RST_BY_SW	1101 = 0xD	Start reset due to pushbutton switch
RECONFIG	1110 = 0xE	Start reset due to reconfig request via RCFG[GO] = 1
POST_RST	1111 = 0xF	Wait for reset requests to clear

9 DIP switches

The LX2160ARDB provides dual inline package (DIP) switches to allow easy configuration of the system for the most popular board options. These switches are stored in BRDCFG and DUTCFG registers by CPLD before being used, allowing software (either local or remote) to reconfigure the system as needed.

The table below explains the DIP switches available in the LX2160ARDB. For each DIP switch:

- If the switch is up (on), the value is 1
- If the switch is down (off), the value is 0

Table 12. Switch settings

<table>
<tr><th>Switch</th><th>Supported function</th><th>Description</th></tr>
<tr><td>SW1[1:4]</td><td>RCW fetch location
CFG_RCW_SRC[3:0]</td><td>SW_RCW_SRC[3:0]
0000: Hard-coded RCW
1000: SDHC1: SD card
1001: SDHC2: eMMC
1010: I2C boot EEPROM
1100: XSPI sNAND, 2 KB pages
1101: XSPI sNAND, 4 KB pages
1111: XSPI serial NOR, 24-bit address (default setting)</td></tr>
<tr><td>SW1[5]</td><td>Reset mode
RESET_REQ_B</td><td>SW_RST_MODE
0: Ignore RESET_REQ_B
1: Trigger system reset on assertion of RESET_REQ_B (default setting)</td></tr>
<tr><td>SW1[6:8]</td><td>XSPI_A device mapping
CFG_XSPI_MAP[3:0]</td><td>SW_XMAP[2:0]: Controls how XSPI_A chip-selects are connected to devices/peripherals.
<table>
<tr><th>Bit value</th><th>XSPI_A_CS0</th><th>XSPI_A_CS1</th><th>Description</th></tr>
<tr><td>000 (default setting)</td><td>DEV#0</td><td>DEV#1</td><td>Boot from default flash memory</td></tr>
<tr><td>001</td><td>DEV#1</td><td>DEV#0</td><td>Boot from alternative flash memory</td></tr>
</table></td></tr>
</table>

Table continues on the next page...

Table 12. Switch settings (continued)

<table>
<tr><th>Switch</th><th>Supported function</th><th>Description</th></tr>
<tr><td></td><td></td><td>
<table>
<tr><th>Bit value</th><th>XSPI_A_CS0</th><th>XSPI_A_CS1</th><th>Description</th></tr>
<tr><td>010</td><td>QSPI emulator</td><td>DEV#0</td><td>Boot from QSPI emulator, program default flash memory</td></tr>
<tr><td>011</td><td>QSPI emulator</td><td>DEV#1</td><td>Boot from QSPI emulator, program alternative flash memory</td></tr>
<tr><td>100</td><td>DEV#0</td><td>QSPI emulator</td><td>Emulator access</td></tr>
</table>
</td></tr>
<tr><td>SW2[1]</td><td>PCIe Spread-Spectrum enable
CFG_SPREAD</td><td>SW_SPREAD
• 0: 100 MHz clocks for PCIe slots are fixed (default setting)
• 1: 100 MHz clocks for PCIe slots are spread-spectrum modulated</td></tr>
<tr><td>SW2[2]</td><td>CS4223 configuration
CFG_40GE_ROM</td><td>SW_P40IN
• 0: CS4223 40 GbE PHY is not self-configured (default setting)
• 1: CS4223 40 GbE PHY is self-configured on reset</td></tr>
<tr><td>SW2[3]</td><td>PCIe slot clock enable
CFG_CLKEN_SLOT[1:2]_B</td><td>SW_SLOTCLK
• 0: PCIe slots are clocked only when a card is installed (default setting)
• 1: PCIe slots are clocked always</td></tr>
<tr><td>SW2[4]</td><td>CS4223 MDC clock generation</td><td>SW_MDC40G_EN
• 0: CS4223 does not receive clock during PORESET_B (default setting)
• 1: CS4223 receives ~1 MHz clock during PORESET_B</td></tr>
<tr><td>SW2[5]</td><td>SDHC voltage control</td><td>SW_SDHC_VCTL
• 0: EVDD switches between 1.8 V and 3.3 V as required (default setting)
• 1: EVDD locked to 1.8 V only. Only low-voltage (LV) SDHC cards are supported in this mode.</td></tr>
<tr><td>SW2[6]</td><td>Unused
CFG_ENG_USE0</td><td>SW_ENGUSE0
Reserved with 1 as the default setting</td></tr>
<tr><td>SW2[7]</td><td>Unused
CFG_ENG_USE1</td><td>SW_ENGUSE1
Reserved with 1 as the default setting</td></tr>
<tr><td>SW2[8]</td><td>DDR clock source selection
CFG_ENG_USE2</td><td>SW_ENGUSE2
• 0: DDR clocked from DDRCLK pin (default setting)
• 1: DDR clocked from differential SYSCLK</td></tr>
<tr><td>SW3[1:3]</td><td>Device type selection
TEST_SEL_B, CFG_SVR[0:1]</td><td>SW_TESTSEL_B + SW_SVR[0:1]
• 011: LX2120A/E
• 101: LX2080C/E
• 111: LX2160A/E (default setting)
• All other values are reserved</td></tr>
<tr><td>SW3[4]</td><td>SoC use
CFG_SOC_USE</td><td>SW_SOCUSE
• 1: Normal mode (default setting)
NOTE: Do not change the default setting of this switch.</td></tr>
<tr><td>SW3[5:6]</td><td>CPU device override</td><td>SW_CPU_SEL</td></tr>
</table>

Table continues on the next page...

Table 12. Switch settings (continued)

Switch	Supported function	Description
		• 00: Override to LS2-family device • 01: Override to LX2-family device • 10: Reserved • 11: Reserved (default setting) **NOTE:** This switch's settings are ignored if SW3[7] is set to 0.
SW3[7]	Force CPU selection	SW_CPU_FORCE • 0: Normal mode (default setting) • 1: Use SW_CPU_SEL instead of CPU_ID **NOTE:** Do not change the default setting of this switch.
SW3[8]	Unused	Reserved with 0 as the default setting
SW4[1]	Bypass mode	SW_BYPASS_B • 0: Disable thermal monitors and other alarms • 1: Normal operation (default setting)
SW4[2]	Automatic power on	SW_AUTO_ON • 0: Normal power on/off (default setting) • 1: Always power up
SW4[3]	System configuration write protect CFG_MEM_WP	SW_CFG_WP • 0: Allow writes to SYSID and I2C flash • 1: Write-protect SYSID and I2C flash (default setting)
SW4[4]	JTAG Scan mode TBSCAN_EN_B	SW_TBSCAN • 0: Boundary Scan mode • 1: Debugging mode (default setting)
SW4[5]	Boot Box mode	SW_BOOTBOX_B • 0: Enable Boot Box mode • 1: Normal operating mode (default setting)
SW4[6]	VDD power enable	SW_VDD_DIS • 0: Enable VDD power supply (default setting) • 1: Disable VDD power supply
SW4[7:8]	General purpose CFG_GPIN[7:6]	SW_GPIN[7:6] • 00: Software or end-user defined (default setting)

The table below summarizes the default switch settings of the LX2160ARDB DIP switches.

Table 13. Default switch settings

DIP switch	Default setting
SW1	1111_1000
SW2	0000_0110
SW3	1111_1100
SW4	1011_1000

10 Getting started with LX2160ARDB

This section explains:

- Prerequisites
- Booting LX2160ARDB

10.1 Prerequisites

To set up your LX2160ARDB, you need the items listed in the table below.

Table 14. Prerequisites

Item	Available in board kit?	Purpose / required action
Hardware		
Host computer system capable of running a terminal emulator	No	Host computer (for example, Windows PC, Linux system, or Mac) to control and monitor the LX2160ARDB from the serial console via a serial terminal emulator, such as Tera Term. **NOTE:** You can also use a Linux machine to connect to the board console via a Linux utility, such as minicom.
AC power cord	Yes	To connect the board to AC power supply
DB9 female to DB9 female serial cable	Yes	To make a console connection from UART1 port of the board
USB-to-serial adapter	No	To connect the serial port of DB9 cable to the USB port of the host computer
Cat-6 Ethernet cable	Yes	To connect the board to network to get updated board software
CodeWarrior TAP (optional)	No	To debug and control the board using the CodeWarrior IDE
Software		
USB to serial/UART/RS-232 driver	No	Download and install on the host computer from Internet
Tera Term (serial terminal emulator)	No	Download and install on the host computer from Internet
TFTP server	No	Download and install on the host computer from Internet

10.2 Booting LX2160ARDB

When power is supplied to the board, then the boot loader (U-Boot) image located in FlexSPI NOR flash DEV#0 runs, if the board is configured with the default switch settings.

Follow these steps to boot the board:

1. Ensure that you have met the prerequisites described in Table 14.
2. Open the chassis top cover and ensure that the board is configured with the default switch settings, as mentioned in Table 13.
3. Verify that the board has default jumper settings (see Jumpers).

4. Connect one end of the AC power cord to the wall mount power switch and the other end of the cable to the power jack available on the chassis back panel, as shown in the figure below.

Figure 6. Power supply connection

NOTE

As a precautionary step, the power switch mounted on the wall (if available) must be turned off before connecting the power cord.

5. Turn on the wall mount power switch. The D28 LED (3VSB) turns ON when the standby power is available (see fgure below).

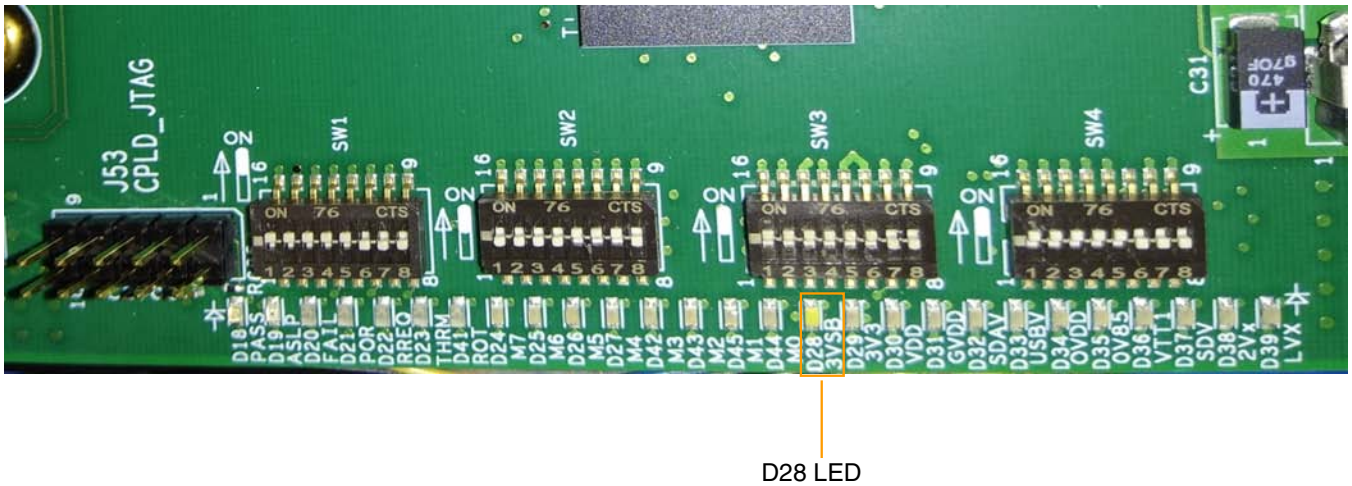

Figure 7. Standby power indicator

6. Connect one end of the DB9 female to DB9 female cable to the UART1 port available on chassis front panel (see figure below) and the other end of the cable to the USB-to-serial adapter. Connect the other end of the USB-to-serial adapter to the USB port of the host machine. This connection allows you to make a console connection between the board and host computer to see the console output.

Figure 8. Console connection

7. Optionally, connect the CodeWarrior TAP to the board by performing the following steps:

NOTE

Follow the instructions included with the CodeWarrior package to set up the environment and host attachment, such as USB and Ethernet.

a. Connect the 10-pin micro adapter (CWH-CTP-CTX10-YE), provided with the CodeWarrior TAP, to the CodeWarrior TAP.
b. Connect one end of the 10-wire cable (gray ribbon cable) to the 10-pin micro adapter (both ends of the wire are keyed and can be connected on either side).
c. Connect the other end of the 10-wire cable to the 10-pin Arm JTAG header (J11) on the board, as shown in the figure below.

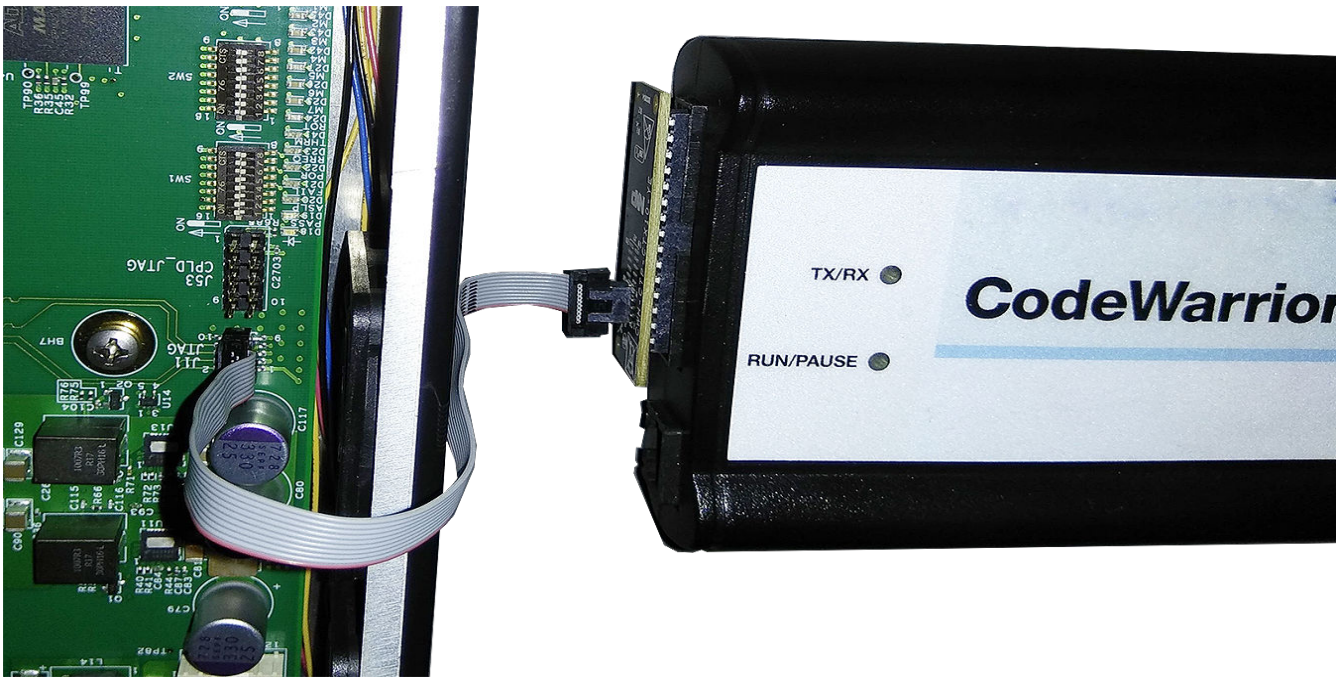

Figure 9. CodeWarrior TAP connection

NOTE

Pin 1 of the gray ribbon cable connector should align with pin 1 of the debug port header on the board.

8. Optionally, connect the Ethernet cable if you want to connect your board to the network, for example, for obtaining latest board software and updating board images.
9. Set up Tera Term on the host computer:
    a. Start Tera Term. The Tera Term console appears along with the **Tera Term: New connection** dialog.
    b. On the **Tera Term: New connection** dialog, select the **Serial** option, and ensure that **COM: USB-to-Serial Comm Port** is selected in the **Port** menu.
    c. Click **OK** to close the **Tera Term: New connection** dialog.
    d. Choose **Setup > Serial port** from the Tera Term console menu bar. The **Tera Term: Serial port setup** dialog appears.
    e. On the **Tera Term: Serial port setup** dialog, configure the serial port of the host computer with the following settings:
        - Baud rate: 115200
        - Data: 8 bit
        - Parity: none
        - Stop: 1 bit
        - Flow control: none
    f. Click **OK** to close the **Tera Term: Serial port setup** dialog and complete setting up Tera Term. This configuration sets a console connection between the board and the host computer.
10. Press the power button available on the chassis front panel. The status LEDs on the PCB run through various patterns while powering up the board. The board boots up and the console shows the U-Boot messages as given below:

```
U-Boot 2017.07+fsl+g3861b57 (Sep 10 2018 - 00:49:18 +0000)

SoC:  LX2160ACE Rev1.0 (0x87360010)
Clock Configuration:
       CPU0(A72):1900 MHz  CPU1(A72):1900 MHz  CPU2(A72):1900 MHz
       CPU3(A72):1900 MHz  CPU4(A72):1900 MHz  CPU5(A72):1900 MHz
       CPU6(A72):1900 MHz  CPU7(A72):1900 MHz  CPU8(A72):1900 MHz
       CPU9(A72):1900 MHz  CPU10(A72):1900 MHz  CPU11(A72):1900 MHz
```

```
       CPU12(A72):1900 MHz  CPU13(A72):1900 MHz  CPU14(A72):1900 MHz
       CPU15(A72):1900 MHz
       Bus:      600  MHz  DDR:      2600 MT/s
Reset Configuration Word (RCW):
       00000000: 4c6b6b30 244c004c 00000000 00000000
       00000010: 00000000 0e010000 00000000 00000000
       00000020: 010001a0 00002580 00000000 00000096
       00000030: 00000000 00000000 00000000 00000000
       00000040: 00000000 00000000 00000000 00000000
       00000050: 00000000 00000000 00000000 00000000
       00000060: 00000000 00000000 00027000 00000000
       00000070: 08b30010 001d0020
Model: NXP Layerscape LX2160ARDB Board
Board: LX2160ACE Rev1.0-RDB, Board version: B, boot from FlexSPI DEV#0
FPGA: v1.8
SERDES1 Reference: Clock1 = 161.13MHz Clock2 = 161.13MHz
SERDES2 Reference: Clock1 = 100MHz Clock2 = 100MHz
SERDES3 Reference: Clock1 = 100MHz Clock2 = 100Hz
I2C:   ready
DRAM:  Initializing DDR....using SPD
Detected UDIMM 18ASF1G72AZ-2G6B1
Detected UDIMM 18ASF1G72AZ-2G6B1
DDR4(0) UDIMM with 2-rank 64-bit bus (x8)
DDR4(1) UDIMM with 2-rank 64-bit bus (x8)
15.9 GiB
DDR    15.9 GiB (DDR4, 64-bit, CL=19, ECC on)
       DDR Controller Interleaving Mode: 256B
       DDR Chip-Select Interleaving Mode: CS0+CS1
VID: Core voltage after adjustment is at 799 mV
PPA Firmware: Version fsl-sdk-v2.0-1703-137-gb0a07cf
Using SERDES1 Protocol: 19 (0x13)
Using SERDES2 Protocol: 5 (0x5)
Using SERDES3 Protocol: 2 (0x2)
MMC:   FSL_SDHC: 0, FSL_SDHC: 1
SF: Detected mt35xu512g with page size 256 Bytes, erase size 128 KiB, total 64 MiB
EEPROM: NXID v1
In:    serial@21c0000
Out:   serial@21c0000
Err:   serial@21c0000
SATA link 0 timeout.
AHCI 0001.0301 32 slots 1 ports 6 Gbps 0x1 impl SATA mode
flags: 64bit ncq pm clo only pmp fbss pio slum part ccc apst
Found 0 device(s).
SCSI:  Net:
CS4223: Using software initialization...
FSL_MDIO1:0 is connected to DPMAC5@25g-aui.  Reconnecting to DPMAC6@25g-aui
PCIe0: pcie@3400000 disabled
PCIe1: pcie@3500000 disabled
PCIe2: pcie@3600000 Root Complex: x1 gen1
PCIe3: pcie@3700000 disabled
PCIe4: pcie@3800000 Root Complex: no link
PCIe5: pcie@3900000 disabled
e1000: 68:05:ca:15:c5:39
       DPMAC2@xlaui4, DPMAC3@xgmii, DPMAC4@xgmii, DPMAC5@25g-aui, DPMAC6@25g-aui,
DPMAC17@rgmii-id, DPMAC18@rgmii-id, e1000#0
crc32+
fsl-mc: Booting Management Complex ... SUCCESS
fsl-mc: Management Complex booted (version: 10.11.0, boot status: 0x1)
Hit any key to stop autoboot:  0
=>
```

NOTE

The above U-Boot log is an example log; the actual U-Boot log may vary slightly depending on the BSP version available with the board.

11 Ethernet port mapping

The LX2160ARDB has seven Ethernet ports that are available on the chassis front panel (see Figure 1). Each Ethernet port is marked with a label on the chassis front panel. Each port is assigned with a name in U-Boot that displays in U-Boot log (see Booting LX2160ARDB). The mapping of Ethernet port names between chassis and U-Boot is shown in the table below.

Table 15. Ethernet port mapping

Identifier on board	Port name on chassis	Interface name in U-Boot	Description
J18	40G MAC2	DPMAC2@xlaui4	40G MAC2 QSFP+ port
J21	10G MAC3	DPMAC3@xgmii	10G MAC3 USXGMII port
J22	10G MAC4	DPMAC4@xgmii	10G MAC4 USXGMII port
J19	25G MAC5	DPMAC5@25g-aui	25G MAC5 SFP port
	25G MAC6	DPMAC6@25g-aui	25G MAC6 SFP port
P1	1G MAC17	DPMAC17@rgmii-id	1G MAC17 RGMII port
	1G MAC18	DPMAC18@rgmii-id	1G MAC18 RGMII port

NOTE

DPMAC is a DPAA2 object that identifies the physical interface.

In Linux, only one MAC is enabled by default as a standard kernel Ethernet interface. This interface is named ni0 by default and it is created automatically by the default data path layout (DPL) prior to Linux boot.

12 Flash image layout

The table below shows the memory layout of various firmware stored in FlexSPI flash device and SD memory card on the LX2160ARDB.

Table 16. Flash image layout

Definition		Max. size	FlexSPI NOR flash offset	SD card start block number
RCW+PBI		1 MB	0x00000000	0x00008
Boot firmware (U-Boot)		2 MB	0x00100000	0x00800
Boot firmware environment		1 MB	0x00300000	0x01800
PPA firmware		2 MB	0x00400000	0x02000
DDR PHY firmware (firmware.itb)		1 MB	0x00800000	0x04000
DPAA2 MC firmware		3 MB	0x00A00000	0x05000
DPAA2 DPL		1 MB	0x00D00000	0x06800
DPAA2 DPC		1 MB	0x00E00000	0x07000
Kernel	kernel-lx2160ardb.itb	16 MB	0x01000000	0x08000
Ramdisk RFS		32 MB	0x02000000	0x10000

13 Upgrading BSP images in LX2160ARDB

This section explains how to upgrade the BSP images in the LX2160ARDB using a prebuilt LX2160ARDB composite firmware image.

Perform the following steps to upgrade the BSP images in the LX2160ARDB:

1. Get the latest LX2160A BSP from your local NXP FAE or sales representative.
2. Copy the LX2160ARDB composite firmware image (`LX2160A_SDK_LX2160ARDB_20180912_XSPI_Flash.bin`) to the TFTP server to download it to the LX2160ARDB.

NOTE

The LX2160ARDB composite firmware image includes RCW+PBI, U-Boot, U-Boot environment, PPA, DDR PHY firmware, DPAA2 MC firmware, DPAA2 DPL, DPAA2 DPC, and kernel + Ramdisk root file system images.

3. Connect anyone of the six Ethernet ports on the chassis front panel to the TFTP server.
4. Start and configure Tera Term.
5. With the default switch settings, boot the board to show U-Boot log. The board boots from FlexSPI NOR flash DEV#0 device.
6. Press any key to stop autoboot.
7. Configure U-Boot environment variables:

```
setenv serverip <ipaddress1>
setnev ipaddr <ipaddress2>
saveenv
```

8. Set `ethact` to the Ethernet port that is connected to the TFTP server. Suppose, 10G MAC3 port is connected to TFTP, then use the following commands:

```
setenv ethact 'DPMAC3@xgmii'
saveenv
```

NOTE

For mapping between Ethernet port names on chassis front panel and Ethernet interface names in U-Boot, see Ethernet port mapping.

9. Run the following command to check the connection between the board and TFTP server:

```
ping $serverip
```

10. If the server connection is working properly, then use the following commands to overwrite existing binaries in FlexSPI NOR flash DEV#1 device:
    a. Select FlexSPI NOR flash DEV#1 device:

```
$i2c mw 66 50 20; sf probe 0:0;
```

    b. Download the LX2160ARDB composite firmware image to the LX2160ARDB:

```
$tftp a0000000 <path>/LX2160A_SDK_LX2160ARDB_20180912_XSPI_Flash.bin
```

NOTE

The name of the LX2160ARDB composite firmware image may vary slightly depending on the version of the LX2160A BSP.

    c. Program the LX2160ARDB composite firmware image on FlexSPI NOR flash DEV#1 device to overwrite existing binaries:

```
$sf erase 0 +4000000; sf write a0000000 0 4000000;
```

d. Switch to FlexSPI NOR flash DEV#1 device using one of the following ways:
   - By running the following U-Boot command:

```
$qixis_reset altbank
```

   - By changing board switch settings: Power off the board, change SW1[6:8] settings from 000 to 001, and power on the board. U-Boot will now boot from FlexSPI NOR flash DEV#1 device.

14 Troubleshooting

This section explains the basic troubleshooting tips for the LX2160ARDB.

14.1 U-Boot log not displaying

Perform the following steps in case console is not showing any print:

- Ensure that the board is configured for the default switch settings, as described in Table 13.
- Ensure that the power cord is connected to the power jack.
- Check D28 LED (3VSB) to verify standby power. It should be ON.
- Ensure that the cables making console connection are properly connected as mentioned in Booting LX2160ARDB.
- Ensure that Tera Term has communication settings as mentioned in section Booting LX2160ARDB.
- Press the reset button. The U-Boot log should be available on the console.
- If U-Boot log is still not showing on console, then the BSP image available in the current FlexSPI NOR flash device (DEV#0) may be corrupt. Try to boot the board from alternative flash device (DEV#1) by powering off the board, changing SW1[6:8] settings from 000 to 001, and then powering on the board.
- If U-Boot log is still not showing on console, then the BSP images on both DEV#0 and DEV#1 may be corrupt. Use CodeWarrior TAP to flash new images and recover the board. For details, see CodeWarrior TAP Probe User Guide.

15 Revision history

The table below summarizes the revisions to this document.

Table 17. Revision history

Revision	Date	Topic cross-reference	Change description
Rev. 0	09/2018		Initial public release

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