How to switch to int. OSC when ext.OSC is lost?

Target on S08PA/PT

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External Use

Agenda

- Trouble Shooting
- Test Result
- Conclusion

Trouble Shooting

- Q: How to switch to internal OSC for keeping application execution if the external OSC clock signal is gone?
  - A: Consider to use external clock monitor to reset MCU but checked the S08PA RM that there is a SYS_SRS[CLK] error as below:

8.2.3.2 External reference clock monitor

In FBE, FEE, FEI, or FBI modes, if ICS_C4[CME] bit is written to 1, the clock monitor is enabled. If the external reference falls below a certain frequency, such as f_{loc_high} or f_{loc_low} depending on the ICS_OSCSC[RANGE] bit, the MCU will reset. The SYS_SRS[CLK] bit will be set to indicate the error.

In FBELP or FBILP modes, the FLL is not on, so the external reference clock monitor will not function even if ICS_C4[CME] bit is written to 1.

External reference clock monitor uses FLL as the internal reference clock. The FLL must be functional before ICS_C4[CME] bit is set.

Address: 3000h base + 0h offset = 3000h

Bit	7	6	5	4	3	2	1	0
Read	POR	PIN	WDOG	ILOP	ILAD	LOC	LVD	0
Write								
Reset	1	0	0	0	0	0	1	0

SYS_SRS field descriptions

Trouble Shooting

- There is a clue in RM to indicate that SYS_SRS[CLK] bit should be SYS_SRS[LOC] bit:

This device has the following sources for reset:

- Power-on reset (POR)
- Low-voltage detect (LVD)
- Watchdog (WDOG) timer
- Illegal opcode detect (ILOP)

System options

- Illegal address detect (ILAD)
- Background debug forced reset
- External reset pin (RESET)
- Internal clock source module reset (CLK)

Address: 3000h base + 0h offset = 3000h

Bit	7	6	5	4	3	2	1	0
Read	POR	PIN	WDOG	ILOP	ILAD	LOC	LVD	0
Write								
Reset	1	0	0	0	0	0	1	0

SYS_SRS field descriptions

2 LOC	Internal Clock Source Module Reset Reset was caused by an ICS module reset.

Table continues on the next page...

SYS_SRS field descriptions (continued)

Field	Description
	0 Reset not caused by ICS module. 1 Reset caused by ICS module.

Test Result

- Tested on TWR-S08PT60, ICS_S[LOLS] may not working including interrupt when we remove ext. OSC in FBE mode.
- Observe that FEE can switch to FEI automatically, but not sure that FBE can auto switch to FBI due to the internal OSC is only 31.25KHz which is far from the 8MHz external OSC.

Conclusion

- Consult with Freescale product expert that:
  - The ICS_S[LOLS] is not used for this purpose, it is used to determine FLL lock status when switch to one of FLL active clock mode.
  - It is a RM error on SYS_SRS[CLK] bit, it should be SYS_SRS[LOC] bit.
  - If you do not enable CME in external clock mode, you will find it will automatically switch to FEI mode from FEE.
  - For FBE, it is not switched to FBI. It is stalling in this mode until external clock is active as system has no clock, after external clock active, program resumes execution.

- For high precision clock requirement application, set ICS_C4[CME] to reset MCU automatically then check SYS_SRS[LOC] to see whether it is lost of external clock is a safety way.

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