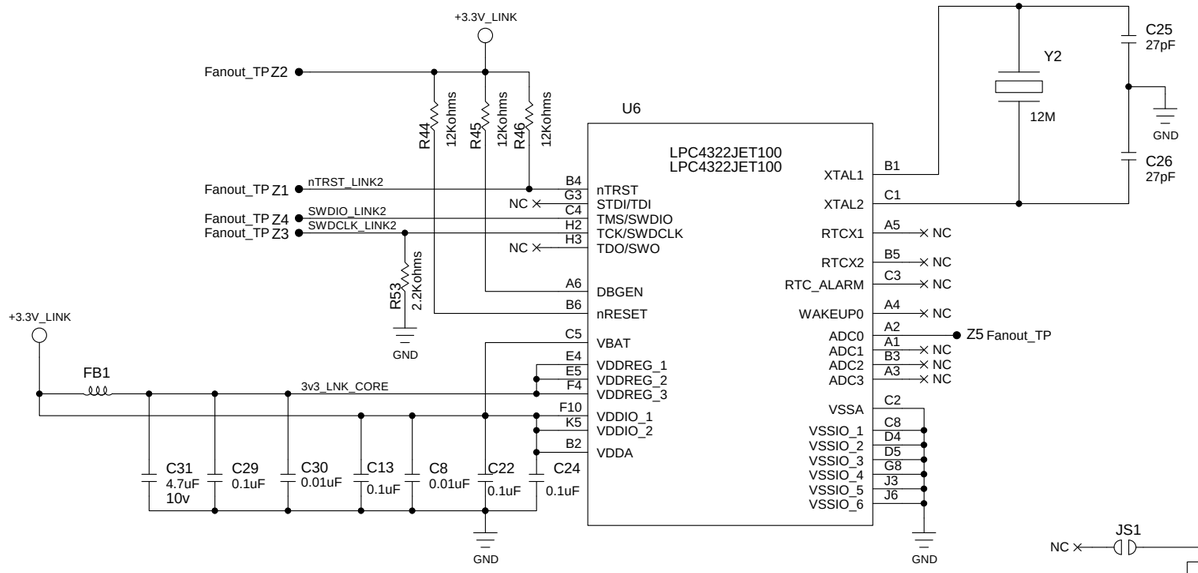
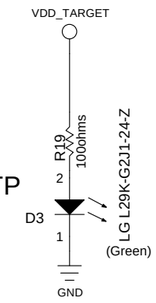
DWG. NO.	SH.	REV.
LPCX1125 LQFP48	1	A

REVISIONS

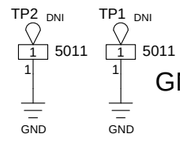
REV	DESCRIPTION	DATE	APPROVED
1	- Reorder RefDes, Release proto build	10/22/2014	
1c	- Install JP5 hdr; sht 2 - Change value of R8 & R9 to 750ohm; sht 4	11/13/2014	
A	- Release to production; no change from rev 1c	12/4/2014	



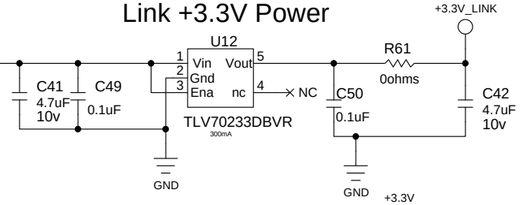
Power-On LED



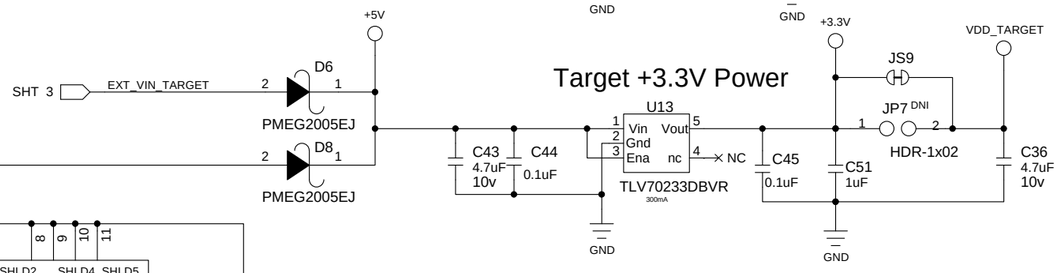
GND TP



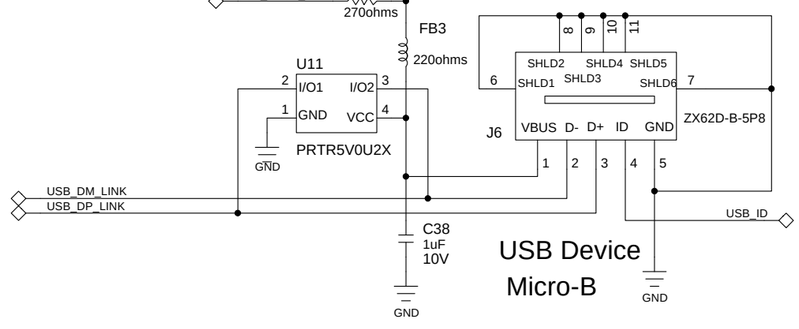
Link +3.3V Power



Target +3.3V Power



USB Device Micro-B



CONTRACT NO.		LINK2 LPC432x
APPROVALS	DATE	**NXP** Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/
DRAWN d.consiglio	12/4/2014	
CHECKED		
ISSUED	12/04/14	SIZE D · FSCM NO. · DWG. NO. LPCX1125 LQFP48 · REV A
		SCALE · SHEET 1 OF 05

H=8ND; V=4LA

DWG. NO. LPCX1125 LQFP48 | SH. 2 | REV. A

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

U6
LPC4322JET100
LPC4322JET100

TRACE_D0 G2
TRACE_D1 G1
P0[0]_/GPIO0[0]/SSP1_MISO/ENET_RXD1/SGPIO0
P0[1]_/GPIO0[1]/SSP1_MOSI/ENET_TXEN/SGPIO1

NC CUR_MEAS_SEL H1
BOOT0_LED K2
BOOT1 K1
NC BRIDGE_MISO JS8 J1
NC BRIDGE_MOSI JS12 J2
TMS_SWDIO_TXEN J4
TMS_SWDIO K4
G4
NC H5
NC J5
NC BRIDGE_INTR JS7 H6
NC J7
NC K7
TRACE_CLK H8
NC J8
TDO_SWO K8
TRACE_D2 H9
TRACE_D3 J10
TCK_SWCLK H10
JTAG_TDI J10
NC BRIDGE_SCK JS6 K9
NC BRIDGE_SSEL JS4 K10

P1[0]_/GPIO0[4]/CTIN_3/EXTBUS_A5
P1[1]_/GPIO0[8]/CTOUT_7/EXTBUS_A6/SGPIO8
P1[2]_/GPIO0[9]/CTOUT_6/EXTBUS_A7/SGPIO9
P1[3]_/GPIO0[10]/CTOUT_8/SGPIO10/EXTBUS_OE
P1[4]_/GPIO0[11]/CTOUT_9/SGPIO11/EXTBUS_BLS0
P1[5]_/GPIO1[8]/CTOUT_10/NC/EXTBUS_CS0
P1[6]_/GPIO1[9]/CTIN_5/NC/EXTBUS_WE
P1[7]_/GPIO1[0]/U1_DSR/CTOUT_13/EXTBUS_D0
P1[8]_/GPIO1[1]/U1_DTR/CTOUT_12/EXTBUS_D1
P1[9]_/GPIO1[2]/U1_RTS/CTOUT_11/EXTBUS_D2
P1[10]_/GPIO1[3]/U1_RI/CTOUT_14/EXTBUS_D3
P1[11]_/GPIO1[4]/U1_CTS/CTOUT_15/EXTBUS_D4
P1[12]_/GPIO1[5]/U1_DCD/NC/EXTBUS_D5
P1[13]_/GPIO1[6]/U1_TXD/NC/EXTBUS_D6
P1[14]_/GPIO1[7]/U1_RXD/NC/EXTBUS_D7
P1[15]_/GPIO0[2]/U2_TXD/SGPIO2/ENET_RXD0
P1[16]_/GPIO0[3]/U2_RXD/SGPIO3/ENET_RX_DV
P1[17]_/GPIO0[12]/U2_UCLK/NC/ENET_MDIO
P1[18]_/GPIO0[13]/U2_DIR/NC/ENET_TXD0
P1[19]_/ENET_TX_REF_CLK/SSP1_SCK/CLKOUT/I2S1_RX_SCK
P1[20]_/GPIO0[15]/SSP1_SSEL/NC/ENET_TXD1

U6
LPC4322JET100
LPC4322JET100

TARGET_UART_RXD G10
TARGET_UART_TXD G7
TARGET_UART_CTRL F5
D8
NC D9
NC D10
JTAG_RESET G9
JTAG_RESET_TXEN C10
BOOT_FLASH C6
BOOT2 B10
BOOT3 E8
NC ISP_CTRL A9
B9
IF_DETECT R28 NC A10
1.5Kohms
A8
NC F7
NC G6
NC SSP0_SCK_LINK A7
B8
NC B7
NC SSP0_MISO_LINK C7
NC SSP0_MOSI_LINK D7
NC SSP0_SSEL_LINK E7

P2[0]_/SGPIO4/U0_TXD/EXTBUS_A13/USB0_PWR_EN
P2[1]_/SGPIO5/U0_RXD/EXTBUS_A12/USB0_PWR_FAULT
P2[2]_/SGPIO6/U0_UCLK/EXTBUS_A11/USB0_IND1
P2[3]_/SGPIO12/I2C1_SDA/U3_TXD/CTIN_1
P2[4]_/SGPIO13/I2C1_SCL/U3_RXD/CTIN_0
P2[5]_/SGPIO14/CTIN_2/USB1_VBUS/ADCTRIG1
P2[6]_/SGPIO7/U0_DIR/EXTBUS_A10/USB0_IND0
P2[7]_/GPIO0[7]/CTOUT_1/U3_UCLK/EXTBUS_A9
P2[8]_/SGPIO15/CTOUT_0/U3_DIR/EXTBUS_A8/GPIO5[7]
P2[9]_/GPIO1[10]/CTOUT_3/U3_BAUD3/EXTBUS_A0
P2[10]_/GPIO0[14]/CTOUT_2/U2_TXD/EXTBUS_A1
P2[11]_/GPIO1[11]/CTOUT_5/U2_RXD/EXTBUS_A2
P2[12]_/GPIO1[12]/CTOUT_4/NC/EXTBUS_A3
P2[13]_/GPIO1[13]/CTIN_4/NC/EXTBUS_A4

P3[0]_/I2S0_RX_SCK/I2S0_RX_MCLK/I2S0_TX_SCK/I2S0_TX_MCLK
P3[1]_/I2S0_TX_WS/I2S0_RX_WS/CAN0_RD/USB1_IND1/GPIO5[8]
P3[2]_/I2S0_TX_SDA/I2S0_RX_SDA/CAN0_TD/USB1_IND0/GPIO5[9]
P3[3]_//SPI_SCK/SSP0_SCK/SPIFI_SCK
P3[4]_/GPIO1[14]///SPIFI_SIO3
P3[5]_/GPIO1[15]///SPIFI_SIO2
P3[6]_/GPIO0[6]/SPI_MISO/SSP0_SSEL/SPIFI_MISO
P3[7]_//SPI_MOSI/SSP0_MISO/SPIFI_MOSI
P3[8]_//SPI_SSEL/SSP0_MOSI/SPIFI_CS

U6
LPC4322JET100
LPC4322JET100

NC H7
NC G5
J9
F6
NC F9
F8
C9
H4

P6[0]_/I2S0_RX_MCLK///I2S0_RX_SCK
P6[1]_/GPIO3[0]/EXTBUS_nDYCS1/U0_UCLK/I2S0_RX_WS
P6[2]_/GPIO3[1]/EXTBUS_CKEOUT1/U0_DIR/I2S0_RX_SDA
P6[4]_/GPIO3[3]/CTIN_6/U0_TXD/EXTBUS_nCAS
P6[5]_/GPIO3[4]/CTOUT_6/U0_RXD/EXTBUS_nRAS
P6[9]_/GPIO3[5]/NC/NC/EXTBUS_nDYCS0
P6[11]_/GPIO3[7]/NC/NC/EXTBUS_CKEOUT0
PF[4]_/SSP1_SCK/SPIFI_CLKIN/TRACECLK///I2S_TX_MCLK/I2S_RX_MCLK

R40 2.2Kohms DNI
R38 2.2Kohms DNI
R39 2.2Kohms DNI
R37 2.2Kohms
GND

Buffer Pwr Select (JP2)
On-board Target 1 - 2 (default)
Off-board Target 2 - 3

VDD_TARGET
M1
JP2 HDR-1x03
D2 PMEG2005EJ

+3.3V_LINK
U5
SN74AVC2T45DCTR
SN74AVC2T45DCTR
TCK_SWCLK
JTAG_TDI
R42 100Kohms
VDD_TRGT_SWD
R31 100ohms
IF_TCK_SWCLK
R41 100ohms
IF_JTAG_TDI
C9 0.1uF
GND

U7
74LVC1T45GW
TDO_SWO
C10 0.1uF
R49 100Kohms
IF_TDO_SWO

U8
74LVC1T45GW
TMS_SWDIO
TMS_SWDIO_TXEN
C14 0.1uF
R50 100Kohms
R51 100ohms
IF_SWDIO_TRGT
R54 2.2Kohms

U1
74LVC1T45GW
JTAG_RESET
JTAG_RESET_TXEN
C1 0.1uF
R4 100Kohms
R5 100ohms
IF_RST
R6 2.2Kohms

+3.3V_LINK
U2
74LVC1G07GW
ISP_CTRL
R16 100ohms
IF_ISPEN

Target (LPC1125)
SWD Debug

C4 10uF
P1
FTSH-105-01-L-DV-K
IF_SWDIO_TRGT SHT 4
IF_TCK_SWCLK
IF_TDO_SWO
IF_JTAG_TDI
IF_RST

IF_DETECT R17 0ohms

TRACE_CLK R29 DNI 0ohms NC
TRACE_D0 R26 DNI 0ohms NC
TRACE_D1 R25 DNI 0ohms NC
TRACE_D2 R30 DNI 0ohms NC
TRACE_D3 R27 DNI 0ohms NC

LPC1125 Target
does not have trace.

VDD_TARGET
C2 0.01uF
GND
R15 100Kohms
U3
NX3L2267GU,115
IF_TCK_SWCLK
IF_RST
SWDCLK_TRGT SHT 4
nRESET_TRGT SHT 4, 6
JP1 HDR-1x02

Target to debug location (JP1)
On-board Target - open (default)
Off-board Target - short

+3.3V_LINK
R34 2.2Kohms
R35 2.2Kohms
BOOT0_LED
BOOT1
BOOT2
BOOT3
R43 2.2Kohms
R56 2.2Kohms
R36 2.2Kohms
BOOT_FLASH
JP5 HDR-1x02
D5 LS Q976-NR-1
GND

Short JP3 to force DFU boot
(when internal flash is programmed)

LPC4322 Boot mode
DFU USB0 = B3:0 = 0101

VDD_TARGET
U10
74LVC1G3157GW
TARGET_UART_CTRL
SHT 5 P1_6-ISP_RX_FTDI
TARGET_UART_RXD
TO_MUX_P1_6-ISP_RX SHT 4
R55 2.2Kohms
GND

+3.3V_LINK
VDD_TARGET
U4
74LVC1T45GW
C5 0.1uF
TARGET_UART_TXD
R47 100ohms
P1_7-ISP_TX SHT 4, 5
GND

IF_ISPEN R18 0ohms P0_1-CT32B0_MAT2-ISP_EN SHT 4, 6

CONTRACT NO.		LINK LPC432x Peripheral	
APPROVALS	DATE	**NXP** Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
DRAWN d.consiglio	11/13/2014		
CHECKED			
ISSUED	12/04/14	SIZE D / FSCM NO. / DWG. NO. LPCX1125 LQFP48 / REV A	
		SCALE / SHEET 2 OF 05	

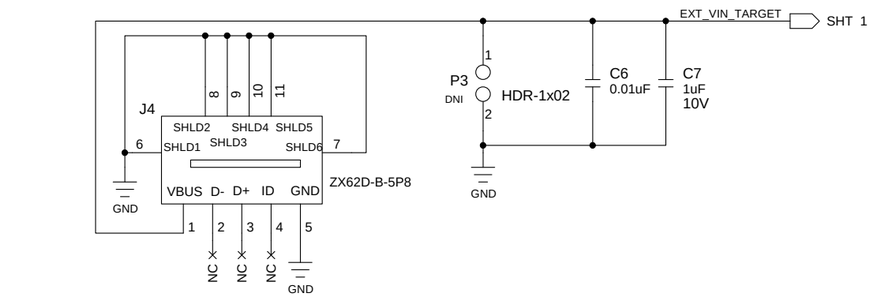
H:8ND; V:4LA

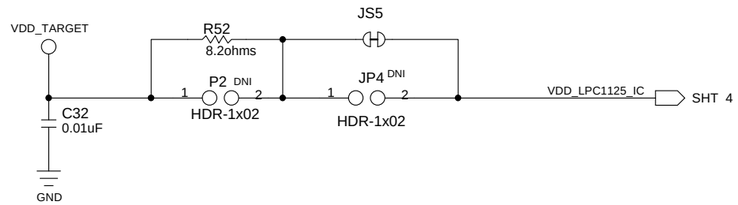
DWG. NO.	SH.	REV.
LPCX1125 LQFP48	3	A

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

Target External Vin 5V





CONTRACT NO.		Target LPC1125 Power	
APPROVALS	DATE	**NXP** Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
DRAWN d.consiglio	11/13/2014		
CHECKED			
ISSUED	12/04/14	SIZE D / FSCM NO. / DWG. NO. LPCX1125 LQFP48 / REV A	
		SCALE / SHEET 3 OF 05	

H=8ND; V=4LA

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

WAKEUP

KMR221GLFS SW2 — ISP Bootload Enable

R3 100ohms — P0_1-CT32B0_MAT2-ISP_EN

KMR221GLFS SW1

R2 100Kohms — VDD_TARGET

R1 100ohms — P1_4-WAKEUP-CT32B1_MAT3-BLUE

VDD_TARGET

JS13 — P1_10-ADC8

RV1 (CW)

C39 0.01uF

RESET

VDD_TARGET VDD_TARGET

R60 100Kohms

R20 100ohms

D4 LG L29K-G2J1-24-Z (Green)

SHT 2, 6 — nRESET_TRGT

R59 100ohms

SW3 KMR221GLFS

C40 0.01uF

RGB LED

VDD_TARGET

D1

P1_4-WAKEUP-CT32B1_MAT3-BLUE — R7 270ohms — Blue

P1_2-CT32B1_MAT1-GRN — R8 750ohms — Green

P1_1-CT32B1_MAT0-RED — R9 750ohms — Red

JS3 — JP3 DNI — HDR-1x02

HSMF-A341-A00J1

VDD_TARGET

R11 2.2Kohms

R10 2.2Kohms

U9

LPC1125JBD48

LPC1125JBD48

nRESET_TRGT	3	RESETn/P0_0
SHT 2, 6 — P0_1-CT32B0_MAT2-ISP_EN	4	P0_1/CLKOUT/CT32B0_MAT2
SHT 5 — BRIDGE_SSEL	10	P0_2/SSP0_SSEL/CT16B0_CAP0/ADC_PIN_TRIG0
SHT 6 — P0_3-U2_RXD	14	P0_3//U2_RXD
SHT 5, 6 — P0_4-I2C0_SCL	15	P0_4/I2C0_SCL
SHT 5, 6 — P0_5-I2C0_SDA	16	P0_5/I2C0_SDA
SHT 5 — BRIDGE_SCK	22	P0_6//SSP0_SCK/U1_TXD
SHT 6 — P0_7-ADC_PIN_TRIG1	23	P0_7/U0_CTS/ADC_PIN_TRIG1/U1_RXD
SHT 5 — BRIDGE_MISO	26	P0_8/SSP0_MISO/CT16B0_MAT0//ADC_PIN_TRIG2
SHT 5 — BRIDGE_MOSI	27	P0_9/SSP0_MOSI/CT16B0_MAT1//ADC_PIN_TRIG3
SHT 5 — SWDCLK_TRGT	28	SWCLK/P0_10/SSP0_SCK/CT16B0_MAT2
SHT 2 — P0_11-CT32B0_MAT3	30	R/P0_11/ADC_7/CT32B0_MAT3
SHT 6 — P1_0-ADC6	31	R/P1_0/ADC_6/CT32B1_CAP0
SHT 6 — P1_1-CT32B1_MAT0-RED	32	R/P1_1/ADC_5/CT32B1_MAT0
SHT 6 — P1_2-CT32B1_MAT1-GRN	35	R/P1_2ADC_4/CT32B1_MAT1
SHT 2 — IF_SWDIO_TRGT	38	SWDIO/P1_3/ADC_3/CT32B1_MAT2
SHT 6 — P1_4-WAKEUP-CT32B1_MAT3-BLUE	39	P1_4/WAKEUP/ADC_2/CT32B1_MAT3
SHT 6 — P1_5	45	P1_5/U0_RTS/CT32B0_CAP0
SHT 2 — TO_MUX_P1_6-ISP_RX	46	P1_6/U0_RXD/CT32B0_MAT0
SHT 2, 5 — P1_7-ISP_TX	47	P1_7/U0_TXD/CT32B0_MAT1
SHT 6 — P1_8-U2_TXD	9	P1_8/CT16B1_CAP0//U2_TXD
SHT 6 — P1_9-SPI1_MOSI-CT16B1_MAT0	17	P1_9/CT16B1_MAT0/SSP1_MOSI
SHT 6 — P1_10-ADC8	29	P1_10/ADC_8/CT16B1_MAT1/SSP1_MISO
SHT 6 — P1_11-ADC1	42	P1_11/ADC_1/CT32B1_CAP1

ABLS2-12.000MHZ-D4Y-T

C20 27pF

Y1 DNI

12M

C19 27pF

6	XTALIN	
7	XTALOUT	
2	P2_0/U0_DTRn/SSP1_SSEL/ADC_PIN_TRIG4	P2_0-SSP1_SSEL-ADC_PIN_TRIG4 — SHT 6
13	P2_1/U0_DSR/SSP1_SCK	P2_1-SPI1_SCK — SHT 6
25	P2_2/U0_DCDn/SSP1_MISO	P2_2-SPI1_MISO — SHT 6
37	P2_3/U0_RIn/SSP1_MOSI	BRIDGE_INTR — SHT 5
19	P2_4/CT16B1_MAT1/SSP1_SSEL	P2_4-SPI1_SSEL-CT16B1_MAT1 — SHT 6
20	P2_5/CT32B0_MAT0/	P2_5-CT32B0_MAT0 — SHT 6
1	P2_6/CT32B0_MAT1	P2_6-CT32B0_MAT1 — SHT 6
11	P2_7/CT32B0_MAT2/U0_RXD	P2_7-CT32B0_MAT2 — SHT 6
12	P2_8/CT32B0_MAT3/U0_TXD	P2_8-CT32B0_MAT3 — SHT 6
24	P2_9/CT32B0_CAP0	BRIDGE_GPIO — SHT 5
36	P3_0/U0_DTRn/CT16B0_MAT0/U0_TXD	P3_0-CT16B0_MAT0 — SHT 6
48	P3_3/U0_RIn/CT16B0_CAP0	P3_3 — SHT 6
18	P3_4/CT16B0_CAP1/U0_RXD	P3_4-U0_RXD — SHT 6
21	P3_5/CT16B1_CAP1/U0_TXD	P3_5-U0_TXD — SHT 6
8, 44	VDD_0, VDD_1	VDD_LPC1125_IC — SHT 3
43, 33	VDDA, VREFP	FB2
5, 41	VSS_0, VSS_1	C16 0.01uF; JS10; C33 0.1uF
40, 34	VSSA, VREFN	C17 0.01uF; JS11

C18 0.01uF; C34 47pF; C35 0.1uF; C15 1uF

JP6 DNI — HDR-1x03

GND

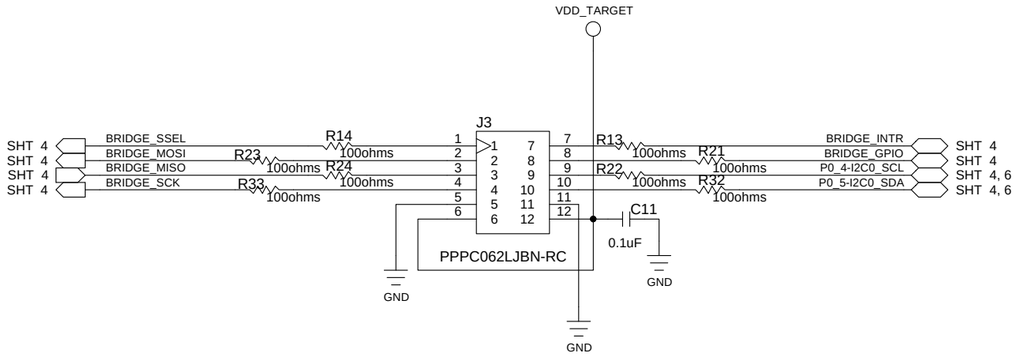
CONTRACT NO.		Target LPC1125 Peripheral	
APPROVALS	DATE	**NXP** Semiconductors	
DRAWN d.consiglio	11/13/2014	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
CHECKED			
ISSUED	12/04/14	SIZE D — FSCM NO. — DWG. NO. LPCX1125 LQFP48 — REV A	
		SCALE — SHEET 4 OF 05	

H=8ND; V=4LA

REVISIONS

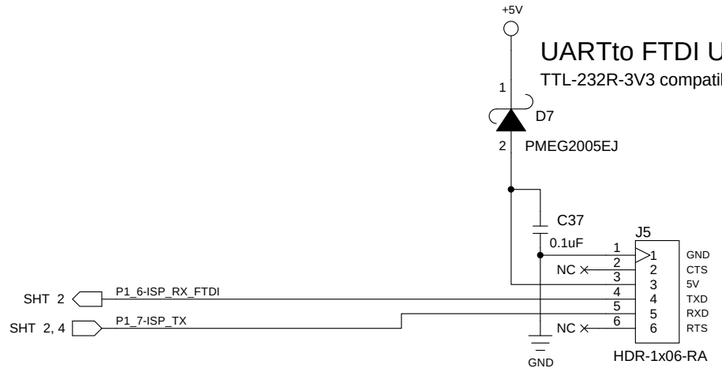
REV	DESCRIPTION	DATE	APPROVED

SPI / I2C brdge header (PMOD compatible)

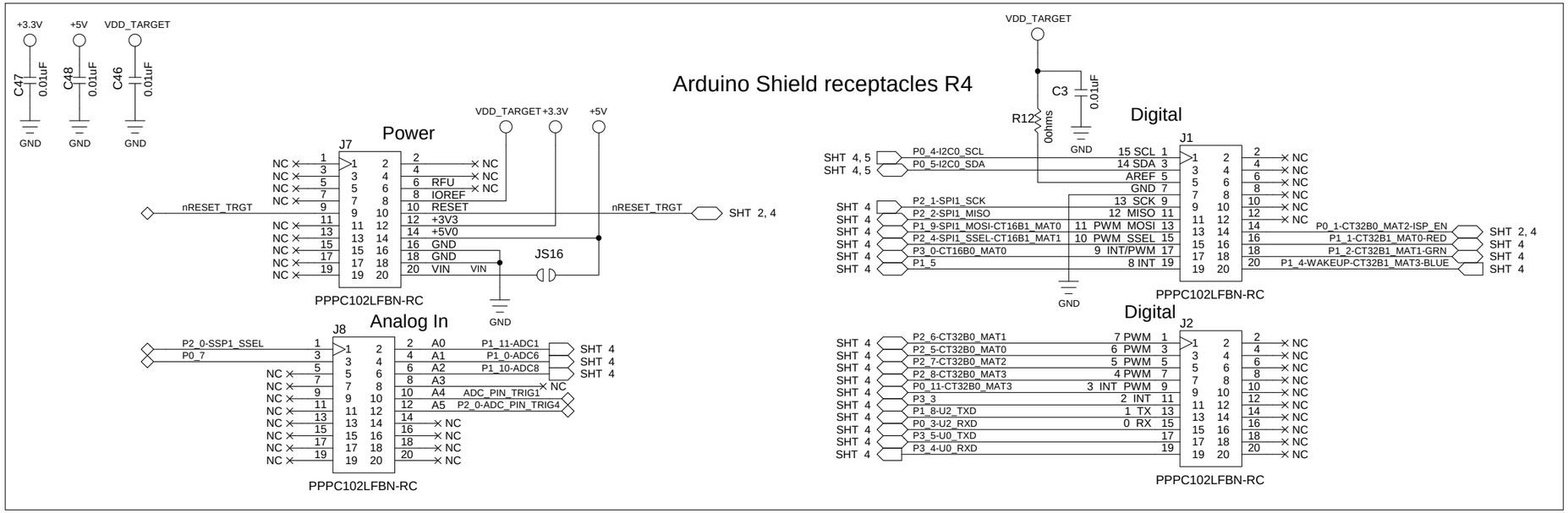


UARTto FTDI USB

TTL-232R-3V3 compatible



Arduino Shield receptacles R4



CONTRACT NO.		Pmod / FTDI / Arduino
APPROVALS	DATE	**NXP** Semiconductors
DRAWN d.consiglio	11/13/2014	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/
CHECKED		
ISSUED	12/04/14	SIZE D | FSCM NO. | DWG. NO. LPCX1125 LQFP48 | REV A
		SCALE | SHEET 5 OF 05

H=8ND, V=4LA