

NXP DEVKIT-S12XE

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Revisions			
Rev	Description	Designer	Date
X	Initial Draft A070 Release	J.Sanchez	05/29/15
A	Post Layout (Back Annotated)	J.Sanchez	
B	Prototype release	J.Sanchez	
C	I/O HEADERS and CAN interface updated	J.Sanchez	

CAUTION:

This schematic is provided for reference purposes only. As such, Freescale does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the NXP S12 family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

User notes are given throughout the schematics.

Specific PCB LAYOUT notes are detailed in ITALICS

3 Different test points used in design:

TPx - Test point pad

TPHx - Through Hole Pad Large (for standard 0.1" header). Also used on IO Matrix (IOMx)

TSx - Surface Mount Wire Loop



Notes:

- All components and board processes are to be ROHS compliant
- All connectors and headers are denoted Jx/Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx.
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always position 1-2.
- 2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

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5

4

3

2

1

D

D

C

C

B

B

A

A



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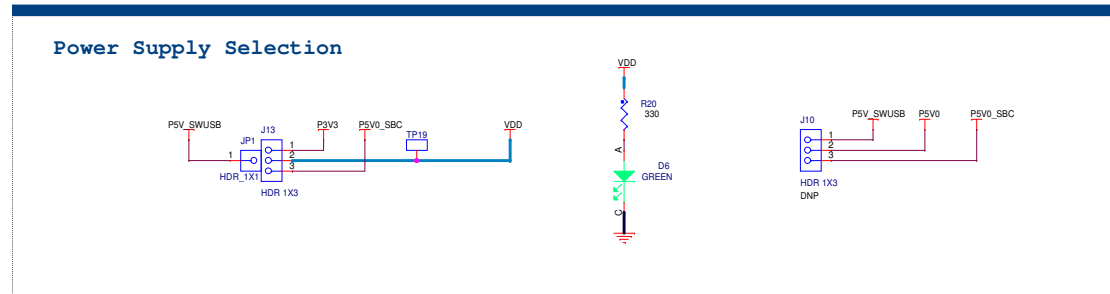
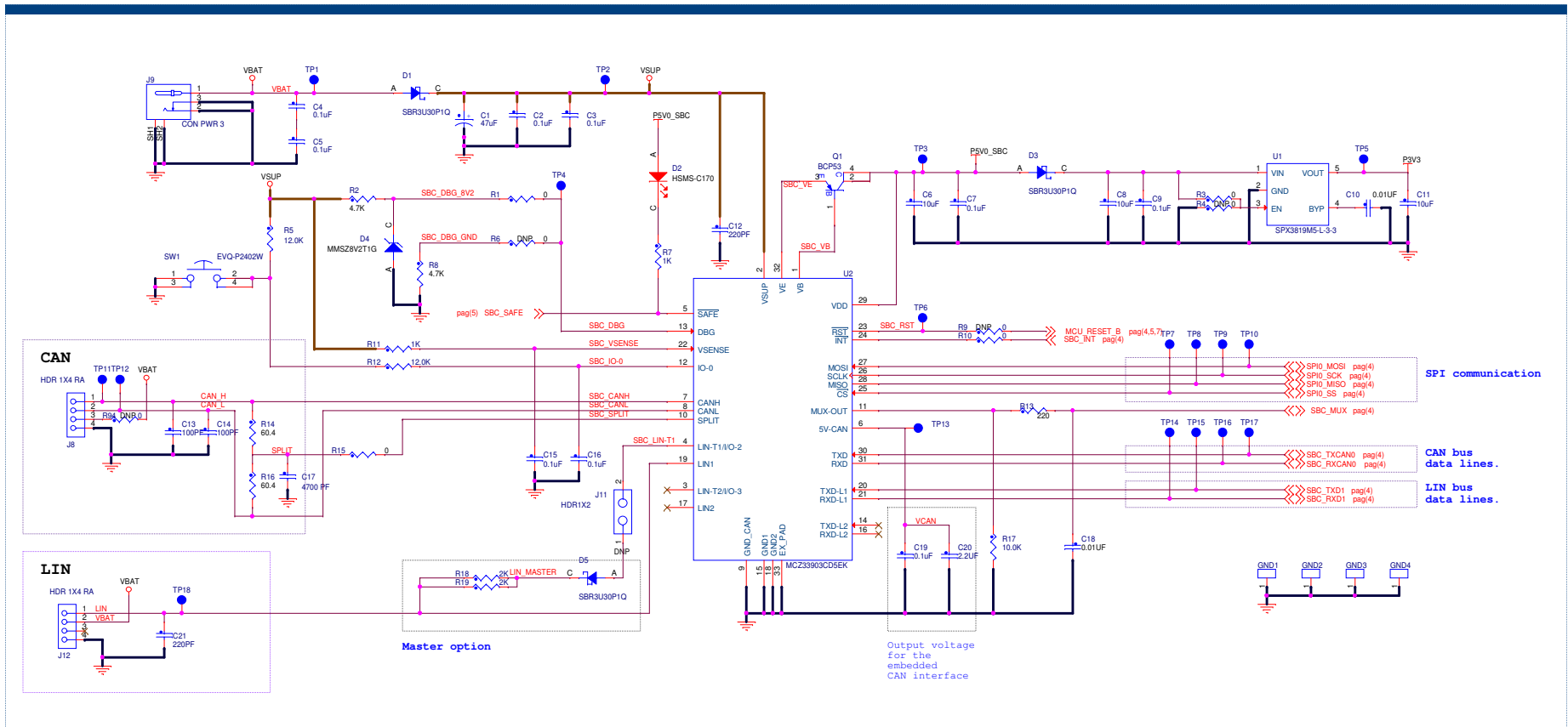
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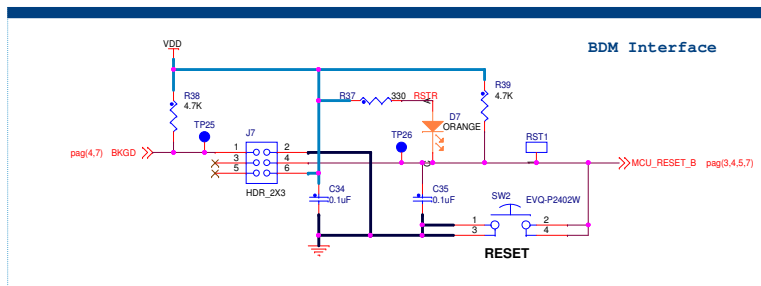
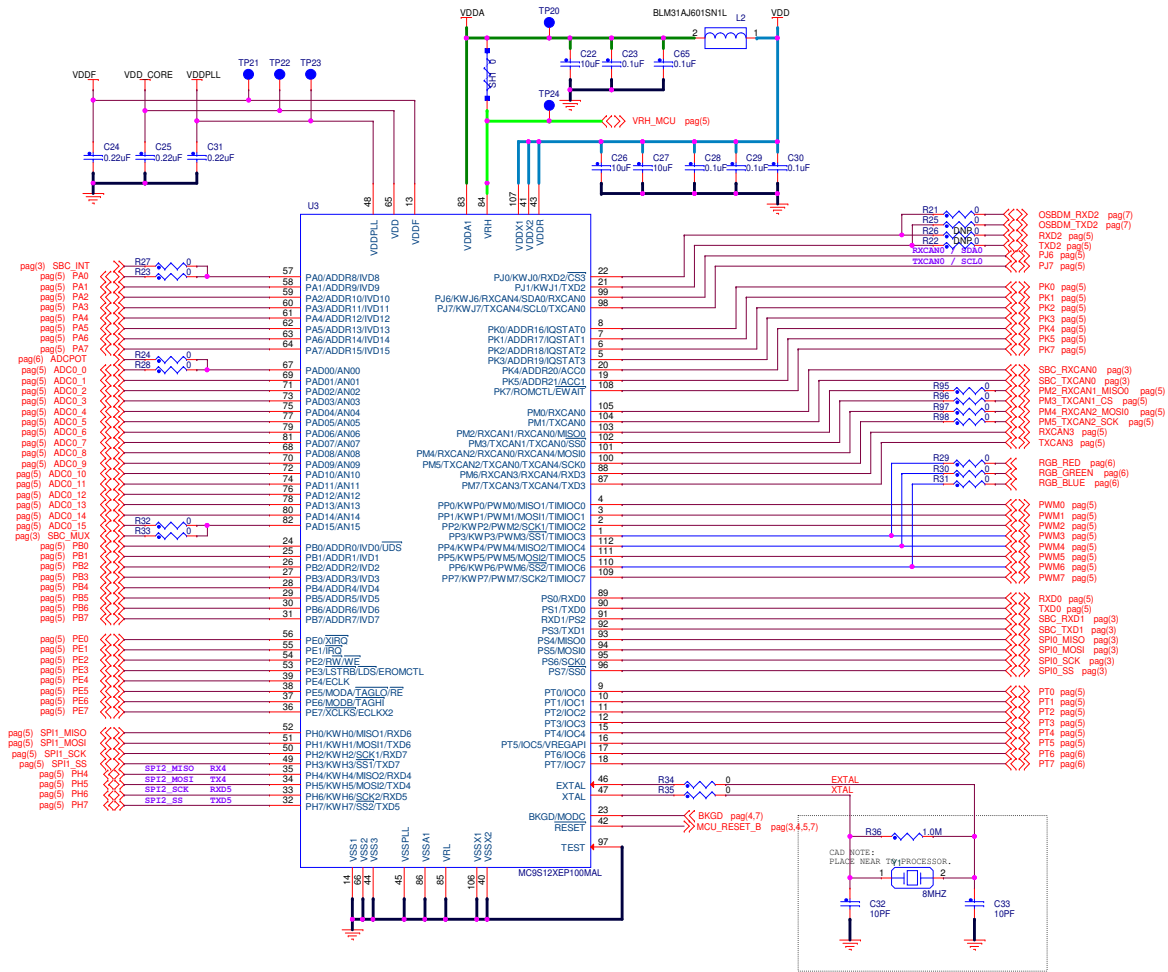
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DEVKIT-S12XE Power Supply

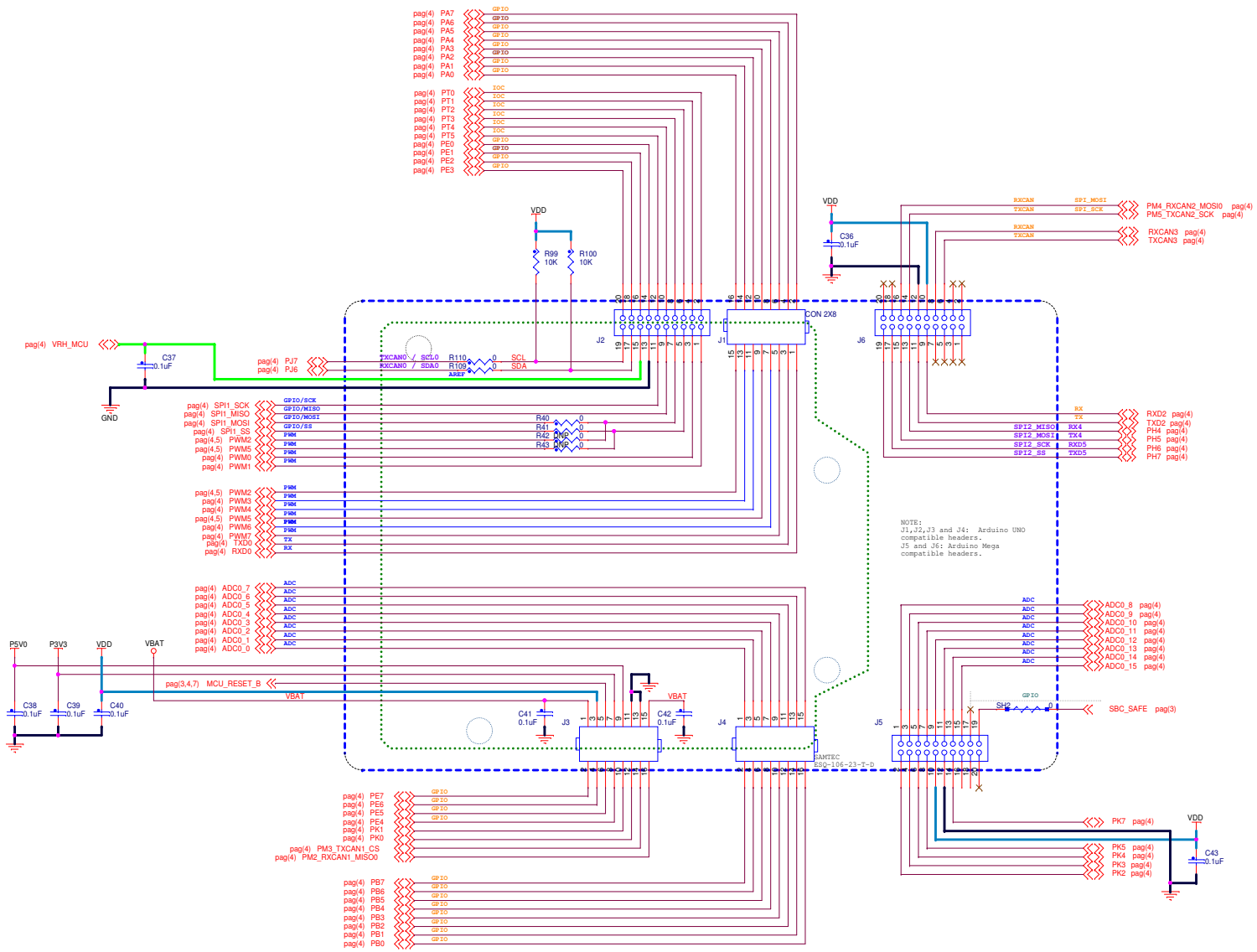
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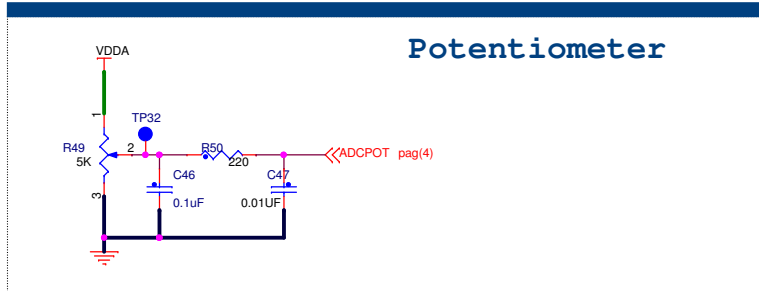
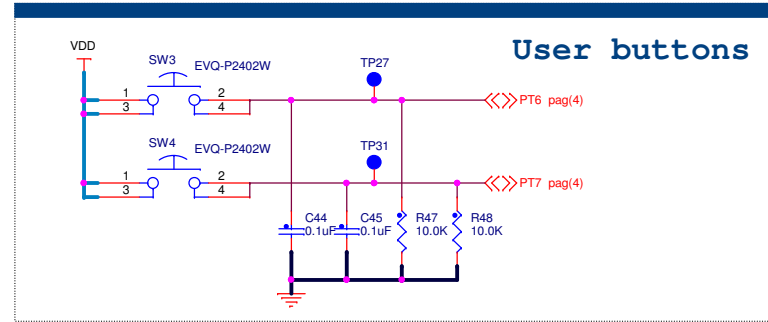
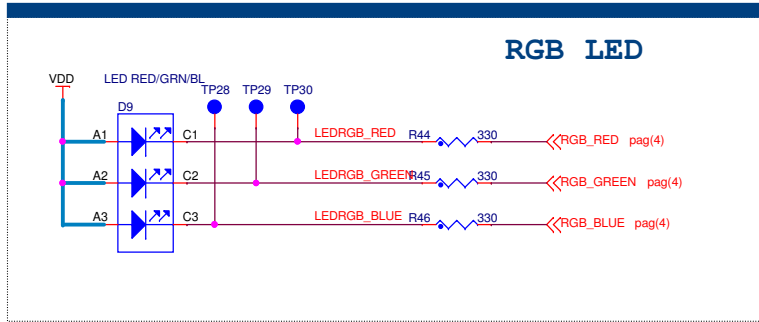
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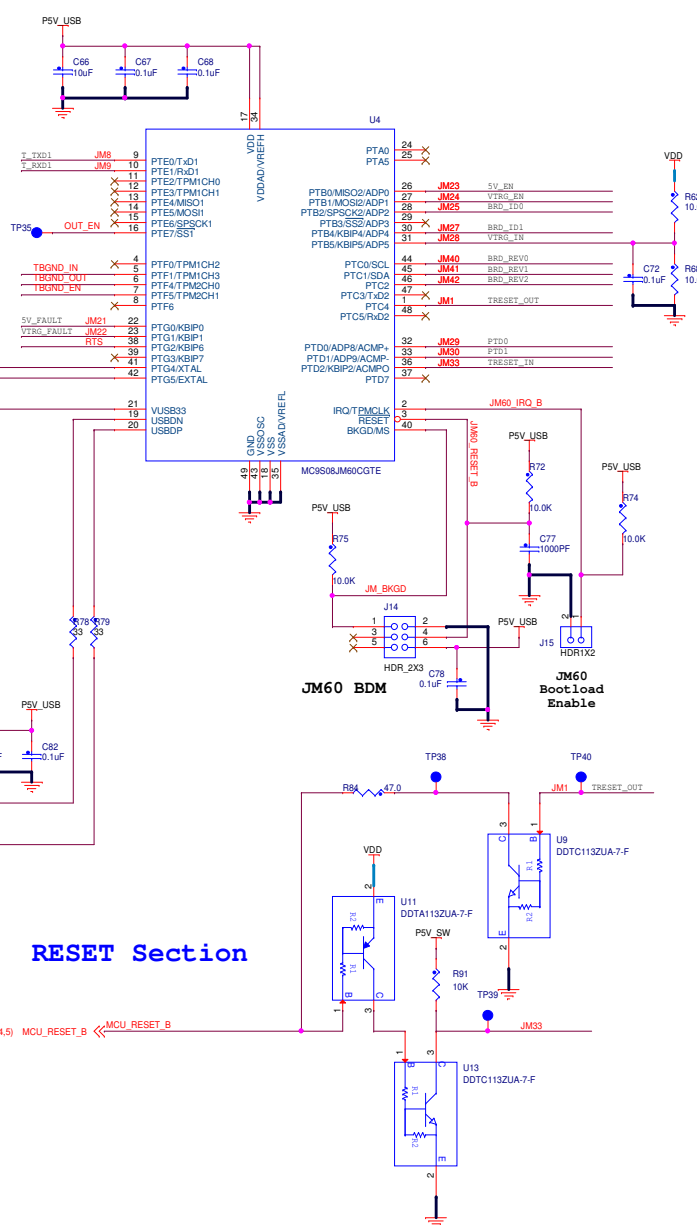
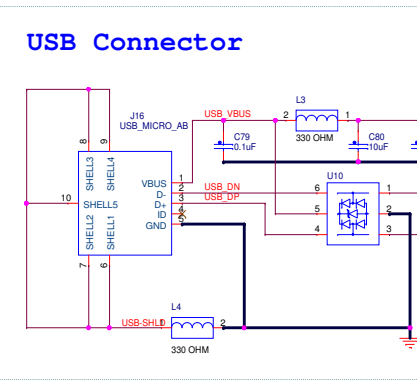
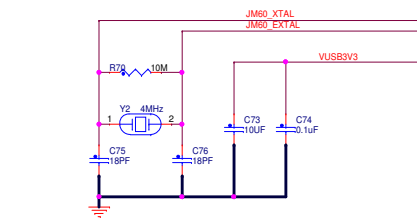
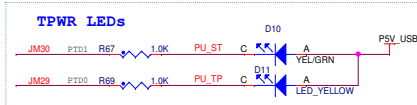
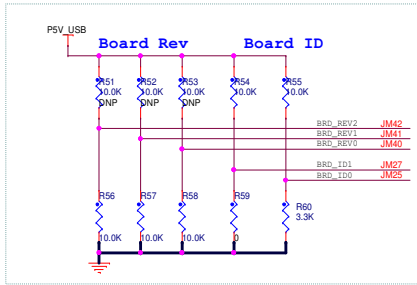


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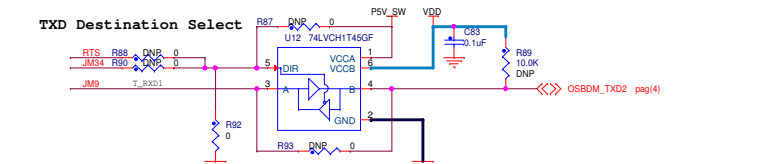
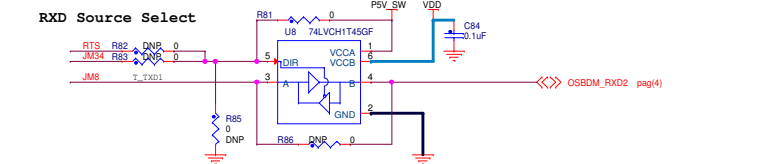
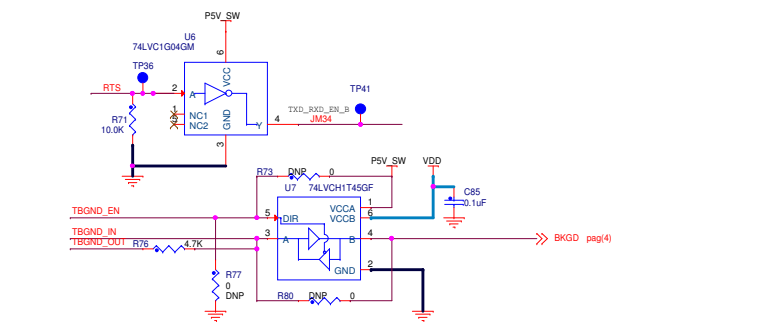
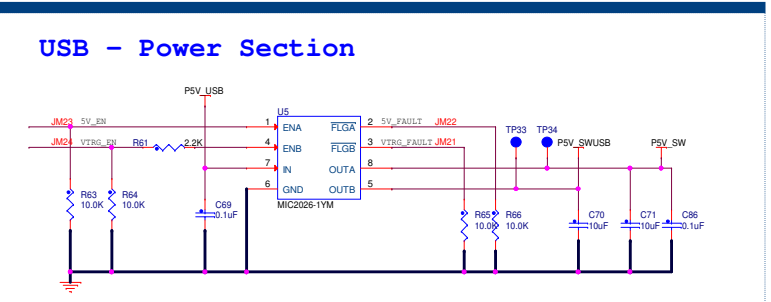
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On board OSBDM/Serial bridge



RESET Section

pag(3,4,5) MCU_RESET_B << MCU_RESET_B



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