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Introduction

The MC9S12D family of MCUs includes a Phase-Locked Loop (PLL) circuit as part of the Clock and Reset Generator (CRG) module. The purpose of the PLL is to generate an internal timebase from the crystal oscillator signal. The PLL allows the internal timebase, usually called the bus clock, to be generated at a higher frequency than the oscillator signal. The use of a relatively low frequency crystal oscillator facilitates lower power consumption in low power modes.

The PLL requires an external passive low pass filter connected to the XFC pin in order to operate. The value of the filter network determines the speed of correction and the stability of the PLL. The external filter network consists of two capacitors and a resistor, as shown in [Figure 1. PLL Filter Components](#).

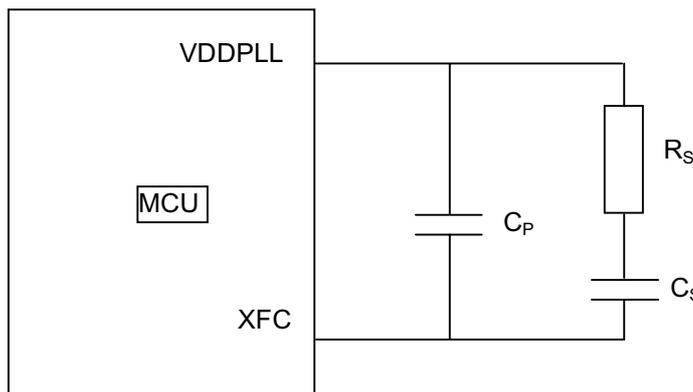


Figure 1. PLL Filter Components

Precise values for R_S , C_S and C_P may readily be calculated using the equations and values provided in the Electrical Characteristics section of the respective microcontroller Device User Guide. However, due to the limited range of standard values for capacitors, one or two iterations may be required. This process is automated by the "HCS12 PLL Filter Calculator" utility that is described in this manual.

S12 PLL Filter Calculator

The S12 PLL Filter Calculator is run by executing the file "HCS12 PLL Filter.exe" on a Personal Computer (PC) running a 32-bit Windows™ operating system. The dialogue box shown in [Figure 2. PLL Filter Calculator](#) is presented.

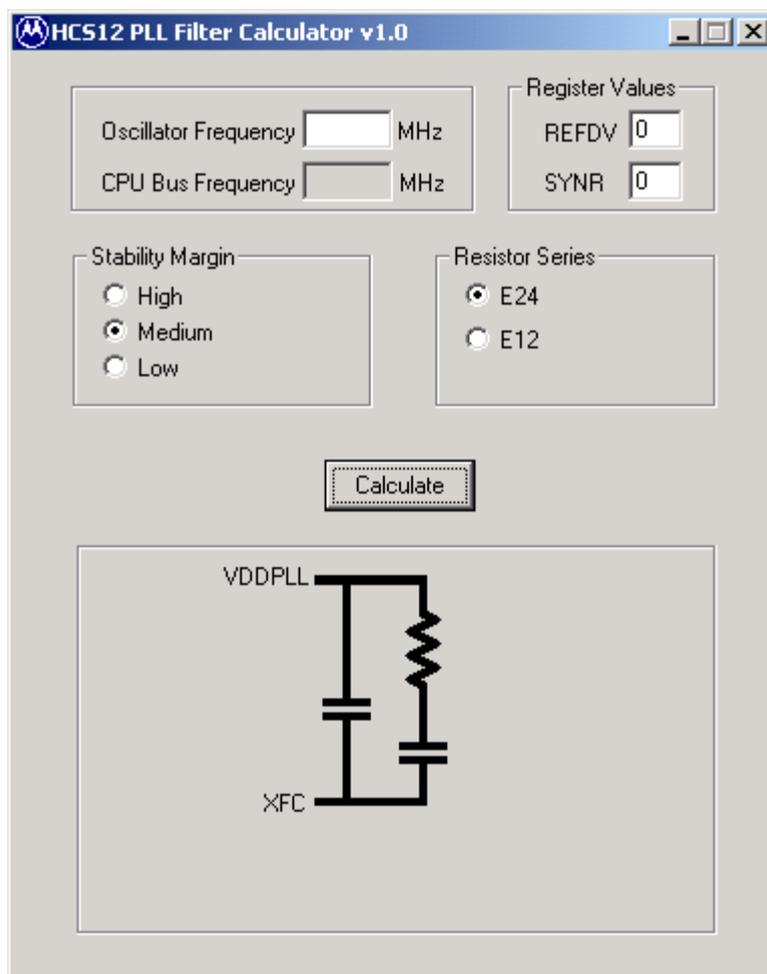


Figure 2. PLL Filter Calculator

The following data is required to be entered in order to calculate the component values:

- Oscillator Frequency** The oscillator frequency in units of MHz is entered into the field next to the "Oscillator Frequency" label. Decimal values are permitted, for example 4.9152 MHz.
- REFDV** The selected value for the REFDV register is entered into the field next to the "REFDV" label. Permitted values are 0... 15. A warning will be given if the value entered exceeds 15.
- SYNR** The selected value for the SYNR register is entered into the field next to the "SYNR" label. Permitted values are 0...63. A warning will be given if the value entered exceeds 63.
- CPU Bus Frequency** The CPU Bus frequency is automatically calculated as soon as valid values are entered for Oscillator Frequency, REFDV and SYNR. The CPU Bus frequency is calculated from the equation:

$$f_{BUS} = \frac{(SYNR + 1)}{(REFDV + 1)} f_{osc}$$

The result is displayed in the field labelled "CPU Bus Frequency".

- Stability Margin** The desired stability margin is selected by selecting one of the "High", "Medium" or "Low" radio buttons.

Gardeners stability criteria is given by a loop bandwidth of:

$$f_c = \frac{f_{osc}}{4(REFDV + 1)}$$

for a damping factor of 0.9.

The "High" radio button selects a target loop bandwidth that is a factor of 125 smaller than Gardeners criteria.

The "Medium" radio button selects a target loop bandwidth that is a factor of 50 smaller than Gardeners criteria. This represents a typical value.

The "Low" radio button selects a target loop bandwidth that is a factor of 20 smaller than Gardeners criteria.

In all cases, the actual loop bandwidth based on the selected resistor and capacitor values may deviate slightly from the target value.

Resistor Series

The desired range of values for selecting the series resistor, R_S , is entered by selecting one of the radio buttons, E12 or E24.

The E12 range includes the following values multiplied by powers of 10:

1.0, 1.2, 1.5, 1.8, 2.2, 2.7, 3.3, 3.9, 4.7, 5.6, 6.8 and 8.2.

The E24 range includes all the values in the E12 range, plus the following values multiplied by powers of 10:

1.1, 1.3, 1.6, 2.0, 2.4, 3.0, 3.6, 4.3, 5.1, 6.2, 7.5 and 9.1.

The E24 range is recommended. Selecting the E12 range may result in a loop damping factor which deviates from the target value of 0.9 or a loop bandwidth which deviates from the selected factor of Gardeners criteria. In most cases, these differences will not have a significant effect on performance.

Calculate

When the "Calculate" button is clicked, the following values are calculated and displayed if no errors are found:

CPU Bus Frequency

The CPU bus frequency is checked and an error message is displayed if the value is greater than 25MHz.

Series Resistance

The value for R_S is calculated and displayed next to the symbol for the series resistor. The selected value will be chosen from the E12 or E24 range of values, depending on the selected "Resistor Series" radio button. The displayed value has units of Ohms.

Series Capacitance

The value for C_S is calculated and displayed next to the symbol for the series capacitor. The selected value will be chosen from a range comprising of the values 1.0, 2.2, 3.3 and 4.7 multiplied by a power of 10. The display value has units of nF.

Parallel Capacitance The value for C_P is calculated and displayed next to the symbol for the parallel capacitor. The selected value is always equal to $C_S/10$. The display value has units of nF.

Lock Time The approximate lock time is estimated and displayed in the field labelled "Approximate Lock Time" in units of ms. Note that this value is an estimated typical value and not a worst case value.

NOTE: *If lock time is important, the customer should characterise this value in their application, as measured values may deviate significantly from the value estimated by this tool.*

PLL Calculator Tool Characteristics

The HCS12 PLL Calculator tool uses the following constants in its equations:

Table 1. PLL Calculator Constants

VCO loop gain fitting parameter	K_1	-100	MHz/V
VCO loop frequency fitting parameter	F_1	60	MHz
Acquisition mode charge pump current	$ i_{ch_a} $	38.5	μA
Tracking mode charge pump current	$ i_{ch_t} $	3.5	μA

The HCS12 PLL Calculator tool is suitable for all HCS12 MCUs that have PLL characteristics that match those in [Table 1. PLL Calculator Constants](#).

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