# This for Copper Wire Qualification of MSDISWA

Freescale Part Numbers: MC33972ATEK/R2 MC33972ATEW/R2

FREESCALE INTERNAL TRACKING NUMBER: 201350130A\_0\_0

TSMC Fab 2 / Mask N39B

**32 SOIC Assembly and Test at Freescale Tianjin, China** 

TEMPE, AZ January 15, 2014



FORMPPAP021DOC Freescale Rev G

## **Table of Contents**

Reference PDF Bookmarks, which link directly to the key elements and contents and are essentially a table of contents for an electronic PDF file.

#### PURPOSE AND BACKGROUND STATEMENT

Customer Part Number: Standard Part	Date: 10 December 2013
Part Name: MSDISWA	Freescale Part Number: MC33972ATEK/R2,
	MC33972ATEW/R2
Customer Ref : NA	Title: MSDISWA Cu Wire Qualification

#### **PURPOSE:**

This PPAP package is intended to present data and information required for the qualification of MSDISWA Cu wire in the TSMC facility in the SOIC package from FSL-TJN-FM.

#### **BACKGROUND:**

Reliability Qualification testing was performed to qualify the addition of Copper Wire as a wirebond material and Sumitomo EME-G630AY Molding Compound as mold material for SMOS5 SOIC32 300ML 4.6EP and Non-EP package devices. These products were previously assembled with Gold (Au) wire and Hitachi CEL9220HF13 Molding compound at Freescale TJN assembly site, Tianjin, China. These products are now qualified for assembly with Copper (Cu) wire and EME-G630AY Molding Compound at Freescale TJN assembly site, Tianjin, China.

The PPAP manufacturing documentation (e.g., control plans, FMEA's, etc.) included in this PPAP File were current when retrieved and reviewed by Freescale during component-level qualification. This documentation (when reviewed by the Customer) may not reflect the latest revision in our document repository. These documents are intended to reflect semiconductor manufacturing processing and capability. In addition, this PPAP submission may contain documents and data generated both before and after Freescale Semiconductor, Inc was organized as a separate business entity from its predecessor company, Motorola. As such, documentation contained herein may contain references to both Freescale and Motorola, depending on the time the document was originally created.

# **Design Records**

Document Number: MC33972

Rev. 19.0, 3/2012

## **√**RoHS

## Multiple Switch Detection Interface with Suppressed Wake-up

The 33972 Multiple Switch Detection Interface with suppressed wake-up is designed to detect the closing and opening of up to 22 switch contacts. The switch status, either open or closed, is transferred to the microprocessor unit (MCU) through a serial peripheral interface (SPI). The device also features a 22-to-1 analog multiplexer for reading inputs as analog. The analog input signal is buffered and provided on the AMUX output pin for the MCU to read.

The 33972 device has two modes of operation, Normal and Sleep. Normal mode allows programming of the device and supplies switch contacts with pull-up or pull-down current as it monitors switch change of state. The Sleep mode provides low quiescent current, which makes the 33972 ideal for automotive and industrial products requiring low sleep-state currents.

#### **Features**

- Designed to operate 5.5 V ≤ V<sub>PWR</sub> ≤ 26 V
- Switch input voltage range -14 V to V<sub>PWR</sub>, 40 V Max
- Interfaces directly to MPU using 3.3 V/5.0 V SPI protocol
- · Selectable wake-up on change of state
- Selectable wetting current (16 or 2.0 mA)
- 8 programmable inputs (switches to battery or ground)
- · 14 switch-to-ground inputs
- Typical standby current V<sub>PWR</sub> = 100 μA and V<sub>DD</sub> = 20 μA
- Active interrupt (INT) on change-of-switch state

#### 33972/A/T

## MULTIPLE SWITCH DETECTION INTERFACE





EW SUFFIX (Pb-FREE) 98ARH99137A 32-PIN SOICW

98ASA10556D 32-PIN SOICW EP

ORDE	RING INFORMAT	ION
Device	Temperature Range (T <sub>A</sub> )	Package
MC33972TEW/R2		32 SOICW
MC33972ATEW/R2	-40 °C to 125 °C	32 3010W
MC33972ATEK/R2		32 SOICW EP

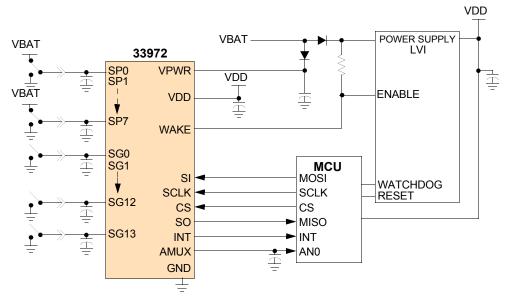


Figure 1. 33972 Simplified Application Diagram

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## **DEVICE VARIATIONS**

**Table 1. Device Variations** 

Device	Switch Input Voltage Range	Reference Location
33972	-14 to 38 V <sub>DC</sub>	<u>5, 6</u>
33972A	-14 to 40 V <sub>DC</sub>	<u>5, 6</u>

#### INTERNAL BLOCK DIAGRAM

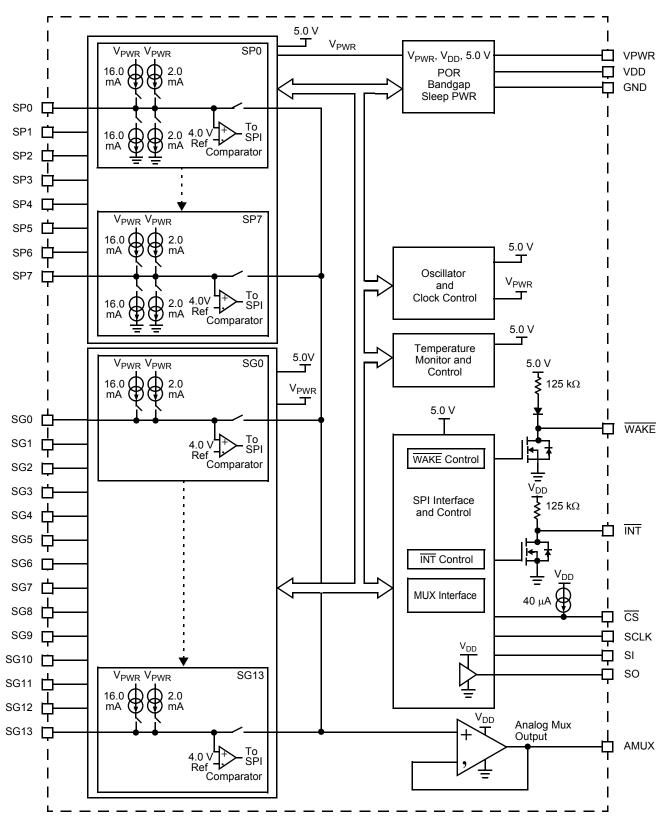


Figure 2. 33972 Simplified Internal Block Diagram

#### **PIN CONNECTIONS**

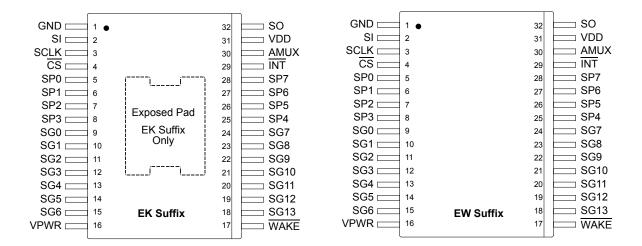


Figure 3. 33972 Pin Connections

Table 2. 33972 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 10.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	GND	Ground	Ground	Ground for logic, analog, and switch to battery inputs.
2	SI	Input	SPI Slave In	SPI control data input pin from the MCU to the 33972.
3	SCLK	Input	Serial Clock	SPI control clock input pin.
4	<u>cs</u>	Input	Chip Select	SPI control chip select input pin from the MCU to the 33972. Logic [0] allows data to be transferred in.
5–8 25–28	SP0-3 SP4-7	Input	Programmable Switches 0–7	Programmable switch-to-battery or switch-to-ground input pins.
9–15, 18–24	SG0-6, SG13-7	Input	Switch-to-Ground Inputs 0–13	Switch-to-ground input pins.
16	VPWR	Input	Battery Input	Battery supply input pin. Pin requires external reverse battery protection.
17	WAKE	Input/Output	Wake-up	Open drain wake-up output. Designed to control a power supply enable pin.
29	ĪNT	Input/Output	Interrupt	Open-drain output to MCU. Used to indicate an input switch change of state.
30	AMUX	Output	Analog Multiplex Output	Analog multiplex output.
31	VDD	Input	Voltage Drain Supply	3.3/5.0 V supply. Sets SPI communication level for the SO driver.
32	SO	Output	SPI Slave Out	Provides digital data from the 33972 to the MCU.
	EP	Ground	Exposed Pad	It is recommended that the exposed pad is terminated to GND (pin 1) and system ground, however, the device will perform as specified with the exposed pad unterminated (floating).

#### **ELECTRICAL CHARACTERISTICS**

#### **MAXIMUM RATINGS**

#### Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS	1		•
VDD Supply Voltage			V <sub>DC</sub>
$\overline{\text{CS}}$ , SI, SO, SCLK, $\overline{\text{INT}}$ , AMUX <sup>(1)</sup>	_	-0.3 to 7.0	
WAKE <sup>(1)</sup>	_	-0.3 to 40	V <sub>DC</sub>
VPWR Supply Voltage <sup>(1)</sup>	_	-0.3 to 50	V <sub>DC</sub>
VPWR Supply Voltage at -40 °C <sup>(1)</sup>	_	-0.3 to 45	V <sub>DC</sub>
Switch Input Voltage Range	_	-14 to 40	V <sub>DC</sub>
Frequency of SPI Operation (V <sub>DD</sub> = 5.0 V)	_	6.0	MHz
ESD Voltage <sup>(3)</sup>			V
Human Body Model <sup>(2)</sup>	V <sub>ESD</sub>	±2000	
Applies to all non-input pins		±2000	
Machine Model		±200	
Charge Device Model			
Corner Pins		750	
Interior Pins		500	
THERMAL RATINGS			•
Operating Temperature			°C
Ambient	T <sub>A</sub>	-40 to 125	
Junction	T <sub>J</sub>	-40 to 150	
Storage Temperature	T <sub>STG</sub>	-55 to 150	°C
Power Dissipation (T <sub>A</sub> = 25 °C) <sup>(4)</sup>	P <sub>D</sub>	1.7	W
Thermal Resistance			°C/W
Non-Exposed Pad			
Junction to Ambient	$R_{ hetaJA}$	74	
Junction to Lead	$R_{\theta JL}$	25	
Exposed Pad	UOL		
Junction to Ambient	$R_{ hetaJA}$	71	
Junction to Exposed Pad	$R_{\theta JC}$	1.2	
Peak Package Reflow Temperature During Reflow <sup>(5), (6)</sup>	T <sub>PPRT</sub>	Note 6	°C

#### Notes

- 1. Exceeding these limits may cause malfunction or permanent damage to the device.
- 2. ESD data available upon request.
- 3. ESD1 testing is performed in accordance with the Human Body Model ( $C_{ZAP}$  = 100 pF,  $R_{ZAP}$  = 1500  $\Omega$ ), and ESD2 testing is performed in accordance with the Machine Model ( $C_{ZAP}$  = 200 pF,  $R_{ZAP}$  = 0  $\Omega$ ).
- 4. Maximum power dissipation at  $T_J = 150^{\circ}$ C junction temperature with no heat sink used.
- 5. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow
  Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes
  and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

#### STATIC ELECTRICAL CHARACTERISTICS

**Table 4. Static Electrical Characteristics** 

Characteristics noted under conditions 3.1 V  $\leq$  V<sub>DD</sub>  $\leq$  5.25 V, 8.0 V  $\leq$  V<sub>PWR</sub>  $\leq$  16 V, -40 °C  $\leq$  T<sub>C</sub>  $\leq$  125 °C, unless otherwise noted.(7) Where applicable, typical values reflect the parameter's approximate average value with V<sub>PWR</sub> = 13 V, T<sub>A</sub> = 25 °C.

Characteristic	Symbol	Min	Тур	Max	Unit
POWER INPUT					
Supply Voltage					V
Supply Voltage Range Quasi-functional <sup>(8)</sup>	$V_{PWR(QF)}$	5.5	_	8.0	
Fully Operational	V <sub>PWR</sub> (FO)	8.0	-	26	
Supply Voltage Range Quasi-functional <sup>(8)</sup>	$V_{PWR(QF)}$	26	_	38/40	
Supply Current	I <sub>PWR(ON)</sub>				mA
All Switches Open, Normal Mode, Tri-state Disabled		-	2.0	4.0	
Sleep State Supply Current	I <sub>PWR(SS)</sub>				μА
Scan Timer = 64 ms, Switches Open		40	70	100	
Logic Supply Voltage	$V_{DD}$	3.1	_	5.25	V
Logic Supply Current	I <sub>DD</sub>				mA
All Switches Open, Normal mode		_	0.25	0.5	
Sleep State Logic Supply Current	I <sub>DD(SS)</sub>				μΑ
Scan Timer = 64 ms, Switches Open		_	10	20	
SWITCH INPUT					
Pulse Wetting Current Switch-to-Battery (Current Sink)	I <sub>PULSE</sub>	12	15	18	mA
Pulse Wetting Current Switch-to-Ground (Current Source)	I <sub>PULSE</sub>	12	16	18	mA
Sustain Current Switch-to-Battery Input (Current Sink)	I <sub>SUSTAIN</sub>	1.8	2.0	2.2	mA
Sustain Current Switch-to-Ground Input (Current Source)	I <sub>SUSTAIN</sub>	1.8	2.0	2.2	mA
Sustain Current Matching Between Channels on Switch-to-Ground I/Os	I <sub>MATCH</sub>				%
I <sub>SUS(MAX)</sub> - I <sub>SUS(MIN)</sub> X 100		_	2.0	4.0	
I <sub>SUS(MIN)</sub>					
Input Offset Current When Selected as Analog	I <sub>OFFSET</sub>	-2.0	1.4	2.0	μА
Input Offset Voltage When Selected as Analog	V <sub>OFFSET</sub>				mV
V <sub>(SP&amp;SGINPUTS)</sub> to AMUX Output		-10	2.5	10	
Analog Operational Amplifier Output Voltage	V <sub>OL</sub>				mV
Sink 250 μA		_	10	30	
Analog Operational Amplifier Output Voltage	V <sub>OH</sub>				V
Source 250 μA		V <sub>DD</sub> -0.1	_	_	
Switch Detection Threshold	V <sub>TH</sub>	3.70	4.0	4.3	V
Switch Input Voltage Range	V <sub>IN</sub>				V
33972		-14	_	38	
33972A		-14	-	40	
Temperature Monitor <sup>(9), (10)</sup>	T <sub>LIM</sub>	155	_	185	°C
Temperature Monitor Hysteresis <sup>(10)</sup>	T <sub>LIM(HYS)</sub>	5.0	10	15	°C
	` '	1		1	

#### Notes

- 7.  $T_C$  is the  $T_{CASE}$  of the package
- 8. Device operational. Table parameters may be out of specification.
- 9. Thermal shutdown of 16 mA pull-up and pulldown current sources only. 2.0 mA current source/sink and all other functions remain active.
- 10. This parameter is guaranteed by design but is not production tested.

#### **Table 4. Static Electrical Characteristics (continued)**

Characteristics noted under conditions 3.1 V  $\leq$  V<sub>DD</sub>  $\leq$  5.25 V, 8.0 V  $\leq$  V<sub>PWR</sub>  $\leq$  16 V, -40 °C  $\leq$  T<sub>C</sub>  $\leq$  125 °C, unless otherwise noted.(7) Where applicable, typical values reflect the parameter's approximate average value with V<sub>PWR</sub> = 13 V, T<sub>A</sub> = 25 °C.

Characteristic	Symbol	Min	Тур	Max	Unit
DIGITAL INTERFACE				II.	
Input Logic Voltage Thresholds <sup>(11)</sup>	V <sub>INLOGIC</sub>	0.8	-	2.2	V
SCLK, SI, Tri-state SO Input Current 0 V to V <sub>DD</sub>	I <sub>SCLK,</sub> I <sub>SI,</sub> I <sub>SO(TRI)</sub>	-10	_	10	μА
CS Input Current CS = V <sub>DD</sub>	I <del>CS</del>	-10	_	10	μΑ
CS Pull-up Current CS = 0 V	I <del>CS</del>	30	_	100	μА
SO High-state Output Voltage I <sub>SO(HIGH)</sub> = -200 μA	V <sub>SO(HIGH)</sub>	V <sub>DD</sub> -0.8	_	V <sub>DD</sub>	V
SO Low-state Output Voltage I <sub>SO(HIGH)</sub> = 1.6mA	V <sub>SO(LOW)</sub>	_	_	0.4	V
Input Capacitance on SCLK, SI, Tri-state SO <sup>(12)</sup>	C <sub>IN</sub>	-	-	20	pF
INT Internal Pull-up Current	-	15	40	100	μА
INT Voltage INT = Open Circuit	V <sub>INT</sub> (HIGH)	V <sub>DD</sub> -0.5	_	V <sub>DD</sub>	V
INT Voltage I <sub>INT</sub> = 1.0 mA	V <sub>INT</sub> (LOW)	-	0.2	0.4	V
WAKE Internal Pull-up Current	IWAKE(PU)	20	40	100	μА
WAKE Voltage WAKE = Open Circuit	VWAKE(HIGH)	4.0	4.3	5.3	V
WAKE Voltage IWAKE = 1.0 mA	VWAKE(LOW)	_	0.2	0.4	V
WAKE Voltage  Maximum Voltage Applied to WAKE Through External Pull-up	V <sub>WAKE</sub> (MAX)	_	-	40	V

#### Notes

<sup>11.</sup> Upper and lower logic threshold voltage levels apply to SI,  $\overline{\text{CS}}$ , and SCLK.

<sup>12.</sup> This parameter is guaranteed by design but is not production tested.

#### **DYNAMIC ELECTRICAL CHARACTERISTICS**

#### **Table 5. Dynamic Electrical Characteristics**

Characteristics noted under conditions 3.1 V  $\leq$  V<sub>DD</sub>  $\leq$  5.25 V, 8.0 V  $\leq$  V<sub>PWR</sub>  $\leq$  16 V, -40 °C  $\leq$  T<sub>C</sub>  $\leq$  125 °C, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V<sub>PWR</sub> = 13 V, T<sub>A</sub> = 25 °C.

Characteristic	Symbol	Min	Тур	Max	Unit
SWITCH INPUT	1			l .	I .
Pulse Wetting Current Time	t <sub>PULSE(ON)</sub>	15	16	20	ms
Interrupt Delay Time	t <sub>INT-DLY</sub>				μS
Normal Mode		_	5.0	16	
Sleep Mode Switch Scan Time	t <sub>SCAN</sub>	100	200	300	μS
Calibrated Scan Timer Accuracy	t <sub>SCAN</sub> TIMER				%
Sleep Mode		_	_	10	
Calibrated Interrupt Timer Accuracy	t <sub>INT TIMER</sub>				%
Sleep Mode		_	_	10	
DIGITAL INTERFACE TIMING <sup>(13)</sup>	·				
Required Low-state Duration on V <sub>PWR</sub> for Reset <sup>(14)</sup>	t <sub>RESET</sub>				μS
$V_{PWR} \le 0.2 \text{ V}$		_	_	10	
Falling Edge of CS to Rising Edge of SCLK	t <sub>LEAD</sub>				ns
Required Set-up Time		100	_	_	
Falling Edge of SCLK to Rising Edge of CS	t <sub>LAG</sub>				ns
Required Set-up Time		50	-	_	
SI to Falling Edge of SCLK	t <sub>SI(SU)</sub>				ns
Required Set-up Time		16	-	_	
Falling Edge of SCLK to SI	t <sub>SI(HOLD)</sub>				ns
Required Hold Time		20	-	_	
SI, CS, SCLK Signal Rise Time <sup>(15)</sup>	t <sub>R(SI)</sub>	_	5.0	_	ns
SI, CS, SCLK Signal Fall Time <sup>(15)</sup>	t <sub>F(SI)</sub>	_	5.0	_	ns
Time from Falling Edge of $\overline{\text{CS}}$ to SO Low-impedance <sup>(16)</sup>	t <sub>SO(EN)</sub>	-	_	55	ns
Time from Rising Edge of $\overline{\text{CS}}$ to SO High-impedance <sup>(17)</sup>	t <sub>SO(DIS)</sub>	_	_	55	ns
Time from Rising Edge of SCLK to SO Data Valid <sup>(18)</sup>	t <sub>VALID</sub>	_	25	55	ns

#### Notes

- 13. These parameters are guaranteed by design. Production test equipment uses 4.16 MHz, 5.0 V SPI interface.
- 14. This parameter is guaranteed by design but not production tested.
- 15. Rise and Fall time of incoming SI, CS, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
- 16. Time required for valid output status data to be available on SO pin.
- 17. Time required for output states data to be terminated at SO pin.
- 18. Time required to obtain valid data out from SO following the rise of SCLK with 200 pF load.

#### **TIMING DIAGRAMS**

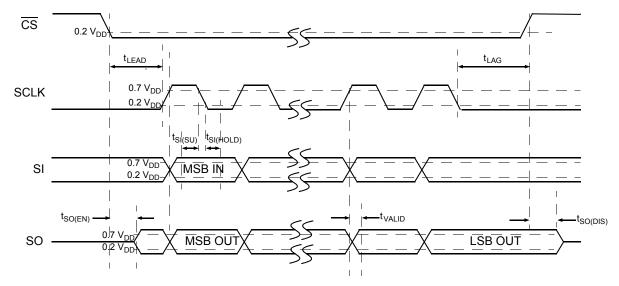


Figure 4. SPI Timing Characteristics

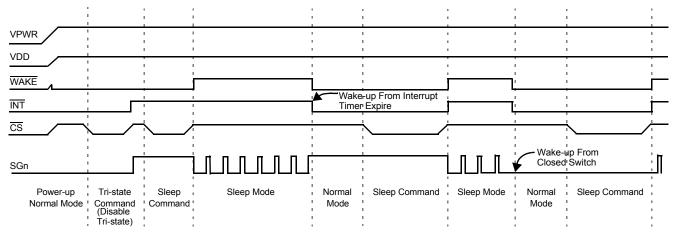


Figure 5. Sleep Mode to Normal Mode Operation

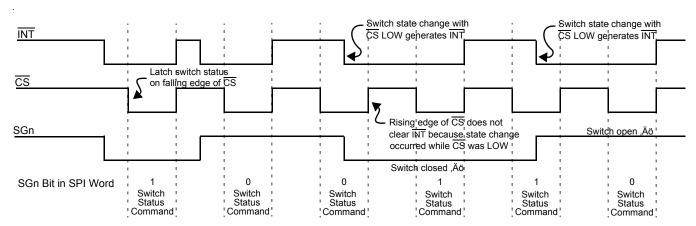


Figure 6. Normal Mode Interrupt Operation

#### **FUNCTIONAL DESCRIPTION**

#### INTRODUCTION

The 33972 device is an integrated circuit designed to provide systems with ultra-low quiescent sleep/wake-up modes, and a robust interface between switch contacts and a microprocessor. The 33972 replaces many of the discrete components required when interfacing to microprocessor-based systems, while providing switch ground offset protection, contact wetting current, and a system wake-up.

The 33972 features 8-programmable switch-to-ground or switch-to-battery inputs and 14 switch-to-ground inputs. All

switch inputs may be read as analog inputs through the analog multiplexer (AMUX). Other features include a programmable wake-up timer, programmable interrupt timer, programmable wake-up/interrupt bits, and programmable wetting current settings.

This device is designed primarily for automotive applications, but may be used in a variety of other applications such as computer, telecommunications, and industrial controls.

#### **FUNCTIONAL PIN DESCRIPTION**

#### CHIP SELECT (CS)

The system MCU selects the 33972 to receive communication using the chip select ( $\overline{CS}$ ) pin. With the  $\overline{CS}$  in a logic LOW state, command words may be sent to the 33972 via the serial input (SI) pin, and switch status information can be received by the MCU via the serial output (SO) pin. The falling edge of  $\overline{CS}$  enables the SO output, latches the state of the  $\overline{INT}$  pin, and the state of the external switch inputs.

Rising edge of the  $\overline{\text{CS}}$  initiates the following operation:

- 1. Disables the SO driver (high-impedance)
- INT pin is reset to logic [1], except when additional switch changes occur during CS LOW. (See <u>Figure 6</u> on page <u>9</u>.)
- 3. Activates the received command word, allowing the 33972 to act upon new data from switch inputs.

To avoid any spurious data, it is essential the HIGH-to-LOW and LOW-to-HIGH transitions of the  $\overline{CS}$  signal occur only when SCLK is in a logic LOW state. A clean  $\overline{CS}$  is needed to ensure no incomplete SPI words are sent to the device. Internal to the 33972 device is an active pull-up to  $V_{DD}$  on  $\overline{CS}$ .

In Sleep mode, the negative edge of  $\overline{\text{CS}}$  (V<sub>DD</sub> applied) will wake up the 33972 device. Data received from the device during  $\overline{\text{CS}}$  wake-up may not be accurate.

#### SYSTEM CLOCK (SCLK)

The system clock (SCLK) pin clocks the internal shift register of the 33972. The SI data is latched into the input shift register on the falling edge of SCLK signal. The SO pin shifts the switch status bits out on the rising edge of SCLK. The SO data is available for the MCU to read on the falling edge of SCLK. False clocking of the shift register must be avoided to ensure validity of data. It is essential the SCLK pin be in a logic LOW state whenever  $\overline{\text{CS}}$  makes any transition. For this reason, it is recommended, that the SCLK pin is commanded to a logic LOW state as long as the device is not accessed and  $\overline{\text{CS}}$  is in a logic HIGH state. When the  $\overline{\text{CS}}$  is in

a logic HIGH state, any signal on the SCLK and SI pins will be ignored and the SO pin is tri-state.

#### SPI SLAVE IN (SI)

The SI pin is used for serial instruction data input. SI information is latched into the input register on the falling edge of SCLK. A logic HIGH state present on SI will program a *one* in the command word on the rising edge of the  $\overline{\text{CS}}$  signal. To program a complete word, 24 bits of information must be entered into the device.

#### **SPI SLAVE OUT (SO)**

The SO pin is the output from the shift register. The SO pin remains tri-stated until the  $\overline{\text{CS}}$  pin transitions to a logic LOW state. All open switches are reported as zero, all closed switches are reported as one. The negative transition of CS enables the SO driver.

The first positive transition of SCLK will make the status data bit 24 available on the SO pin. Each successive positive clock will make the next status data bit available for the MCU to read on the falling edge of SCLK. The SI/SO shifting of the data follows a first-in, first-out protocol, with both input and output words transferring the most significant bit (MSB) first.

#### INTERRUPT (INT)

The  $\overline{\text{INT}}$  pin is an interrupt output from the 33972 device. The  $\overline{\text{INT}}$  pin is an open-drain output with an internal pull-up to  $\underline{V_{DD}}.$  In Normal mode, a switch state change will trigger the INT pin (when enabled). The  $\overline{\text{INT}}$  pin and  $\overline{\text{INT}}$  bit in the SPI register are latched on the falling edge of  $\overline{\text{CS}}.$  This permits the MCU to determine the origin of the interrupt. When two 33972 devices are used, only the device initiating the interrupt will have the INT bit set. The  $\overline{\text{INT}}$  pin is cleared on the rising edge of  $\overline{\text{CS}}.$  The  $\overline{\text{INT}}$  pin will not clear with rising edge of  $\overline{\text{CS}}$  if a switch contact change has occurred while  $\overline{\text{CS}}$  was LOW.

In a multiple 33972 device system with  $\overline{\text{WAKE}}$  HIGH and  $V_{DD}$  in (Sleep Mode), the falling edge of  $\overline{\text{INT}}$  will place all 33972s in Normal mode.

#### WAKE-UP (WAKE)

The WAKE pin is an open-drain output and a wake-up input. The pin is designed to control a power supply Enable pin. In the Normal mode, the WAKE pin is LOW. In the Sleep mode, the WAKE pin is HIGH. The WAKE pin has a pull-up to the internal +5.0 V supply.

In Sleep mode with the  $\overline{\text{WAKE}}$  pin HIGH, the falling edge of  $\overline{\text{WAKE}}$  will place the 33972 in Normal mode. In Sleep mode with  $V_{DD}$  applied, the  $\overline{\text{INT}}$  pin must be HIGH for negative edge of  $\overline{\text{WAKE}}$  to wake up the device. If  $V_{DD}$  is not applied to the device in Sleep mode,  $\overline{\text{INT}}$  does not affect  $\overline{\text{WAKE}}$  operation.

#### **BATTERY INPUT (VPWR)**

The VPWR pin is battery input and Power-ON Reset to the 33972 IC. The VPWR pin requires external reverse battery and transient protection. Maximum input voltage on VPWR is 50 V. All wetting, sustain, and internal logic current is provided from the VPWR pin.

#### **VOLTAGE DRAIN SUPPLY (VDD)**

The VDD input pin is used to determine logic levels on the microprocessor interface (SPI) pins. Current from VDD is used to drive SO output and the pull-up current for  $\overline{CS}$  and  $\overline{INT}$  pins. VDD must be applied for wake-up from negative edge of  $\overline{CS}$  or  $\overline{INT}$ .

#### **GROUND (GND)**

The GND pin provides ground for the IC as well as ground for inputs programmed as switch-to-battery inputs.

#### PROGRAMMABLE SWITCHES (SP0:SP7)

The 33972 device has 8 switch inputs capable of being programmed to read switch-to-ground or switch-to-battery contacts. The input is compared with a 4.0 V reference. When programmed to be switch-to-battery, voltages greater than 4.0 V are considered closed. Voltages less than 4.0 V are considered open. The opposite holds true when inputs are programmed as switch-to-ground. Programming features are defined in Table 6 through Table 11 in the Functional Device Operation section of this datasheet beginning on page 13. Voltages greater than the VPWR supply voltage will source current through the SP inputs to the VPWR pin. Transient battery voltages greater than 38/40 V must be clamped by an external device. This is not a normal operating condition and can damage the IC.

#### SWITCH-TO-GROUND INPUTS (SG0:SG13)

The SGn pins are switch-to-ground inputs only. The input is compared with a 4.0 V reference. Voltages greater than 4.0 V are considered open. Voltages less than 4.0 V are considered closed. Programming features are defined in Table 6 through Table 11 in the Functional Device Operation section of this datasheet beginning on page 13. Voltages greater than the VPWR supply voltage will source current through the SG inputs to the VPWR pin. Transient battery voltages greater than 40 V must be clamped by an external device. This is not a normal operating condition and can damage the IC.

#### FUNCTIONAL INTERNAL BLOCK DESCRIPTION

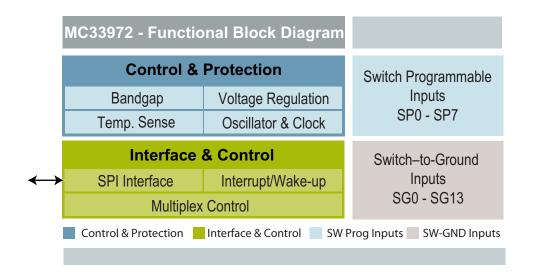


Figure 7. Functional Internal Block Description

#### CONTROL AND PROTECTION CIRCUITRY:

The 33972 is designed to operate from 5.5 V to 38/40 V on the VPWR terminal. Characteristics are provided for  $V_{PWR}$  from 8.0 to 26 V for the IC (parametric tests are done from 8.0 to 16.0v). Switch contact currents and the internal logic supply are generated from the VPWR terminal. The VDD supply terminal is used to set the SPI communication voltage levels, current source for the SO driver, and pull-up current on  $\overline{INT}$  and  $\overline{CS}$ .

The on-chip voltage regulator and bandgap supplies the required voltages to the internal monitor circuitry. The temperature monitor is active in the Normal mode.

#### **INTERFACE AND CONTROL:**

The 33972 Multiple Switch Detection Interface with Suppressed Wake-up is designed to detect the closing and opening of up to 22 switch contacts. The switch status, either open or closed, is transferred to the microprocessor unit (MCU) through a serial peripheral interface (SPI).

The device also features a 22-to-1 analog multiplexer for reading inputs as analog. The 33972 device has two modes of operation, Normal and Sleep.

#### **SWITCH PROGRAMMABLE INPUTS:**

Programmable switch detection inputs. These 8 inputs can selectively detect switch closures to Ground or Battery. The 33972 device has 8 switch inputs capable of being programmed to read switch-to-ground or switch-to-battery contacts. The input is compared with a 4.0 V reference. When programmed to be switch-to-battery, voltages greater than 4.0 V are considered closed. Voltages less than 4.0 V are considered open. The opposite holds true when inputs are programmed as switch-to-ground.

#### SWITCH-TO-GROUND INPUTS:

Switch detection interface inputs. These 14 inputs can detect switch closures to ground only. The input is compared with a 4.0 V reference. Voltages greater than 4.0 V are considered open. Voltages less than 4.0 V are considered closed. Note: Each of these inputs may be used to supply current to sensors external to a module.

#### **FUNCTIONAL DEVICE OPERATION**

#### **OPERATIONAL MODES**

#### MCU INTERFACE DESCRIPTION

The 33972 device directly interfaces to a 3.3 or 5.0 V microcontroller unit (MCU). SPI serial clock frequencies up to 6.0 MHz may be used for programming and reading switch input status (production tested at 4.16 MHz). Figure 8 illustrates the configuration between an MCU and one 33972.

Serial peripheral interface (SPI) data is sent to the 33972 device through the SI input pin. As data is being clocked into the SI pin, status information is being clocked out of the device by the SO output pin. The response to a SPI command will always return the switch status, interrupt flag, and thermal flag. Input switch states are latched into the SO register on the falling edge of the chip select  $(\overline{\text{CS}})$  pin. Twenty-four bits are required to complete a transfer of information between the 33972 and the MCU.

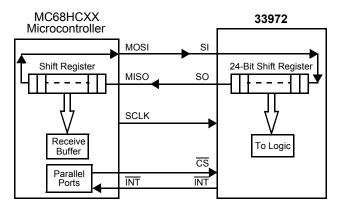


Figure 8. SPI Interface with Microprocessor

Two or more 33972 devices may be used in a module system. Multiple ICs may be SPI-configured in parallel or serial. Figures 9 and 10 show the configurations. When using the serial configuration, 48-clock cycles are required to transfer data in/out of the ICs.

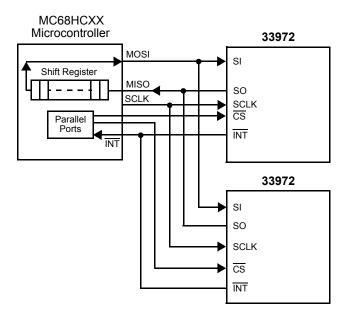


Figure 9. SPI Parallel Interface with Microprocessor

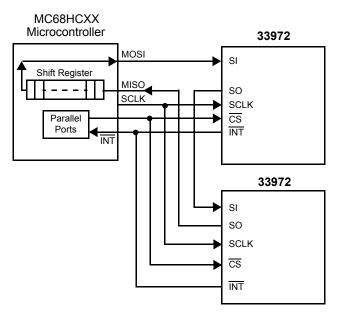


Figure 10. SPI Serial Interface with Microprocessor

#### **POWER SUPPLY**

The 33972 is designed to operate from 5.5 to 40 V on the VPWR pin. Characteristics are provided from 8.0 to 16 V for the device. Switch contact currents and the internal logic supply are generated from the VPWR pin. The VDD supply pin is used to set the SPI communication voltage levels, current source for the SO driver, and pull-up current on  $\overline{\text{INT}}$  and  $\overline{\text{CS}}$ .

The VDD supply may be removed from the device to reduce quiescent current. If  $V_{DD}$  is removed while the device is in Normal mode, the device will remain in Normal mode. If  $V_{DD}$  is removed in Sleep mode, the device will remain in Sleep mode until a wake-up input is received (WAKE HIGH to LOW, switch input or interrupt timer expires).

Removing  $V_{DD}$  from the device disables SPI communication and will not allow the device to wake up from  $\overline{INT}$  and  $\overline{CS}$  pins.

#### **POWER-ON RESET (POR)**

Applying  $V_{\text{PWR}}$  to the device will cause a Power-ON Reset and place the device in Normal mode.

Default settings from Power-ON Reset via  $V_{PWR}$  or the Reset Command are as follows:

- · Programmable switch set to switch to battery
- · All inputs set as wake-up
- Wetting current on (16 mA)
- Wetting current timer on (20 ms)
- · All inputs tri-state
- · Analog select 00000 (no input channel selected)

#### **NORMAL AND SLEEP MODES**

The 33972 has two operating modes, Normal mode and Sleep mode. A discussion on Normal mode begins below. A discussion on Sleep mode begins on page 19.

#### **Normal Mode**

Normal mode may be entered by the following events:

- Application of V<sub>PWR</sub> to the IC
- · Change-of-switch state (when enabled)

- Falling edge of WAKE
- Falling edge of INT (with V<sub>DD</sub> = 5.0 V and WAKE at Logic [1])
- Falling edge of CS (with V<sub>DD</sub> = 5.0 V)
- · Interrupt timer expires

Only in Normal mode with  $V_{\rm DD}$  applied can the registers of the 33972 be programmed through the SPI.

The registers that may be programmed in Normal mode are listed below. Further explanation of each register is provided in subsequent paragraphs.

- •Programmable Switch Register (Settings Command)
- •<u>Wake-Up/Interrupt Register</u> (*Wake-up/Interrupt Command*)
- Wetting Current Register (Metallic Command)
- •Wetting Current Timer Register (Wetting Current Timer Enable Command)
- •<u>Tri-State Register</u> (*Tri-state Command*)
- Analog Select Register (Analog Command)
- •Calibration of Timers (Calibration Command)
- •Reset (Reset Command)

<u>Figure 6</u>, page 9, is a graphical description of the device operation in Normal mode. Switch states are latched into the input register on the falling edge of  $\overline{CS}$ . The  $\overline{INT}$  to the MCU is cleared on the rising edge of  $\overline{CS}$ . However,  $\overline{INT}$  will not clear on rising edge of  $\overline{CS}$  if a switch has closed during SPI communication ( $\overline{CS}$  LOW). This prevents switch states from being missed by the MCU.

#### PROGRAMMABLE SWITCH REGISTER

Inputs SP0 to SP7 may be programmable for switch-to-battery or switch-to-ground. These inputs types are defined using the *settings command* (Table 6). To set an SPn input for switch-to-battery, a logic [1] for the appropriate bit must be set. To set an SPn input for switch-to-ground, a logic [0] for the appropriate bit must be set. The MCU may change or update the programmable switch register via software at any time in Normal mode. Regardless of the setting, when the SPn input switch is closed a logic [1] will be placed in the serial output response register (Table 17, page 19).

**Table 6. Settings Command** 

		Sett	ings (	Comm	nand			Not used								Battery/Ground Select							
23	22	21	20	19	18	17	16	15	15 14 13 12 11 10 9 8								6	5	4	3	2	1	0
0	0	0	0	0	0	0	1	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Х	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0

#### WAKE-UP/INTERRUPT REGISTER

The wake-up/interrupt register defines the inputs that are allowed to wake the 33972 from Sleep Mode or set the INT pin LOW in Normal mode. Programming the wake-up/interrupt bit to logic [0] will disable the specific input from generating an interrupt and will disable the specific input from

waking the IC in Sleep mode (<u>Table 7</u>). Programming the wake-up/interrupt bit to logic [1] will enable the specific input to generate an interrupt with switch change of state and will enable the specific input as wake-up. The MCU may change or update the wake-up/interrupt register via software at any time in Normal mode.

Table 7. Wake-up/Interrupt Command

	Wak	e-up	/Inter	rupt (	Comm	nand								Co	omma	nd Bi	ts						
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	Χ	Х	Х	Х	Х	Х	Χ	Χ	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0
0	0	0	0	0	0	1	1	Х	Χ	sg13	sg12	sg11	sg10	sg9	sg8	sg7	sg6	sg5	sg4	sg3	sg2	sg1	sg0

#### WETTING CURRENT REGISTER

The 33972 has two levels of switch contact current, 16 and 2.0 mA (see Figure 11). The metallic command is used to set the switch contact current level (Table 8). Programming the metallic bit to logic [0] will set the switch wetting current to 2.0 mA. Programming the metallic bit to logic [1] will set the switch contact wetting current to 16 mA. The MCU may change or update the wetting current register via software at any time in Normal mode.

Wetting current is designed to provide higher levels of current during switch closure. The higher level of current is designed to keep switch contacts from building up oxides that form on the switch contact surface.

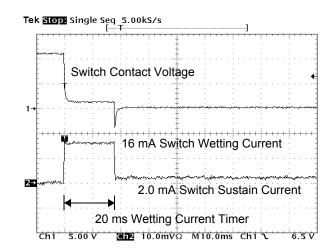


Figure 11. Contact Wetting and Sustain Current

**Table 8. Metallic Command** 

		Meta	allic C	omm	nand									Co	omma	nd Bit	s						
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	Х	Х	Х	Х	Х	Х	Х	Х	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0
0	0	0	0	0	1	0	1	Х	Х	sg13	sg12	sg11	sg10	sg9	sg8	sg7	sg6	sg5	sg4	sg3	sg2	sg1	sg0

#### WETTING CURRENT TIMER REGISTER

Each switch input has a designated 20 ms timer. The timer starts when the specific switch input crosses the comparator threshold (4.0 V). When the 20 ms timer expires, the contact current is reduced from 16 to 2.0 mA. The wetting current timer may be disabled for a specific input. When the timer is disabled, 16 mA of current will continue to flow through the

closed switch contact. With multiple wetting current timers disabled, power dissipation for the IC must be considered.

The MCU may change or update the wetting current timer register via software at any time in Normal mode. This allows the MCU to control the amount of time wetting current is applied to the switch contact. Programming the wetting current timer bit to logic [0] will disable the wetting current timer. Programming the wetting current timer bit to logic [1] will enable the wetting current timer (Table 9).

Table 9. Wetting Current Timer Enable Command

٧	Vettin	g Cur	rent 7	Гimer	Com	mand	s							Co	mma	nd Bit	s						
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	1	Χ	Х	Х	Х	Х	Х	Χ	Х	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0
0	0	0	0	1	0	0	0	Х	Х	sg13	sg12	sg11	sg10	sg9	sg8	sg7	sg6	sg5	sg4	sg3	sg2	sg1	sg0

#### TRI-STATE REGISTER

The tri-state command is use to set the SPn or SGn input node as high-impedance (<u>Table 10</u>). By setting the tri-state register bit to logic [1], the input will be high-impedance regardless of the metallic command setting. The comparator

on each input remains active. This command allows the use of each input as a comparator with a 4.0 V threshold. The MCU may change or update the tri-state register via software at any time in Normal mode.

Table 10. Tri-State Command

		Tri-S	tate C	omm	ands									Co	mma	nd Bit	s						
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	1	Χ	Χ	Х	Х	Х	Х	Х	Х	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0
0	0	0	0	1	0	1	0	Χ	Х	sg13	sg12	sg11	sg10	sg9	sg8	sg7	sg6	sg5	sg4	sg3	sg2	sg1	sg0

#### **ANALOG SELECT REGISTER**

The analog voltage on switch inputs may be read by the MCU using the analog command (Table 11). Internal to the IC is a 22-to-1 analog multiplexer. The voltage present on the selected input pin is buffered and made available on the AMUX output pin. The AMUX output pin is clamped to a maximum of VDD volts regardless of the higher voltages present on the input pin. After an input has been selected as the analog, the corresponding bit in the next SO data stream will be logic [0]. When selecting a channel to be read as analog, the user must also set the desired current (16 mA, 2.0 mA, or high-impedance). Setting bit 6 and bit 5 to 0,0

selects the input as high-impedance. Setting bit 6 and bit 5 to 0,1 selects 2.0 mA, and 1,0 selects 16 mA. Setting bit 6 and bit 5 to 1,1 in the analog select register is not allowed and will place the input as an analog input with high-impedance.

Analog currents set by the analog command are pull-up currents for all SGn and SPn inputs (<u>Table 11</u>). The analog command does not allow pull-down currents on the SPn inputs. Setting the current to 16 or 2.0 mA may be useful for reading sensor inputs. Further information is provided in the <u>Typical Applications</u> section of this datasheet beginning on page <u>21</u>. The MCU may change or update the analog select register via software at any time in Normal mode.

**Table 11. Analog Command** 

		Ana	log C	omm	and						N	ot use	ed				Curren	t Select	Ana	log C	hann	el Se	lect
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	0	Χ	Х	Х	Х	Χ	Х	Х	Х	Х	16 mA	2.0 mA	0	0	0	0	0

Table 12. Analog Channel

Bits 43210	Analog Channel Select
00000	No Input Selected
00001	SG0
00010	SG1
00011	SG2
00100	SG3
00101	SG4
00110	SG5
00111	SG6
01000	SG7
01001	SG8
01010	SG9
01011	SG10
01100	SG11
01101	SG12
01110	SG13
01111	SP0
10000	SP1
10001	SP2
10010	SP3
10011	SP4
10100	SP5
10101	SP6
10110	SP7

#### **CALIBRATION OF TIMERS**

In cases where an accurate time base is required, the user may calibrate the internal timers using the calibration command (Table 13). After the 33972 device receives the calibration command, the device expects 512  $\mu s$  logic [0] calibration pulse on the  $\overline{\text{CS}}$  pin. The pulse is used to calibrate the internal clock. No other SPI pins should transition during

this 512  $\mu$ s calibration pulse. Because the oscillator frequency changes with temperature, calibration is required for an accurate time base. Calibrating the timers has no affect on the quiescent current measurement. The calibration command simply makes the time base more accurate. The calibration command may be used to update the device on a periodic basis.

**Table 13. Calibration Command** 

		Calib	ration	Com	mand									C	omma	nd Bi	ts						
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	1	1	Х	Χ	Χ	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х

#### **RESET**

The reset command resets all registers to Power-ON Reset (POR) state. Refer to <u>Table 15</u>, page <u>18</u>, for POR

states or the paragraph entitled  $\underline{Power-ON\ Reset\ (POR)}$  on page  $\underline{14}$  of this datasheet.

Table 14. Reset Command

		Re	set Co	omma	nd									C	omma	nd Bi	ts						
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	1	1	Χ	Χ	Χ	Χ	Х	Χ	Х	Х	Χ	Х	Х	Χ	Х	Χ	Χ	Х

#### **SPI COMMAND SUMMARY**

<u>Table 15</u> below provides a comprehensive list of SPI commands recognized by the 33972 and the reset state of each register. <u>Table 16</u> and <u>Table 17</u> contain the serial

output (SO) data for input voltages greater or less than the threshold level. Open switches are always indicated with a logic [0], closed switches are indicated with logic [1].

**Table 15. SPI Command Summary** 

	MSB		C	omn	nand	Bits									Set	ting E	Bits							LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Switch Status Command	0	0	0	0	0	0	0	0	х	Х	Х	х	х	х	х	Х	Х	Х	Х	Х	Х	Х	Х	Х
Settings Command Bat=1, Gnd=0 (Default state = 1)	0	0	0	0	0	0	0	1	х	х	х	х	х	х	х	х	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Wake-Up/Interrupt Bit Wake-Up=1	0	0	0	0	0	0	1	0	Х	Х	Х	Х	Х	Х	Х	Х	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Non-Wake-Up=0 (Default state = 1)	0	0	0	0	0	0	1	1	х	х	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Metallic Command Metallic = 1	0	0	0	0	0	1	0	0	х	Х	Х	х	Х	Х	Х	Х	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Non-metallic = 0 (Default state = 1)	0	0	0	0	0	1	0	1	х	Х	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Analog Command	0	0	0	0	0	1	1	0	х	х	х	х	х	х	х	х	х	16mA 0	2.0mA 0	0	0	0	0	0
Wetting Current Timer Enable Command	0	0	0	0	0	1	1	1	х	Х	Х	х	х	Х	Х	Х	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Timer ON = 1 Timer OFF = 0 (Default state = 1)	0	0	0	0	1	0	0	0	х	х	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Tri-State Command	0	0	0	0	1	0	0	1	Х	Х	Х	Х	х	Х	Х	Х	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Input Tri-State=1 Input Active = 0 (Default state = 1)	0	0	0	0	1	0	1	0	х	Х	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Calibration Command (Default state – □uncalibrated)	0	0	0	0	1	0	1	1	x	х	х	x	х	x	х	х	х	х	х	х	х	х	х	х
Sleep Command (Refer to Sleep Mode on page 19.)	0	0	0	0	1	1	0	0	х	Х	x	х	х	х	х	x	x	х	int timer	int timer	int timer	scan timer	scan timer	scan timer
Reset Command	0	1	1	1	1	1	1	1	Х	Х	Х	Х	х	Х	х	Х	Х	Х	Х	Х	Х	Х	Х	Х
SO Response Will Always Send	them flg	int flg	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0

Table 16. Serial Output (SO) Bit Data

Type of Input	Input Programmed	Voltage on Input Pin	SO SPI Bit
SP	Switch to Ground	SPn < 4.0V	1
	Switch to Ground	SPn > 4.0V	0
	Switch to Battery	SPn < 4.0V	0
	Switch to Battery	SPn > 4.0V	1
SG	N/A	SGn < 4.0V	1
	N/A	SGn > 4.0V	0

Table 17. Serial Output (SO) Response Register

SO Response Will Always Send	them flg	int flg	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0	
---------------------------------	-------------	------------	-----	-----	-----	-----	-----	-----	-----	-----	------	------	------	------	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	--

#### **EXAMPLE OF NORMAL MODE OPERATION**

The operation of the device in Normal mode is defined by the states of the programmable internal control registers. A typical application may have the following settings:

- Programmable switch set to switch-to-ground
- · All inputs set as wake-up
- Wetting current on (16 mA)
- Wetting current timer on (20 ms)
- All inputs tri-state-disabled (comparator is active)
- Analog select 00000 (no input channel selected)

With the device programmed as above, an interrupt will be generated with each switch contact change of state (open-to-close or close-to-open) and 16 mA of contact wetting current will be source for 20 ms. The  $\overline{\text{INT}}$  pin will remain LOW until switch status is acknowledged by the microprocessor. It is critical to understand  $\overline{\text{INT}}$  will not be cleared on the rising edge of  $\overline{\text{CS}}$  if a switch closure occurs while  $\overline{\text{CS}}$  is LOW. The maximum duration a switch state change can exist without acknowledgement depends on the software response time to the interrupt. Figure 6, page 9, shows the interaction between changing input states and the  $\overline{\text{INT}}$  and  $\overline{\text{CS}}$  pins.

If desired the user may disable interrupts (wake up/interrupt command) from the 33972 device and read the switch states on a periodic basis. Switch activation and deactivation faster than the MCU read rate will not be acknowledged.

The 33972 device will exit the Normal mode and enter the Sleep mode only with a valid sleep command.

#### **SLEEP MODE**

Sleep mode is used to reduce system quiescent currents. Sleep mode may be entered only by sending the sleep command. All register settings programmed in Normal mode will be maintained in Sleep mode.

The 33972 will exit Sleep mode and enter Normal mode when any of the following events occur:

- Input switch change of state (when enabled)
- · Interrupt timer expire
- Falling edge of WAKE
- Falling edge of INT (with V<sub>DD</sub> = 5.0 V and WAKE at Logic [1])
- Falling edge of CS (with V<sub>DD</sub> = 5.0 V)
- Power-ON Reset (POR)

The  $V_{DD}$  supply may be removed from the device during Sleep mode. However removing  $V_{DD}$  from the device in Sleep mode will disable a wake-up from falling edge of  $\overline{INT}$  and  $\overline{CS}$ .

**Note** In cases where  $\overline{\text{CS}}$  is used to wake the device, the first SO data message is not valid.

The sleep command contains settings for two programmable timers for Sleep mode, the interrupt timer and the scan timer, as shown in <u>Table 18</u> The interrupt timer is used as a periodic wake-up timer. When the timer expires, an interrupt is generated and the device enters Normal mode.

**Note** The interrupt timer in the 33972 device may be disabled by programming the interrupt bits to logic [1 1 1].

<u>Table 19</u> shows the programmable settings of the Interrupt timer.

Table 18. Sleep Command

		Sle	ep C	omma	nd									C	omma	nd Bi	ts						
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	int timer	int timer	int timer	scan timer	scan timer	scan timer

Table 19. Interrupt Timer

Bits 543	Interrupt Period
000	32 ms
001	64 ms
010	128 ms
011	256 ms
100	512 ms
101	1.024 s
110	2.048 s
111	No interrupt wake-up

The scan timer sets the polling period between input switch reads in Sleep mode. The period is set in the sleep command and may be set to 000 (no period) to 111 (64 ms). In Sleep mode when the scan timer expires, inputs will behave as programmed prior to sleep command. The 33972 will wake up for approximately 125  $\mu$ s and read the switch inputs. At the end of the 125  $\mu$ s, the input switch states are compared with the switch state prior to sleep command. When switch state changes are detected, an interrupt is generated (when enabled; refer to wake-up/interrupt command description on page 15), and the device enters Normal mode. Without switch state changes, the 33972 will reset the scan timer, inputs become tri-state, and the Sleep mode continues until the scan timer expires again.

<u>Table 20</u> shows the programmable settings of the Scan timer.

Table 20. Scan Timer

Bits 210	Scan Period
000	No Scan
001	1.0 ms
010	2.0 ms
011	4.0 ms
100	8.0 ms
101	16 ms
110	32 ms
111	64 ms

**Note** The interrupt and scan timers are disabled in the Normal Mode.

Figure 5, page 9, is a graphical description of how the 33972 device exits Sleep mode and enters Normal mode. Notice that the device will exit Sleep mode when the interrupt timer expires or when a switch change of state occurs. The falling edge of  $\overline{\text{INT}}$  triggers the MCU to wake from Sleep state. Figure 12 illustrates the current consumed during Sleep mode. During the 125 μs, the device is fully active and switch states are read. The quiescent current is calculated by integrating the normal running current over scan period plus approximately 60 μA.

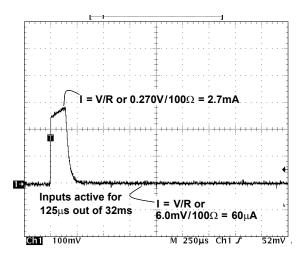


Figure 12. Sleep Current Waveform

#### **TEMPERATURE MONITOR**

With multiple switch inputs closed and the device programmed with the wetting current timers disabled, considerable power will be dissipated by the IC. For this reason, temperature monitoring has been implemented. The temperature monitor is active in the Normal mode only. When the IC temperature is above the thermal limit, the temperature monitor will do all of the following:

- · Generate an interrupt.
- Force all 16 mA pull-up and pull-down current sources to revert to 2.0 mA current sources.
- Maintain the 2.0 mA current source and all other functionality.
- · Set the thermal flag bit in the SPI output register.

The thermal flag bit in the SPI word will be cleared on rising edge of  $\overline{\text{CS}}$  provided the die temperature has cooled below the thermal limit. When die temperature has cooled below thermal limit, the device will resume previously programmed settings.

#### **TYPICAL APPLICATIONS**

#### **INTRODUCTION**

The 33972's primary function is the detection of open or closed switch contacts. However, there are many features that allow the device to be used in a variety of applications. The following is a list of applications to consider for the IC:

Sensor Power Supply

Switch Monitor for Metallic or Elastomeric Switches

Analog Sensor Inputs (Ratiometric)

Power MOSFET/LED Driver and Monitor

Multiple 33972 Devices in a Module System

The following paragraphs describe the applications in detail.

#### SENSOR POWER SUPPLY

Each input may be used to supply current to sensors external to a module. Many sensors such as Hall effect, pressure sensors, and temperature sensors require a supply voltage to power the sensor and provide an open collector or analog output. Figure 13 shows how the 33972 may be used to supply power and interface to these types of sensors. In an application where the input makes continuous transitions, consider using the wake-up/interrupt command to disable the interrupt for the particular input.

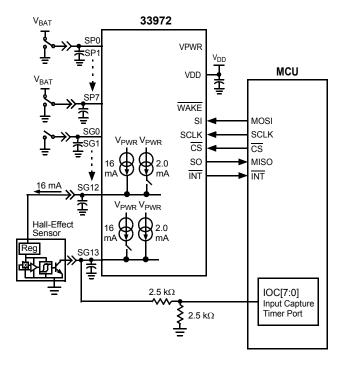


Figure 13. Sensor Power Supply

#### METALLIC/ELASTOMERIC SWITCH

Metallic switch contacts often develop higher contact resistance over time owing to contact corrosion. The corrosion is induced by humidity, salt, and other elements that exist in the environment. For this reason the 33972 provides two settings for contacts. When programmed for metallic switches, the device provides higher wetting current to keep switch contacts free of oxides. The higher current occurs for the first 20 ms of switch closure. Where longer duration of wetting current is desired, the user may send the wetting current timer command and disable the timer. Wetting current will be continuous to the closed switch. After the time period set by the MCU, the wetting current timer command may be sent again to enable the timer. The user must consider power dissipation on the device when disabling the timer. (Refer to the paragraph entitled Temperature Monitor, page <u>20</u>.)

To increase the amount of wetting current for a switch contact, the user has two options. Higher wetting current to a switch may be achieved by paralleling SGn or SPn inputs. This will increase wetting current by 16 mA for each input added to the switch contact. The second option is to simply add an external resistor pull-up to the  $V_{PWR}$  supply for switch-to-ground inputs or a resistor to ground for a switch-to-battery input. Adding an external resistor has no effect on the operation of the device.

Elastomeric switch contacts are made of carbon and have a high contact resistance. Resistance of 1.0 k $\Omega$  is common. In applications with elastomeric switches, the pull-up and pulldown currents must be reduced to prevent excessive power dissipation at the contact. Programming for a lower current settings is provided in the <u>Functional Device</u> <u>Operation</u> section beginning on page <u>13</u> under <u>Table 8</u>, Metallic Command.

#### **ANALOG SENSOR INPUTS (RATIOMETRIC)**

The 33972 features a 22-to-1 analog multiplexer. Setting the binary code for a specific input in the analog command allows the microcontroller to perform analog to digital conversion on any of the 22 inputs. On rising edge of CS the multiplexer connects a requested input to the AMUX pin. The AMUX pin is clamped to max of VDD volts regardless of the higher voltages present on the input pin. After an input has been selected as the analog, the corresponding bit in the next SO data stream will be logic [0].

The input pin, when selected as analog, may be configured as analog with high-impedance, analog with 2.0 mA pull-up, or analog with 16 mA pull-up. Figure 14, page 22, shows how the 33972 may be used to provide a ratiometric reading of variable resistive input.

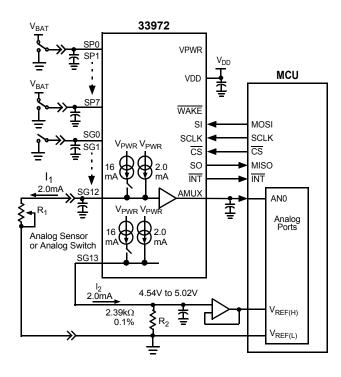


Figure 14. Analog Ratiometric Conversion

To read a potentiometer sensor, the wiper should be grounded and brought back to the module ground, as illustrated in <u>Figure 14</u>. With the wiper changing the impedance of the sensor, the analog voltage on the input will represent the position of the sensor.

Using the Analog feature to provide 2.0 mA of pull-up current to an analog sensor may induce error due to the accuracy of the current source. For this reason, a ratiometric conversion must be considered. Using two current sources (one for the sensor and one to set the reference voltage to the A/D converter) will yield a maximum error (owing to the 33972) of 4%.

Higher accuracy may be achieved through module level calibration. In this example, we use the resistor values from Figure 14 and assume the current sources are 4% from each other. The user may use the module end-of-line tester to calculate the error in the A/D conversion. By placing a 2.0 k $\Omega$ , 0.1% resistor in the end-of-line test equipment and assuming a perfect 2.0 mA current source from the 33972, a calculated A/D conversion may be obtained. Using the equation yields the following:

ADC = 
$$\frac{11 \times R1}{12 \times R2} \times 255$$
  
ADC =  $\frac{2.0 \text{mA} \times 2.0 \text{k}\Omega}{2.0 \text{mA} \times 2.39 \text{k}\Omega} \times 255$   
ADC = 213 counts

The ADC value of 213 counts is the value with 0% error (neglecting the resistor tolerance and AMUX input offset voltage). Now we can calculate the count value induced by the mismatch in current sources. From a sample device the maximum current source was measured at 2.05 mA and minimum current source was measured at 1.99 mA. This yields 3% error in A/D conversion. The A/D measurement will be as follows:

ADC = 
$$\frac{1.99\text{mA} \times 2.0\text{k}\Omega}{2.05\text{mA} \times 2.39\text{k}\Omega} \times 255$$
ADC = 207 counts

This A/D conversion is 3% low in value. The error correction factor of 1.03 may be used to correct the value:

An error correction factor may then be stored in  $E^2$  memory and used in the A/D calculation for the specific input. Each input used as analog measurement will have a dedicated calibrated error correction factor.

#### POWER MOSFET/LED DRIVER AND MONITOR

Because of the flexible programming of the 33972 device, it may be used to drive small loads like LEDs or MOSFET gates. It was specifically designed to power up in the Normal mode with the inputs tri-state. This was done to ensure the LEDs or MOSFETs connected to the 33972 power up in the off-state. The switch programmable inputs (SP0–SP7) have a source-and-sink capability, providing effective MOSFET gate control. To complete the circuit, a pull-down resistor should be used to keep the gate from floating during the Sleep modes. Figure 15, page 23, shows an application where the SG0 input is used to monitor the drain-to-source voltage of the external MOSFET. The 1.5 k $\Omega$  resistor is used to set the drain-to-source trip voltage. With the 2.0 mA current source enabled, an interrupt will be generated when the drain-to-source voltage is approximately 1.0 V.

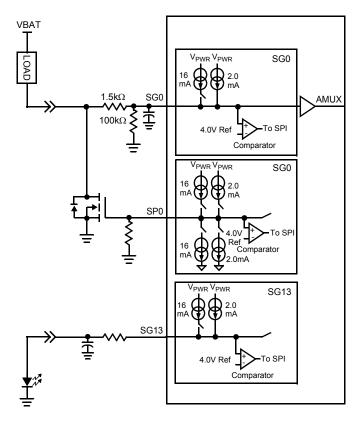


Figure 15. MOSFET or LED Driver Output

The sequence of commands (from Normal mode with inputs tri-state) required to set up the device to drive a MOSFET are as follows:

- wetting current timer enable command –Disable SPn wetting current timer (refer to <u>Table 9</u>, page <u>15</u>).
- metallic command –Set SPn to 16 or 2.0 mA gate drive current (refer to <u>Table 8</u>, page <u>15</u>).
- settings command –Set SPn as switch-to-battery (refer to <u>Table 6</u>, page <u>14</u>).
- tri-state command –Disable tri-state for SPn (refer to <u>Table 10</u>, page <u>16</u>).

After the tri-state command has been sent (tri-state disable), the MOSFET gate will be pulled to ground. From this point forward the MOSFET may be turned on and off by sending the settings command:

- settings command –SPn as switch-to-ground (MOSFET ON).
- settings command –SPn as switch-to-battery (MOSFET OFF).

Monitoring of the MOSFET drain in the OFF state provides open load detection. This is done by using an SGn input comparator. With the SGn input in tri-state, the load will pull up the SGn input to battery. With open load the SGn pin is pulled down to ground through an external resistor. The open load is indicated by a logic [1] in the SO data bit.

The analog command may be used to monitor the drain voltage in the MOSFET ON state. By sourcing 2.0 mA of

current to the 1.5 k $\Omega$  resistor, the analog voltage on the SGn pin will be approximately:

$$V_{SGn} = I_{SGn} \times 1.5 k\Omega + V_{DS}$$

As the voltage on the drain of the MOSFET increases, so does the voltage on the SGn pin. With the SGn pin selected as analog, the MCU may perform the A/D conversion.

Using this method for controlling unclamped inductive loads is not recommended. Inductive flyback voltages greater than  $V_{PWR}$  may damage the IC.

The SP0:SP7 pins of this device may also be used to send signals from one module to another. Operation is similar to the gate control of a MOSFET.

- For LED applications a resistor in series with the LED is recommended but not required. The switch-to-ground inputs are recommended for LED application. To drive the LED use the following commands:
- wetting current timer enable command –Disable SGn wetting current timer.
- metallic command –Set SGn to 16 mA.

From this point forward the LED may be turned on and off using the tri-state command:

- · tri-state command Disable tri-state for SGn (LED ON).
- tri-state command Enable tri-state for SGn (LED OFF).

These parameters are easily programmed via SPI commands in Normal mode.

#### **MULTIPLE 33972 DEVICES IN A MODULE SYSTEM**

Connecting power to the 33972 and the MCU for Sleep mode operation may be done in several ways. <u>Table 21</u> shows several system configurations for power between the MCU and the 33972 and their specific requirements for functionality.

Table 21. Sleep Mode Power Supply

MCU V <sub>DD</sub>	33972 V <sub>DD</sub>	Comments
5.0 V	5.0 V	All wake-up conditions apply. (Refer to <u>Sleep Mode</u> , page <u>19</u> .)
5.0 V	0 V	SPI wake-up is not possible.
0 V	5.0 V	Sleep mode not possible. Current from $\overline{\text{CS}}$ pullup will flow through MCU to $\text{V}_{\text{DD}}$ that has been switched off. Negative edge of $\overline{\text{CS}}$ will put 33972 in Normal mode.
0 V	0 V	SPI wake-up is not possible.

Multiple 33972 devices may be used in a module system. SPI control may be done in parallel or serial. However when parallel mode is used, each device is addressed independently (refer to MCU Interface Description, page 13). Therefore when sending the sleep command, one device will enter sleep before the other. For multiple devices in a system, it is recommended that the devices are controlled in serial (S0

## TYPICAL APPLICATIONS INTRODUCTION

from first device is connected to SI of second device). With two devices, 48 clock pulses are required to shift data in. When the WAKE feature is used to enable the power supply, both WAKE pins should be connected to the enable pin on the power supply. The INT pins may be connected to one interrupt pin on the MCU or may have their own dedicated interrupt to the MCU.

The transition from Normal to Sleep mode is done by sending the sleep command. With the devices connected in serial and the sleep command sent, both will enter Sleep mode on the rising edge of  $\overline{CS}$ . When Sleep mode is entered, the  $\overline{WAKE}$  pin will be logic [1]. If either device wakes up, the  $\overline{WAKE}$  pin will transition LOW, waking the other device.

A condition exists where the MCU is sending the sleep command (CS logic [0]) and a switch input changes state. With this event the device that detects this input will not transition to Sleep mode, while the second device will enter Sleep mode. In this case two switch status commands must be sent to receive accurate switch status data. The first switch status command will wake the device in Sleep mode. Switch status data may not be valid from the first switch status command because of the time required for the input voltage to rise above the 4.0 V input comparator threshold. This time is dependant on the impedance of SGn or SPn node. The second switch status command will provide accurate switch status information. It is recommended that software wait 10 to 20 ms between the two switch status commands, allowing time for switch input voltages to stabilize. With all switch states acknowledged by the MCU. the sleep sequence may be initiated. All parameters for Sleep mode should be updated prior to sending the sleep command.

The 33972 IC has an internal 5.0 V supply from the VPWR pin. A POR circuit monitors the internal 5.0 V supply. In the

event of transients on the VPWR pin, an internal reset may occur. Upon reset the 33972 will enter Normal mode with the internal registers as defined in <a href="Table 15">Table 15</a>, page <a href="18">18</a>. Therefore it is recommended that the MCU periodically update all registers internal to the IC.

#### **USING THE WAKE FEATURE**

The 33972 provides a  $\overline{\text{WAKE}}$  output and wake-up input designed to control an enable pin on system power supply. While in the Normal mode, the  $\overline{\text{WAKE}}$  output is LOW, enabling the power supply. In the Sleep mode, the  $\overline{\text{WAKE}}$  pin is high, disabling the power supply. The  $\overline{\text{WAKE}}$  pin has a passive pull-up to the internal 5.0 V supply but may be pulled up through a resistor to the V<sub>PWR</sub> supply (see Figure 17, page 25)

When the  $\overline{\text{WAKE}}$  output is not used, the pin should be pulled up to the  $V_{DD}$  supply through a resistor as shown in Figure 16, page 25.

During the Sleep mode, a switch closure will set the WAKE pin LOW, causing the 33972 to enter the Normal mode. The power supply will then be activated, supplying power to the VDD pin and the microprocessor and the 33972. The microprocessor can determine the source of the wake-up by reading the interrupt flag.

#### **COST AND FLEXIBILITY**

Systems requiring a significant number of switch interfaces have many discrete components. Discrete components on standard PWB consume board space and must be checked for solder joint integrity. An integrated approach reduces solder joints, consumes less board space, and offers wider operating voltage, analog interface capability, and greater interfacing flexibility.

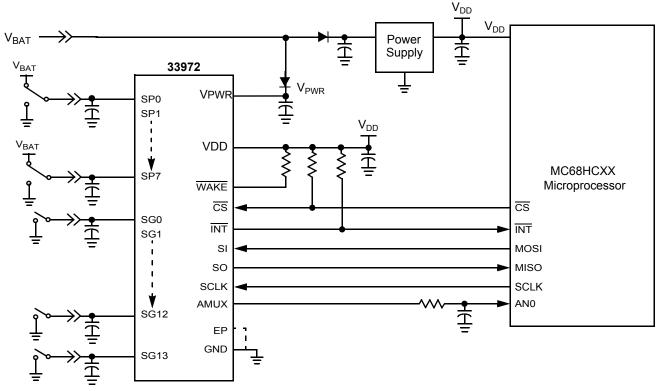


Figure 16. Power Supply Active in Sleep Mode

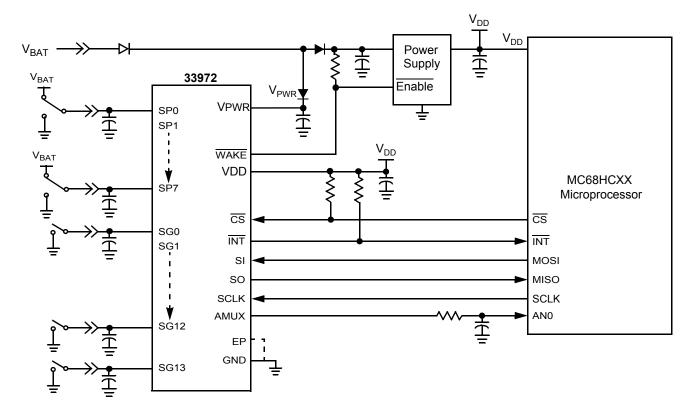
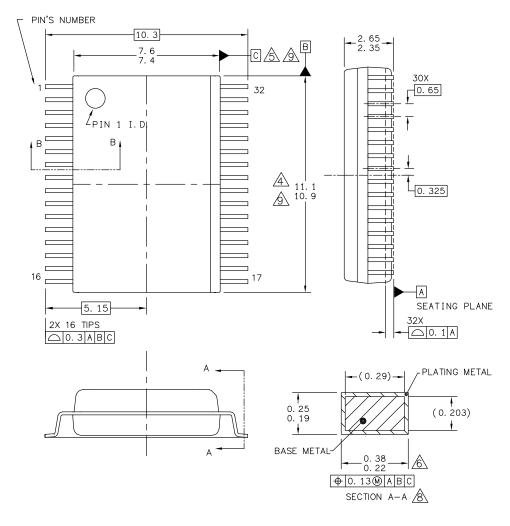


Figure 17. Power Supply Shutdown in Sleep Mode

#### **PACKAGING**

#### **PACKAGE DIMENSIONS**

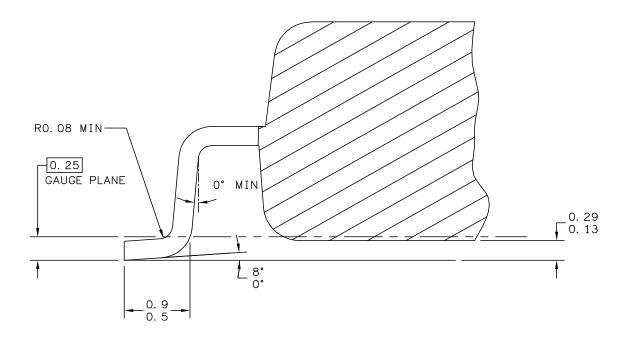
For the most current package revision, visit <u>www.freescale.com</u> and perform a keyword search using the 98A listed below.



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EW SUFFIX (Pb-FREE) 32-LEAD SOIC WIDE BODY 98ARH99137A ISSUE B

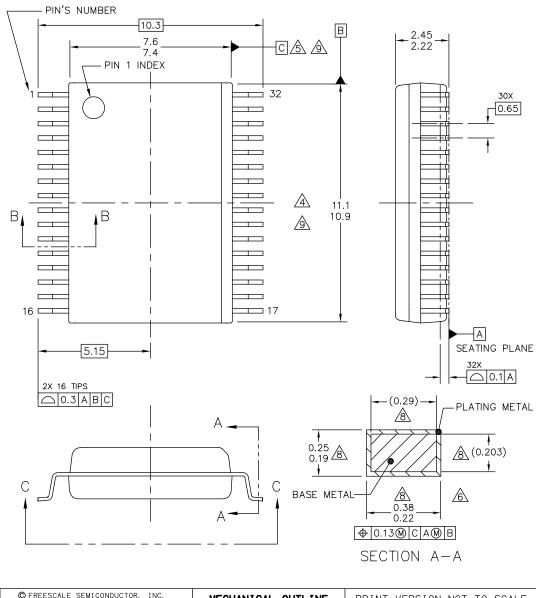
## **PACKAGE DIMENSIONS (CONTINUED)**



SECTION B-B

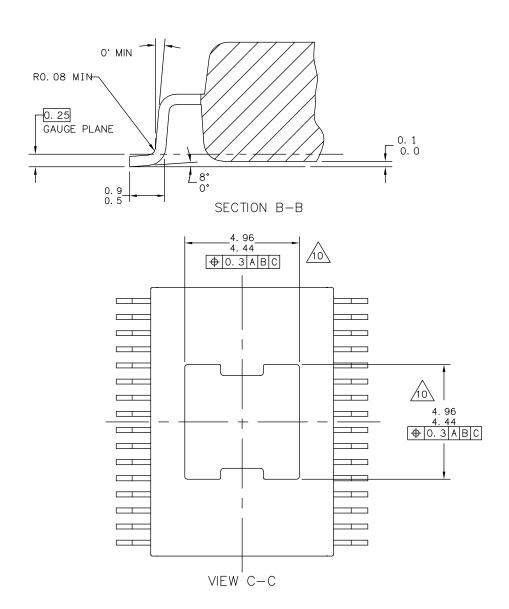
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TITLE: 32LD SOIC W/B, 0.65 PITCH 4.7 X 4.7 EXPOSED PAD, CASE—OUTLINE  DOCUMENT NO: 98ASA10556D REV: D CASE NUMBER: 1454-04 20 JUN 2008 STANDARD: NON-JEDEC	ALL RIGHTS RESERVED.	MECHANICA	L OUTLINE	PRINT VERSION NO	OT TO SCALE
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CASE-OUTLINE STANDARD: NON-JEDEC		CASE NUMBER	2: 1454–04	20 JUN 2008	
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#### NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.



THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.



THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.



THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.



EXACT SHAPE OF EACH CORNER IS OPTIONAL.



THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.



THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.



THESE DIMENSION RANGES DEFINE THE PRIMARY KEEP—OUT AREA. MOLD LOCKING AND RESIN BLEED CONTROL FEATURES MAY BE VISIBLE AND THEY MAY EXTEND TO 0.34mm FROM MAXIMUM EXPOSED PAD SIZE

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		CASE NUMBER	1: 1454-04	20 JUN 2008
CASE-OUTLINE	STANDARD: NO	N-JEDEC		

EK SUFFIX (Pb-FREE)
32-LEAD SOIC WIDE BODY
EXPOSED PAD
98ASA10556D
ISSUE D

## **REVISION HISTORY**

REVISION	DATE	DESCRIPTION OF CHANGES
4.0	2/2006	<ul> <li>Converted to Freescale format</li> <li>Added PC33972A version</li> <li>Changed Figure 15, Power Supply Active in Sleep Mode</li> <li>Changed Figure 16, Power Supply Shutdown in Sleep Mode</li> <li>Updated Outline Drawing for package</li> </ul>
5.0	6/2006	Update to the prevailing Freescale form and style.
6.0	7/2006	<ul> <li>Added MC33972T devices.</li> <li>Updated StatiC Electrical Characteristics on page 6 with 33972T parameters.</li> </ul>
7.0	11/2006	<ul> <li>Changed Human Body Model parameters in Maximum Ratings table.</li> <li>Replaced Part Number MC33972TEW/R2 with MCZ33972TEW/R2</li> <li>Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from Maximum Ratings on page 5. Added note with instructions to obtain this information from www.freescale.com.</li> </ul>
8.0	12/2006	Restated note (6)     Changed Part Number MCZ33972TEW/R2 with MC33972TEW/R2
9.0	4/2007	<ul> <li>Removed all references to the 33972T device.</li> <li>Removed the MC33972TDWB/R2, MC33972TEW/R2, and PC33972AEW/R2 from the ordering information.</li> <li>Added MCZ33972AEW/R2 to the ordering information.</li> </ul>
10.0	6/2007	<ul> <li>Added MC33972EW/R2, MC33972TDWB/R2, MC33972TEW/R2, and MCZ33972TEW/R2 to the ordering information.</li> </ul>
11.0	11/2007	<ul> <li>Updated to the current Freescale form and style</li> <li>Added MC33972AEK/R2 to the ordering information.</li> <li>Included device specific information relevant to the EK suffix on pages 1, 2, 4, 5, 6, 27, and 28.</li> <li>Added sentence to CHIP SELECT (CS) on page 10</li> <li>Made calculation corrections to Analog Sensor Inputs (Ratiometric)</li> </ul>
12.0	12/2007	Corrected Device Variation Table on page 2.
13.0	12/2007	Replaced Outline Drawing 98ARL10543D with 98ASA10556D.
14.0	6/2008	Added Note 7, "T <sub>C</sub> is the T <sub>CASE</sub> of the package" to Electrical Characteristics Table.
15.0	8/2008	Updated package drawing 98ASA10556D
16.0	10/2009	<ul> <li>Updated data sheet status from Advance Information to Technical Data</li> <li>Updated to the current Freescale form and style</li> </ul>
17.0	2/2011	<ul><li>Updated Freescale form and style</li><li>Added RoHS symbol</li></ul>
18.0	8/2011	<ul> <li>Revised Ordering Information Table by adding part numbers MC33972AEK/R2 and MC33972ATEW/R2, and removing part numbers MC33972DWB/R2 and MC33972TDWB/R2.</li> </ul>
19.0	3/2012	<ul> <li>Added the sentence "This condition in not a normal operating condition and can cause damage to the IC." to Programmable Switches (SP0:SP7) and Switch-to-ground Inputs (SG0:SG13)</li> <li>Changed sentence in Control and Protection Circuitry: "Characteristics are provided for V<sub>PWR</sub> from 8.0v to 26v for the IC (parametric tests are done from 8.0v to 16.0v)."</li> </ul>

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Document Number: MC33972

Rev. 19.0 3/2012



# MC33972

### Multiple Switch Detection Interface with Suppressed Wake-up

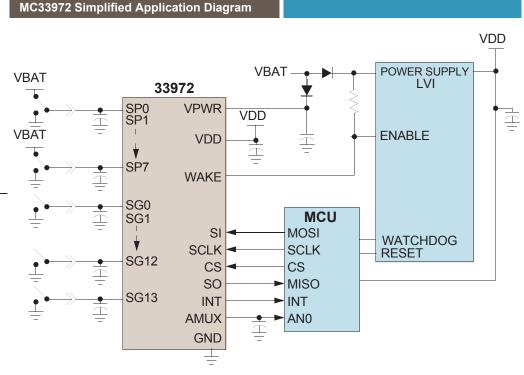
### **Applications**

- · Automotive Systems
- · Aircraft Systems
- · Industrial Control Systems
- · Process Control Systems
- · Security Systems
- Critical systems requiring switch status verification for safety, operation, or process control purposes

### Overview

The 33972 Multiple Switch Detection Interface with Suppressed Wake-up is designed to detect the closing and opening of up to 22 switch contacts. The switch status, either open or closed, is transferred to the microprocessor unit (MCU) through a serial peripheral interface (SPI). The device also features a 22-to-1 analog multiplexer for reading inputs as analog. The analog input signal is buffered and provided on the AMUX output terminal for the MCU to read.

The 33972 device has two modes of operation, Normal and Sleep. Normal mode allows programming of the device and supplies switch contacts with pullup or pulldown current as it monitors switch change of state. The Sleep mode provides low quiescent current, which makes the 33972 ideal for automotive and industrial products requiring low sleep state currents.



Performance	Typical Values
Operating Voltage	5.5 V ≤ V <sub>PWR</sub> ≤ 26 V
Switch Voltage Range	-14 to V <sub>PWR</sub>
Contact Wetting Current	2.0 or 16 mA
Quiescent Current:	
VPWR	< 100 µA
VDD	< 20 µA
Control	SPI
Outputs	4
Operating Temperature	-40 °C ≤ T <sub>A</sub> ≤ 125 °C



#### **Features**

- Switch input voltage range -14 V to V<sub>PWR</sub>, 40 V Max
- Interfaces directly to microprocessor using 3.3 V/5.0 V SPI protocol
- Selectable wake-up on change of state
- Selectable wetting current (16 mA or 2.0 mA)
- 8 programmable inputs (switches to battery or ground)
- · 14 switch-to-ground inputs
- V<sub>PWR</sub> standby current 100 μA typical,
   V<sub>DD</sub> standby current 20 μA typical
- Active interrupt (INT) on change-ofswitch state
- Pb-free packaging designated by suffix code EW and EK
- Devices available for comparison are in the Analog Product Selector Guide -SG1002 and Automotive Product Selector Guide - SG187

#### **Customer Benefits**

- Optimized multiple switch OPEN/ CLOSE status verification with immediate reporting to the MCU
- Interfaces to 3.3 V/5.0 V MCUs with SPI
- Surface-mounted device, requires minimal PC board space, few components, enhanced application reliability, and lower costs
- Simple power conservation solution providing a WAKE output for system wake-up from Sleep mode

#### Questions

- Do you need to confirm the status of multiple switches in your system?
- Do you need to verify a switch is closed to battery or ground?
- Do you need a switch verification device capable of analog voltage multiplex readout of sensing inputs?
- Do you need a switch verification device that is also capable of controlling small LEDs as well as MOSFET transistors?
- Do you need a switch verification device programmed and controlled via SPI?
- Do you need a switch monitoring device that "sleeps" until switches change status and then alerts the MCU that a switch state has changed?

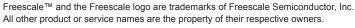
Ordering Information		
Device	Remperature Range	Package
MC33972TEW/R2	-40 to 125°C	32 SOICW
MC33972ATEW/R2	-40 to 125°C	32 SOICW
MC33972ATEK/R2	-40 to 125°C	32 SOICW-EP
Evaluation Board		
KIT33972AEWEVBE	Evaluation Board	
Documentation		
MC33972	Data sheet order number	
SG1002	Analog Product Selector	Guide
SG 187	Automotive Product Selec	ctor Guide

32 SOICW/EP



0.65 mm Pitch 7.5 x 11.0 mm Body

**Learn More**: For current information about Freescale products, please visit **www.freescale.com**.



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**URL** for Additional Information

PART INFORMATION

Mfg Item Number

Mfg Item Name

KC33972ATEK

SOIC 32 300ML 4.6EP.

SUPPLIER Company Name Freescale Semiconductor Inc Company Unique ID 14-141-7928 Response Date 2013-12-27 Response Document ID 007YK10945D016A1.2 Contact Name Freescale Semiconductor Inc Contact Title Product Technical Support **Contact Phone** 1-800-521-6274 Contact Email support@freescale.com Daniel Binyon **Authorized Representative** Representative Title **EPP Customer Response** Representative Phone 512-895-3406 Representative Email eppanlst@freescale.com

DECLARATION

EU RoHS
Pb Free
Yes
HalogenFree
Plating Indicator
EU RoHS Exemption(s)

www.freescale.com

MANUFACTURING Mfg Item Number KC33972ATEK Mfg Item Name SOIC 32 300ML 4.6EP. Version ALL Weight 0.472000 UoM Unit Volume EACH J-STD-020 MSL Rating 3 Peak Processing Temperature 260 C Max Time at Peak Temperature 40 seconds Number of Processing Cycles 3

RoHS	
RoHS Directive	2011/65/EU
RoHS Definition	RoHS Definition: Quantity limit of 0.1% by mass (1000 PPM) of homogeneous material for: Lead (Pb), Mercury, Hexavalent Chromium, Polybrominated Biphenyls (PBB), Polybrominated Diphenyl Ethers (PBDE) and quantity limit of 0.01% by mass (100 PPM) of homogeneous material of Cadmium
RoHS Legal Definition	Please indicate whether any homogeneous material (as defined by the RoHS Directive, EU 2011/65/EU and implemented by the laws of the European Union member states) of the part(s) identified on this form contains lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls and/or polybrominated diphenyl ethers (each a RoHS restricted substance) in excess of the applicable quantity limit, please indicate below which, if any, RoHS exemption you believe may apply. If the part is an assembly with lower level components, the declaration shall encompass all such components. Supplier certifies that it gathered the information it provides in this form using appropriate methods to ensure its accuracy and that such information is true and correct to the best of its knowledge and belief, as of the date that Supplier completes this form. Supplier acknowledges that Company will rely on this certification in determining the compliance of its products with European Union member state laws that implement the RoHS Directive. Company acknowledges that Supplier may have relied on information provided by others in completing this form, and that Supplier may not have independently verified such information. However, in situations where Supplier has not independently verified information provided by others, Supplier agrees that, at a minimum, its suppliers have provided certifications regarding their contributions to the part(s), and those certifications are at least as comprehensive as the certification in this paragraph. If the Company and the Supplier enter into a written agreement with respect to the identified part(s), the terms and conditions of that agreement, including any warranty rights and/or remedies provided as part of that agreement, will be the sole and exclusive source of the Suppliers liability and the Companys remedies for issues that arise regarding information the Supplier provides in this form. In the absence of such written agreement, the warranty rights and/or remedies of Suppliers Standard Terms and Co
RoHS Declaration	1 - Item(s) do not contain RoHS restricted substances per the definition above
Supplier Acceptance	Accepted
Signature	Daniel Binyon
Exemption List Version	2012/51/EU
List of Freescale Accepted Exemptions	6(a): Lead as an alloying element in steel for machining purposes and in galvanized steel containing up to 0.35% lead by weight
Exemptions	6(b): Lead as an alloying element in aluminium containing up to 0.4% lead by weight
	6(c): Copper alloy containing up to 4% lead by weight
	7(a): Lead in high melting temperature type solders (i.e. lead-based alloys containing 85% by weight or more lead)
	7(b): Lead in solders for servers, storage and storage array systems, network infrastructure equipment for switching, signaling, transmission, and network management for telecommunications
	7(c)-I : Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors, e.g. piezoelectronic devices, or in a glass or ceramic matrix compound
	7(c)-II: Lead in dielectric ceramic in capacitors for a rated voltage of 125 V AC or 250 V DC or higher
	7(c)-III: Lead in dielectric ceramic in capacitors for a rated voltage of less than 125 V AC or 250 V DC
	7(c)-IV: Lead in PZT based dielectric ceramic materials for capacitors being part of integrated circuits or discrete semiconductors
	15: Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip chip packages

Homogeneous Material	Weight	SubstanceClass	Substance	CAS	Exemption	SubstanceWeight	UoM	SubPart PPM	SubPart%	ARTICLEPPM	ARTICLE%
Epoxy Die Attach	0.0008						g				
Epoxy Die Attach		Cadmium/Cadmium Compounds	Cadmium	7440-43-9		0	g	3	0.0003	0	0
Epoxy Die Attach		Plastics/polymers	Phenolic Polymer Resin, Epikote 155	9003-36-5		0.00014913	g	186411	18.6411	315	0.0315
Epoxy Die Attach		Lead/Lead Compounds	Lead	7439-92-1		0.00000001	g	7	0.0007	0	0
Epoxy Die Attach		Metals	Silver, metal	7440-22-4		0.00065086	g	813579	81.3579	1378	0.1378
Copper Lead Frame	0.126						g				
Copper Lead Frame		Metals	Copper, metal	7440-50-8		0.12145833	g	963955	96.3955	257326	25.7326
Copper Lead Frame		Solvents, additives, and other materials	Phosphorus	7723-14-0		0.00010395	g	825	0.0825	220	0.022
Copper Lead Frame		Metals	Iron, metal	7439-89-6		0.002961	g	23500	2.35	6273	0.6273
Copper Lead Frame		Lead/Lead Compounds	Lead	7439-92-1		0.00002142	g	170	0.017	45	0.0045
Copper Lead Frame		Metals	Silver, metal	7440-22-4		0.00126	g	10000	1	2669	0.2669
Copper Lead Frame		Metals	Tin, metal	7440-31-5		0.0000378	g	300	0.03	80	0.008
Copper Lead Frame		Metals	Zinc, metal	7440-66-6		0.0001575	g	1250	0.125	333	0.0333
Lead Frame Plating	0.0032						g				
Lead Frame Plating		Lead/Lead Compounds	Lead	7439-92-1		0.00000064	g	200	0.02	1	0.0001
Lead Frame Plating		Metals	Tin, metal	7440-31-5		0.00319936	g	999800	99.98	6778	0.6778
Silicon Semiconductor Die	0.0098						g				
Silicon Semiconductor Die		Solvents, additives, and other materials	Other miscellaneous substances (less than 5%).	-		0.000196	g	20000	2	415	0.0415
Silicon Semiconductor Die		Glass	Silicon, doped	-		0.009604	g	980000	98	20347	2.0347
Die Encapsulant, Halogen-free	0.3311						g				
Die Encapsulant, Halogen-free		Solvents, additives, and other materials	Acrylonitrile/Butadiene copolymer, carboxyl terminated (26/74)	68891-46-3		0.0003311	g	1000	0.1	701	0.0701
Die Encapsulant, Halogen-free		Plastics/polymers	Ortho-Cresol, Polymer with 1-Chloro-2,3-Epoxypropane and Formaldehyde	29690-82-2		0.0072842	g	22000	2.2	15432	1.5432
Die Encapsulant, Halogen-free		Plastics/polymers	Proprietary Material-Other Epoxy resins	-		0.0109263	g	33000	3.3	23148	2.3148
Die Encapsulant, Halogen-free		Solvents, additives, and other materials	Carbon Black	1333-86-4		0.0009933	g	3000	0.3	2104	0.2104
Die Encapsulant, Halogen-free		Plastics/polymers	Proprietary Material-Other phenolic resins	-		0.0142373	g	43000	4.3	30163	3.0163
Die Encapsulant, Halogen-free		Glass	Silicon dioxide	7631-86-9		0.013244	g	40000	4	28059	2.8059
Die Encapsulant, Halogen-free		Glass	Silica, vitreous	60676-86-0		0.2840838	g	858000	85.8	601884	60.1884
Bonding Wire, Copper	0.0011						g				
Bonding Wire, Copper		Metals	Copper, metal	7440-50-8		0.001067	g	970000	97	2260	0.226
Bonding Wire, Copper		Solvents, additives, and other materials	Other miscellaneous substances (less than 5%).	-		0.000033	g	30000	3	69	0.0069

LINKS

MCD LINK

http://www.freescale.com Freescale website

GENERAL ENVIRONMENTAL COMPLIANCE LINKS

http://www.freescale.com/files/abstract/corporate/ehs\_epp/ENV\_ROHS\_Freescale\_Response.pdf RoHS signed letter

China RoHS http://www.freescale.com/chinarohs

REACH signed letter  $http://www.freescale.com/files/abstract/corporate/ehs\_epp/ENV\_REACH\_Freescale\_Response.pdf$ ELV signed letter http://www.freescale.com/files/abstract/corporate/ehs\_epp/ENV\_ELV\_Freescale\_Reponse.pdf

**Conflict Minerals statement**  $http://www.freescale.com/files/abstract/corporate/ehs\_epp/ENV\_CONFLICT\_METAL\_Freescale\_Response.pdf$ 

FREESCALE ENVIRONMENTAL INFORMATION

EPP website http://www.freescale.com/epp

FAQ http://www.freescale.com/webapp/sps/site/overview.jsp?code=ENVIRON\_FAQ

Technical Service Request https://www.freescale.com/webapp/servicerequest.create\_SR.framework?defaultCategory=Hardware Product Support&defaultTopic=Environmentally Preferred Prod

LINKS TO BLANK IPC1752 FORMS

Blank IPC1752 v1.1 Form http://www.freescale.com/files/abstract/corporate/ehs\_epp/IPC-1752-2\_v1.1\_MCD\_Template.pdf

### IPC1752 XML LINKS

http://www.freescale.com/mcds/KC33972ATEK\_IPC1752\_v11.xml

http://www.freescale.com/mcds/KC33972ATEK\_IPC1752A.xml

**URL** for Additional Information

PART INFORMATION

Mfg Item Number

Mfg Item Name

SOIC 32 300ML

SUPPLIER Company Name Freescale Semiconductor Inc Company Unique ID 14-141-7928 Response Date 2013-11-15 Response Document ID 2013K10517D034A1.1 Contact Name Freescale Semiconductor Inc Contact Title Product Technical Support **Contact Phone** 1-800-521-6274 Contact Email support@freescale.com **Authorized Representative** Daniel Binyon Representative Title **EPP Customer Response** Representative Phone 512-895-3406 Representative Email eppanlst@freescale.com

DECLARATION

EU RoHS
Pb Free
Yes
HalogenFree
Plating Indicator
EU RoHS Exemption(s)

www.freescale.com

MANUFACTURING Mfg Item Number KC33972ATEW Mfg Item Name SOIC 32 300ML Version ALL Weight 0.510000 UoM Unit Volume EACH J-STD-020 MSL Rating 3 Peak Processing Temperature 260 C Max Time at Peak Temperature 40 seconds Number of Processing Cycles 3

RoHS	
RoHS Directive	2011/65/EU
RoHS Definition	RoHS Definition: Quantity limit of 0.1% by mass (1000 PPM) of homogeneous material for: Lead (Pb), Mercury, Hexavalent Chromium, Polybrominated Biphenyls (PBB), Polybrominated Diphenyl Ethers (PBDE) and quantity limit of 0.01% by mass (100 PPM) of homogeneous material of Cadmium
RoHS Legal Definition	Please indicate whether any homogeneous material (as defined by the RoHS Directive, EU 2011/65/EU and implemented by the laws of the European Union member states) of the part(s) identified on this form contains lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls and/or polybrominated diphenyl ethers (each a RoHS restricted substance) in excess of the applicable quantity limit, please indicate below which, if any, RoHS exemption you believe may apply. If the part is an assembly with lower level components, the declaration shall encompass all such components. Supplier certifies that it gathered the information it provides in this form using appropriate methods to ensure its accuracy and that such information is true and correct to the best of its knowledge and belief, as of the date that Supplier completes this form. Supplier acknowledges that Company will rely on this certification in determining the compliance of its products with European Union member state laws that implement the RoHS Directive. Company acknowledges that Supplier may have relied on information provided by others in completing this form, and that Supplier may not have independently verified such information. However, in situations where Supplier has not independently verified information provided by others, Supplier agrees that, at a minimum, its suppliers have provided certifications regarding their contributions to the part(s), and those certifications are at least as comprehensive as the certification in this paragraph. If the Company and the Supplier enter into a written agreement with respect to the identified part(s), the terms and conditions of that agreement, including any warranty rights and/or remedies provided as part of that agreement, will be the sole and exclusive source of the Suppliers liability and the Companys remedies for issues that arise regarding information the Supplier provides in this form. In the absence of such written agreement, the warranty rights and/or remedies of Suppliers Standard Terms and Co
RoHS Declaration	1 - Item(s) do not contain RoHS restricted substances per the definition above
Supplier Acceptance	Accepted
Signature	Daniel Binyon
Exemption List Version	2012/51/EU
List of Freescale Accepted Exemptions	6(a): Lead as an alloying element in steel for machining purposes and in galvanized steel containing up to 0.35% lead by weight
Exemptions	6(b): Lead as an alloying element in aluminium containing up to 0.4% lead by weight
	6(c): Copper alloy containing up to 4% lead by weight
	7(a): Lead in high melting temperature type solders (i.e. lead-based alloys containing 85% by weight or more lead)
	7(b): Lead in solders for servers, storage and storage array systems, network infrastructure equipment for switching, signaling, transmission, and network management for telecommunications
	7(c)-I : Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors, e.g. piezoelectronic devices, or in a glass or ceramic matrix compound
	7(c)-II: Lead in dielectric ceramic in capacitors for a rated voltage of 125 V AC or 250 V DC or higher
	7(c)-III: Lead in dielectric ceramic in capacitors for a rated voltage of less than 125 V AC or 250 V DC
	7(c)-IV: Lead in PZT based dielectric ceramic materials for capacitors being part of integrated circuits or discrete semiconductors
	15: Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip chip packages

Homogeneous Material	Weight				SubstanceWeight	UoM	SubPart PPM	SubPart%	ARTICLEPPM	ARTICLE%
Epoxy Die Attach	0.0011					g				
Epoxy Die Attach		Cadmium/Cadmium Compounds	Cadmium	7440-43-9	0	g	3	0.0003	0	0
Epoxy Die Attach		Plastics/polymers	Phenolic Polymer Resin, Epikote 155	9003-36-5	0.00020505	g	186411	18.6411	402	0.0402
Epoxy Die Attach		Lead/Lead Compounds	Lead	7439-92-1	0.00000001	g	7	0.0007	0	0
poxy Die Attach		Metals	Silver, metal	7440-22-4	0.00089494	g	813579	81.3579	1754	0.1754
Copper Lead Frame	0.1359					g				
opper Lead Frame		Metals	Copper, metal	7440-50-8	0.13100148	g	963955	96.3955	256865	25.6865
opper Lead Frame		Solvents, additives, and other materials	Phosphorus	7723-14-0	0.00011212	g	825	0.0825	219	0.0219
opper Lead Frame		Metals	Iron, metal	7439-89-6	0.00319365	g	23500	2.35	6262	0.6262
opper Lead Frame		Lead/Lead Compounds	Lead	7439-92-1	0.0000231	g	170	0.017	45	0.0045
opper Lead Frame		Metals	Silver, metal	7440-22-4	0.001359	g	10000	1	2664	0.2664
opper Lead Frame		Metals	Tin, metal	7440-31-5	0.00004077	g	300	0.03	79	0.0079
opper Lead Frame		Metals	Zinc, metal	7440-66-6	0.00016988	g	1250	0.125	333	0.0333
ead Frame Plating	0.0032					g				
ead Frame Plating		Lead/Lead Compounds	Lead	7439-92-1	0.00000064	g	200	0.02	1	0.0001
ead Frame Plating		Metals	Tin, metal	7440-31-5	0.00319936	g	999800	99.98	6273	0.6273
licon Semiconductor Die	0.0098					g				
licon Semiconductor Die		Solvents, additives, and other materials	Other miscellaneous substances (less than 5%).	-	0.000196	g	20000	2	384	0.0384
licon Semiconductor Die		Glass	Silicon, doped	-	0.009604	g	980000	98	18831	1.8831
e Encapsulant, Halogen-free	0.3589					g				
ie Encapsulant, Halogen-free		Solvents, additives, and other materials	Acrylonitrile/Butadiene copolymer, carboxyl terminated (26/74)	68891-46-3	0.0003589	g	1000	0.1	703	0.0703
ie Encapsulant, Halogen-free		Plastics/polymers	Ortho-Cresol, Polymer with 1-Chloro-2,3-Epoxypropane and Formaldehyde	29690-82-2	0.0078958	g	22000	2.2	15481	1.5481
e Encapsulant, Halogen-free		Plastics/polymers	Proprietary Material-Other Epoxy resins		0.0118437	g	33000	3.3	23222	2.3222
e Encapsulant, Halogen-free		Solvents, additives, and other materials	Carbon Black	1333-86-4	0.0010767	g	3000	0.3	2111	0.2111
e Encapsulant, Halogen-free		Plastics/polymers	Proprietary Material-Other phenolic resins		0.0154327	g	43000	4.3	30260	3.026
e Encapsulant, Halogen-free		Glass	Silicon dioxide	7631-86-9	0.014356	g	40000	4	28149	2.8149
ie Encapsulant, Halogen-free		Glass	Silica, vitreous	60676-86-0	0.3079362	g	858000	85.8	603806	60.3806
onding Wire, Copper	0.0011					g				
onding Wire, Copper		Metals	Copper, metal	7440-50-8	0.001067	g	970000	97	2092	0.2092
onding Wire, Copper		Solvents, additives, and other materials	Other miscellaneous substances (less than 5%).		0.000033	q	30000	3	64	0.0064

LINKS

MCD LINK

http://www.freescale.com Freescale website

GENERAL ENVIRONMENTAL COMPLIANCE LINKS

http://www.freescale.com/files/abstract/corporate/ehs\_epp/ENV\_ROHS\_Freescale\_Response.pdf RoHS signed letter

China RoHS http://www.freescale.com/chinarohs

REACH signed letter  $http://www.freescale.com/files/abstract/corporate/ehs\_epp/ENV\_REACH\_Freescale\_Response.pdf$ ELV signed letter http://www.freescale.com/files/abstract/corporate/ehs\_epp/ENV\_ELV\_Freescale\_Reponse.pdf

**Conflict Minerals statement**  $http://www.freescale.com/files/abstract/corporate/ehs\_epp/ENV\_CONFLICT\_METAL\_Freescale\_Response.pdf$ 

FREESCALE ENVIRONMENTAL INFORMATION

EPP website http://www.freescale.com/epp

FAQ http://www.freescale.com/webapp/sps/site/overview.jsp?code=ENVIRON\_FAQ

Technical Service Request https://www.freescale.com/webapp/servicerequest.create\_SR.framework?defaultCategory=Hardware Product Support&defaultTopic=Environmentally Preferred Prod

LINKS TO BLANK IPC1752 FORMS

Blank IPC1752 v1.1 Form http://www.freescale.com/files/abstract/corporate/ehs\_epp/IPC-1752-2\_v1.1\_MCD\_Template.pdf IPC1752 XML LINKS

http://www.freescale.com/mcds/KC33972ATEW\_IPC1752\_v11.xml

http://www.freescale.com/mcds/KC33972ATEW\_IPC1752A.xml

# **Engineering Change Documents**



# AEC Q100 Certification of Design, Construction and Qualification Q100base-revG; -001revC, -002revD, -003revE, -004revC, -005recC, -006revD, -007revA, -008revA, -009revB, -010revA, -011revB, -012Rev.

П	Supplier Name: Freescale Semiconductor	Date:
	Item Name	Supplier Response
1.	User's Part Number:	See PPAP
2.	Supplier's Part Number/Data Sheet:	MC33972ATEKR2/48ASA12749D
3.	Device Description:	MSDISW_N39B SM5AP(EP)
4.	Wafer/Die Fab Facility & Process ID:	MSDISW_NSBI SWISAI (EL)
Ι*	•	
	a. Facility name/plant #:	TSMC
	b. Street address:	.No. 121 Park Ave. III, Hsinchu Science Park; Hsinchu, Taiwan 300, R.O.C. (TSMC2)
	c. Country:	Taiwan
	c. country.	Taiwan
5.	Wafer Probe Location:	
	- F114	Freescale-Qualified Probe Site(s); Available Upon
	a. Facility name/plant #:	Request
	b. Street address:	Available Upon Request
	c. Country:	Available Upon Request
6.	Assembly Location & Process ID:	
	a. Facility name/plant #:	FSL-TJN-FM
	b. Street address:	No.15, Xing Hua Avenue; XiQing 300385 Tianjin China (TJN)
	c. Country:	China
7.	Final Quality Control A (Test) Facility:	
	a. Facility name/plant #:	FSL-TJN-FM
	b. Street address:	No.15, Xing Hua Avenue; XiQing 300385 Tianjin China (TJN)
	c. Country:	China
8.	Wafer/Die:	Cinia
	a. Wafer Size:	150 mm
	h Die femilier	MCDI N20D
	b. Die family:	MSDI-N39B
	c. Die mask set revision & name:	N39B-MASK
	d. Die photo:	Available upon request-linrick
9.	Die Technology Description:	
	a. Wafer/Die process technology:	u065
	b. Die channel length (μM):	1.6um
	c. Die gate length (µM): d. Die supplier process ID (mask #):	1.6um N39B
	e. Number of transistors or gates:	26917
		18
10	f. Number of mask steps: Die Dimensions:	10
1.0.	a. Die width (mm):	2.9464 mm
1	b. Die length (mm):	4.04622 mm
1	c. Die thickness (finished) (mm):	0.381 mm
11.	Die Metallization:	
1	a. Die metallization materials:	AlCuSi
1	b. Number of layers:	2
	c. Thickness (per layer):	M1: 6kA M2: 20kA
1	d. % of alloys (if present):	99.5% Al/0.5% Cu
1	a. // or anoys (ii present).	22.0 % 1110.0 % Cu



# AEC Q100 Certification of Design, Construction and Qualification Q100base-revG; -001revC, -002revD, -003revE, -004revC, -005recC, -006revD, -007revA, -

	008revA, -009revB, -010revA, -011revB, -012Rev					
	Supplier Name: Freescale Semiconductor	Date:				
12.	Die Passivation:					
	a. Number of passivation layers:	2				
	b. Die passivation material(s):	SiO2/Si3N4				
	c. Thickness (es) & tolerances:	2kÅ /7kÅ				
13.	Die Overcoat Material (e.g., Polyimide)	Polyimide				
	Die Cross-Section Photo/Drawing:	Available upon request				
15.	Die Prep Backside:					
	a. Die prep method:	None				
	b. Die metallization:	None				
	c. Thickness(es) & tolerances:	N/A				
16.	Die Separation Method (Kerf Depth):					
	a. Kerf width (um):	20 - 100um				
	b. Kerf depth (if not 100% saw):	100% Sawn				
	c. Saw method:	Dual				
17.	Die Attach:					
	a. Die attach material ID:	Sumitomo CRM-1064MBL				
	b. Die attach method:	Epoxy				
	c. Die placement diagram:	Available upon request				
18.	Package:					
	<ul> <li>Type of package (e.g. plastic, ceramic,</li> </ul>	Plastic				
	unpackaged):					
	b. Ball/lead count:	32LD SOIC EP				
	<ul> <li>JEDEC designation (e.g., MS029, MS034,</li> </ul>	NON-JEDEC				
	d. Lead (Pb) free (<.1% homogenouse material)	Yes				
	e. Package outline drawing	See PPAP				
19.	Mold Compound:					
	<ul> <li>a. Plastic mold compound supplier &amp; ID:</li> </ul>	Sumitomo EME-G630AY				
	b. Mold compound type:	Epoxy Resin				
	c. Flammability rating:	UL 94 V0				
	d. Fire Retardant type/composition	Resin system				
	e. Tg (glass transition temperature) (°C):	Tg=120C				
	f. CTE (above & below Tg) (ppm/°C):	CTE1 (below Tg) = 10 ppm/°C, CTE2 (above				
		Tg) = 40 ppm/ °C				
20.	Wire Bond:					
	a. Wire bond material:	Cu				
	b. Wire bond diameter (mm):	0.033				
	c. Type of wire bond at die:	Ball bond				
	d. Type of wire bond at leadframe:	Stitch bond				
L	e. Wire bonding diagram:	Available upon request				
21.	Leadframe (if applicable):					
	a. Paddle/flag material:	Cu				
	b. Paddle/flag width (mils):	5.1562 mm				
	c. Paddle/flag length (mils):	5.1562 mm				
	d. Paddle/flag plating composition:	None				
	e. Paddle/flag plating thickness (μin):	NA				
	f. Leadframe material:	Cu				
	g. Leadframe bonding plating composition:	Ag				
	h. Leadframe bonding plating thickness (um):	1.78 - 7.62				
l	<ol> <li>External lead plating composition:</li> </ol>	Sn				
	j. External lead plating thickness (um):	7.62 - 17.8				



# AEC Q100 Certification of Design, Construction and Qualification Q100base-revG; -001revC, -002revD, -003revE, -004revC, -005recC, -006revD, -007revA, -

	008revA, -009revB, -010revA, -011revB, -012Rev					
	Supplier Name: Freescale Semiconductor	Date:				
22.	Substrate (if applicable):	Not applicable				
	a. Substrate material (e.g., FR5, BT, etc.):					
	b. Substrate thickness (mm):					
	c. Number of substrate metal layers:					
	d. Plating composition of ball solderable surface:					
	e. Panel singulation method:					
	f. Solder ball composition:					
	g: Solder ball diameter (mm):					
23.	Unpackaged Die (if not packaged):	Not Applicable				
	a. Under Bump Metallurgy (UBM):					
	b. Thickness of UBM metal:					
	c. Bump composition:					
	d. Bump size:					
	Header material (if applicable):	Not Applicable				
25.	Thermal Resistance:	Leave blank				
	a. ØJA °C/W (approx):	74				
	b. ØJC °C/W (approx):	26				
	c. Special thermal dissipation construction	Not Applicable				
	techniques:	1vot repricasio				
	Test circuits, bias levels and operational					
26.	conditions imposed during the supplier's life and	Available upon request				
	environmental tests:					
27.	Fault grade coverage (%):					
28.	Maximum Process Exposure Conditions:	Note: Temperatures are as measured on the center of the plastic package body top surface.				
	a. MSL @ rated SnPb temperature:	NA				
	b. MSL @ rated Pb-free temperature:	MSL3 at 260°C				
	c. Maximum dwell time @ maximum process	40				
	temperature:	40				
	Attachments:	Requirements:				
	Die Photo:	<ol> <li>A separate Certification of Design,</li> </ol>				
	Available Upon Request	Construction & Qualification must be submitted				
	Package Outline Drawing:	for each part number, wafer fab, and assembly				
	See PPAP	location.				
	Die Cross-Section Photos/Drawing:					
	Available Upon Request					
	Wire Bonding Diagram	Design, Construction & Qualification shall be				
	Available Upon Request	compiled by the responsible individual at the				
	Die Placement Diagram	supplier who can verify the above information is				
	See PPAP	accurate and complete.				
	Test Circuits, Bias Levels, & Conditions					
<u> </u>	Available Upon Request					
	Completed by and Date:	Completed by: Wang Brenda / 11-DEC-2013				
	Certified by (electronic signature) and Date:	Completed by: Wang Brenda / 11-DEC-2013				



# AEC Q100 Certification of Design, Construction and Qualification Q100base-revG; -001revC, -002revD, -003revE, -004revC, -005recC, -006revD, -007revA, -008revA, -009revB, -010revA, -011revB, -012Rev.

	Supplier Name: Freescale Semiconductor	Date:
	Item Name	Supplier Response
1.	User's Part Number:	See PPAP
2.	Supplier's Part Number/Data Sheet:	MC33972ATEWR2/48ASA12749D
3.	Device Description:	MSDISW_N39B SM5AP(non EP)
4.	Wafer/Die Fab Facility & Process ID:	
	a. Facility name/plant #:	TSMC
	b. Street address:	No. 121 Park Ave. III, Hsinchu Science Park; Hsinchu, Taiwan 300, R.O.C. (TSMC2)
	c. Country:	Taiwan
5.	Wafer Probe Location:	
	a. Facility name/plant #: b. Street address: c. Country:	Freescale-Qualified Probe Site(s); Available Upon Request Available Upon Request Available Upon Request
6.	Assembly Location & Process ID:	Available Opoli Request
	a. Facility name/plant #:	FSL-TJN-FM
	b. Street address:	No.15, Xing Hua Avenue; XiQing 300385 Tianjin China (TJN)
	c. Country:	China
7.	Final Quality Control A (Test) Facility:	
	a. Facility name/plant #:	FSL-TJN-FM
	b. Street address:	No.15, Xing Hua Avenue; XiQing 300385 Tianjin China (TJN)
	c. Country:	China
8.	Wafer/Die:	
	a. Wafer Size:	150 mm
	b. Die family:	MSDI-N39B
L	c. Die mask set revision & name: d. Die photo:	N39B-MASK Available upon request
9.	Die Technology Description:	-065
	<ul> <li>a. Wafer/Die process technology:</li> <li>b. Die channel length (μM):</li> </ul>	u065 1.6um
	c. Die gate length (µM):	1.6um
	d. Die supplier process ID (mask #):	N39B
	e. Number of transistors or gates:	26917
	f. Number of mask steps:	18
10.	Die Dimensions:	<u> </u>
	a. Die width (mm):	2.9464 mm
	b. Die length (mm): c. Die thickness (finished) (mm):	4.04622 mm 0.381 mm
11.	Die Metallization:	5.551 MIII
	a. Die metallization materials:	AlCuSi
	b. Number of layers:	2
	c. Thickness (per layer):	M1: 6kA M2: 20kA
	d. % of alloys (if present):	99.5% Al/0.5% Cu



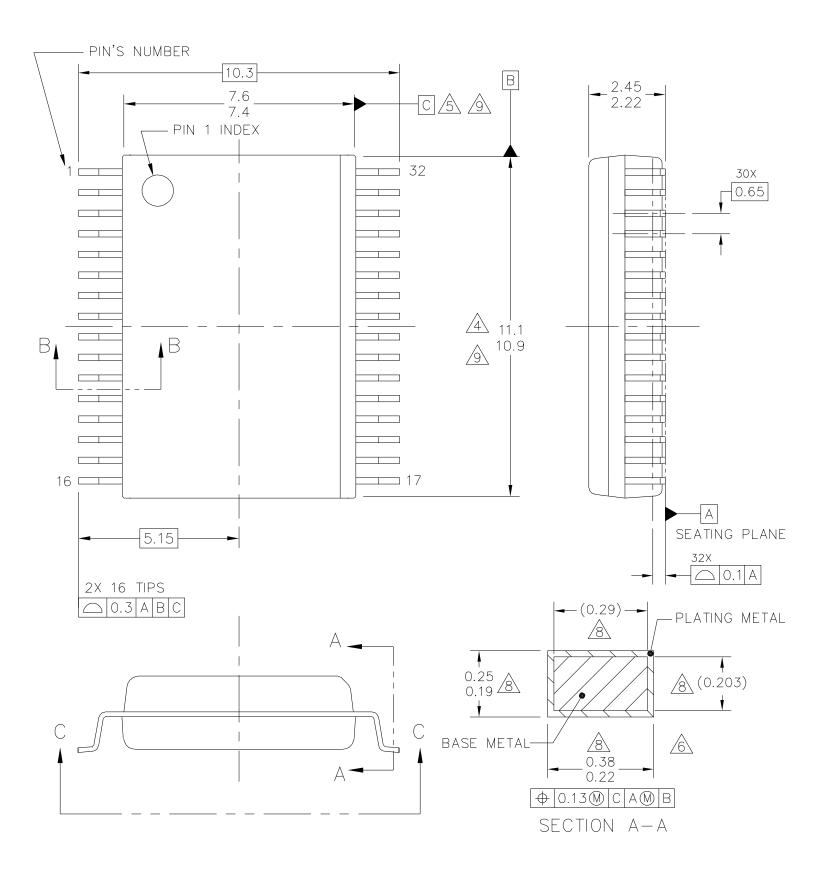
# AEC Q100 Certification of Design, Construction and Qualification Q100base-revG; -001revC, -002revD, -003revE, -004revC, -005recC, -006revD, -007revA, -008revA. -009revB. -010revA. -011revB. -012Rev.

	008revA, -009revB, -010re	evA, -011revB, -012Rev
	Supplier Name: Freescale Semiconductor	Date:
12.	Die Passivation:	
	a. Number of passivation layers:	2
	b. Die passivation material(s):	SiO2/Si3N4
	c. Thickness (es) & tolerances:	2kÅ /7kÅ
13.	Die Overcoat Material (e.g., Polyimide)	Polyimide
14.	Die Cross-Section Photo/Drawing:	Available upon request
15.	Die Prep Backside:	
	a. Die prep method:	None
	b. Die metallization:	None
	c. Thickness(es) & tolerances:	N/A
16.	Die Separation Method (Kerf Depth):	
	a. Kerf width (um):	20 - 100um
	b. Kerf depth (if not 100% saw):	100% Sawn
	c. Saw method:	Dual
17.	Die Attach:	
	a. Die attach material ID:	Sumitomo CRM-1064MBL
	b. Die attach method:	Epoxy
	c. Die placement diagram:	Available upon request
18.	Package:	
	a. Type of package (e.g. plastic, ceramic,	
	unpackaged):	Plastic
	b. Ball/lead count:	32LD SOIC
	c. JEDEC designation (e.g., MS029, MS034,	NON-JEDEC
	d. Lead (Pb) free (<.1% homogenouse material)	Yes
	e. Package outline drawing	See PPAP
19.	Mold Compound:	
	a. Plastic mold compound supplier & ID:	Sumitomo EME-G630AY
	b. Mold compound type:	Epoxy Resin
	c. Flammability rating:	UL 94 V0
	d. Fire Retardant type/composition	Resin system
	e. Tg (glass transition temperature) (°C):	Tg=120C
	c. 1g (glass transition temperature) ( C).	CTE1 (below Tg) = 10 ppm/°C, CTE2 (above
	f. CTE (above & below Tg) (ppm/°C):	Tg) = 40 ppm/ $^{\circ}$ C
20.	Wire Bond:	
	a. Wire bond material:	Cu
	<ul><li>b. Wire bond diameter (mils):</li></ul>	0.033
	c. Type of wire bond at die:	Ball bond
	d. Type of wire bond at leadframe:	Stitch bond
	e. Wire bonding diagram:	Available upon request
21.	Leadframe (if applicable):	
	a. Paddle/flag material:	Cu
	b. Paddle/flag width (mils):	5.1562 mm
	c. Paddle/flag length (mils):	5.1562 mm
	d. Paddle/flag plating composition:	None
	e. Paddle/flag plating thickness (µin):	NA
	f. Leadframe material:	Cu
	g. Leadframe bonding plating composition:	Ag
	h. Leadframe bonding plating thickness (um):	1.78 - 7.62
	i. External lead plating composition:	Sn
	j. External lead plating thickness (um):	7.62 - 17.8
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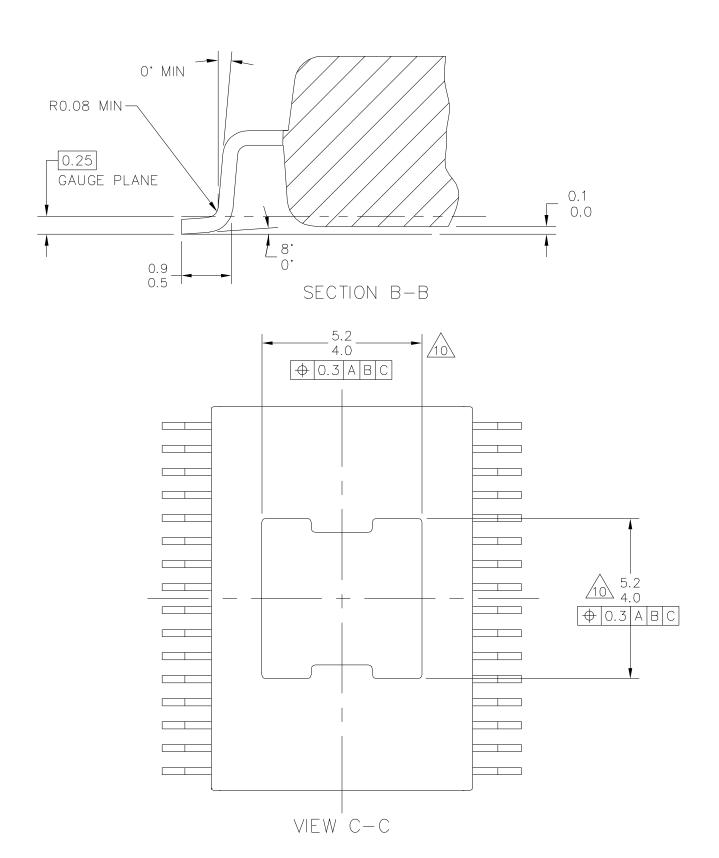


# AEC Q100 Certification of Design, Construction and Qualification Q100base-revG; -001revC, -002revD, -003revE, -004revC, -005recC, -006revD, -007revA, -

	008revA, -009revB, -010revA, -011revB, -012Rev						
	Supplier Name: Freescale Semiconductor	Date:					
22.	Substrate (if applicable):	Not applicable					
	a. Substrate material (e.g., FR5, BT, etc.):						
	b. Substrate thickness (mm):						
	c. Number of substrate metal layers:						
	d. Plating composition of ball solderable surface:						
	e. Panel singulation method:						
	f. Solder ball composition:						
	g: Solder ball diameter (mm):						
23.	Unpackaged Die (if not packaged):	Not Applicable					
	<ul> <li>a. Under Bump Metallurgy (UBM):</li> </ul>						
	b. Thickness of UBM metal:						
	c. Bump composition:						
	d. Bump size:						
	Header material (if applicable):	Not Applicable					
25.	Thermal Resistance:	Leave blank					
	a. ØJA °C/W (approx):	74					
	b. ØJC °C/W (approx):	26					
	c. Special thermal dissipation construction	Not Applicable					
	techniques:	Not Applicable					
	Test circuits, bias levels and operational						
26.	conditions imposed during the supplier's life and	Available upon request					
	environmental tests:						
27.	Fault grade coverage (%):						
28.	Maximum Process Exposure Conditions:	Note: Temperatures are as measured on the center					
	•	of the plastic package body top surface.					
	a. MSL @ rated SnPb temperature:	NA					
	b. MSL @ rated Pb-free temperature:	MSL-3 at 260C					
	c. Maximum dwell time @ maximum process	40					
	temperature:						
	Attachments:	Requirements:					
	Die Photo:	A separate Certification of Design,					
	Available Upon Request	Construction & Qualification must be submitted					
	Package Outline Drawing:	for each part number, wafer fab, and assembly					
	See PPAP	location.					
	Die Cross-Section Photos/Drawing:						
	Available Upon Request	- D   G					
	Wire Bonding Diagram	Design, Construction & Qualification shall be					
	Available Upon Request	compiled by the responsible individual at the					
	Die Placement Diagram	supplier who can verify the above information is					
	See PPAP	accurate and complete.					
	Test Circuits, Bias Levels, & Conditions						
-	Available Upon Request	g 1 1 1 W P 1 100 P 5					
	Completed by and Date:	Completed by:Wang Brenda/ 09-Dec-2013					
<u> </u>	Certified by (electronic signature) and Date:	Completed by: Wang Brenda/ 09-Dec-2013					
	Typed/Printed:						
	Signature:						
	Title:						



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TITLE:		D: 98ASAO0259D	REV: 0			
32LD SOIC W/B, 0.65 PITC 4 6 X 4 6 FXPOSED PAD	I CASE NUMBER	CASE NUMBER: 2150-01				
T.O X T.O EXIOSED I AD		STANDARD: NON-JEDEC				



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TITLE:	5 DITOLI	DOCUMENT NO	REV: 0	
32LD SOIC W/B, 0.6 4.6 X 4.6 FXPOSFI		CASE NUMBER	R: 2150-01	29 JUL 2010
7.0 X 4.0 LXI 03LI		STANDARD: NO	N-JEDEC	

### NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.



THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.



THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.



THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.



EXACT SHAPE OF EACH CORNER IS OPTIONAL.



THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.



THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.



THESE DIMENSION RANGES DEFINE THE PRIMARY PCB KEEP-OUT AREA. MOLD LOCKING AND RESIN BLEED CONTROL FEATURES MAY BE VISIBLE.

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32LD SOIC W/B, 0.6 4.6 X 4.6 FXPOSE		CASE NUMBER	2: 2150-01	29 JUL 2010
4.0 X 4.0 LXI USL	DIAD	STANDARD: NO	N-JEDEC	

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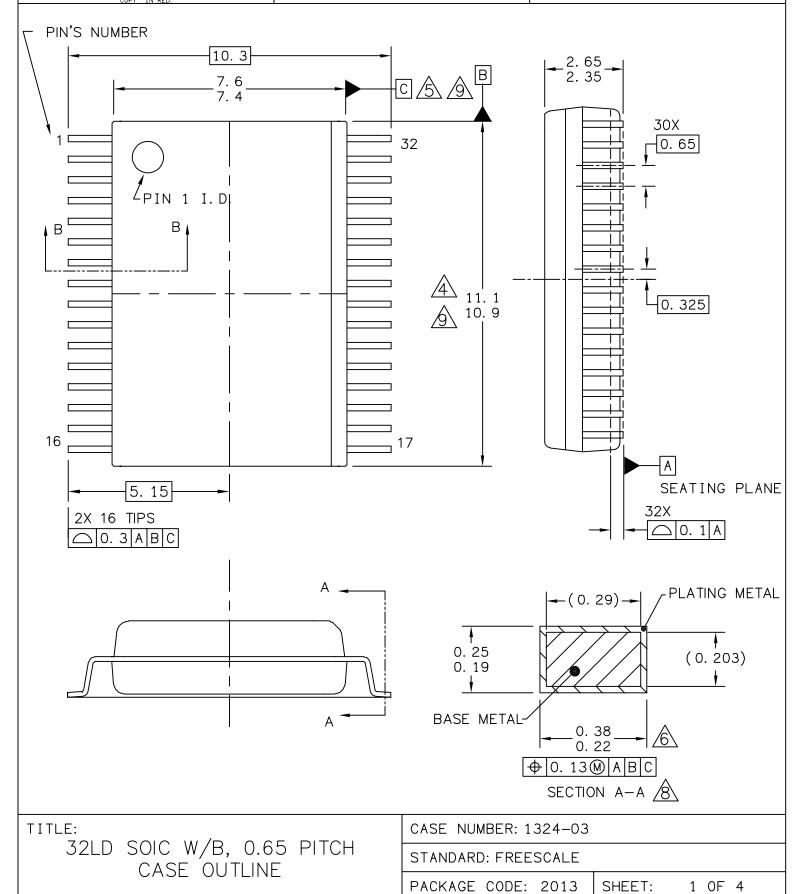
# MECHANICAL OUTLINES DICTIONARY

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PAGE: 1324

REV: B





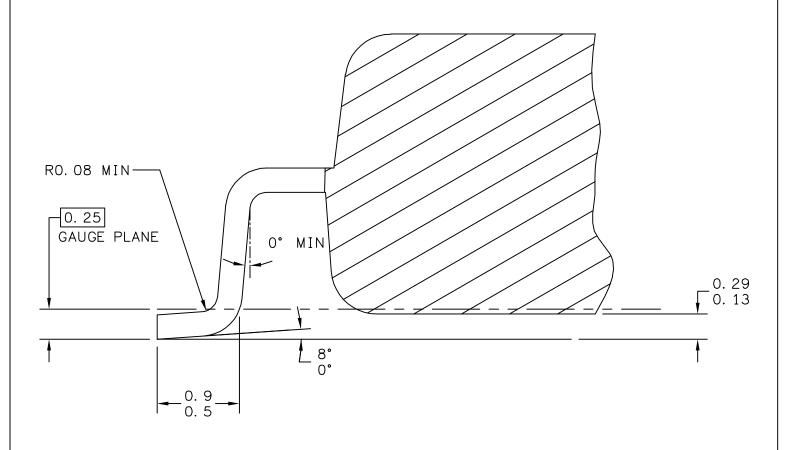
### MECHANICAL OUTLINES **DICTIONARY**

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1324

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SECTION B-B

TITLE:

32LD SOIC W/B, 0.65 PITCH CASE OUTLINE

CASE NUMBER: 1324-03

STANDARD: FREESCALE

PACKAGE CODE: 2013 SHEET: 2 OF 4



# MECHANICAL OUTLINES DICTIONARY

DOCUMENT	NO: 98ARH99137A
PAGE:	1324
 REV.	R

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### NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
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- THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
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- EXACT SHAPE OF EACH CORNER IS OPTIONAL.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER—LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

32LD SOIC W/B, 0.65 PITCH, CASE OUTLINE CASE NUMBER: 1324-03

STANDARD: FREESCALE

PACKAGE CODE: 2013 | SHEET: 3 OF 4



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### REVISION HISTORY

DOCUMENT NO: 98ARH99137A
PAGE: 1324

В

REV:

LTR	ORIGINATOR	REVISIONS	DRAI	FTER		DATE
0	GARY JOHNSON	RELEASED FOR PRODUCTION		CUPID	LEE	02NOV00
A	GARY JOHNSON	UPDATED TO NEW DRAWING FORMAT. CHANGED LEADFRAME THICKNESS FROM 0.152 TO 0.203 MM CHANGED CASE NO. FROM 1324-01 TO 1324-02 CHANGED LEAD WIDTH FROM 0.24 TO 0.29 MM CHANGED STAND-OFF FROM 0.15/0.05 TO 0.29/0.13 ADDED SECTION A-A CHANGED NOTE 2, 3, 4, 5 AND 6 ADDED NOTE 9		CUPID	LEE	28AUG01
В	TAYLOR LIU	UPDATED TO FREESCALE FORMAT. SHO1, ADDED DIMENSION 0.325 SHO1, CHANGED TOLERANCE FROM +0.13@ C A@ B TO +0.13@ A B C  CREATED EXTERNAL CASE OUTLINE.		TAYLO	R LIU	07APR05

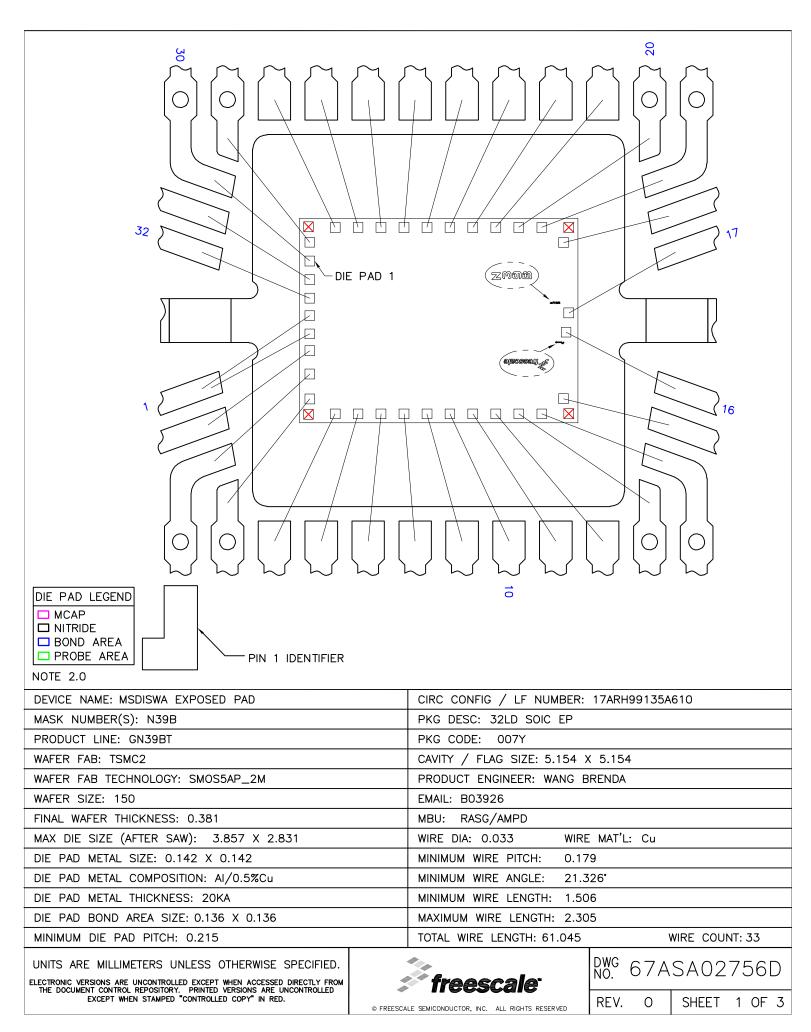
TITLE:

32LD SOIC W/B, 0.65 PITCH, CASE OUTLINE

CASE NUMBER: 1324-03

STANDARD: FREESCALE

PACKAGE CODE: 2013 | SHEET: 4 OF 4



### NOTES:

- 1.0 BONDING ALLOWED ONLY WITHIN DESIGNATED DIE BOND PAD AREAS. AUTO-CENTERING ON DIE PADS THAT HAVE SEPARATE BOND AND PROBE AREAS IS NOT ALLOWED.
- 2.0 ONLY THE DIE NITRIDE LAYER SHOWN. SEE OLP FOR OTHER COLOR CODED LAYERS. NOTE SOME DIE TECHNOLOGIES MAY NOT HAVE BOND AND PROBE LAYERS.
- 3.0 "X" LOCATED ON DIE PADS OR BOND FINGERS INDICATES NON-BONDED LOCATION.
- 4.0 DIE METAL PAD SIZE AND DIE BOND AREA SIZE DIMENSIONS IN THE TABLE ARE THE SMALLEST THAT OCCUR ON THIS DEVICE.
- 5.0 QUALIFICATION TIER: AEC1
- 6.0 ASSEMBLY DESIGN RULE DEVIATIONS:
  - 6.1 DIE TECHNOLOGY SMOS5AP\_2M IS NOT QUALIFIED WITH CU WIRE. DESIGN RULES USED ARE QUALIFIED FOR THIS DESIGN ONLY. DO NOT USE FOR NEW PRODUCT INTRODUCTION (NPI) DESIGNS. MOVED TO PRODUCTION BASED ON CAB# 13120651M

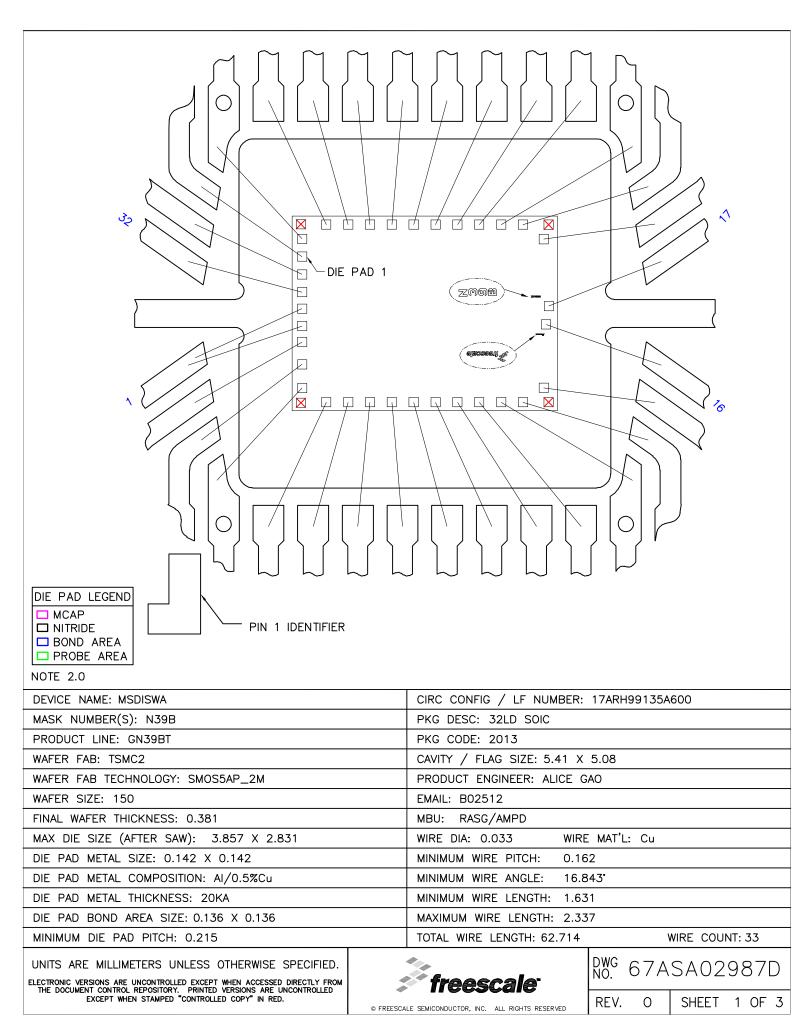




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LTR	ORIGINATOR		REVISIONS		DRAFTER	DATE						
XO	MARIANO CHING	RELEASED (DAR #205	TO ENGINEERING EVALUATION 92)	GIDEON	04 JUN 2013							
0	MARIANO CHING	REVISION IS WITH NO CO BEEN RUNI FOR SEVER VIOLATIONS DESIGN RU NOT CHECK TEAMS HAS CONVERSICE HISTORY. F	FOR PRODUCTION.THIS BONDING DIS FOR CU WIRE DOCUMENTATION OF THANGE TO THE DESIGN. THIS DESIGNING IN HIGH VOLUME MANUFACTURES TO CURRENT FSL DIE AND PACKALES, HOWEVER THE DESIGN RULES OF APPROVED THESE LEGACY PARTINS BASED ON THEIR MANUFACTURES REFERENCED CU BOND DIAGRAM IS 56D_XO. (DAR #21398)	NLY GN HAS RING TAIN AGE WERE PPE T	NS	17 DEC 2013						



### NOTES:

- 1.0 BONDING ALLOWED ONLY WITHIN DESIGNATED DIE BOND PAD AREAS. AUTO-CENTERING ON DIE PADS THAT HAVE SEPARATE BOND AND PROBE AREAS IS NOT ALLOWED.
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  - 6.1 DIE TECHNOLOGY SMOS5AP\_2M IS NOT QUALIFIED WITH CU WIRE. DESIGN RULES USED ARE QUALIFIED FOR THIS DESIGN ONLY. DO NOT USE FOR NEW PRODUCT INTRODUCTION (NPI) DESIGNS. MOVED TO PRODUCTION BASED ON CAB# 13120651M.





# REVISION HISTORY

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LTR	ORIGINATOR		REVISIONS	DRAFTER	DATE						
0	MARIANO CHING	REVISION I WITH NO C BEEN RUNI FOR SEVEF VIOLATIONS DESIGN RU NOT CHECI TEAMS HA' CONVERSION HISTORY. F	FOR PRODUCTION.THIS BONDING DIS FOR CU WIRE DOCUMENTATION OF THANGE TO THE DESIGN. THIS DESIGNING IN HIGH VOLUME MANUFACTURED YEARS. THIS DESIGN MAY CONSTRUCTOR OF THE PROPURE AND PACKALES, HOWEVER THE DESIGN RULES OF THE PROPURE APPROVED THESE LEGACY PARTICLES BASED ON THEIR MANUFACTURES REFERENCED AU BOND DIAGRAM IS TOD_O. (DAR #21200)	NLY GN HAS RING TAIN AGE WERE PPE T	GIDEON	03 OCT 2013					

# Customer Engineering Approval

# **Design FMEA**

### POTENTIAL FAILURE MODE AND EFFECTS ANLAYSIS (Design FMEA)

System Subsystem			Control Number / Issue: 83AS	SA10126D/O
✓ Component:	MSDI	Erik Thompson  Prepared By: RS585 (480) 413-8408	FMEA Date (Orig.) :	10/15/01
		Motorola SPS, TSPG,		
	Compar	y, Group, Site/Business Unit: APD	(Rev.) :	11/11/02
Core Tean	: Frik Thompson (Design) Robe	ert Divon (Design) Peter Bills (Applications) Tiffany Le (Product)		

		1											ACTIO	N RE	SUL.	TS	
L i n e	Item Pin	POTENTIAL FAILURE MODE	POTENTIAL EFFECT(S) OF FAILURE	S E V	C L A S	POTENTIAL CAUSE(S)/ MECHANISIM(S) OF FAILURE	C U R		D E T E C	R P N	RECOMMENDED ACTION(S)	RESPONSIBILITY & TARGET COMPLETION DATE	ACTION TAKEN	E	c	E	R P N
1	Pin 1 / GND	Open	Drive MCU I/O to VPWR	8		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	8	None						
2		Short Ground	N/A														
3		Short Vdd	AMUX non-functional, SPI non- functional	- 5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None					T	
4		Short Vpwr	IC non-functional	8		IC Metalization/process	1	Testing at probe and again at assembly site	1	8	None						
5		Short to Pin 2 SI	SPI non-functional	5		IC Metalization/process short, Bond wire short	1	Testing at probe and again at assembly site	1	5	None						
6	Pin 2 / SI	Open	SPI non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
7		Short Ground	SPI non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
8		Short Vdd	SPI non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
9		Short Vpwr	Permanent Damage to IC	8		IC Metalization/process short	1	Testing at probe and again at assembly site	1	8	None					T	
10		Short to Pin 3 SCLK	SPI non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None					T	
11	Pin 3 / SCLK	Open	SPI non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None					T	
12		Short Ground	SPI non-functional	5		IC Metalization/process	1	Testing at probe and again at assembly site	1	5	None					T	
13		Short Vdd	SPI non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None					T	
14		Short Vpwr	Permanent Damage to IC	8		IC Metalization/process short	1	Testing at probe and again at assembly site	1	8	None					T	
15		Short to Pin 4 CSB	SPI non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None					T	
16	Pin 4 / CSB	Open	SPI non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None					T	
17		Short Ground	SO in unknown state, SPI non- functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None					T	
18		Short Vdd	SPI non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None			$\Box$	$\top$	$\top$	
19		Short Vpwr	Permanent Damage to IC	8		IC Metalization/process short	1	Testing at probe and again at assembly site	1	8	None				$\top$	$\top$	
20		Short to Pin 5 SP0	SPI non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None			П	$\top$	$\top$	
21	Pin 5 / SP0	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None			П	$\top$	$\top$	

### POTENTIAL FAILURE MODE AND EFFECTS ANLAYSIS (Design FMEA)

System Subsystem			Control Number / Issue: 83A	SA10126D/O
✓ Component:	MSDI	Erik Thompson	FMFA Data (Origin)	10/15/01
	MSDI	Prepared By: RS585 (480) 413-8408  Motorola SPS, TSPG.	FMEA Date (Orig.) :	10/15/01
		Company, Group, Site/Business Unit: APD	(Rev.) :	11/11/02
Core Tean	n: Erik Thompson /	(Dosign) Pobort Divon (Dosign) Potor Bills (Applications) Tiffany Lo (Product)		

													ACTIO	N RE	SUL	.TS	
L i n	Item Pin	POTENTIAL FAILURE MODE	POTENTIAL EFFECT(S) OF FAILURE	S E V	C L A S	MECHANISIM(S) OF FAILURE	O C C U R		D E T E C	R P N	RECOMMENDED ACTION(S)	RESPONSIBILITY & TARGET COMPLETION DATE	ACTION TAKEN	S E V	С	D E T	R P N
22		Short Ground	SP0 non-functional	5	ľ	IC Metalization/process	1	Testing at probe and again at	1	5	None			П	$\neg$	$\exists$	$\neg$
						short		assembly site									
23		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
24		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
25		Short to Pin 6 SP1	SP0 and SP1 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None					T	$\Box$
26	Pin 6 / SP1	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
27		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
28		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
29		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
30		Short to Pin 7 SP2	SP1 and SP2 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None					T	
31	Pin 7 / SP2	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None					$\Box$	
32		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
33		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
34		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
35		Short to Pin 8 SP3	SP2 and SP3 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
36	Pin 8 / SP3	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
37		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
38		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
39		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None					$\top$	
40		Short to Pin 9 SG0	SP3 and SG0 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						

System				
Subsystem			Control Number / Issue: 83A	SA10126D/O
		Erik Thompson		
✓ Component:	MSDI	Prepared By: RS585 (480) 413-8408	FMEA Date (Orig.) :	10/15/01
		Motorola SPS, TSPG,		
		Company, Group, Site/Business Unit: APD	(Rev.) :	11/11/02
Core Tear	m: Frik Thompson (I	Design) Robert Dixon (Design) Peter Bills (Applications) Tiffany Le (Product)		

													ACTIO	N RE	SUL	.TS	
L i n e	Item Pin	POTENTIAL FAILURE MODE	POTENTIAL EFFECT(S) OF FAILURE	S E V	C L A S	POTENTIAL CAUSE(S)/ MECHANISIM(S) OF FAILURE	O C C U R		D E T E C	R P N	RECOMMENDED ACTION(S)	RESPONSIBILITY & TARGET COMPLETION DATE	ACTION TAKEN	S E V	С	D E T	R P N
41	Pin 9 / SG0	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None					$\top$	
42		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None					T	
43		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None					T	$\exists$
44		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None					1	
45		Short to Pin 10 SG1	SG0 and SG1 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None					T	
46	Pin 10 / SG1	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
47		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
48		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1		None						
49		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
50		Short to Pin 11 SG2	SG1 and SG2 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None					$\top$	$\Box$
51	Pin 11 / SG2	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
52		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
53		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
54		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
55		Short to Pin 12 SG3	SG2 and SG3 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None					T	
56	Pin 12 / SG3	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
57		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
58		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
59		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						

System Subsystem			Control Number / Issue: 83A	SA10126D/O
✓ Component:	MSDI	Erik Thompson Prepared By: RS585 (480) 413-8408	FMEA Date (Orig.) :	10/15/01
		Motorola SPS, TSPG,		
		Company, Group, Site/Business Unit: APD	(Rev.) :	11/11/02
Core Tean	n: Frik Thompson (D	esign) Robert Divon (Design) Peter Rills (Applications) Tiffany Le (Product)	<del></del>	

		1											ACTIO	N RE	SULT	rs	
L i n e	Item Pin	POTENTIAL FAILURE MODE	POTENTIAL EFFECT(S) OF FAILURE	S E V	C L A S	POTENTIAL CAUSE(S)/ MECHANISIM(S) OF FAILURE	0 C C U R	CURRENT PROCESS CONTROLS	D E T E C	R P N	RECOMMENDED ACTION(S)	RESPONSIBILITY & TARGET COMPLETION DATE	ACTION TAKEN	E		E   1	R P N
60		Short to Pin 13 SG4	SG3 and SG4 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None				T	T	٦
61	Pin 13 / SG4	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None				T	T	
62		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None				T	T	
63		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None				T	T	
64		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
65		Short to Pin 14 SG5	SG4 and SG5 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
66	Pin 14 / SG5	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
67		Short Ground	SP0 non-functional	5		IC Metalization/process short		Testing at probe and again at assembly site	1	5	None				$\perp$		
68		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None					$\perp$	
69		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
70		Short to Pin 15 SG6	SG5 and SG6 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None				T	Τ	
71	Pin 15 / SG6	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None				I	$\Box$	
72		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
73		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
74		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1		None						
75		Short to Pin 16 VPWR	SG6 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None				$\perp$	$\perp$	
	Pin 16 / VPWR	Open	IC non-functional, remains in reset	8		Open bond wire, metal migration		Testing at probe and again at assembly site	1	8	None				$\perp$	$\perp$	
77		Short Ground	AMUX non-functional, SPI non- functional	5		IC Metalization/process short		Testing at probe and again at assembly site	1	5	None				$\perp$	$\perp$	
78		Short Vdd	Permanent Damage to IC	8		IC Metalization/process short	1	Testing at probe and again at assembly site	1	8	None						

System Subsystem			Control Number / Issue: 83A	SA10126D/O
Component:	MSDI	Erik Thompson  Prepared By: RS585 (480) 413-8408	FMEA Date (Orig.) :	10/15/01
Core Tean	n: Frik Thompson	Motorola SPS, TSPG,  Company, Group, Site/Business Unit: APD  (Design) Robert Dixon (Design) Peter Bills (Applications). Tiffany Le (Product)	(Rev.) :	11/11/02

		1							П				ACTIO	N RE	SUL	TS	
L i n	Item Pin	POTENTIAL FAILURE MODE Function	POTENTIAL EFFECT(S) OF FAILURE	S E V	C L A S	POTENTIAL CAUSE(S)/ MECHANISIM(S) OF FAILURE	O C C U R	CURRENT PROCESS CONTROLS	D E T E C	R P N	RECOMMENDED ACTION(S)	RESPONSIBILITY & TARGET COMPLETION DATE	ACTION TAKEN		0 C C	E	R P N
79		Short Vpwr	N/A														
80		Short to Pin 17 WAKEB	Permanent Damage to WAKEB pin	8		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	8	None					T	
81	Pin 17 / WAKEB	Open	WAKEB non-functional	5		Open bond wire, metal migration		Testing at probe and again at assembly site	1	5	None						
82		Short Ground	WAKEB non-functional	5		IC Metalization/process short		Testing at probe and again at assembly site	1	5	None						
83		Short Vdd	WAKEB non-functional	5		IC Metalization/process short		Testing at probe and again at assembly site	1	5	None						
84		Short Vpwr	Permanent Damage to WAKEB pin	8		IC Metalization/process short		Testing at probe and again at assembly site	1	8	None						
85		Short to Pin 18 SG13	WAKEB and SG13 non- functional	5		Solder short, Bond wire short, short PCB trace		Testing at probe and again at assembly site	1	5	None						
86	Pin 18 / SG13	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
87		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
88		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
89		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
90		Short to Pin 19 SG12	SG13 and SG12 non- functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
91	Pin 19 / SG12	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
92		Short Ground	SP0 non-functional	5		IC Metalization/process short		Testing at probe and again at assembly site	1	5	None						
93		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
94		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
95		Short to Pin 20 SG11	SG12 and SG11 non- functional	5		Solder short, Bond wire short, short PCB trace		Testing at probe and again at assembly site	1	5	None						
96	Pin 20 / SG11	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
97		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
98		Short Vdd	SP0 non-functional	5		IC Metalization/process short		Testing at probe and again at assembly site	1	5	None					T	

System Subsystem		, · · · · · · · · · · · · · · · · · · ·	Control Number / Issue: 83AS	SA10126D/O
✓ Component:	MSDI	Erik Thompson Prepared By: RS585 (480) 413-8408	FMEA Date (Orig.) :	10/15/01
		Motorola SPS, TSPG,		
	Compa	ny, Group, Site/Business Unit: APD	(Rev.) :	11/11/02
Core Tean	: Frik Thompson (Design) Robe	ert Dixon (Design), Peter Rills (Applications), Tiffany Le (Product)		

		1											ACTIO	N RES	SULT	rs
L i n	Item Pin	POTENTIAL FAILURE MODE Function	POTENTIAL EFFECT(S) OF FAILURE	S E V	CLASS	POTENTIAL CAUSE(S)/ MECHANISIM(S) OF FAILURE	O C C U R		D E T E C	R P N	RECOMMENDED ACTION(S)	RESPONSIBILITY & TARGET COMPLETION DATE	ACTION TAKEN	E		D R E P T N
99		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None					
100		Short to Pin 21 SG10	SG11 and SG10 non- functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None					
101	Pin 21 / SG10	Open	SP0 non-functional	5	$\overline{}$	Open bond wire, metal	1	Testing at probe and again at	1	5	None			$\vdash$	+	+
	217 0010	Opon		Ü		migration	١.	assembly site	'		110110					
102		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None				T	
103		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None				T	
104		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None				1	
105		Short to Pin 22 SG9	SG10 and SG9 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None				T	
106	Pin 22 / SG9	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None				T	
107		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None				T	
108		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None				T	
109		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None					$\top$
110		Short to Pin 23 SG8	SG9 and SG8 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None				T	
111	Pin 23 / SG8	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None				T	
112		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None					
113		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None				1	
114		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None					
115		Short to Pin 24 SG7	SG8 and SG7 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None					
116	Pin 24 / SG7	Open	SP0 non-functional	5		Open bond wire, metal migration		Testing at probe and again at assembly site	1	5	None					
117		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None					

System Subsystem			Control Number / Issue: 83A	SA10126D/O
✓ Component:	MSDI	Erik Thompson Prepared By: RS585 (480) 413-8408	FMEA Date (Orig.) :	10/15/01
		Motorola SPS, TSPG,		
		Company, Group, Site/Business Unit: APD	(Rev.) :	11/11/02
Core Tean	n: Frik Thompson (D	esign) Robert Divon (Design) Peter Rills (Applications) Tiffany Le (Product)	<del></del>	

													ACTIO	N RE	SUL	TS	
L i n	Item Pin	POTENTIAL FAILURE MODE Function	POTENTIAL EFFECT(S) OF FAILURE	S E V	C L A S	MECHANISIM(S) OF FAILURE	0 C C U R		D E T E C	R P N	RECOMMENDED ACTION(S)	RESPONSIBILITY & TARGET COMPLETION DATE	ACTION TAKEN	E		E	R P N
118		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None			П	T	Т	٦
119		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None					1	
120		Short to Pin 25 SP4	SG7 and SP4 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None					$\top$	٦
121	Pin 25 / SP4	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None					T	$\exists$
122		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None					T	П
123		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None					T	
124		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
125		Short to Pin 26 SP5	SP4 and SP5 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None					$\top$	$\exists$
126	Pin 26 / SP5	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None					T	П
127		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None					T	
128		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None					T	
129		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
130		Short to Pin 27 SP6	SP5 and SP6 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None					$\top$	٦
131	Pin 27 / SP6	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None					T	$\Box$
132		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None					T	
133		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None			П		T	$\neg$
134		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
135		Short to Pin 28 SP7	SP6 and SP7 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None					$\top$	
136	Pin 28 / SP7	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None					T	$\exists$

System Subsystem		Control Number / Issue: 83ASA10126D/O
✓ Component:	Erik Thompson  MSDI	FMEA Date (Orig.) : 10/15/01
Core Teen	Motorola SPS, TSPG,  Company, Group, Site/Business Unit: APD  Frilk Thompson (Design), Robert Diver (Design), Robert Pills (Applications), Tiffony Lo (Product)	(Rev.):11/11/02

													ACTIO	N RE	SUL	TS	
L i n	Item Pin	POTENTIAL FAILURE MODE	POTENTIAL EFFECT(S) OF FAILURE	S E V	C L A S	MECHANISIM(S) OF FAILURE	0 C C U R		D E T E C	R P N	RECOMMENDED ACTION(S)	RESPONSIBILITY & TARGET COMPLETION DATE	ACTION TAKEN		c		R P N
137		Short Ground	SP0 non-functional	5		IC Metalization/process	1	Testing at probe and again at assembly site	1	5	None			П	Т	T	$\neg$
138		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None					T	
139		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
140		Short to Pin 29 INTB	INTB and SP7 clamped to pad zener (~10V)	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None					T	$\neg$
141	Pin 29 / INTB	Open	INTB non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
142		Short Ground	INTB non-functional, excessive current in VDD	5		IC Metalization/process short		Testing at probe and again at assembly site	1	5	None						
143		Short Vdd	INTB non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
144		Short Vpwr	Permanent Damage to IC	8		IC Metalization/process short	1	Testing at probe and again at assembly site	1	8	None					$\perp$	
145		Short to Pin 30 AMUX	INTB non-functional, AMUX non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None					$\perp$	
"	Pin 30 / AMUX	Open	AMUX non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None					$\perp$	
147		Short Ground	AMUX non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1		None					$\perp$	
148		Short Vdd	AMUX non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None					$\perp$	
149		Short Vpwr	Possible IC damage, excessive voltage on VDD	8		IC Metalization/process short		Testing at probe and again at assembly site	1	8	None			Ш		$\perp$	
150		Short to Pin 31 VDD	AMUX non-functional	5		Solder short, Bond wire short, short PCB trace		Testing at probe and again at assembly site	1	5	None					$\downarrow$	_
	Pin 31 / VDD	Open	AMUX non-functional, SPI non-functional			Open bond wire, metal migration		Testing at probe and again at assembly site	1	5	None					$\downarrow$	_
152		Short Ground	Permanent damage to IC, excessive current in VDD	8		IC Metalization/process short	1	Testing at probe and again at assembly site	1	8	None					$\downarrow$	_
153		Short Vdd	N/A					-			N				_	$\perp$	$\Box$
154		Short Vpwr	Permanent damage to IC	8		IC Metalization/process short		Testing at probe and again at assembly site	1	8	None					$\perp$	$\Box$
155		Short to Pin 32 SO	SPI non-functional, excessive current in VDD	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None				_	$\perp$	
	Pin 32 / SO	Open	SPI non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1		None				_	$\perp$	$\perp$
157		Short Ground	SPI non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None					$\perp$	

System Subsystem		Control Number / Issue: 83ASA10126D/O	
✓ Component:	Erik Thompson  MSDI	FMEA Date (Orig.) :10/15/01	
Core Team:	Company, Group, Site/Business Unit: APD  Erik Thompson (Design), Robert Dixon (Design), Peter Bills (Applications), Tiffany Le (Product)	(Rev.):11/11/02	

													ACTIO	N RE	SUL	TS	
ı,	Item Pin	POTENTIAL	POTENTIAL EFFECT(S) OF		С		0	CURRENT PROCESS CONTROLS	D		RECOMMENDED	RESPONSIBILITY &	ACTION			$\blacksquare$	
7	item i iii	FAILURE MODE	FAILURE	S	L	MECHANISIM(S) OF FAILURE	С		E	R	ACTION(S)	TARGET	TAKEN	S		D	
'		Function		Е	Α		С		T	Р		COMPLETION DATE		Е			Р
l n		runction		٧	S		U		E	N				٧	c	т	N
e					S		R		C						_	4	
15	3	Short Vdd	SPI non-functional	5		IC Metalization/process	1	Testing at probe and again at	1	5	None						
						short		assembly site									
15	9	Short Vpwr	Permanent damage to IC	8		IC Metalization/process	1	Testing at probe and again at	1	8	None						
			_			short		assembly site									
16		Short to Pin 1	SPI non-functional	5		Solder short, Bond wire	1	Testing at probe and again at	1	5	None				П	Т	П
		GND				short, short PCB trace		assembly site									
16	1															$\Box$	

# **Process Flow Diagrams**

High Level Flow

(Detailed Process Flow Diagrams are part of the Freescale Control Plans, if applicable to this PPAP)



#### HIGH LEVEL FLOW CHART

Customer Part Number:	Various	Date:	12 December, 2013
Part Name:	MSDISWA	Freescale Part Number:	MC33972ATEK(R2)/ MC33972ATEW(R2)

Process	Location	City, State or Country
Design	FSL-AMPD	Tempe,Arizona,USA
Wafer Fab	TSMC2 FAB	Hsinchu, Taiwan
Assembly	FSL-TJN-FM	Tianjin, China
Burn-in	NA	NA
Final Test	FSL-TJN-FM	Tianjin, China
Tape & Reel	FSL-TJN-FM	Tianjin, China
Final Inspection	FSL-TJN-FM	Tianjin, China
Any Subcontractor Process	TSMC2 FAB	Hsinchu, Taiwan
PDC (Product Distribution Center)	Various	Various
Customer Ship-to Locations	Various	Various

Note: This is a sequential listing of the major process steps, including all subcontractor processes and may include any alternate sites which are used for processing. There may be multiple sites listed for the various process steps.

# **Process FMEA**

# **TSMC PPAP Documents**

- TSMC PPAP documents (FMEAs, Control Plans, Cpks, and GR&R) are considered proprietary information by TSMC, classified as "TSMC INTERNAL USE ONLY" and cannot be distributed with Freescale PPAPs in accordance with an agreement with TSMC.
- The PPAP documents are pulled by Freescale External Manufacturing Quality and checked for compliance with TS16949 requirements.
- For special requests, Freescale may be able to review these documents on a limited basis with customers at the local Freescale sales office.
- If there are any questions, please contact:

Sally Cadena Massey, Freescale MSG NPI Reliability, 512-895-7310 sally.cadena.massey@freescale.com

Jeff Martsching, Freescale External Manufacturing, 512-996-4282 <u>Jeff.Martsching@freescale.com</u>



Item:	SOIC16/28/32/54	4ld							(	Contr	ol Number/Issue:	83MCT00002A/B	Y				
Type:	Design	_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FM	1				
Prepared By:	Amanda Wang										FMEA Date:	05-Oct-94	(Orig.)				
		I.J. Liu,Ivory Guo	o,JU	N YI	ING ZHENG,XIA	\OI	HUI KANG,SHUAI	N YAO,Cyndi Hu,Grayson	Ch	en,L	ANPING BAI,JIN	14-Nov-13	(Rev.)				
•		-						•									
													Action R	esu	lts		_
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/ Process	D	R	Recommended	Responsibility &	Actions Taken &		0	nΤ	R
Function/	Mode	Effect(s) of	E	1	Cause(s)/	C	Process Controls	Controls Detection	E		Action(s)	Target	Effective Date	E		E	
	Mode	Failure	V					Controls Detection	T		Action(s)			V	C		
Requirements		ranure	v	a	Mechanism(s)	C	Prevention		1	IN		Completion Date		V		1	IN
				S	of Failue												
				S													
1. Wafer Mount	wafer broken	Yield lost.(6)	6			2	Quarterly PM	Machine auto alarm (2)	2	24	None						
					table problem												
					(wrong clamp												
			6		gan) Roller pressure	1	Quarterlly PM	Machine auto alarm(2)	2.	12	None				-	+	
			O		Roller pressure	1	Quarterny 1 W	Macinic auto alami(2)	_	12	None						
			6		Higher/uneven	1	Quarterly PM	Machine auto alarm(2)	2	12	None					1	
					attachment table		,	( )									
			6		Improper vacuum	1	Check per	Machine auto alarm(2)	2	12	None						
					pressure		TCM/device change										
																_	
		dicing saw	4		Wafer mount	2	Use wafer	25 points detection for the	2	16	None						
		failure(4)			wrong orientation		orientation system	first piece of wafer by lot (4)									
							with bar code scan.	Mount orientation auto									
								check (2)									
	bubble	die fly-off(5)	8		Contaminated	1		Check every piece of wafer	4	32	None					<b>-</b>	
		die			Mylar			by lot(4)									
		chipping&crack(5			•												
		)															
		electrical															
2 11/1 6	G. 1 1 C	failure(8)	0		, DI .	_	CI 1 TCD ( 1 '01	05 1 1 1 1 6 1	_	<i>C</i> 1	N.T.					4	
		electrical failure	8		Improper DI water	2	Check TCM shiftly	25 points detection for the	4	64	None						
UV	topside	due to corrosion			pressure during			first piece of wafer by lot(4)									
		or weak bond(8) Reliability failure			saw												
		due to corrosion															
		or weak bond(8)															
		NSOP in WB															
		11301 III WD															
			8		Improper cleaning	2	Check TCM shiftly.	25 points detection for the	4	64	None						
					parameter		Quarterly PM.	first piece of wafer by lot(4)	1								
							Implement two-fluid										
							nozzle clean.		1		1						

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI.	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)

													Action I				
Process	Potential Failure		S		Potential	О	Current Design/	Current Design/ Process	D		Recommended	Responsibility &			O		
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е	P	Action(s)	Target	Effective Date			E	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
				s	of Failue												ı
				s													ı
			8		Foreign matter	2	Implement a cover	25 points detection for the	4	64	None						_
							on the top of wafer	first piece of wafer by lot(4)									ı
	1					_	cassette.	25	ļ.,								_
	die scratch	electrical	8		blade breakage	2	Check BBD sensor	25 points detection for the	4	64	None						ı
		failure.(8) Reliability					BBD sensor auto	first piece of wafer by lot(4)									ı
		failure(8)					alarm.										ı
		ranure(o)					alaim.										ı
			8		blade worn out.	1	Check and control	Machine auto alarm(2)	2	16	None						1
							remained exposure										ı
							length per TCM.										ı
							Blade wore out auto										ı
			8		die fly-off	2	Check cutting table	25 points detection for the	4	64	None						_
					,		surface condition	first piece of wafer by lot(4)									ı
							during yearly PM.										ı
							Visual check bubble										ı
							after mount.										ı
																	ı
			8		BBD sensor fail	1	Check and clean	25 points detection for the	4	32	None						
					to detect blade		BBD sensor	first piece of wafer by lot(4)									ı
					broken/chipping		sensitivity per TCM.										ı
							Quarterly PM to										ı
							maintain BBD.										ı
			8		Mishandling	2	Operator follow WI	25 points detection for the	4	64	None						_
					operation during			first piece of wafer by lot(4)									ı
					wafer inspection			Sample PBI (4)									ı
	die chipping	electrical	8		uneven wheel	2.	yearly PM.	25 points detection for the	4	64	None			$\vdash$	_		—
		failure.(8)			mount	ľ	dressing if	first piece of wafer by lot	ľ	0 1							ı
		Reliability					unevenness found	and auto check every 1~30									ı
		failure(8)					during blade	lines (4)									ı
							exchange										

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)
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								-					Action R				
Process	Potential Failure	Potential	S	C	Potential	О	C	Current Design/ Process	D	R	Recommended	Responsibility &	Actions Taken &	S	O		
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е	P	Action(s)	Target	Effective Date			E	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
				s	of Failue												ĺ
				s													İ
			8		improper	1	set checking item in	25 points detection for the	4	32	None						Г
					installation of saw		yearly PM plan.	first piece of wafer by lot									İ
					blade due to		check blade shaft	and auto check every 1~30									İ
					contamination on		before installation	lines (4)									İ
					shaft.		and dressing if										ĺ
							contamination is										İ
			8		spindle speed out	1	control spindle	25 points detection for the	4	32	None						Г
					of control.		speed within +/- 5%	first piece of wafer by lot									ĺ
							rpm during yearly	and auto check every 1~30									ĺ
							PM. Check spindle	lines (4)									ĺ
							speed per TCM.										ĺ
			8		improper blade	1	check blade setup	25 points detection for the	4	32	None						T
					setup sensitivity.		sensitivity voltage at	first piece of wafer by lot									ĺ
							pcb during yearly	and auto check every 1~30									ĺ
			0		T .		PM	lines (4)	4	22	27						
			8		Incorrect saw	1	Check blade label before installation	Visual check before saw(4)	4	32	None						İ
			8		blade type BBD sensor fail	2.	Check and clean	25 points detection for the	4	64	None						Н
					to detect blade	Ĩ	BBD sensor	first piece of wafer by lot			Tione						ĺ
					broken/chipping		sensitivity per TCM.	and auto check every 1~30									ĺ
					11 6		Quarterly PM to	lines (4)									İ
							maintain BBD.	, ,									İ
			8		Adjust parameters	2	Check per TCM.	25 points detection for the	1	64	None						H
			0		in saw recipe and	2	Lock saw recipe.	first piece of wafer of every	4	04	None						İ
					machine		Lock saw recipe.	lot and auto check every									İ
					improperly.			1~30 lines(4)									ĺ
								. ,							_		L
			8		ZZ Reil elleek	2	Lock saw recipe.	25 points detection for the	4	64	None						ĺ
					caused partical			first piece of wafer of every									ĺ
					attach to Z2 blade.			lot and auto check every									ĺ
			1	I				1~30 lines(4)	I	l							1

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)
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													Action F				
Process	Potential Failure	Potential	S	С	Potential	O	Current Design/	Current Design/ Process	D	R	Recommended	Responsibility &	Actions Taken &	S	O	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е	P	Action(s)	Target	Effective Date	Ε	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	С	Prevention		Т	N		Completion Date		V	C	Т	N
•				s	of Failue							•					
				s													
			8		Un-optimized saw	2	SEM inspection to	25 points detection for the	4	64	None					Н	$\overline{}$
					blade for solid		check the saw blade	first piece of wafer of every									1
					metal design in		status during new	lot and auto check every									1
					saw street		saw blade	1~30 lines(4)									1
							qualification.										
	mis-cutting	electrical	8		improper hairline	1	Check hairline	Visual sample check during	4	32	None					Н	$\vdash$
	mis-cutting	failure.(8)	0		alignment after	1	alignment on	saw(5)	4	32	None						
		Tallule.(6)			blade change.		dummy mylar after	Machine auto check after									
					olade change.		saw blade change.	piece start(4)									1
							saw blade change.	Machine auto check every									
								1~30 lines(4)									
			8		Theta Axis DDM	2	Change cable during	Visual sample check during	5	80	None						
					encoder cable fail		yearly PM	saw(5)									1
	Incomplete Cut	Yield loss (6)	6		Improper dicing	1	Set up per TCM.	Visual sample check during	4	24	None					Н	
		(0)	ľ		parameter or		The second	saw(5)		-							1
					cutting mode			Machine auto check after									
								piece start(4)									
								Machine auto check every									
								1~30 lines(4)	<u> </u>							Ш	<u> </u>
			6		Uneven chuck	1	Check chuck table	Visual sample check during	4	24	None						
					table.		surface condition	saw(5)									
							during yearly PM.	Machine auto check after									1
							Clean the chuck	piece start(4)									1
							table per setup	Machine auto check every									
			6		Improper blade	1	Check NCS	Sample check during saw(5)	4	24	None						
					setup sensitivity		sensitivity when	Machine auto check after									l
							machine setup.	piece start(4)									l
							Control set up	Machine auto check every									l
							interval below	1~30 lines(4)									l
							1x/120 feet per										l
							catur chacklist			<u> </u>						ш	4

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)
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													Action F				
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/ Process	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/ Requirements	Mode	Effect(s) of Failure	E V	l a s	Cause(s)/ Mechanism(s) of Failue	C C	Process Controls Prevention	Controls Detection	E T	P N	Action(s)	Target Completion Date	Effective Date	E V			P N
		Scrap on D/B for Mylar torn out/pick up failure(6)	6	5	Improper dicing parameter or cutting mode	1	Set up per TCM.	Visual sample check during saw(5) Machine auto check after piece start(4) Machine auto check every	4	24	None						
			6		Improper blade setup sensitivity	1	Check NCS sensitivity when machine setup. Control set up interval below 1x/120 feet per	Visual sample check during saw(5) Machine auto check after piece start(4) Machine auto check every 1~30 lines(4)	4		None						
		Assembly yield loss (6)	6		Incompleted UV	1	Check TCM regularly	DB process (2)	2	12	None						
	·	electrical failure.(8) Wire bond alignment error(4) Reliability failure(8)	8		Incomplete UV	2	Check TCM regularly	Visual sample check during DB(5) Post bond inpsection & auto alarm during DB process(2)	2	32	None						
3. Die bond & Epoxy cure	die	Electrical failure.(8) Reliability failure.(8)	8		wrong ejector pin number, pattern, coplanarity, position & tip radius.	2	Select ejector pin number&pattern per B/D, calibrate ejector pin position at center of die when device	Check the eject pin mark on backside of dummy die (4)	4	64	None						
			8		improper ejector pin height.	2	Adjust eject pin height in the range 0.5~1.2mm per TCM.	Check the eject pin mark on backside of dummy die(4) PM system auto monitor eject pin height and auto alarm if out of control(3)	3	48	None						

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XL	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)
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													Action F	Resu	lts		
Process	Potential Failure	Potential	S	С	Potential	0	Current Design/	Current Design/ Process	D	R	Recommended	Responsibility &				D	R
Function/ Requirements	Mode Mode	Effect(s) of Failure	E V	l a s	Cause(s)/ Mechanism(s) of Failue	C C	Process Controls	Controls Detection	E T		Action(s)	Target Completion Date	Effective Date	E V	C	Е	P N
			8		poor epoxy coverage	3	Check epoxy coverage per TCM during DB	Visual sample check during DB(5) OBC/ODC auto alarm(2)	2	48	None						
			8		Incorrect pick up parameters	1	Set up per TCM	Check the pin mark on backside of dummy die(4)	4	32	None						
	epoxy on die	electrical failure(8)	8		die drop.	2	check vacuum efficiency when device change	Auto alarm by die drop sensor(2) Visual sample check during DB(5) Trial run on the first strip		32	None						
			8		rubber tip was contaminated	2	divide epoxy pump adjustment work and rubber tip installation work to 2 different person. Operator has no chance to touch the epoxy directly.	Visual sample check during DB(5)	5	80	None						
			8		rubber tip was contaminated by clean paper	2	Operator must use new cleaning paper to scrub the rubber tip.	Visual sample check during DB(5)	5	80	None						
			8			3	set dispense parameter per positrol log check epoxy expiration date	DB(5) Trial run on the first strip after set up(4) OBC/ODC auto alarm(2)	2	48	None						
			8		Wrong rubber tip size	2	Check rubber tip size per bonding diagram Change rubber tip per device change	Visual sample check during DB(5) Trial run on the first strip after set up(4)	4	64	None						

Item: SOIC16/28/32/54ld	Control Number/Issue: 8	3MCT00002A/	/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: I	Freescale, TJN-F	TM
Prepared By: Amanda Wang	FMEA Date:	05-Oct-94	(Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XL	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN	14-Nov-13	(Rev.)
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													Action F	esui	lts	_	_
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/ Process	D	R	Recommended	Responsibility &				D	R
Function/ Requirements	Mode	Effect(s) of Failure	E V	l a s	Cause(s)/ Mechanism(s) of Failue	C C	Process Controls	Controls Detection	E T		Action(s)	Target Completion Date	Effective Date		C	E T	P N
		reliability failure.(8) electrical failure.(8) wire bond non-	8	5	improper dispensering position.	2	calibrate dispensering height & position per TCM	Visual sample check during DB(5)	5	80	None						
		511/4 / 11	8		air trapped in syringe.	2	follow right epoxy thawing procedure.	Visual sample check during DB(5)	5	80	None						
			8		gradient "index"	2	Quarterly PM	Visual sample check during DB(5)	5	80	None						
			8		Incorrect bonding parameter.	1	Check per TCM checklist.	Visual sample check during DB(5)	5	40	None						
	Bent lead	electrical failure.(8)	8		"index" jamming	2	sensor to prevent iamming.	Visual sample check during DB(5)	5	80	None						
	Die scratch	electrical failure.(8) Reliability problem(8)	8		Stained rubber tip.	2	Change rubber tip per SOP.	Visual sample check during DB(5)	5	80	None						
			8		Mishandling operation during sampling inspection	2	Operator follow SOP and WI	Visual sample check during DB(5)	5	80	None						
		electrical failure.(8) Wire bond alignment error(4) Reliability problem(8)	8		bondhead rail worn out.	2	checking during quarterly PM replace with new one during yearly PM.	Visual sample check during DB(5). Post bond inpsection & auto alarm (2)	2	32	None						
			8		"y shuttle" worn out.	2	yearly PM & replace with new one if necessary	Visual sample check during DB(5)	5	80	None						

Item: SOIC16/28/32/54ld	Control Number/Issue:	83MCT00002A/	/BY	
Type: Design _x_ Process	Company, Group, Site/Business Unit:	Freescale,TJN-F	FM	
Prepared By: Amanda Wang	FMEA Date:	05-Oct-94	(Orig.)	
Core Team: Amanda Wang,H.J. Liu,Ivory Guo,JUN YING ZHENG,XI	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN	14-Nov-13	(Rev.)	

													Action F				
Process	Potential Failure		S		Potential	О		Current Design/ Process	D		Recommended	Responsibility &	Actions Taken &		O		
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е	P	Action(s)	Target	Effective Date			E	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
				s	of Failue												ĺ
				s													İ
			8		improper rubber	3	Select rubber tip per	Visual sample check during	2	48	None						
					tip size.		B/D when device	DB(5)									İ
							change.	Post bond inpsection & auto									
								alarm (2)									İ
			8		Improper PRS	1		Visual sample check during	5	40	None						Г
					teaching.			DB(5)									
			8		Improper eject pin	1	Calibrate eject when	Visual sample check during	5	40	None						İ
					set up		quarterly PM.	DB(5)									İ
			8		Epoxy dispensing	1	Setup using ink die	Visual sample check during	5	40	None						Н
					off center		every device change										İ
							& die bonder										İ
							parameter change										İ
			8		Rubber tip worn	3	Shiftly change the	Visual sample check during	5	120	To qualify new	JUN YING					H
					out.		rubber tip.	DB (5)				ZHENG B09174					İ
											higher hardness.	05/13/2014					ĺ
											Sev(8) Occ(2)						ĺ
											Det(5)						İ
	Low die shear	Reliablity	8		inadequate curing	2	Select the proper	Die shear test (4)	4	64	None						Ī
		failure(8)			temp/time.		cure profile per										ĺ
							TCM.										İ
							replace the thermal										ĺ
							couple every year calibrate tunnel										İ
							tomp quartarly										
			8		expired epoxy	2	record & check	Die shear test (4)	2	32	None						
							epoxy expiration	MMS system alarm (1)									ĺ
	L/F discoloration	Reliability	8	1	Improper N2 flow	2	date per TCM. Check the N2 flow	Visual sample check during	5	80	None			$\vdash$	$\dashv$		┢
	L/1 discoloration	failure.(8)	0		rate.		rate per TCM.	DB(5)	,	30	None						ĺ
		Non-stick on					Set up and mark	22(0)									ĺ
		lead.(4)					acceptable flow rate										ĺ
							on flow meter										

Item: SOIC16/28/32/54ld	Control Number/Issue: 8	83MCT00002A/	/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: I	Freescale,TJN-F	FM
Prepared By: Amanda Wang	FMEA Date:	05-Oct-94	(Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XL	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN	14-Nov-13	(Rev.)
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													Action F	Resu	lts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/ Process	D	R	Recommended	Responsibility &	Actions Taken &			D	
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е	P	Action(s)	Target	Effective Date	Е	C	Е	
Requirements		Failure	V	a	Mechanism(s)	С	Prevention		Т	N		Completion Date		V	C	T	]
•				s	of Failue							_					ı
				s													ı
			8		Improper tunnel	2	Auto alarm when	Visual sample check during	2.	32	None			H		$\dashv$	$\vdash$
					temp.		the temperature is	DB(5) machine auto alarm									i
					r .		too high.	(2)									l
							Č	, ,									_
	Bondline	Reliability	8		improper bond	1	Autoteach bond	Visual sample check during	5	40	None						i
	thickness issue	failure(8)			height	_	height	DB(5)	_	10					_		<u> </u>
			8		Tilted pick-up holder	1	Quarterly PM	Visual sample check during DB(5)	5	40	None						l
			8		Blocked dispenser	2	Pump change per 4		5	80	None				_	$\dashv$	
			0		pump	_	days	Sampling measure BET(3)	9	00	None						ł
			8		Improper rubbler	1	Standard operation	Sampling measure BLT(5)	4	32	None					$\neg$	
					tip installation		procedure in WI	Trial run on the first strip									ı
								after set up(4)									<u> </u>
	Excessive die tilt	W/B bond	8		Bond head tilt	1	Quarterly PM	Sampling measure BLT (5)	5	40	None						l
		performance															i
		issue(4)															i
		Reliability															i
		failure(X)	8		Wrong dispensing	1	Dedicated	Measure the die tilt with	4	32	None					$\dashv$	
					status / setup		technician for	dummy die before									i
					<u>I</u>		convertion/setup	production. (4)									
			8		Impurity in epoxy	2		Measure the die tilt with	4	64	None						ı
								dummy die before									i
					****		CI 1 11 d	production. (4)	_	40	N.T.				_		
			8		Wrong rubber tip	1	Check rubber tip	Sampling measure BLT(5)	5	40	None						ı
							size per bonding diagram										ı
			8		Bond Force/Scrub	1	Set up per TCM	Sampling measure BLT (5)	4	32	None				-	$\dashv$	
					settings too low	1	Set up per Tem	Sampling measure BE1 (3)		32	rvone						l
			ļ.		_				L.					$\sqcup$			⊢
	Wrong orientation		4		Edder sensor	2		Visual sample check during	4	32	None						i
		failure(4)			failure			DB(5)									ı
	1				I		<u> </u>	Daily check the sensor(4)		1	<u>I</u>	<u> </u>					

Item: SOIC16/28/32/54ld	Control Number/Issue: 8	3MCT00002A/	BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: F	Freescale, TJN-F	M
Prepared By: Amanda Wang	FMEA Date:	05-Oct-94	(Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XL	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN	14-Nov-13	(Rev.)
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													Action F		lts	_	
Process	Potential Failure	Potential	S	C	Potential	О	Current Design/	Current Design/ Process	D		Recommended	Responsibility &	Actions Taken &	S			
Function/	Mode	Effect(s) of	E	1	Cause(s)/	C	Process Controls	Controls Detection	Е		Action(s)	Target	Effective Date	Е		Е	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
				S	of Failue												
				S													i l
	contamination on	W/B non-stick(5)	8		excessive epoxy	2	set dispense	Visual sample check during	2	32	None						
	lead	Electrical					parameter per	DB(5)									i
		failure(8)					positrol log.	OBC/ODC auto alarm(2)									i
		reliability					checking epoxy										i
		failure(8)					expiration date per										i l
			8		inconsistent	2	checking epoxy	Visual sample check during	5	80	None						
					epoxy dispensing.		expiration date per	DB(5)									
							TCM.										i
							dispensing vacuum										i
							checking per TCM										i l
	Too much resin	W/B nonstick(4)	4		L/F quality issue	3	L/F suppliers	Visual sample check during	5	60	None					П	
	bleed						*	DB(5)									
			4		11.	_	bleed test by lot	*** 1 1 1 1 1 1	~	40	<b>N</b> 7					Ш	$\vdash$
			4		epoxy quality issue	2		Visual sample check during DB(5)	5	40	None						
	epoxy under/over	Reliability	8		Curing oven issue	1	Auto locking when	Die shear monitor(4);	2	16	None					П	
	cure	failure(8)						Curing profile monitor(3);									i
							alarm when curing	Over heat auto alarm(2);									i
							finished										i l
	epoxy void	Reliability	8		Mylar tape	1	D870 UV-mylar	Visual sample check during	5	40	None					П	l
		failure(8)			residua		using integrated UV	DB(5)									i
							illumination in Saw										
			8		Wrong dispenser	2	machine Auto teach	Visual sample check during	5	80	None					Н	$\vdash$
			٥		Z-height	_	dispenser Z-height	DB(5)	٥	80	none						l I
					Z noight	L	dispenser 2 neight										<u>.                                    </u>
	wrong epoxy	Reliability	8		Operator select	3			2	48	None						
		failure(8)			wrong epoxy type			and epoxy change(4)									l l
								Check epoxy in SFC									ı l
	l							system(2)	<u> </u>	]						ш	

Item: SOIC16/28/32/54ld	Control Number/Issue: 83	3MCT00002A/	ВҮ	
Type: Design _x_ Process	Company, Group, Site/Business Unit: Fr	reescale,TJN-F	M	
Prepared By: Amanda Wang	FMEA Date:	05-Oct-94	(Orig.)	
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN	14-Nov-13	(Rev.)	
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		_											Action F				
Process	Potential Failure	Potential	S	C	Potential	О	Current Design/	Current Design/ Process			Recommended	Responsibility &	Actions Taken &	S			
Function/	Mode	Effect(s) of	E	1	Cause(s)/	C	Process Controls	Controls Detection	Е	P	Action(s)	Target	Effective Date		C	Е	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
				s	of Failue												1
				s													1
	mixed lots	Electrical	8		wafer or material	3	Genesis system can	Visual sample check during	2	48	None						Π
		failure(8)			mismatch with		only move account	DB(5)									l
					ASO		when the materials	System auto alarm for BOM									l
							being used is match	mismatch(2)									l
							with the BOM.										l
	L/F deformation	electrical	8		"index" jamming	2	equipped with detect	Visual sample check during	5	80	None						Г
		failure.(8)					sensor to prevent	DB(5)									l
							iamming.										L
			8		L/F deformation	2	Control dispenser	Visual sample check during	5	80	None						l
					by dispenser needle		needle height to L/F no less than 0.15mm	DB(5)									
					needie		Quarterly adjust and										l
							calibrate L/F clamp										l
							Canorate L/1 Clamp										l
																	$\vdash$
			8		Improper position	1	Check L/F picking	Visual sample check during	5	40	None						1
					of L/F input		up motion when setup machine and	DB(5)									1
					gripper		device change										1
			8		L/F droped	1	THE VICE COMMISSION	Visual sample check during	5	40	None						
								DB(5).									
			8		Load L/F into	1	Load L/F into		5	40	None						l
					cassette directly		cassette with bundle	DB(5).									l
					no bundle protect.		protect										l
	Epoxy expired	Reliability	8		Operator miss	1		Material system auto alarm	2	16	None						
		failure(8)			handling			for overdue epoxy(2)									l
			_						_								<u> </u>
	1 ,	Electrical	8		Excessive epoxy	2	Set up per TCM	Visual sample check during	2	32	None						l
		failure(8)						DB(5)									l
		Reliability						Trial run on the first strip									l
		failure(8)						after set up(4) OBC/ODC auto alarm(2)									l

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)
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													Action F			
Process Function/	Potential Failure Mode	Potential Effect(s) of	S E	C 1	Potential Cause(s)/	O C	Current Design/ Process Controls	Current Design/ Process Controls Detection	D E		Recommended Action(s)	Responsibility & Target	Actions Taken & Effective Date		D E	
Requirements	Mode	Failure	V	a s s	Mechanism(s) of Failue	C	Prevention Prevention	Controls Detection	T		Action(s)	Completion Date	Effective Date	V	T	N
			8		Epoxy off center dispensing	1	Set up per TCM	Machine auto alarm(2) Visual monitor during bonding(4)			None					
	leadframe backside	Resin bleed happened in mold process (5)	5		Incorrect dispensing pressure & vacuum setting	1	Set up TCM package	Visual sample check during DB (5)	5	25	None					
	Wrong L/F	Wire bond failure(4)	4		Mishandling on L/F selection	1	Check per bonding diagram and assembly shop order. Use index sensor to identify LF. Check the bar code on the LF packaging	Die bonder auto alarm(2) Visual sample check during DB(5)	2	8	None					
	Wrong die picked (EWM only)	Final Test Yield loss (6)	6		Load wrong wafer map	1	Read barcode (sticked automatically by machine before dicing saw) information automatically on	skeleton. (5) 100% Electrical Test (5) Visual check on sticked barcode. (4)		24	None					
			6		Wrong barcode printed due to scribe ID area is less recognizable	1		Visual inspection on sticked barcode (4)	4	24	None					
			6		Wrong reference die.	1	Verify reference die location with wafer map.	skeleton. (5) Electrical Test (5)		30	None					
	Wrong bin picked (EWM only)	Final Test Yield loss (6)	6		Wrong bin selection	1	Check good die quantity before lot start	Visual inspection on wafer skeleton. (5) Electrical Test (5)	5	30	None					

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Item: SOIC16/28/32/54ld	Control Number/Issue: 8	3MCT00002A/	BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: F	Freescale, TJN-F	M
Prepared By: Amanda Wang	FMEA Date:	05-Oct-94	(Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN	14-Nov-13	(Rev.)
<u> </u>			
			Action Results

												Action I			
Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	S E V	Potential Cause(s)/ Mechanism(s) of Failue	O C C	Process Controls	Current Design/ Process Controls Detection	D E T		Recommended Action(s)	Responsibility & Target Completion Date	Effective Date	Е	D E T	
	1	Final Test Yield loss (6)	6	Wafer Alignment Problem	1	Die bond machine will stop immediately once met alignment fail.	Machine auto alarm(2) Visual sample check during DB on wafer skeleton(5) Electrical Test (5)	2	12	None					
3.2 Pre-wire bonding plasma clean	Incomplete cleanliness	Nonstick on W/B(5) Delamination after mold(6) Reliability failure(8)	8	malfunction	2	Quarterly PM	Machine auto alarm (2) Measure contact angle on die and Leadframe(5)		32	None					
			8	no/insufficient gas/vaccum	2	Quarterly PM	Machine auto alarm (2) Measure contact angle on die and Leadframe(5)		32	None					ı
4. Wire bond (Au wire)	golf ball, smash	Reliability failure(8) Electrical failure(8)	8	Improper EFO strike pole position	2	Quarterly PM		5	80	None					
			8	USG transfer malfunction	2	Calibrate impedance when changing capillary. Qualified technician can change the capillary.	Visual sample check (5) Sample PBI (5) AutoPBI(5) Machine auto alarm after capillary calibration fails(2)	2	32	None					
			8	Improper wire bond parameters	2	Lock key paramters by PM and only technician or above can change the parameters. Check parameters in TCM.	Visual sample check (5) Sample PBI (5) AutoPBI(5)	5	80	None					

Item: SOIC16/28/32/54ld	Control Number/Issue: 8	3MCT00002A/	BY
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Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XL	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN	14-Nov-13	(Rev.)
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													Action F	Resu	lts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/ Process	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е		Action(s)	Target	Effective Date			Е	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
				s	of Failue											i '	
				s													
			8		Missing of bond	1	Machine auto	· · · · · · · · · · · · · · · · · · ·	5	40	None					1	
					height teach		reteach	Sample PBI (5)								i '	
			8		Improper bond	2	Quarterly PM	AutoPBI(5) Visual sample check (5)	5	80	None				_	—	-
					force calibration	_	Quarterly 1 W	Sample PBI (5)	,	00	rone					i '	
								AutoPBI(5)								l	
	_	Electrical failure	8		Head Block and	2	Technician check	· · · · · · · · · · · · · · · · · · ·	4	64	None					1	
		(8)			window clamping		heat block under	Sample PBI (5)								i '	
		Reliability			malfunction		microscope	Wire pull SPC monitor(4)								i '	
		issue(8)					quarterly and qualified technician									i '	
							can change heat									i '	
							block.									i '	
							check under									l '	
			8		Capillary out of	1	Set up capillary life	Visual sample check (5)	2	16	None					$\Box$	
					life		limit in wire	Sample PBI (5)								i '	
							bonding machine	Wire pull SPC monitor(4)								i '	
								Machine auto alarm when								i '	
								capillary life exceeds								i '	
			8		Wire clamp issue	2	Quarterly PM	Visual sample check (5)	4	64	None					_	
								Sample PBI (5)								i '	
			0					Wire pull SPC monitor(4)								<u>—</u>	<u> </u>
			8		Improper bonding	2	Lock the recipe per device	Visual sample check (5)	4	64	None					i '	
					parameters		Check loop height	Sample PBI (5) Wire pull SPC monitor(4)								l '	
							after set up	whe pun 31 C monitor(4)								i '	
																<u> </u>	<u> </u>
			8		Gold wire quality	1	IQC imcoming	r	4	32	None					l '	1
					issue		check	Sample PBI (5) Wire pull SPC monitor(4)								1	1
			8		Index malfunction	2	Quarterly PM		4	64	None				$\dashv$	一	
			ľ			<u> </u>		Sample PBI (5)	ľ							1	1
								Wire pull SPC monitor(4)								1	

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)
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Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/ Process	D	R	Recommended	Responsibility &	Actions Taken &	S	O	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	С	Process Controls	Controls Detection	Е	P	Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		Т	N		Completion Date		V	C	T	N
•				s	of Failue							Î					i
				s													i
			8		Gold wire path	2	Quarterly PM	Visual sample check (5)	4	64	None						i
					issue			Sample PBI (5)									i
								Wire pull SPC monitor(4)									<u> </u>
			8		Lead vibration	1	Leadframe incoming	1 · · · · · · · · · · · · · · · · · · ·	4	32	None						i
							check	Sample PBI (5)									ı
								Wire pull SPC monitor(4)									ı
								Function line test of									ı
			8		Mishandling	2.	Standardize the	Leadframe(5) Visual sample check (5)	4	64	None				_		
					operation( load	_	inspection method	Sample PBI (5)	ľ	0.	rone						l
					magazine, unit		Operators follow	Wire pull SPC monitor(4)									l
					inspection,wire		SOP and WI	· · · · · · · · · · · · · · · · · · ·									ı
					change etc)												<u> </u>
			8		Foreign matter on	1	Technician check	Visual sample check (5)	4	32	None						i
					heat block		heat block under	Sample PBI (5)									ı
							microscope	Wire pull SPC monitor(4)									ı
							quarterly and										ı
							qualified technician										ı
							can change heat										
	Pad bond & post	Intermittent	8		PRS failure	2	PM calibrated PRS	Non-stick auto alarm (2)	2	32	None						Ī
	bond placement	electrical					when quarterly PM.	Visual sample check (5)									l
		fail/short(8)						Sample PBI (5)									l
		Reliability						AutoPBI(5)									ı
		failure(8)															i
			8		x-y table problem	1	PM maintain X-Y	Non-stick auto alarm (2)	2	16	None						
							table in yearly PM	Visual sample check (5)									ı
								Sample PBI (5)									ı
			1_			_		AutoPBI(5)	<u> </u>					Щ	_		Ь—
			8		improper offset	2	teach offset when	(-)	2	32	None						i
					between actual		capillary change	Visual sample check (5)									ı
					tool position &			Sample PBI (5)									i
					camera			AutoPBI(5)									i '
																	i

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)
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													Action I			
Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	S E V	C 1 a s	Potential Cause(s)/ Mechanism(s) of Failue	O C C	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	D E T	P	Recommended Action(s)	Responsibility & Target Completion Date	Effective Date	Е	D E T	1
			8		Improper manual alignment	2	Use special target point to do alignment when setup. Training operators how to using auto alignment instead of manual alignment.	Non-stick auto alarm (2) Visual sample check (5) Sample PBI (5) AutoPBI(5)	2	32	None					
			8		Lens air cooling system issue	2		Non-stick auto alarm (2) Visual sample check (5) Sample PBI (5) AutoPBI(5)	2	32	None					
	Wire deformation( tight,sagging, leaning, smashed,excess loop etc)	Electrical failure(8)	8		Window clamping and heat block issue	2	Technician check heat block under microscope quarterly and qualified technician can change heat	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None					
			8		Wire clamp issue( abrasion, contamination, loose, tighten etc.)		Quarterly PM	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None					
			8		Improper looping parameters		Lock loop parameters	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None					
			8		Capillary issue( wrong type, life etc)	1	Check capillary type in TCM and B/D. Capillary life is locked in recipe.	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	32	None					

Item:	SOIC16/28/32/5	4ld							C	ontr	ol Number/Issue:	83MCT00002A/E	3Y				
Type:	Design	_x_ Process						Company,C	Grou	ıp,Si	te/Business Unit:	Freescale, TJN-FN	Л				
Prepared By:	Amanda Wang										FMEA Date:	05-Oct-94	(Orig.)				
Core Team:	Amanda Wang,F	I.J. Liu,Ivory Gu	o,JU	N YI	NG ZHENG,XIA	OF	IUI KANG,SHUAI	N YAO,Cyndi Hu,Grayson	Che	en,L	ANPING BAI,JIN	14-Nov-13	(Rev.)				
								•					•				
													Action I	Resi	ults		
Process	Potential Failure	Potential	S	С	Potential	0	Current Design/	Current Design/ Process	D	R	Recommended	Responsibility &			_	D	R
Process Function/	Potential Failure Mode	Potential Effect(s) of	S E	C 1	Potential Cause(s)/	O C	Current Design/ Process Controls	Ŭ .		R P		Responsibility & Target		S	О		
				1		O C C	Process Controls	Ŭ .					Actions Taken & Effective Date	S E	O C	Е	

Operators follow

SOP and WI

Yearly PM

Die bon placement

and orientation

and technician or

above can change

the parameters; check parameters in

Machine auto

Only process

engineers have authority to edit the recipe; wirebond recipe name rule align with bonding diagram no and rev;recipe modification approval system

control

TCM

reteach

Mishandling

operation( load

magazine, unit

inspection,wire

indexer/elevator

Improper die bond 2

Machine

problem.

placement

bonding

parameters

Missing of bond

Die quality issue

Wrong recipe

height teach

Improper pad

Cratering

Miss bond

Electrical

failure(8)

Reliability

failure(8)

Electrical

failure(8)

Visual sample check (5)

Wire pull SPC monitor(4)

Visual sample check (5)

Wire pull SPC monitor(4)

Visual sample check (5)

Non-stick auto alarm (2)

Visual sample check (5)

Machine auto alarm(2)

Visual sample check (5)

Sample PBI (5)

Sample PBI (5)

Sample PBI (5)

Sample PBI (5) Wire pull SPC monitor(4)

Lock key parameters Non-stick auto alarm (2)

64

64

64

2 32

16

32

40

None

None

None

None

None

None

None

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)
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							-						Action F		_		
Process	Potential Failure		S		Potential	О	~	Current Design/ Process				Responsibility &					
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е		Action(s)	Target	Effective Date		C		
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
				S	of Failue												
				S													
			8		Mixed devices	1	Check the assembly	· (- )	2	16	None						
							shop order before	Sample PBI (5)									
							lot start.and record	PRS Auto alarm(2)									
							the magazine number										
							number										
			8		Wrong wire bond	2	Lock the " always"	Visual sample check (5)	2	32	None						
					start sequence		start from seleted	Sample PBI (5)									
							wire function	PRS Auto alarm(2)									
	Deform Lead		8		Index jamming	3	Equipped with	Machine jam alarm(2)	2	48	None						
		bleed(4)					detect	Non stick auto alarm (2)									
		Electrical					sensor to prevent	Visual sample check (5)									
		failure(8)					jamming. PM check index	Sample PBI (5)									
							quarterly										
			8		Window clamping	2	Technician check	Machine jam alarm(2)	2	32	None						
					and heat block		heat block under	Non stick auto alarm (2)									
					issue		microscope	Visual sample check (5)									
							quarterly and	Sample PBI (5)									
							qualified technician can change heat										
							block.										
			<u> </u>						_								
			8		Leadframe quality	1	_	Machine jam alarm(2)	2	16	None						
					issue		check;	Non stick auto alarm (2) Visual sample check (5)									
								Sample PBI (5)									
								Function line test of									
								Leadfram(5)									
								. ,									Ц_

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00	002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale,	ГJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct	i-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XIA	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov	v-13 (Rev.)

													Action I	Resi	lts	_	
Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	S E V	C 1 a s	Potential Cause(s)/ Mechanism(s) of Failue	O C C	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	D E T		Recommended Action(s)	Responsibility & Target Completion Date	Actions Taken & Effective Date	S E V	C	Е	P
		Electrical failure(8) Reliability failure(8)	8	*	Insufficient heat transfer/downhold er clamping	1	Check heat block quarterly	Wire pull SPC monitor(4)	4	32	None						
			8	*	Wafer/Die issue ( Pad metal problems:big probe mark; pad scratch,contamina tion etc)	2	DI water cleaning during saw for wafer	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Wafer incoming check(4)	4	64	None						
			8	*	USG transfer malfunction	1	when changing capillary.	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Machine auto alarm after capillary calibration fails(2)	2	16	None						
			8	*	Capillary issue( wrong type, life etc)	1	Check capillary type in TCM and B/D. Capillary life is locked in recipe.	Ball shear SPC monitor(4) Wire pull SPC monitor(4)	4	32	None						
			8	*	Improper wire bond parameters	2	Lock key parameters and technician or above can change the parameters; check parameters in TCM	Ball shear SPC monitor(4) Wire pull SPC monitor(4)	4	64	None						
			8	**	Floating leadframe(Flag)on heat block.	3	Setup check. Qualified technician do the conversion and teach bond.	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Sample PBI (5) Machine auto alarm when vacuum out of control(2)	2	48	None						

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY	
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM	
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)	
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XIA	OHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)	

		-											Action F				
Process	Potential Failure	Potential	S		Potential	О	Current Design/	Current Design/ Process			Recommended	Responsibility &	Actions Taken &			D	
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е	P	Action(s)	Target	Effective Date		C	Е	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
				S	of Failue											ıl	11
				S												ıl	ii.
	Weak bond on	Electrical	8	*	Head Block and	2	Technician check	Visual sample check (5)	4	64	None					П	
	lead(( Stitch bond	failure(8)			window clamping		heat block under	Sample PBI (5)								ıl	ii
	deformation,	Reliability			malfunction		microscope	Wire peel test (4)								ıl	ii
	peeling, crack	failure(8)					quarterly and									ıl	i
	etc)						qualified technician									ıl	1
							can change heat									ıl	ii
			8	*	USG transfer	1	Calibrate impedance	Visual sample check (5)	2	16	None					П	
					malfunction		when changing	Sample PBI (5)								ıl	i
							capillary.	Wire peel test (4)								ıl	i
							Qualified technician	Machine auto alarm after								ıl	i
							can change the	capillary calibration fails(2)								ıl	i
							capillary.									ıl	i
																il	iı
			8	*	Capillary issue(	1	Check capillary type	Visual sample check (5)	4	32	None					一	
					wrong type, life		in TCM and B/D.	Sample PBI (5)								ıl	1
					etc)		Capillary life is	Wire peel test (4)								ıl	i
							locked in recipe.									il	iı
			8	sk:	Imamanan yezina	2.	Lock key parameters	Visual sample check (5)	4	64	None				-	$\dashv$	—
			٥		Improper wire bond parameters		and technician or	Sample PBI (5)	4	04	none					ıJ	11
					bond parameters		above can change	Wire peel test (4)								ıJ	i
							the parameters;	The peer test (4)								ıJ	i
							check paramters in									ıJ	i
							TCM									ıJ	i
			1	l													

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)
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													Action F				
Process	Potential Failure	Potential	S		Potential	О	U	Current Design/ Process			Recommended	Responsibility &	Actions Taken &				
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е		Action(s)	Target	Effective Date			Е	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
				s	of Failue												
				s													
			8	*	Leadframe defect	2	Preserve leadframe	Visual sample check (5)	4	64	None						
					before wire bond		in cabinet well with	Sample PBI (5)									
					(contamination,		N2 gas protection.	Wire peel test (4)									
					oxidization, lead		Hand free method										
					damage, foreign		during sample										
					matter, etc. )		checking										
							Function line test										
							and pick out the defect lead frame										
							Machine cover										
							above work holder										
							Use pre-wire										
							bonding plasma										
							clean										
			8	*	Insufficient heat	1	Check heat block	Visual sample check (5)	4	32	None						
					transfer/downhold		quarterly	Sample PBI (5)									
				ļ. —	er clamping			Wire peel test (4)									
			8		Improper second	1	Locked second bond	Visual sample check (5)	4	32	None						
					bond position		position in recipe	Wire peel test(4)									
			8	*	Mishandling	2	Operators follow	Visual sample check (5)	4	64	None						
					operation( load		SOP and WI	Sample PBI (5)									
					magazine, unit			Wire peel test(4)									
					inspection,wire												
			8	sk	change etc) Excessive epoxy	2	Set dispense	Visual sample check (5)	2	48	None						<u> </u>
			0		Excessive epoxy	3	parameter per	Setup check before W/B(4)		40	none						
							positrol log	OBC/ODC auto alarm(2)									
							check epoxy	OBC/OBC auto ararm(2)									
							expiration date										
			8	*	Foreign matter	2	Monthly cleaning	Visual sample check (5)	4	64	None						
							wire bonder index	Sample PBI (5)									
					<u>l</u>		İ	Wire peel test(4)									

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI.	OHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)
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	_	_											Action I				
Process Function/	Potential Failure Mode	Potential Effect(s) of	S E	C 1	Potential Cause(s)/	O C	Current Design/ Process Controls	Current Design/ Process Controls Detection	Е	P	Recommended Action(s)	Responsibility & Target	Actions Taken & Effective Date	Е		Е	F
Requirements		Failure	V	a s s	Mechanism(s) of Failue	С	Prevention		Т	N		Completion Date		V	C	Т	N
	Foreign matter(wire tail, epoxy, particle ect)	Electrical failure(8) Reliability failure(8)	8		Wafer incoming issue	2	DI water cleaning during saw	Visual sample check (5) Sample PBI (5)	5	80	None						
			8		Wire clamper issue( tight,contaminatio n,worn out etc)	2	Wire clamp PM quarterly	Visual sample check (5) Sample PBI (5)	5	80	None						
			8		Mishandling of wire( removing bond off wires, wire theading etc)	3	Standard operation following WI	Visual sample check (5) Sample PBI (5)	5	120	Qualify OCP (Out Chamfer Polish) Capillary on COSSLITE_TSM C to improve the 2nd bond performance. Sev(8) Occ(2) Det(5)	SHUAN YAO B07524/05-11- 2014					
			8		Epoxy on lead or die	2	Die bond fillet height and resin bleed control	Visual sample check (5) Sample PBI (5)	5	80	None						
			8		Particles in air	2	Operation following FE cleaning room SOP	Visual sample check (5) Sample PBI (5)	5	80	None						
	Non stick on pad	Electrical failure (8)	8		Insufficient heat transfer/downhold er clamping		Check heat block quarterly	Non stick auto alarm(2) Ball shear SPC monitor(4) Wire pull SPC monitor(4)	2	16	None						
			8		Wafer/die issue ( Pad metal problems:big probe mark; pad scratch,contamina	2	DI water cleaning during saw for wafer	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Wafer incoming check(4) Non stick auto alarm(2)	2	32	None						

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI.	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)

													Action F	 		
Process	Potential Failure	Potential	S		Potential	О	Current Design/	Current Design/ Process	D		Recommended	Responsibility &			D	
Function/ Requirements	Mode	Effect(s) of Failure	E V	l a	Cause(s)/ Mechanism(s)	C C	Process Controls Prevention	Controls Detection	E T	P N	Action(s)	Target Completion Date	Effective Date	C C	E T	
				s s	of Failue											
			8		USG transfer malfunction	1	when changing capillary.	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Machine auto alarm after capillary calibration fails(2) Non stick auto alarm(2)	2	16	None					
			8		Capillary issue( wrong type, life etc)	1	Check capillary type in TCM and B/D. Capillary life is locked in recipe.	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Non stick auto alarm(2)	2	16	None					
			8		Improper wire bond parameters	2	Lock key parameters and technician or above can change the parameters; check paramter in TCM	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Non stick auto alarm(2)	2	32	None					
			8		Floating leadframe(Flag) on heat block.	2	Qualified technician do the conversion and teach bond.	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Machine auto alarm when vacuum out of control(2) Non stick auto alarm(2)	2	32	None					
	Non stick on lead	Electrical failure (8)	8		Head Block and window clamping malfunction	2	Technician check heat block under microscope quarterly and qualified technician can change heat	Visual sample check (5) Sample PBI (5) Wire peel test (4) Non stick auto alarm(2)	2	32	None					<u>-</u>

Item: SOIC16/28/32/54ld							Control Number/Issue: 83MCT00002A/BY											
Type: Designx_ Process							Company, Group, Site/Business Unit: Freescale, TJN-FM											
Prepared By: Amanda Wang							FMEA Date: 05-Oct-94 (Orig.)											
Core Team:	Amanda Wang,H	.J. Liu,Ivory Gu	IN Y	ING ZHENG,XI	IAOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)													
		•						•										
													Action Results					
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/ Process	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R	
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е	P	Action(s)	Target	Effective Date	Е	C	E	P	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N	
				s	of Failue												1	
				s													i	
			8		USG transfer	1	Calibrate impedance	Visual sample check (5)	2	16	None							
					malfunction		when changing	Sample PBI (5)									i	
							1 *	Wire peel test (4)									i	
							~	Machine auto alarm after									i	
								capillary calibration fails(2)									i	
							capillary.	Non stick auto alarm(2)									i	
		_	8		Capillary issue(	1	Check capillary type	Visual sample check (5)	2	16	None							
					wrong type, life		in conversion	Sample PBI (5)									ii.	

Wire peel test (4)

Sample PBI (5)

Wire peel test (4)

Non stick auto alarm(2)

Visual sample check (5)

Non stick auto alarm(2)

2 32

None

checklist and B/D.

Lock key parameters

and technician or

above can change the parameters;

check paramter in

TCM

Capillary life is

locked in recine

etc)

Improper wire

bond parameters

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY									
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM									
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)									
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)									
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														Action Results					
Process	Potential Failure		S	C	Potential	О	C	Current Design/ Process			Recommended	Responsibility &	Actions Taken &			D			
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е	P	Action(s)	Target	Effective Date	Е		E	P		
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N		
				S	of Failue														
				s															
			8		Leadframe defect	2	Preserve leadframe	Visual sample check (5)	2	32	None								
					before wire bond		in cabinet well with	Sample PBI (5)											
					(contamination,		N2 gas protection.	Wire peel test (4)											
					oxidization, lead		Hand free method	Non stick auto alarm(2)											
					damage,etc.)		during sample												
							checking												
							Function line test												
							and pick out the												
							defect lead frame												
							Machine cover												
							above work holder												
							Use pre-wire												
							bonding plasma												
							clean.( only for bga												
							,lga sony, leaded												
					T CC 1 1 1		pkgs)	77' 1 1 1 (5)	2	1.6	3.7								
			8		Insufficient heat	I	Check heat block	· · · · · · · · · · · · · · · · · · ·	2	16	None								
					transfer/downhold		quarterly	Sample PBI (5)											
					er clamping			Wire peel test (4) Non stick auto alarm(2)											
	Excessive "Tail"	Eletrcial failure	8		Improper wire	2	Lock key parameters		5	80	None								
		(8)			bond parameters		and technician or	Sample PBI (5)			- 1 - 1 - 1								
					I		above can change	1 ( )											
							the parameters;												
							check paramter in												
							TCM												
	Wrong wire type	Reliability	8		Mishandling on	1	Follow assembly	SFC auto alarm when	2	16	None								
	Wrong wire type used	failure(8)	٥		wrong wire type	1	shop order and SFC	material part number not		10	none								
	useu	Electrical			wrong whe type		system control	match with system record(2)											
		failure(8)					system control	materi with system record(2)											

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI.	OHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)
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				 								Action I			
Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	S E V	Potential Cause(s)/ Mechanism(s) of Failue	O C C	Process Controls	Current Design/ Process Controls Detection	D E T	P	Recommended Action(s)	Responsibility & Target Completion Date	Effective Date	Е	Е	P
	Ball neck crack	Electrical failure(8) Reliability failure(8)	8	Incorrect parameters on first bond and loop formation	2	Lock loop parameters; Lock key parameters and technician or above can change the parameters; Check paramters in TCM	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None					
4. Wire bond (Cu wire)	golf ball, smash	Reliability failure(8) Electrical failure(8)	8	Improper EFO strike pole position condition	2	Quarterly PM	Visual sample check (5) Sample PBI (5)	5	80	None					
			8		2	Calibrate impedance when changing capillary. Qualified technician can change the capillary.	Visual sample check (5) Sample PBI (5) AutoPBI(5) Machine auto alarm after capillary calibration fails(2)	2	32	None					
			8	Improper wire bond parameters	2	Lock key paramters by PM and only technician or above can change the parameters. Check parameters in TCM.	Visual sample check (5) Sample PBI (5) AutoPBI(5)	5	80	None					
			8	Missing of bond height teach	1	Machine auto reteach	Visual sample check (5) Sample PBI (5) AutoPBI(5)		40	None					
			8	Improper bond force calibration	2	Quarterly PM	Visual sample check (5) Sample PBI (5) AutoPBI(5)	5	80	None					

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI.	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)

													Action I				
Process	Potential Failure	Potential	S	C	Potential	О	Current Design/	Current Design/ Process			Recommended	Responsibility &	Actions Taken &				R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е		Action(s)	Target	Effective Date	Е		Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	Т	N
				s	of Failue												
				s													
			8		Cu wire oxidation	4	Cu wire shelf life and work life control; Forming gas flow monitor(auto)	Visual sample check (5) Sample PBI (5) AutoPBI(5) Machine auto alarm when forming gas flow out of control(2) Material system auto alarm	2	64	None						
	W. I	Fi 4: 16 1	0		H IN I	2		when Cu wire expired shelf life or work life(2)	4		N.						
	_	Electrical failure (8) Reliability issue(8)	8		Head Block and window clamping malfunction	2	Technician check heat block under microscope quarterly and qualified technician can change heat block. check under	Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8		Capillary out of life	1	Set up capillary life limit in wire bonding machine	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4) Machine auto alarm when capillary life exceeds			None						
			8		Wire clamp issue	2	Quarterly PM	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4		None						
			8		Improper bonding parameters	2	Lock the recipe per device Check loop height after set up	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						

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Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI	OHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)
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													Action F	Resu	lts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/ Process	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	С	Process Controls	Controls Detection	Е	P	Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	С	Prevention		Т	N		Completion Date		V	C	Т	N
•				s	of Failue							•					l
				s													l
			8		Copper wire	1	IQC imcoming	Visual sample check (5)	4	32	None					П	
					quality issue		check	Sample PBI (5)									l
					Ť			Wire pull SPC monitor(4)									
			8		Index malfunction	2	Quarterly PM	Visual sample check (5)	4	64	None						l
								Sample PBI (5)									l
			_					Wire pull SPC monitor(4)								Ш	—
			8		- 11	2	Quarterly PM	· · · · · · · · · · · · · · · · · · ·	4	64	None						l
					issue			Sample PBI (5)									l
			8		Lead vibration	1	Leadframe incoming	Wire pull SPC monitor(4)	4	32	None					Н	<del>                                     </del>
			8		Lead vibration	1	Į.	·(- /	4	32	None						l
							check	Sample PBI (5)									l
								Wire pull SPC monitor(4) Function line test of									l
								Leadframe(5)									l
			8		Mishandling	2	Standardize the	Visual sample check (5)	4	64	None					П	
					operation( load		inspection method	Sample PBI (5)									l
					magazine, unit		Operators follow	Wire pull SPC monitor(4)									l
					inspection,wire		SOP and WI	, ,									l
					change etc)											Ш	
			8		Foreign matter on	1	Technician check	Visual sample check (5)	4	32	None						l
					heat block		heat block under	Sample PBI (5)									l
							microscope	Wire pull SPC monitor(4)									l
							quarterly and										l
							qualified technician									, 1	l
							can change heat										l
	Pad bond & post	Intermittent	8		PRS failure	2	PM calibrated PRS	Non-stick auto alarm (2)	2	32	None					$\sqcap$	$\Box$
		electrical					when quarterly PM.	Visual sample check (5)								, 1	l
		fail/short(8)						Sample PBI (5)									l
		Reliability						AutoPBI(5)									l
		failure(8)						` '								, 1	1
			8		x-y table problem	1	PM maintain X-Y	Non-stick auto alarm (2)	2	16	None				-	$\dashv$	$\vdash$
			ľ		J more problem	ľ	table in yearly PM	Visual sample check (5)	١	1.5	1.5110					, 1	l
							more in journ in	Sample PBI (5)								, 1	l
								AutoPBI(5)								, 1	l

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
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													Action I			
Process	Potential Failure		S		Potential	О		Current Design/ Process				Responsibility &				
Function/ Requirements	Mode	Effect(s) of Failure	E V	l a s	Cause(s)/ Mechanism(s) of Failue	C C	Process Controls Prevention	Controls Detection	E T	P N	Action(s)	Target Completion Date	Effective Date	E V	C C	
				s												
			8		improper offset between actual tool position & camera	2	teach offset when capillary change	Non-stick auto alarm (2) Visual sample check (5) Sample PBI (5) AutoPBI(5)	2	32	None					
			8		Improper manual alignment	2	Use special target point to do alignment when setup. Training operators how to using auto alignment instead of manual alignment.	Non-stick auto alarm (2) Visual sample check (5) Sample PBI (5) AutoPBI(5)	2	32	None					
			8		Lens air cooling system issue	2		Non-stick auto alarm (2) Visual sample check (5) Sample PBI (5) AutoPBI(5)	2	32	None					
	Wire deformation( tight,sagging, leaning, smashed,excess loop etc)	Electrical failure(8)	8		Window clamping and heat block issue		Technician check heat block under microscope quarterly and qualified technician can change heat	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)			None					
			8		Wire clamp issue( abrasion, contamination, loose, tighten etc.)	2	Quarterly PM	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None					

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													Action F	Resu	lts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/ Process	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/ Requirements	Mode	Effect(s) of Failure	E V	l a s	Cause(s)/ Mechanism(s) of Failue	C C	Process Controls Prevention	Controls Detection	E T	P N	Action(s)	Target Completion Date	Effective Date	E V	C C	E T	P N
				S												Ш	
			8		Improper looping parameters	2	Lock loop parameters	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8		Capillary issue( wrong type, life etc)	1	in TCM and B/D.	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	32	None						
			8		Mishandling operation( load magazine, unit inspection, wire change etc)	2		Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8			2	Yearly PM	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8		Improper die bond placement	2	Die bon placement and orientation control	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
		Electrical failure(8) Reliability failure(8)	8		Improper pad bonding parameters	2	Lock key parameters and technician or above can change the parameters; check parameters in TCM	Non-stick auto alarm (2)	2	32	None						
			8		Missing of bond height teach	1	Machine auto reteach	Non-stick auto alarm (2)	2	16	None						
			8		Die quality issue	2		Visual sample check (5) Machine auto alarm(2)	2	32	None						

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
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Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI	OHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)
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	_												Action I			
Process	Potential Failure		S		Potential	О		Current Design/ Process					Actions Taken &			
Function/ Requirements	Mode	Effect(s) of Failure	E V	a s	Cause(s)/ Mechanism(s) of Failue	C C	Process Controls Prevention	Controls Detection	E T	P N	Action(s)	Target Completion Date	Effective Date	E V	C C	
	Miss bond	Electrical failure(8)	8	S	Wrong recipe	1	Only process engineers have authority to edit the recipe; wirebond recipe name rule align with bonding diagram no and rev;recipe modification approval system	Visual sample check (5) Sample PBI (5)		40	None					
			8		Mixed devices	1	Check the assembly shop order before lot start.and record the magazine number	Visual sample check (5) Sample PBI (5) PRS Auto alarm(2)	2	16	None					
			8		Wrong wire bond start sequence	2	Lock the " always" start from seleted wire function	Visual sample check (5) Sample PBI (5) PRS Auto alarm(2)	2	32	None					
		Mold flash/resin bleed(4) Electrical failure(8)	8		Index jamming	3	Equipped with detect sensor to prevent jamming. PM check index	Machine jam alarm(2) Non stick auto alarm (2) Visual sample check (5) Sample PBI (5)	2	48	None					

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							-						Action F				
Process	Potential Failure		S		Potential	О	C	Current Design/ Process	D		Recommended	Responsibility &		S			
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е		Action(s)	Target	Effective Date	E		Е	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
				S	of Failue												1
				S													1
			8		Window clamping	2	Technician check	Machine jam alarm(2)	2	32	None						
					and heat block		heat block under	Non stick auto alarm (2)									l
					issue		microscope	Visual sample check (5)									l
							quarterly and	Sample PBI (5)									l
							qualified technician										l
							can change heat										l
							block.										
			8		Leadframe quality	1		Machine jam alarm(2)	2	16	None						
					issue		check;	Non stick auto alarm (2)									l
								Visual sample check (5)									1
								Sample PBI (5)									l
								Function line test of									l
								Leadfram(5)									l
	Weak bond on pad		8		Insufficient heat	1	Check heat block	Buil blieur br C mointor(1)	4	32	None						
		failure(8)			transfer/downhold		quarterly	Wire pull SPC monitor(4)									l
		Reliability			er clamping												l
		failure(8)	8	*	Wafer/Die issue (	2	DI water cleaning	Ball shear SPC monitor(4)	1	64	None						$\vdash$
			0		Pad metal	_	during saw for	Wire pull SPC monitor(4)		04	None						l
					problems:big		wafer	Wafer incoming check(4)									l
					probe mark; pad		Walci	water meening eneek(1)									l
					scratch,contamina												l
					tion etc)												
			8	sk:	USG transfer	1	Calibrata immadanaa	Ball shear SPC monitor(4)	2.	16	None						$\vdash$
			٥		malfunction	1	when changing	Wire pull SPC monitor(4)	2	10	None						l
					manunction		capillary.	Machine auto alarm after									l
								capillary calibration fails(2)									l
							can change the	capitally canoration rans(2)									l
							capillary.										1
			1														l

Item:	SOIC16/28/32/54	41d							(	Contr	ol Number/Issue:	83MCT00002A/E	BY				
Type:	Design	_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FN	Л				
	Amanda Wang										FMEA Date:		(Orig.)				
Core Team:	Amanda Wang,H	I.J. Liu,Ivory Gu	o,JU	JN Y	ING ZHENG,XI	4OF	HUI KANG,SHUAN	N YAO,Cyndi Hu,Grayson	Ch	en,L	ANPING BAI,JIN	14-Nov-13	(Rev.)				
													Action I				
Process	Potential Failure	Potential	S	C	Potential	О	Current Design/	Current Design/ Process	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е	P	Action(s)	Target	Effective Date	Е	C	Ε	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
_				s	of Failue												ı
				s													i
			8	*	Capillary issue(	1	Check capillary type	Ball shear SPC monitor(4)	4	32	None						
					wrong type, life		in TCM and B/D.	Wire pull SPC monitor(4)									i
					etc)		Capillary life is										i
							locked in recipe.										i
			8	*	Improper wire	2	Lock key parameters	Ball shear SPC monitor(4)	4	64	None						
					bond parameters	_		Wire pull SPC monitor(4)	_	04	rone						i
					cona parameters		above can change	, no pan or e monter(1)									i
							the parameters;										i
							check parameters in										ı
							TCM										l
			Q	*	Floating	3	Setup check.	Ball shear SPC monitor(4)	2	48	None						
			0		leadframe(Flag)on	,		Wire pull SPC monitor(4)	_	70	None						ı
					heat block.			Sample PBI (5)									ı
					neur oroem		and teach bond.	Machine auto alarm when									ı
								vacuum out of control(2)									<u> </u>
			8		Cu wire oxidation	4		Ball shear SPC monitor(4)	2	64	None						i
			1				and work life	Wire pull SPC monitor (4)									i '
							control;	Machine auto alarm when									1 '

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forming gas flow out of

Material system auto alarm when Cu wire expired shelf life or work life(2)

control(2)

Forming gas flow

monitor(auto)

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								Action Results									
Process	Potential Failure		S		Potential	О		Current Design/ Process			Recommended	Responsibility &					
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е	P	Action(s)	Target	Effective Date	Е	C	Е	I
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
				S	of Failue											ı	
				S													
	Weak bond on	Electrical	8	*	Head Block and	2	Technician check	Visual sample check (5)	4	64	None						
	lead(( Stitch bond	` '			window clamping		heat block under	Sample PBI (5)									
	deformation,	Reliability			malfunction		microscope	Wire peel test (4)									
	peeling, crack	failure(8)					quarterly and									ı	
	etc)						qualified technician can change heat									ı	
							block									l	
			8	*	USG transfer	1	Calibrate impedance	Visual sample check (5)	2	16	None					ı	
					malfunction		when changing	Sample PBI (5)								ı	
							capillary.  Qualified technician	Wire peel test (4) Machine auto alarm after								ı	
							can change the	capillary calibration fails(2)									
							capillary.	capillary canoration rans(2)									
							cupinary.									ı	
					G 111 1 /		Cl. 1 '11 .	TT' 1 1 1 (5)		22	3.7				_	$\blacksquare$	
			8	*	Capillary issue(	1	Check capillary type in TCM and B/D.	Visual sample check (5) Sample PBI (5)	4	32	None					ı	
					wrong type, life etc)		Capillary life is	Wire peel test (4)								ı	
					cic)		locked in recipe.	whe peer test (4)								ı	
							1										
			8	*	Improper wire	2	Lock key parameters		4	64	None						
					bond parameters		and technician or	Sample PBI (5)								ı	
							above can change	Wire peel test (4)									
							the parameters; check paramters in										
							TCM									ı	
							I CIVI									, 1	

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													Action F				
Process	Potential Failure	Potential	S		Potential	О	C	Current Design/ Process			Recommended	Responsibility &	Actions Taken &				
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е		Action(s)	Target	Effective Date			Е	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
				s	of Failue												
				s													
			8	*	Leadframe defect	2	Preserve leadframe	Visual sample check (5)	4	64	None						
					before wire bond		in cabinet well with	Sample PBI (5)									
					(contamination,		N2 gas protection.	Wire peel test (4)									
					oxidization, lead		Hand free method										
					damage, foreign		during sample										
					matter, etc. )		checking										
							Function line test										
							and pick out the defect lead frame										
							Machine cover										
							above work holder										
							Use pre-wire										
							bonding plasma										
							clean										
			8	*	Insufficient heat	1	Check heat block	Visual sample check (5)	4	32	None						
					transfer/downhold		quarterly	Sample PBI (5)									
				ļ. —	er clamping			Wire peel test (4)									
			8		Improper second	1	Locked second bond	Visual sample check (5)	4	32	None						
					bond position		position in recipe	Wire peel test(4)									
			8	*	Mishandling	2	Operators follow	Visual sample check (5)	4	64	None						
					operation( load		SOP and WI	Sample PBI (5)									
					magazine, unit			Wire peel test(4)									
					inspection,wire												
			8	sk	change etc) Excessive epoxy	2	Set dispense	Visual sample check (5)	2	48	None						<u> </u>
			0		Excessive epoxy	3	parameter per	Setup check before W/B(4)		40	none						
							positrol log	OBC/ODC auto alarm(2)									
							check epoxy	OBC/OBC auto ararm(2)									
							expiration date										
			8	*	Foreign matter	2	Monthly cleaning	Visual sample check (5)	4	64	None						
							wire bonder index	Sample PBI (5)									
					<u>l</u>		İ	Wire peel test(4)									

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	_												Action F				
Process	Potential Failure		S		Potential	О	~	Current Design/ Process				Responsibility &					
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е		Action(s)	Target	Effective Date		C		
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
				S	of Failue												
				s													
			8		Cu wire oxidation	4	Cu wire shelf life	Ball shear SPC monitor(4)	2	64	None						
							and work life	Wire pull SPC monitor (4)									
							control;	Machine auto alarm when									
							Forming gas flow	forming gas flow out of									
							monitor(auto)	control(2)									
								Material system auto alarm when Cu wire expired shelf									
								life or work life(2)									
								ine of work ine(2)									
		Electrical	8		Wafer incoming	2	DI water cleaning	Visual sample check (5)	5	80	None						
		failure(8)			issue		during saw	Sample PBI (5)									
	1 7 1	Reliability															
	ect)	failure(8)	8		Wire clamper	2	Wire clamp PM	Visual sample check (5)	5	80	None						
			0		issue(	_	quarterly	Sample PBI (5)	5	80	TVOIC						
					tight,contaminatio		quarterry	Sumple I BI (5)									
					n,worn out etc)												
					,												
			8		Mishandling of	2	Standard operation	Visual sample check (5)	5	80	None						
					wire( removing bond off wires,		following WI	Sample PBI (5)									
					wire theading etc)												
					wire theading etc)												
			8		Epoxy on lead or	2	Die bond fillet	Visual sample check (5)	5	80	None						
					die		height and resin	Sample PBI (5)									
							bleed control										

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY	
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM	
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)	
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XL	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)	

	-												Action F				
Process	Potential Failure		S		Potential	О	C	Current Design/ Process				Responsibility &					
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е		Action(s)	Target	Effective Date		$\mathbf{C}$	Е	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	$\mathbf{C}$	T	N
				S	of Failue												
				S													
			8		Particles in air	2	Operation following	Visual sample check (5)	5	80	None						
							FE cleaning room	Sample PBI (5)									
							SOP										
	Non stick on pad	Electrical failure	8		Insufficient heat	1	Check heat block	Non stick auto alarm(2)	2	16	None						
	1	(8)			transfer/downhold		quarterly	Ball shear SPC monitor(4)									
					er clamping		· ·	Wire pull SPC monitor(4)									
			8		Wafer/die issue (	2	DI water cleaning	Ball shear SPC monitor(4)	2	32	None						
					Pad metal		during saw for	Wire pull SPC monitor(4)									
					problems:big		wafer	Wafer incoming check(4)									
					probe mark; pad scratch,contamina			Non stick auto alarm(2)									
					tion etc)												
			8		USG transfer	1	Calibrate impedance	Ball shear SPC monitor(4)	2	16	None						
					malfunction		when changing	Wire pull SPC monitor(4)									
							capillary.	Machine auto alarm after									
							Qualified technician	capillary calibration fails(2)									
							can change the	Non stick auto alarm(2)									
							capillary.										
			8		Capillary issue(	1		Ball shear SPC monitor(4)	2	16	None						
					wrong type, life		in TCM and B/D.	Wire pull SPC monitor(4)									
					etc)		Capillary life is locked in recipe.	Non stick auto alarm(2)									
							locked in recipe.										
			8		Improper wire	2		Ball shear SPC monitor(4)	2	32	None		_				
					bond parameters		and technician or	Wire pull SPC monitor(4)									
							above can change	Non stick auto alarm(2)									
							the parameters;										
							check paramter in										
							TCM										

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)
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													Action F				
Process	Potential Failure		S	C	Potential	О	C	Current Design/ Process			Recommended	Responsibility &	Actions Taken &				
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е		Action(s)	Target	Effective Date	Е		Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
				s	of Failue												
				S													
			8		Floating	2	Setup check.	Buil blieur bi C mointer(1)	2	32	None						
					leadframe(Flag)			Wire pull SPC monitor(4)									
					on heat block.		do the conversion	Machine auto alarm when									
							and teach bond.	vacuum out of control(2)  Non stick auto alarm(2)									
			8		Cu wire oxidation	4	Cu wire shelf life		2	64	None						
							and work life	Wire pull SPC monitor(4)									
							control;	Machine auto alarm when									
							Forming gas flow	forming gas flow out of									
							monitor(auto)	control(2) Material system auto alarm									
								when Cu wire expired shelf									
								life or work life(2)									
								Non stick auto alarm(2)									
	Non stick on lead	Electrical failure	8		Head Block and	2	Technician check	Visual sample check (5)	2	32	None						
		(8)			window clamping		heat block under	Sample PBI (5)									
					malfunction		microscope	Wire peel test (4)									
							quarterly and	Non stick auto alarm(2)									
							qualified technician can change heat										
							block										
			8		USG transfer	1	Calibrate impedance	1 · · · · · · · · · · · · · · · · · · ·	2	16	None						
					malfunction		when changing	Sample PBI (5)									
							capillary. Qualified technician	Wire peel test (4) Machine auto alarm after									
							can change the	capillary calibration fails(2)									
							capillary.	Non stick auto alarm(2)									
								2.2.2.2.2.2.2.2.2.2.2.2.2.2.2.2.2.2.2.									
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Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI.	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)

Requirements														Action F				
Requirements   Failure   V   a   Mechanism(s)   C   Prevention   S   Of Failue   S   Of Fail	Process	Potential Failure			C			~										
s of Failue s Capillary issue( wrong type, life etc)  8 Improper wire bond parameters  8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)  8 Leadframe defect ad frame damage,etc.)  1 Check capillary type (isoual sample check (5) sample PBI (5) wire peet lest (4) (and the parameters) (isoual sample check (5) sample PBI (5) wire parameters)  8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)  8 Leadframe defect ad frame damage,etc.)  8 Leadframe defect ad frame wire peet lest (4) (isoual sample check (5) wire peet lest (4) (is		Mode			1	Cause(s)/			Controls Detection			Action(s)		Effective Date			E	P
8 Capillary issue( wrong type, life etc)  8 Improper wire bond parameters  8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)  8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)  8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)  8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)  8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)  8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)	Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
8 Capillary issue( wrong type, life etc)  8 Improper wire bond parameters  8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)  9 Lecking ample check (5) and technician or above can change the parameters yellow (contamination, oxidization, lead damage,etc.)  1 Preserve leadframe and pick out the defect lead frame Machine cover and pick out the defect loss and pick out the defect loss and pick out the defect loss and lead, only for bga, lags snow, leaded dam, only for bga, lags snow, leaded dam, only for bga, lags snow, leaded dam, only for bga, lags snow, leaded dam, only for bga, lags snow, leaded dam, only for bga, lags snow, leaded dam, only for bga, lags snow, leaded dam, only for bga, lags snow, leaded dawn, and the converse of the check (5) and the check (5					S	of Failue												
wrong type, life etc)  in conversion checklist and B/D.  Capillary life is locked in recine bond parameters  in check by parameters and technician or above can change the parameters; check parameter in TCM  Item of the parameter in to the fore wire bond (contamination, oxidization, lead damage.etc.)  Item of the parameter in to the fore wire bond (contamination, oxidization, lead damage.etc.)  Item of the parameter in to the fore wire bond (contamination, oxidization, lead damage.etc.)  Item of the parameter in to the fore wire bond (contamination, oxidization, lead damage.etc.)  Item of the parameter in to the parameter in the p					S													
etc)  checklist and B/D. Capillary life is  Improper wire bond parameters bond parameters and technician or above can change the parameters; check parameter in TCM   8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)  8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)  8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)  8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)  8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)  8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)  8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)  8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)  8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)  9 Preserve leadframe Wisual sample check (5) Sample PBI (5) Wire peel test (4) Non stick auto alarm(2)  Wire peel test (4) Non stick auto alarm(2)  None  8 None  8 None  8 None  9				8			1		Visual sample check (5)	2	16	None						
Sample   Part   Capillary life is   Non stick auto alarm(2)   Capillary life is   Non stick auto alarm(2)   Capillary life is   Non stick auto alarm(2)   Capillary life is   Non stick auto alarm(2)   Capillary life is   Non stick auto alarm(2)   Capillary life is   Non stick auto alarm(2)   Capillary life   C						wrong type, life												
South   Cocked in recipe   Clock   Cock   Cocked   Cock						etc)												
Improper wire bond parameters   2   Lock key parameters and technician or above ean change the parameters; check parameter in TCM   Non stick auto alarm(2)   Sample PBI (5)   Wire peel test (4)   Non stick auto alarm(2)   No									Non stick auto alarm(2)									
bond parameters above can change the parameters; check paramter in TCM Wire peel test (4) Wire peel test (4) Non stick auto alarm(2) Sample PBI (5) Non stick auto alarm(2) Sample PBI (5) None to store wire bond (contamination, oxidization, lead damage.etc.) Sample PBI (5) Wire peel test (4) Non stick auto alarm(2) Sample PBI (5) None to store wire bond during sample checking Function line test and pick out the defect lead frame Machine cover above work holder Use pre-wire bonding plasma clean, (only for bga, Jga sony, leaded				8		Improper wire	2	Lock key parameters	Visual sample check (5)	2	32	None						
the parameters; check paramter in TCM  8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)  1 Parameters; check paramter in TCM  8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)  1 Preserve leadframe in cabinet well with N2 gas protection.  1 Hand free method during sample checking  1 Function line test and pick out the defect lead frame Machine cover above work holder Use pre-wire bonding plasma clean, (only for bga, lga sony, leaded)  1 Dreserve leadframe Visual sample check (5) (5) (2) (32) (32) (32) (32) (33) (33) (34) (34) (34) (34) (34) (34																		
check paramter in TCM  8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)  1						_		above can change	Wire peel test (4)									
8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)  1 Preserve leadframe in cabinet well with N2 gas protection. Hand free method during sample checking Function line test and pick out the defect lead frame Machine cover above work holder Use pre-wire bonding plasma clean.(only for bga ,lga sony, leaded									Non stick auto alarm(2)									
8 Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)  1 Preserve leadframe in cabinet well with N2 gas protection. Hand free method during sample checking Function line test and pick out the defect lead frame Machine cover above work holder Use pre-wire bonding plasma clean. (only for bga] Iga sony, leaded																		
before wire bond (contamination, oxidization, lead damage,etc.)  In cabinet well with N2 gas protection. Wire peel test (4)  Hand free method during sample checking Function line test and pick out the defect lead frame Machine cover above work holder Use pre-wire bonding plasma clean.( only for bga]  Jaga sony, leaded								TCM										
(contamination, oxidization, lead damage,etc. )  N2 gas protection. Hand free method during sample checking Function line test and pick out the defect lead frame Machine cover above work holder Use pre-wire bonding plasma clean.(only for bga ,lga sony, leaded				8		Leadframe defect	2			2	32	None						
oxidization, lead damage,etc.)  Hand free method during sample checking Function line test and pick out the defect lead frame Machine cover above work holder Use pre-wire bonding plasma clean.( only for bga ,lga sony, leaded						before wire bond												
damage,etc.)  during sample checking Function line test and pick out the defect lead frame Machine cover above work holder Use pre-wire bonding plasma clean.( only for bga ,lga sony, leaded						,		- 1										
checking Function line test and pick out the defect lead frame Machine cover above work holder Use pre-wire bonding plasma clean.( only for bga ,lga sony, leaded						· · · · · · · · · · · · · · · · · · ·			Non stick auto alarm(2)									
Function line test and pick out the defect lead frame Machine cover above work holder Use pre-wire bonding plasma clean.( only for bga ,lga sony, leaded						damage,etc.)												
and pick out the defect lead frame Machine cover above work holder Use pre-wire bonding plasma clean.( only for bga ,lga sony, leaded																		
defect lead frame Machine cover above work holder Use pre-wire bonding plasma clean.( only for bga ,lga sony, leaded																		
Machine cover above work holder Use pre-wire bonding plasma clean.( only for bga ,lga sony, leaded																		
above work holder Use pre-wire bonding plasma clean.( only for bga ,lga sony, leaded																		
bonding plasma clean.( only for bga ,lga sony, leaded																		
clean.( only for bga ,lga sony, leaded								Use pre-wire										
,lga sony, leaded																		
																		1
pkgs)				0		T CC' 1 1 1			77' 1 1 1 1 (6)	_	17	<b>&gt;</b> 7						
8 Insufficient heat transfer/downhold transfer/downhold quarterly Visual sample check (5) 2 16 None Sample PBI (5)				8			1			2	16	None						
transfer/downhold quarterly Sample PBI (5) er clamping Wire peel test (4)								quarterry										
Non stick auto alarm(2)						ci ciamping												

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI.	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)

												_	Action F			
Process	Potential Failure		S	С	Potential	О	C	Current Design/ Process	D		Recommended	Responsibility &	Actions Taken &		O	
Function/ Requirements	Mode	Effect(s) of Failure	E V	1 a s	Cause(s)/ Mechanism(s) of Failue	C C	Process Controls Prevention	Controls Detection	E T	P N	Action(s)	Target Completion Date	Effective Date	E V	C C	
			8	S	Cu wire oxidation	4	Cu wire shelf life and work life control; Forming gas flow monitor(auto)	Wire peel test (4) Machine auto alarm when forming gas flow out of control(2) Material system auto alarm when Cu wire expired shelf life or work life(2) Non stick auto alarm(2)	2	64	None					
		Eletrcial failure (8)	8		Improper wire bond parameters	2	Lock key parameters and technician or above can change the parameters; check parameter in TCM	Visual sample check (5) Sample PBI (5)	5	80	None					
	used	Reliability failure(8) Electrical failure(8)	8		Mishandling on wrong wire type	1	Follow assembly shop order and SFC system control	SFC auto alarm when material part number not match with system record(2)	2	16	None					
		Electrical failure(8) Reliability failure(8)	8		Incorrect parameters on first bond and loop formation	2	Lock loop parameters; Lock key parameters and technician or above can change the parameters; Check paramters in TCM	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None					
5.1 Pre-mold blasma clean	cleanliness	Delamination after mold(6) Reliability issue(8)	8		Plasma generator malfunction	2	Quarterly PM	Machine auto alarm (2) Measure contact angle on die and Leadframe(5)		32	None					

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	SOIC16/28/32/5					_						83MCT00002A/E						-
		_x_ Process						Company,	Gro	up,Si		Freescale, TJN-FN						_
Prepared By:	Amanda Wang					_					FMEA Date:		(Orig.)					
Core Team:	Amanda Wang,F	I.J. Liu,Ivory Gu	o,JU	N Y	ING ZHENG,XI	4OF	HUI KANG,SHUA	N YAO,Cyndi Hu,Grayson	Ch	en,L	ANPING BAI,JIN	14-Nov-13	(Rev.)					
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																		İ
													Action F	Resu	lts			۰
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/ Process	D	R	Recommended	Responsibility &	Actions Taken &	S	0	D	R	•
Function/	Mode	Effect(s) of	E	1	Cause(s)/	C	_	Controls Detection	E		Action(s)	Target	Effective Date	Ē				
Requirements	Wiode	Failure	V	a	Mechanism(s)	C		Controls Detection	T	N	7 Iction(s)	Completion Date	Effective Bute	V		T		
Requirements		ranuic	*		of Failue		1 icvention		1	11		Completion Date		٧		1	11	
				S	of Failue													
				S														
			8		No/Insufficient	2	Quarterly PM	Machine auto alarm (2)	2	32	None							
					gas/Vaccum			Measure contact angle on die										
C M 11	M 1 / CC	D 1		-	N. 11 1	2	II 10 1 DM	and Leadframe(5)	4	48	NT.							_
6. Mold	Mismatch / off-	Package	О		Mold chase top	2	Half-yearly PM	First-piece check by	4	48	None							
	center	chip/crack (6)			and bottom cavity mismatch.			microscope (4)										
			6		Location pin & set	2	Half-yearly PM	First-piece check by	4	48	None							-
			U		block worn out	_	Train-yearry 1 ivi	microscope (4)	_	70	TVOIC							
					block worll out			пистозсорс (4)										
	Wire damaged	Electrical failure.	8		Loader catch	2	Monthly PM	First-piece check by X-ray	2	32	None							•
		(8)			hooker			(4)										
		Reliability defect			misalignment			Sampling check by X-ray(5)										
		(8)						Machine auto alarm(2)										
																		_
			8		Incorrect input	2	Monthly PM	First-piece check by X-ray	2	32	None							
					buffer pusher			(4)										
					position			Sampling check by X-ray(5)										
								Machine auto alarm(2)										
			8		Incorrect input	2	Monthly PM	First-piece check by X-ray	2	32	None							
			0		buffer pusher	_	Wionumy 1 Wi	(4)	_	32	None							
					position			Sampling check by X-ray(5)										
					position			Machine auto alarm(2)										
								Machine auto alami(2)										
			8		Magazine falls on	2	Follow standard	First-piece check by X-	4	64	None							٠
					floor and wire is		handling requirment	ray(4)										
					touched by	I		Sampling check by X-ray(5)						l				
					operator	I								l				
			Ш						_						Щ	Щ		-
			8		Loader does not	2	Monthly PM	First-piece check by X-	2	32	None			l				
					catch lead frame			ray(4)										
		]			well			Sampling check by X-ray(5)		l								

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Machine auto alarm(2)

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)
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													Action F		lts		
Process	Potential Failure	Potential	S	C	Potential	О		Current Design/ Process			Recommended	Responsibility &					
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е	P	Action(s)	Target	Effective Date		C	Е	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
				s	of Failue												
				s													
	Mold flash/ resin	Electrical	8		Foreign matter on	2	Trial run dummy	First-piece check by	3	48	None						
	bleed	failure(8)			mold cavity		after mold cleaning	microscope (4)									
		Solderability					and conditioning;	Sampling check (5)									
		failure (8)					Clean vacuum box	100% final visual inspection									
							shiftly;	(3)									
							Change										
							pot&plunger while										
							worn out										
			8		Expose pad is	2	Monthly PM;	First-piece check by	3	48	None						
					deformed before		Follow standard	microscope(4)									
					molding		handling	Sampling check(5)									
							requirement	100% final visual inspection									
								(3)									
			8		Incorrect mold	2	Set up parameter per	r not proce encourery	2	32	None						
					parameters setting		TCM	microscope(4)									
								Sampling check(5)									
								100% final visual									
								inspection(3)  Machine auto alarm(2)									
			8		Load strip in	2	Monthly PM		2	32	None						
					wrong position			microscope (4)									
								Sampling check (5)									
								100% final visual inspection									
								(3)									
	F 4 1	77' 1 ' (/A)	1		т ,	_	G	Machine auto alarm (2)	2	1.6	NI						
	External	Visual reject(4)	4		incorrect process	2	Set up parameter per TCM	That piece check by	2	16	None						
	void/Incomplete fill				parameters setting		I CIVI	microscope (4) Sampling check (5)									
	11111							100% final visual									
								inspection(3)									
								Machine auto alarm (2)									

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI.	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)

							-					_	Action F				
Process	Potential Failure	Potential	S		Potential	О	C	Current Design/ Process	D		Recommended	Responsibility &	Actions Taken &		О		
Function/	Mode	Effect(s) of	E	1	Cause(s)/	C	Process Controls	Controls Detection	Е	P	Action(s)	Target	Effective Date		C		
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	Т	N
				s	of Failue											l	
				s												l	
			4		Air vent block	2	Perform mold	First-piece check by	3	24	None						
							cleaning and	microscope(4)								l	
							conditioning daily at	Sampling check(5)								l	
							least;	100% final visual								l	
							Trial run dummy	inspection(3)								l	
							after cleaning and									l	
			4		Runner block	2	Perform mold	First-piece check by	3	24	None				_	$\vdash$	+
							cleaning and	microscope (4)		-	- 1 - 1 - 1					l	
							conditioning	Sampling check (5)								l	
							regularly daily at	100% final visual								l	
							least;	inspection(3)								l	
							Trial run dummy									l	
							after cleaning and									l	
			4		Plunger jam	2	Monthly PM	First-piece check by	2	16	None					$\vdash$	t
					. 8. 3		J	microscope (4)								l	
								Sampling check (5)								l	
								100% final visual								l	
								inspection(3)								l	
			4		M 11 '. '	2	D C 11	Machine auto alarm (2)	4	32	N.T.					$\vdash$	╄
			4		Mold cavity is dirty	2	Perform mold cleaning and	First-piece check by	4	32	None					l	
					dirty		conditioning daily at	microscope (4)								l	
							least;	100% final visual								l	
							Trial run dummy	inspection(3)								l	
							after cleaning and	mspection(3)								l	
							conditioning									$\vdash$	┖
			4		Gate insert block	2	Perform mold	First-piece check by	4	32	None					l	
							cleaning and	microscope (4)								l	
							conditioning daily at									l	
							least;	100% final visual								l	
							Trial run dummy	inspection(3)								l	
							after cleaning and									l	

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)
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													Action F	Resu	lts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/ Process	D	R	Recommended	Responsibility &	Actions Taken &	S	O	D	R
Function/ Requirements	Mode	Effect(s) of Failure	E V	l a s	Cause(s)/ Mechanism(s) of Failue	C C	Process Controls Prevention	Controls Detection	E T	P N	Action(s)	Target Completion Date	Effective Date	E V			P N
			4		Use expired or unthawy compound	2	Genesis system control	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection(3) System alarm (2)	2	16	None						
			4		Unsuitable Tablet size	2	Tablet length sensor check		2	16	None						
			4		Mold die temperature out of control	2	Real time PID control	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection(3) Machine auto plant (2)	2	16	None						
			4		Inproper eject pin dimension	3	PM check the matching(type, dimension etc.) before eject pin chane. Clean the eject pin holder and mold chase basic board monthly		3	36	None						
			4		Use wrong type compound	2	Clean out the compound when compound is converted,then double check by operator/leader; Genesis system	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection(3) System alarm(2)	2	16	None						

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XIA	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)
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													Action F				
Process	Potential Failure	Potential	S	C	Potential	Ο	Current Design/	Current Design/ Process			Recommended	Responsibility &	Actions Taken &				
Function/	Mode	Effect(s) of	E	1	Cause(s)/	C	Process Controls	Controls Detection	Е		Action(s)	Target	Effective Date		C	E	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
				S	of Failue												l
				S													
		Electrical failure	8		Incorrect process	2		First-piece check by X-ray	2	32	None						
		(8)			parameter		TCM	(4)									ı
								Sampling check by X-ray (5)									
								Machine auto alarm (2)									1
			8		Use expired or	2	Genesis system	First-piece check by X-ray	4	64	None						
					unthawy		control	(4)									ı
					compound			Sampling check by X-ray (5)									
			8		Use expired or	2	Genesis system	First-piece check by X-ray	4	64	None						
					unthawy		control	(4)									ı
					compound			Sampling check by X-ray (5)									
			8		Magazine falls on	2	Follow standard	First-piece check by X-ray	4	64	None						
					floor and wire		handling requirment										ı
					touched by			Sampling check by X-ray (5)									ı
			8		operator Magazine falls on	2	Follow standard	First-piece check by X-ray	4	64	None						-
					floor and wire		handling requirment										
					touched by			Sampling check by X-ray (5)									ı
			0		operator M. 11.1:	2	D 14' DID	F' 4 ' 1 11 V	2	22	NI						
			8		Mold die temperature out of	2	Real time PID	r not piece encen of 11 fag	2	32	None						ı
					control		control	(4) Sampling check by X-ray (5)									ı
					control			Machine auto alarm(2)									ı
								. ,									
			8		Mold die	2	Real time PID	That piece eneck by 11 ray	2	32	None						ı
					temperature out of		control	(4)									
					control			Sampling check by X-ray (5)									
								Machine auto alarm(2)									

Item: SOIC16/28/32/54ld	Control Number/Issue: 8	3MCT00002A	/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: I	Freescale,TJN-F	FM
Prepared By: Amanda Wang	FMEA Date:	05-Oct-94	(Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XIA	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN	14-Nov-13	(Rev.)
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													Action F		lts		
Process	Potential Failure	Potential	S	C	Potential	О	Current Design/	Current Design/ Process			Recommended	Responsibility &					
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е	P	Action(s)	Target	Effective Date		$\mathbf{C}$		
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	$\mathbf{C}$	Т	N
				s	of Failue												
				s													
			8		Use wrong type	2	Clean out the	First-piece check by X-ray	2	32	None						
					compound		compound when	(4)									
							compound is	Sampling check by X-ray (5)									
							converted,then	System alarm(2)									
							double check by										
							operator/leader;										
							Genesis system										
	Pitting	Visual reject (4)	4		Mold die	2	Real time PID	First-piece check by	2	16	None						
					temperature out of		control	microscope (4)									
					control			Sampling check (5)									
								100% final visual									
								inspection(3)									
			4		A :	2	Df14	Machine auto alarm(2)	3	24	None						
			4		Air vent block	2	Perform mold cleaning and	First-piece check by	3	24	None						
								microscope (4) Sampling check (5)									
							least;	100% final visual									
							trial run dummy	inspection(3)									
							after cleaning and	mspection(3)									
							conditioning										
			4		Air vent block	2	Perform mold	First-piece check by	3	24	None						
							cleaning and	microscope (4)									
							least;	100% final visual									
							trial run dummy	inspection(3)									
							after cleaning and										
			4		Incorrect process	2	Set up parameter per	First-piece check by	2	16	None						
					parameters setting		TCM	microscope (4)									
								Sampling check (5)									
								100% final visual									
								inspection(3)									
	1	<u> </u>	1				l	Machine auto alarm (2)		<u> </u>							

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI.	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)

													Action F				
Process	Potential Failure	Potential	S	C	Potential	О	Current Design/	Current Design/ Process			Recommended	Responsibility &	Actions Taken &				
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е		Action(s)	Target	Effective Date	Е		Е	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date	!	V	C	T	N
				s	of Failue								!				l
				s									!				l
			4		Incorrect process	2	Set up parameter per	First-piece check by	2	16	None		l				
					parameter setting		TCM	microscope (4)					!				i
								Sampling check (5)					!				l
								100% final visual					!				l
								inspection(3) Machine auto alarm (2)					!				l
			4		Mold chase cavity	2	Perform cleaning		3	24	None						
					is dirty		and conditioning	microscope (4)					!				l
							daily at least;	Sampling check (5)					!				l
							trial run dummy	100% final visual					!				l
							after cleaning and	inspection(3)					!				l
			4		Mold chase cavity	2	Conditioning Perform cleaning	First-piece check by	3	24	None						<del>                                     </del>
					is dirty	_	and conditioning	microscope (4)	5	2-7	Tronc		!				l
							daily at least;	Sampling check (5)					!				l
							trial run dummy	100% final visual					!				l
							after cleaning and	inspection(3)					!				l
	Package	Visual reject (4)	8		Eject pin worn out	2	Conditioning Half-yearly PM	First-piece check by	3	48	None		<u> </u>				-
	protrusion	Solderability(8)	0		Eject pili worli out	_	riani-yeariy rivi	microscope (4)	3	40	None		!				i
	protrusion	Solder ability (6)						Sampling check (5)					!				l
								100% final visual					!				l
								inspection(3)									
	1 0 1	Visual reject (4)	8		Use wrong mold	1	To verify the	First-piece check by	2	16	None		!				l
		Customer difficult			chase		package dimension	microscope (4)					!				l
	tool	application(8)					before production	Machine auto Alarm(2)					!				l
							start; Loader with						!				l
							different sensors to						!				l
							identify different										l
	Mold Package	Reliability	8		Improper degator	2.	Monthly PM	Sampling check by	5	80	None		<del> </del>				$\vdash$
		failure(8)	ľ		position setting	ľ		microscope(5)		30	1.010						l
		Electrical						1 . (- /									
		failure(8)															i

Item:	SOIC16/28/32/54	4ld							(	Contr	ol Number/Issue:	83MCT00002A/E	BY				
	Design	_x_ Process						Company,				Freescale, TJN-FN					
	Amanda Wang										FMEA Date:		(Orig.)				
Core Team:	Amanda Wang,F	I.J. Liu,Ivory Gu	o,JU	N Y	ING ZHENG,XI	AOI	HUI KANG,SHUAI	N YAO,Cyndi Hu,Grayson	Ch	en,L	ANPING BAI,JIN	14-Nov-13	(Rev.)				
	T	T					_	T					Action I				
	Potential Failure	Potential	S		Potential	О	C	Current Design/ Process	D							D	
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C		Controls Detection	Е		Action(s)	Target	Effective Date	Е	C		
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
				S	of Failue												
				S													
			8		Mold cavity is too	2	Perform mold	Sampling check by	5	80	None						
					sticky		cleaning and conditioning daily at	microscope(5)									
							least										i
	Delamination	Reliability failure	8		Incorrect process	2	Set up parameter per	Regular CSAM inspection	2	32	None						
		(8)			parameters setting		TCM and check	(5)									
							oven temperature	Machine auto alarm (2)									
			8		Use expired or	2	shiftly Genesis system	Regular CSAM	2.	32	None						
					unthawy	ľ	control	inspection(5)	Ĩ	32	Trone						
					compound			System alarm(2)									
			8		Leadframe is over	2	Take out L/F	Regular CSAM inspection	5	80	None						i
					oxidated on mold		promptly while	(5)									
					die		equipement alarm										i
			8		Leadframe	1	N2 protection in	Regular CSAM	5	40	None						
					contaminated		storage area	inspection(5)									
			8		Plasma clean	2	Genesis system	System alarm(2)	2	32	None						i
			8		expiration Internal stress	2	control	Regular CSAM	5	80	None						
			0		caused by	_		inspection(5)		00	Trone						i
					Leadframe			1									
					warpage (Fused												
					leadframe												
					17ASH70187A61												i
			8		Use wrong type	2	Clean out the	Regular CSAM	2	32	None						
					compound		compound when	inspection(5)	1								1
							compound is	System alarm(2)	1								1
							converted,then		1								1
							double check by										1
			1	l			operator/leader;		1								

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Genesis system

POTENTIAL FA							RE MODE A	AND EFFECTS	Al	NA.	LYSIS (FM	IEA)	Page 4	9 o	f 61		
Item:	SOIC16/28/32/54	4ld							(	Contr	ol Number/Issue:	83MCT00002A/B	Y				
Type:	Design	_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FM	1				
Prepared By:	Amanda Wang										FMEA Date:	05-Oct-94	(Orig.)				
		I.J. Liu,Ivory Gu	o,JU	IN Y	ING ZHENG,XL	AOF	iui kang,shuai	N YAO,Cyndi Hu,Grayson	Ch	en,L	ANPING BAI,JIN	14-Nov-13	(Rev.)				
								•									
													Action F	Resu	ılts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/ Process	D	R	Recommended	Responsibility &	Actions Taken &	S	O	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е	P	Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		Т	N		Completion Date		V	C	T	N
				s	of Failue												
				s													
	Foreign matter in	Visual reject(4)	4		Compound	2	Try run dummy	Regular CSAM	5	40	None						
	package				residual around		after cleaning and	inspection(5)									
					pot		conditioning;										
							Clean vacuum box										
							shiftly;										
							Change										
							pot&plunger while										
ı							worn out Clean mold surface										
							post each shot by										
İ						I	auto cleaner										

Sampling check(5)

Sampling check(5)

Sampling check(5)

Sampling check(5)

Sampling check(5)

First-piece check by X-ray

Sampling check by X-ray (5)

System auto alarm(2)

Machine auto alarm (2)

24

60

24

60

60

None

None

None

None

None

None

Setup parameter per

ГСМ

control

manually

Perform mold

cleaning and conditioning daily at

Perform mold

cleaning and

conditioning regularly daily at

Trial run dummy after cleaning and

least;

Monthly PM

Genesis system

Forbid break cull

Cull remain

Internal void

package

chip/crack(6)

Reliability failure 8

Insufficient cure

Improper degator

position setting
Use expired or

time

unthawy

sticky

compound Operator break

cull manually

Runner block

Mold cavity is too 2

		POT	re:	NT	IAL FAIL	Ul	RE MODE A	AND EFFECTS	Αľ	NA]	LYSIS (FM	IEA)	Page 5	<sub>'</sub> U 01	61		
Item:	SOIC16/28/32/54	41d				_			(	Contr	ol Number/Issue:	83MCT00002A/B	Y				
Type:	Design	_x_ Process				_		Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FM	1				
Prepared By:	Amanda Wang					_					FMEA Date:	05-Oct-94	(Orig.)				
Core Team:	Amanda Wang,H	I.J. Liu,Ivory Gu	ıo,JU	JN Y	ING ZHENG,XI	AOI	HUI KANG,SHUAI	N YAO,Cyndi Hu,Grayson	Ch	en,L	ANPING BAI,JIN	14-Nov-13	(Rev.)				
													Action F				
Process	Potential Failure	Potential	S	C	Potential	О	Current Design/	Current Design/ Process	D	R	Recommended	Responsibility &	Actions Taken &	S	O	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е	P	Action(s)	Target	Effective Date	Е	C	E	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
				S	of Failue												
				s													
			8		Air vent block	2	Perform mold	First-piece check by X-ray	4	64	None						
							cleaning and	(4)									
							conditioning daily at	Sampling check by X-ray (5)									
							least;										
							Trial run dummy										
							after cleaning and										
			8		Gate insert block	2	Perform mold	First-piece check by X-ray	4	64	None						

Sampling check by X-ray (5)

First-piece check by X-ray

Sampling check by X-ray (5) Machine auto alarm(2) First-piece check by X-ray

Sampling check by X-ray (5) First-piece check by X-ray

Sampling check by X-ray (5) System auto alarm(2)

First-piece check by X-ray

Sampling check by X-ray (5) Machine auto alarm(2)

32

32

32

None

None

None

cleaning and

conditioning regularly daily at

Trial run dummy after cleaning and Mothly PM

Set up parameter per

Genesis system

Real time PID

least;

TCM

control

control

Plunger jam

Incorrect process parameter setting

Use expired

unthawy

compound

Mold die

control

temperature out of

compound or

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI.	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)

													Action I			
Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	S E V	C 1 a s s	Potential Cause(s)/ Mechanism(s) of Failue  Unsuitable tablet size	O C C		Current Design/ Process Controls Detection  First-piece check by X-ray (4) Sampling check by X-ray (5)	E T	P N	Recommended Action(s)	Responsibility & Target Completion Date	Actions Taken & Effective Date	C	D E T	P
			8		Use wrong type compound	2	Clean out the compound when compound is converted,then double check by operator/leader; Genesis system	Machine auto alarm(2)	2	32	None					
7. Marking		Reject by visual inspection or vision system(4)	4		L/F input sensor accidently disable.	1	Check L/F input sensor status shiftly, dummy L/F check by Assy. lot.	sensor auto alarm(2) Visual sample check after marking(5)100% final visual inspection(3)		8	None					
			4		Laser lamp broken.	1	Check the laser power value shiftly, dummy L/F check by Assy. lot.	Machine auto alarm(2) Visual sample check after marking(5)100% final visual inspection(3)	2	8	None					
		Reject by visual inspection or vision system(4)	4		wrong laser power	2	Check the laser power value shiftly, dummy L/F check by Assy. lot. Monthly change laser lamp.	Visual sample check after marking(5) QA visual inspection 200 units/lot(4) 100% final visual inspection(3)	3	24	None					
			4		low vacuum suck	1	Clean dust collector shiftly, dummy L/F check by Assy. lot.	Visual sample check after marking(5) QA visual inspection 200 units/lot(4) 100% final visual inspection(3)	3	12	None					

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY	
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM	
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)	
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XL	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)	

	-						_						Action F		lts		
Process	Potential Failure	Potential	S	C	Potential	О		Current Design/ Process			Recommended	Responsibility &	Actions Taken &		-		
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е	P	Action(s)	Target	Effective Date		C	Е	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
				s	of Failue												
				s													
	misalignment	Reject by visual	4		leadframe wrong	1	Dummy L/F check	Machine auto alarm(2)	2	8	None						
		inspection or			location		by Assy. lot.	Visual sample check after									
		vision system(4)					Check the	marking(5)100% final visual									
							orientation sensor	inspection(3)									
							shiftly.	QA visual inspection 200									
			1		Incorrect marking	3	Dummy marking	Visual sample check after	3	36	None						1
			4		parameters	3	before production	marking(5)100% final visual	3	30	None						
					settings		start	inspection(3)									
					settings		Start	QA visual inspection 200									
								units/lot(4)									
	reverse mark	Reject by visual	4		L/F orientation	2	Check the	Visual sample check after	3	24	None						
		inspection or			fail		orientation sensor	marking(5)100% final visual									
		vision system(4)					shiftly.	inspection(3)									
							dummy L/F check										
	crack	reliability	8		Lead fame jamed	1	hy Assy lot Check rail status.	sensor auto alarm(2)	2	16	None						1
	Clack	failure.(8)	0		on track.	1	dummy L/F check	Visual sample check after	_	10	None						
		ranuic.(6)			on track.		by Assy. lot.	marking(5)100% final visual									
							Regular PM.	inspection(3)									
	Wrong marking	Reject by visual	4		Auto marking	2	Marking	Visual sample check after	3	24	None						
		inspection or			information error		confirmation with	marking(5)									
		vision system(4)					dummy L/F by	QA visual inspection 200									
							Assy. lot.	units/lot(4)									
								100% final visual									
3. Post mold cure	Overcure	Reliability failure	8		Temperature	2	Set up parameter per	Visual check temperature	2	32	None						$\vdash$
		(8)			excursion		TCM and check	meter(6)			- 1 - 1 - 1						
		(-)					oven temperature	Machine auto alarm (2)									
							shiftly	, ,									
	Undercure	Reliability failure	8		Temperature	2	Set up parameter per	Visual check temperature	2	32	None						
		(8)			excursion		TCM and check	meter(6)									
							oven temperature	Machine auto alarm (2)									
							shiftly										丄

Item: SOIC16/28/32/54ld	Control Number/Issue: 83M	/ICT00002A/	/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Free	escale,TJN-F	FM
Prepared By: Amanda Wang	FMEA Date: 0	05-Oct-94	(Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XIA	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 1	14-Nov-13	(Rev.)

							_	-				_	Action I		lts		
Process	Potential Failure		S		Potential	О	Current Design/	e e			Recommended	Responsibility &				D	
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е		Action(s)	Target	Effective Date			Е	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
				s	of Failue											,	l
				s												,	i
			8		Insufficient cure	2	Check cure shiftly	Visual check temperature	2	32	None					П	l
					time		per TCM;	meter(6)								,	ł
			1				Mothly PM	Machine auto alarm (2)	_							,—/	<u> </u>
	Non Cure	Reliability failure	8		Missing PMC	1	Genesis system	System alarm(2)	2	16	None					,	ł
9. plating (not	bent lead	(8) Electrical Failure	8		load,unload jam	2	control Check Adjustment	Visual sample check after	2	32	None				_	$\dashv$	_
applicable for PPI		(8)	0		load,umoad jam	_	load and unload	plating(5)	_	32	Tronc					,	i
L/F)	•	(0)					system monthly &	Auto alarm(2)								,	i
							half-year by PM	` ,									<u></u>
			8		Jam in process	2	Check/Adjustment	Visual sample check after	2	32	None						ı
					cell		belt, air knivies	plating(5)								,	i
						_	monthly by PM	Auto alarm(2)	_	22				$\vdash$	_	$\blacksquare$	<u>—</u>
			8		Jam in high	2	Check rinse nozzle	Visual sample check after	2	32	None					,	i
					pressure water		monthly by PM;	plating(5) Auto alarm(2)								,	i
					rinse		Check per positrol	Auto aiarm(2)								,	ł
	discoloration &	Solderability	8		Insufficient air	1	Check air knives	Visual sample check after	5	40	None					一	
	stain	Failure(8)			knives flow		monthly by PM;	plating(5)								,	i
							Clean air nozzle and									,	i
							mechanical structure									,	i
							monthly by PM.									,	i
			8		Insufficient water	2	Check rinse nozzle	Visual sample check after	5	80	None				-	$\dashv$	_
			0		rinse	_	monthly by PM;	plating(5)	5	00	Tronc					,	l
					i i i i i i i i i i i i i i i i i i i		Check rinse per	plumg(3)								,	i
							setup checklist									,	i
							shiftly										
			8		THIS GITTIETE TO	2	Analyses and adjust	I	5	80	None					,	i
					additives		additive weekly.	plating(5)								,	i
	rough plating	Visual Defect(6)	8		Particles, anode	2	Replace filter	Visual sample check after	5	80	None					$\dashv$	$\overline{}$
		Solderability	1		sludge, dirty		elements at most	plating(5)								,	ı
		Failure (8)			<i>9.17</i> 1.7		2weeks									,	ı
			1				Filter plating									,	ı
							solution every									,	ı
							3months										

Item: SOIC16/28/32/54ld	Control Number/Issue: 8	3MCT00002A	/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: F	Freescale,TJN-F	FM
Prepared By: Amanda Wang	FMEA Date:	05-Oct-94	(Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN	14-Nov-13	(Rev.)
			Action Results

S (C) E : :	Cause(s)/ Mechanism(s)	O C C	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	D E T	R P	Recommended Action(s)	Responsibility & Target	Actions Taken & Effective Date				R
V	Mechanism(s) of Failue			Controls Detection			Action(s)	Target	Effective Date	Е	C	т-	
	of Failue	С	Prevention		т				Litective Date			Е	P
	3				1	N		Completion Date		V	C	T	N
3	Excessive current												
	Excessive carrent	2	Shiftly check	Visual sample check after	5	80	None						
			current per positrol	plating(5)									
2	Low metal	2	log Analysed the metal	Visual sample check after	5	80	None				$\dashv$	$\dashv$	
,		_	•		)	30	TVOILE						
	solution		shiftly	practing(b)									
3	Insufficient	1	Analyses and adjust	Visual sample check after	5	40	None						
	additive		additives weekly	plating(5)									
3	Improper acid	2	Analyses and adjust	Visual sample check after	5	80	None				1	十	
		ľ	content of the acid	_		00	TVOILE						
	solution		shiftly										
3		2		-	5	80	None						
	pretreatment		<u> </u>	plating(5)									
			log silitiy										
3	Higher tin	1	Tighten the	Chemical analysis shiftly(4).	4	32	None						
	electrolyte.		Pb-free electrolyte.										
3	Organic	2	Analyses carbon	Visual sample check after	5	80	None						
	contamination			plating(5)									
			conduct active										
3	Insufficient	2	Check and analyses	Visual sample check after	5	80	None				寸	一	
	pretreatment		•	-									
			solution per positrol										
			log shiftly										
3 3 3	3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	content of solution Insufficient additive  Improper acid content of plating solution insufficient pretreatment  Higher tin concentration in Pb-free electrolyte.  Organic contamination  Insufficient	content of solution  Insufficient additive  Improper acid content of plating solution  insufficient pretreatment  Higher tin concentration in Pb-free electrolyte.  Organic contamination  Insufficient 2  Insufficient 2  Insufficient 2  Insufficient 2	Low metal content of solution shiftly  Insufficient additive	Low metal content of solution shiftly  Insufficient additive  Improper acid content of plating solution  Improper acid content of plating solution  Insufficient additive  Improper acid content of plating solution  Insufficient pretreatment  Improper acid content of plating solution  Insufficient pretreatment  Insufficient plating(5)  Insufficient plating(5)  Insufficient plating(5)  Insufficient plating(5)  Insufficient plating(5)  Insufficient plating(5)  Insufficient plating(5)  Insufficient plating(5)	Low metal content of solution shiftly  Insufficient additive  Improper acid content of plating solution  Improper acid content of plating solution  Insufficient and insufficient  Insufficient pretreatment  Improper acid content of plating solution  Insufficient pretreatment  Insufficient plating(5)  I	Low metal content of solution shiftly  Insufficient additive  Improper acid content of plating solution  Improper acid content of plating solution  Insufficient pretreatment  Improper acid content of plating solution  Insufficient pretreatment  Improper acid content of plating solution  Improper acid content of plating solution  Improper acid content of the acid shiftly  Improper acid content of plating solution  Improper acid content of the acid shiftly  Improper acid content of the acid shif	Low metal content of solution shiftly  Insufficient additive  Improper acid content of plating solution  Insufficient pretreatment  Improper acid content of plating solution  Insufficient pretreatment  Improper acid content of plating solution  Improper acid content of plating solution  Improper acid content of plating solution  Improper acid content of the acid shiftly  Check and analyses the pretreatment solution per positrol log shiftly  Improper acid content of the acid shiftly  Improper acid content of the acid shiftly  Check and analyses the pretreatment solution per positrol log shiftly  Check and analyses the pretreatment of tin concentration for Pb-free electrolyte.  Chemical analysis shiftly(4).  Chemical analysis shiftly(4).  Chemical analysis shiftly(4).  Chemical analysis shiftly(4).  Chemical analysis shiftly(5)  None  None  None  None  None  None  Tighten the maintenance limit of tin concentration for Pb-free electrolyte.  Chemical analysis shiftly(5)  None  None  None  None  Visual sample check after plating(5)  None  Tighten the maintenance limit of tin concentration for Pb-free electrolyte.  Insufficient contamination  Insufficient pretreatment  Check and analyses the pretreatment solution per positrol  Visual sample check after plating(5)  Visual sample check after plating(5)  Visual sample check after plating(5)	Low metal content of solution solution solution Insufficient additive weekly additives weekly additives weekly content of plating solution solution additive weekly additives weekly additives weekly solution additive solution per positrol log shiftly  By a content of plating solution additive weekly additives weekly additives weekly additives weekly additives weekly additives weekly plating(5)  By a content of plating additives weekly additives weekly additives weekly additives weekly plating(5)  By a content of plating additives weekly additives weekly additives weekly additives weekly plating(5)  By a content of plating additives weekly additives weekly additives weekly additives weekly plating(5)  By a content of plating additives weekly addi	Low metal content of solution solution shiftly  Insufficient additive additives weekly additives weekly additives weekly solution solution solution  Improper acid content of plating solution solution solution solution additives weekly additives weekly additives weekly additives weekly plating(5)  Improper acid content of plating solution solution solution solution solution as insufficient pretreatment  Improper acid content of the acid shiftly visual sample check after plating(5)  Improper acid content of the acid shiftly visual sample check after plating(5)  Improper acid content of the acid shiftly visual sample check after plating(5)  Improper acid content of the acid shiftly visual sample check after plating(5)  Improper acid content of the acid shiftly visual sample check after plating(5)  Improper acid content of plating solution of the acid shiftly visual sample check after plating(5)  Improper acid content of the acid shiftly visual sample check after plating(5)  Improper acid content of the acid shiftly visual sample check after plating(5)  None  None  None  None  Chemical analysis shiftly(4). 4 32 None  Chemical analysis shiftly(4). 4 32 None  Tighten the maintenance limit of tin concentration for pb-free electrolyte.  Organic contamination  Organic contamination  Insufficient plating(5)  I	Low metal content of content of solution per positrol log shiftly  3 Higher tin concentration in Pb-free electrolyte.  3 Organic Contamination 2 Analyses carbon monthly and conduct active carbon reteatment solution per positrol solution per positrol solution solution solution solution solution solution solution solution solution solution solution solution solution per positrol solution solution per solution solution solution per solution solution solution solution solution solution solution per solution solutio	Low metal content of content of solution solution solution solution solution solution solution solution solution solution solution solution solution solution solution solution solution solution additives weekly additives weekly solution solution solution solution solution solution solution solution solution solution solution solution solution solution solution solution solution solution per positrol log shiftly  3	Low metal content of content of solution solution solution solution solution solution solution solution solution additives weekly additives weekly plating(5)  Improper acid content of plating content of plating solution  Improper acid content of plating solution  Improper acid content of plating solution  Improper acid content of plating solution  Improper acid content of plating solution  Improper acid content of the acid shiftly  Check and analyses the pretreatment solution per positrol log shiftly  Improper acid content of the acid shiftly  Improper acid content of the acid shiftly  Improper acid content of the acid shiftly  Improper acid content of the acid shiftly  Improper acid content of the acid shiftly  Improper acid content of the acid shiftly  Improper acid content of the acid shiftly  Improper acid content of the acid shiftly  Improper acid content of the acid shiftly  Implementation of the plating(5)  Improper acid content of the acid shiftly  Implementation of the acid shiftly  Implementation of the acid shiftly  Improper acid content of the acid shiftly  Implementation of the ac

Item: SOIC16/28/32/54ld	Control Number/Issue: 8	3MCT00002A/E	BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: F	reescale,TJN-FN	M
Prepared By: Amanda Wang	FMEA Date:	05-Oct-94	(Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI.	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN	14-Nov-13	(Rev.)
			•
		•	Action Results

													Action F				
Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	S E V	C 1 a	Potential Cause(s)/ Mechanism(s)	O C C	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	D E T		Recommended Action(s)	Responsibility & Target Completion Date	Actions Taken & Effective Date	S E V	C	D E T	R P N
				s s	of Failue												
		Solderability failure(8)	8		Insufficient Solution flowrate/ additive	1	Replace filter elements two weeks at most/Weekly Analyses additives weekly	1	5	40	None						Ī
			8		Foreign matter may resist the Tin deposit on lead frame	2	Clean water knife in plating solution cell weekly	·	5	80	None						
	peeling	Solderability failure(8)	8		pretreatment	2	Check and adjust the pretreatment solution per positrol log shiftly	palting(5)	5		None						
	1 1	Solderability failure(8)	8	*	metal composition	2	, ,	SPC control(4) Solderability sampling check(5)			None						
			8	*	Temperature is too high	1	Heaters & temperature system check monthly by PM; shiftly check bath temperature per positral log	SPC control(4) Solderability sampling check(5) Machine Auto alarm(2)	2		None						
			8	*	Improper current density	2	shiftly check current per positrol log	SPC control(4) Solderability sampling check(5)	4	64	None						
	improper thickness	Solderability failure(8)	8	*	Improper current density	3	shiftly check per positrol log	SPC control(4) Solderability sampling check(5) Auto alarm system to detect current range(2)	2	48	None						
			8	*	Insufficient anode balls	2	shiftly check per set- up check list	SPC control(4) Solderability sampling check(5)	4	64	None						

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)
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								-				_	Action R				
Process	Potential Failure	Potential	S	C	Potential	О	Current Design/	Current Design/ Process	D	R	Recommended	Responsibility &	Actions Taken &			D	
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е	P	Action(s)	Target	Effective Date	Ε	$\mathbf{C}$	Е	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	$\mathbf{C}$	T	N
				S	of Failue											l '	ĺ
				s												i '	ĺ
			8	*	Improper belt	1	shiftly check per	SPC control(4)	4	32	None					Π	
					speed		positrol log	Solderability sampling								l '	ĺ
					-			check(5)									
			8	*	Poor electrical	2	Shiftly check	SPC control(4)	2	32	None					l '	ĺ
					connection			Solderability sampling								l '	ĺ
							per set-up check list	check(5)Auto alarm system								l '	ĺ
								to detect poor electrical								i '	ĺ
								connection issue(2)								l '	ĺ
	Whiskers (Only	Electrical failure	8		Insufficient	2	Check and analyses	Sampling check(5)	4	64	None					Π	Г
	for lead-free)	(8)			descale			Chemical analysis shiftly(4).								l '	İ
							per positrol log	•								l '	ĺ
							shiftly;Post Plating									i '	İ
							Bake									l '	İ
			8		high carbon or	1	Check and analyses	Sampling check(5);Chemical	4	32	None						
			0		organic content	1		analysis shiftly(4).	4	32	None					l '	ĺ
					organic content		per positrol log	anarysis simuy(+).								l '	ĺ
							shiftly;									l '	ĺ
							Post Plating Bake									l '	İ
			8		riigii ilictai	2	Purify the plating	Sampling check(5);Analyse	4	64	None					l '	ĺ
					impurity		solution every 3	the metal impurity in bath								l '	ĺ
					content(Iron, lead		months; Monitor the	monthly(4)								l '	İ
					copper, nickel)		content of metal									l '	İ
			8		Incorrect current	2	impurity Check rectifier	Sampling check(5);Check	4	64	None			H		$\overline{}$	H
			ľ		density	ľ	current shiftly.	current shiftly(4)	ľ							l '	ĺ
			8		Improper	1	Check temperature	Machine Auto alarm(2)	2	16	None						
					temperature in		shiftly									l '	ĺ
					plating									Ш		<u> </u>	
			8		Insufficient	2	Check belt speed	SPC control(4)	4	64	None					i '	ĺ
					deposite thickness		and current density									l '	ĺ
	1						shiftly						<u> </u>				

	THE MODE IN (B ELLECTS IN METERS (11)		
Item: SOIC16/28/32/54ld	Control Number/Issue: 8	3MCT00002A/	BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: F	reescale,TJN-FI	M
Prepared By: Amanda Wang	FMEA Date:	05-Oct-94	(Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XIA	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN	14-Nov-13	(Rev.)
			Action Results

													Action F	Resu	lts		
Process	Potential Failure	Potential	S	C	Potential	O	Current Design/	Current Design/ Process	D	R	Recommended	Responsibility &	Actions Taken &	S	O	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е	P	Action(s)	Target	Effective Date	Е	$\mathbf{C}$	Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	$\mathbf{C}$	T	N
				s	of Failue												
				s													
10. plating gate	overcure	electrical	8		wrong	1	temperature	check oven temp.controller 9	2	16	None					П	
(not applicable for PPF L/F)		failure(8)			temperature setup		autoalarm system	points(4)									
,							follow TCM table	temperature autoalarm									
							Check oven	system(2)									
							temp.controller 9										
							points monitor 1x										
	undercure	electrical	8		wrong	1	temperature	check oven temp.controller 9	2	16	None					П	
		failure(8)			temperature setup		autoalarm system	points(4)									
							follow TCM table	temperature autoalarm									
							Check oven	system(2)									
							temp.controller 9										
							points monitor 1x										
11. Trim&form	chip/crack/microg	Reject by visual	8		Dieset broken	2	PM replace worn-	Visual sample check after	5	80	None					П	
	ap	inspection or					out part regularly	Trim&Form(5)									
		vision system(4)															
		reliability fail(8)	8		foreign matter	2.	Clean tooling per lot	Visual sample check after	5	80	None					Н	
			0		reside on bottom	_	Cican tooming per for	Trim&Form(5)		00	rvone						
					supporting block			(-)									
			8		unit remain/drop	2	Detect by sensor at	sensor check automatically	2	32	None					Н	
			ľ		in dieset	ľ	dieset	(2)	آ	32	i cone						
			8		L/F feed	3	Detect by sensor	sensor check automatically	2	48	None						
					abnormally			(2)								Ш	
	foreign matter	Reject by visual	4			2	Clean the TF tool	100% final visual inspection	3	24	None						
		inspection or			die/punch		per lot.	(3)									
		vision system(4)					Clean vacuum system shiftly										
	Į.	I.			1		SVSICIII SIIIIIIV	l .	1		1	l .	l .			ш	

Item: SOIC16/28/32/54ld	Control Number/Issue: 8	3MCT00002A	/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: I	Freescale,TJN-F	FM
Prepared By: Amanda Wang	FMEA Date:	05-Oct-94	(Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XIA	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN	14-Nov-13	(Rev.)
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													Action F	Resu	lts		
Process	Potential Failure		S	C	Potential	О	C	Current Design/ Process			Recommended	Responsibility &					R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е		Action(s)	Target	Effective Date	Е		Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
				s	of Failue												
				s													
			4		scratch on	3	Clean the TF tool	100% final visual inspection	3	36	None						
					lead/package		per lot.	(3)									
					body		Clean vacuum system shiftly										
	bent lead	Reject by visual	8		Lead Frame	2	PM check	100% final visual inspection	3	48	None						
	oun road	inspection or			jammed at		singulation tool	(3)		.0	10110						
		vision system(4)			unloader station		shiftly	,									
		Electrical															
		failure(8)	8		forming tooling	1	PM check tool	100% final visual inspection	2	24	None						
			8		parts broken	1	shiftly before	(3)	3	24	None						1
					parts broken		production.	(3)									1
							operator clean and										
							check forming										
							bending part per lot										
							before production.										
	metal bridge	Reject by visual	8		Die set broken	2	Check/replace piece	Visual sample check after	3	48	None						
		inspection or					part of T/F tooling	Trim&Form(5).									
		vision system(4)					on PM schedulely	100% final visual inspection									
		electrical						(3)									
	Excessive	failure(8) Customer	8		Die set broken.	2	PM check shiftly	Visual sample check after	4	64	None						
		application failure	ľ					Trim&Form(5);SPC									
	• •	(8)						monitor(4)									
			8		L/F damaged by	1		100% strip check (3)	3	24	None						
					former step			Visual sample check after									
								TrimForm(5)SPC monitor(4)									
			8		L/F jamed on	1		Sensor pin auto check (2).	2	16	None						
					track			Visual sample check after									
								Trim&Form(5)SPC									
			<u> </u>					monitor(4)									

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI.	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)

													Action I	 lts		
Process	Potential Failure		S	C	Potential	О	Current Design/	Current Design/ Process				Responsibility &				
Function/ Requirements	Mode	Effect(s) of Failure	E V	l a s	Cause(s)/ Mechanism(s) of Failue	C C	Process Controls Prevention	Controls Detection	E T	P N	Action(s)	Target Completion Date	Effective Date	C C	E T	
	physical dimension ( stand off, tip to tip distance, lead length/angle)	Customer application failure(8)	8		Punch guide was broken or worn out	1	Check punch guide shiftly. Replace worn-out punch guide regularly	Visual sample check after Trim&Form(5)	5	40	None					
			8		Cutting punch was broken or worn out	1	shiftly. Replace worn-out cutting punch regularly	Visual sample check after Trim&Form(5)		40	None					
			8		Cutting plate was broken or worn out		Check cutting plate shiftly Replace worn-out cutting plate	Visual sample check after Trim&Form(5)	5	40	None					
	Uncut Dambar	Reject by visual inspection or vision system (4) Electrical failure (8)	8		Dambar punch/insert chipped	2	PM check the punch and dambar insert shiftly	Auto alarm for dambar check(2) 100% final visual inspection (3)	2	32	None					
	slug pull	Reject by visual inspection or vision system (4) electrial failure (8)	8		vacuum cleaning system breaks down/ do not function effectively	2	PM check and clean vacuum system monthly	Automatically check by machine (2) 100% final visual inspection (3)	2	32	None					
	L/F damaged	Reject by visual inspection or vision system(4)	4		L/F was loaded in wrong orientation	1		auto alarm for sensor check(2)	2	8	None					
	dambar burr	Reject by visual inspection or vision system(4) electrical failure	8		Dambar punch was broken(chipping) or worn out	3	Check dambar punch shiftly. Replace worn-out dambar punch regularly	Visual sample check after Trim&Form(5)100% final visual inspection (3) Auto dambar check function (2)	2	48	None					

Item: SOIC16/28/32/54ld	Control Number/Issue: 83MCT00002A/BY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Amanda Wang	FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI.	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN 14-Nov-13 (Rev.)

	-						-						Action F	Resu	lts		
Process	Potential Failure	Potential	S		Potential	О	Current Design/	Current Design/ Process	D		Recommended	Responsibility &				D	I
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Controls Detection	Е	P	Action(s)	Target	Effective Date	Е	C	E	I
Requirements		Failure	V	a	Mechanism(s)	C	Prevention		T	N		Completion Date		V	C	T	N
-				s	of Failue							_					
				s													
			8		Dambar insert was	1	Check dambar insert	Visual sample check after	2	16	None					$\neg$	_
					broken and worn		shiftly	Trim&Form(5)100% final									
					out		Replace worn-out	visual inspection (3)									
							dambar insert	Auto dambar check									
							reoularly	function (2)									
			8		Higher tin	1		Visual sample check after	2	16	None						
					concentration in			Trim&Form(5)100% final									
					Pb-free			visual inspection (3)									
					electrolyte.			Auto dambar check									
			8		Tin patch sticking	3	Check dambar	function (2) Visual sample check after	2	48	None					$\dashv$	_
					on the punch		punch shiftly.	Trim&Form(5)100% final	Ĩ		Tione						
					on the puner		Replace worn-out	visual inspection (3)									
							dambar punch	Auto dambar check function									
							regularly	(2)									
	Lead damaged	Reject by visual	8		realiser stag	2	Sensor checking	Auto detect scrap/slug bin	2	32	None						
		inspection or			remain in dieset			(2)									
		vision system(4)			due to slug bin			100% final visual inspection									
		electrical failure			full			(3)									
		(8)															
		Customer															
		application															
		foilma(7)	8		foreign matter	2	operator clean	100% final visual inspection	3	48	None					$\neg$	
					dropping onto		tooling per lot	(3)									
					dieset		100% strip										
							inspection										
			8		Dambar punch	2	PM check shiftly	Visual sample check after	3	48	None						
	incomplete cut	inspection or			Dambar insert			Trim&Form(5)100% final									
		vision system(4)			chipped			visual inspection (3)									
		electrical failure															
		(8)															

Item: SOIC16/28/32/54ld	Control Number/Issue: 8	3MCT00002A	BY	
Type: Design _x_ Process	Company, Group, Site/Business Unit: F	reescale,TJN-F	M	
Prepared By: Amanda Wang	FMEA Date:	05-Oct-94	(Orig.)	
Core Team: Amanda Wang, H.J. Liu, Ivory Guo, JUN YING ZHENG, XI.	AOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN	14-Nov-13	(Rev.)	

													Action I			
Process	Potential Failure		S	C	Potential	О	Current Design/	Current Design/ Process				Responsibility &				
Function/ Requirements	Mode	Effect(s) of Failure	E V	l a	Cause(s)/ Mechanism(s)	C C	Process Controls Prevention	Controls Detection	E T	P N	Action(s)	Target Completion Date	Effective Date	E V	E T	P N
requirements		1 andie	`	S	of Failue		1 ievention		1	11		Completion Date		•	1	11
				s												
			8		L/F inaccurate	2	100% strip	Visual sample check after	2	32	None					
					location		inspection to mark out deformation L/F	Trim&Form(5) 100% final visual inspection								
							before T/F. Safety	(3)								
							pin checked shiftly.	Safety pin alarm								
			8		foreign matter	2	Clean tooling per lot	Visual sample check after	5	80	None					
					reside on bottom supporting block			Trim&Form(5)								
					supporting block											
	copper exposure	solderability	8		forming parts	1	PM check shiftly	Visual sample check after	3	24	None					
		failure (8)			broken		,	Trim&Form(5)								
								100% final visual inspection								
					non-conductive	3	Sampling strip	1	5	120	Study the	Wei-Zhen Jin				
					foreign matter sticking on lead		inspection to mark out contaminaiton	Trim&Form(5)			•	R04247 05/13/2014				
					Sticking on read		L/F before T/F.				setup to improve	03/13/2011				
											the detection					
											capability for exposed Cu on					
											lead issue. Sev(8)					
											Occ(3) Det(2)					
	Patchback	Reject by visual	8		Excessive tin built	2	Use DLC forming	Visual sample check after	3	48	None					
		inspection or			up on forming			Trim&Form(5)								
		vision system(4) Electrical failure			tool		design. ,brush the T/F tool every lot,	100% final visual inspection (3)								
		(8)					Clean T/F Tool									
	scratch on	Reject by visual	4		Lead Frame	3	1v/shift 100% incoming	100% finial inspection (3)	3	36	None					
	lead/package body	inspection(4)			jammed at input station		inspection before TF									

			1 -				111022111	E EITE C	_		(11111111111111111111111111111111111111	(= 1:===)					
	Burn In/Final Te					_						83MCT00018A/A					
		_x_ Process						Company,C	Gro	up,Si		Freescale, TJN-FN					
Prepared By:						_					FMEA Date:		(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZH	II REN,LINGXUA	N.	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)				
												_	Action F				
Process	Potential Failure		S	C	Potential		Current Design/		D	R			Actions Taken &		О		R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/			Process Controls		P	Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				S	of Failue												
				S													
Burn in	ESD/EOS	-Electrical	8		-Wrist strap	1	-Turnstile wrist	-Q-check yield	3	24	None						
		failure(8)			and/or shoes		strap check during	control (3)									
		-Reliability failure			function fail		every entry to test										
		(8)					floor										
			0		***		26 41	0 1 1 11	2	2.1	N						
			8		-Workstation and	1	-Monthly check/half year	-Q-check yield control (3)	3	24	None						
					equipment are not properly grounded		PM	control (3)									
					property grounded		1 141										
	Product	-Electrical	8		-Operate more	2	-Handle only one	-Quantity count (6)	4	64	None						
	mixed/escaped	failure(8)			than one lot at		lot in one table /	-Sampling check									
		-Reliability failure			same time		Loader &	the marking (8)									
		(8)					Unloader	-100% auto VM									
							-Perform marking	inspection in									
							inspection before	packaging process.									
							lot start	(4)									
							-Material status										
							identification										
							before/after										
							process										
							-100% check										
							before next chamber start										
							chamber start										
						Ļ.		5 11 1 1 =	_	2.1							
			8		-Wrong program	1	-Only the latest	•	3	24	None						
	ĺ	1	I	1	used	I	Rev. program	<ul> <li>Q check detection</li> </ul>		1	1	1	1 ,			1 1	

(3)

available

Item:     Burn In/Final Test/Test Backend     Control Number/Issue:     83MCT00018A/AY       Type:     Design     _x_ Process     Company, Group, Site/Business Unit:     Freescale, TJN-FM       Prepared By:     Liang Yang     FMEA Date:     27-Jun-01     (Orig.)       Core Team:     Peg Tang, ZJ-TEST2 Hu, Peter Zhang, Dong Gao, Liang Yang, Wei Chen, HONGZHI REN, LINGXUAN XU, Sinbad Liu, Peng E     06-Sep-13     (Rev.)		ults		_	
Prepared By: Liang Yang FMEA Date: 27-Jun-01 (Orig.)		ults			
		ults			
Core Team: Peg Tang, ZJ-TEST2 Hu, Peter Zhang, Dong Gao, Liang Yang, Wei Chen, HONGZHI REN, LINGXUAN XU, Sinbad Liu, Peng D 06-Sep-13 (Rev.)		ults			
		ults			
		ults			
		ults			
Action I	S				
Process Potential Failure Potential S C Potential O Current Design/ Current Design/ D R Recommended Responsibility & Actions Taken &			) [		
Function/ Mode   Effect(s) of   E   1   Cause(s)/   C   Process Controls   Process Controls   E   P   Action(s)   Target   Effective Date	Е	C		Ξ	
Requirements Failure V a Mechanism(s) C Prevention Detection T N Completion Date	V	C	T	Γ	N
s of Failue					
Miss Burnin -Customer 8 -Operator miss lot 1 -Follow TSO and -Buddy check (7) 4 32 None					
application in Burnin peocess SFC instruction - 100% auto					
failure(8) -Auto start BI electrical test in					
-Reliability failure function to prevent packaging process					
(8) miss BI (4)			_	4	
8 -Socket 2 -Check and changeQ check & BIN2 3 48 None					
open/short socket during PM check detection (3) -Check before -Sampling check in					
loading units loading process (8)					
loading times loading process (8)					
Bend lead & -Visual 8 -Nonstandard 2 Set up standard -100% VM 4 64 None			+	十	_
coplanarity mechanical failure manual handling inspection (6)					
(6) mode method -100% auto VM					
-Customer inspection in					
application packaging process					
failure(8) (4)				$\perp$	
8 Bad socket 2 -Check and change -100% VM 4 64 None					
socket during PM inspection (6)					
-Check before -100% auto VM					
loading units inspection in					
packaging process (4)					
8 -Loader & 2 -Half year PM -In-process 4 64 None		-	+	+	
unloader machine   2   -Haif year PM   -In-process   4   64   None		ĺ			
misalignment handler by setup -100% auto VM					
checklist inspection in		ĺ			

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packaging process

		POIL	A T	IA.	LFAILUN	C	MODE AN	DEFFEC	13	$\mathbf{A}$	VAL I SIS	(FWILA)					
Item:	Burn In/Final Te	st/Test Backend				_			(	Contr	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process				_		Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FN	Л				
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZH	II REN,LINGXU <i>A</i>	AN 2	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)				
								•					•				
													Action I	Resu	ılts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е		Е	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				s	of Failue												
				s													
	Foreign matter on	- Electrical failure	8		-Particle from B/I	1	-Periodical clean	-100% VM	6	48	None						
	lead	(8)			board		B/I boards	inspection(6)									
							-Check B/I boards										
							by lot										
	Ball damage	-Visual	8		-Nonstandard	2	Standard manual	100 /0 4440 1111	4	64	None						
		mechanical failure			manual handling		handling method	inspection in									
		(6) -Customer			mode			packaging process									
		application						(4) -In-process									
		failure(8)						sampling check (8)									
		ranure(o)						sampling check (6)									
Material receiving	Product mixed	-Yield Loss (7)	8		Multiple lot	2	Periodical	- Manual verify	4	64	Auto Print Box	Liang Yang					
(Receive & store		-Customer Line			processed		Training to MTL	box label LOT#,				R57253/06-30-					
material)		pull (8)			simultaneously		Operators	device #, box			Barcode label	2014					
							2. Mobile SFC	quantity against			Sev=8, Occ=1,						
							terminal to	packing list & SFC			Det=4, RPN=32						
							eliminate bulk	- Accept on zero									
								discrepancy (6)									
							order	- 100% Marking check by Vision									
								system in									
								Packaging									
	I	1		1	1	1	I				I	I			1		

process(4)

		POTEN	T	IA	L FAILUR	$\mathbf{E}$	MODE AN	ID EFFECT	ΓS	$\mathbf{A}$	NALYSIS (	(FMEA)		Pag	e 4,	of 4	16	
Item:	Burn In/Final Te	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	Υ					
Type:	Design	_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FM	1					
Prepared By:	Liang Yang					_					FMEA Date:	27-Jun-01	(Orig.)					
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zh	ang,	Dong	g Gao,Liang Yang	z,W	ei Chen,HONGZH	II REN,LINGXU	AN 2	XU,S	inbad Liu,Peng D	06-Sep-13	(Rev.)					
								•										
													Action I	Resi	alts			
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R	<u>.                                    </u>
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	Е	P	)
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N	1
				s	of Failue													
				s														
	Count variance	Qty shortage	3		Miss Counting by	2	Mobile SFC	- Manual verify	5	30	None							_
	(CV)				Assembly or BI		terminal to	box label LOT#,										
					Site		eliminate bulk	device #, box					<u> </u>					
					ļ	1	processing of shop	quantity against										
		1				1	order	packing list & SFC						1				

- Accept on zero discrepancy (6) - 100% Count Qty by Test operator

- Manual verify

box label LOT#,

quantity against

- Accept on zero

discrepancy (6) - 100% Count Qty by Test operator

- Sampling

check (5)

Marking inspection

during incoming

packing list & SFC

device #, box

None

45

None

(5)

(5)

Miss Counting by 2 NA

Assembly or BI

Device mixed at

Assembly or BI

process

3 NA

Site

INCOMING

Mechanical only

Assembly & BI

CHECK

(Visual

applies to

rawstock)

Count variance

Raw stock issue

(CV)

Qty shortage

Marking

order

mismatch with

System/shop

												,					
Item:	Burn In/Final Te	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	Υ				
Type:	Design	_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FM	1				
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	Dong	Gao,Liang Yang	g,W	ei Chen,HONGZH	II REN,LINGXU <i>A</i>	AN I	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)				
		· · · · · · · · · · · · · · · · · · ·			<u>, , , , , , , , , , , , , , , , , , , </u>	,	· · · · · · · · · · · · · · · · · · ·	•			, 6	•	`				
													Action R	Rest	ılts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	0	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/		Process Controls				Action(s)	Target	Effective Date	Е		Е	
Requirements		Failure	V	a	Mechanism(s)	C		Detection	Т	N		Completion Date		V	C	T	N
1			ľ	s	of Failue				_					·			
				s	or runde												
	V/M Defect	-Visual	8		V/M defect	2	NA	- Sampling V/M	4	64	None						
	VIIII Beleet	mechanical failure	0		introduced by	_	11/1	inspection during	ľ		Trone						
		(6)			Assembly or BI			incoming check (5)									
		-Customer			process			- 100% Marking									
		application			1			check by Vision									
		failure(8)			ļ			system in									
					ļ			Packaging									
					ļ			process(4)									
ELECTRICAL	Lot Combination	Yield Loss (7)	8		Mixed with Other	1	Config lot combine	- ATE Test (3)	3	24	None						
ΓEST as per test	by mistake	Customer line pull			device		rule in SFC system										
shop order	•	(8)			ļ												
1. Machine					ļ												
oreparation					ļ												
2. Start lot					ļ												
<ol><li>Electrical</li></ol>					ļ												
parameters tests					ļ												
4. End lot					ļ												
(Hot/Cold/Room)					ļ												

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Item:	Burn In/Final Te	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process				-		Company,C	Gro	up,Si	te/Business Unit:	Freescale, TJN-FN	Л				
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZH	II REN,LINGXUA	N.	XU,S	inbad Liu,Peng D	06-Sep-13	(Rev.)				
								-									
													Action I				
Process	Potential Failure	Potential	S	C	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Ε	1	Cause(s)/	С	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	С	Е	P
Requirements		Failure	V	a	Mechanism(s)	С	Prevention	Detection	T	N		Completion Date		V	C	T	N
				S	of Failue												
				s													
			8		mixed with other	1	Config lot combine	-lot information	4	32	None						
					trace code		rule in SFC system										
								post combination									
								(6)									
								-100% Count Qty by Test operator									
								before test(5)									
								-100% auto VM									
								inspection in									
								Packaging process.									
								(4)									
	Expired BI	Infant mortality,	8		Lot staged for too	1	Daily WIP review		2	16	None						
	window	fail electrical test			long after BI		by mfg and	with expired BI									
		during board					planner. Test	window (2)									
		assembly (8)					priority given to										
							material with BI window. Expected										
							BI expiry date can										
							be viewed in										
							genesis through lot										
							enquiry screen										
	Wrong machine	Fail 1st article	3		Use wrong tester	1	Listed Tester	- Operator check	1	3	None					П	
	setup	check (3)					information on	tester vs. TSO									
		Unable to perform					TSO	during setup (5)									
		test (2)					Test program is	- Program auto									
							configed by tester	verify during									
			L			_		download (1)	_	20						Ш	
			3		Use wrong handler	2	Listed handler	- Operator check Handler vs. TSO	5	30	None						
		1	1	ı	mandier		mnormation on	manuer vs. 150		1							

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during setup (5)

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Freescale Rev D

FUIENTIAL FAILUR	LE MODE AND EFFECTS ANALISIS (F	WILLA)	C
Item: Burn In/Final Test/Test Backend	Control Number/Issue: 83	3MCT00018A/A	AY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Fr	reescale,TJN-FN	Λ
Prepared By: Liang Yang	FMEA Date:	27-Jun-01	(Orig.)
Core Team: Peg Tang, ZJ-TEST2 Hu, Peter Zhang, Dong Gao, Liang Yang	g,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng D	06-Sep-13	(Rev.)
	_		
			Action Results
Process Potential Failure Potential S C Potential	O Current Design/ Current Design/ D R Recommended R	Responsibility &	Actions Taken & S O D R
		m .	

					_						_		Action I		_		
Process	Potential Failure		S		Potential	О		_		R	Recommended	Responsibility &			O		R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е		Action(s)	Target	Effective Date	Е	C		
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				S	of Failue												
				s													
			3		Wrong loadboard	3	Engineer create	- Manual visual	5	45	None					П	
					identification			verification on									
							•	loadboad ID									
							before releasing to	_									
							production (applies										
							for NPI as well)	M (5)									
																Ш	<u> </u>
			3		Wrong shoporder	3	NA	`	6	54	Work with IT	Wei Chen					
					loadboard ID			Audit (6)				R65950/06-30-					
					setup						LB information to	2014					
											SFC system. Sev=3, Occ=2,						
											Det=6, RPN=36						
			3		Tray loaded in	1	Poka Yoke	- Auto alarm for	2	6	None					$\vdash$	┢
					wrong orientation	1	mechanism on	wrong orientation	_	O	Trone						
					wrong orientation			(2)									
								- ATE Test (3)									
	Wrong test	Yield Loss (7)	8		Error during	2	SC2 auto	- QC in line gate	4	64	None					П	T
	temperature	Customer line pul	1		manual		temperature	(4)									
		(8)			temperature		loading	- QA Document									
					selection		(except MST)	Audit (6)									
								- QA shiftly audit									
								(8)									

Item:	Burn In/Final Te		11	1/1.	LIAILUN		WIODE AN	(D EFFEC)				83MCT00018A/A	Y	_			
	Design	_x_ Process				•		Company.				Freescale, TJN-FN					
Prepared By:	_									F ,	FMEA Date:		(Orig.)				
		ST2 Hu.Peter Zh	ang.	Dong	Gao.Liang Yang	z.W	ei Chen.HONGZH	II REN,LINGXU <i>A</i>	AN :	XU.S			(Rev.)				
		,	/ن			<i></i>	· · · · · · · · · · · · · · · · · · ·	•			, ,		.` ′				
													Action F	Resu	ılts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	С	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	С	Е	P
Requirements		Failure	V	a	Mechanism(s)	С	Prevention	Detection	Т	N		Completion Date		V	С	T	N
				s	of Failue												
				S													
			8		Wrong O/I	3	Dedicate	- QA Document	3	72	Download	Liang Yang					
					configuration		engineering	Audit (6)			Gen2Spec	R57253/05-30-					
					setup		personel to	- Auto-trigger on			parameters to auto-	2014					
							perform O/I	missing			generate SC						
							configuration	configuration to			configuration file						
								respective PE			using SC Config						
								through scheduled auto database			file generation						
								check (3)			tool						
								check (3)			Sev=8, Occ=2,						
											Det=3, RPN=48						
	Use wrong	Customer Line	8		TSO not updated	1	Only effective	-Auto verify	2	16	None						
	program	pull (8)			timely to reflect		version of Test	program									
		Yield Loss (7)			program revision		program is	information before									
							available in Server	test start (2)									
								- First 200 units									
								yield check(5)									
								- QA Document									
								Audit (6)									
			Q		Program selection	2	Listed test	- QA Document	4	64	None					$\vdash \vdash$	
			O		error	_	program	Audit (6)	ľ	04	TAOHE						
							information on	- Buddy check									
							TSO;	before test (7)									
							2. Listed handler	- QC in line gate									
							information on	(4)									

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3. Auto-program loading except for A5 & MST

- QA shiftly audit

Item: Burn In/Final Test/Test Backend	Control Number/Issue: 83	3MCT00018A/	'AY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Fr	reescale,TJN-F	M
Prepared By: Liang Yang	FMEA Date:	27-Jun-01	(Orig.)
Core Team: Peg Tang, ZJ-TEST2 Hu, Peter Zhang, Dong Gao, Liang Y	ang, Wei Chen, HONGZHI REN, LINGXUAN XU, Sinbad Liu, Peng Γ	06-Sep-13	(Rev.)
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			_		_		_				_		Action I				
Process	Potential Failure		S		Potential	О		Current Design/				Responsibility &					
Function/ Requirements	Mode	Effect(s) of Failure	E V	l a s	Cause(s)/ Mechanism(s) of Failue	C C	Process Controls Prevention	Process Controls Detection	E T		Action(s)	Target Completion Date	Effective Date	E V	C C	E T	P N
				S													
			8		SPV Program selection error	1	1. Enforce expiry duration on program reside in SPV 2. Auto SPV program loading on SC2	- QC in line gate (4) - QA Document Audit (6) - QA shiftly audit (8)			None						
			8		Wrong O/I configuration setup	2	Dedicate engineering personel to perform O/I configuration Download Gen2Spec parameters to autogenerate SC configuration file	- QA Document Audit (6) - Auto-trigger on missing configuration to respective PE through scheduled auto database check (3)	3	48	None						
		Customer Line pull (8) Yield Loss (7)	8		-Wrist strap and/or shoes function fail	1		-Yield limit and SBL check (3) -JVT test at last insertion (3)	3	24	None						
			8		No grounding (work station / rack)	1	-Quarterly check	-Yield limit and SBL check (3) -JVT test at last insertion (3)	3	24	None						

		PUIL	<b>1</b> T	IA	LFAILUK	L	MODE AN	DEFFEC.				,		-			
Item:	Burn In/Final Tes	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	ΑY				
Type:	Design	_x_ Process				_		Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FN	Л				
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TES	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZH	II REN,LINGXU	AN I	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)				
								•					•				
													Action I				
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	0	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	Т	N
				s	of Failue												
				s													
			8		Inaccurate	1	Use bracket to hold	- QC in line gate	3	24	None						
					placement for		ionizer at a specific	` '									
					ionizer		correct place	- High electrical									
								fall out at next									
								insertion for leakage or idd									
								failure (3)									
								- JVT test at last									
								insertion (3)									
			8		Testers / Handlers	2	Check grounding	- JVT test at last	3	48	None				-	-	
			Ü		environment	[~	-	insertion (3)	5	10	Tione						
							properly installed	(-)									
							during half year										
							PM										
			8		Spike voltage on	1	Spike check during	-Yield limit and	3	24	None						
					the DC		NPI release	SBL check (3)									
					measurement			-JVT or equivalent									
								test methodology									
								(3)	_	40					┝	_	
			8		Loadboard traces	2	continuity check	-Yield limit and	3	48	None						
					shorted		during Loadboard buyoff and	SBL check (3) -JVT or equivalent									
			1		ĺ		buyon and	-J v 1 or equivalent									

test methodology

(3)

Loadboard PM

1012112		1111111	
Item: Burn In/Final Test/Test Backend	Control Number/Issue: 8	83MCT00018A/	/AY
Type: Designx_ Process	Company, Group, Site/Business Unit: 1	Freescale,TJN-F	FM
Prepared By: Liang Yang	FMEA Date:	27-Jun-01	(Orig.)
Core Team: Peg Tang,ZJ-TEST2 Hu,Peter Zhang,Dong (	Gao, Liang Yang, Wei Chen, HONGZHI REN, LINGXUAN XU, Sinbad Liu, Peng C	06-Sep-13	(Rev.)

													Action I				
Process	Potential Failure	Potential	S	C	Potential	О	Current Design/	Current Design/	D		Recommended	Responsibility &		S	O		
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Ε			
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	
				S	of Failue												
				S													
	Product	Customer Line	8			4	-Handle only one	-Quantity count (6)	2	64	None						Ī
	mixed/escaped	pull (8)			and tested units		lot in one station	-Sampling check									l
		Yield Loss (7)			/ Mix of rawstock		-Perform marking	the marking (8)									l
					and reject from		inspection before	-QC in line gating									
					different lot		lot start	(4)									
							-Material status	-100% auto VM									ı
							identification before/after	inspection in									ı
							process	packaging process. (4)									ı
							-Treat all	-Test program auto									
							uncomfirming	detect part									
							units and PE used	difference (3)									
							units as rejects	-Optimize ECID									
							- Proper labeling	system to auto hold									
							using lot	material if the									
							identification	ECID doesn't									
							barcode	match between									
							- Pending rack,	different insertion									ı
							Input & output	(2)									ı
							rack with proper										
							labeling										
							- Label all work										
							place for proper										ı
							material										ı
							segregation -All tested good										ı
							partial/full tube are										ı
							to be placed inside										ı
							or next to the										ı
							tested good box										
							-Identified color										
							tray/tube to collect										
							rejects										
							-Separate pending										
		,	DIL- · ·			4	rack away from	0000000 4:1	£			.,					١
		]	Eleci	ronic	versions are unc	onti	rack away from olled except when input rack by ontrolled except v	accessed directly	Iro	m [do	cument repositor	<b>y</b> ].	D		a D		Į
				Pri	nted versions are	unc	ontrolled except v	nen stamped "Co	ntro	ned (	copy" in red.		Free	tsca	C K	ev.	f
			1	I			appearance and	ĺ	1	I	1	I	1				

			1 -	<b>T</b> 1			MODE III	DELLE				,					
	Burn In/Final Tes											83MCT00018A/A					
		_x_ Process						Company,	Gro	up,Si		Freescale, TJN-FM					
Prepared By:											FMEA Date:		(Orig.)				
Core Team:	Peg Tang, ZJ-TES	ST2 Hu,Peter Zh	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZE	II REN,LINGXU <i>A</i>	AN:	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)				
													Action I	Resu	ılts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е		Cause(s)/	С	Process Controls			P	Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	С		Detection	Т	N		Completion Date		V	C		
•				s	of Failue							•					
				s													
			8		Miss test insertion	1	Test flow configed	- Genesis auto	1	8	None						
					or in line gate		and auto controlled			O	Trone						
					S		by Genesis system	•									
								(1)									
			8		-Wrong binning	1	-Disable the bin	-QA document	4	32	None						
					setting of handler		setting button at	audit (6)									
							the operation	-QC in line gate									
							interface to prevent	(4)									
							misclick.										
							-Use SC2 auto										
							control bin setting										
			8		-Leftover unit in	2	-Clear machine		3	48	None						
					equipment		before and after	inspection for first									
							test	200 units (5)									
							-Lot count before	-Quantity count (6)									
							start testing	-Using SC2 auto									
							-Centralized reject	count lot quantity									
								except MST, A5									
							area after QA validation	(3)									
							vanuation										
						ļ			<u> </u>	L_							
			8		-speed sort device	1	-Using different	C	4	32	None						
					mixed		color tray/tube to	audit (6)									
							replace different	-QC in line gate									
							color clip for	(4)									

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identification

		POIL	11.	IA.	LFAILUN	L	MODE AN	DEFFEC.	19	$\mathbf{A}$	VAL I SIS	(FIMILA)					
Item:	Burn In/Final Tes	st/Test Backend				_						83MCT00018A/A					
	•	_x_ Process						Company,	Gro	up,Si		Freescale, TJN-FM	Л				
Prepared By:						_					FMEA Date:		(Orig.)				
Core Team:	Peg Tang,ZJ-TES	ST2 Hu,Peter Zh	ang,l	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZE	II REN,LINGXU	AN 2	XU,S	inbad Liu,Peng I	06-Sep-13	(Rev.)				
													Action F				
Process	Potential Failure	Potential	S	C	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S			
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls			Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				S	of Failue												
				S													
			8		-Wrong customer	1	-Add password	-QA document	3	24	None						
					code key in for		verification to	audit (6)									
					factory		guaratee correct	-QC in line gate									
					programming		customer code	(4)									
					product		input	-100% EEV test									
							-Add customer	(3)									
							code check on gate test										
			0			<u> </u>				2.2							
			8		-Engineer/ Techincian	1	-Handle only one	-Quantity count (6)	4	32	None						
					mishandling		lot in one station -follow on line	-Sampling check the marking (8)									
					during on line		debug instruction	-QC in line gate									
					debug		-Material status	(4)									
					desug		identification										
							before/after										
							process										
							-Treat PE used										
							units as rejects										
							-System auto clear										
							testsite when quit										
							engineer testing										
							mode and sort all										
							verification units into reject trav										
	I I		1		I	1	mile reject tray		1	1	I		4				

Item: Burn In/Final Test/Test Backend	Control Number/Issue:	83MCT00018A/	AY
Type: Design _x_ Process	Company, Group, Site/Business Unit:	Freescale,TJN-F	M
Prepared By: Liang Yang	FMEA Date:	27-Jun-01	(Orig.)
Core Team: Peg Tang, ZJ-TEST2 Hu, Peter Zhang, Dong Gao, Liang Yang	,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng Γ	06-Sep-13	(Rev.)
	<u> </u>		

													Action I				
Process	Potential Failure	Potential	S	C	Potential	О		Current Design/				Responsibility &	Actions Taken &	S	О		
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C		Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C		
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				S	of Failue												
				s													
			8		Leftover unit on	2	-Check recycle tray	-100% auto VM	4	64	None						
					recycle tray			inspection in									
								packaging process									
								(4)									
							operation of	-Quantity count (6)									
							recycle tray	-Sampling check									
							checking	the marking (8)									
							-partial tray alert	-QC in line gate (4)									
								(4)									
			8		D - 44 D1	1	Castle handler	1. QC in line gate.	4	32	None						₩
			8		Battery Backup Unit (BBU)	1	firmware upgraded		4	32	None						
					memory full			2. QA shiftly audit									
					causing Castle			(8)									
					handler fail to			3. Quantity count									
					pickup rawstock		* *	(6)									
					unit and indexed												
					to main tray												
					buffer as an												
					empty tray												
			8		Bin1 units from	5	NA	- QC in line gate.	2	80	Station Controller	Peng Lin					
					previous insertion			(4)			auto stop test	R65908/06-28-					
					are not cleared			2. QA shiftly audit			program loading	2014					
					from output bin1			(8)			if any units						
					stacker / rack			3. ECID detection			detected at output						
			1					method for			area						
								applicable products			SEV=8, OCC=2,						
			1					(2)			DET=2, RPN=32						
								4. Quantity count (6)									
			1					(0)									
																	<u> L</u>

	Burn In/Final Te		`_				1,1022111			Contr		83MCT00018A/A					
		_x_ Process						Company,C	iroر	up,Si		Freescale, TJN-FN					
Prepared By:		CT2 H., D., 7h.		D	- C I : V	. 337	-: Ch HONGZI	II REN,LINGXUA	NT.	VIIC	FMEA Date:		(Orig.) (Rev.)				
Core Team:	Peg Tang,ZJ-TE	S12 Hu, Peter Zna	ang,	Dong	g Gao, Liang Tang	3, <b>v</b> v	ei Chell, HONGZE	II KEN,LINGAUA	IIN .	AU,3	ilibad Liu,Pelig L	06-Sep-13	(Kev.)				
													Action R	Resu	lts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &			D	R
Function/	Mode	Effect(s) of	E	1	Cause(s)/			Process Controls		P	Action(s)	Target	Effective Date	E			P
Requirements	111000	Failure	V	a	Mechanism(s)	C		Detection	T	N	11011011(5)	Completion Date		V		T	
				s	of Failue				_								- '
				s													
			8		Reject mixed into	2	1. Rawstock and	-QC in line gate.	3	48	None						
					good during		tested material	(4)									
					machine		segregation by	- QA shiftly audit									
					downtime eg.		operator during	(8)									
					During		machine down	- ECID detection									
					maintenance		2. Technician to	method for									
								applicable products									
							1	(3)									
							during										
							maintenance. All units are to be										
							placed back into										
							rawstock material										
							3. Scrap jammed										
							units										
							Centralized										
							reject scrapping in										
							QA area after QA										
							validation										
	Non qualified	Customer	8		Use production	2	Any engineering	All engineering lot	2	32	None				_		
	engineering lot	application failure	-		lot class for	_	lot need to use	class require MDR	_	32	TVOILE						
	shipped to	(8)			engineerig			prior shipment. (2)									
	customer	(-)			purpose causing		class.	r (2)									
					lot shipped as		Log in MDR for										
					production lot to		engineering lot										
					customer.		class to ship as										
							normal production										
			1				lot class.										

			•					-				,					
Item: Burn In/Final Test/Test Backend												83MCT00018A/A					
Type:	Design	_x_ Process						Company,	Gro	up,Si		Freescale, TJN-FN	1				
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TES	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZF	II REN,LINGXU	AN:	XU,S	Sinbad Liu,Peng I	06-Sep-13	(Rev.)				
								-					•				
													Action I	Resi	ults		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	С	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	С	Prevention	Detection	Т	N		Completion Date		V	C	T	N
•				s	of Failue							•					
				s													
	Low yield or SBL	- Yield loss (7)	7		Tester out of	1	- Tester calibration	- Yield limit	2	14	None						
	over limit				calibration			control in Genesis									
	(DC, functional,							(3)									
	parametric,							- SBL limit control									
	open/short,							(3)									
	electrical)							-Auto calibration									
								every program									
								loading (2) -Diagnostic during									
								PM (5)									
			<u> </u>			_	5: 11 1 1			20	2.7						
			7		-Wrong binning	1	-Disable the bin setting button at	-QA document audit (6)	4	28	None						
					setting of handler		the operation	-QC in line gate									
							interface to prevent										
							misclick.	(4)									
							-Use SC2 auto										
							control bin setting										
			7		- Handler setup	1	- Handler regular	- Yield limit	3	21	None						
					problem		PM	control in Genesis									
							- Set up check	(3)									
								- SBL limit control									
								(3)									
								- First 200 units									
			<u> </u>			_		yield check (4)							<u> </u>		
			7		- Load Board	3	- Load board	- Yield limit	3	63	None						
					problem		regular PM	control in Genesis (3)									
								- SBL limit control									
								(3)									
								- First 200 units									
								yield check (4)									

		POTE	NT	IA	L FAILUR	Œ	MODE AN	D EFFEC	ΓS	Al	NALYSIS (	(FMEA)	F	Page	17	of ·	46	
Item:	Burn In/Final Tes	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	ΑY					
Type:	Design	_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FN	Л					
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)					
Core Team:	Peg Tang,ZJ-TES	T2 Hu,Peter Zh	ang,	Dong	g Gao,Liang Yang	g,W	Vei Chen, HONGZH	II REN,LINGXU	AN 2	XU,S	inbad Liu,Peng D	06-Sep-13	(Rev.)					
								•										
													Action I	Resi	ults			
Process	Potential Failure	Potential	S	C	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	) [	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	Е		P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	' I	N
				s	of Failue													
				s	ļ								1					
			7		- Tester board	1	- Tester regular	- Yield limit	3	21	None							
					problem		PM	control in Genesis										
					ļ			(3)										
					Į.			- SBL limit control										
								(3)					1					
					1		1	- First 200 units			Ī		ı		1		1	,

Contact interface

regular

replacement

-Half year PM

-Shiftly check

checklist

Input quad

overpress

hardstop to preven

handler by setup

Poor contact at

(device under test)

DUT socket

-Device

hanlder

misplacement by

Unit overpress

during test

Bend lead &

coplanarity

-Visual

-Customer

application

failure(8)

(6)

mechanical failure

yield check (4)

control in Genesis

- SBL limit control

- First 200 units yield check (4)

sampling check (8)

-100% auto VM

packaging process

sampling check (8) -100% auto VM

inspection in

-In-process

inspection in packaging process

-In-process

63

32

None

None

None

- Yield limit

(3)

(3)

(4)

(4)

		POIL	<b>1</b> I.	IA	LFAILUN	C	MODE AN	DEFFEC	19	$\mathbf{A}$	ALL 1919	(FIMILA)					
Item:	Burn In/Final Tes	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	Υ				
Type:	Design	_x_ Process				-		Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FM	1				
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TES	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZE	II REN,LINGXU	AN 2	XU,S	inbad Liu,Peng I	06-Sep-13	(Rev.)				
								-									
													Action F	Resu	lts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	С	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	С	Prevention	Detection	T	N		Completion Date		V	C	T	N
-				s	of Failue							-					
				s													
			8		Bad socket/pogo	2	-Hard stopper	-In-process	4	64	None						
					pin		configuration	sampling check (8)									
							- Load board	-100% auto VM									
							regular PM	inspection in									
							- Contact interface	packaging process									
							regular	(4)									
							replacement										
			8		ATU causing	2	1. Use	-In-process		64	None						
					drop units		CASM/CAIM to	sampling check (8)									
							cycle ATU and	-100% auto VM									
							observe for mechanical	inspection in packaging process									
							binding issue	(4)									
							during handler PM	(4)									
							2. Designed tray										
							catcher with										
							loaded spring										
							3. Add mounting										
							plate to tighten										
							door sensor										
			8		Unit misplaced in	2	Handler buyoff	-In-process	4	64	None					寸	_
					tray at output		ofter DM and	compling check (8)	1								

conversion

sort xyz alignment

handler

-100% auto VM

packaging process

inspection in

	Burn In/Final Tes	t/Test Backend					111022111	(D EITE)		Contr		83MCT00018A/A					
		_x_ Process						Company,	Gro	up,Si		Freescale, TJN-FN					
Prepared By:		T2 Hu Peter Zh	ano	Done	g Gao Liang Yang	. W	ei Chen,HONGZF	II REN LINGXII	۱N	XUS	FMEA Date:		(Orig.) (Rev.)				
Core realin	108 14118,20 125	12 114,1 0001 231		2017	5 Gue, Estang Tung	,,	<u> </u>			110,0	ameno Bru,r ving E		.(110 / 1)				
	T						1	T			1	· · · · · · · · · · · · · · · · · · ·	Action I				
Process	Potential Failure	Potential	S	C	Potential		Current Design/			R		Responsibility &			0		
Function/ Requirements	Mode	Effect(s) of Failure	E V	1	Cause(s)/ Mechanism(s)	C	Process Controls Prevention	Detection	E T	P N	Action(s)	Target Completion Date	Effective Date	E V	C C	E T	P N
Requirements		ranute	ľ	a s	of Failue	١	Fievention	Detection	1	11		Completion Date		v	C	1	11
				s	or runde												
			8		- Operator handles	2	- Certify operators'	-In-process	4	64	None						
					material			sampling check (8)									
					manually.		yearly exam to check	-100% auto VM inspection in									
							- Treat manual	packaging process									
							operated material	(4)									
							as VM reject and										
							scrap.										
			8		-Frost inside test	2	-Warm up handler	-In-process	4	64	None						
			0		chamber	_	periodically	sampling check (8)	4	04	None						
							-Use air pressure to										
							prevent frozen	inspection in									
							during cold	packaging process									
							temperature test -System auto warm	(4)									
							up cold										
							temperature										
							handler										
							- SC2 Auto-defrost										
							function										
			8		-Hit by damaged	2	-Add chamfer at	-In-process	4	64	None					H	
			1		track corner		soak booster track	sampling check (8)									
			1				and singulator	-100% auto VM									
			1				track -Perform Track	inspection in packaging process									
							inspection when	(4)									
			1				replacement during										
							PM										

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	Burn In/Final Te											83MCT00018A/A						
		_x_ Process						Company,	Gro	up,Si		Freescale, TJN-FM						
Prepared By:											FMEA Date:		(Orig.)					
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ıng,	Dong	g Gao,Liang Yang	,W	ei Chen,HONGZH	II REN,LINGXU <i>A</i>	AN I	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)					
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													Action I					
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	0	D	R	
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	С	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	Е	P	
Requirements		Failure	V	a	Mechanism(s)	С	Prevention	Detection	T	N		Completion Date		V	С	T	N	
•				s	of Failue							•						
				s														
	Ball damage	-Visual	8		Bad socket/pogo	2	-Hard stopper	-In-process	4	64	None							-
		mechanical failure	pin		configuration	sampling check (8)	-											
		(6)			- Load board	-100% auto VM												
		-Customer				regular PM	inspection in											
		application				- Contact interface	packaging process											
		failure(8)				regular	(4)											
							replacement											
			8		Unit jam at core	2	1. Periodic handler	-In-process	4	64	None							
					section		PM to minimize	sampling check (8)										
							jamming	-100% auto VM										
								inspection in										
								packaging process										
							unit that jammed at	(4)										
							core section											
																		_
			8		-Device	2	-Half year PM	m process	4	64	None							
					misplacement by		-Shiftly check	sampling check (8)										
					hanlder		handler by setup	-100% auto VM										
							checklist	inspection in										
								packaging process (4)										
								(4)										
			0		Linit axiomnas-	_	Innut and	In manage	4	32	None			-	<u> </u>			_
			0		Unit overpress	1	Input quad	-In-process sampling check (8)	4	32	none							
					during test		hardstop to prevent overpress	-100% auto VM										
							overpress	inspection in										
								packaging process										
								(4)										
				•	1			N /			i l							

Item:	Burn In/Final Tes		11.	17	LIAILUN		WIODE AI	DEFFEC				83MCT00018A/A	v	_				_
		_x_ Process				-		Company (				Freescale, TJN-FN						_
Prepared By:								company,	010	ар,ы	FMEA Date:		(Orig.)					_
		T2 Hu.Peter Zha	ang.	Dong	Gao.Liang Yans	.W	ei Chen.HONGZE	HI REN,LINGXUA	N/	XU.S			(Rev.)					
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													Action I	Resi	ılts			_
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	I	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	Е	]	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	Т	N		Completion Date		V	С	Т	1	N
_				s	of Failue													
				s														
			8		Unit misplaced in	2	Handler buyoff	-In-process		64	None							
					tray at output		after PM and	sampling check (8)										
					handler		conversion	-100% auto VM										
							sort xyz alignment	inspection in										
							jig	packaging process (4)										
								(4)										
			8		FM on substrate	1	1. Use hanging	-In-process	4	32	None						┢	_
					I IVI on substrate	1	nest with mold	sampling check (8)		-								
							guided &	-100% auto VM										
							chamfered design.	inspection in										
							2. Auto-defrost for	packaging process										
							J750	(4)										
							3. Periodical											
							handler cleaning 4. Boat clean											
							during conversion											
							during conversion											
			8		- Operator handles	2	- Certify operators'	-In-process	4	64	None						$\vdash$	_
					material		operation skill and	sampling check (8)										
					manually.		yearly exam to	-100% auto VM										
							check	inspection in										
							- Treat manual	packaging process										
							operated material	(4)										
							as VM reject and											
						1	scrap.											

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	Burn In/Final Te											83MCT00018A/A					
		_x_ Process						Company,	Gro	up,Si		Freescale, TJN-FM					
Prepared By:											FMEA Date:		(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZE	II REN,LINGXUA	AN 2	XU,S	Sinbad Liu,Peng L	06-Sep-13	(Rev.)				
													Action F	2001	ılta		
Process	Potential Failure	Potential	S	С	Potential	Ω	Current Design/	Current Design/	D	R	Recommended	Responsibility &				D	p
Function/	Mode	Effect(s) of	E		Cause(s)/			Process Controls		P	Action(s)	Target	Effective Date	E	C		
Requirements	Wiode	Failure	V	a	Mechanism(s)	C		Detection	Т	N	7 tetion(s)	Completion Date		V	C	T	N
Requirements		ranare		S	of Failue		Trevention	Detection	•	11		Completion Date		'		1	11
				s	or runae												
	Crack/chip	- Reliability	8		-Wrong handler	1	-Hard stopper	-In-process	2	16	None						
	r	failure (8)			adjustment		configuration	sampling check (8)									
		-Electrical failure						-Hard stopper auto									
		(8)						alarm (2)									
		-Visual mechanical failure															
		(6)															
		(0)	Q		-Incorrect bushing	1	-Hard stopper	-In-process	2	16	None						
			0		on L/B	1	configuration	sampling check (8)	_	10	None						
								-Hard stopper auto									
								alarm (2)									
			8		- Operator handles	2	- Certify operators'	7 0 1	4	64	None						
					material manually		operation skill and										
					in tray.		yearly exam to check	-100% auto VM									
								inspection in packaging process									
								(4)									
							as VM reject and										
							scrap.										
							- Put a empty tray										
							on the top before										
							move out material										
							from machine										

			` _				111022111	E EITE C	_ ~		11121818	(111111)					
	Burn In/Final Te											83MCT00018A/A					
		_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FM					
Prepared By:						_					FMEA Date:		(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zh	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZH	II REN,LINGXUA	AN :	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)				
								_					Action R		_		
	Potential Failure		S	С	Potential		Current Design/		D	R					О	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/		Process Controls			P	Action(s)	Target	Effective Date	Е	C		P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				S	of Failue												
				S													
	Sliver &	Short circuit or	8		High plating	2	Socket cleaning	- Yield limit	3	48	None						
	patchback (non	leakage (8)			material build up		and replace	control in Genesis									
	pogo socket only)				at test socket		regularly	(3) - SBL limit control									
								(3)									
								- First 200 units									
								yield check (4)									
								-V/M gate									
								sampling check (8)									
	Pogo Burr	Visual	6		Mechanical	2	Check for socket	- V/M gate	5	60	None						
		Mechanical			Contact offset on		bushing conditions	sampling check (8)									
		Failure (6)			device lead due		during PM.	- First 200 units									
					wear and tear of		Replace socket if	V/M check (5)									
					test socket pogo		pogo holes found										
					holes		wear and tear										
	D 11 1	0.11. 1.22	0				D 1 1 DM	37/34	5	10	None						
	Damaged lead foot plating	Solderability Failure (8)	8		test finger deformation	1	-Board regular PM - Check Pogo	sampling check (8)	3	40	None						
	surface	ranuic (8)			derormation		pin/socket	- First 200 units									
	Surruce						befor&after each	V/M check (5)									
							use	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,									
	Foreign Matter On	Solderability	8		Dirt accumulated	1	1. handler cleaning	- V/M gate	5	40	None						
	Lead	Failure (8)			in handler boat		during shift start	sampling check (8)									
							2. boat clean	- First 200 units									
							during conversion	V/M check (5)									

Prepared By:	Design Liang Yang Peg Tang,ZJ-TES  Potential Failure Mode	_x_ Process  ST2 Hu,Peter Zh  Potential  Effect(s) of	s E		g Gao,Liang Yang Potential Cause(s)/	О	Current Design/	II REN,LINGXUA	AN D	-	FMEA Date: Sinbad Liu,Peng I		(Orig.) (Rev.)			D E	
Requirements	Wiode	Failure	V	a s	Mechanism(s) of Failue	C		Detection	T	N	retion(s)	Completion Date		V	C	Т	N
			8	S	Unit drop out of tray	2	1. Strap Bin1 tray with cover tray right after testing 2. Unstrap rawstock bundle just before loading to ATU 3. Use CASM/CAIM to cycle ATU and observe for mechanical binding issue during handler PM (ATU issue) 4. Designed tray catcher with loaded spring (ATU issue) 5. Standardize tray latch spring to 0.32mm diameter (ATU issue) 6. Add mounting plate to tighten door sensor (ATU issue) 7. Treat dropped unit as reject	- V/M gate sampling check (8) - First 200 units V/M check (5) -100% auto VM inspection in packaging process (4)	4	64	None						

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	Burn In/Final Te							~				83MCT00018A/A					
• •	•	_x_ Process						Company,	Gro	up,Si		Freescale, TJN-FN					
Prepared By:											FMEA Date:		(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zh	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZH	II REN,LINGXU	AN :	XU,S	Sinbad Liu,Peng I	06-Sep-13	(Rev.)				
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Process	Potential Failure		S		Potential		Current Design/			R		Responsibility &				D	
Function/	Mode	Effect(s) of	Е	1	Cause(s)/		Process Controls			P	Action(s)	Target	Effective Date	Е	C		P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				S	of Failue												
				S										Ш			
			8		Usage of fibrous	1	Banned cotton	- QA shiftly audit	5	40	None						
					material at			(8)									
					production floor		and cloth from	- V/M gate									
							production floor	sampling check (8)									
								- First 200 units V/M check (5)									
								V/WI CHECK (3)									
			0	-	FM stick on pogo	2	Socket cleaning	- Yield limit	2.	48	None			Н			
			٥		pin	3	and replace if	control in Genesis	2	40	None						
					Pili		necessary	(3)									
							necessary	- SBL limit control									
								(3)									
			8		FM from	1	Top tray cover for	-V/M gate	4	32	None			П		Ħ	
					incoming/environ		trays during	sampling check (8)									
					ment dropped to		staging period to	-100% auto VM									
					staging trays		prevent FM	inspection in									
					causing FM to			packaging process									
					attach to units			(4)									
					when the trays are												
					used.												
														Ш			
	Foreign Matter On	•	8		FM from	1	1 "		6	48	None						
	Package Body	Failure (8)			incoming/environ			using 3x inspection									
					ment dropped to			(6)									
			1		staging trays		prevent FM										
			1		causing FM to												

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when the trays are

used.

Item:	Burn In/Final Te	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FM	1				
Prepared By:	Liang Yang					_					FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ing,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZH	II REN,LINGXU	AN :	XU,S	inbad Liu,Peng D	06-Sep-13	(Rev.)				
								-									
													Action R	lesu	lts		
Process	Potential Failure	Potential	S	C	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	O	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C		P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	Т	N		Completion Date		V	C	T	N
				s	of Failue												
				s													
Laser mark	Missing mark	-customer	8		-Laser generator	1	-Machine auto	-First piece part	2	16	None						
		application failure			fail		check laser power	verification after									
		- 8					before marking.	marking(4)									
								-Machine auto									
								alarm when power									
								out of control(2)									
								-QA Gate(8)									
	Illegible mark	Customer	8		Inappropriate	2	Machine auto	-First piece part	2	32	None						
		application failure			laser power		check laser power	verification after									
		- 8					before marking.	marking(4) - Machine marking									
								100% auto scan in									
								subsequent process									
								(4)									
								-QA visual									
								inspection 200									
								units/lot(8)									
								-Machine auto									
								alarm when laser									
								power									
								abnormal.(2)									

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	Burn In/Final Te											83MCT00018A/A					
		_x_ Process						Company,	Gro	up,Si		Freescale, TJN-FN					
Prepared By:											FMEA Date:		(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZF	II REN,LINGXUA	AN 2	XU,S	Sinbad Liu,Peng I	06-Sep-13	(Rev.)				
													Action F				
Process	Potential Failure	Potential	S		Potential			Current Design/			Recommended	Responsibility &	Actions Taken &	S			
Function/	Mode	Effect(s) of	Ε	1	Cause(s)/			Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	E T	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				S	of Failue												
				s													
			8		Laser generator	1	NA	-First piece part	2	16	None						
					worn out			verification after									
								marking(4)									
								- Machine marking									
								100% auto scan in									
								subsequent process									
								(4)									
								-QA visual									
								inspection 200									
								units/lot(8)									
								-Machine auto									
								alarm when laser									
								power									
								abnormal.(2)									
	Marking	Customer	8		Location pin	1	NA	-First piece part	4	32	None						
	misalignment	application failure			damaged			verification after									
		- 8						marking(4)									
								- Machine marking									
								100% auto scan in									
								subsequent process									
								(4)									
								-QA visual									
								inspection 200									

units/lot(8)

Item:	Burn In/Final Te		11	1/1.	LIAILUN	<u>. 12</u>	MODE AIV	DEFFEC				83MCT00018A/A	Y	_			
		_x_ Process				•		Company, C				Freescale, TJN-FN					
Prepared By:								1 37		Τ,	FMEA Date:		(Orig.)				
		ST2 Hu,Peter Zha	ing,	Don	g Gao,Liang Yang	,W	ei Chen,HONGZH	II REN,LINGXUA	N Z	XU,S	Sinbad Liu,Peng D		(Rev.)				
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													Action R				
Process	Potential Failure	Potential	S	С	Potential		Current Design/			R	Recommended	Responsibility &	Actions Taken &	S		D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/			Process Controls		P	Action(s)	Target	Effective Date	Е			P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				s	of Failue												
				S													
	Wrong marking	Customer	8		Marking	1	-Auto load	-First piece part	4	32	None						
		application failure			information input		marking	verification after					j				
		- 8			error during		information	marking(4)									
					manual operation			- Machine marking 100% auto scan in									
								subsequent process									
								(4)									
								-QA visual									
								inspection 200									
								units/lot(8)									
40x Inspection	Burr&sliver on	-Visual	8		Shoulder	2	NA	-10x V/M gate (8)	2	32	None						
	shoulder/riser/	mechanical failure			damaged by BI			- 100% auto vision									
	lead	(6)			(failure identified			inspection on					j				
		-Customer			by KLM)			device (2)									
		application failure(8)															
	Bend lead &	-Visual	8		Unit out of pocket	2	Strap the tray	-V/M gate (8)	2.	32	None			_			
	coplanarity	mechanical failure			Unit out of pocket	2	whenever moving	- 100% auto vision	2	32	None						
	copianarity	(6)					the material	inspection on					j				
		-Customer						device (2)					j				
		application					check tray gap	` ,									
		failure(8)					before and after										
							strapping to ensure										
							no unit jump out										
							the pocket										
		I		ı			I			ı	I						

Type: Prepared By:	Liang Yang	_x_ Process	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZF	Company,	Gro	Contr up,Si	te/Business Unit: FMEA Date:	83MCT00018A/A Freescale,TJN-FN 27-Jun-01					
													Action R	0 0 0 1 1	140		
Process	Potential Failure	Potential	S	С	Potential	Ω	Current Design/	Current Design/	D	R	Recommended	Desponsibility &	Actions Taken &		O	D	R
Function/	Mode Mode	Effect(s) of	E	1	Cause(s)/			Process Controls		P	Action(s)	Target	Effective Date	E	C		P
Requirements	Wiode	Failure	V	a	Mechanism(s)	C		Detection	T	N	7 tetion(s)	Completion Date		V	C		N
1				s	of Failue							r					
				s													
			8		Mishandling the unit	2	1. Strap the tray whenever moving the material 2. Operator to check tray gap before and after strapping to ensure no unit jump out	-V/M gate (8) - 100% auto vision inspection on device (2)	2	32	None						
	Wrong orientation		8		Unit replaced in	2	the pocket  Pin1 reverification	-V/M gate	1	16	None						
	Mixed product	application failure (8)			misorientated form	2	after unit replacement	sampling check (8) -Vision system auto detect and alarm (2) -Auto-Pin 1 locate system by vision(1) -Pin1 bar setting for tray locate(1)	2	22	Nana						
	Mixed product	-Electrical failure (8) -Reliability failure (8)			Stray units at inspection table	12		-V/M gate sampling check (8) -Count quantity per shop order (6) - Vision 100% inspection (2)	2	32	None						

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	: Burn In/Final Te					-		_				83MCT00018A/A					
• •	: Design	_x_ Process						Company,	Gro	up,Si		Freescale, TJN-FN					
	: Liang Yang					-					FMEA Date:		(Orig.)				
Core Team	: Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZI	II REN,LINGXU <i>A</i>	AN .	XU,S	Sinbad Liu,Peng I	06-Sep-13	(Rev.)				
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Process	Potential Failure		S		Potential		Current Design/			R			Actions Taken &			D	
Function/	Mode	Effect(s) of	Е	1	Cause(s)/		Process Controls			P	Action(s)	Target	Effective Date	Е	C	E	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				S	of Failue												
				S													
			8		Swap Shop order	2	Process 1 lot at a	-System record the	2	32	None						
							time	marking teach									
								history in test									
								summary, operator 100% check									
								summary(4)									
								-System auto check									
								and judge if									
								marking is correct									
								or not after key in									
								the actual marking									
								(2)									
								100% vision									
								inspection									
			8		Swap bundle	2	Process 1 lot at a	1. Lot no	2	32	None						
							time	verification on									
								barcode label vs									
								TSO (3)									
								2. 100% vision									
								scanning (2)									
								3. QA VM Gate									
								(8)									
10x Inspection	Burr&sliver on	-Visual	8		Shoulder	2	NA	6	2	32	None						
	shoulder/riser/	mechanical failure			damaged by BI			- 100% auto vision									
	lead	(6)	I	1	(failure identified			inspection on		1	1		1			- 1	

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device (2)

-Customer

application failure(8)

by KLM)

		10121	<u> </u>				111022111	ELLEG	_ ~		11121010	(2 1/123/2)					
Item:	Burn In/Final Te	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FN	1				
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zh	ang,	,Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZH	II REN,LINGXU <i>A</i>	AN 2	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)				
								•									
													Action F	lesv	ılts		
Process	Potential Failure	Potential	S	C	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				S	of Failue												
				s													
	Bend lead &	-Visual	8		Unit out of pocket	2	1. Strap the tray	-V/M gate (8)	2	32	None			П			
	coplanarity	mechanical failure	;				whenever moving	- 100% auto vision									
		(6)						inspection on									
		-Customer						device (2)									
		application					check tray gap										
		failure(8)					before and after										
							strapping to ensure										
							no unit jump out the pocket										
							the pocket										
														$\sqcup$			
			8		Mishandling the	2	1. Strap the tray	17111 gate (6)	2	32	None						
					unit		whenever moving the material	- 100% auto vision									
								inspection on device (2)						, 1			
							check tray gap	device (2)						, 1			
							before and after							, 1			
							strapping to ensure							, 1			
							no unit jump out							, 1			
							the pocket										

		10121	1 - 2					D EITE	_ ~	1 - 1	WILD I DID	(= 1,111)					
Item:	Burn In/Final Te	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	Υ				
Type:	Design	_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FN	Л				
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,I	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZF	II REN,LINGXU	AN I	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)				
								•					•				
													Action F	Resu	ılts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	O	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	E	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				S	of Failue												
				S													
	Wrong orientation		8		Unit replaced in misorientated	2	Pin1 reverification after unit	-V/M gate	1	16	None			П			
		application failure (8)			form		replacement	sampling check (8) -Vision system									
		(6)			TOTH		replacement	auto detect and									
								alarm (2)									
								-Auto-Pin 1 locate									
								system by									
								vision(1)									
								-Pin1 bar setting									
								for tray locate(1)									
	Mixed product	-Electrical failure	8		Stray units at	2	Clear work station	-V/M gate	2	32	None						
		(8)			inspection table			sampling check (8)									
		-Reliability failure					lot.	-Count quantity						1 1			
		(8)						per shop order (6)									
								- Vision 100%									
								inspection (2)									
	I	I	1 1		ĺ		I	I	1		1		1	1			

	Item: Burn In/Final Test/Test Backend  Control Number/Issue: 83MCT00018A/AY																		
					Control Number/Issue: 83MCT00018A/AY														
	Design	_x_ Process				Company, Group, Site/Business Unit: Freescale, TJN-FM													
Prepared By:		ama ** =		_	~						FMEA Date:		(Orig.)						
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zh	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZF	II REN,LINGXUA	AN .	XU,S	inbad Liu,Peng E	06-Sep-13	(Rev.)						
													A .: T		1.				
	B	<b>.</b>	I a		T 5	_	[ a . p /	G . B /	_	I 5	ъ	D 11 11 0	Action R			ъ.	ъ		
Process	Potential Failure		S	C	Potential		Current Design/		D	R			Actions Taken &			D	R		
Function/	Mode	Effect(s) of	Е	1	Cause(s)/			Process Controls		P	Action(s)	Target	Effective Date	Е		Е			
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N		
				S	of Failue														
				S															
			8		Swap Shop order	2	Process 1 lot at a	-System record the	2	32	None								
							time	marking teach history in test											
								summary, operator											
								100% check											
								summary(4)											
								-System auto check											
								and judge if											
								marking is correct											
								or not after key in											
								the actual marking											
								(2)											
								100% vision											
								inspection											
			8		Swap bundle	2	Process 1 lot at a	1. Lot no	2	32	None								
					1		time	verification on											
								barcode label vs											
								TSO (3)											
								2. 100% vision											
								scanning (2)											
								3. QA VM Gate											
								(8)											
Bake	Mixed product	-Electrical failure	8		-Operator handles	3	-Ensure only one	-Count the quantity	4	96	Using bakeable	HONGZHI REN							
		(8)			the wrong device		lot in work table	for tube			tube to avoid	B06298/04-30-							
		-Reliability failure	:		without check		for tube package.	package(6)			mistake during	2014							
		(8)			marking		- Verify lot	-100% auto vision			tube to tube								
							number/ magazine	inspection in			process								
							number vs. shop	subsequence			SEV=8, OCC=1,								
		ĺ	1		ĺ		order	process (4)		I	DET=4, RPN=32								

		TOTE	<b>1</b> T	17.	LIAILUN	THE WOODE AND EFFECTS ANALISIS (FINEA)												
Item:	Burn In/Final Te	st/Test Backend				Control Number/Issue: 83MCT00018A/AY												
Type:	Design	_x_ Process				Company, Group, Site/Business Unit: Freescale, TJN-FM												
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)					
		ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZF	II REN,LINGXU <i>A</i>	AN 2	XU,S	inbad Liu,Peng I		(Rev.)					
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													Action R	Resu	lts			
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	0	D	R	
Function/	Mode	Effect(s) of	Ε	1	Cause(s)/	С	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е		Е	P	
Requirements		Failure	V	a	Mechanism(s)	С		Detection	Т	N		Completion Date		V		Т		
1				s	of Failue							•						
				s														
	Miss bake	-Reliability failure	8	_	-Operator forgets	2.	-Follow TSO and	-Genesis system	2	32	None							
	171100 Ount	(8)			to do bake step	Ī	SFC instruction	control (2)	_	-	1,0110							
		(-)			and transfer the			-Buddy check (7)										
					material to the			•										
					next step.													
			8		-Place pre-bake	2	-Different	-Genesis system	2	32	None							
					units into post-		requirement lot	control (2)										
					bake units		stock in different	` ´										
							area											
	Time/Temperature	-Customer	8		-Wrong time and	1	-Fix timer and	-Auto check	2	16	None							
	incompetent	application failure			temperature		temperature	system alarm(2)										
		(8)					controller to auto-											
							monitor											
Dry air storage	Moisture out of	- Delamination	8		- Dry air	1	N/A	- Flow meter check	6	48	None							
	control	issue (8)			barometric			per setup checklist										
		-Customer			pressure low			(6)										
		application failure						- HIC monitor /										
		(8)						open the Dry air										
								cabinet (6)										
	Miss Dry air	- Delamination	8		-Operator forgets	2	-Follow SFC	(, )	2	32	None					Ī		
	storage	issue (8)			to put the lot into		instruction.	-Genesis system										
		-Customer			the Dry air			control (2)										
		application failure			cabinet													

												,									
Item:	Burn In/Final Te	st/Test Backend				Control Number/Issue: 83MCT00018A/AY															
Type:	Design				Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FN	1											
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)								
Core Team:	Peg Tang,ZJ-TES	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	,W	ei Chen,HONGZE	II REN,LINGXU	AN :	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)								
							·	•				•									
														Action Results							
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R				
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	Е	P				
Requirements		Failure	V	a	Mechanism(s)	С	Prevention	Detection	Т	N		Completion Date		V		T	N				
•				s	of Failue							•									
				s																	
3x inspection	Bend lead &	-Visual	8		Unit out of pocket	2	1. Strap the tray	-V/M gate (8)	2	32	None				1						
1	coplanarity	mechanical failure			1		whenever moving	- 100% auto vision													
		(6)					the material	inspection on													
		-Customer					1	device (2)													
		application					check tray gap														
		failure(8)					before and after														
							strapping to ensure														
							no unit jump out														
							the pocket														
															_						
			8		Mishandling the	2	1. Strap the tray	-V/M gate (8)	2	32	None										
					unit		whenever moving the material	- 100% auto vision													
								inspection on device (2)													
							check tray gap	device (2)													
							before and after														
							strapping to ensure														
							no unit jump out														
							the pocket														
	ĺ	I			1		ĺ						, 1								

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Item:	Burn In/Final Te	st/Test Backend				Control Number/Issue: 83MCT00018A/AY													
Type:	Design	_x_ Process				Company, Group, Site/Business Unit: Freescale, TJN-FM													
Prepared By:											FMEA Date:		(Orig.)						
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZH	II REN,LINGXU	AN :	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)						
								•											
													Action Results						
Process	Potential Failure	Potential	S	C	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	O	D	R		
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е			P		
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N		
				s	of Failue														
				s															
	Wrong orientation	-Customer	8		Unit replaced in	2	Pin1 reverification	-V/M gate	1	16	None			П					
		application failure			misorientated		after unit	sampling check (8)											
		(8)			form		replacement	-Vision system											
								auto detect and											
								alarm (2)											
								-Auto-Pin 1 locate system by											
								vision(1)											
								-Pin1 bar setting											
								for tray locate(1)											
								, , ,											
	Mixed product	-Electrical failure	8		Stray units at	2	Clear work station	-V/M gate	2	32	None			П					
	•	(8)			inspection table			sampling check (8)											
		-Reliability failure					lot.	-Count quantity											
		(8)						per shop order (6)											
								- Vision 100%											
								inspection (2)											

		POTE	N.T.	IA.	L FAILUK	Œ	MODE AN	D EFFEC.	13	A	NALYSIS (	(FMEA)	1	agc	51 (	01 +	U
Item:	Burn In/Final Tes	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	Υ				
Type:	Design	_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FN	Л				
Prepared By:	Liang Yang									-	FMEA Date:	27-Jun-01	(Orig.)				
		ST2 Hu,Peter Zh	ang,	Dong	Gao,Liang Yang	z.W	ei Chen,HONGZF	II REN,LINGXU	AN I	XU,S	Sinbad Liu,Peng I		(Rev.)				
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													Action F	Resi	ılts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	E	1	Cause(s)/			Process Controls			Action(s)	Target	Effective Date	Е			P
Requirements	1,1000	Failure	V	a	Mechanism(s)	C		Detection	T	N	110tion(s)	Completion Date		V			
1				s	of Failue					- '						_	
				s	or runae												
			8	3	Swap Shop order	2	Process 1 lot at a	-System record the	2	32	None			<b>—</b>			
			O		Swap Shop order	_	time	marking teach	_	32	None						
							time	history in test									
								summary, operator									
								100% check									
								summary(4)									
								-System auto check									
								and judge if									
								marking is correct									
								or not after key in									
								the actual marking									
								(2)									
								100% vision									
								inspection									
			8		Swap bundle	2	Process 1 lot at a	1. Lot no	2	32	None						
							time	verification on									
								barcode label vs									
								TSO (3)									
								2. 100% vision									
								scanning (2)									
			1	I	1	ı	1	<ol><li>QA VM Gate</li></ol>		1	1		1	1 '			

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(8)

Lead scan

Bend lead &

coplanarity

-Visual

application

failure(8)

(6) -Customer

mechanical failure

-Bent tray

2 NA

-Operator 100%

- 100% auto vision

check tray (6)

inspection on

device (2)

32

None

		TOTE	11	1/1.	LIAILUN	T'	MODE AN	DEFFEC.	IO		IAL I BIB						
Item:	Burn In/Final Te	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	Υ				
Type:	Design	_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FM	1				
Prepared By:	Liang Yang					_					FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	,Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZE	II REN,LINGXU	AN :	XU,S	Sinbad Liu,Peng I	06-Sep-13	(Rev.)				
								•									
													Action F	Resu	llts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	$\mathbf{C}$	Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	$\mathbf{C}$	T	N
				s	of Failue												
				s													
			8		- Unit misplace in	2	-Half yearly PM	-V/M gate (8)	2	32	None						
					tray caused by			- 100% auto vision									
					handler precision			inspection on									
								device (2)									
	2D matrix	-Visual	6		- Bypass 2D	2	-High level	-System real time	2	24	None						
	unreadable	mechanical failure			matrix inspection		password control	monitor (2)									
		(6)			function												
			6		- Dongle is	2	NA	-Program auto	2	24	None						
					unworkable			alarm and stop handler when									
								dongle is									
								unworkable(2)									
	Unit wrong	-Customer	8		-Improper vision	1	-Regular setup	-V/M gate	1	8	None						
	_	application failure	~		set	1	checklist check.	sampling check (8)	1	o	None						
	orientation in tray	(8)			SCC		checkingt check.	-Vision system									
								auto detect and									
								alarm (2)									
								-Auto-Pin 1 locate									
								system by									
								vision(1)									
								-Pin1 bar setting									
								for tray locate(1)									
	l	ľ	1	1	I		ĺ		1	I	I						

		TOTE	11.	17	LIAILUN	112	MIODE AN	DEFFEC				` ′						_
	Burn In/Final Te											83MCT00018A/A						_
		_x_ Process						Company,	Gro	up,Si		Freescale, TJN-FM						
Prepared By:						_					FMEA Date:		(Orig.)					
Core Team:	Peg Tang, ZJ-TES	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZF	II REN,LINGXU <i>A</i>	AN I	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)					
							_				•		Action I					_
	Potential Failure		S	С	Potential		Current Design/					Responsibility &				D	R	
Function/	Mode	Effect(s) of	Е	1	Cause(s)/		Process Controls				Action(s)	Target	Effective Date	Е	C	Е	P	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N	
				S	of Failue													
				S														_
			8		-Wrong teach on	1		-V/M gate first	1	8	None							
					material for pin1		system by vision	piece check (4)										
								Buddy check(7) -Auto-Pin 1 locate										
								system by										
								vision(1)										
								-Pin1 bar setting										
								for tray locate(1)										
	Mixed product	-Electrical	8		-Operator does	2	-Equipment clean	-V/M gate	2	32	None							
	1	failure(8)			not clear the		after lot end	sampling check (8)										
		-Reliability failure			machine when			-Count quantity										
		(8)			finished lot			per shop order (6)										
								- Vision 100%										
								inspection (2)										
																		_
			8		-Operator teach	3	NA	-System record the	2	48	None							
					wrong marking			marking teach										
								history in test summary, operator										
								100% check										
								summary(4)										
								-System auto check										
								and judge if										
								marking is correct										
								or not after key in										
								the actual marking										
								(2)										
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Item:	Burn In/Final Tes	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/	AY					
Type:	Design	_x_ Process						Company,	Grou	up,Si	te/Business Unit:	Freescale, TJN-Fl	M					
Prepared By:	Liang Yang					_					FMEA Date:	27-Jun-01	(Orig.)					
Core Team:	Peg Tang,ZJ-TES	T2 Hu,Peter Zl	hang,	Dong	Gao,Liang Yan	g,W	ei Chen,HONGZH	II REN,LINGXU	AN 2	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)					ł
								•					_					
														Action R	esults	s		
Process	Potential Failure	Potential	S	C	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions 7	Гaken &	SC	) D	R	. 7

													Action I				
Process	Potential Failure	Potential	S	C	Potential		Current Design/				Recommended	Responsibility &					
Function/	Mode	Effect(s) of	Е	1	Cause(s)/			Process Controls			Action(s)	Target	Effective Date			Е	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				S	of Failue												
				S													
	Crack/chip		8		- Operator handles		- Certify operators'		2	32	None						
		failure (8) -Electrical failure			material manually in tray.		operation skill and yearly exam to	(6) - 100% auto vision									
		(8)			ili tray.		check	inspection (2)									
		-Visual					- Treat manual	mspection (2)									
		mechanical failure					operated material										
		(6)					as VM reject and										
							scrap.										
Tape & Reel		-Device fail out or	8	*	-Peel back force is	1	-Follow setup	- SPC system	4	32	None						
	/ tighten	cover tape split at			out of control		checklist to set up machine	control (4)									
		customer (8)					macnine	-QA audit peel back force test									
								record (6)									
								-QA sealing line									
								check (8)									
	2D matrix	-Visual	6		- Bypass 2D	2	-High level	-System real time	2	24	None						
	unreadable	mechanical failure			matrix inspection		password control	monitor (2)									
		(6)			function												
			6		- Dongle is	2	NA	-Program auto	2	24	None						
			O		- Dongie is unworkable		INA	alarm and stop		24	INOILE						
					un workhole			handler when									
								dongle is									
								unworkable(2)									

												<u> </u>						_
_	Burn In/Final Te					į.						83MCT00018A/A						
		_x_ Process						Company,	Gro	up,Si		Freescale, TJN-FN						
Prepared By:											FMEA Date:		(Orig.)					
Core Team:	Peg Tang, ZJ-TES	ST2 Hu,Peter Zha	ıng,	Dong	g Gao,Liang Yang	,W	ei Chen,HONGZF	II REN,LINGXUA	AN :	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)					
													Action I	Resi	ılts			
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	F	₹
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	С	Е	F	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	Т	N		Completion Date		V	С	T	N	V
				s	of Failue													
				s														
	Unit wrong	-Customer	8		-Wrong teach on	1	-Auto-Pin 1 locate	-V/M gate first	1	8	None							_
	orientation in tape				material for pin1		system by vision	piece check (4)										
	reel	(8)			1			Buddy check(7)										
								-Auto-Pin 1 locate										
								system by										
								vision(1)										
								-Pin1 bar setting										
								for tray locate(1)										
			8		-Improper vision	1	-Regular setup	-V/M gate	1	8	None							
					setting		checklist check.	sampling check (8)										
								-Vision system										
								auto detect and										
								alarm (2) -Auto-Pin 1 locate										
								system by										
								vision(1)										
								-Pin1 bar setting										
								for tray locate(1)										
	Bend lead	-Visual	8		-Machine pick up	2	- Cross beam	-V/M gate	2	32	None						H	_
		mechanical failure			head is not in the			sampling check (8)										
		(6)			perfect position		reel equipment.	-Handler cross										
		-Customer			along the X,Y,Z			sensor 100% check										
		application			direction			unit position and										
		failure(8)						auto alarm(2)										
								-Check per setup										
								checklist (6)										
					I	ı	I	1		1	I						1	

		POIL	1 T	IA.	LFAILUN	T.	MODE AN	D EFFEC.	19	AI	VAL I SIS	(FWILA)						
Item:	Burn In/Final Te	st/Test Backend				_			(	Contr	ol Number/Issue:	83MCT00018A/A	ΛY					
Type:	Design	_x_ Process				=		Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FN	Л					
Prepared By:	Liang Yang										FMEA Date:		(Orig.)					
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZF	II REN,LINGXU	AN I	XU,S	inbad Liu,Peng I	06-Sep-13	(Rev.)					
													•					
													Action I	Resi	ılts			
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S			F	R
Function/	Mode	Effect(s) of	Ε	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C		J	Ρ
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	Т	1	N
_				S	of Failue													
				s														
	Empty pocket	-Quantity	8		-Pocket2 sensor	2	NA	-Machine auto	2	32	None						T	_
		shortage for			does not work			alarm (2)										
		customer (8)			properly			-Reel counter setup										
								check (4)										
								'-PM daliy check										
								per setup check list										
								(6)										
	Tono vymana	-Electrical failure	0		On anoton format	1	-Using black or	-QA 100% check	6	48	None						╄	_
	Tape wrong revolution in reel	(8)	٥		-Operator forget to wind back	1		tape revolution for	O	40	None							
	revolution in reel	(8)			orginal reel after		reel.	every reel (6)										
					reel to reel		-Fix color reel to	every reer (o)										
					process		prevent mixed											
							handling by											
							operator											
			8		-Use white reel on	1	-Using black or	-QA 100% check	6	48	None							
					reel to reel		blue reel for reel to											
					process		reel.	every reel (6)										
							-Fix color reel to											
							prevent wrong reel											
			_				used.										Ļ	_
	Ball damage	-Visual	8		-Machine pick up	2	- Cross beam	-Handler cross	2	32	None							
		mechanical failure			head is not in the		_	sensor 100% check										
		(6)			perfect position		reel equipment.	unit position and										
		-Customer	I	I	along the X,Y,Z	1	1	auto alarm(2)	I							I		

-Check per setup checklist (6)

-Customer application

failure(8)

direction

												` '					
Item:	Burn In/Final Te	st/Test Backend										83MCT00018A/A					
• •	•	_x_ Process						Company,	Gro	up,Si		Freescale, TJN-FM					
Prepared By:						_					FMEA Date:		(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	z,W	ei Chen,HONGZI	II REN,LINGXU	AN :	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)				
						_											
		T			_		_						Action I				
Process	Potential Failure		S	С	Potential		Current Design/					Responsibility &			О		
Function/	Mode	Effect(s) of	Е	1	Cause(s)/			Process Controls			Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	Т	N		Completion Date		V	C	T	N
				S	of Failue												
				S													
	Cover tape		8		-Technician adjust	2	NA	-Technician first	4	64	None						
	misalignment with				the guider width			piece check under									
	carrier tape	(8)			or carrier tape			10X microscope									
					location pins			after technician									
					improperly.			adjust the guider width or carrier									
								tape location pins.									
								(4)									
	Mixed product	-Electrical	8		-Operator does	2	-Equipment clean	-V/M gate	2	32	None						
		failure(8)			not clear the		after lot end	sampling check (8)									
		-Reliability failure			machine when			-Count quantity									
		(8)			finished lot			per shop order (6)									
								- Vision 100%									
								inspection (2)									
			0		-Operator teach	3	NA	-System record the	2	48	None					Н	
			٥		wrong marking	3	NA	marking teach	2	46	None						
					wrong marking			history in test									
								summary, operator									
								100% check									
								summary(4)									
								-System auto check									
								and judge if									
								marking is correct									
								or not after key in									
						1		the actual marking (2)									
								(2)									

Item:	Burn In/Final Te		`-				WIODE AI					83MCT00018A/A	ΛY					
Type:	Design	_x_ Process				_		Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FN	Л					
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)					
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,l	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZF	II REN,LINGXU <i>A</i>	AN I	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)					
								•					•					
													Action I	Resi	ılts			
Process	Potential Failure	Potential	S	C	Potential	О		Current Design/		R	Recommended	Responsibility &	Actions Taken &	S				
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	Е	,	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	Т	١.	N
				s	of Failue													
				s														
TTT	Lead defect in	-Visual	8		-Tube and	1	-Re-design the	-V/M Gate	4	32	None							
	tube	mechanical failure			tracking		tracking to	sampling check (8)										
		(6)			alignment		optimize alignment	Frist piece check										
		-Customer						(4)										
		application																
	20 1	failure(8)				_		770.5		22						1	+	
	Mixed product	-Electrical failure(8)	8		-Operator does not clear the	2	-Equipment clean	-V/M gate	2	32	None							
		-Reliability failure			machine when		after lot end	sampling check (8) -Count quantity										
		(8)			finished lot			per shop order (6)										
		(0)			imisiica iot			- Vision 100%										
								inspection (2)										
			8		-Operator teach	3	NA	-System record the	2	48	None					Ī		
					wrong marking			marking teach										
								history in test										
								summary, operator										
								100% check										
								summary(4) -System auto check										
								and judge if										
								marking is correct								1		
								or not after key in										
								the actual marking								1		
								(2)										
																1	I	

Item:	Burn In/Final Te		11	1/1.	LIAILUN		WIODE AI	D EFFEC				83MCT00018A/A	Ϋ́				
	Design	_x_ Process						Company.				Freescale, TJN-FN					
Prepared By:								- · · · · · · · · · · · · · · · · · · ·		1	FMEA Date:		(Orig.)				
		ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yan	g,W	ei Chen,HONGZF	HI REN,LINGXUA	AN I	XU,S	inbad Liu,Peng [	06-Sep-13	(Rev.)				
								_			_		1				
													Action R				
Process	Potential Failure		S	C	Potential	О	U	Current Design/					Actions Taken &		О		R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/			Process Controls		P	Action(s)	Target	Effective Date	Е			P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				S	of Failue												
				S													
	Unit wrong	-Customer	8		-Wrong teach on	1	-Auto-Pin 1 locate	-V/M gate first	1	8	None						
	orientation in tube	application failure (8)			material for pin1		system by vision	piece check (4)Buddy check(7)									
		(0)						-Auto-Pin 1 locate									
								system by									
								vision(1)									
			8		-Improper vision	1	-Regular setup	-V/M gate	1	8	None						
					setting		checklist check.	sampling check (8) -Vision system									
								auto detect and									
								alarm (2)									
								-Auto-Pin 1 locate									
								system by									
								vision(1)									
DRY PACK	Bag leakage	-Reliability failure	8		-Break MBB	1	N/A	-QA 100% check packing quality for		48	None						
		(8)						every box (6)									
								every box (o)									
			8		-Poor dry pack	1	N/A	-QA 100% check	6	48	None						
					bag quality			packing quality for									
								every box (6)									
	No-dry pack	-Reliability failure	8		-Miss dry pack	1	N/A	-QA 100% check	6	48	None						
		(8)			process			packing quality for									
								every box(6)									

Item:	Burn In/Final Te	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process				)i		Company,				Freescale, TJN-FN					
-	Liang Yang					i)					FMEA Date:		(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	Don	g Gao,Liang Yang	y,W	ei Chen,HONGZI	II REN,LINGXU	AN .	XU,S	Sinbad Liu,Peng I	06-Sep-13	(Rev.)				
													Action I	Resu	ılts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	E	l	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	E	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				S	of Failue												
				S													<u> </u>
	Mixed product	-Electrical	8		-Operator handles	2	-One time one lot	-Automated	2	32	None						
		failure(8) -Reliability failure			more than one lot at same time.			verification barcode of box,									
		(8)			at same time.			dry bag by auto-									
								verify machine (2)									
								-QA check (8)									
	Duration time out	- Delamination	8		-The lot duration	2	N/A	- System auto	2	32	None						
	of control	issue (8) - Solderability			time was out of control			detect duration time before dry									
		issue (8)			Control			packing (2)									

Item:	Burn In/Final Te		11	IA.	LIAILUN		MODE AN	D EFFECT				83MCT00018A/A	ΑΥ				
		_x_ Process				-		Company.C				Freescale, TJN-FN					
Prepared By:	•							,		F ,	FMEA Date:		(Orig.)				
		ST2 Hu Peter Zha	anσ	Done	Gao Liang Yang	W	ei Chen HONGZE	II REN,LINGXUA	N.	XUS			(Rev.)				
	88,				5 5 5	ə, ··				,			.(====,)				
													Action F	Resu	ılts		
Process	Potential Failure	Potential	S	С	Potential	0	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &			D	R
Function/	Mode	Effect(s) of	E	1	Cause(s)/			Process Controls			Action(s)	Target	Effective Date	Ē		E	
Requirements	111000	Failure	V	a	Mechanism(s)	C		Detection	T	N	1 Tetron(s)	Completion Date		V	C	T	N
			`	S	of Failue				_					·			- '
				s													
Burn in	ESD/EOS	-Electrical	8	_	-Wrist strap	1	-Turnstile wrist	-Q-check yield	3	24	None						
	202/205	failure(8)			and/or shoes	1	strap check during	- •									
		-Reliability failure			function fail		every entry to test	. ,									
		(8)					floor										
			8		-Workstation and	1	-Monthly		3	24	None						
					equipment are not		check/half year	control (3)									
					properly grounded		PM										
		<b>F</b> 1	0													Н	
	Product	-Electrical	8		-Operate more	2	-Handle only one	-Quantity count (6)	4	64	None						
	mixed/escaped	failure(8) -Reliability failure			than one lot at same time		lot in one table / Loader &	-Sampling check the marking (8)									
		(8)			same time		Unloader	-100% auto VM									
		(6)						inspection in									
							2	packaging process.									
							lot start	(4)									
							-Material status	, ,									
							identification										
							before/after										
							process										
							-100% check										
							before next										
			I				chamber start										
																Ш	
			8		-Wrong program	1	-Only the latest	-Buddy check (7)	3	24	None					l I	

(3)

-Q check detection

Rev. program

available

used

IOIENTIAL FAILU	RE MODE AND EFFECTS ANALISIS (		C
Item: Burn In/Final Test/Test Backend	Control Number/Issue: 8	A/AY	
Type: Design _x_ Process	Company, Group, Site/Business Unit: 1	Freescale,TJN-I	FM
Prepared By: Liang Yang	FMEA Date:	27-Jun-01	(Orig.)
Core Team: Peg Tang, ZJ-TEST2 Hu, Peter Zhang, Dong Gao, Liang Y	ang,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng [	06-Sep-13	(Rev.)
			_
			Action Results
		D 11.11.	0 4 4 70 1 0 0 0 0

	1	•			•			•			1	•	Action I				
	Potential Failure		S		Potential	О		_				Responsibility &					F
Function/	Mode	Effect(s) of	Е	1	Cause(s)/		Process Controls				Action(s)	Target	Effective Date	Е		E	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				S	of Failue												ĺ
				S													
	Miss Burnin	-Customer	8		-Operator miss lot	1	-Follow TSO and	-Buddy check (7)	4	32	None						
		application			in Burnin peocess		SFC instruction	- 100% auto									
		failure(8)					-Auto start BI	electrical test in									İ
		-Reliability failure					function to prevent										İ
		(8)						(4)									
			8		-Socket	2	_	Q check & BIN2		48	None						İ
					open/short			check detection (3)									ĺ
							-Check before	-Sampling check in									İ
							loading units	loading process (8)									İ
																	İ
	Bend lead &	-Visual	8		-Nonstandard	_	0 1 . 1	-100% VM	4	64	None						<b>!</b>
		mechanical failure	-		manual handling	2	Set up standard manual handling	inspection (6)	4	04	None						ĺ
	copianarity	(6)			mode		method	-100% auto VM									İ
		-Customer			mode		metriod	inspection in									ĺ
		application						packaging process									ĺ
		failure(8)						(4)									İ
			8		-Bad socket	2	-Check and change	-100% VM	4	64	None						Г
							socket during PM	inspection (6)									ĺ
							-Check before	-100% auto VM									İ
							loading units	inspection in									İ
								packaging process									ĺ
								(4)									
			8		-Loader &	2	-Half year PM	-In-process		64	None						
					unloader machine		-Shiftly check	sampling check (8)									ĺ
					misalignment		handler by setup	-100% auto VM									ĺ
							checklist	inspection in									ĺ
								packaging process									ĺ
								(4)									ĺ
	1																1

IOIENTIAL PAILU	RE MODE AND EFFECTS ANALTSIS (FMEA)	
Item: Burn In/Final Test/Test Backend	Control Number/Issue: 83MCT00018A/AY	
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM	
Prepared By: Liang Yang	FMEA Date: 27-Jun-01 (On	rig.)
Core Team: Peg Tang, ZJ-TEST2 Hu, Peter Zhang, Dong Gao, Liang Y	ang, Wei Chen, HONGZHI REN, LINGXUAN XU, Sinbad Liu, Peng D 06-Sep-13 (Re	ev.)
		Action Results
Process Potential Failure Potential S C Potential	O Current Design/ Current Design/ D R Recommended Responsibility & Ac	tions Taken & S O D R

													Action F				
Process	Potential Failure	Potential	S	C	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	O	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е		Action(s)	Target	Effective Date			Е	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				S	of Failue												l
				S													l
	Foreign matter on	- Electrical failure	8		-Particle from B/I	1	-Periodical clean	-100% VM	6	48	None						l
	lead	(8)			board		B/I boards	inspection(6)									l
							-Check B/I boards										l
	Ball damage	-Visual	8		-Nonstandard	2	by lot Standard manual	-100% auto VM	4	C 1	None			$\vdash \vdash$	_	Н	
	Dan damage	mechanical failure	-		manual handling	2	handling method	inspection in	4	04	None						l
		(6)			mode		mananing metriod	packaging process									l
		-Customer						(4)									l
		application						-In-process									l
		failure(8)						sampling check (8)									l
M-4i-1i-i	Due des et essère e d	-Yield Loss (7)	8		M14:1 - 1 - 4	2	Periodical	- Manual verify	4	<i>C</i> 1	Auto Print Box	I : V		$\vdash$	_	Ш	
Material receiving (Receive & store	Product mixed	-Yield Loss (7) -Customer Line	8		Multiple lot processed	2	Training to MTL	box label LOT#,	4		Oty and # on	Liang Yang R57253/06-30-					l
material)		pull (8)			simultaneously		Operators	device #, box			Barcode label	2014					l
,		F (*)					2. Mobile SFC	quantity against			Sev=8, Occ=1,						l
							terminal to	packing list & SFC			Det=4, RPN=32						l
							eliminate bulk	- Accept on zero									l
							processing of shop	1									l
							order	- 100% Marking									l
								check by Vision									l
								system in Packaging									ı
								process(4)									ı
																	l
			1		i e	1	1	I		ı	I	ĺ	1	1		1 1	

Item: Burn In/Final Test/	/Test Backend	Control Number/Issue:	83MCT00018A/	AY
Type: Designx	x_ Process	Company, Group, Site/Business Unit:	Freescale, TJN-F	M
Prepared By: Liang Yang		FMEA Date:	27-Jun-01	(Orig.)
Core Team: Peg Tang,ZJ-TEST	Γ2 Hu,Peter Zhang,Dong Gao,Liang Yan	g,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng D	06-Sep-13	(Rev.)
<u> </u>				_

	_										-		Action I				
Process	Potential Failure	Potential	S	C	Potential	О		Current Design/			Recommended	Responsibility &	Actions Taken &	S	О		R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/		Process Controls				Action(s)	Target	Effective Date	Е		Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				s	of Failue												i
				s													<u></u>
		Qty shortage	3		Miss Counting by	2	Mobile SFC		5	30	None						i
	(CV)				Assembly or BI		terminal to	box label LOT#,									i
					Site		eliminate bulk	device #, box									i
								quantity against									i
							order	packing list & SFC									i
								- Accept on zero discrepancy (6)									i
								- 100% Count Qty									i
								by Test operator									i
								(5)									i
																	l
NCOMING	Count variance	Qty shortage	3		Miss Counting by	2.	NA	- Manual verify	5	30	None						$\overline{}$
CHECK	(CV)	Ç.,g.			Assembly or BI			box label LOT#,									i
Visual	,				Site			device #, box									i
Mechanical only								quantity against									i
applies to								packing list & SFC									i
Assembly & BI								- Accept on zero									i
awstock)								discrepancy (6)									i
								- 100% Count Qty									i
								by Test operator									i
								(5)									l
	Raw stock issue	Marking	3		Device mixed at	3	NA	- Sampling	5	45	None						_
		mismatch with			Assembly or BI	,	13/1	Marking inspection	-	13	Tione						ı
		System/shop			process			during incoming									ı
		order			r			check (5)									ı
								. /									i

												,					
Item:	Burn In/Final Te	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FM	1				
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,I	Dong	Gao,Liang Yang	.W	ei Chen,HONGZH	II REN,LINGXU <i>A</i>	AN I	XU,S	Sinbad Liu, Peng D	06-Sep-13	(Rev.)				
		· · · · · · · · · · · · · · · · · · ·			, , ,	,	·	·			, ,	•	· `				
													Action F	Resu	lts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	0	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	С	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	С	Prevention	Detection	T	N		Completion Date		V	C	T	N
•				s	of Failue							•					
				s													
	V/M Defect	-Visual	8		V/M defect	2	NA	- Sampling V/M	4	64	None					1	
		mechanical failure			introduced by			inspection during									
		(6)			Assembly or BI			incoming check (5)									
		-Customer			process			- 100% Marking									
		application						check by Vision									
		failure(8)						system in									
								Packaging									
								process(4)									
			Ш														
	Lot Combination	Yield Loss (7)	8		Mixed with Other	1	Config lot combine	- ATE Test (3)	3	24	None						
	by mistake	Customer line pull			device		rule in SFC system										
shop order  1. Machine		(8)															
oreparation																	
2. Start lot																	
3. Electrical																	
parameters tests																	
4. End lot																	
(Hot/Cold/Room)																	
		ĺ			ĺ		1			I	1						

		POTE	N.T.	IA	LFAILUR	(E	MODE AN	D EFFEC	15	Al	NALYSIS	(FMEA)		1 ago		JI <del>T</del> (	5
Item:	Burn In/Final Te	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FN	Л				
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zh	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZH	II REN,LINGXU	AN 2	XU,S	Sinbad Liu,Peng I	06-Sep-13	(Rev.)				
													•				
													Action F				
Process	Potential Failure	Potential	S	C	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	O	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/		Process Controls	Process Controls		P	Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				s	of Failue									l l			,
				s													ı
			8		mixed with other	1	Config lot combine	-lot informaiton	4	32	None						
					trace code		rule in SFC system	and marking check						l l			,
								post combination						l l			,
								(6)						l l			,
								-100% Count Qty						1			,
								by Test operator						l l			,
								before test(5) -100% auto VM						l l			,
								inspection in						1			,
								Packaging process.						l l			,
								(4)						l l			,
																	1
	Expired BI	Infant mortality,	8		Lot staged for too	1	Daily WIP review	- Auto hold lot	2.	16	None			一			
	window	fail electrical test			long after BI	ľ	by mfg and	with expired BI	Ĩ	10	TVOILE			l l			,
		during board					planner. Test	window (2)						l l			,
		assembly (8)					priority given to	` '						1			,
							material with BI							l l			,
							window. Expected							i l			,
							BI expiry date can							i l			,
							be viewed in							1			,
							genesis through lot							i l			,
							enquiry screen							Ιl			, ,
														l			,
	Wrong machina	Foil 1st orticle	2		Heaverong toster	11	Listed Testan	Operator about	1 1	2	Mono						

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information on

Test program is

Listed handler

information on

configed by tester

TSO

TSO

Use wrong

handler

tester vs. TSO

during setup (5)

- Program auto

Handler vs. TSO

during setup (5)

30

None

verify during download (1) - Operator check

check (3)

test (2)

Unable to perform

setup

	,		
Item: Burn In/Final Test/Test Backend	Control Number/Issue: 8	83MCT00018A/	/AY
Type: Design _x_ Process	Company, Group, Site/Business Unit: 1	Freescale, TJN-F	FM
Prepared By: Liang Yang	FMEA Date:	27-Jun-01	(Orig.)
Core Team: Peg Tang, ZJ-TEST2 Hu, Peter Zhang, Do	ong Gao,Liang Yang,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng D	06-Sep-13	(Rev.)
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													Action I	Resu	lts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	0	D	F
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	$\mathbf{C}$	Е	F
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	$\mathbf{C}$	Т	N
				s	of Failue											l	
				s												l	
			3		Wrong loadboard	3	Engineer create	- Manual visual	5	45	None						
					identification		loadboard ID and	verification on								l	
								loadboad ID								l	
							before releasing to	0								l	
							production (applies									l	
							for NPI as well)	M (5)								l	
			2		*** 1 1	2	374	0.1.0	_	~ 4	XX 1 1.1 TD	W : CI				$\vdash$	₩
			3		Wrong shoporder loadboard ID	3	NA	- QA Document Audit (6)	6	54	Work with IT team to convert	Wei Chen R65950/06-30-				l	
					setup			Audit (0)			LB information to					l	
					setup						SFC system.	2014				l	
											Sev=3, Occ=2,					l	
											Det=6, RPN=36					l	
			3		Tray loaded in	1	Poka Yoke	- Auto alarm for	2	6	None					$\vdash$	T
					wrong orientation		mechanism on	wrong orientation								l	
							Handler	(2)								l	
								- ATE Test (3)								<u></u>	
	Wrong test	Yield Loss (7)	8		Error during	2	SC2 auto	- QC in line gate	4	64	None						
	temperature	Customer line pull	1		manual		*	(4)								l	
		(8)			temperature		loading	- QA Document								l	
					selection		(except MST)	Audit (6)								l	
								- QA shiftly audit								l	
				I		l	1	(8)				ĺ				ı	1

1 0 121 (1112 1112)	
Item: Burn In/Final Test/Test Backend	Control Number/Issue: 83MCT00018A/AY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Liang Yang	FMEA Date: 27-Jun-01 (Orig.)
Core Team: Peg Tang, ZJ-TEST2 Hu, Peter Zhang, Dong Gao, Liang Y	ang,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng Γ 06-Sep-13 (Rev.)

													Action I	Resi	ılts		
Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	S E V	C 1 a s	Potential Cause(s)/ Mechanism(s) of Failue			Current Design/ Process Controls Detection		R P N	Recommended Action(s)	Responsibility & Target Completion Date	Actions Taken & Effective Date	S E V		Е	P
			8		Wrong O/I configuration setup	3	Dedicate engineering personel to perform O/I configuration	- QA Document Audit (6) - Auto-trigger on missing configuration to respective PE through scheduled auto database check (3)	3			Liang Yang R57253/05-30- 2014					
		Customer Line pull (8) Yield Loss (7)	8		TSO not updated timely to reflect program revision	1	Only effective version of Test program is available in Server	-Auto verify program information before test start (2) - First 200 units yield check(5) - QA Document Audit (6)	2	16	None						
			8		Program selection error	2	Listed test     program     information on     TSO;     Listed handler     information on     TSO;     Auto-program     loading except for     A5 & MST	- QA Document Audit (6) - Buddy check before test (7) - QC in line gate (4) - QA shiftly audit (8)	4	64	None						

								_					Action I				
Process	Potential Failure	Potential	S	C	Potential	О		Current Design/			Recommended	Responsibility &	Actions Taken &	S	O		R
Function/ Requirements	Mode	Effect(s) of Failure	E V	l a s	Cause(s)/ Mechanism(s) of Failue	C C	Process Controls Prevention	Process Controls Detection	E T		Action(s)	Target Completion Date	Effective Date	E V	C C	E T	P N
			8	S	SPV Program selection error	1	program reside in SPV 2. Auto SPV	- QC in line gate (4) - QA Document Audit (6) - QA shiftly audit (8)	4	32	None						
			8		Wrong O/I configuration setup	2	configuration Download Gen2Spec parameters to auto-	- QA Document Audit (6) - Auto-trigger on missing configuration to respective PE through scheduled auto database check (3)	3	48	None						
	ESD/EOS	Customer Line pull (8) Yield Loss (7)	8		-Wrist strap and/or shoes function fail	1	, ,	-Yield limit and SBL check (3) -JVT test at last insertion (3)	3	24	None						
			8		No grounding (work station / rack)	1	-Quarterly check	-Yield limit and SBL check (3) -JVT test at last insertion (3)	3	24	None						

		IOIL	11.		LIAILUN	T'	MODE AN	DEFFEC.	IO	A	ALIBID						
Item:	Burn In/Final Tes	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process				•		Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FM	1				
Prepared By:										-	FMEA Date:	27-Jun-01	(Orig.)				
		ST2 Hu,Peter Zh	ang,	Dong	g Gao,Liang Yang	,W	ei Chen,HONGZE	H REN,LINGXU	AN I	XU,S	Sinbad Liu, Peng I		(Rev.)				
		,	,		, , ,	<i></i>	,	<u>.</u>		ĺ	, &		.` ′				
													Action I	Resu	lts		
Process	Potential Failure	Potential	S	С	Potential	0	Current Design/	Current Design/	D	R	Recommended	Responsibility &				D	R
Function/	Mode	Effect(s) of	Ē	1	Cause(s)/		Process Controls				Action(s)	Target	Effective Date	E			P
Requirements	141046	Failure	V	a	Mechanism(s)	C		Detection	Т	N	riction(b)	Completion Date	Effective Bute	V		T	
requirements		Tulluic	1	S	of Failue	~	Trevention	Detection	1	11		Completion Date		•		1	11
					Of Failue												
			0	S	т .	1	TT 1 1 4 1 11	00: 1:	2	2.4	NT.						
			8		Inaccurate	1	Use bracket to hold	-	3	24	None						
					placement for ionizer		ionizer at a specific correct place	(4) - High electrical									
					IOIIIZCI		correct place	fall out at next									
								insertion for									
								leakage or idd									
								failure (3)									
								- JVT test at last									
								insertion (3)									
			0		Testers / Handlers	2	Check grounding	- JVT test at last	3	48	None						
			0		environment	_		insertion (3)	3	40	None						
					environment		properly installed	insertion (3)									
							during half year										
							PM										
			Q		Spike voltage on	1	Spike check during	Viald limit and	3	24	None				-	$\dashv$	
			0		the DC	1	NPI release	SBL check (3)	3	24	INOME						
					measurement		INI I ICICASC	-JVT or equivalent									
					measurement			test methodology									
						ı	1	icsi memodology	1								

(3)

(3)

continuity check

Loadboard PM

buyoff and

during Loadboard

Loadboard traces 2

shorted

-Yield limit and

-JVT or equivalent test methodology

SBL check (3)

48

None

POIENTIAL FAII	LUKE MODE AND EFFECTS ANALYSIS (	rvica)	
Item: Burn In/Final Test/Test Backend	Control Number/Issue:	83MCT00018A/A	AY
Type: Design _x_ Process	Company, Group, Site/Business Unit:	Freescale, TJN-FI	M
Prepared By: Liang Yang	FMEA Date:	27-Jun-01	(Orig.)
Core Team: Peg Tang, ZJ-TEST2 Hu, Peter Zhang, Dong Gao, Lian	g Yang, Wei Chen, HONGZHI REN, LINGXUAN XU, Sinbad Liu, Peng D	06-Sep-13	(Rev.)
			Action Results

													Action I			
Process	Potential Failure	Potential	S	С	Potential	О					Recommended	Responsibility &			О	
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls				Action(s)	Target	Effective Date	Е		E
equirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T
				s	of Failue											
				s												
	Product	Customer Line	8		-Mix of rawstock	4	-Handle only one	-Quantity count (6)	2	64	None					
	mixed/escaped	pull (8)			and tested units		lot in one station	-Sampling check								
		Yield Loss (7)			/ Mix of rawstock		-Perform marking	the marking (8)								
					and reject from		inspection before	-QC in line gating								
					different lot		lot start	(4)								
							-Material status identification	-100% auto VM								
							before/after	inspection in packaging process.								
							process	(4)								
							-Treat all	-Test program auto								
							uncomfirming	detect part								
							units and PE used	difference (3)								
							units as rejects	-Optimize ECID								
							- Proper labeling	system to auto hold								
							using lot	material if the								
							identification	ECID doesn't								
							barcode	match between								
							- Pending rack,	different insertion								
							Input & output	(2)								
							rack with proper									
							labeling - Label all work									
							place for proper									
							material									
							segregation									
							-All tested good									
							partial/full tube are									
							to be placed inside									
							or next to the									
							tested good box									
							-Identified color									
							tray/tube to collect									
	1						rejects									
							-Separate pending									
			Elect	ronic	versions are unc	onti	rack away from plied except when	accessed directly	froi	n [do	cument repositor	y].				
				Pri	nted versions are	unc	rack away from olled except when input rack by ontrolled except v	hen stamped "Co	ntro	lled (	Copy" in red.	=	Free	sca	e R	ev
							appearance and	1	1	I						

	Item: Burn In/Final Test/Test Backend  POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)  Control Number/Issue: 83MCT00018A/A														12 (	01 40	,
Item:	Burn In/Final Tes	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process				•		Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FN	1				
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TES	ST2 Hu,Peter Zh	ang,	,Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZH	II REN,LINGXU	AN :	XU,S	Sinbad Liu,Peng I	06-Sep-13	(Rev.)				
								•					•				
													Action I				
	Potential Failure	Potential	S		Potential		Current Design/					Responsibility &					
Function/	Mode	Effect(s) of	Е	1	Cause(s)/		Process Controls			P	Action(s)	Target	Effective Date	E	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				s	of Failue												
				S													
			8		Miss test insertion	1	Test flow configed		1	8	None						
					or in line gate		and auto controlled										
							by Genesis system	(1)									
								(1)									
			8		-Wrong binning	1	-Disable the bin	-QA document	4	32	None					+	
					setting of handler		setting button at	audit (6)									
							the operation	-QC in line gate									
							interface to prevent	(4)									
							misclick.										
							-Use SC2 auto										
							control bin setting										
			0	-	-Leftover unit in	2	-Clear machine	-Marking	3	48	None					+	
			0		equipment	2	before and after	inspection for first	3	40	None						
					equipment		test	200 units (5)									
							-Lot count before	-Quantity count (6)									
							start testing	-Using SC2 auto									
								count lot quantity									
								except MST, A5									
							_	(3)									
							validation										
						_	77 1 1100		_	22					_	_	
			8	1	-speed sort device	1	<ul> <li>-Using different</li> </ul>	<ul> <li>-QA document</li> </ul>	4	32	None						

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audit (6) -QC in line gate

(4)

color tray/tube to

replace different color clip for

material identification

mixed

		POIE	N I	IA.	LFAILUK	L	MODE AN	DEFFEC	13	Al	NAL Y 515 (	(FMLA)	•	uge	15	01 .	0
Item:	Burn In/Final Tes	st/Test Backend							C	Contr	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process						Company,C	Grou	up,Si	te/Business Unit:	Freescale, TJN-FN	1				
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang, ZJ-TES	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZI	II REN,LINGXUA	N Z	XU,S	Sinbad Liu,Peng I	06-Sep-13	(Rev.)				
								_			_	-					
													Action I	₹esτ	ılts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	С	T	N
•				s	of Failue							Î		ı '			
				s										i '			
			8		-Wrong customer code key in for factory programming product	1	-Add password verification to guaratee correct customer code input -Add customer code check on gate test	audit (6) -QC in line gate (4) -100% EEV test (3)			None						
			8		-Engineer/ Techincian mishandling during on line debug	1	-Handle only one lot in one station -follow on line debug instruction -Material status identification before/after process	-Quantity count (6) -Sampling check the marking (8) -QC in line gate (4)	4	32	None						

-Treat PE used units as rejects -System auto clear testsite when quit engineer testing mode and sort all verification units into reject tray

Item: Burn In/Final Test/Test Backend	Control Number/Issue: 83MCT00018A/AY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-FM
Prepared By: Liang Yang	FMEA Date: 27-Jun-01 (Orig.)
Core Team: Peg Tang,ZJ-TEST2 Hu,Peter Zhang,Dong Gao,Liang Yan	g,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng [ 06-Sep-13 (Rev.)

													Action I	Resi	ılts	
Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	S E V	C 1 a s s	Potential Cause(s)/ Mechanism(s) of Failue  Leftover unit on	O C C	Current Design/ Process Controls Prevention  -Check recycle tray	Process Controls Detection	E T	R P N	Recommended Action(s)  None	Responsibility & Target Completion Date	Actions Taken & Effective Date	S E V	O C C	P
					recycle tray		before putting them into machine -Standard operation of recycle tray checking -partial tray alert	inspection in								
			8		Battery Backup Unit (BBU) memory full causing Castle handler fail to pickup rawstock unit and indexed to main tray buffer as an empty tray	1	Castle handler firmware upgraded to auto clear BBU once 'handler empty' status is prompt.	<ol> <li>QC in line gate.</li> <li>(4)</li> <li>QA shiftly audit</li> <li>(8)</li> <li>Quantity count</li> <li>(6)</li> </ol>		32	None					
			8		Bin1 units from previous insertion are not cleared from output bin1 stacker / rack	5	NA	- QC in line gate. (4) 2. QA shiftly audit (8) 3. ECID detection method for applicable products (2) 4. Quantity count (6)	2			Peng Lin R65908/06-28- 2014				

		POTEN	T	[A]	L FAILUR	E	MODE AN	ID EFFECT	ΓS	Al	NALYSIS (	(FMEA)	P	age	15 c	of 46	5
Item:	Burn In/Final Tes	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process						Company,0	Gro	up,Si	te/Business Unit:	Freescale, TJN-FM	1				
Prepared By:	Liang Yang					_					FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang, ZJ-TES	T2 Hu,Peter Zh	ang,	Donş	g Gao,Liang Yang	z,W	ei Chen,HONGZH	II REN,LINGXU <i>A</i>	AN 2	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)				
								-					•				
													Action R				
Process	Potential Failure	Potential	S	C	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				S	of Failue									ıl			
				S										ı			
			8		Reject mixed into	2	1. Rawstock and	-QC in line gate.	3	48	None						
				i	good during		tested material	(4)						ıl			
				ı	machine		segregation by	- QA shiftly audit						ıl			
					downtime eg.		1	(8)						ıl			
				l	During		machine down	- ECID detection						ı			
				i	maintenance	İ	2. Technician to	method for						ıl			
				i	ļ		•	applicable products						, I			
				ı		1	material for setup	(3)									

during maintenance. All units are to be placed back into rawstock material 3. Scrap jammed

units
4. Centralized
reject scrapping in
QA area after QA
validation

Any engineering

lot need to use

engineering lot

Log in MDR for

engineering lot

class to ship as normal production lot class.

class.

Use production

purpose causing

production lot to

lot shipped as

lot class for

engineerig

customer.

Non qualified

engineering lot

shipped to

customer

Customer

(8)

application failure

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All engineering lot 2

class require MDR

prior shipment. (2)

32

None

	POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)														16	of 40	)
Item:	Burn In/Final Tes	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FN	1				
Prepared By:						_					FMEA Date:		(Orig.)				
Core Team:	Peg Tang,ZJ-TES	ST2 Hu,Peter Zh	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZI	II REN,LINGXU	AN 2	XU,S	inbad Liu,Peng I	06-Sep-13	(Rev.)				
					_								Action F		_		
Process	Potential Failure	Potential	S	C	Potential	О	U	Current Design/				Responsibility &					R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C		Process Controls		P	Action(s)	Target	Effective Date	Е	C	Е	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				S	of Failue												
				S													
	Low yield or SBL	- Yield loss (7)	7		Tester out of	1	- Tester calibration		2	14	None						
	over limit				calibration		during regular PM	control in Genesis									
	(DC, functional, parametric,							(3) - SBL limit control									
	open/short,							(3)									
	electrical)							-Auto calibration									
								every program									
								loading (2)									
								-Diagnostic during									
								PM (5)									
			7		-Wrong binning	1	-Disable the bin	-QA document	4	28	None						
					setting of handler		setting button at	audit (6)									
							the operation	-QC in line gate									
							interface to prevent	(4)									
							misclick.										
							-Use SC2 auto										
							control bin setting										
			7		- Handler setup	1	- Handler regular	- Yield limit	3	21	None						
					problem		PM	control in Genesis									
							- Set up check	(3)									
								- SBL limit control									
								(3)									
								- First 200 units									
			1					yield check (4)	1								

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- Yield limit

(3)

control in Genesis

- SBL limit control

- First 200 units yield check (4)

None

- Load board

regular PM

Load Board

problem

			·	
Item: Burn In/Final To	est/Test Backend	Control Number/Issue:	83MCT00018A	/AY
Type: Design	_x_ Process	Company, Group, Site/Business Unit:	Freescale, TJN-F	FM
Prepared By: Liang Yang		FMEA Date:	27-Jun-01	(Orig.)
Core Team: Peg Tang,ZJ-TE	EST2 Hu,Peter Zhang,I	Dong Gao,Liang Yang,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng [	06-Sep-13	(Rev.)

					-								Action I				
Process	Potential Failure	Potential	S		Potential	О	_	Current Design/			Recommended	Responsibility &		S			
Function/ Requirements	Mode	Effect(s) of Failure	E V	1 a s s	Cause(s)/ Mechanism(s) of Failue	C	Process Controls Prevention	Process Controls Detection	E T		Action(s)	Target Completion Date	Effective Date	E V	C C	E T	l
			7		- Tester board problem	1	- Tester regular PM	- Yield limit control in Genesis (3) - SBL limit control (3) - First 200 units yield check (4)	3	21	None						
			7		- Poor contact at DUT socket (device under test)	3	- Contact interface regular replacement	- Yield limit control in Genesis (3) - SBL limit control (3) - First 200 units yield check (4)	3	63	None						
		-Visual mechanical failure (6) -Customer application failure(8)	8		-Device misplacement by hanlder	2	-Half year PM -Shiftly check handler by setup checklist	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)		64	None						
			8		Unit overpress during test	1	Input quad hardstop to prevent overpress	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)		32	None						

TOTENTIAL FAILU	KE MODE AND EFFECTS ANALISIS (	rwitza)	
Item: Burn In/Final Test/Test Backend	Control Number/Issue: 8	3MCT00018A/	'AY
Type: Design _x_ Process	Company, Group, Site/Business Unit: I	Freescale,TJN-F	M
Prepared By: Liang Yang	FMEA Date:	27-Jun-01	(Orig.)
Core Team: Peg Tang, ZJ-TEST2 Hu, Peter Zhang, Dong Gao, Liang Ya	nng,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng [	06-Sep-13	(Rev.)
		•	Action Results

					ī		T	ī			1	ī	Action I		_		
	Potential Failure	Potential	S		Potential	О		Current Design/					Actions Taken &		О		F
Function/	Mode	Effect(s) of	Е	1	Cause(s)/		Process Controls				Action(s)	Target	Effective Date			Е	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	Ì
				s	of Failue												l
				S													ı
			8		Bad socket/pogo	2	-Hard stopper	-In-process	4	64	None						ı
					pin		configuration	sampling check (8)									ı
							- Load board	-100% auto VM									l
							-	inspection in									l
								packaging process (4)									ı
							replacement	(4)									l
			8		ATU causing	2	1. Use	-In-process	4	64	None					$\dashv$	Г
					drop units	_	CASM/CAIM to	sampling check (8)	_	0-1	Tione						ı
							cycle ATU and	-100% auto VM									l
							observe for	inspection in									l
								packaging process									l
							-	(4)									l
							during handler PM										l
							2. Designed tray										ı
							catcher with loaded spring										ı
							3. Add mounting										ı
							plate to tighten										l
							door sensor										ı
																	l
			8		Unit misplaced in	2	Handler buyoff	-In-process	4	64	None			H		$\dashv$	Γ
			ľ		tray at output		after PM and	sampling check (8)								, ,	ı
					handler		conversion	-100% auto VM									l
							sort xyz alignment	inspection in								, ,	ı
							jig	packaging process								, ,	ı
								(4)								, ,	ı
																	ı

		POIL	<b>1</b>	IAJ	LTAILUN	.L	MODE AN	(DEFFEC.	19	$\mathbf{A}$	VAL I DID	(FIVILA)						
Item:	Burn In/Final Tes	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	·Υ					
Type:	Design	_x_ Process						Company,	Groi	up,Si	te/Business Unit:	Freescale, TJN-FM	Л					
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)					
Core Team:	Peg Tang,ZJ-TES	ST2 Hu,Peter Zh	ang,	,Dong	g Gao,Liang Yang	z,W	ei Chen,HONGZH	II REN,LINGXU/	AN I	XU,S	Sinbad Liu,Peng I	06-Sep-13	(Rev.)					
					-			•			_		1					
													Action I	₹esul	lts			1
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R	1
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	Е	P	ļ
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date	1	V	C	T	N	ļ
				S	of Failue							_		1 1				
				s														Į
			8		- Operator handles	2	- Certify operators'	-In-process	4	64	None			П	寸	一		1
					material			sampling check (8)										1
					manually.		yearly exam to	-100% auto VM										1
							check	inspection in	'					1				
								packaging process						1				
							1	(4)										
							as VM reject and											
							scrap.		'					1				ļ
			丄	<b>↓</b>		L				<u>↓</u>				Ш	_			
			8		-Frost inside test	2	1	-In-process		64	None			1				
					chamber		periodically	sampling check (8)	'					1				ļ
							-Use air pressure to		'					1				ļ
							*	inspection in	'					1				ļ
							_	packaging process	'					1				ļ
							1	(4)	'					1				ļ
							-System auto warm up cold		'					1				ļ
							temperature		'					1				ļ
					!	1	1 11		'					1				Į

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-In-process

sampling check (8)

-100% auto VM

inspection in packaging process

None

SC2 Auto-defrost

-Add chamfer at

-Perform Track inspection when replacement during

soak booster track and singulator

function

track

PM

-Hit by damaged

track corner

		TOTE	1 1	111.	DIME	<u> </u>	MODETAL	D EITEC.		1 1	WILL DID	(I IVILIII)					
Item:	Burn In/Final Te	est/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process						Company,	Gro	up,Si		Freescale, TJN-FN					
Prepared By:						_					FMEA Date:		(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen, HONGZH	II REN,LINGXU	AN 2	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)				
								•									
													Action F	Resu	ılts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	С	Process Controls		Е	P	Action(s)	Target	Effective Date	Е	С	Е	P
Requirements		Failure	V	a	Mechanism(s)	С		Detection	Т	N		Completion Date		V	С		
•				s	of Failue							•					
				s													
	Ball damage	-Visual	8		Bad socket/pogo	2	-Hard stopper	-In-process	4	64	None					$\Box$	
	g.	mechanical failure			pin		configuration	sampling check (8)									
		(6)					- Load board	-100% auto VM									
		-Customer					regular PM	inspection in									
		application					- Contact interface	packaging process									
		failure(8)					regular	(4)									
							replacement										
			8		Unit jam at core	2	1. Periodic handler	-In-process	4	64	None						
					section		PM to minimize	sampling check (8)									
							jamming	-100% auto VM									
								inspection in									
								packaging process									
							unit that jammed at	(4)									
							core section										
			_					_									
			8		-Device	2	-Half year PM	-In-process	4	64	None						
					misplacement by		-Shiftly check	sampling check (8)									
					hanlder		handler by setup	-100% auto VM									
							checklist	inspection in packaging process									
								(4)									
								(4)									
			8		Unit overpress	1	Input quad	-In-process	4	32	None					H	
			0		during test	1		sampling check (8)	ľ	22	110110						
					daring test		overpress	-100% auto VM	l		1						
							o . crpress	inspection in									
								packaging process									
								(4)									

101EMINE IME	THE MODE IN THE ETT LETS MINIETS (	11111111	
Item: Burn In/Final Test/Test Backend	Control Number/Issue: 8	3MCT00018A/	AY
Type: Design _x_ Process	Company, Group, Site/Business Unit: I	Freescale,TJN-Fl	M
Prepared By: Liang Yang	FMEA Date:	27-Jun-01	(Orig.)
Core Team: Peg Tang, ZJ-TEST2 Hu, Peter Zhang, Dong Gao, Liang Yar	ng,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng D	06-Sep-13	(Rev.)
			Action Results

											Action F	kesu	Its		
Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	S E V	Potential Cause(s)/ Mechanism(s) of Failue		Current Design/ Process Controls Prevention		P	Recommended Action(s)	Responsibility & Target Completion Date		S E V		D E T	P
			8	Unit misplaced in tray at output handler	2	Handler buyoff after PM and conversion sort xyz alignment jig	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	64	None						
			8	FM on substrate	1	2. Auto-defrost for	sampling check (8) -100% auto VM inspection in	32	None						
			8	- Operator handles material manually.	2	yearly exam to check - Treat manual	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	64	None						

		POIL	11	IA	LFAILUK	L	MODE AN	D EFFEC.	19	AI	ALL 1919 (	(FIVILA)					
Item:	Burn In/Final Te	st/Test Backend							C	Contro	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process				_		Company,	Grou	up,Si	te/Business Unit:	Freescale, TJN-FM	1				
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZF	II REN,LINGXU	AN 2	XU,S	inbad Liu,Peng D	06-Sep-13	(Rev.)				
•								-									
													Action I	Resu	lts		
Process	Potential Failure	Potential	S	C	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/			Process Controls	E	P	Action(s)	Target	Effective Date	Е			P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				s	of Failue												
				s													
	Crack/chip	- Reliability	8		-Wrong handler	1	-Hard stopper	-In-process	2	16	None						
		failure (8)			adjustment		configuration	sampling check (8)									
		-Electrical failure						-Hard stopper auto									
		(8)						alarm (2)									
		-Visual mechanical failure															
		(6)															
		(0)	0		T (1 1)	1	TT 1 .	T		1.6	N						
			8		-Incorrect bushing on L/B	1	-Hard stopper configuration	-In-process sampling check (8)	2	16	None						
					Oli L/B		Configuration	-Hard stopper auto									
								alarm (2)									
								(=)									
			8		- Operator handles	2	- Certify operators'	- Tray gap check	4	64	None						
					material manually		operation skill and	(6)									
					in tray.		yearly exam to	-100% auto VM									
							check	inspection in									
							- Treat manual	packaging process									
							operated material	(4)									
							as VM reject and										
							scrap Put a empty tray										
							on the top before										
							move out material										

from machine

TOTENTIAL PARENCE MODE	THE EFFECTS MINIBIDIS (FINERY)	
Item: Burn In/Final Test/Test Backend	Control Number/Issue: 83MCT00018A	/AY
Type: Design _x_ Process	Company, Group, Site/Business Unit: Freescale, TJN-1	FM
Prepared By: Liang Yang	FMEA Date: 27-Jun-01	(Orig.)
Core Team: Peg Tang, ZJ-TEST2 Hu, Peter Zhang, Dong Gao, Liang Yang, Wei Chen, HON	NGZHI REN,LINGXUAN XU,Sinbad Liu,Peng Γ 06-Sep-13	(Rev.)
		Action Results

	1	ī			ī	_	1				1	1	Action I				_
Process	Potential Failure		S		Potential	О	_	Current Design/			Recommended	Responsibility &		S	О		
Function/	Mode	Effect(s) of	Е	1	Cause(s)/		Process Controls				Action(s)	Target	Effective Date	E		E	
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	
				S	of Failue												l
				S													
	Sliver &	Short circuit or	8		High plating	2	Socket cleaning	- Yield limit	3	48	None					П	ĺ
		leakage (8)			material build up		and replace	control in Genesis									l
	pogo socket only)				at test socket		regularly	(3)									l
								- SBL limit control									l
								(3) - First 200 units									l
								yield check (4)									l
								-V/M gate									l
								sampling check (8)									l
																ļ	l
	Pogo Burr	Visual	6		Mechanical	2	Check for socket	- V/M gate	5	60	None					$\dashv$	r
		Mechanical			Contact offset on			sampling check (8)									l
		Failure (6)			device lead due		during PM.	- First 200 units									l
					wear and tear of		Replace socket if	V/M check (5)									l
					test socket pogo		pogo holes found										l
					holes		wear and tear									ļ	l
	D 11 1	0.11. 122.	0				D 1 1 DM	77/2.6	-	40	) ·					$\dashv$	L
	U	Solderability	8		test finger deformation	1	-Board regular PM - Check Pogo	<ul> <li>V/M gate sampling check (8)</li> </ul>		40	None						l
	surface	Failure (8)			deformation		pin/socket	- First 200 units									l
	surface						befor&after each	V/M check (5)									l
							use	vivi check (5)									l
																ļ	l
	Foreign Matter On	Solderability	8		Dirt accumulated	1	1. handler cleaning	- V/M gate	5	40	None				一	寸	Γ
		Failure (8)	1		in handler boat		during shift start	sampling check (8)								ļ	l
			1				2. boat clean	- First 200 units								ļ	l
			1				during conversion	V/M check (5)									l
			1													ļ	l
																	ĺ

Item:	Burn In/Final Tes	st/Test Backend					(	Contr	ol Number/Issue:	83MCT00018A/A	Υ					-		
		_x_ Process				•		Company,				Freescale, TJN-FN						-
Prepared By:		_						1 3,			FMEA Date:		(Orig.)					_
Core Team:	Peg Tang,ZJ-TES	ST2 Hu,Peter Zh	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZI	II REN,LINGXU	٨N	XU,S	Sinbad Liu,Peng I	06-Sep-13	(Rev.)					
																		_
	I I		-	_	T =	T _	T	T =	-		T	I=	Action F			-	_	_
Process	Potential Failure	Potential	S	C	Potential		Current Design/						Actions Taken &			D		
Function/	Mode	Effect(s) of	Е	1	Cause(s)/		Process Controls				Action(s)	Target	Effective Date	Е	C	Е	P	
Requirements		Failure	V	a	Mechanism(s)	С	Prevention	Detection	T	N		Completion Date		V	C	1	N	
				S	of Failue												ĺ	
			8	S	II.:4 J4 -£	2.	1. Ct Di. 1 t	- V/M gate	4	64	N						⊢	_
			8		Unit drop out of tray	2	Strap Bin1 tray with cover tray	sampling check (8)	4	04	None						ĺ	
					liay		right after testing	- First 200 units									ĺ	
							2. Unstrap	V/M check (5)									ĺ	
							rawstock bundle	-100% auto VM									ĺ	
							just before loading										ĺ	
							to ATU	packaging process									ĺ	
							3. Use CASM/CAIM to	(4)									ĺ	
							cycle ATU and										ĺ	
							observe for										ĺ	
							mechanical										ĺ	
							binding issue										ĺ	
							during handler PM										ĺ	
							(ATU issue)										ĺ	
							4. Designed tray										ĺ	
							catcher with										ĺ	
							loaded spring										ĺ	
							(ATU issue) 5. Standardize tray										ĺ	
							latch spring to										ĺ	
							0.32mm diameter										ĺ	
							(ATU issue)										ĺ	
							6. Add mounting										ĺ	
							plate to tighten										ĺ	
							door sensor (ATU										ĺ	
							issue)										ĺ	
							7. Treat dropped										ĺ	
							unit as reject										ĺ	
																	ĺ	
											1				l		ĺ	

Item: Burn In/Final Test/Test Backend	Control Number/Issue: 8	83MCT00018A/	'AY
Type: Designx_ Process	Company, Group, Site/Business Unit: I	Freescale,TJN-F	M
Prepared By: Liang Yang	FMEA Date:	27-Jun-01	(Orig.)
Core Team: Peg Tang, ZJ-TEST2 Hu, Peter Zhang	, Dong Gao, Liang Yang, Wei Chen, HONGZHI REN, LINGXUAN XU, Sinbad Liu, Peng C	06-Sep-13	(Rev.)
	<u> </u>		_

												Action Results					
Process	Potential Failure		S		Potential	О	_	Current Design/				Responsibility &		S			
Function/ Requirements	Mode	Effect(s) of Failure	E V	l a	Cause(s)/ Mechanism(s) of Failue	C C	Process Controls Prevention	Process Controls Detection	E T		Action(s)	Target Completion Date	Effective Date	E V	C C	E T	
			8	S S	Usage of fibrous	1	Banned cotton	- QA shiftly audit	5	40	None						
			0		material at production floor	1	bud, fibrous glove and cloth from production floor	(8) - V/M gate sampling check (8) - First 200 units V/M check (5)									
			8		FM stick on pogo pin	3	Socket cleaning and replace if necessary	<ul><li>Yield limit control in Genesis</li><li>(3)</li><li>SBL limit control</li><li>(3)</li></ul>		48	None						
			8		FM from incoming/environ ment dropped to staging trays causing FM to attach to units when the trays are used.	1	Top tray cover for trays during staging period to prevent FM	-V/M gate sampling check (8) -100% auto VM inspection in packaging process (4)		32	None						
	Foreign Matter On Package Body	Solderability Failure (8)	8		FM from incoming/environ ment dropped to staging trays causing FM to attach to units when the trays are used.	1	Top tray cover for trays during staging period to prevent FM	Detection at TBE using 3x inspection (6)		48	None						

			•									,					
Item:	Burn In/Final Te		Control Number/Issue: 83MCT00018A/AY														
Type: Design _x_ Process							Company, Group, Site/Business Unit: Freescale, TJN-FM										
Prepared By: Liang Yang											FMEA Date:		(Orig.)				
Core Team: Peg Tang, ZJ-TEST2 Hu, Peter Zhang, Dong Gao, Liang Yang							ei Chen, HONGZE	II REN,LINGXU <i>A</i>	AN :	XU,S	Sinbad Liu, Peng D	06-Sep-13	(Rev.)				
		· · · · · · · · · · · · · · · · · · ·			, ,	,	· · · · · · · · · · · · · · · · · · ·	•			, ,	•					
						Action Results											
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	O	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	С	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	С	Prevention	Detection	Т	N		Completion Date		V	C	T	N
•				s	of Failue							•					
				s													
Laser mark	Missing mark	-customer	8		-Laser generator	1	-Machine auto	-First piece part	2	16	None						
		application failure			fail		check laser power	verification after									
		- 8					before marking.	marking(4)									
								-Machine auto									
								alarm when power									
								out of control(2)									
								-QA Gate(8)									
	Illegible mark	Customer	8		Inappropriate	2	Machine auto	-First piece part	2	32	None						
		application failure			laser power		check laser power	verification after									
		- 8					before marking.	marking(4)									
								- Machine marking 100% auto scan in									
								subsequent process									
								(4)									
								-QA visual									
								inspection 200									
								units/lot(8)									
								-Machine auto									
								alarm when laser									
								power									
								abnormal.(2)									

		POTEN	N.T.	IA	L FAILUK	$\mathbb{E}$	MODE AN	D EFFEC.	15	Al	NALYSIS	(FMEA)	1	agc	21	л т	U
Item:	Burn In/Final Te	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FN	1				
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TES	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZH	HI REN,LINGXU	AN 2	XU,S	Sinbad Liu,Peng I	06-Sep-13	(Rev.)				
		,			, , ,	,	•	•			, ,		.` ′				
													Action I	Rest	lts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	С		Process Controls			Action(s)	Target	Effective Date	Е		Е	
Requirements		Failure	V	a	Mechanism(s)	C		Detection	Т	N		Completion Date		V			N
1				s	of Failue							<b>1</b>					
				S													
			8		Laser generator	1	NA	-First piece part	2	16	None						
					worn out	1	1421	verification after	_	10	Tronc						
					worn out			marking(4)									
								- Machine marking									
								100% auto scan in									
								subsequent process									
								(4)									
								-QA visual									
								inspection 200									
								units/lot(8)									
								-Machine auto									
								alarm when laser									
								power									
								abnormal.(2)									
	Marking	Customer	8		Location pin	1	NA	-First piece part	4	32	None						
	misalignment	application failure			damaged			verification after									
		- 8						marking(4)									
								- Machine marking									

100% auto scan in subsequent process

-QA visual inspection 200 units/lot(8)

Itami	Burn In/Final Te		11.		LIAILUN	<b>.</b> L'	WIODE AIV	DEFFEC				83MCT00018A/A	V	_			
		_x_ Process						Company				Freescale, TJN-FM		—			
Prepared By:		_x_110cess						Company,	JIU	up,si	FMEA Date:		(Orig.)				
		ST2 Hu Peter Zha	no	Dong	Gao Liang Yang	w	ei Chen,HONGZH	II REN LINGXIIA	N.	XIIS			(Rev.)				
Core Team.	1 cg rang,25-12.	312 Hu,I Cici Zili	1115,	Dong	g Gao, Liang Tang	5, **	er enem, rrorvoza	H KEN,EHOKO7	1112	<b>AU</b> ,0	mioad Liu,i eng L	00-5ср-13	(Rev.)				
													Action R	₹esτ	lts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/		Process Controls			Р	Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	С	Prevention	Detection	T	N		Completion Date	ı	V		T	N
•				s	of Failue							•	ı				
				s													
	Wrong marking	Customer	8		Marking	1	-Auto load	-First piece part	4	32	None			П			
		application failure			information input		marking	verification after					ı				
		- 8			error during		information	marking(4)					į				
					manual operation			- Machine marking					ı				
								100% auto scan in subsequent process					ı				
								(4)					ı				
								-QA visual					ı				
								inspection 200					ı				
								units/lot(8)					ı				
0x Inspection	Burr&sliver on	-Visual	8		Shoulder	2	NA	-10x V/M gate (8)	2	32	None			П			
	shoulder/riser/	mechanical failure			damaged by BI			- 100% auto vision					ı				
	lead	(6)			(failure identified			inspection on					ı				
		-Customer			by KLM)			device (2)					ı				
		application											ı				
	D 11 10	failure(8)	0		TT '2 4 C 1 4	2	1 0	<b>N/M</b> (0)	2	22	NT.			Щ			
	Bend lead & coplanarity	-Visual mechanical failure	8		Unit out of pocket	2	Strap the tray     whenever moving	-V/M gate (8) - 100% auto vision	2	32	None						
	сорганатту	(6)					the material	inspection on					ı				
		-Customer						device (2)					ı				
		application					check tray gap	,					ı				
		failure(8)					before and after							, 1			
							strapping to ensure										
							no unit jump out							, 1			
							the pocket							, 1			

			1 1	<b>A</b> 7 <b>B</b> 3			MODETH	DELLE				,					
-	Burn In/Final Te	st/Test Backend										83MCT00018A/A					
Type:	Design	_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FM	1				
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TES	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZF	II REN,LINGXU <i>A</i>	AN I	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)				
•								•									
													Action I	Resu	ılts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	С	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	С		Detection	Т	N	, ,	Completion Date		V		Т	
1				s	of Failue							1					
				s													
			8		Mishandling the	2	1. Strap the tray	-V/M gate (8)	2	32	None						
					unit	<u> </u>	whenever moving	- 100% auto vision	_	-	Tione						
							the material	inspection on									
							2.Operator to	device (2)									
							check tray gap										
							before and after										
							strapping to ensure										
							no unit jump out										
							the pocket										
	Wrong orientation	-Customer	8		Unit replaced in	2	Pin1 reverification		1	16	None						
		application failure			misorientated		after unit	sampling check (8)									
		(8)			form		replacement	-Vision system									
								auto detect and									
								alarm (2)									
								-Auto-Pin 1 locate									
								system by									
								vision(1)									
								-Pin1 bar setting									
								for tray locate(1)									
										<u> </u>							
	Mixed product	-Electrical failure	8		Stray units at	2		., 8	2	32	None						
		(8)			inspection table		_	sampling check (8)									
		-Reliability failure					lot.	-Count quantity									
		(8)						per shop order (6)									
								- Vision 100%									
								inspection (2)						l			

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		TOTE	11		LIAILUN	112	MODE AN	DEFFEC.	10		NAL I DID	(I'IVIII/A)					
Item:	Burn In/Final Tes	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process				-		Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FM	Л				
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TES	ST2 Hu,Peter Zh	ang,	,Donş	g Gao,Liang Yang	g,W	ei Chen,HONGZH	II REN,LINGXU/	AN I	XU,S	Sinbad Liu,Peng I	06-Sep-13	(Rev.)				
								,					1				
													Action F	Resul	lts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е	l	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				s	of Failue							-					
				s				1				ļ					
			8		Swap Shop order	2	Process 1 lot at a	-System record the	2	32	None			H	寸	$\exists$	
							time	marking teach				ļ					
								history in test				ļ					
								summary, operator				ļ					
								100% check				ļ					
								summary(4)				ļ					
								-System auto check				ļ					
								and judge if				ļ					
								marking is correct				ļ					
								or not after key in				ļ					
								the actual marking				ļ					
								(2) 100% vision				ļ					
												ļ					
								inspection				ļ					
												ļ					
														Ш			
			8		Swap bundle	2	Process 1 lot at a	1. Lot no	2	32	None						
							time	verification on				ļ '	1 '	i I			

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barcode label vs TSO (3) 2. 100% vision scanning (2) 3. QA VM Gate

-10x V/M gate (8)

- 100% auto vision

inspection on

device (2)

32

None

(8)

10x Inspection

Burr&sliver on

shoulder/riser/

lead

-Visual

-Customer

application failure(8)

(6)

mechanical failure

Shoulder

by KLM)

damaged by BI

(failure identified

2 NA

		TOTE	11		LIAILUN	112	MODE AN	DEFFEC.	IO	AI	ALL 1 DID						
Item:	Burn In/Final Te	st/Test Backend				_			(	Contr	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FN	1				
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZH	II REN,LINGXU	AN I	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)				
													Action F				
Process	Potential Failure	Potential	S	C	Potential		Current Design/	_			Recommended	Responsibility &	Actions Taken &	S			
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е		Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				s	of Failue									ı			
				s										ı			
	Bend lead & coplanarity	-Visual mechanical failure (6) -Customer application failure(8)	8		Unit out of pocket	2	2.Operator to check tray gap before and after strapping to ensure no unit jump out the pocket	-V/M gate (8) - 100% auto vision inspection on device (2)		32	None						
			8		Mishandling the unit	2	1. Strap the tray whenever moving the material 2. Operator to check tray gap before and after strapping to ensure no unit jump out the pocket	-V/M gate (8) - 100% auto vision inspection on device (2)	2	32	None						

		1 0 121	1 -				111022111	ID BITEU	_~		11121010	(111111)					
Item:	Burn In/Final Te	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	·Υ				
Type:	Design	_x_ Process						Company,	Gro	up,Si	ite/Business Unit:	Freescale, TJN-FM	1				
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZF	HI REN,LINGXU	AN I	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)				
													Action R	Resu	lts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/		Process Controls	_			Action(s)	Target		Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	С		Detection	Т	N		Completion Date		v	С	T	
1				s	of Failue							<b>r</b>					
				s													
	Wrong orientation	-Customer	8		Unit replaced in	2	Pin1 reverification	-V/M gate	1	16	None			Н			
	Wrong orientation	application failure	-		misorientated	_	after unit	sampling check (8)	1	10	rone						
		(8)			form		replacement	-Vision system									
		(-)						auto detect and									
								alarm (2)									
								-Auto-Pin 1 locate									
								system by									
								vision(1)						1 1			
								-Pin1 bar setting						1 1			
								for tray locate(1)									
	Mixed product	-Electrical failure	8		Stray units at	2	Clear work station	-V/M gate	2	32	None			П			
		(8)			inspection table			sampling check (8)									
		-Reliability failure					lot.	-Count quantity									
		(8)						per shop order (6)						1			
								- Vision 100%									
								inspection (2)						1			

			<u> </u>	IA.	L FAILUK	L	MODE AN	DEFFEC				` /	1	50		01 1	
	Burn In/Final Te											83MCT00018A/A					
	_	_x_ Process						Company,	Grou	up,Si		Freescale, TJN-FN					
	Liang Yang										FMEA Date:		(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZF	II REN,LINGXUA	AN 2	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)				
													A .: T		1.		
D.	D ( ( 1E 1	D 4 41 1	С		D ( ( 1		[C + D + 7	C (D : /	Ъ	ъ	In 1.1	D 11.11. 0	Action R			ъ	D
Process	Potential Failure		S		Potential			Current Design/					Actions Taken &				
Function/	Mode	Effect(s) of	E	1	Cause(s)/	C		Process Controls		P	Action(s)	Target	Effective Date	E V	C C	E T	P
Requirements		Failure	V	a	Mechanism(s) of Failue	١	Prevention	Detection	T	N		Completion Date		v	C	1	IN
				S	of Failue												
			8	S	C C11	2	D 1 1-4 -4 -	C4	2	22	None				_		
			٥		Swap Shop order	2	Process 1 lot at a time	-System record the marking teach	2	32	None						
							time	history in test									
								summary, operator									
								100% check									
								summary(4)									
								-System auto check									
								and judge if									
								marking is correct									
								or not after key in the actual marking									
								(2)									
								100% vision									
								inspection									
			8		Swap bundle	2.	Process 1 lot at a	1. Lot no	2.	32	None						
					5 wap canale	<u> </u>	time	verification on	_	-							
								barcode label vs									
								TSO (3)									
								2. 100% vision									
								scanning (2)									
								3. QA VM Gate									
								(8)									
Bake	Mixed product	-Electrical failure	8		-Operator handles	3	-Ensure only one	-Count the quantity	4	96	Using bakeable	HONGZHI REN					
		(8)			the wrong device		lot in work table	for tube			tube to avoid	B06298/04-30-					
		-Reliability failure (8)	1		without check marking		for tube package Verify lot	package(6) -100% auto vision			mistake during tube to tube	2014					
		(0)	1	1	marking		- verify for	-100% auto vision		I	tube to tube	l l	4			1 1	

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inspection in

subsequence

process (4)

process

SEV=8, OCC=1,

DET=4, RPN=32

number/ magazine

number vs. shop

order

		POIL	<u> 1                                   </u>	IA.	LFAILUN	T.	MODE AN	DEFFEC	19	AI	NALISIS	(FWIEA)					
Item:	Burn In/Final Te	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FN	Л				
Prepared By:	Liang Yang					_					FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zh	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZF	II REN,LINGXU	AN 2	XU,S	Sinbad Liu,Peng I	06-Sep-13	(Rev.)				
													Action F				
Process	Potential Failure	Potential	S	C	Potential	О	U	Current Design/			Recommended	Responsibility &		S			
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C		P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				s	of Failue								,				
				s									,				
	Miss bake	-Reliability failure	8		-Operator forgets	2	-Follow TSO and	-Genesis system	2	32	None						
		(8)			to do bake step		SFC instruction	control (2)					,				
					and transfer the			-Buddy check (7)									
					material to the								,				
					next step.								,				
			0		Dlaga mua halra	2	-Different	Canasia avatam	2	32	None						
			8		-Place pre-bake units into post-	2	requirement lot	-Genesis system control (2)	2	32	None		,				
					bake units		stock in different	Control (2)									
					oute units		area										
	Time/Temperature	-Customer	8		-Wrong time and	1	-Fix timer and	-Auto check	2	16	None						
	incompetent	application failure			temperature		temperature	system alarm(2)									
		(8)					controller to auto-										
							monitor										
Dry air storage	Moisture out of	- Delamination	8		- Dry air	1	N/A	- Flow meter check	6	48	None						
	control	issue (8)			barometric			per setup checklist									
		-Customer			pressure low			(6)									
		application failure						- HIC monitor /									
		(8)						open the Dry air cabinet (6)									
	Miss Dry air	- Delamination	8		Omanatan fans -t-	2	-Follow SFC	` ′	2.	32	None				$\vdash$	$\vdash$	
	storage	issue (8)	ð		-Operator forgets to put the lot into	2	instruction.	-Buddy check (7) -Genesis system	2	32	none						
	Storage	-Customer			the Dry air		mou uction.	control (2)									

application failure

cabinet

		TOIL	1 1	<b>1</b> / <b>1</b> /	DIME	<u> </u>	MODE	D LITEC.		1 1 1	WILL DID	(I IVIII)					
Item:	Burn In/Final Te	st/Test Backend				_			(	Contr	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FN	Л				
Prepared By:						_					FMEA Date:		(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZI	II REN,LINGXU	AN 2	XU,S	Sinbad Liu,Peng I	06-Sep-13	(Rev.)				
								-									
													Action F				
Process	Potential Failure	Potential	S	C	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е			P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				S	of Failue									ı '	ı		
				S										i '	il		
3x inspection	Bend lead & coplanarity	-Visual mechanical failure (6) -Customer application failure(8)	8		Unit out of pocket	2	1. Strap the tray whenever moving the material 2. Operator to check tray gap before and after strapping to ensure no unit jump out the pocket				None						
			8		Mishandling the unit	2	1. Strap the tray whenever moving the material 2. Operator to check tray gap before and after strapping to ensure no unit jump out the pocket	-V/M gate (8) - 100% auto vision inspection on device (2)	2	32	None						

			' - '				112022121	D EITEU	_ ~		111211010	(= = : = = - )					
Item:	Burn In/Final Te	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	Υ				
Type:	Design	_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FM	1				
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,l	Dong	g Gao,Liang Yang	,W	ei Chen,HONGZF	HI REN,LINGXU	AN I	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)				
								•									
													Action R	Resu	ılts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	0	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	С		P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	С	T	N
				s	of Failue										l		
				S											l		
	Wrong orientation	-Customer application failure (8)	8		Unit replaced in misorientated form	2	Pin1 reverification after unit replacement	-V/M gate sampling check (8) -Vision system auto detect and alarm (2) -Auto-Pin 1 locate system by vision(1) -Pin1 bar setting for tray locate(1)	1	16	None						
	Mixed product	-Electrical failure (8) -Reliability failure (8)			Stray units at inspection table	2		-V/M gate sampling check (8) -Count quantity per shop order (6) - Vision 100% inspection (2)	2	32	None						

		/	
Item: Burn In/Final Test/Test Backend	Control Number/Issue:	83MCT00018A/	AY
Type: Design _x_ Process	Company, Group, Site/Business Unit:	Freescale,TJN-F	M
Prepared By: Liang Yang	FMEA Date:	27-Jun-01	(Orig.)
Core Team: Peg Tang, ZJ-TEST2 Hu, Peter Zha	ang,Dong Gao,Liang Yang,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng D	06-Sep-13	(Rev.)

													Action I		lts		
Process	Potential Failure	Potential	S		Potential	О		Current Design/			Recommended	Responsibility &	Actions Taken &	S		D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls				Action(s)	Target	Effective Date	Е		Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				s	of Failue												
				s													
			8		Swap Shop order	2	Process 1 lot at a	-System record the	2	32	None						
							time	marking teach									
								history in test									
								summary, operator									
								100% check									
								summary(4) -System auto check									
								and judge if									
								marking is correct									
								or not after key in									
								the actual marking									
								(2)									
								100% vision									
								inspection									
			8		Swap bundle	2	Process 1 lot at a	1. Lot no	2	32	None						
							time	verification on									
								barcode label vs									
								TSO (3)									
								2. 100% vision									
								scanning (2)									
								3. QA VM Gate									
					_			(8)							_	_	
Lead scan	Bend lead &	-Visual	8		-Bent tray	2	NA	- I	2	32	None						
		mechanical failure (6)	1					check tray (6) - 100% auto vision									
		(6) -Customer						inspection on									
		application						device (2)									
		failure(8)						de vice (2)									
		11010(0)	<u> </u>			<u> </u>			l								

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		POIL	N I	IA.	LFAILUK	L	MODE AN	DEFFEC.	19	Al	NAL Y 515 (	(FMLA)	•	uge	50 0	,, ,,	
Item:	Burn In/Final Te	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process				-		Company,	Grou	up,Si	te/Business Unit:	Freescale, TJN-FN	Л				
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZF	II REN,LINGXU	AN 2	XU,S	inbad Liu,Peng D	06-Sep-13	(Rev.)				
								-					-				
													Action I	Resu	lts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	С	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	С	Prevention	Detection	T	N				V	C	T	N
•				s	of Failue							•					
				s													
			8		- Unit misplace in	2	-Half yearly PM	-V/M gate (8)	2	32	None						
					tray caused by			- 100% auto vision									
					handler precision			inspection on									
								device (2)									
	2D matrix	-Visual	6		- Bypass 2D	2	-High level	-System real time	2	24	None						
							password control	monitor (2)									
		(6)			function												
															_		
Prepared By: Liang Yang Core Team: Peg Tang,ZJ-TEST2 Hu,Peter Zhang,Dong Gao,Liang Yang,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng E  Process Function/ Mode Pfailure Potential Failure Potential Failure V a Requirements  8																	
	Remark   Burn In/Final Test/Test Backend   Type:																
			Process														
								_									
	Unit wrong	-Customer	8		-Improper vision	1	-Regular setup		1	8	None				-	-	
	_		O						1		rone						
								-Auto-Pin 1 locate									
			l					_									
							ĺ	for tray locate(1)									

			1 T	IA	LFAILUN	Ŀ	MODE AN	DEFFEC.				,		-6-			
Item:	Burn In/Final Te	st/Test Backend				_			(	Contr	ol Number/Issue:	83MCT00018A/A	·Υ				
- 1		_x_ Process						Company,	Gro	up,Si	ite/Business Unit:	Freescale, TJN-FM					
Prepared By:						_					FMEA Date:		(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	,Donş	g Gao,Liang Yang	5,W	ei Chen,HONGZH	II REN,LINGXU	AN	XU,S	Sinbad Liu,Peng I	06-Sep-13	(Rev.)				
													Action R				
Process	Potential Failure	Potential	S		Potential	О	C				Recommended		Actions Taken &				
Function/	Mode	Effect(s) of	Е	l	Cause(s)/		Process Controls		Е		Action(s)	Target				Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
		1		S	of Failue	ĺ											
				S		L											<u> </u>
			8		-Wrong teach on	1		-V/M gate first	1	8	None						1
		1			material for pin1	ĺ	system by vision	piece check (4)									
		1			ļ	ĺ		Buddy check(7)									
		1			ļ	ĺ		-Auto-Pin 1 locate									l
		1			ļ	ĺ		system by vision(1)									
		1			ļ	ĺ		-Pin1 bar setting									
		1			ļ	ĺ		for tray locate(1)									I
		1			ļ	ĺ											
						ĺ									ŀ		l
	Mixed product	-Electrical	8		-Operator does	2	-Equipment clean	-V/M gate	2	32	None			$\dashv$	$\dashv$	П	
		failure(8)			not clear the	ĺ	after lot end	sampling check (8)									
		-Reliability failure			machine when	ĺ		-Count quantity									l
		(8)			finished lot	ĺ		per shop order (6)									
		1			ļ	ĺ		- Vision 100%									
		1			ļ	ĺ		inspection (2)									l
		1			ļ	ĺ											
			0	—		_	27.4	9 . 1.1	_	40	27			_		$\vdash$	
		1	8		-Operator teach wrong marking	3	NA	-System record the marking teach	2	48	None						
		1			wrong marking	ĺ		history in test									
						ĺ		summary, operator						ļ	ŀ		
						ĺ		100% check						ļ	ŀ		
		1				ĺ		summary(4)									

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(2)

-System auto check and judge if marking is correct or not after key in the actual marking

	-		
Item: Burn In/Final Test/Test Backend	Control Number/Issue:	83MCT00018A/	'AY
Type: Design _x_ Process	Company, Group, Site/Business Unit: 1	Freescale, TJN-F	M
Prepared By: Liang Yang	FMEA Date:	27-Jun-01	(Orig.)
Core Team: Peg Tang,ZJ-TEST2 Hu,Peter Zhang,Dong Ga	no,Liang Yang,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng Γ	06-Sep-13	(Rev.)

	-										-		Action I				
Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	S E V	C l a	Potential Cause(s)/ Mechanism(s)			Current Design/ Process Controls Detection			Action(s)	Responsibility & Target Completion Date	Effective Date	S E V	O C C	Е	P
·				s s	of Failue							·					
	Crack/chip	- Reliability failure (8) -Electrical failure (8) -Visual mechanical failure (6)	8		- Operator handles material manually in tray.	2	- Certify operators' operation skill and yearly exam to check - Treat manual operated material as VM reject and scrap.		2	32	None						
Tape & Reel	Cover tape loosen / tighten	-Device fail out or cover tape split at customer (8)	8	*	-Peel back force is out of control	1	-Follow setup checklist to set up machine	- SPC system control (4) -QA audit peel back force test record (6) -QA sealing line check (8)	4	32	None						
	2D matrix unreadable	-Visual mechanical failure (6)	6		- Bypass 2D matrix inspection function	2	-High level password control	-System real time monitor (2)	2	24	None						
			6		- Dongle is unworkable	2	NA	-Program auto alarm and stop handler when dongle is unworkable(2)	2	24	None						

			1 1	<b>11 N</b> .	Limbon		MODETH	D LITEC				· /					
	Burn In/Final Te											83MCT00018A/A					
	•	_x_ Process						Company,	Gro	up,Si		Freescale, TJN-FN					
Prepared By:											FMEA Date:		(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZF	II REN,LINGXUA	N/	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)				
													Action F	Resu	ılts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	С		Detection	Т	N		Completion Date		V	С		N
•				s	of Failue							1					
				s													
	Unit wrong	-Customer	8		-Wrong teach on	1	-Auto-Pin 1 locate	-V/M gate first	1	8	None						
	orientation in tape		Ü		material for pin1		system by vision	piece check (4)	1	O	Trone						
	reel	(8)			material for pini		by steril by vision	Buddy check(7)									
								-Auto-Pin 1 locate									
								system by									
								vision(1)									
								-Pin1 bar setting									
								for tray locate(1)									
			8		-Improper vision	1	-Regular setup	-V/M gate	1	8	None						
					setting		checklist check.	sampling check (8)									
								-Vision system									
								auto detect and									
								alarm (2)									
								-Auto-Pin 1 locate									
								system by									
								vision(1)									
								-Pin1 bar setting									
								for tray locate(1)									
	Bend lead	-Visual	8		-Machine pick up	2	- Cross beam	., 8	2	32	None						
		mechanical failure			head is not in the			sampling check (8)									
		(6)			perfect position		reel equipment.	-Handler cross									
		-Customer			along the X,Y,Z			sensor 100% check									
		application			direction			unit position and									
		failure(8)						auto alarm(2)									
								-Check per setup									
								checklist (6)									

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Item:	Burn In/Final Tes	st/Test Backend							C	Contr	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process						Company,	Grou	up,Si	te/Business Unit:	Freescale, TJN-FN	1				
Prepared By:	Liang Yang					_					FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TES	T2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	y,W	ei Chen,HONGZH	II REN,LINGXU <i>A</i>	AN 2	XU,S	inbad Liu,Peng D	06-Sep-13	(Rev.)				
								•					•				
													Action F	lesi	ılts		
Process	Potential Failure	Potential	S	C	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	0	D	R
Function/	Mode	Effect(s) of	E	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N

Itam.	Burn In/Final Te		1 4	<b>A</b> / <b>A</b> /	Dimile		NODE	D LITEC				83MCT00018A/A	v					_
		_x_ Process				-		Company				Freescale, TJN-FM						-
Prepared By:		_x_110cess						Company,	JIU	up,si	FMEA Date:		(Orig.)					-
		ST2 Hu Peter 7hs	anσ	Dong	Gao Liang Vand	. W	ei Chen HONGZE	II REN,LINGXUA	M.	XII S			(Rev.)					
core ream.	1 cg 1 ang,23-12	512 Hu,i etci Zili	mg,	Dong	g Gao, Liang Tang	5, **	er enen,morvoza	II KEN,EINGKO	111	20,0	mioad Liu,i chg L	00-5ср-13	(Rev.)					
													Action I	Resu	ılts			-
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &				D	R	-
Function/	Mode	Effect(s) of	E	1	Cause(s)/			Process Controls			Action(s)	Target	Effective Date	Ē	C	E		
Requirements		Failure	V	a	Mechanism(s)	C		Detection	T	N	(*)	Completion Date		V	C	T	N	
1				s	of Failue				_	- '				·				
				s														
	Cover tape	-Customer	8	_	-Technician adjust	2.	NA	-Technician first	4	64	None							-
		application failure			the guider width	Ī		piece check under	ľ									
	carrier tape	(8)			or carrier tape			10X microscope										
	•				location pins			after technician										
					improperly.			adjust the guider										
								width or carrier										
								tape location pins.										
								(4)										
	Mixed product	-Electrical	8		-Operator does	2	-Equipment clean	., 8	2	32	None							
		failure(8)			not clear the		after lot end	sampling check (8)										
		-Reliability failure			machine when			-Count quantity										
		(8)			finished lot			per shop order (6)										
								- Vision 100%										
								inspection (2)										
			0		0 1 1	2	NT A	0 1 11	_	40	NT.							_
			8		-Operator teach wrong marking	3	NA	-System record the marking teach	2	48	None							
					wrong marking			history in test										
								summary, operator										
								100% check										
								summary(4)										
								-System auto check										
								and judge if										
			I					marking is correct										
								or not after key in										
			I					the actual marking										
			I					(2)										
			l															

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	Mode Effect(s) of Failure V a Mechanism(s) of Failure S and I tube																
Item:	Burn In/Final Te	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FM	1				
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZH	II REN,LINGXUA	AN :	XU,S	Sinbad Liu,Peng D	06-Sep-13	(Rev.)				
								•					•				
													Action R	Resu	lts		
Process	Potential Failure	Potential	S	С	Potential	О	Current Design/	Current Design/	D	R	Recommended	Responsibility &	Actions Taken &	S	О	D	R
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	С	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	С	Prevention	Detection	Т	N				V	C		N
•				s								•					
				s													
ГТТ	Lead defect in	-Visual	8		-Tube and	1	-Re-design the	-V/M Gate	4	32	None						
	tube	mechanical failure			tracking												
		(6)															
		-Customer						(4)									
		failure(8)															
	Mixed product		8		•	2	-Equipment clean		2	32	None						
							after lot end										
		(8)			finished lot												
								inspection (2)									
			Q		Operator teach	3	NΑ	System record the	2	18	None					H	
			o		wrong marking	3	NA.	marking teach	_	40	None						
					wrong marking			history in test									
								summary, operator									
								100% check									
								summary(4)									
								-System auto check									
								and judge if									
								marking is correct									
								or not after key in									
								the actual marking									
								(2)									
		ĺ			ĺ		l				1						

Item:	Burn In/Final Te	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	Y				
Type:	Design	_x_ Process						Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FN	1				
Prepared By:	Liang Yang					_					FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	Dong	g Gao,Liang Yang	g,W	ei Chen,HONGZF	II REN,LINGXU	AN :	XU,S	Sinbad Liu,Peng I	06-Sep-13	(Rev.)				
					_		_				_		Action R				
	Potential Failure		S		Potential		Current Design/						Actions Taken &			D	
Function/	Mode	Effect(s) of	Е	1	Cause(s)/		Process Controls			P	Action(s)	Target	Effective Date	Е	C	Е	P
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				S	of Failue												
				S													
	Unit wrong	-Customer	8		-Wrong teach on	1	-Auto-Pin 1 locate	-V/M gate first	1	8	None						
	orientation in tube	application failure (8)			material for pin1		system by vision	piece check (4)Buddy check(7)									
		(0)						-Auto-Pin 1 locate									
								system by									
								vision(1)									
			8		-Improper vision	1	-Regular setup	-V/M gate	1	8	None						
					setting		checklist check.	sampling check (8)									
								-Vision system									
								auto detect and alarm (2)									
								-Auto-Pin 1 locate									
								system by									
								vision(1)									
DRY PACK	Bag leakage	-Reliability failure	8		-Break MBB	1	N/A		6	48	None						
		(8)						packing quality for									
								every box (6)									
			0		D 1 1		NT/A	O A 1000/ 1 1	_	40	NT.						
			8		-Poor dry pack bag quality	1	N/A	-QA 100% check packing quality for	6	48	None						
					dag quanty			every box (6)									
								2 : 2 - 3   0 0 11 (0)									
	No-dry pack	-Reliability failure	8		-Miss dry pack	1	N/A	-QA 100% check	6	48	None					1	

(8)

process

packing quality for

every box(6)

Item:	Burn In/Final Te	st/Test Backend							(	Contr	ol Number/Issue:	83MCT00018A/A	ΛY				
Type:	Design	_x_ Process				)		Company,	Gro	up,Si	te/Business Unit:	Freescale, TJN-FN	Л				
Prepared By:	Liang Yang										FMEA Date:	27-Jun-01	(Orig.)				
Core Team:	Peg Tang,ZJ-TE	ST2 Hu,Peter Zha	ang,	Don	g Gao,Liang Yang	,W	ei Chen,HONGZF	II REN,LINGXU	AN I	XU,S	Sinbad Liu,Peng I	06-Sep-13	(Rev.)				
					•		_					T	Action I	_	_		
Process	Potential Failure	Potential	S	C	Potential	О		_			Recommended	Responsibility &					
Function/	Mode	Effect(s) of	Е	1	Cause(s)/	C	Process Controls	Process Controls	Е	P	Action(s)	Target	Effective Date	Е			
Requirements		Failure	V	a	Mechanism(s)	C	Prevention	Detection	T	N		Completion Date		V	C	T	N
				s	of Failue												
				s													
	Mixed product	-Electrical	8		-Operator handles	2	-One time one lot	-Automated	2	32	None						
		failure(8)			more than one lot			verification									
		-Reliability failure			at same time.			barcode of box,									
		(8)						dry bag by auto-									
								verify machine (2)									
								-QA check (8)									
	Duration time out	- Delamination	8		-The lot duration	2	N/A	- System auto	2	32	None					$\rightarrow$	
		issue (8)	Ü		time was out of	1	1 1/2 1	detect duration	ľ	22	110110						
		- Solderability			control			time before dry									
		issue (8)						packing (2)									

## **Control Plan**

## **TSMC PPAP Documents**

- TSMC PPAP documents (FMEAs, Control Plans, Cpks, and GR&R) are considered proprietary information by TSMC, classified as "TSMC INTERNAL USE ONLY" and cannot be distributed with Freescale PPAPs in accordance with an agreement with TSMC.
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- For special requests, Freescale may be able to review these documents on a limited basis with customers at the local Freescale sales office.
- If there are any questions, please contact:

Sally Cadena Massey, Freescale MSG NPI Reliability, 512-895-7310 sally.cadena.massey@freescale.com

Jeff Martsching, Freescale External Manufacturing, 512-996-4282 Jeff.Martsching@freescale.com



#### **Assembly Process Control Plan-SOIC**

	Plan Number/Iss	sue		Prototype Pre-launch (XC)	Key Contact/Phone				Date(Orig.)			Date (Rev.)
	00015A002/O		L	Production		Amanda Wang	g/6368		30-Nov-13			30-Nov-13
Part Nur	nber			Core Team			aohui, Yao Shuan, Chen Grayson, Wang , Derk Song, Ma Qianfeng	Jinsheng, Tao Xin,	Customer Engineering	g Approval (If Heq'd)		
		6/28/32 /54 LD Assembly	Cu wire	Supplier/Plant	FSL-TJN-FM		Supplier Code		Customer Quality App	proval/Date (If Req'd)		
FLOW	CHART LEG	GEND	PROD=Production (	Operation INSP=Ins	pection MEAS=Me	easurement	QA=QA Monitor GATE=QA	Gate XFER=M	laterial Transfer MAT=Material Ins	pection		
					cteristics				Sample	p		
Chart	Process/ Operation	Process Name/	Machine, Device, Jig, Tools for			Special Char.	Product/Process Specification/	Evaluation Measurement				
Symbol		Operation Description	Mfg.	Product	Process	Class	Tolerance	Technique	Size	Freq.	Control Method	Reaction Plan
PROD	3.2	pre-wire bond plasma clean	plasma machine		parameter		12MCT20031B007	visual	NA .	1. 1x/machine/shift     2. 1x/after machine repair	12MCT20070A 12MCT10020A 12MCT20120A004 12MCT20110A001 12MCT20031B007	12MCT20070A 12MCT20031B003
MEAS		pre-wire bond plasma clean monitor	goniometer	contact angle			<10deg for die surface	measurement	2 points/strip, 3 strips/x	1x/machine/shift		
							<50deg for leadframe surface	measurement	1point/strip, 3 strips/x	1x/machine/shift		
PROD	4	Cu wire bond 1 / To bond wires from pad to post	wire bonder		parameter		12MCT20031S020	visual	NA	1.1x/device change; 2.1x/parameter change; 3.1x/after machine repair.	12MCT20070A 12MCT10020A 12MCT20070A006 12MCT20070A006 12MCT200315020 12MCT10110A001	12MCT20070A 12MCT20031K004
			Cu wire		Cu wire work life		144hrs	auto control system	N/A	100% material system auto control		
			capillary	•	capillary life		12MCT20031S020	visual	N/A	machine auto control	•	
INSP		wire bond monitor 1	microscope (>=30x)	visual & mechanical defects			12M54564J	visual	3 pitches/strip; 2 strips/magazine	1x/magazine	12MCT20070A 12MCT10020A 12MCT10110A001	12MCT20070A 12MCT20031K004
MEAS		wire pull monitor 1	wire pull tester	wire pull strength		*	12MCT20070A	measurement	6 wires/x	1. 1x/machine/shift;     2. 1x/device change;     3. 1x/parameter change;     4. 1x/capillary change.	12MCT20070A 12MCT10020A 12MCT10030A 12MCT20080C	12MCT20070A 12MCT20031K004
		ball shear monitor 1	ball shear tester	ball shear strength		*	12MCT20070A	measurement	6 wires/x	1. 1x/machine/shift;     2. 1x/device change;     3. 1x/parameter change;     4. 1x/capillary change.	12MCT20070A 12MCT10020A 12MCT10030A 12MCT20080C	12MCT20070A 12MCT20031K004
		ball size monitor	microscope(>=200x)	ball size			12MCT20070A	measurement	4 balls/x	1. 1x/device change;     1x/parameter change;     1x/capillary change.	12MCT20070A 12MCT10020A 12MCT20070A006 12MCT10110A001	12MCT20070A 12MCT20031K004
		ball height monitor	microscope(>=200x)	ball height			12MCT20070A	measurement	4 balls/x	1. 1x/device change;     1x/parameter change;     1x/capillary change.	12MCT20070A 12MCT10020A 12MCT20070A006 12MCT10110A001	12MCT20070A 12MCT20031K004

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Control Plai	n Number/Iss	sue		Prototype Pre-launch (XC)	Key Contact/Phone				Date(Orig.)	Date (Rev.)		
70MCT000			X	Production	Tang Peg (85686866)/h	Hu Z.J(85686	770)		5/10/1997	11/25/2013		
Part Numbe	r			Core Team				Customer Engineerin	ng Approval (If Req'd)			
GENERAL	TEST			Duan Peng, Chen Wei, Yin Wally, Xu Lingxuar	Diao William, Liu X.J., 0 1.	Sao Dong, Y	ang Liang, Wang K.Q.,					
Name/Desc	ription			Supplier/Plant		Supplier Co	de	Customer Quality App	proval/Date (If Req'd)			
GENERAL	TEST FLOV	V		FSL-TJN-FM								
			<b>PROD</b> =Pr	oduction Operation INSF	P=Inspection MEAS=Me		OWCHART LEGEND  OA=OA Monitor GAT	E=QA Gate XFER=N	Material Transfer MAT=	Material Inspection		
Flow Chart	Process		Machine Device, Jip, Tools		teristics	Special	Product/Process	Evaluation		ample	Control	
Symbol	Operation Number	Process Name/Operation	for Mfg	Product	Process	Char. Class	/Specification /Tolerance	Measurement Technique	Size	Freq.	Method	Reaction Plan
MAT	1	MATERIAL RECEIVING	Assembly Shop Order Packing list, SFC System		Documentation		12MCT50044C	Visual	100%	Every lot	Verify box label LOT#, device #, box quantity against packing list & SFC	Hold lot for disposition 12MCT50040A
PROD		INCOMING CHECK	Assembly Shop Order Test Shop Order		Quantity		12MCT50044C	Visual	100%	Every lot	Count physical quantity againest assembly shop order	Hald les for discoursion
11102	2	(Visual Mechanical only applies to assembly & BI rawstock)	SFC System		Documentation		12.001300440	Visual	100%	Every lot	Verify box label LOT#, device #, lot status in SFC system	Hold lot for disposition 12MCT50040A 12MCT50040A020 12MCT50040A021
INSP			vision machine (optional)		Visual Mechanical		12MRM09116A	Visual or vision machine (optional)	Per 12ACT20080A	Every lot	Visual verification for visual defect	-
PROD			Test Shop Order		Machine Type		12MCT50040A	Visual	100%	Every conversion	Manual visual verification machine according to test shop order	Hold for disposition 12MCT50040A
PROD			Test Shop Order		Temperature		Test Shop Order	Continuous Test Temperature monitoring	100%	Every test insertion	Handler temperature auto- guardbanding using temperature controller	Handler stop until temperature is within guardband
PROD			Test Shop Order SFC system		Yield (Start lot)		12MCT50040A 12MCT10240A	Electrical Test	Per 12ACT20080A	Every lot	Calculate the yield after sampling test done and compare with shut down yield	Stop the machine and call PE/TPE/PM. 12MCT50040A 12MCT5040A 12MCT5040A010 12MCT50040A010 12MCT50040A015 12MCT50040A015
INSP		ELECTRICAL TEST as per test shop order	vision machine (optional)		Visual Mechanical (Start lot)		12MRM09116A	Visual or vision machine (optional)	Per 12ACT20080A	Every lot	Visual verification for visual defect	Stop the machine and call supervisor. 12MCT50040A 12MCT50040A01 12MCT50040A010 12MCT50040A012 12MCT50040A015
PROD	3	Machine preparation     Start lot     Start lot     Electrical parameters tests     Hend lot     (Hot/Cold/Room)	ATE	Electrical Parameter			12MCT50040A	Electrical Test Program	100%	Every lot	Electrical Yield limit per SFC System	Stop the machine and call PE/TPE/PM. 12/MCT50040A 12/MCT50040A014 12/MCT50040A010 12/MCT50040A012 12/MCT50040A012 12/MCT50040A015 12/MCT50040A018
INSP			Vision machine (optional)		Visual Mechanical (In process)		12MRM09116A	Visual or vision machine (optional)	Per 12ACT20080A	Every lot	Visual verification for visual defect	Stop the machine and call supervisor. 12MCT50040A 12MCT50040A004 12MCT50040A010 12MCT50040A012 12MCT50040A015
					Yield (End lot)		12MCT50040A 12MCT10240A	Electrical Test	100%	Every lot	Electrical Yield limit per SFC System	Hold lot for disposition 12MCT10240A

Control Pla	n Number/Iss	sue		Prototype	Key Contact/Phone				Date(Orig.)	Date (Rev.)		
				Pre-launch (XC)	.,				(= 3)	( - ,		
70MCT000			X	Production	Tang Peg (85686866)/h	łu Z.J(85686	770)		5/10/1997	11/25/2013		
Part Number	r			Core Team				Customer Engineerin	g Approval (If Req'd)			
GENERAL	TEST			Duan Peng, Chen Wei, Yin Wally, Xu Lingxuan		ao Dong, Ya	ang Liang, Wang K.Q.,					
Name/Desc				Supplier/Plant		Supplier Cod	le	Customer Quality App	oroval/Date (If Req'd)			
GENERAL	TEST FLOV	ı		FSL-TJN-FM								
							WCHART LEGEND					
	Process		<b>PROD</b> =Pr	oduction Operation INSP		asurement (	Product/Process	E=QA Gate XFER=N Evaluation	Material Transfer MAT=		1	
Flow Chart	Operation	Process Name/Operation	Machine Device, Jip, Tools	Charac	eristics	Special	/Specification	Measurement	S	ample	Control	Reaction Plan
Symbol	Number		for Mfg	Product	Process	Char. Class	/Tolerance	Technique	Size	Freq.	Method	
PROD			Test Shop Order SFC system		Quantity		12MCT50040P	Visual	100%	Every lot	Count physical quantity and record on test shop order & SFC	Hold lot for disposition 12MCT50040A 12MCT50040A005 12MCT50040A019
					Documentation		121001300401	Visual	100%	Every lot	Check test result againest physical quantity, confirm the lot status in SFC system	Hold lot for disposition 12MCT50040A
		ELECTRICAL TEST (QC In- line) as per shop order (Hot/Room/Cold): Applicable for specific products as specified in the Test Shop Order or SFC system		Electrical Parameter			12MCT50040A 12ACT20080A	Electrical Test Program	Per 12ACT20080A	Per Skip Plan	Accept on zero failure	Hold lot for disposition 12ACT20080A 12MCT50040A 12MCT50040A010 12MCT50040A012 12MCT50040A013 12MCT50040A015
GATE	4		ATE Test Shop Order SFC system		Quantity			Visual	100%	Every lot	Count physical quantity and record on test shop order & SFC	Hold lot for disposition 12MCT50040A 12MCT50040A005 12MCT50040A019
					Documentation		12MCT50040P	Visual	100%	Every lot	Check test result againest physical quantity, tranfer the lot to next step in SFC system	Hold lot for disposition 12MCT50040A
PROD		QUALITY CONTROL			Quantity		12MCT10123G	Visual	100%	Every lot	Count physical quantity againset test shop order	Hold lot for disposition 12MCT50040A 12MCT50040A005 12MCT50040A019
FHOD	5	Stage: 1. Verification for test result 2. Visual inspection on final good unit			Documentation		Destritorist	Visual	100%	Every lot	Check test result againest test shop order, verify lot status in SFC system	Hold lot for disposition 12MCT50040A
INSP			Microscope(optional)		Visual Mechanical		12MRM09116A	Visual or Microscope(optional )	Per 12ACT20080A	Every lot	Visual verification for visual defect	Hold lot for disposition 12MCT50040A 12MCT50040A004

NOTE 1. ATE:Auto Testing Equipment

Visual: Unaided eye or 3x magnifier (optional)

Part Number:	GENERAL TEST	Control Plan Number/Issue:	70MCT00019A/AW	_
Name/Description:	GENERAL TEST FLOW	Control plan Date:	5/10/1997	(Orig.)
Supplier/Plant:	FSL-TJN-FM	Control plan Date.	11/25/2013	(Rev.)

<b>Revision Date</b>	Description of Revison & Writer	Spec Coord	Effectivity Date
0	VERSION O	J.W ZHANG	5/10/1997
A	CHANGE ERROR WORD	J.H ZHANG	12/14/1997
В	CHANGE CORE TEAM MEMBER	J.H ZHANG	3/3/1998
С	CHANG FORMAT	J.H ZHANG	5/10/1998
D	CHANG DOCUMENT TITLE	J.H ZHANG	6/6/1998
Е	spelling mistake	J.H ZHANG	10/10/1998
F	Modify "Key contact/phone and Core team"	J.H ZHANG	12/20/1998
G	Change Format	J.H ZHANG	5/15/1999
Н	Change format, change flow chart symbol to term per 12MRM96619A request	M.H LI	9/1/1999
J	Change sample size and QA gate method	Robert Wang	9/19/1999
K	Change Format	Robert Wang	4/10/2000
L	Change 24ape1n	Allan Li	6/9/2000
M	Change MCEL to BAT3	Lucy Bai	2/26/2001
N	change "per spec" to specific SPEC name chang QA gate to GATE	J.W Zhang	7/26/2001
P	Modify "Key contact/phone and Core team", Then change CA to ZH	J.W Zhang	11/30/2001
R	change file name to " SOIC and PDIP Test Flow " Modify "Key contact/phone and Core team"	H.L Sun	9/20/2002
S	Change test account from zh630 to ZH630/ZH660, adding packing in QA step, delete zh850	YuPeng Zhang/linda bo	5/22/2003
T	Adding "packing" in FOI gate	YuPeng Zhang/linda bo	6/6/2003
U	Changed the Part number, changed flow from INSP. To MAT, and QA to Gate, Deleted all 48A from control method	YuPeng Zhang/Wang Peng/Berts Li	4/5/2004
V	Modify the format;replace PROD with XFER in ZH650.adding "visual" in incoming check	Zhang Yupeng /Wang Peng	4/26/2004
W	Change sample size to 200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k) from 200 Units/Lot(Lot size<10k) or 315 Units(lot size>10k)	Zhang Yupeng /Wang Peng	5/13/2004
X	Change Core Team member from David zhang to Yang Liang	Yang Liang	9/13/2004

Y	Change Process Description from TTT or Tape&Reel to Test Backend	Yang Liang	4/14/2005
Z	Change 'TTT or Tape&Reel' to 'Test Backend'	Yang Liang	4/19/2005
AA	Change Process No from ZH670 to ZH670/ZH720	Yang Liang	5/16/2005
AB	Added "V/M Sample Check" process in electrical test.	Wang Peng	9/9/2005
AC	Updated "Core Team Member".	Wang Peng	10/25/2006
	1. Updated "Core Team Member" and revised some characteristics from process		
AD	column to product column;		
AD	2. change 'VM sample check' to 'Machine Setup VM check' to clarify the VM check		
	purpose on Electrical test process.	Wang Peng/Yang Liang	9/28/2007
	Change sample size to 200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k)		
AE	from 200 Units/Lot(Lot size<10k) or 315 Units(lot size>10k)	Zhang Yupeng/ Wang Peng	5/13/2004
	1. Add '12MCT50040A' in control method and Reaction Plan column of INSP.		
	step		
	2. Change Core Team name from		
AF	'Zhang Yupeng' to 'Yang Liang'	Yang Liang	9/21/2004
	1.Add "PQFN" in "Title,Part Number & Name/Description"		
	2.Add"Albert Zheng(6192)" in" Key Contact/Phone".		
	3.Change "SPS" to "Freescale"		
	4.Add "Yield" in "char.process of Electrical Test"		
	5.Delete "Electrical Test" in "char. Product" column.		
	6.Take place "200 units/Lot" with "200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k)"		
	7.Add "Electrical Parameter" in" char. Process" column		
AG	8.Add note of "F/T" and "ATE"	Wang Peng	11/30/2004
AH	Added "V/M Sample Check" process in electrical test.	Wang Peng	11/23/2005
AJ	Updated "Core Team Member" and "Supplier/Plant Name"	Wang Peng/Yang Liang	11/10/2006
713	opaned Core ream Member and Supplient fant (value	wang reng, rang Liang	11/10/2000
	Updated "Core Team Member" and revised some characteristics from process		
	column to product column; change 'VM sample check' to		
	'Machine Setup VM check' to clarify the VM check purpose on Electrical test		
AK	process.	Wang Peng/Yang Liang	9/28/2007
AL	Delete the process description of B/I, Lot process & T/R from test process.	Wang Peng	4/15/2008
	1. Core Team Review		
	2. Update "Core Team Member"		
	3. Change title from "ZH630/ZH660 Test Flow" to "GENERAL TEST FLOW"		

1	1	1	1
	4. Change part number from "ZH630/ZH660 Test Bank" to "GENERAL TEST" 5. Change description from "ZH630/ZH660 Test Bank Test Flow" to "GENERAL TEST FLOW"		
	6. Change incoming check sample size from "200 Units/Lot (Lot Size <10K);315 Units/Lot (Size>=10K)" to "200 Units/Lot (Lot Size =<10K);315 Units/Lot (Size>10K)"		
	7. Change start lot check sample size from "200 Units/Lot (Lot Size <10K);315 Units/Lot (Size>=10K)" to "200 Units/Lot (Lot Size =<10K);315 Units/Lot (Size>10K)"		
	8. Change machine setup & V/M check sample size from "200 Units/Lot (Lot Size <10K);315 Units/Lot (Size>=10K)" to "200 Units/Lot (Lot Size =<10K);315 Units/Lot (Size>10K)"		
	9. Change ILG sample size from "Per Skip Plan" to "Per 12ACT20080A" 10. Change VM gate sample size from "200 Units/Lot (Lot Size <10K);315 Units/Lot (Size>=10K)" to "200 Units/Lot (Lot Size =<10K);315 Units/Lot		
AM	(Size>10K)"	Chen Wei/Yang Liang	5/5/2009
AN	12months review	Yang Liang/Chen Wei	5/4/2010
AP	12months review,no content change.	Yang Liang/Chen Wei	4/18/2011
	1. Add "ZHPT0" to process operation number		
	2. Change the reference of sample size to "Per 12ACT20080A"		
	3. Update the document numbers of "Specification", "Control Method" and "Control		
	plan" acoording to Doc_Rebuild project		
	4. Change step name from "VM Gate (Per shop order)" to "VM Inspection", change the step symbol from "GATE" to "INSP"		
	5. For "VM Insepction" step, change the "Machine, Tools" and "Evaluation		
	Measurement Technique" to "Visual"		
AR	6. Add NOTE 3	Yang Liang/Chen Wei	10/17/2011
		0 0	
	1. Remove Han Z.L from core team member;		
	2. Replace "A" with "Visual Mechanical Defect";		
	3. Replace process specification of electrical test/gate process from "48A Spec" to		
	"Test Program" / "Gate Program"		
	4. Replace "Test Program" & "Gate Program" Measurement to "Electrical Test";		1.0.10.10.11
AS	5. Replace gate process tool from "ILG" to "ATE"	Chen Wei/Yang Liang	12/9/2011

AT	Update core team member     Split out "CENTRAL MATERIAL STAGING" step from "INCOMING CHECK" step, add detailed items into "INCOMING CHECK" step     Add detailed control method and reaction plan     Change freq. from "1x/lot" to "Every lot"	Chen Wei	9/21/2012
AU	Core team review: 1. Change the process name from "CENTRAL MATERIAL STAGING" to "MATERIAL RECEIVING" 2. Move "machine preparation" from "INCOMING CHECK" to "ELECTRICAL TEST" 3. Update the wording of Characteristics	Chen Wei/Yang Liang	11/9/2012
AV	Update Core team member     Update reaction plan  2013 annual control plan review, no content change.	Chen Wei/Yang Liang Chen Wei/Yang Liang	9/6/2013

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Control Plai	n Number/Iss	sue		Prototype Pre-launch (XC)	Key Contact/Phone				Date(Orig.)	Date (Rev.)		
70MCT000			X	Production	Tang Peg (85686866)/I	łu Z.J(85686	770)		5/10/1997	11/25/2013		
Part Numbe	r			Core Team				Customer Engineerin	g Approval (If Req'd)			
GENERAL	TEST			Duan Peng, Chen Wei, Yin Wally, Xu Lingxuan	Diao William, Liu X.J., 0 ı.	iao Dong, Y	ang Liang, Wang K.Q.,					
Name/Desc	ription			Supplier/Plant		Supplier Co	de	Customer Quality App	proval/Date (If Req'd)			
GENERAL	TEST FLOV	V		FSL-TJN-FM								
			<b>PROD</b> =Pr	oduction Operation INSF	P=Inspection MEAS=Me		OWCHART LEGEND  OA=OA Monitor GAT	E=QA Gate XFER=N	Material Transfer MAT=	Material Inspection		
Flow Chart	Process		Machine Device, Jip, Tools		teristics	Special	Product/Process	Evaluation		ample	Control	
Symbol	Operation Number	Process Name/Operation	for Mfg	Product	Process	Char. Class	/Specification /Tolerance	Measurement Technique	Size	Freq.	Method	Reaction Plan
МАТ	1	MATERIAL RECEIVING	Assembly Shop Order Packing list, SFC System		Documentation		12MCT50044C	Visual	100%	Every lot	Verify box label LOT#, device #, box quantity against packing list & SFC	Hold lot for disposition 12MCT50040A
PROD		INCOMING CHECK	Assembly Shop Order Test Shop Order		Quantity		12MCT50044C	Visual	100%	Every lot	Count physical quantity againest assembly shop order	I lad las fau diagonision
11105	2	(Visual Mechanical only applies to assembly & BI rawstock)	sual Mechanical only slies to assembly & BI		Documentation		121401300440	Visual	100%	Every lot	Verify box label LOT#, device #, lot status in SFC system	Hold lot for disposition 12MCT50040A 12MCT50040A020 12MCT50040A021
INSP			vision machine (optional)		Visual Mechanical		12MRM09116A	Visual or vision machine (optional)	Per 12ACT20080A	Every lot	Visual verification for visual defect	-
PROD			Test Shop Order		Machine Type		12MCT50040A	Visual	100%	Every conversion	Manual visual verification machine according to test shop order	Hold for disposition 12MCT50040A
PROD			Test Shop Order		Temperature		Test Shop Order	Continuous Test Temperature monitoring	100%	Every test insertion	Handler temperature auto- guardbanding using temperature controller	Handler stop until temperature is within guardband
PROD			Test Shop Order SFC system		Yield (Start lot)		12MCT50040A 12MCT10240A	Electrical Test	Per 12ACT20080A	Every lot	Calculate the yield after sampling test done and compare with shut down yield	Stop the machine and call PE/TPE/PM. 12MCT50040A 12MCT50240A 12MCT5040A010 12MCT50040A010 12MCT50040A015 12MCT50040A015
INSP		ELECTRICAL TEST as per test shop order	vision machine (optional)		Visual Mechanical (Start lot)		12MRM09116A	Visual or vision machine (optional)	Per 12ACT20080A	Every lot	Visual verification for visual defect	Stop the machine and call supervisor. 12MCT50040A 12MCT50040A01 12MCT50040A010 12MCT50040A012 12MCT50040A015
PROD	3	Machine preparation     Start lot     Start lot     Electrical parameters tests     Hend lot     (Hot/Cold/Room)	ATE	Electrical Parameter			12MCT50040A	Electrical Test Program	100%	Every lot	Electrical Yield limit per SFC System	Stop the machine and call PE/TPE/PM. 12/MCT50040A 12/MCT50040A014 12/MCT50040A010 12/MCT50040A012 12/MCT50040A012 12/MCT50040A015 12/MCT50040A018
INSP			Vision machine (optional)		Visual Mechanical (In process)		12MRM09116A	Visual or vision machine (optional)	Per 12ACT20080A	Every lot	Visual verification for visual defect	Stop the machine and call supervisor. 12MCT50040A 12MCT50040A01 12MCT50040A010 12MCT50040A012 12MCT50040A015
					Yield (End lot)		12MCT50040A 12MCT10240A	Electrical Test	100%	Every lot	Electrical Yield limit per SFC System	Hold lot for disposition 12MCT10240A

Control Pla	n Number/Iss	sue		Prototype	Key Contact/Phone				Date(Orig.)	Date (Rev.)		
				Pre-launch (XC)								
Part Number			Х	Production Core Team	Tang Peg (85686866)/I	Hu Z.J(85686	770)	Customer Engineerin	5/10/1997 ng Approval (If Reg'd)	11/25/2013		
T dit Hambe				Duan Peng, Chen Wei,	Diao William. Liu X.J 0	Sao Dong. Y	ang Liang, Wang K.Q.,	Captomor Engineerii	ig / pp.ora. (ii rioqa)			
GENERAL				Yin Wally, Xu Lingxuan								
Name/Desc	ription			Supplier/Plant		Supplier Cod	de	Customer Quality Ap	proval/Date (If Req'd)			
GENERAL	TEST FLOV	V		FSL-TJN-FM				<u> </u>				
			PROD=Pr	roduction Operation INSF	P=Inspection MFAS=Me		WCHART LEGEND  OA=OA Monitor GAT	F=OA Gate XFFR=I	Material Transfer MAT=	Material Inspection		
Flow Chart	Process		Machine Device, Jip, Tools		teristics	Special	Product/Process	Evaluation		Sample	Control	
Symbol	Operation Number	Process Name/Operation	for Mfg	Product	Process	Char. Class	/Specification /Tolerance	Measurement Technique	Size	Freq.	Method	Reaction Plan
PROD			Test Shop Order SFC system		Quantity		12MCT50040P	Visual	100%	Every lot	Count physical quantity and record on test shop order & SFC	Hold lot for disposition 12MCT50040A 12MCT50040A005 12MCT50040A019
					Documentation		121001300401	Visual	100%	Every lot	Check test result againest physical quantity, confirm the lot status in SFC system	Hold lot for disposition 12MCT50040A
		ELECTRICAL TEST (QC In- line) as per shop order (Hot/Room/Cold): Applicable for specific products as specified in the Test Shop Order or SFC system		Electrical Parameter			12MCT50040A 12ACT20080A	Electrical Test Program	Per 12ACT20080A	Per Skip Plan	Accept on zero failure	Hold lot for disposition 12ACT20080A 12MCT50040A 12MCT50040A010 12MCT50040A012 12MCT50040A013 12MCT50040A015
GATE	4		ATE Test Shop Order SFC system		Quantity			Visual	100%	Every lot	Count physical quantity and record on test shop order & SFC	Hold lot for disposition 12MCT50040A 12MCT50040A005 12MCT50040A019
					Documentation		12MCT50040P	Visual	100%	Every lot	Check test result againest physical quantity, tranfer the lot to next step in SFC system	Hold lot for disposition 12MCT50040A
PROD		QUALITY CONTROL			Quantity		12MCT10123G	Visual	100%	Every lot	Count physical quantity againset test shop order	Hold lot for disposition 12MCT50040A 12MCT50040A005 12MCT50040A019
11105	5	Stage: 1. Verification for test result 2. Visual inspection on final good unit			Documentation		.E.WOTTOTESC	Visual	100%	Every lot	Check test result againest test shop order, verify lot status in SFC system	Hold lot for disposition 12MCT50040A
INSP			Microscope(optional)		Visual Mechanical		12MRM09116A	Visual or Microscope(optional )	Per 12ACT20080A	Every lot	Visual verification for visual defect	Hold lot for disposition 12MCT50040A 12MCT50040A004

NOTE 1. ATE:Auto Testing Equipment

2. Visual: Unaided eye or 3x magnifier (optional)

Part Number:	GENERAL TEST	Control Plan Number/Issue:	70MCT00019A/AW	_
Name/Description:	GENERAL TEST FLOW	Control plan Date:	5/10/1997	(Orig.)
Supplier/Plant:	FSL-TJN-FM	Control plan Date.	11/25/2013	(Rev.)

<b>Revision Date</b>	Description of Revison & Writer	Spec Coord	Effectivity Date
О	VERSION O	J.W ZHANG	5/10/1997
A	CHANGE ERROR WORD	J.H ZHANG	12/14/1997
В	CHANGE CORE TEAM MEMBER	J.H ZHANG	3/3/1998
С	CHANG FORMAT	J.H ZHANG	5/10/1998
D	CHANG DOCUMENT TITLE	J.H ZHANG	6/6/1998
Е	spelling mistake	J.H ZHANG	10/10/1998
F	Modify "Key contact/phone and Core team"	J.H ZHANG	12/20/1998
G	Change Format	J.H ZHANG	5/15/1999
Н	Change format, change flow chart symbol to term per 12MRM96619A request	M.H LI	9/1/1999
J	Change sample size and QA gate method	Robert Wang	9/19/1999
K	Change Format	Robert Wang	4/10/2000
L	Change 24ape1n	Allan Li	6/9/2000
M	Change MCEL to BAT3	Lucy Bai	2/26/2001
N	change "per spec" to specific SPEC name chang QA gate to GATE	J.W Zhang	7/26/2001
P	Modify "Key contact/phone and Core team", Then change CA to ZH	J.W Zhang	11/30/2001
R	change file name to " SOIC and PDIP Test Flow " Modify "Key contact/phone and Core team"	H.L Sun	9/20/2002
S	Change test account from zh630 to ZH630/ZH660, adding packing in QA step, delete zh850	YuPeng Zhang/linda bo	5/22/2003
T	Adding "packing" in FOI gate	YuPeng Zhang/linda bo	6/6/2003
U	Changed the Part number, changed flow from INSP. To MAT, and QA to Gate, Deleted all 48A from control method	YuPeng Zhang/Wang Peng/Berts Li	4/5/2004
V	Modify the format;replace PROD with XFER in ZH650.adding "visual" in incoming check	Zhang Yupeng /Wang Peng	4/26/2004
W	Change sample size to 200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k) from 200 Units/Lot(Lot size<10k) or 315 Units(lot size>10k)	Zhang Yupeng /Wang Peng	5/13/2004
X	Change Core Team member from David zhang to Yang Liang	Yang Liang	9/13/2004

Change Process Description from TTT or Tape&Reel to Test Backend	Yang Liang	4/14/2005
Change 'TTT or Tape&Reel' to 'Test Backend'	Yang Liang	4/19/2005
Change Process No from ZH670 to ZH670/ZH720	Yang Liang	5/16/2005
Added "V/M Sample Check" process in electrical test.	Wang Peng	9/9/2005
Updated "Core Team Member" .	Wang Peng	10/25/2006
1. Updated "Core Team Member" and revised some characteristics from process		
column to product column;		
	Wang Peng/Yang Liang	9/28/2007
	Zhang Yupeng/ Wang Peng	5/13/2004
1. Add '12MCT50040A' in control method and Reaction Plan column of INSP.		
step		
	Yang Liang	9/21/2004
4.Add "Yield" in "char.process of Electrical Test"		
5.Delete "Electrical Test" in "char. Product" column.		
6.Take place "200 units/Lot" with "200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k)"		
7.Add "Electrical Parameter" in" char. Process" column		
8.Add note of "F/T" and "ATE"	Wang Peng	11/30/2004
Added "V/M Sample Check" process in electrical test.	Wang Peng	11/23/2005
Updated "Core Team Member" and "Supplier/Plant Name"	Wang Peng/Yang Liang	11/10/2006
	wang rung rung bang	11,10,2000
Updated "Core Team Member" and revised some characteristics from process		
	Wang Peng/Yang Liang	9/28/2007
I.		4/15/2008
	wang i ciig	7/13/2000
2. Update Core ream Member		
3. Change title from "ZH630/ZH660 Test Flow" to "GENERAL TEST FLOW"		
	Change Process No from ZH670 to ZH670/ZH720  Added "V/M Sample Check" process in electrical test.  Updated "Core Team Member".  1. Updated "Core Team Member" and revised some characteristics from process column to product column;  2. change "VM sample check' to 'Machine Setup VM check' to clarify the VM check purpose on Electrical test process.  Change sample size to 200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k) from 200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k) from 200 Units/Lot(Lot size<10k) or 315 Units(lot size>10k)  1. Add '12MCT50040A' in control method and Reaction Plan column of INSP. step  2. Change Core Team name from 'Zhang Yupeng' to 'Yang Liang'  1. Add "PQFN" in "Title, Part Number & Name/Description"  2. Add"Albert Zheng(6192)" in" Key Contact/Phone".  3. Change "SPS" to "Freescale"  4. Add "Yield" in "char.process of Electrical Test"  5. Delete "Electrical Test" in "char. Product" column.  6. Take place "200 units/Lot" with "200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k)"  7. Add "Electrical Parameter" in" char. Process" column  8. Add note of "F/T" and "ATE"  Added "V/M Sample Check" process in electrical test.  Updated "Core Team Member" and "Supplier/Plant Name"  Updated "Core Team Member" and revised some characteristics from process column to product column; change 'VM sample check' to 'Machine Setup VM check' to clarify the VM check purpose on Electrical test process.  Delete the process description of B/I, Lot process & T/R from test process.  1. Core Team Review  2. Update "Core Team Member"	Change TTT or Tape&Reel' to Test Backend' Change Process No from ZH670 to ZH670/ZH720 Yang Liang Added "VM Sample Check" process in electrical test.  Updated "Core Team Member"  1. Updated "Core Team Member" and revised some characteristics from process column to product column; 2. change "VM sample check" to 'Machine Setup VM check' to clarify the VM check purpose on Electrical test process.  Change sample size to 200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k) from 200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k) from 200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k) Throm 200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k) Throm 200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k) Throm 200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k) Throm 200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k) Throm 200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k) Throm 200 Units/Lot(Lot size<10k) Throm 200 Units/Lot(Lot size<10k) Throm 200 Units/Lot(Lot size<10k) Throm 200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k) Throm 200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k) Throm 200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k) Throm 200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k) Throm 200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k) Throm 200 Units/Lot(Lot siz

		1	1
	4. Change part number from "ZH630/ZH660 Test Bank" to "GENERAL TEST"		
	5. Change description from "ZH630/ZH660 Test Bank Test Flow" to "GENERAL		
	TEST FLOW"		
	6. Change incoming check sample size from "200 Units/Lot (Lot Size <10K);315 Units/Lot (Size>=10K)" to "200 Units/Lot (Lot Size =<10K);315 Units/Lot (Size>10K)"		
	7. Change start lot check sample size from "200 Units/Lot (Lot Size <10K);315 Units/Lot (Size>=10K)" to "200 Units/Lot (Lot Size =<10K);315 Units/Lot (Size>10K)"		
	8. Change machine setup & V/M check sample size from "200 Units/Lot (Lot Size <10K);315 Units/Lot (Size>=10K)" to "200 Units/Lot (Lot Size =<10K);315 Units/Lot (Size>10K)"		
	9. Change ILG sample size from "Per Skip Plan" to "Per 12ACT20080A"		
	10. Change VM gate sample size from "200 Units/Lot (Lot Size <10K);315		
	Units/Lot (Size>=10K)" to "200 Units/Lot (Lot Size =<10K);315 Units/Lot		
AM	(Size>10K)"	Chen Wei/Yang Liang	5/5/2009
AN	12months review	Yang Liang/Chen Wei	5/4/2010
AP	12months review,no content change.	Yang Liang/Chen Wei	4/18/2011
	1. Add "ZHPT0" to process operation number		
	2. Change the reference of sample size to "Per 12ACT20080A"		
	3. Update the document numbers of "Specification", "Control Method" and "Control		
	plan" acoording to Doc_Rebuild project		
	4. Change step name from "VM Gate (Per shop order)" to "VM Inspection", change		
	the step symbol from "GATE" to "INSP"		
	5. For "VM Insepction" step, change the "Machine, Tools" and "Evaluation		
	Measurement Technique" to "Visual"		
AR	6. Add NOTE 3	Yang Liang/Chen Wei	10/17/2011
	1. Remove Han Z.L from core team member;		
	2. Replace "A" with "Visual Mechanical Defect";		
	3. Replace process specification of electrical test/gate process from "48A Spec" to		
	"Test Program" / "Gate Program"		
	4. Replace "Test Program" & "Gate Program" Measurement to "Electrical Test";		
AS	5. Replace gate process tool from "ILG" to "ATE"	Chen Wei/Yang Liang	12/9/2011

Update core team member     Split out "CENTRAL MATERIAL STAGING" step from "INCOMING CHECK" step, add detailed items into "INCOMING CHECK" step     Add detailed control method and reaction plan     Change freq. from "1x/lot" to "Every lot"	Chen Wei	9/21/2012
Core team review: 1. Change the process name from "CENTRAL MATERIAL STAGING" to "MATERIAL RECEIVING" 2. Move "machine preparation" from "INCOMING CHECK" to "ELECTRICAL TEST" 3. Update the wording of Characteristics	Chen Wei/Yang Liang	11/9/2012
Update Core team member     Update reaction plan	Chen Wei/Yang Liang	9/6/2013
	2. Split out "CENTRAL MATERIAL STAGING" step from "INCOMING CHECK" step, add detailed items into "INCOMING CHECK" step 3. Add detailed control method and reaction plan 4. Change freq. from "1x/lot" to "Every lot"  Core team review: 1. Change the process name from "CENTRAL MATERIAL STAGING" to "MATERIAL RECEIVING" 2. Move "machine preparation" from "INCOMING CHECK" to "ELECTRICAL TEST" 3. Update the wording of Characteristics  1. Update Core team member	2. Split out "CENTRAL MATERIAL STAGING" step from "INCOMING CHECK" step, add detailed items into "INCOMING CHECK" step  3. Add detailed control method and reaction plan  4. Change freq. from "1x/lot" to "Every lot"  Core team review:  1. Change the process name from "CENTRAL MATERIAL STAGING" to "MATERIAL RECEIVING"  2. Move "machine preparation" from "INCOMING CHECK" to "ELECTRICAL TEST"  3. Update the wording of Characteristics  Chen Wei/Yang Liang  1. Update Core team member  2. Update reaction plan  Chen Wei/Yang Liang

# Measurement System Studies (Gage R&R)

# **TSMC PPAP Documents**

- TSMC PPAP documents (FMEAs, Control Plans, Cpks, and GR&R) are considered proprietary information by TSMC, classified as "TSMC INTERNAL USE ONLY" and cannot be distributed with Freescale PPAPs in accordance with an agreement with TSMC.
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- If there are any questions, please contact:

Sally Cadena Massey, Freescale MSG NPI Reliability, 512-895-7310 sally.cadena.massey@freescale.com

Jeff Martsching, Freescale External Manufacturing, 512-996-4282 <u>Jeff.Martsching@freescale.com</u>





# **Gage Study Summary Report**

<b>Customer Part Number:</b>			
Company/Manufacturing Site ID:	Freescale / TJN		
Designate only one of the following	g and enter the appropriate information:		
Wafer Fab Process Technolog	gy:		
<b>Assembly Process Package Fa</b>	mily: SOIC32LD		
Physical Dimensions Package	<b>Drawing #:</b> 98ASA00259D_O		
	98ARH99137A_B		
☐ Test			
Special/Important	Measurement	%R&R	<b>Date Study</b>
Characteristic	Gage/Tool/Equipment	<u>1</u> /	Performed
Wire Pull	Wire pull tester – Dage4000 BBT-01	0.30%	May 11,2013
Ball Shear	Ball Shear tester – Dage4000 BBT-01	0.12%	May 11,2013
Plating Thickness	SFT3200 32300018	3.50%	Mar 05,2013
Tip-to-Tip	Projector - Nikon V-12BDC MPJ-03	0.21%	May 09, 2013
Coplanarity	Microscope- Nikon- MM-40 MMP-02	8.34%	May 09, 2013

1/1 If R&R > 10%, attach containment action, corrective action, or justification (as appropriate)

FORMPPAP007DOC Freescale Rev K

# **Dimensional Results**



#### PHYSICAL DIMENSION MEASUREMENT RESULT

rackage Type.	SOIC SZIU EF					
Assembly Site:	Freescale TJN	_		_		
Freescale 98A:	98ASA00259D	98A Rev:	0	98A Rev Date:	29-Jul-10	
ate of Teet Populter	16-Doc-13	<del>-</del>				

Freescale 98A:	98ASA00259D			-	98A Rev:	0		98A Rev Date:	29-Jul-10	-	
				-	96A HeV:			96A Rev Date:	29-Jul-10		
Date of Test Results:	16-Dec-13			-							
				Pa	ackage Dimensions p	er Freescale 98A (exa	ımple lenath, width, e	tc.)			
Dimension I	Description	Package width	Package length	Package height	Tip to Tip	Full height	Lead width	Lead lenth	Exposed Pad, X	Exposed Pad, Y	Coplanarity
	Min Per Freescale	·									
Spec Limits	98A	7.40	10.90	2.12	10.00	2.22	0.22	0.50	4.00	4.00	0.00
	Max Per Freescale										
Spec Limits	98A	7.60	11.10	2.45	10.60	2.45	0.38	0.90	5.20	5.20	0.10
Enter the measure	ed value for each										
dimension per unit fr	om 3 assembly lots										
Assembly Lot #	Unit #										
	1	7.536	11.017	2.276	10.298	2.337	0.328	0.668	4.484	4.487	0.016
	2	7.530	11.030	2.292	10.295	2.392	0.324	0.638	4.462	4.495	0.023
	3	7.547	11.026	2.303	10.294	2.350	0.326	0.667	4.488	4.448	0.014
	4	7.544	11.013	2.298	10.305	2.336	0.326	0.650	4.492	4.508	0.011
	5	7.542	11.006	2.292	10.300	2.334	0.332	0.647	4.480	4.485 4.493	0.020
	6	7.549 7.540	11.012 11.018	2.300 2.286	10.307 10.294	2.355 2.354	0.328 0.325	0.664 0.663	4.482 4.478	4.493 4.488	0.020 0.018
	8	7.539	11.018	2.299	10.294	2.354	0.325	0.662	4.475	4.488	0.009
	9	7.540	11.000	2.300	10.300	2.364	0.329	0.665	4.481	4.485	0.009
	10	7.536	11.016	2.303	10.303	2.350	0.326	0.649	4.490	4.500	0.017
Assembly Lot #	Unit #										
	1	7.544	11.011	2.295	10.294	2.339	0.328	0.668	4.484	4.487	0.016
	2	7.540	11.009	2.293	10.298	2.354	0.324	0.638	4.462	4.495	0.023
	3	7.539	11.020	2.301	10.302	2.337	0.326	0.667	4.488	4.448	0.014
	4	7.539	11.018	2.291	10.295	2.350	0.326	0.650	4.492	4.508	0.011
	5	7.542	11.009	2.296	10.298	2.336	0.332	0.647	4.480	4.485	0.020
	6	7.540	11.012	2.288	10.300	2.351	0.328	0.664	4.482	4.493	0.020
	7 8	7.539 7.549	11.018 11.016	2.292 2.303	10.300 10.296	2.358 2.339	0.325 0.331	0.663 0.662	4.478 4.475	4.488 4.473	0.018 0.009
	9	7.544	11.010	2.294	10.294	2.362	0.329	0.665	4.481	4.485	0.009
	10	7.543	11.015	2.300	10.298	2.358	0.326	0.649	4.490	4.500	0.017
		7.010	11.010	2.000	10.200	2.000	0.020	0.010	1.100	1.000	0.017
Lot #	Unit #										
	1	7.539	11.021	2.299	10.303	2.356	0.328	0.668	4.484	4.487	0.016
	2	7.539	11.019	2.298	10.301	2.344	0.324	0.638	4.462	4.495	0.023
	3	7.545	11.013	2.288	10.300	2.359	0.326	0.667	4.488	4.448	0.014
	4	7.536	11.015	2.304	10.296	2.353	0.326	0.650	4.492	4.508	0.011
	5	7.543	11.009	2.300	10.294	2.339	0.332	0.647	4.480	4.485	0.020
	<u>6</u> 7	7.546 7.540	11.012 11.018	2.282 2.293	10.302 10.292	2.332 2.361	0.328 0.325	0.664 0.663	4.482 4.478	4.493 4.488	0.020 0.018
	8	7.540	11.018	2.293	10.292	2.351	0.325	0.662	4.475	4.488	0.009
	9	7.542	11.011	2.296	10.298	2.380	0.329	0.665	4.481	4.485	0.011
	10	7.545	11.016	2.301	10.300	2.356	0.326	0.649	4.490	4.500	0.017
											*****
Calculate the following	for each dimension									1	
	MIN	7.530	11.006	2.276	10.292	2.332	0.324	0.638	4.462	4.448	0.009
	MAX	7.549	11.030	2.304	10.307	2.392	0.332	0.668	4.492	4.508	0.023
	AVERAGE	7.541	11.015	2.295	10.298	2.352	0.328	0.657	4.481	4.486	0.016
	STDEV	0.004	0.005	0.007	0.004	0.013	0.003	0.010	0.008	0.016	0.004
	WITHIN LIMIT	TRUE	TRUE	TRUE	TRUE	TRUE	TRUE	TRUE	TRUE	TRUE	TRUE
	Ср	8.16	6.25	8.33	27.45	2.86	10.66	6.66	24.07	12.62	3.81
	Cpk	4.80	5.33	7.81	27.30	2.44	7.00	5.24	19.30	10.22	6.41

27.30 2.44 1/ If Ppk < 1.67 or Cpk < 1.67 attach justification

FORMPPAP028XLS Freescale Rev G

# Material, Performance Test Results

			AUTOM	IOTIVE PRO	אוומכ	CT AF	C-Q100G Qua	lification	Test P	lan			
	Ohiectivo	Qualification of TSMC Fab SOIC32 4.6				J . AL	_		10011				
	ual Vehicle PN:	MC33972ATEK/R2 MSDISWA(EP)	Customer Name(s) PN(s)	: General Market			Test Program ID: Test Program Rev:	VARIOUS			Revision #:	QUAL PLAN 19Aug13	
							Rel. Circuits Doc. #:				Date:		
Packa	Technology: ge Description:	SM5AP SOIC 32 300ML 4.6EP	Mask set# Revision #				CAB #: FSL Qual Quartz Tracking #:	13342133M			Rel. Engr. Approval Signature: Date:	19Aug13	
	Assembly site: Final Test site:	FSL-TJN-FM	Product Engr Packaging Engr Reliability Engr	: Wang Brenda : Hosoda Daisuke : Tian Meng			Target Dates Test Start: Test Finish:	NA			CAB Approval	Yanil Cruz August 22 2013	
D	Rel Test site: ie Size (in mm) W x L x T	3.857x2.831	Part Operating Temp. Range AEC Grade				PPAP target date: Freescale Contact: Phone Number:	Bai Yun +86-85684236			Customer Approval Signature: Date:		
			ALO GIAGE		E-STR	ESS REC	UIREMENTS/OPTI	ONS			Date.		
Stress	JEDEC22	Test Conditions	End Point	Minimum	# of	Total			Results				Comments
	Reference		Requirements	Sample Size per lot	Lots	Units including spares	Lot A nominal	Lot B nominal		Lot C nominal	Lot D HH	Lot E LL	(Generic Data: Note 2)
PC	A113 J-STD-020	Preconditioning (PC) MSL 3 at 260 °C, +5/-0 °C CSAM: Note 3	TEST at RH (add C if PC before HTOL); CSAM	All surface mount THB/HAST, AC/U PC+PTC, or as re	HST, TO	prior to							PC is performed and results reported as part of the individual stress tests.
	ļ.								<u> </u>				
				GROUP A A	CELE	DATED	NVIRONMENTAL S	TDEGG TEG	re				
HAST	A110	Highly Accelerated Stress Test (HAST):	TEST @ RH;	77	5	400	.ivvinonivieni AL S	INESS IES	13				When biased humidity is
		PC before HAST if required. HAST = 110 °C/85%RH for 264hrs,528hrs FIO Bias: per HAST schematic Timed RO of 48hrs. MAX	CSAM										required either HAST or THE can be performed. HAST is the preferred biased humidity test.
UHST	A118	Unbiased HAST (UHST): PC before UHST if required. UHST = 110 °C/85%RH for 264hrs,528hrs FIO Timed RO of 48hrs. MAX	TEST @ R; CSAM	77	5	400							When unbaised humidity testing is required, UHST is the preferred unbiased humidity test. The AC optic is NOT recommended.
тс	A104 AEC Q100- Appendix 3	Temperature Cycle (TC): PC before TC if required. TC = -50 ℃ to 150 ℃ for 1000 cycles,2000cycles FIO WBP after qual readpoint on 5 devices from each lot; 2 bonds per corner and one mid-bond per side on each device. Record which pins	TEST @ H WBP =/> 3 grams CSAM	77	5	400							If WP is to be performed at interim readpoints, add additional samples so that the minimum sample size is maintained for the final readpoint.
HTSL	A103	were used.  High Temperature Storage Life (HTSL):  HTSL = 150 ℃ for 1008 hrs,2016hrs FIO  Timed RO = 96hrs. MAX	TEST @ RH	45	3	144							
		Timed 110 – 90113. WAX		TEST GROUP I	B - ACC	CELERAT	ED LIFETIME SIMU	JLATION TES	STS				
HTOL	A108	High Temperature Operating Life (HTOL): HTOL = 100 ℃ for 1008 hrs,2016hrs FIO Bias:5V and 28V Timed RO of 96hrs. MAX	TEST @ RHC;	77	3	240							Perform HTOL on two lots and reuse third lot from Cosslite TSMC
ELFR	AEC Q100- 008	Early Life Failure Rate ELFR): ELFR = 100 ℃ for 48 hrs; Timed RO of 48 hrs MAX	TEST @ RH	800	3	2409							Perform ELFR on two lots and reuse third lot from Cosslite TSMC
				TEST GROU	PC-P	ACKAGE	ASSEMBLY INTE	GRITY TESTS	}				
ull Assy. CZ + Cu WB Cz	FSL Internal Requirement	Full assembly process CZ Data collection per FSL CZ template (for Cu WB) for 3 tech cert lots with nominal Cu WB process.  Perform Wire Bond CZ specifically for Copper Wire for 1 HH and 1 LLTech Cert lots.			5	- i - i - i - i - i - i - i - i - i - i							
WBS	AEC Q100- 001	Wire Bond shear (WBS)	Cpk = or > 1.67	30 bonds from minimum 5 units	3	15							Performed by Assembly Site during qual lot builds - PE to include this requirement in th qual lot build ERF.

WBP	MilStd883- 2011	Wire Bond Pull (WBP): Cond. C or D	Cpk = or > 1.67	30 bonds from minimum 5 units		15 <b>ΣΙΕ ΕΔΒΙ</b>	RICATION RELIAB	II ITY TESTS		Performed by Assembly Site during qual lot builds - PE to include this requirement in the qual lot build ERF
							RICAL VERIFICATI			
TEST	48A	Pre- and Post Functional / Parametrics (TEST): Test software shall meet requirements of AEC-Q100-007. Testing performed to the limits of device specification in temperature and limit value.	0 Fails	All	All	All				TEST results is shown for each individual stress test in the qual results report generated upon qual completion. FSL SQA release required for qual test program.
ED	AEC-Q100- 009, Freescale 48A spec	Electrical Distribution (ED)	TEST @ RHC Cpk = or > 1.67	30	3	90				dour test brogram.

General Notes: Generic Data Reference List: Notes:This Data will be used to qualify the following devices:

	al Vahiela PNI	MC33972ATEK/R2	Customer Name(s):	General Market			Test Program ID:	VARIOUS		Report Type:	QUALRESULT	
		MSDISWA(EP)	PN(s):				Test Program Rev:				28Oct2013	
Quai V	cincic riame	MISDISWA(EF)	114(3).				restriogrammer.	•		Date:	200012010	
							Rel. Circuits Doc. #:			Duio		
	Technology:	SM5AP	Mask set#:	N39B			CAB #:	: 13342133M		Rel. Engr. Approval	Tian Meng	
Package	e Description:	SOIC 32 300ML 4.6EP	Revision #:					222708 G630AY			28Oct2013	
							Tracking #:			Date:		
		TSMC-Fab		Wang Brenda			Target Dates			CAB Approval		
		FSL-TJN-FM		Hosoda Daisuke	•		Test Start:				07NOV2013	
		FSL-TJN-FM	Reliability Engr:	Tian Meng			Test Finish:			Date:		
	Rel Test site:						PPAP target date:					
Die	Size (in mm)		Part Operating				Freescale Contact:			Customer Approval		
	WxLxT		Temp. Range:				Phone Number:	+86-85684236		Signature:		
			AEC Grade:							Date:		
				PR	E-STR	RESS REQ	UIREMENTS/OPTI	IONS				
Stress	JEDEC22	Test Conditions	End Point	Minimum	# of	Total			esults			Comments
	Reference		Requirements	Sample Size per	Lots	Units	Lot A	Lot B	Lot C	Lot D	Lot E	(Generic Data: Note 2)
				lot		including	nominal	nominal	nominal	HH	LL	
						spares						
PC	A113	Preconditioning (PC)	TEST at RH (add C if									PC is performed and results
		MSL 3 at 260 °C, +5/-0 °C	PC before HTOL);	THB/HAST, AC/L								reported as part of the
		CSAM: Note 3	CSAM	PC+PTC, or as re	equired	per						individual stress tests.

				GROUP A - AC	CELE	RATED F	NVIRONMENTAL	STRESS TESTS				
HAST	A110	Highly Accelerated Stress Test (HAST):	TEST @ RH;	77	5	400			Reuse Cosslite Data	Reuse Cosslite Data	Reuse Cosslite Data	When biased humidity is
	,	PC before HAST if required. HAST = 110 °C/85%RH for 264hrs,528hrs FIO Bias: per HAST schematic Timed RO of 48hrs. MAX	CSAM		Ü	.00	264hrs: 0/80 528hrs: 0/80	264hrs: 0/80 528hrs: 0/80	264hrs: 0/80 528hrs: 0/80	264hrs: 0/80 528hrs: 0/80	264hrs: 0/80 528hrs: 0/80	required either HAST or THB can be performed. HAST is the preferred biased humidity test.
UHST		Unblased HAST (UHST): PC before UHST if required. UHST = 110 °C/85%-RH for 264hrs,528hrs FIO Timed RO of 48hrs. MAX	TEST @ R; CSAM	77	5	400	264hrs: 0/80 528hrs: 0/80	96hrs: 0/80 192hrs: 0/80	Reuse Cosslite Data 96hrs: 0/80 192hrs: 0/80	264hrs: 0/80 528hrs: 0/80	264hrs: 0/80 528hrs: 0/80	When unbaised humidity testing is required, UHST is the preferred unbiased humidity test. The AC option is NOT recommended.
тс	A104 AEC Q100- Appendix 3	Temperature Cycle (TC): PC before TC if required. TC = -50°C to 150°C for 1000 cycles,2000cycles FIO WBP after qual readpoint on 5 devices from each lot; 2 bonds per corner and one mid-bond per side on each device. Record which pins were used.	TEST @ H WBP =/> 3 grams CSAM	77	5	400	1000cyc: 0/80 2000cyc: 0/80 WP pass	Reuse Cosslite Data 1000cyc: 0/80 2000cyc: 0/80 WP pass	Reuse Cosslite Data 1000cyc: 0/80 2000cyc: 0/80 WP pass	1000cyc: 0/80 2000cyc: 0/80 WP pass	1000cyc: 0/80 2000cyc: 0/80 WP pass	If WP is to be performed at interim readpoints, add additional samples so that the minimum sample size is maintained for the final readpoint.
HTSL	A103	High Temperature Storage Life (HTSL):  HTSL = 150 ℃ for 1008 hrs,2016hrs FIO  Timed RO = 96hrs. MAX	TEST @ RH	45	3	144	1008hrs: 0/48 2016hrs: 0/48			Reuse Cosslite Data 1008hrs: 0/48 2016hrs: 0/48	Reuse Cosslite Data 1008hrs: 0/48 2016hrs: 0/48	
				TEST GROUP B	- AC	CELEBAT	ED LIFETIME SIM	III ATION TESTS				
HTOL	A108	High Temperature Operating Life (HTOL): HTOL = 100 °C for 1008 hrs,2016hrs FIO Bias:5V and 28V Timed RO of 96hrs. MAX	TEST @ RHC;	77	3	240	1008hrs: 0/80 2016hrs: 0/80	Reuse Cosslite data 1008hrs: 0/80 2016hrs: 0/80			1008hrs: 0/80 2016hrs: 0/80	Perform HTOL on two lots and reuse third lot from Cosslite TSMC
ELFR	AEC Q100- 008	Early Life Failure Rate ELFR): ELFR = 100 °C for 48 hrs; Timed RO of 48 hrs MAX	TEST @ RH	800	3	2409	0/803	0/803	Reuse Cosslite data 0/803			Perform ELFR on two lots and reuse third lot from Cosslite TSMC
				TEST GROUP	- C -	PACKAGE	ASSEMBLY INTE	GRITY TESTS				
Full Assy. CZ + Cu WB Cz		Full assembly process CZ Data collection per FSL CZ template (for Cu WB) for 3 tech cert lots with nominal Cu WB process. Perform Wire Bond CZ specifically for Copper Wire for 1 HH and 1 LLTech Cert lots.			5		Pass	Pass	Pass	Pass	Pass	
WBS	AEC Q100- 001	Wire Bond shear (WBS)	Cpk = or > 1.67	30 bonds from minimum 5 units	3	25	Pass			Pass	Pass	Performed by Assembly Site during qual lot builds - PE to include this requirement in the qual lot build ERF.
WBP	MilStd883- 2011	Wire Bond Pull (WBP): Cond. C or D	Cpk = or > 1.67	30 bonds from minimum 5 units	3	25	Pass			Pass	Pass	Performed by Assembly Site during qual lot builds - PE to include this requirement in the qual lot build ERF
							RICATION RELIAB					
TEAT		Due and Deat Franchis 112	05."				RICAL VERIFICAT	ION TESTS				TEOT
TEST	Freescale 48A	Pre- and Post Functional / Parametrics (TEST): Test software shall meet requirements of AEC- Q100-007. Testing performed to the limits of device specification in temperature and limit value.	0 Fails	All	All	All						TEST results is shown for each individual stress test in the qual results report generated upon qual completion. FSL SQA release required for qual test program.
ED	AEC-Q100- 009, Freescale 48A spec	Electrical Distribution (ED)	TEST @ RHC Cpk = or > 1.67	30	3	90	Pass	Pass	Pass			



#### PRODUCT AND PROCESS CHANGE NOTIFICATION

Generic Copy

ISSUE DATE: 12-Dec-2013 NOTIFICATION: 15977

TITLE: SOIC32 300ML 4.6EP/Non-EP TSMC SMOS5 Copper Wire Qualification

**EFFECTIVE DATE:** 12-Mar-2014

#### **DEVICE(S)**

MPN

MC33972ATEK

MC33972ATEKR2

MC33972ATEWR2

MC33972TEW

MC33972TEWR2

MC33975ATEK

MC33975ATEKR2

MC33975TEK

MC33975TEK

MC33975TEK

MC33975TEK

MC34972ATEKR2

MC34972ATEKR2

MC34972ATEKR2

MC34972ATEWR2

MC34975ATEK MC34975ATEKR2

#### **AFFECTED CHANGE CATEGORIES**

BILL OF MATERIAL CHANGE (SAME ASSEMBLY SITE)

#### **DESCRIPTION OF CHANGE**

Freescale Semiconductor announces the addition of Copper Wire as a wirebond material and Sumitomo EME-G630AY Molding Compound as mold material for SMOS5 SOIC32 300ML 4.6EP and Non-EP package devices displayed in this notification. These products were previously assembled with Gold (Au) wire and Hitachi CEL9220HF13 mold compound at Freescale TJN assembly site, Tianjin, China. These products are now qualified for assembly with Copper (Cu) wire and EME-G630AY mold compound at Freescale TJN assembly site, Tianjin, China.

Sample Parts Available: KC33972ATEK/R2 KC33972ATEW/R2 KC33975TEK/R2 KC33975ATEK/R2

#### **REASON FOR CHANGE**

The transfer from Gold to Copper wire and CEL9220HF13 to EME-G630AY mold compound are required to mitigate against raw material cost increases and for supply assurance.

#### ANTICIPATED IMPACT OF PRODUCT CHANGE(FORM, FIT, FUNCTION, OR RELIABILITY)

Freescale Confidential Proprietary

No change to form, fit or function. Reliability is equivalent or improved.

Freescale will consider specific conditions of acceptance of this change submitted within 30 days of receipt of this notice on a case by case basis. To request further data or inquire about the notification, please enter a Service Request. For sample inquiries - please go to http://freescale.com/

**QUAL DATA AVAILABILITY DATE:** 29-Nov-2013

**QUALIFICATION STATUS:** COMPLETED

**QUALIFICATION PLAN:** 

See attached qualification results.

#### **RELIABILITY DATA SUMMARY:**

See attached qualification results.

#### **ELECTRICAL CHARACTERISTIC SUMMARY:**

No change to datasheet. No change to Electrical Distributions.

#### **CHANGED PART IDENTIFICATION:**

There is no change to orderable part number. The Tracecode marking on the device includes assembly site and datecode. Freescale will have traceability by assembly site and datecode.

#### **NOTIFICATION CONTACT:**

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#### **SAMPLE AVAILABILITY DATE:** 17-Dec-2013

#### ATTACHMENT(S):

External attachment(s) for this notification can be viewed at: 15977\_Analog\_Cu\_Wire\_SOIC\_Mold\_Compound\_Change\_GPCN.pdf 15977\_MSDISW\_Copper\_Wire\_G630AY\_Electrical\_Distribution\_GPCN.pdf 15977\_SOIC\_MSDI\_Family\_Copper\_Wire\_with\_G630AY\_MC\_Qual\_Results\_GPCN.pdf

							Lo	ot1			Lo	t2			Lo	ot3	
Test#	Test Name	Lo Limit	Hi Limit	Unit	Temp	Mean	Std Dev	Ср	Cpk	Mean	Std Dev	Ср	Cpk	Mean	Std Dev	Ср	Cpk
2	IPWR on @ 8v	0	4	mA	HT	2.82	0.02	36.96	21.86	2.82	0.02	36.36	21.44	2.82	0.02	38.92	22.95
2	IPWR on @ 8v	0	4	mA	RT	2.86	0.02	37.81	21.52	2.86	0.02	35.78	20.37	2.86	0.02	28.98	16.45
2	IPWR on @ 8v	0	4	mA	CT	2.85	0.02	26.79	15.39	2.85	0.02	27.27	15.74	2.85	0.03	22.78	13.08
3	IPWR on @ 16v	0	4	mA	HT	3.18	0.02	31.73	12.93	3.19	0.02	31.92	12.88	3.19	0.02	50.30	13.56
3	IPWR on @ 16v	0	4	mA	RT	3.23	0.02	34.19	13.18	3.23	0.02	31.96	12.25	3.24	0.03	25.52	9.76
3	IPWR on @ 16v	0	4	mA	CT	3.18	0.03	24.57	10.11	3.18	0.03	25.96	10.70	3.18	0.03	20.30	8.31
4	IPWR ss	40	100	uA	HT	80.15	0.74	13.43	8.88	81.22	0.78	12.89	8.07	80.43	0.56	17.78	11.60
4	IPWR ss	40	100	uA	RT	79.74	0.54	18.68	12.62	80.49	0.76	13.09	8.51	80.03	0.47	21.14	14.07
4	IPWR ss	40	100	uA	CT	75.27	0.78	12.87	10.61	75.93	0.72	13.93	11.17	75.45	0.58	17.26	14.12
5	IDD ss	-20	20	uA	HT	12.09	0.21	15.65	12.38	12.25	0.20	16.70	12.94	12.14	0.24	13.81	10.86
5	IDD ss	-20	20	uA	RT	12.45	0.28	11.78	8.90	12.58	0.26	12.62	9.37	12.46	0.30	11.28	8.50
5	IDD ss	-20	20	uA	CT	11.29	0.29	11.33	9.87	11.40	0.30	11.13	9.57	11.34	0.35	9.41	8.15
8	IDD @ 5vdd	-500	500	uA	HT	37.29	0.72	116.17	17.33	37.37	0.58	144.83	21.65	37.16	0.70	118.80	17.66
8	IDD @ 5vdd	-500	500	uA	RT	55.36	1.03	80.76	17.88	55.39	0.91	92.00	20.38	55.17	1.04	80.35	17.73
8	IDD @ 5vdd	-500	500	uA	CT	76.83	1.67	49.86	15.32	76.54	1.34	62.33	19.08	76.32	1.66	50.08	15.29
9	SP0 iwetting batt = 28v	12	18	mA	HT	16.32	0.16	6.26	3.50	16.32	0.16	6.20	3.46	16.36	0.14	3.65	3.30
9	SP0 iwetting batt = 28v	12	18	mA	RT	16.22	0.16	6.38	3.78	16.20	0.16	6.31	3.78	16.24	0.17	5.97	3.49
9	SP0 iwetting batt = 28v	12	18	mA	CT	15.98	0.18	5.49	3.70	15.94	0.19	3.56	3.46	16.01	0.21	4.76	3.16
10	SP1 iwetting batt 268v	12	18	mA	HT	16.34	0.15	6.54	3.62	16.33	0.15	6.63	3.70	16.38	0.13	3.76	3.46
10	SP1 iwetting batt 268v	12	18	mA	RT	16.28	0.16	6.31	3.62	16.25	0.14	4.20	4.19	16.29	0.15	6.73	3.82
10	SP1 iwetting batt 268v	12	18	mA	CT	16.08	0.19	5.19	3.32	16.03	0.16	4.07	4.01	16.11	0.20	3.37	3.19
11	SP2 iwetting batt 28v	12	18	mA	HT	16.36	0.15	6.61	3.62	16.37	0.17	6.02	3.27	16.40	0.14	3.67	3.42
11	SP2 iwetting batt 28v	12	18	mA	RT	16.31	0.14	6.94	3.92	16.30	0.16	3.66	3.56	16.33	0.16	6.24	3.48
11	SP2 iwetting batt 28v	12	18	mA	CT	16.13	0.18	5.50	3.43	16.09	0.18	3.67	3.51	16.14	0.20	3.26	3.02
12	SP3 iwetting batt 28v	12	18	mA	HT	16.30	0.15	6.62	3.75	16.30	0.16	6.28	3.57	16.34	0.12	4.26	3.81
12	SP3 iwetting batt 28v	12	18	mA	RT	16.25	0.15	6.51	3.79	16.23	0.13	4.45	4.40	16.27	0.13	7.59	4.37
12	SP3 iwetting batt 28v	12	18	mA	CT	16.07	0.18	5.52	3.55	16.01	0.17	3.92	3.91	16.09	0.19	3.58	3.41
13	SP4 iwetting batt = 28v	12	18	mA	HT	16.29	0.16	6.42	3.66	16.27	0.15	6.73	3.87	16.33	0.12	4.03	3.56
13	SP4 iwetting batt = 28v	12	18	mA	RT	16.21	0.15	6.53	3.91	16.15	0.13	4.35	4.10	16.21	0.15	6.83	4.08
13	SP4 iwetting batt = 28v	12	18	mA	CT	15.98	0.18	5.67	3.82	15.90	0.16	4.29	4.06	15.99	0.20	3.36	3.34
14	SP5 iwetting batt = 28v	12	18	mA	HT	16.30	0.16	6.11	3.47	16.32	0.15	6.63	3.71	16.35	0.13	3.76	3.39
14	SP5 iwetting batt = 28v	12	18	mA	RT	16.24	0.16	6.19	3.63	16.24	0.14	4.12	4.09	16.28	0.15	6.46	3.71
14	SP5 iwetting batt = 28v	12	18	mA	CT	16.04	0.20	5.07	3.31	16.02	0.17	4.00	3.96	16.08	0.21	3.22	3.09
15	SP6 iwetting batt = 28v	12	18	mA	HT	16.33	0.15	6.88	3.83	16.34	0.16	6.45	3.58	16.38	0.14	3.49	3.20
15	SP6 iwetting batt = 28v	12	18	mA	RT	16.28	0.13	7.46	4.27	16.26	0.14	4.12	4.11	16.30	0.16	6.28	3.55
15	SP6 iwetting batt = 28v	12	18	mA	CT	16.11	0.16	6.16	3.89	16.04	0.18	3.67	3.59	16.12	0.21	3.23	3.03
16	SP7 iwetting batt = 28v	12	18	mA	HT	16.27	0.14	7.20	4.15	16.28	0.15	6.46	3.70	16.31	0.14	3.62	3.16
16	SP7 iwetting batt = 28v	12	18	mA	RT	16.21	0.13	7.44	4.45	16.19	0.16	3.72	3.58	16.22	0.16	6.33	3.75
16	SP7 iwetting batt = 28v	12	18	mA	CT	16.01	0.16	6.19	4.10	15.97	0.19	3.51	3.45	16.03	0.21	3.24	3.19
17	SP0 iwetting gnd vbatt=28v	-18	-12	mA	HT	-16.06	0.12	8.07	5.22	-16.09	0.17	6.02	3.83	-16.11	0.12	5.42	5.24
17	SP0 iwetting gnd vbatt=28v	-18	-12	mA	RT	-16.13	0.12	8.11	5.05	-16.12	0.17	3.85	3.70	-16.18	0.14	4.60	4.28
17	SP0 iwetting gnd vbatt=28v	-18	-12	mA	CT	-15.86	0.16	6.11	4.35	-15.83	0.18	5.44	3.93	-15.91	0.17	5.98	4.17
18	SP1 iwetting gnd vbatt=28v	-18	-12	mA	HT	-16.02	0.13	7.49	4.95	-16.04	0.15	4.38	4.34	-16.08	0.13	5.19	5.12
18	SP1 iwetting gnd vbatt=28v	-18	-12	mA	RT	-16.10	0.14	7.29	4.61	-16.07	0.14	4.64	4.59	-16.13	0.13	4.91	4.69
18	SP1 iwetting gnd vbatt=28v	-18	-12	mA	CT	-15.82	0.17	5.78	4.19	-15.77	0.16	6.10	4.53	-15.85	0.16	6.28	4.50
19	SP2 iwetting gnd vbatt=28v	-18	-12	mA	HT	-16.02	0.14	7.08	4.66	-16.05	0.16	4.18	4.18	-16.07	0.12	5.57	5.52
19	SP2 iwetting gnd vbatt=28v	-18	-12	mA	RT	-16.10	0.14	7.26	4.60	-16.09	0.15	4.27	4.19	-16.11	0.13	4.86	4.71
19	SP2 iwetting gnd vbatt=28v	-18	-12	mA	CT	-15.81	0.17	5.93	4.33	-15.76	0.17	6.02	4.49	-15.81	0.17	6.04	4.42
20	SP3 iwetting gnd vbatt=28v	-18	-12	mA	HT	-15.99	0.15	6.88	4.60	-16.02	0.17	3.93	3.86	-16.06	0.14	4.75	4.73
20	SP3 iwetting gnd vbatt=28v	-18	-12	mA	RT	-16.05	0.14	7.02	4.56	-16.03	0.15	4.25	4.21	-16.09	0.15	4.19	4.10
20	SP3 iwetting gnd vbatt=28v	-18	-12	mA	CT	-15.77	0.18	5.61	4.18	-15.71	0.18	5.64	4.30	-15.79	0.18	5.50	4.05
21	SP4 iwetting gnd vbatt=28v	-18	-12	mA	HT	-15.97	0.12	8.17	5.52	-16.05	0.15	4.27	4.26	-16.03	0.14	4.72	4.68
21	SP4 iwetting gnd vbatt=28v	-18	-12	mA	RT	-16.04	0.12	8.43	5.51	-16.10	0.16	4.07	3.97	-16.10	0.16	4.03	3.94
21	SP4 iwetting gnd vbatt=28v	-18	-12	mA	CT	-15.76	0.15	6.53	4.89	-15.78	0.18	5.45	4.03	-15.79	0.19	5.35	3.95
22	SP5 iwetting gnd vbatt=28v	-18	-12	mA	HT	-15.96	0.13	7.95	5.39	-16.01	0.17	3.80	3.72	-16.01	0.11	5.81	5.70
22	SP5 iwetting gnd vbatt=28v	-18	-12	mA	RT	-16.04	0.13	7.45	4.88	-16.04	0.15	4.20	4.19	-16.06	0.14	4.77	4.73
22	SP5 iwetting gnd vbatt=28v	-18	-12	mA	CT	-15.77	0.16	6.12	4.55	-15.74	0.17	5.96	4.49	-15.78	0.16	6.34	4.69
23	SP6 iwetting gnd vbatt=28v	-18	-12	mA	HT	-15.99	0.14	7.04	4.73	-16.04	0.16	4.13	4.11	-16.04	0.11	5.70	5.67
23	SP6 iwetting gnd vbatt=28v	-18	-12	mA	RT	-16.07	0.13	7.65	4.92	-16.09	0.15	4.35	4.27	-16.08	0.12	5.28	5.18
23	SP6 iwetting gnd vbatt=28v	-18	-12	mA	CT	-15.79	0.16	6.40	4.71	-15.79	0.18	5.47	4.04	-15.81	0.16	6.23	4.54
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Test#	Test Name	Lo Limit	Hi Limit	Unit	Temp	Mean	Std Dev	Ср	Cpk	Mean	Std Dev	Ср	Cpk	Mean	Std Dev	Ср	Cpk
24	SP7 iwetting gnd vbatt=28v	-18	-12	mA	HT	-16.01	0.15	6.86	4.56	-16.05	0.16	4.10	4.09	-16.06	0.12	5.60	5.58
24	SP7 iwetting gnd vbatt=28v	-18	-12	mA	RT	-16.09	0.15	6.60	4.19	-16.03	0.16	4.18	4.05	-16.13	0.12	5.04	4.84
24	SP7 iwetting gnd vbatt=28v	-18	-12	mA	CT	-15.82	0.13	5.86	4.19	-15.83	0.10	5.75	4.03	-15.86	0.13	7.19	5.12
25	SG0 wetting grid vbatt=28v	-18	-12	mA	HT	-16.08	0.17	7.03	4.49	-16.10	0.17	4.25	4.17	-16.13	0.14	5.55	5.33
25	SG0 wetting current vbatt=28v	-18	-12	mA	RT	-16.13	0.14	7.03	4.49	-16.12	0.13	4.50	4.33	-16.15	0.12	4.91	4.63
25	SG0 wetting current vbatt=28v	-18	-12	mA	CT	-15.83	0.14	5.77	4.18	-10.12	0.14	6.24	4.58	-15.86	0.13	6.43	4.58
26	SG1 wetting current vbatt=28v	-18	-12	mA	HT	-16.02	0.17	7.14	4.71	-16.03	0.10	3.84	3.80	-16.08	0.10	5.20	5.12
26	SG1 wetting current vbatt=28v	-18	-12	mA	RT	-16.06	0.14	7.13	4.61	-16.03	0.17	4.15	4.10	-16.10	0.13	4.57	4.45
26	SG1 wetting current vbatt=28v	-18	-12	mA	CT	-15.76	0.17	5.91	4.42	-15.70	0.18	5.55	4.26	-15.78	0.17	5.87	4.34
27	SG2 wetting current vbatt=28v	-18	-12	mA	HT	-16.01	0.17	7.60	5.05	-16.05	0.10	3.83	3.82	-16.07	0.17	4.93	4.88
27	SG2 wetting current vbatt=28v	-18	-12	mA	RT	-16.04	0.13	7.48	4.88	-16.06	0.17	3.83	3.82	-16.11	0.15	4.41	4.28
27	SG2 wetting current vbatt=28v	-18	-12	mA	CT	-15.75	0.17	5.99	4.49	-15.73	0.17	5.37	4.07	-15.79	0.17	6.02	4.44
28	SG3 wetting current vbatt=28v	-18	-12	mA	HT	-16.06	0.13	7.62	4.92	-16.09	0.16	4.15	4.07	-16.12	0.12	5.25	5.05
28	SG3 wetting current vbatt=28v	-18	-12	mA	RT	-16.11	0.12	8.03	5.05	-16.11	0.15	4.44	4.30	-16.17	0.14	4.66	4.37
28	SG3 wetting current vbatt=28v	-18	-12	mA	CT	-15.81	0.16	6.45	4.70	-15.79	0.17	5.94	4.37	-15.86	0.17	6.06	4.31
29	SG4 wetting current vbatt=28v	-18	-12	mA	HT	-15.99	0.13	7.90	5.28	-16.04	0.16	4.09	4.07	-16.05	0.17	4.88	4.87
29	SG4 wetting current vbatt=28v	-18	-12	mA	RT	-16.06	0.13	7.82	5.06	-16.09	0.16	4.10	4.02	-16.12	0.16	4.17	4.02
29	SG4 wetting current vbatt=28v	-18	-12	mA	CT	-15.78	0.15	6.62	4.90	-15.79	0.18	5.58	4.12	-15.82	0.10	5.37	3.90
30	SG5 wetting current vbatt=28v	-18	-12	mA	HT	-15.99	0.13	7.70	5.17	-16.04	0.16	4.07	4.04	-16.05	0.13	5.55	5.54
30	SG5 wetting current vbatt=28v	-18	-12	mA	RT	-16.05	0.13	7.82	5.08	-16.08	0.16	4.11	4.05	-16.09	0.12	5.28	5.17
30	SG5 wetting current vbatt=28v	-18	-12	mA	CT	-15.77	0.16	6.09	4.52	-15.77	0.18	5.65	4.19	-15.79	0.15	6.78	5.00
31	SG6 wetting current vbatt=28v	-18	-12	mA	HT	-16.04	0.14	7.37	4.82	-16.10	0.17	3.75	3.65	-16.11	0.12	5.25	5.10
31	SG6 wetting current vbatt=28v	-18	-12	mA	RT	-16.13	0.13	7.49	4.67	-16.18	0.17	3.84	3.59	-16.20	0.13	5.09	4.71
31	SG6 wetting current vbatt=28v	-18	-12	mA	CT	-15.87	0.16	6.34	4.50	-15.88	0.18	5.67	4.01	-15.91	0.15	6.50	4.53
32	SG7 wetting current vbatt=28v	-18	-12	mA	HT	-15.97	0.13	7.99	5.42	-16.01	0.15	4.39	4.31	-16.02	0.11	5.79	5.71
32	SG7 wetting current vbatt=28v	-18	-12	mA	RT	-16.04	0.12	8.20	5.36	-16.06	0.14	4.55	4.53	-16.09	0.13	4.84	4.73
32	SG7 wetting current vbatt=28v	-18	-12	mA	CT	-15.77	0.15	6.79	5.04	-15.77	0.17	5.98	4.44	-15.82	0.17	6.03	4.38
33	SG8 wetting current vbatt=28v	-18	-12	mA	HT	-15.93	0.13	7.60	5.24	-15.95	0.15	4.22	4.00	-15.99	0.13	4.92	4.78
33	SG8 wetting current vbatt=28v	-18	-12	mA	RT	-16.01	0.13	7.93	5.25	-15.99	0.14	4.55	4.41	-16.05	0.16	4.10	4.10
33	SG8 wetting current vbatt=28v	-18	-12	mA	CT	-15.72	0.17	6.03	4.58	-15.69	0.16	6.31	4.86	-15.75	0.19	5.20	3.90
34	SG9 wetting current vbatt=28v	-18	-12	mA	HT	-15.96	0.14	21.91	4.97	-16.00	0.14	4.50	4.39	-16.02	0.13	5.06	4.97
34	SG9 wetting current vbatt=28v	-18	-12	mA	RT	-16.03	0.12	8.31	5.45	-16.05	0.14	4.66	4.65	-16.08	0.14	4.74	4.67
34	SG9 wetting current vbatt=28v	-18	-12	mA	CT	-15.74	0.14	6.92	5.20	-15.75	0.16	6.31	4.73	-15.78	0.16	6.41	4.74
35	SG10 wetting current vbatt=28v	-18	-12	mA	HT	-15.95	0.13	7.65	5.24	-16.00	0.15	4.37	4.25	-16.03	0.12	5.46	5.41
35	SG10 wetting current vbatt=28v	-18	-12	mA	RT	-16.01	0.13	7.59	5.03	-16.04	0.14	4.63	4.60	-16.11	0.13	5.00	4.85
35	SG10 wetting current vbatt=28v	-18	-12	mA	CT	-15.73	0.16	6.13	4.64	-15.73	0.17	5.90	4.46	-15.81	0.16	6.22	4.54
36	SG11 wetting current vbatt=28v	-18	-12	mA	HT	-15.95	0.13	7.42	5.07	-16.01	0.14	4.57	4.49	-16.02	0.13	4.96	4.90
36	SG11 wetting current vbatt=28v	-18	-12	mA	RT	-16.02	0.13	7.52	4.96	-16.06	0.14	4.80	4.76	-16.10	0.14	4.70	4.57
36	SG11 wetting current vbatt=28v	-18	-12	mA	CT	-15.73	0.16	6.42	4.85	-15.77	0.16	6.35	4.72	-15.81	0.16	6.35	4.63
37	SG12 wetting current vbatt=28v	-18	-12	mA	HT	-15.96	0.13	7.50	5.10	-16.01	0.15	4.28	4.20	-16.03	0.12	5.29	5.22
37	SG12 wetting current vbatt=28v	-18	-12	mA	RT	-16.03	0.13	7.44	4.89	-16.05	0.15	4.40	4.39	-16.08	0.13	4.94	4.86
37	SG12 wetting current vbatt=28v	-18	-12	mA	CT	-15.75	0.16	6.11	4.58	-15.76	0.16	6.23	4.65	-15.80	0.15	6.53	4.79
38	SG13 wetting current vbatt=28v	-18	-12	mA	HT	-15.95	0.14	7.34	5.02	-16.01	0.15	4.39	4.30	-16.01	0.12	5.21	5.10
38	SG13 wetting current vbatt=28v	-18	-12	mA	RT	-16.05	0.14	7.25	4.72	-16.09	0.15	4.42	4.33	-16.10	0.13	5.20	5.06
38	SG13 wetting current vbatt=28v	-18	-12	mA	CT	-15.79	0.16	6.19	4.57	-15.80	0.17	6.03	4.43	-15.82	0.15	6.89	5.01
39	SP0 isustain batt 28v	1.8	2.2	mA	HT	2.12	0.02	3.17	1.33	2.12	0.02	3.37	1.43	2.12	0.02	3.94	1.67
39	SP0 isustain batt 28v	1.8	2.2	mA	RT	2.11	0.02	3.26	1.45	2.11	0.02	3.65	1.71	2.11	0.02	3.33	1.54
39	SP0 isustain batt 28v	1.8	2.2	mA	CT	2.09	0.02	2.71	1.54	2.08	0.02	3.10	1.89	2.09	0.03	2.46	1.44
40	SP1 isustain batt 28v	1.8	2.2	mA	HT	2.12	0.02	3.15	1.31	2.12	0.02	3.20	1.30	2.12	0.02	3.42	1.35
40	SP1 isustain batt 28v	1.8	2.2	mA	RT	2.12	0.02	3.11	1.22	2.12	0.02	3.08	1.31	2.12	0.02	2.97	1.21
40	SP1 isustain batt 28v	1.8	2.2	mA	CT	2.10	0.03	2.62	1.28	2.09	0.03	2.54	1.39	2.10	0.03	2.18	1.10
41	SP2 isustain batt 28v	1.8	2.2	mA	HT	2.12	0.02	3.52	1.48	2.12	0.02	2.99	1.17	2.12	0.02	3.72	1.46
41	SP2 isustain batt 28v	1.8	2.2	mA	RT	2.12	0.02	3.98	1.53	2.12	0.02	2.90	1.15	2.12	0.02	3.19	1.24
41	SP2 isustain batt 28v	1.8	2.2	mA	CT	2.11	0.02	3.30	1.56	2.10	0.03	2.49	1.24	2.11	0.03	2.31	1.10
42	SP3 isustain batt 28v	1.8	2.2	mA	HT	2.11	0.02	3.08	1.38	2.12	0.02	3.42	1.44	2.12	0.02	3.77	1.63
42	SP3 isustain batt 28v	1.8	2.2	mA	RT	2.12	0.02	3.17	1.32	2.12	0.02	3.54	1.50	2.12	0.02	3.20	1.38
42	SP3 isustain batt 28v	1.8	2.2	mA	CT	2.10	0.03	2.62	1.31	2.10	0.02	2.85	1.51	2.10	0.03	2.34	1.20
43	SP4 isustain batt 28v	1.8	2.2	mA	HT	2.11	0.02	3.08	1.40	2.11	0.02	3.35	1.49	2.12	0.02	3.72	1.60
43	SP4 isustain batt 28v	1.8	2.2	mA	RT	2.11	0.02	3.25	1.43	2.11	0.02	3.42	1.65	2.11	0.02	3.06	1.40
43	SP4 isustain batt 28v	1.8	2.2	mA	CT	2.09	0.02	3.01	1.67	2.08	0.02	2.84	1.76	2.09	0.03	2.24	1.28
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Test#	Test Name	Lo Limit	Hi Limit	Unit	Temp	Mean	Std Dev	Ср	Cpk	Mean	Std Dev	Ср	Cpk	Mean	Std Dev	Ср	Cpk
44	SP5 isustain batt 28v	1.8	2.2	mA	HT	2.11	0.02	3.14	1.41	2.12	0.02	3.40	1.44	2.12	0.02	3.69	1.57
44	SP5 isustain batt 28v	1.8	2.2	mA	RT	2.12	0.02	3.29	1.36	2.12	0.02	3.22	1.40	2.12	0.02	3.24	1.38
44	SP5 isustain batt 28v	1.8	2.2	mA	CT	2.10	0.03	2.60	1.31	2.09	0.02	2.64	1.43	2.10	0.03	2.29	1.17
45	SP6 isustain batt 28v	1.8	2.2	mA	HT	2.12	0.02	3.25	1.38	2.12	0.02	3.43	1.38	2.12	0.02	3.64	1.46
45	SP6 isustain batt 28v	1.8	2.2	mA	RT	2.12	0.02	3.25	1.28	2.12	0.02	3.49	1.41	2.12	0.02	3.02	1.20
45	SP6 isustain batt 28v	1.8	2.2	mA	CT	2.10	0.02	2.76	1.31	2.10	0.02	2.88	1.46	2.11	0.03	2.26	1.09
46	SP7 isustain batt 28v	1.8	2.2	mA	HT	2.11	0.02	3.14	1.51	2.11	0.02	3.58	1.58	2.11	0.02	3.58	1.63
46	SP7 isustain batt 28v	1.8	2.2	mA	RT	2.11	0.02	3.35	1.56	2.11	0.02	3.47	1.61	2.11	0.02	3.10	1.45
46	SP7 isustain batt 28v	1.8	2.2	mA	CT	2.09	0.02	2.73	1.51	2.09	0.02	2.78	1.60	2.09	0.03	2.34	1.31
47	SP0 isustain gnd batt=28v	-2.2	-1.8	mA	HT	-2.01	0.02	4.31	4.15	-2.01	0.02	3.49	3.37	-2.01	0.01	3.90	3.69
47	SP0 isustain gnd batt=28v	-2.2	-1.8	mA	RT	-2.01	0.01	4.65	4.36	-2.01	0.02	39.85	3.30	-2.02	0.02	3.55	3.17
47	SP0 isustain gnd batt=28v	-2.2	-1.8	mA	CT	-1.98	0.02	3.46	3.09	-1.97	0.02	3.16	2.77	-1.98	0.02	3.03	2.81
48	SP1 isustain gnd batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	4.16	4.08	-2.00	0.02	3.42	3.27	-2.01	0.01	4.12	3.81
48	SP1 isustain gnd batt=28v	-2.2	-1.8	mA	RT	-2.01	0.02	3.93	3.71	-2.01	0.02	3.57	3.39	-2.01	0.02	4.27	3.91
48	SP1 isustain gnd batt=28v	-2.2	-1.8	mA	CT	-1.98	0.02	3.04	2.76	-1.97	0.02	3.18	2.72	-1.98	0.02	3.61	3.24
49	SP2 isustain gnd batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	3.77	3.72	-2.00	0.02	3.60	3.47	-2.00	0.01	4.09	3.72
49	SP2 isustain gnd batt=28v	-2.2	-1.8	mA	RT	-2.01	0.02	3.94	3.76	-2.00	0.02	3.81	3.62	-2.01	0.02	4.10	3.84
49	SP2 isustain gnd batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.29	2.92	-1.97	0.02	3.46	2.93	-1.97	0.02	3.42	2.99
50	SP3 isustain gnd batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	3.74	3.72	-2.00	0.02	3.31	3.25	-2.00	0.02	3.54	3.21
50	SP3 isustain gnd batt=28v	-2.2	-1.8	mA	RT	-2.00	0.02	3.89	3.81	-2.00	0.02	3.54	3.46	-2.01	0.02	3.34	3.13
50	SP3 isustain gnd batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.19	2.75	-1.96	0.02	3.03	2.48	-1.97	0.02	2.86	2.49
51	SP4 isustain gnd batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	4.04	4.02	-2.01	0.02	3.50	3.31	-2.00	0.02	3.57	3.23
51	SP4 isustain gnd batt=28v	-2.2	-1.8	mA	RT	-2.00	0.02	4.33	4.24	-2.01	0.02	3.41	3.16	-2.01	0.02	3.59	3.33
51	SP4 isustain gnd batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.45	2.99	-1.97	0.02	3.10	2.72	-1.97	0.02	3.01	2.64
52	SP5 isustain gnd batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	3.97	3.97	-2.00	0.02	3.42	3.34	-2.00	0.02	3.77	3.39
52	SP5 isustain gnd batt=28v	-2.2	-1.8	mA	RT	-2.01	0.02	3.89	3.75	-2.00	0.02	3.98	3.83	-2.01	0.02	3.51	3.29
52	SP5 isustain gnd batt=28v SP6 isustain gnd batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.09	2.72	-1.96	0.02	3.62	3.06	-1.97	0.02	3.04	2.68
53 53	- · · · · · · · · · · · · · · · · · · ·	-2.2 -2.2	-1.8 -1.8	mA mA	HT RT	-2.00 -2.01	0.02 0.02	3.72 4.06	3.68 3.96	-2.00 -2.00	0.02 0.02	3.31 3.35	3.20 3.20	-2.00 -2.00	0.01 0.02	4.10 4.21	3.64 4.01
53	SP6 isustain gnd batt=28v SP6 isustain gnd batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.43	2.99	-1.97	0.02	2.87	2.48	-1.97	0.02	3.24	2.84
54	SP7 isustain gnd batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	3.71	3.70	-2.00	0.02	3.41	3.30	-2.00	0.02	3.86	3.51
54	SP7 isustain gnd batt=28v	-2.2	-1.8	mA	RT	-2.00	0.02	3.68	3.53	-2.00	0.02	3.43	3.26	-2.00	0.01	3.74	3.45
54	SP7 isustain gnd batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.09	2.77	-1.97	0.02	3.02	2.63	-1.98	0.02	3.24	2.94
55	SG0 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.01	0.02	3.58	3.39	-2.01	0.02	3.52	3.26	-2.01	0.02	4.33	4.15
55	SG0 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.01	0.02	3.83	3.56	-2.01	0.02	3.75	3.46	-2.02	0.02	4.14	3.68
55	SG0 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.98	0.02	3.10	2.83	-1.97	0.02	3.46	3.02	-1.98	0.02	3.48	3.20
56	SG1 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.01	0.02	3.63	3.51	-2.01	0.02	3.24	3.05	-2.01	0.01	4.14	3.90
56	SG1 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.01	0.02	3.66	3.48	-2.01	0.02	3.30	3.13	-2.01	0.02	3.96	3.61
56	SG1 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.30	2.93	-1.96	0.02	2.93	2.46	-1.97	0.02	3.23	2.86
57	SG2 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.01	0.02	3.84	3.70	-2.01	0.02	3.27	3.03	-2.01	0.02	3.52	3.35
57	SG2 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.01	0.02	4.10	3.87	-2.01	0.02	3.33	3.07	-2.02	0.02	3.66	3.28
57	SG2 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.25	2.89	-1.97	0.02	2.93	2.54	-1.98	0.02	3.24	2.91
58	SG3 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.01	0.02	3.91	3.78	-2.01	0.02	3.42	3.17	-2.01	0.01	4.37	4.17
58	SG3 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.01	0.02	4.17	3.93	-2.01	0.02	3.48	3.20	-2.02	0.02	4.27	3.79
58	SG3 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.50	3.13	-1.97	0.02	3.05	2.68	-1.98	0.02	3.44	3.15
59	SG4 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.01	0.02	3.96	3.85	-2.01	0.02	3.55	3.29	-2.01	0.01	3.83	3.58
59	SG4 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.01	0.02	4.03	3.79	-2.01	0.02	3.64	3.29	-2.01	0.02	3.78	3.40
59	SG4 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.98	0.02	3.37	3.09	-1.98	0.02	3.17	2.87	-1.98	0.02	3.13	2.85
60	SG5 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	4.04	4.00	-2.00	0.02	3.32	3.20	-2.00	0.01	3.93	3.56
60	SG5 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.00	0.02	4.19	4.10	-2.01	0.02	3.23	3.07	-2.01	0.01	4.42	4.11
60	SG5 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.40	2.96	-1.97	0.02	2.89	2.48	-1.97	0.02	3.71	3.26
61	SG6 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	3.85	3.83	-2.00	0.02	3.35	3.21	-2.01	0.02	3.72	3.41
61	SG6 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.01	0.02	4.08	3.94	-2.01	0.02	3.59	3.38	-2.01	0.02	4.01	3.69
	SG6 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.64	3.21	-1.97	0.02	3.32	2.86	-1.97	0.02	3.42	3.05
62	SG7 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	3.95	3.89	-2.00	0.02	3.54	3.37	-2.01	0.01	4.03	3.72
	SG7 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.01	0.02	4.35	4.11	-2.01	0.02	3.73	3.45	-2.01	0.02	3.83	3.47
	SG7 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.98	0.02	3.43	3.13	-1.97	0.02	3.21	2.85	-1.98	0.02	3.07	2.81
	SG8 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	3.88	3.79	-2.00	0.02	3.47	3.46	-2.00	0.02	3.58	3.15
	SG8 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.00	0.02	4.25	4.17	-2.00	0.02	3.87	3.79	-2.00	0.02	3.36	3.19
63	SG8 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.18	2.73	-1.96	0.02	3.54	2.93	-1.97	0.02	2.75	2.39

							Lo	t1			Lo	t2			Lo	t3	
Test#	Test Name	Lo Limit	Hi Limit	Unit	Temp	Mean	Std Dev	Ср	Cpk	Mean	Std Dev	Ср	Cpk	Mean	Std Dev	Ср	Cpk
64	SG9 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	3.91	3.84	-2.00	0.02	3.78	3.68	-2.00	0.02	3.53	3.15
64	SG9 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.00	0.02	4.13	4.06	-2.00	0.01	4.36	4.14	-2.01	0.02	3.57	3.34
64	SG9 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.47	2.98	-1.97	0.02	3.87	3.34	-1.97	0.02	3.16	2.78
65	SG10 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	4.02	3.96	-2.00	0.02	3.59	3.46	-2.00	0.01	3.82	3.46
65	SG10 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.00	0.02	3.93	3.85	-2.01	0.02	3.58	3.38	-2.01	0.02	3.74	3.42
65	SG10 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.35	2.91	-1.97	0.02	3.12	2.70	-1.98	0.02	3.02	2.71
66	SG11 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	3.96	3.89	-2.00	0.02	3.80	3.67	-2.00	0.01	3.82	3.44
66	SG11 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.00	0.02	4.16	4.09	-2.01	0.02	3.87	3.65	-2.01	0.02	3.95	3.65
66	SG11 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.40	2.94	-1.97	0.02	3.42	2.98	-1.97	0.02	3.22	2.87
67	SG12 sustain current batt=28v	-2.2	-1.8		HT	-2.00	0.02	4.18	4.08	-2.00	0.02		3.57	-2.00	0.02	5.26	3.56
				mA								3.63					
67	SG12 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.00	0.02	4.38	4.31	-2.00	0.02	3.52	3.40	-2.00	0.02	4.23	4.03
67	SG12 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.60	3.12	-1.97	0.02	3.27	2.78	-1.97	0.02	3.46	3.00
68	SG13 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	4.02	3.96	-2.00	0.02	3.53	3.44	-2.00	0.01	3.89	3.47
68	SG13 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.00	0.02	4.35	4.27	-2.00	0.02	3.67	3.52	-2.01	0.02	3.92	3.68
68	SG13 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.57	3.12	-1.97	0.02	3.29	2.80	-1.97	0.02	3.09	2.71
69	IMATCH	-4	4	%	HT	1.33	0.34	3.87	2.59	1.25	0.42	3.17	2.18	1.29	0.25	5.26	3.56
69	IMATCH	-4	4	%	RT	1.55	0.32	4.21	2.58	1.44	0.35	3.76	2.41	1.50	0.32	4.12	2.58
69	IMATCH	-4	4	%	CT	1.85	0.40	3.30	1.77	1.67	0.42	3.17	1.84	1.72	0.35	3.78	2.15
70	SP0 ioffset analog	-2	2	uA	HT	-0.44	0.01	88.68	69.08	-0.44	0.01	103.60	80.99	-0.44	0.01	82.06	63.93
70	SP0 ioffset analog	-2	2	uA	RT	-0.29	0.01	123.72	106.03	-0.29	0.01	98.44	84.32	-0.29	0.01	111.09	95.13
70	SP0 ioffset analog	-2	2	uA	CT	-0.25	0.01	113.05	99.18	-0.24	0.01	115.11	101.13	-0.25	0.01	107.11	93.99
71	SP1 ioffset analog	-2	2	uA	HT	-0.31	0.01	123.04	103.72	-0.31	0.00	152.59	128.91	-0.32	0.01	66.13	35.40
71	SP1 ioffset analog	-2	2	uA	RT	-0.21	0.01	130.71	117.15	-0.21	0.00	183.92	165.05	-0.21	0.01	72.79	65.25
71	SP1 ioffset analog	-2	2	uA	CT	-0.18	0.00	135.27	122.79	-0.18	0.00	175.86	159.81	-0.18	0.00	168.34	152.84
72	SP2 ioffset analog	-2	2	uA	HT	-0.31	0.00	134.72	113.84	-0.31	0.01	118.55	100.43	-0.31	0.01	71.87	38.14
72	SP2 ioffset analog	-2	2	uA	RT	-0.20	0.00	157.16	141.08	-0.20	0.01	129.78	116.52	-0.21	0.01	131.23	117.73
72	SP2 ioffset analog	-2	2	uA	CT	-0.18	0.00	146.38	132.85	-0.18	0.00	149.73	136.03	-0.18	0.00	139.21	126.35
73	SP3 ioffset analog	-2	2	uA	HT	-0.09	0.00	146.01	139.53	-0.09	0.00	155.46	148.77	-0.09	0.00	81.17	27.51
73	SP3 ioffset analog	-2	2	uA	RT	-0.05	0.00	537.09	523.85	-0.05	0.00	522.48	509.94	-0.05	0.00	600.37	585.62
73	SP3 ioffset analog	-2	2	uA	CT	-0.06	0.00	417.62	404.84	-0.06	0.00	427.48	414.77	-0.06	0.00	509.56	494.40
74	SP4 ioffset analog	-2	2	uA	HT	-0.42	0.01	110.14	86.98	-0.42	0.01	103.10	81.59	-0.42	0.01	49.52	31.18
74	SP4 ioffset analog	-2	2	uA	RT	-0.28	0.00	141.56	121.80	-0.28	0.01	96.87	83.48	-0.28	0.00	138.13	118.85
74	SP4 ioffset analog	-2	2	uA	CT	-0.24	0.01	129.03	113.65	-0.24	0.01	121.31	106.91	-0.24	0.01	117.10	103.11
75	SP5 ioffset analog	-2	2	uA	HT	-0.43	0.01	65.77	51.71	-0.43	0.01	73.39	57.76	-0.43	0.01	48.90	30.93
75	SP5 ioffset analog	-2	2	uA	RT	-0.49	0.01	95.46	81.73	-0.29	0.01	93.91	80.50	-0.29	0.01	79.77	68.37
75	SP5 ioffset analog	-2	2	uA	CT	-0.24	0.01	100.54	88.24	-0.24	0.01	123.96	108.89	-0.24	0.01	81.45	71.47
76	SP6 ioffset analog	-2	2	uA	HT	-0.42	0.01	64.91	51.21	-0.42	0.01	69.50	54.90	-0.42	0.01	39.99	25.20
76	SP6 ioffset analog	-2	2	uA	RT	-0.42	0.01	87.97	75.56	-0.42	0.01	85.05	73.11	-0.42	0.01	92.47	79.54
76	SP6 ioffset analog	-2	2	uA	CT	-0.24	0.01	115.48	101.62	-0.24	0.01	102.84	90.56	-0.24	0.01	102.22	90.00
77	SP7 ioffset analog	-2	2	uA	HT	-0.42	0.01	57.82	45.63	-0.42	0.01	73.39	58.12	-0.42	0.01	42.97	27.00
77	SP7 ioffset analog	-2	2	uA	RT	-0.42	0.01	104.54	89.84	-0.42	0.01	91.01	78.27	-0.42	0.01	112.12	96.32
77	SP7 ioffset analog	-2	2	uA	CT	-0.24	0.01	88.94	78.21	-0.24	0.01	104.24	91.88	-0.24	0.01	94.54	83.19
78	ū	-2	2	uA	HT	-0.24	0.01	95.10	75.42	-0.24	0.01	80.79	64.15	-0.42	0.01	48.16	29.96
78	SG0 ioffset analog				RT					-0.41			123.37				
	SG0 ioffset analog	-2	2	uA 		-0.27	0.01	124.41	107.45		0.00	142.81		-0.27	0.01	116.73	100.81
78	SG0 ioffset analog	-2	2	uA 	CT	-0.23	0.01	98.12	86.74	-0.23	0.01	129.97	114.81	-0.23	0.01	107.64	95.06
79	SG1 ioffset analog	-2	2	uA	HT	-0.28	0.00	168.94	145.36	-0.28	0.00	141.19	121.63	-0.28	0.00	104.89	52.97
79	SG1 ioffset analog	-2	2	uA	RT	-0.18	0.00	180.63	164.08	-0.18	0.00	189.65	172.59	-0.18	0.00	205.34	186.59
79	SG1 ioffset analog	-2	2	uA	CT	-0.16	0.00	196.03	179.87	-0.16	0.00	169.67	155.80	-0.17	0.00	173.15	158.83
80	SG2 ioffset analog	-2	2	uA	HT	-0.42	0.01	79.06	62.40	-0.42	0.01	72.78	57.52	-0.43	0.01	38.84	24.51
80	SG2 ioffset analog	-2	2	uA	RT	-0.28	0.01	131.33	113.21	-0.27	0.01	92.09	79.45	-0.28	0.00	134.41	115.83
80	SG2 ioffset analog	-2	2	uA	CT	-0.23	0.01	108.20	95.57	-0.23	0.01	87.97	77.70	-0.23	0.01	116.10	102.50
81	SG3 ioffset analog	-2	2	uA	HT	-0.31	0.01	123.64	104.61	-0.30	0.01	123.93	105.06	-0.31	0.00	88.43	46.93
81	SG3 ioffset analog	-2	2	uA	RT	-0.20	0.00	146.94	132.13	-0.20	0.00	152.90	137.65	-0.20	0.01	133.04	119.60
81	SG3 ioffset analog	-2	2	uA	CT	-0.18	0.00	149.23	135.74	-0.18	0.00	160.27	145.98	-0.18	0.00	162.83	148.18
82	SG4 ioffset analog	-2	2	uA	HT	-0.42	0.01	105.67	83.56	-0.42	0.01	77.30	61.17	-0.42	0.01	68.71	43.12
82	SG4 ioffset analog	-2	2	uA	RT	-0.28	0.01	113.17	97.57	-0.27	0.02	29.94	25.91	-0.28	0.01	117.37	101.07
82	SG4 ioffset analog	-2	2	uA	CT	-0.23	0.01	116.50	102.86	-0.23	0.01	82.62	73.00	-0.24	0.01	118.29	104.30
83	SG5 ioffset analog	-2	2	uA	HT	-0.41	0.01	87.41	69.63	-0.40	0.01	79.81	63.70	-0.41	0.01	58.82	36.12
83	SG5 ioffset analog	-2	2	uA	RT	-0.27	0.01	129.13	111.92	-0.26	0.01	117.60	102.07	-0.26	0.01	103.85	90.16
83	SG5 ioffset analog	-2	2	uA	CT	-0.23	0.01	107.71	95.45	-0.23	0.01	107.25	95.14	-0.23	0.01	104.52	92.68
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							10	t1			I o	t2			Ic	t3	
Test#	Test Name	Lo Limit	Hi Limit	Unit	Temp	Mean	Std Dev	Ср	Cpk	Mean	Std Dev	Cp	Cpk	Mean	Std Dev	Ср	Cpk
84	SG6 ioffset analog	-2	2	uA	HT	-0.41	0.01	70.33	55.96	-0.41	0.01	85.94	68.37	-0.41	0.01	38.43	23.81
84	SG6 ioffset analog	-2	2	uA	RT	-0.41	0.01	114.62	99.38	-0.41	0.01	83.49	72.34	-0.41	0.01	89.95	77.81
84	SG6 ioffset analog	-2	2	uA	CT	-0.27	0.01	124.88	110.55	-0.27	0.01	96.68	85.54	-0.27	0.01	92.87	82.03
85	SG7 ioffset analog	-2	2	uA	HT	-0.23	0.01	63.30	50.36	-0.23	0.01		55.49	-0.23	0.01	39.39	24.36
		-2			RT	-0.41		91.06	78.81	-0.40	0.01	69.55 99.10	85.80	-0.41	0.01	93.75	81.08
85	SG7 ioffset analog		2	uA 			0.01										
85	SG7 ioffset analog	-2	2	uA	CT	-0.23	0.01	95.76	84.68	-0.23	0.01	93.43	82.71	-0.23	0.01	88.29	78.11
86	SG8 ioffset analog	-2	2	uA	HT	-0.42	0.01	105.01	83.07	-0.42	0.01	98.82	78.27	-0.42	0.01	55.26	34.66
86	SG8 ioffset analog	-2	2	uA	RT	-0.27	0.01	70.43	60.75	-0.28	0.01	109.85	94.69	-0.28	0.01	125.21	107.72
86	SG8 ioffset analog	-2	2	uA	CT	-0.24	0.01	115.88	102.15	-0.24	0.01	108.25	95.48	-0.24	0.00	144.55	127.46
87	SG9 ioffset analog	-2	2	uA	HT	-0.41	0.01	67.83	53.76	-0.41	0.01	91.31	72.60	-0.42	0.01	58.61	36.51
87	SG9 ioffset analog	-2	2	uA	RT	-0.27	0.02	28.08	24.30	-0.27	0.01	54.23	46.90	-0.28	0.01	96.66	83.30
87	SG9 ioffset analog	-2	2	uA	CT	-0.24	0.01	99.68	87.96	-0.23	0.01	130.44	115.36	-0.24	0.01	122.57	108.12
88	SG10 ioffset analog	-2	2	uA	HT	-0.42	0.01	75.45	59.63	-0.42	0.01	99.06	78.30	-0.42	0.01	51.06	32.16
88	SG10 ioffset analog	-2	2	uA	RT	-0.27	0.03	26.64	23.03	-0.28	0.01	57.74	49.76	-0.28	0.01	103.20	88.72
88	SG10 ioffset analog	-2	2	uA	CT	-0.24	0.01	100.45	88.51	-0.24	0.00	137.04	120.71	-0.24	0.01	98.99	87.04
89	SG11 ioffset analog	-2	2	uA	HT	-0.43	0.01	64.70	50.65	-0.43	0.01	67.36	52.81	-0.44	0.01	38.90	24.94
89	SG11 ioffset analog	-2	2	uA	RT	-0.29	0.01	85.96	73.60	-0.29	0.02	42.07	36.04	-0.29	0.01	72.75	62.10
89	SG11 ioffset analog	-2	2	uA	CT	-0.25	0.01	94.68	83.03	-0.25	0.01	94.28	82.68	-0.25	0.01	76.68	67.16
90	SG12 ioffset analog	-2	2	uA	HT	-0.43	0.01	84.90	66.68	-0.43	0.01	95.95	75.48	-0.43	0.01	51.84	33.05
90	SG12 ioffset analog	-2	2	uA	RT	-0.28	0.01	105.40	90.41	-0.28	0.01	118.30	101.51	-0.29	0.01	108.35	92.91
90	SG12 ioffset analog	-2	2	uA	CT	-0.24	0.01	108.48	95.29	-0.24	0.01	121.22	106.46	-0.24	0.01	118.05	103.60
91	SG13 ioffset analog	-2	2	uA	HT	-0.43	0.01	85.38	67.20	-0.42	0.01	67.95	53.58	-0.43	0.01	71.81	56.43
91	SG13 ioffset analog	-2	2	uA	RT	-0.28	0.01	85.70	73.62	-0.28	0.01	96.24	82.62	-0.28	0.01	94.91	81.58
91	SG13 ioffset analog	-2	2	uA	CT	-0.24	0.01	96.56	84.93	-0.24	0.01	101.51	89.39	-0.24	0.01	85.90	75.59
92	Sp0 output offset voltage	-10	10	mV	HT	2.41	0.27	12.52	9.51	2.46	0.34	9.85	7.43	2.42	0.38	8.68	6.58
92	Sp0 output offset voltage	-10	10	mV	RT	1.16	0.27	12.31	10.87	1.23	0.25	13.37	11.72	1.24	0.33	10.25	8.99
92	Sp0 output offset voltage	-10	10	mV	CT	0.59	0.31	10.78	10.15	0.53	0.31	10.62	10.05	0.66	0.36	9.19	8.59
93	Sp1 output offset voltage	-10	10	mV	HT	2.64	0.27	12.56	9.24	2.72	0.32	10.49	7.63	2.69	0.33	10.24	7.49
93	Sp1 output offset voltage	-10	10	mV	RT	1.39	0.24	11.98	8.19	1.45	0.23	14.35	12.28	1.45	0.33	10.17	8.70
93	Sp1 output offset voltage	-10	10	mV	CT	0.82	0.29	11.46	10.52	0.84	0.27	12.54	11.49	0.93	0.33	10.09	9.15
94	Sp2 output offset voltage	-10	10	mV	HT	2.04	0.28	12.09	9.62	2.08	0.30	11.07	8.76	2.09	0.35	9.44	7.46
94	Sp2 output offset voltage	-10	10	mV	RT	0.90	0.26	11.16	8.26	0.94	0.26	12.98	11.76	0.98	0.30	11.14	10.05
94	Sp2 output offset voltage	-10	10	mV	CT	0.33	0.37	9.01	8.71	0.34	0.34	9.76	9.43	0.39	0.39	8.52	8.18
95	Sp3 output offset voltage	-10	10	mV	HT	2.15	0.25	13.10	10.28	2.21	0.32	10.51	8.18	2.18	0.32	10.41	8.14
95	Sp3 output offset voltage	-10	10	mV	RT	0.93	0.23	12.32	9.07	0.95	0.21	15.85	14.34	0.96	0.32	10.34	9.35
95	Sp3 output offset voltage	-10	10	mV	CT	0.28	0.36	9.36	9.10	0.33	0.30	11.11	10.74	0.34	0.39	8.65	8.35
96	Sp4 output offset voltage	-10	10	mV	HT	1.70	0.32	10.43	8.65	1.79	0.35	9.65	7.92	1.75	0.37	8.93	7.36
96	Sp4 output offset voltage	-10	10	mV	RT	0.46	0.26	10.90	8.62	0.52	0.25	13.21	12.53	0.51	0.35	9.54	9.06
96	Sp4 output offset voltage	-10	10	mV	CT	-0.21	0.37	9.08	8.89	-0.19	0.37	9.13	8.96	-0.14	0.42	8.00	7.89
97	Sp5 output offset voltage	-10	10	mV	HT	1.57	0.26	12.75	10.75	1.61	0.35	9.61	8.06	1.65	0.33	10.13	8.46
97	Sp5 output offset voltage	-10	10	mV	RT	0.28	0.25	11.53	9.35	0.32	0.28	11.83	11.46	0.34	0.34	9.85	9.51
97	Sp5 output offset voltage	-10	10	mV	CT	-0.45	0.37	9.11	8.70	-0.40	0.37	9.06	8.69	-0.36	0.42	8.02	7.73
98	Sp6 output offset voltage	-10	10	mV	HT	1.83	0.26	13.07	10.67	1.91	0.31	10.66	8.63	1.84	0.33	10.18	8.31
98	Sp6 output offset voltage	-10	10	mV	RT	0.60	0.25	11.75	9.09	0.62	0.29	11.54	10.82	0.59	0.36	9.17	8.63
98	Sp6 output offset voltage	-10	10	mV	CT	-0.13	0.37	8.97	8.85	-0.05	0.34	9.88	9.83	-0.05	0.43	7.80	7.76
99	Sp7 output offset voltage	-10	10	mV	HT	1.75	0.26	12.95	10.68	1.79	0.32	10.29	8.45	1.78	0.36	9.33	7.66
99	Sp7 output offset voltage	-10	10	mV	RT	0.62	0.30	9.60	7.42	0.65	0.27	12.51	11.70	0.64	0.32	10.32	9.67
99	Sp7 output offset voltage	-10	10	mV	CT	0.00	0.37	9.07	9.06	-0.02	0.36	9.17	9.15	0.10	0.46	7.33	7.25
100	Sg0 output offset voltage	-10	10	mV	HT	0.03	0.11	29.51	29.44	0.03	0.12	27.67	27.58	0.03	0.13	25.50	25.43
100	Sg0 output offset voltage	-10	10	mV	RT	-0.01	0.14	20.43	17.27	-0.02	0.13	24.93	24.89	-0.01	0.14	23.37	23.34
100	Sg0 output offset voltage	-10	10	mV	CT	0.04	0.17	19.67	19.59	0.02	0.12	28.11	28.06	0.01	0.13	25.15	25.13
101	Sg1 output offset voltage	-10	10	mV	HT	2.15	0.27	12.54	9.84	2.16	0.29	11.32	8.88	2.17	0.30	11.06	8.67
101	Sg1 output offset voltage	-10	10	mV	RT	0.90	0.24	12.09	8.95	0.95	0.24	14.13	12.78	0.94	0.31	10.60	9.61
101	Sg1 output offset voltage	-10	10	mV	CT	0.22	0.35	9.47	9.27	0.31	0.32	10.38	10.06	0.33	0.39	8.58	8.30
102	Sg2 output offset voltage	-10	10	mV	HT	2.60	0.28	12.11	8.96	2.64	0.31	10.90	8.02	2.62	0.33	10.05	7.41
102	Sg2 output offset voltage	-10	10	mV	RT	1.34	0.27	10.88	7.49	1.38	0.27	12.20	10.52	1.42	0.30	11.11	9.53
102	Sg2 output offset voltage	-10	10	mV	CT	0.72	0.29	11.34	10.53	0.75	0.35	9.59	8.88	0.79	0.41	8.16	7.51
103	Sg3 output offset voltage	-10	10	mV	HT	2.63	0.24	13.84	10.19	2.68	0.31	10.74	7.87	2.65	0.33	10.21	7.51
103	Sg3 output offset voltage	-10	10	mV	RT	1.47	0.23	12.51	8.42	1.48	0.22	14.86	12.66	1.48	0.30	11.30	9.63
103	Sg3 output offset voltage	-10	10	mV	CT	0.94	0.26	12.66	11.48	0.97	0.27	12.53	11.32	0.99	0.32	10.40	9.37
	1030 output officer voltage	10	.0	1.11	٥,	0.07	0.20	12.00	11.70	0.01	V.Z1	12.00	11.02	0.00	0.02	10.70	0.01

							Lo	t1			Lo	t2			Lo	t3	
Test#	Test Name	Lo Limit	Hi Limit	Unit	Temp	Mean	Std Dev	Ср	Cpk	Mean	Std Dev	Ср	Cpk	Mean	Std Dev	Ср	Cpk
104	Sg4 output offset voltage	-10	10	mV	HT	2.40	0.30	11.02	8.37	2.48	0.34	9.76	7.34	2.44	0.37	9.06	6.85
104	Sg4 output offset voltage	-10	10	mV	RT	1.20	0.31	9.27	6.54	1.25	0.27	12.31	10.77	1.25	0.35	9.55	8.36
104	Sg4 output offset voltage	-10	10	mV	CT	0.64	0.30	11.09	10.38	0.69	0.30	10.94	10.18	0.69	0.38	8.73	8.13
105	Sg5 output offset voltage	-10	10	mV	HT	0.04	0.16	21.41	21.33	-0.03	0.16	21.40	21.34	0.02	0.12	27.77	27.73
105	Sg5 output offset voltage	-10	10	mV	RT	0.02	0.13	21.71	18.28	0.02	0.13	25.60	25.55	0.01	0.11	29.74	29.70
105	Sg5 output offset voltage	-10	10	mV	CT	0.05	0.14	23.88	23.77	0.06	0.15	21.80	21.66	0.04	0.16	21.47	21.38
106	Sg6 output offset voltage	-10	10	mV	HT	0.02	0.14	24.66	24.63	0.05	0.13	25.37	25.25	0.02	0.13	25.52	25.48
106	Sg6 output offset voltage	-10	10	mV	RT	0.02	0.13	21.70	18.26	0.00	0.13	25.84	25.84	0.07	0.14	23.27	23.10
106	Sg6 output offset voltage	-10	10	mV	CT	0.03	0.14	23.89	23.82	0.04	0.17	19.18	19.09	0.05	0.15	22.94	22.84
107	Sg7 output offset voltage	-10	10	mV	HT	1.71	0.27	12.38	10.26	1.79	0.33	9.98	8.20	1.75	0.35	9.59	7.91
107	Sg7 output offset voltage	-10	10	mV	RT	0.49	0.22	13.13	10.34	0.53	0.26	13.00	12.32	0.53	0.31	10.87	10.29
107	Sg7 output offset voltage	-10	10	mV	CT	-0.23	0.33	10.03	9.80	-0.19	0.34	9.76	9.57	-0.20	0.46	7.30	7.16
108	Sg8 output offset voltage	-10	10	mV	HT	1.79	0.29	11.31	9.29	1.80	0.32	10.28	8.43	1.78	0.33	9.95	8.19
108	Sg8 output offset voltage	-10	10	mV	RT	0.55	0.28	10.36	8.09	0.57	0.26	12.80	12.07	0.56	0.31	10.80	10.19
108	Sg8 output offset voltage	-10	10	mV	CT	-0.19	0.37	8.91	8.75	-0.08	0.39	8.56	8.49	-0.07	0.40	8.37	8.31
109	Sg9 output offset voltage	-10	10	mV	HT	1.80	0.32	10.52	8.63	1.83	0.32	10.31	8.42	1.84	0.36	9.26	7.56
109	Sg9 output offset voltage	-10	10	mV	RT	0.60	0.29	10.00	7.75	0.61	0.28	11.99	11.25	0.60	0.31	10.67	10.03
109	Sg9 output offset voltage	-10	10	mV	CT	-0.18	0.38	8.82	8.66	-0.18	0.38	8.68	8.52	-0.11	0.45	7.33	7.25
110	Sg10 output offset voltage	-10	10	mV	HT	1.84	0.31	10.86	8.87	1.81	0.33	10.08	8.26	1.85	0.33	10.05	8.19
110	Sg10 output offset voltage	-10	10	mV	RT	0.52	0.24	11.98	9.39	0.55	0.26	12.65	11.96	0.52	0.32	10.55	10.00
110	Sg10 output offset voltage	-10	10	mV	CT	-0.22	0.37	8.91	8.71	-0.17	0.38	8.85	8.70	-0.18	0.43	7.69	7.56
111	Sg11 output offset voltage	-10	10 10	mV	HT	1.83	0.31	10.87	8.88	1.86	0.30	11.11	9.04	1.88	0.35	9.41	7.65
111	Sg11 output offset voltage	-10 -10	10	mV	RT	0.58	0.28	10.12	7.86	0.61	0.23	14.43	13.54	0.63	0.29	11.35	10.63
111	Sg11 output offset voltage	-10 -10	10	mV	CT HT	-0.08	0.32	10.27	10.19 9.11	-0.09	0.38	8.78	8.70	-0.06	0.47 0.37	7.04 9.09	6.99
112 112	Sg112 output offset voltage Sg112 output offset voltage	-10 -10	10	mV mV	RT	1.83 0.51	0.30 0.30	11.14 9.52	7.47	1.85 0.56	0.35 0.29	9.56 11.51	7.79 10.87	1.85 0.50	0.37	10.01	7.41 9.51
112	Sg112 output offset voltage	-10 -10	10	mV	CT	-0.23	0.35	9.52	9.21	-0.18	0.29	9.91	9.73	-0.08	0.33	7.71	7.64
113	Sg13 output offset voltage	-10	10	mV	HT	1.75	0.33	12.33	10.17	1.80	0.34	10.77	8.83	1.77	0.43	9.11	7.49
113	Sq13 output offset voltage	-10	10	mV	RT	0.60	0.27	11.72	9.08	0.63	0.31	11.97	11.22	0.65	0.37	10.21	9.55
113	Sg13 output offset voltage	-10	10	mV	CT	-0.11	0.25	9.21	9.11	-0.10	0.39	8.53	8.45	-0.10	0.33	8.02	7.94
114	AMUX vol	-30	30	mV	HT	8.20	0.30	65.57	47.64	8.18	0.13	39.87	21.74	8.16	0.42	26.61	14.47
114	AMUX vol	-30	30	mV	RT	6.78	0.10	48.65	21.98	6.84	0.10	50.08	22.83	6.60	0.10	48.28	21.24
114	AMUX vol	-30	30	mV	CT	5.75	0.12	43.09	16.52	5.53	0.13	38.63	14.25	5.89	0.12	42.90	16.85
115	AMUX voh	4.9	5.1	V	HT	4.93	0.00	35.05	9.64	4.93	0.00	44.04	11.96	4.93	0.00	32.07	8.76
115	AMUX voh	4.9	5.1	V	RT	4.95	0.00	96.77	44.98	4.95	0.00	96.52	44.62	4.95	0.00	108.04	50.11
115	AMUX voh	4.9	5.1	V	CT	4.96	0.00	80.87	46.49	4.96	0.00	132.85	76.20	4.96	0.00	69.36	39.84
116	Sp0 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
116	Sp0 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
116	Sp0 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
117	Sp1 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
117	Sp1 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
117	Sp1 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
118	Sp2 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
118	Sp2 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
118	Sp2 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
119	Sp3 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
119	Sp3 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
119	Sp3 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
	Sp4 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		1
	Sp4 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
	Sp4 Vth				CT	1.00	0.00			1.00	0.00			1.00	0.00		<del> </del>
	Sp5 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
	Sp5 Vth Sp5 Vth	1			RT CT	1.00	0.00			1.00	0.00			1.00 1.00	0.00		-
121 122	Sp6 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		-
122	Sp6 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
122	Sp6 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
	Sp7 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
	Sp7 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
	Sp7 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		<del> </del>
.20	Op. 701	1			<b>0</b> 1	1.00				1.00	0.00		<u> </u>	1.00	0.00		ı

							Lo	t1			Lo	ot2	1		Lo	ot3	
Test#	Test Name	Lo Limit	Hi Limit	Unit	Temp	Mean	Std Dev	Ср	Cpk	Mean	Std Dev	Ср	Cpk	Mean	Std Dev	Ср	Cpk
124	Sg0 Vth	1			HT	1.00	0.00		op.t	1.00	0.00	- 06	op	1.00	0.00	- Op	- Op.:
124	Sg0 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
124	Sg0 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
125	Sg1 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
125	Sg1 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
125	Sg1 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
126	Sg2 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
126	Sg2 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
126	Sg2 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
127		1			HT	1.00	0.00			1.00	0.00			1.00	0.00		-
	Sg3 Vth	1															
127	Sg3 Vth				RT	1.00	0.00			1.00	0.00			1.00	0.00		
127	Sg3 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
128	Sg4 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
128	Sg4 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
128	Sg4 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
129	Sg5 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
129	Sg5 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
129	Sg5 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
130	Sg6 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
130	Sg6 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
130	Sg6 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
131	Sg7 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
131	Sg7 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
131	Sg7 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
132	Sg8 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
132	Sg8 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
132	Sg8 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
133	Sg9 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
133	Sg9 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
133	Sg9 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
134	Sg10 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
134	Sg10 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
134	Sg10 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
135	Sg11 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
135	Sg11 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		1
135	Sg11 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
136	Sg12 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
136	Sg12 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
136	Sg12 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
137	Sg13 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
137	•	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		-
137	Sg13 Vth Sg13 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		+
169	•	-10	10	uA	HT	0.00	0.00	3905.33	3903.57	0.00	0.00	4020.88	4019.16	0.00	0.00	799.16	762.85
	SCLK to VDDQ lkg										1						
169	SCLK to VDDQ lkg	-10 10	10	uA ^	RT	0.00	0.00	3319.62	3319.11	0.00	0.00	3890.78	3890.18	0.00	0.00	3817.19	3816.69
169	SCLK to VDDQ lkg	-10	10	uA 	CT	0.00	0.00	5126.08	5125.22	0.00	0.00	4181.85	4181.20	0.00	0.00	4778.82	4778.13
170	SI to VDDQ lkg	-10	10	uA	HT	0.01	0.00	4617.66	4613.52	0.01	0.00	4399.03	4395.14	0.01	0.00	743.35	710.90
170	SI to VDDQ lkg	-10	10	uA	RT	0.00	0.00	2779.66	2778.73	0.00	0.00	2774.13	2773.29	0.00	0.00	3021.26	3020.33
170	SI to VDDQ lkg	-10	10	uA	CT	0.00	0.00	3562.81	3561.80	0.00	0.00	2800.15	2799.34	0.00	0.00	2884.98	2884.17
171	SO to VDDQ lkg	-10	10	uA	HT	0.01	0.00	4029.42	4025.56	0.01	0.00	4950.42	4945.67	0.01	0.00	840.84	804.47
171	SO to VDDQ lkg	-10	10	uA	RT	0.00	0.00	4113.93		0.00	0.00	3888.17		0.00	0.00	3655.81	3654.16
171	SO to VDDQ lkg	-10	10	uA	CT	0.00	0.00	3420.58	3419.29	0.00	0.00	2957.33	2956.19	0.00	0.00	3696.07	3694.45
172	SCLK to GND lkg	-10	10	uA	HT	-0.01	0.00	4610.94	4607.81	-0.01	0.00	4056.92	4054.19	-0.01	0.00	844.09	801.26
172	SCLK to GND lkg	-10	10	uA	RT	0.00	0.00	3771.43	3771.12	0.00	0.00	3037.48	3037.30	0.00	0.00	2983.93	2983.66
172	SCLK to GND lkg	-10	10	uA	CT	0.00	0.00	3473.57	3473.32	0.00	0.00	3931.77	3931.58	0.00	0.00	3477.99	3477.70
173	SI to GND lkg	-10	10	uA	HT	0.00	0.00	4553.59	4551.41	0.00	0.00	4449.75	4447.75	0.00	0.00	1016.97	970.62
173	SI to GND lkg	-10	10	uA	RT	0.00	0.00	4036.84	4035.06	0.00	0.00	4318.07	4316.31	0.00	0.00	4343.79	4341.82
173	SI to GND lkg	-10	10	uA	CT	0.00	0.00	3832.37	3830.91	0.00	0.00	3901.58	3900.12	0.00	0.00	5010.25	5008.26
174	SO to GND lkg	-10	10	uA	HT	0.00	0.00	5584.12	5581.58	0.00	0.00	4359.68	4357.77	0.00	0.00	1027.52	980.49
174	SO to GND lkg	-10	10	uA	RT	0.00	0.00	4659.42	4657.42	0.00	0.00	4814.58	4812.50	0.00	0.00	3815.81	3814.11
174	SO to GND lkg	-10	10	uA	CT	0.00	0.00	3815.67	3814.29	0.00	0.00	4360.30	4358.62	0.00	0.00	3727.76	3726.24
	<u> </u>						noolo Confi			•							

Test   Test   Parte								Lo	ot1			Lo	t2			Lo	t3	
175   SSS   Input current vol-9-by   1-6   19	Test#	Test Name	Lo Limit	Hi I imit	Unit	Temn	Mean			Cnk	Mean			Cnk	Mean			Cnk
175   CSB Ingal current cod-of-																		
177   CSS   Ingel Current vertice    -10																		
176   CSB pullup current																		
176   CSS pellus current																		
177   SC   graft up current   100   30   LA   CT   51.47   1.92   6.99   3.74   2.95   5.00   3.95   2.74   2.99   0.00   1.97   7.39   4.61   7.75   7.39   4.61   7.75   7.39   4.61   7.75   7.39   4.61   7.75   7.39   4.61   7.75   7.39   4.61   7.75   7.39   7.75   7.39   7.75   7.39   7.75   7.39   7.75   7.39   7.75																		
177   S. Figh State output voltage   4.8   6   V   Fif   4.98   0.00   38-88   20-96   4.99   0.00   43-87   27-71   4.99   0.00   34-16   20-77   27-77   5.01   36-88   0.00   48-78   27-71   4.99   0.00   34-16   27-71   37-78																		
177   SO High State output outsings																		
177   SO Tright State Configure   48   5																		
178   SO low state voltage																		
178   178   178   179					•													
178   So low talex youtgag					mV													
NTB puls-gournerd					mV		63.94	0.27	43.09			0.38		29.30		0.32		
NTS pulsp current	178	SO low state voltage	-400	400	mV	CT	59.38	0.36	184.29	54.71	58.36	0.50	28.59	28.01	59.67	0.43	154.02	45.96
NTB pul-up current	179	INTB pull-up current	-100	-15	uA	HT	-25.01	0.57	24.71	5.82	-24.90	0.53	10.96	5.61	-24.79	0.62	9.63	5.27
NTB pulse current	179	INTB pull-up current	-100	-15	uA	RT	-42.36	0.87	16.30	10.49	-42.29	0.89	14.91	8.31	-42.10	0.95	14.05	7.76
HTG open	179	INTB pull-up current	-100	-15	uA					8.02	-63.84	1.32	10.11	9.14				7.90
NTB copen																		
NTB coen																		
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INTERVIDENCE   The Providence   The Pr		·																
181 NTB voltage@tima																		
182   WAKEB pul-up current		ů ů																
192   WAKEB pullup current																		
193 WAKEB pulsey current																		
183   WAKEB voltage(open)																		
183   WAKEB voltage(open)																		
183   WAKEB voltage ma load		0 1 1 /																
184   WAKEB voltage final bad																		
184   WAKEB voltage Ima load		WAKEB voltage(open)			V		4.60	0.01	12.09		4.61	0.02	9.47	8.77	4.60	0.01	14.35	13.35
144   WAKER voltage fmalload	184	WAKEB voltage 1ma load	-400	400	mV	HT	314.02	1.67	39.80	17.11	312.61	1.93	25.91	15.09	314.39	2.05	15.48	9.06
186   SPO wetting current pulse   15   20   ms   HT   18.88   0.03   25.19   11.27   18.87   0.04   22.67   10.25   18.88   0.04   20.32   9.10	184	WAKEB voltage 1ma load	-400	400	mV	RT	279.13	1.57	15.37	9.72	277.15	1.70	39.19	24.07	278.76	1.75	38.20	23.16
186   SPO wetting current pulse   15   20 ms   RT   18.92   0.04   21.95   9.44   18.93   0.03   22.43   9.86   18.90   0.04   21.79   9.56   186   SPO wetting current pulse   15   20 ms   RT   18.92   0.04   21.95   9.44   18.93   0.03   22.43   10.62   18.93   0.05   12.89   7.95   187   SP1 wetting current pulse   15   20 ms   RT   17.24   0.03   25.31   22.88   17.25   0.04   21.80   19.62   17.25   0.04   19.54   17.86   187   SP1 wetting current pulse   15   20 ms   RT   17.24   0.03   25.31   22.88   17.24   0.03   16.87   17.25   0.04   19.54   17.85   187   SP1 wetting current pulse   15   20 ms   RT   17.24   0.04   20.43   18.34   17.26   0.04   21.28   19.21   17.25   0.04   16.47   6.87   188   SP2 wetting current pulse   15   20 ms   RT   17.26   0.04   21.02   15.93   17.27   0.03   16.82   7.21   17.25   0.04   16.47   6.87   188   SP2 wetting current pulse   15   20 ms   RT   17.26   0.04   21.02   15.93   17.27   0.03   16.82   7.21   17.25   0.04   22.57   20.51   18.85   SP2 wetting current pulse   15   20 ms   RT   17.26   0.04   21.02   15.93   17.27   0.03   16.82   7.21   17.28   0.04   22.57   20.51   18.95   18.95   19.9	184	WAKEB voltage 1ma load	-400	400	mV	CT	257.93	1.79	11.61	8.74	256.19	1.72	12.14	9.48	258.38	1.94	34.32	24.30
186   SPO wetting current pulse   15   20 ms	186	SP0 wetting current pulse	15	20	ms	HT	18.88	0.03	25.19	11.27	18.87	0.04	22.67	10.25	18.88	0.04	20.32	9.10
187   SPT wetting current pulse   15   20   ms   RT   17.23   0.03   27.19   24.29   17.25   0.04   21.80   19.62   17.25   0.04   19.54   17.58   187   SPT wetting current pulse   15   20   ms   RT   17.24   0.03   25.31   22.88   17.24   0.03   16.67   6.88   17.24   0.03   25.37   22.88   17.24   0.04   21.80   19.62   17.25   0.04   16.47   6.87   188   SPZ wetting current pulse   15   20   ms   RT   17.25   0.04   21.34   17.26   0.03   25.77   23.32   17.27   0.04   22.57   20.51   188   SPZ wetting current pulse   15   20   ms   RT   17.25   0.04   21.25   20.41   17.26   0.03   25.77   23.32   17.27   0.04   22.57   20.51   188   SPZ wetting current pulse   15   20   ms   RT   17.25   0.04   21.20   18.93   17.27   0.03   16.82   7.21   17.26   0.04   22.137   19.35   188   SPZ wetting current pulse   15   20   ms   RT   17.25   0.04   21.02   18.93   17.27   0.03   16.82   7.21   17.26   0.04   21.37   19.35   188   SPZ wetting current pulse   15   20   ms   RT   17.25   0.05   17.89   16.12   17.25   0.04   20.65   18.57   17.24   0.04   20.76   18.95   189   SPZ wetting current pulse   15   20   ms   RT   17.25   0.04   20.94   18.85   17.25   0.04   20.65   18.77   17.24   0.04   20.76   18.95   1	186	SP0 wetting current pulse	15	20	ms	RT	18.89	0.04	20.50	9.09	18.90	0.04	22.43	9.86	18.90	0.04	21.79	9.56
187   SPT wetting current pulse   15   20   ms   RT   17.23   0.03   27.19   24.29   17.25   0.04   21.80   19.62   17.25   0.04   19.54   17.58   187   SPT wetting current pulse   15   20   ms   RT   17.24   0.03   25.31   22.88   17.24   0.03   16.67   6.88   17.24   0.03   25.37   22.88   17.24   0.04   21.80   19.62   17.25   0.04   16.47   6.87   188   SPZ wetting current pulse   15   20   ms   RT   17.25   0.04   21.34   17.26   0.03   25.77   23.32   17.27   0.04   22.57   20.51   188   SPZ wetting current pulse   15   20   ms   RT   17.25   0.04   21.25   20.41   17.26   0.03   25.77   23.32   17.27   0.04   22.57   20.51   188   SPZ wetting current pulse   15   20   ms   RT   17.25   0.04   21.20   18.93   17.27   0.03   16.82   7.21   17.26   0.04   22.137   19.35   188   SPZ wetting current pulse   15   20   ms   RT   17.25   0.04   21.02   18.93   17.27   0.03   16.82   7.21   17.26   0.04   21.37   19.35   188   SPZ wetting current pulse   15   20   ms   RT   17.25   0.05   17.89   16.12   17.25   0.04   20.65   18.57   17.24   0.04   20.76   18.95   189   SPZ wetting current pulse   15   20   ms   RT   17.25   0.04   20.94   18.85   17.25   0.04   20.65   18.77   17.24   0.04   20.76   18.95   1	186	•				CT	18.92	0.04	21.95	9.44	18.93	0.03		10.62	18.93	0.05	12.89	7.95
187   SPI wetting current pulse   15   20   ms   RT   17.24   0.03   25.31   22.88   17.24   0.03   16.67   6.88   17.26   0.03   25.37   22.88   17.24   0.03   16.67   6.88   17.26   0.03   25.37   22.88   17.24   0.04   22.45   17.25   0.04   21.28   19.21   17.25   0.04   22.57   20.51   188   SP2 wetting current pulse   15   20   ms   HT   17.26   0.04   22.57   20.41   17.26   0.03   25.77   23.32   17.27   0.04   22.57   20.51   188   SP2 wetting current pulse   15   20   ms   RT   17.25   0.04   21.02   18.93   17.27   0.03   16.82   7.21   17.26   0.04   21.37   19.35   188   SP2 wetting current pulse   15   20   ms   RT   17.25   0.04   21.02   18.93   17.27   0.03   16.82   7.21   17.26   0.04   21.37   19.35   188   SP2 wetting current pulse   15   20   ms   HT   17.25   0.04   21.02   18.93   17.27   0.03   16.82   7.21   17.26   0.04   21.37   19.35   188   SP2 wetting current pulse   15   20   ms   HT   17.25   0.04   20.94   18.85   17.25   0.04   20.65   18.57   17.24   0.04   20.76   18.59   18.99   SP3 wetting current pulse   15   20   ms   RT   17.25   0.04   20.94   18.85   17.25   0.04   20.65   18.57   17.24   0.04   20.76   18.59   18.99   SP3 wetting current pulse   15   20   ms   RT   17.24   0.04   21.47   19.24   17.25   0.04   20.18   18.19   17.25   0.04   15.76   6.64   19.93   19.90   SP4 wetting current pulse   15   20   ms   RT   18.87   0.04   20.34   18.85   0.04   20.34   19.22   19.05   18.87   0.04   19.05   19.05   18.87   0.04   19.05   19.05   18.87   0.04   19.05   18.87   0.04   19.05   18.88   0.05   18.50   19.05   19.05   19.05   18.87   0.04   20.01   19.22   19.05   19.05   19.05   19.05   19.05   19.05   18.87   0.04   20.01   19.22   19.05   19.05   19.05   19.05   19.05   19.05   19.05   18.87   0.04   20.05   19.05   18.87   0.04   20.05   18.89		•																
187   SP1 wetting current pulse		<u> </u>																
188   SP2 wetting current pulse   15   20   ms   HT   17.26   0.04   22.57   20.41   17.26   0.03   25.77   23.32   17.27   0.04   22.57   20.51		0 1																
188   SP2 wetting current pulse   15   20   ms   RT   17.25   0.04   21.02   18.93   17.27   0.03   16.82   7.21   17.26   0.04   21.37   19.35     188   SP2 wetting current pulse   15   20   ms   CT   17.26   0.05   17.89   16.12   17.25   0.04   20.65   18.57   17.24   0.04   20.76   18.59     189   SP3 wetting current pulse   15   20   ms   RT   17.25   0.05   17.89   16.12   17.25   0.04   20.65   18.57   17.24   0.04   20.76   18.59     189   SP3 wetting current pulse   15   20   ms   RT   17.25   0.04   20.94   18.85   17.25   0.04   14.79   6.17   17.24   0.04   19.33   17.35     189   SP3 wetting current pulse   15   20   ms   RT   17.25   0.04   20.94   18.85   17.25   0.04   14.79   6.17   17.24   0.04   19.33   17.35     189   SP3 wetting current pulse   15   20   ms   CT   17.24   0.04   21.47   19.24   17.25   0.04   20.18   18.19   17.25   0.04   15.76   6.64     190   SP4 wetting current pulse   15   20   ms   RT   18.86   0.04   23.04   10.53   18.86   0.04   19.32   8.83   18.85   0.04   20.01   9.22     190   SP4 wetting current pulse   15   20   ms   RT   18.87   0.04   19.60   8.84   18.87   0.04   15.95   10.32   18.88   0.05   18.20     191   SP5 wetting current pulse   15   20   ms   RT   18.86   0.04   23.04   10.53   18.86   0.04   19.32   8.83   18.85   0.04   20.01   9.22     191   SP5 wetting current pulse   15   20   ms   RT   18.86   0.04   23.04   10.53   18.86   0.04   19.32   8.83   18.85   0.04   20.01   9.22     191   SP5 wetting current pulse   15   20   ms   RT   18.87   0.04   19.60   8.84   18.87   0.04   19.32   8.83   18.85   0.04   20.01   9.22     192   SP6 wetting current pulse   15   20   ms   RT   18.87   0.04   19.60   8.84   18.87   0.04   19.32   8.83   18.85   0.04   20.01   9.22     192   SP6 wetting current pulse   15   20   ms   RT   18.87   0.04   19.60   8.84   18.87   0.04   19.32   8.83   18.85   0.04   20.01   9.22     192   SP6 wetting current pulse   15   20   ms   RT   18.87   0.04   20.15   91.5   18.87   0.04   20.59   91.50   18.23   91.50   18.2		<u> </u>																
188   SP2 wetting current pulse   15   20   ms   CT   17.26   0.03   28.29   25.62   17.27   0.03   25.98   23.55   17.27   0.04   15.51   6.66     189   SP3 wetting current pulse   15   20   ms   RT   17.25   0.04   20.94   18.85   17.25   0.04   20.65   18.57   17.24   0.04   20.76   18.59     189   SP3 wetting current pulse   15   20   ms   RT   17.25   0.04   20.94   18.85   17.25   0.04   20.65   18.57   17.24   0.04   20.76   18.59     189   SP3 wetting current pulse   15   20   ms   CT   17.24   0.04   21.47   19.24   17.25   0.04   20.18   18.19   17.25   0.04   15.76   6.64     190   SP4 wetting current pulse   15   20   ms   RT   18.86   0.04   23.04   10.53   18.86   0.04   19.32   18.88   18.55   0.04   20.10   19.22     190   SP4 wetting current pulse   15   20   ms   RT   18.87   0.04   19.60   8.84   18.87   0.04   15.95   10.32   18.88   0.05   18.50   8.26     190   SP4 wetting current pulse   15   20   ms   RT   18.86   0.04   19.60   8.84   18.87   0.04   15.95   10.32   18.88   0.05   18.50   8.26     190   SP5 wetting current pulse   15   20   ms   RT   18.86   0.04   23.04   10.53   18.86   0.04   19.32   18.88   0.05   18.50   8.26     191   SP5 wetting current pulse   15   20   ms   RT   18.87   0.04   23.04   10.53   18.86   0.04   19.32   18.88   0.05   18.50   8.26     191   SP5 wetting current pulse   15   20   ms   RT   18.87   0.04   10.53   18.86   0.04   19.32   18.88   0.05   18.50   0.04   19.92     191   SP5 wetting current pulse   15   20   ms   RT   18.87   0.04   19.60   8.84   18.87   0.04   15.95   10.32   18.88   0.05   18.50   0.04   19.92     191   SP5 wetting current pulse   15   20   ms   RT   18.87   0.04   23.80   10.38   18.90   0.04   12.96   8.22     192   SP6 wetting current pulse   15   20   ms   RT   18.87   0.04   23.31   10.14   18.90   0.05   12.89   8.12   18.89   0.04   12.96   8.22     192   SP6 wetting current pulse   15   20   ms   RT   18.87   0.04   20.15   9.15   18.87   0.04   23.80   10.38   18.89   0.04   23.80   10.38   18.89   0.04   23.80		<u> </u>																
189   SP3 wetting current pulse   15   20   ms   HT   17.25   0.05   17.89   16.12   17.25   0.04   20.65   18.57   17.24   0.04   20.76   18.59   18.95   SP3 wetting current pulse   15   20   ms   RT   17.25   0.04   20.94   18.85   17.25   0.04   14.79   6.17   17.24   0.04   19.33   17.35   18.95   SP3 wetting current pulse   15   20   ms   RT   17.24   0.04   21.47   19.24   17.25   0.04   20.18   18.19   17.25   0.04   15.76   6.64   190   SP4 wetting current pulse   15   20   ms   HT   18.86   0.04   23.04   10.53   18.86   0.04   19.32   18.85   0.04   20.01   9.22   190   SP4 wetting current pulse   15   20   ms   RT   18.87   0.04   19.60   8.84   18.87   0.04   15.95   10.32   18.88   0.05   18.50   8.26   190   SP4 wetting current pulse   15   20   ms   RT   18.87   0.04   19.60   8.84   18.87   0.04   19.32   18.88   0.05   18.50   8.26   191   SP5 wetting current pulse   15   20   ms   HT   18.86   0.04   23.04   10.53   18.86   0.04   19.32   18.88   0.05   18.50   8.26   191   SP5 wetting current pulse   15   20   ms   RT   18.87   0.04   23.04   10.53   18.86   0.04   19.32   18.88   0.05   18.50   8.26   191   SP5 wetting current pulse   15   20   ms   RT   18.87   0.04   19.60   8.84   18.87   0.04   15.95   10.32   18.88   0.05   18.50   8.26   191   SP5 wetting current pulse   15   20   ms   RT   18.87   0.04   19.60   8.84   18.87   0.04   15.95   10.32   18.88   0.05   18.50   8.26   191   SP5 wetting current pulse   15   20   ms   RT   18.87   0.04   23.04   10.53   18.86   0.04   15.95   10.32   18.88   0.05   18.50   8.26   191   SP5 wetting current pulse   15   20   ms   RT   18.87   0.04   23.04   10.53   18.86   0.04   15.95   10.32   18.88   0.05   18.50   8.26   191   SP5 wetting current pulse   15   20   ms   RT   18.87   0.04   23.04   10.53   18.86   0.04   15.95   10.32   18.88   0.05   18.50   8.26   192   SP6 wetting current pulse   15   20   ms   RT   18.87   0.04   20.15   9.15   18.87   0.04   20.15   9.75   18.87   0.04   20.15   9.75   18.87   0.04   20.15   9.75   18.		<u> </u>																
189   SP3 wetting current pulse   15   20   ms   RT   17.25   0.04   20.94   18.85   17.25   0.04   14.79   6.17   17.24   0.04   19.33   17.35		<u> </u>																
189   SP3 wetting current pulse   15   20   ms   CT   17.24   0.04   21.47   19.24   17.25   0.04   20.18   18.19   17.25   0.04   15.76   6.64     190   SP4 wetting current pulse   15   20   ms   HT   18.86   0.04   23.04   10.53   18.86   0.04   19.32   8.83   18.85   0.04   20.01   9.22     190   SP4 wetting current pulse   15   20   ms   RT   18.87   0.04   19.60   8.84   18.87   0.04   15.95   10.32   18.88   0.05   18.50   8.26     190   SP4 wetting current pulse   15   20   ms   CT   18.90   0.05   18.23   8.05   18.91   0.04   23.80   10.38   18.90   0.04   12.96   8.22     191   SP5 wetting current pulse   15   20   ms   HT   18.86   0.04   23.04   10.53   18.86   0.04   19.32   8.83   18.85   0.04   20.01   9.22     191   SP5 wetting current pulse   15   20   ms   RT   18.87   0.04   19.60   8.84   18.87   0.04   15.95   10.32   18.88   0.05   18.50   8.26     191   SP5 wetting current pulse   15   20   ms   CT   18.90   0.05   18.23   8.05   18.91   0.04   23.80   10.38   18.90   0.04   12.96   8.22     192   SP6 wetting current pulse   15   20   ms   CT   18.90   0.05   18.23   8.05   18.91   0.04   23.80   10.38   18.90   0.04   12.96   8.22     192   SP6 wetting current pulse   15   20   ms   RT   18.87   0.04   20.15   9.15   18.87   0.04   21.59   9.75   18.87   0.04   19.64   8.84     192   SP6 wetting current pulse   15   20   ms   RT   18.91   0.04   23.31   10.14   18.90   0.05   12.89   8.12   18.91   0.04   22.29   9.73     192   SP6 wetting current pulse   15   20   ms   CT   18.92   0.04   20.79   9.00   18.93   0.04   21.66   9.27   18.92   0.04   13.34   8.27     193   SP7 wetting current pulse   15   20   ms   CT   18.87   0.04   20.15   9.75   18.87   0.04   21.66   9.27   18.92   0.04   13.34   8.27     193   SP7 wetting current pulse   15   20   ms   CT   18.89   0.04   20.38   18.87   0.04   21.66   9.27   18.92   0.04   13.34   8.27     194   SGO wetting current pulse   15   20   ms   CT   18.89   0.04   23.30   10.58   18.89   0.04   23.35   9.88   18.89   0.04   15.26   9.89		<u> </u>																
190   SP4 wetting current pulse   15   20   ms   HT   18.86   0.04   23.04   10.53   18.86   0.04   19.32   8.83   18.85   0.04   20.01   9.22		<u> </u>																
190   SP4 wetting current pulse   15   20   ms   RT   18.87   0.04   19.60   8.84   18.87   0.04   15.95   10.32   18.88   0.05   18.50   8.26		<u> </u>																
190   SP4 wetting current pulse   15   20   ms   CT   18.90   0.05   18.23   8.05   18.91   0.04   23.80   10.38   18.90   0.04   12.96   8.22		<u> </u>																
191   SP5 wetting current pulse   15   20   ms   HT   18.86   0.04   23.04   10.53   18.86   0.04   19.32   8.83   18.85   0.04   20.01   9.22																		
191   SP5 wetting current pulse   15   20   ms   RT   18.87   0.04   19.60   8.84   18.87   0.04   15.95   10.32   18.88   0.05   18.50   8.26		•																
191   SP5 wetting current pulse   15   20   ms   CT   18.90   0.05   18.23   8.05   18.91   0.04   23.80   10.38   18.90   0.04   12.96   8.22		•																
192   SP6 wetting current pulse   15   20   ms   HT   18.87   0.04   20.15   9.15   18.87   0.04   21.59   9.75   18.87   0.04   19.64   8.84     192   SP6 wetting current pulse   15   20   ms   RT   18.91   0.04   23.31   10.14   18.90   0.05   12.89   8.12   18.91   0.04   22.29   9.73     192   SP6 wetting current pulse   15   20   ms   CT   18.92   0.04   20.79   9.00   18.93   0.04   21.66   9.27   18.92   0.04   13.34   8.27     193   SP7 wetting current pulse   15   20   ms   HT   18.84   0.03   25.37   11.74   18.84   0.03   24.96   11.53   18.85   0.04   21.83   10.05     193   SP7 wetting current pulse   15   20   ms   RT   18.87   0.04   21.43   9.72   18.87   0.04   15.26   9.89   18.87   0.04   19.35   8.77     193   SP7 wetting current pulse   15   20   ms   CT   18.89   0.04   23.80   10.58   18.89   0.04   22.35   9.88   18.89   0.04   15.23   9.75     194   SG0 wetting current pulse   15   20   ms   RT   18.82   0.04   21.42   10.08   18.82   0.04   23.15   10.71   18.83   0.04   23.60   11.19     194   SG0 wetting current pulse   15   20   ms   RT   18.85   0.04   23.47   10.82   18.84   0.04   23.15   10.71   18.83   0.04   23.60   11.19     195   SG1 wetting current pulse   15   20   ms   RT   17.24   0.04   20.18   18.11   17.24   0.04   20.38   18.27   17.25   0.04   20.87   18.85     195   SG1 wetting current pulse   15   20   ms   RT   17.25   0.04   20.76   18.70   17.25   0.04   15.79   6.58   17.26   0.04   20.87   18.85     196   SG1 wetting current pulse   15   20   ms   RT   17.24   0.04   20.76   18.70   17.25   0.04   20.38   18.27   17.25   0.04   20.87   18.85     195   SG1 wetting current pulse   15   20   ms   RT   17.25   0.04   20.76   18.70   17.25   0.04   20.87   18.85     196   SG1 wetting current pulse   15   20   ms   RT   17.25   0.04   20.76   18.70   17.25   0.04   20.38   18.27   17.25   0.04   20.87   18.85     196   SG1 wetting current pulse   15   20   ms   RT   17.25   0.04   20.76   18.70   17.25   0.04   20.38   18.27   17.25   0.04   20.87   18.85     197		SP5 wetting current pulse			ms													
192   SP6 wetting current pulse   15   20   ms   RT   18.91   0.04   23.31   10.14   18.90   0.05   12.89   8.12   18.91   0.04   22.29   9.73   192   SP6 wetting current pulse   15   20   ms   CT   18.92   0.04   20.79   9.00   18.93   0.04   21.66   9.27   18.92   0.04   13.34   8.27   193   SP7 wetting current pulse   15   20   ms   RT   18.84   0.03   25.37   11.74   18.84   0.03   24.96   11.53   18.85   0.04   21.83   10.05   193   SP7 wetting current pulse   15   20   ms   RT   18.87   0.04   21.43   9.72   18.87   0.04   15.26   9.89   18.87   0.04   19.35   8.77   193   SP7 wetting current pulse   15   20   ms   CT   18.89   0.04   23.80   10.58   18.89   0.04   22.35   9.88   18.89   0.04   15.23   9.75   194   SG0 wetting current pulse   15   20   ms   RT   18.82   0.04   22.49   10.80   18.80   0.03   24.84   11.92   18.79   0.04   20.68   10.04   19.48   SG0 wetting current pulse   15   20   ms   RT   18.82   0.04   21.42   10.08   18.82   0.04   23.47   10.82   18.84   0.04   23.15   10.61   18.81   0.04   23.60   11.19   194   SG0 wetting current pulse   15   20   ms   CT   18.85   0.04   23.47   10.82   18.84   0.04   23.15   10.71   18.83   0.04   23.60   11.19   194   SG0 wetting current pulse   15   20   ms   CT   18.85   0.04   23.47   10.82   18.84   0.04   23.15   10.71   18.83   0.04   23.60   11.19   194   SG0 wetting current pulse   15   20   ms   CT   18.85   0.04   23.47   10.82   18.84   0.04   23.15   10.71   18.83   0.04   23.60   11.19   195   SG1 wetting current pulse   15   20   ms   RT   17.24   0.04   20.18   18.11   17.24   0.04   20.38   18.27   17.25   0.04   20.87   18.85   195   SG1 wetting current pulse   15   20   ms   RT   17.25   0.04   20.76   18.70   17.25   0.04   15.79   6.58   17.26   0.04   20.87   18.85   18	191	SP5 wetting current pulse			ms	CT	18.90	0.05	18.23	8.05	18.91	0.04	23.80	10.38	18.90	0.04	12.96	8.22
192         SP6 wetting current pulse         15         20         ms         RT         18.91         0.04         23.31         10.14         18.90         0.05         12.89         8.12         18.91         0.04         22.29         9.73           192         SP6 wetting current pulse         15         20         ms         CT         18.92         0.04         20.79         9.00         18.93         0.04         21.66         9.27         18.92         0.04         13.34         8.27           193         SP7 wetting current pulse         15         20         ms         HT         18.84         0.03         25.37         11.74         18.84         0.03         24.96         11.53         18.85         0.04         21.83         10.05           193         SP7 wetting current pulse         15         20         ms         RT         18.87         0.04         21.43         9.72         18.87         0.04         15.26         9.89         18.87         0.04         19.35         8.77           193         SP7 wetting current pulse         15         20         ms         CT         18.89         0.04         23.80         10.58         18.89         0.04         22.35 </td <td>192</td> <td>SP6 wetting current pulse</td> <td>15</td> <td>20</td> <td>ms</td> <td>HT</td> <td>18.87</td> <td>0.04</td> <td>20.15</td> <td>9.15</td> <td>18.87</td> <td>0.04</td> <td>21.59</td> <td>9.75</td> <td>18.87</td> <td>0.04</td> <td>19.64</td> <td>8.84</td>	192	SP6 wetting current pulse	15	20	ms	HT	18.87	0.04	20.15	9.15	18.87	0.04	21.59	9.75	18.87	0.04	19.64	8.84
192         SP6 wetting current pulse         15         20         ms         CT         18.92         0.04         20.79         9.00         18.93         0.04         21.66         9.27         18.92         0.04         13.34         8.27           193         SP7 wetting current pulse         15         20         ms         HT         18.84         0.03         25.37         11.74         18.84         0.03         24.96         11.53         18.85         0.04         21.83         10.05           193         SP7 wetting current pulse         15         20         ms         RT         18.87         0.04         21.43         9.72         18.87         0.04         15.26         9.89         18.87         0.04         19.35         8.77           193         SP7 wetting current pulse         15         20         ms         CT         18.89         0.04         23.80         10.58         18.89         0.04         15.26         9.89         18.87         0.04         19.35         8.77           194         SG0 wetting current pulse         15         20         ms         HT         18.89         0.04         23.80         10.58         18.89         0.04         22.35 </td <td>192</td> <td>000 111</td> <td>15</td> <td>20</td> <td>ms</td> <td>RT</td> <td>18.91</td> <td>0.04</td> <td>23.31</td> <td>10.14</td> <td>18.90</td> <td>0.05</td> <td>12.89</td> <td>8.12</td> <td>18.91</td> <td>0.04</td> <td>22.29</td> <td>9.73</td>	192	000 111	15	20	ms	RT	18.91	0.04	23.31	10.14	18.90	0.05	12.89	8.12	18.91	0.04	22.29	9.73
193         SP7 wetting current pulse         15         20         ms         HT         18.84         0.03         25.37         11.74         18.84         0.03         24.96         11.53         18.85         0.04         21.83         10.05           193         SP7 wetting current pulse         15         20         ms         RT         18.87         0.04         21.43         9.72         18.87         0.04         15.26         9.89         18.87         0.04         19.35         8.77           193         SP7 wetting current pulse         15         20         ms         CT         18.89         0.04         23.80         10.58         18.89         0.04         22.35         9.88         18.89         0.04         15.23         9.75           194         SG0 wetting current pulse         15         20         ms         HT         18.80         0.04         22.49         10.80         18.89         0.04         22.35         9.88         18.89         0.04         15.23         9.75           194         SG0 wetting current pulse         15         20         ms         RT         18.80         0.04         22.49         10.80         18.80         0.03         24.84<																		
193         SP7 wetting current pulse         15         20         ms         RT         18.87         0.04         21.43         9.72         18.87         0.04         15.26         9.89         18.87         0.04         19.35         8.77           193         SP7 wetting current pulse         15         20         ms         CT         18.89         0.04         23.80         10.58         18.89         0.04         22.35         9.88         18.89         0.04         15.23         9.75           194         SG0 wetting current pulse         15         20         ms         HT         18.80         0.04         22.49         10.80         18.80         0.03         24.84         11.92         18.79         0.04         20.68         10.04           194         SG0 wetting current pulse         15         20         ms         RT         18.82         0.04         21.42         10.08         18.82         0.04         15.62         10.61         18.81         0.04         23.60         11.19           194         SG0 wetting current pulse         15         20         ms         CT         18.85         0.04         23.47         10.82         18.84         0.04         23.1																		
193         SP7 wetting current pulse         15         20         ms         CT         18.89         0.04         23.80         10.58         18.89         0.04         22.35         9.88         18.89         0.04         15.23         9.75           194         SG0 wetting current pulse         15         20         ms         HT         18.80         0.04         22.49         10.80         18.80         0.03         24.84         11.92         18.79         0.04         20.68         10.04           194         SG0 wetting current pulse         15         20         ms         RT         18.82         0.04         21.42         10.08         18.82         0.04         15.62         10.61         18.81         0.04         23.60         11.19           194         SG0 wetting current pulse         15         20         ms         CT         18.85         0.04         23.47         10.82         18.84         0.04         23.15         10.71         18.83         0.04         13.50         9.05           195         SG1 wetting current pulse         15         20         ms         HT         17.24         0.04         20.18         18.11         17.24         0.04         20																		
194         SG0 wetting current pulse         15         20         ms         HT         18.80         0.04         22.49         10.80         18.80         0.03         24.84         11.92         18.79         0.04         20.68         10.04           194         SG0 wetting current pulse         15         20         ms         RT         18.82         0.04         21.42         10.08         18.82         0.04         15.62         10.61         18.81         0.04         23.60         11.19           194         SG0 wetting current pulse         15         20         ms         CT         18.85         0.04         23.47         10.82         18.84         0.04         23.15         10.71         18.83         0.04         13.50         9.05           195         SG1 wetting current pulse         15         20         ms         HT         17.24         0.04         20.18         18.11         17.24         0.04         20.38         18.27         17.25         0.04         23.09         20.82           195         SG1 wetting current pulse         15         20         ms         RT         17.25         0.04         20.76         18.70         17.25         0.04		•																
194         SG0 wetting current pulse         15         20         ms         RT         18.82         0.04         21.42         10.08         18.82         0.04         15.62         10.61         18.81         0.04         23.60         11.19           194         SG0 wetting current pulse         15         20         ms         CT         18.85         0.04         23.47         10.82         18.84         0.04         23.15         10.71         18.83         0.04         13.50         9.05           195         SG1 wetting current pulse         15         20         ms         HT         17.24         0.04         20.18         18.11         17.24         0.04         20.38         18.27         17.25         0.04         23.09         20.82           195         SG1 wetting current pulse         15         20         ms         RT         17.25         0.04         20.76         18.70         17.25         0.04         15.79         6.58         17.26         0.04         20.87         18.85																		
194         SG0 wetting current pulse         15         20         ms         CT         18.85         0.04         23.47         10.82         18.84         0.04         23.15         10.71         18.83         0.04         13.50         9.05           195         SG1 wetting current pulse         15         20         ms         HT         17.24         0.04         20.18         18.11         17.24         0.04         20.38         18.27         17.25         0.04         23.09         20.82           195         SG1 wetting current pulse         15         20         ms         RT         17.25         0.04         20.76         18.70         17.25         0.04         15.79         6.58         17.26         0.04         20.87         18.85		ů																
195         SG1 wetting current pulse         15         20         ms         HT         17.24         0.04         20.18         18.11         17.24         0.04         20.38         18.27         17.25         0.04         23.09         20.82           195         SG1 wetting current pulse         15         20         ms         RT         17.25         0.04         20.76         18.70         17.25         0.04         15.79         6.58         17.26         0.04         20.87         18.85		ů i																
195 SG1 wetting current pulse 15 20 ms RT 17.25 0.04 20.76 18.70 17.25 0.04 15.79 6.58 17.26 0.04 20.87 18.85		ů i																
195 SG1 wetting current pulse   15   20   ms   CT   17.26   0.03   25.79   23.30   17.25   0.04   20.11   18.07   17.26   0.04   15.97   6.78		ů i																
	195	SG1 wetting current pulse	15	20	ms	CT	17.26	0.03	25.79	23.30	17.25	0.04	20.11	18.07	17.26	0.04	15.97	6.78

Test   Test								Lo	t1			Lo	t2			Lo	t3	
1989   5552 welling screet place   15   23   ms   HT   18.97   0.03   24.38   19.08   19.07   0.04   15.06   2.58   18.97   0.03   24.17   9.91	Test#	Test Name	Lo Limit	Hi I imit	Unit	Temn	Mean			Cnk	Mean			Cnk	Mean			Cnk
196   Sc2 weiging current public with a company of the company o																		
196   Sick welfung current pubme   16   20 ms   CT   1962   20.04   21.89   19.05   20.04   20.01   20.07   19.05   20.05   10.17   16.27   10.05																		
197   Sci welling current pube   15																		
197   Side setting current pulse   15   20 ms   RT   17/23   0.04   16.98   16.58   17.22   0.04   14.48   9.58   17.24   0.04   12.03   16.71		ů i																
Fig.   Set   Setting current policy   19   20   mg   CT   1724   0.04   2.050   18.45   17.24   0.04   2.101   18.87   17.24   0.04   14.83   6.14																		
1985   Sed westing current pulse																		
168   S64 westing current pulses   16   20 ms   FT   1897   0.03   26.08   10.55   18.97   0.04   15.87   9.41   18.98   0.04   0.05   24.09   0.84   18.98   0.04   10.95   18.98																		
1989   SGA westing current pulse   18   20 ms   CT   19.00   0.03   24.78   9.91   19.99   0.04   15.91   9.22   18.99   0.04   15.91   9.22   18.99   0.04   15.91   9.22   18.99   0.04   15.91   9.22   18.99   0.04   15.91   9.22   18.99   0.04   15.91   9.22   18.99   0.04   15.91   9.22   18.99   0.04   15.91   9.22   18.99   0.04   15.91   9.22   18.99   0.04   15.91   9.22   18.99   0.04   15.91   9.22   18.99   0.04   15.91   9.22   18.99   0.04   15.91   9.22   18.99   0.04   15.91   9.22   18.99   9.22   9.23																		
1989   SGS wetting current pulse   18   20   ms   HT   18.85   0.04   10.57   0.38   18.85   18.86   0.04   20.15   0.21   18.86   0.04   20.28   22.17   0.78   18.85   18.																		
1989   SGS wetting current pube																		
169   SG wetting current pulse																		
200   S69 wetting current pulse																		
200 SG6 wetting current pulse 15 20 ms RT 1678 0.04 19.05 9.33 16.77 0.04 15.84 10.86 16.77 0.04 18.86 9.32 20.50 SG6 wetting current pulse 15 20 ms LT 1678 0.04 22.76 11.57 0.04 15.87 0.04 12.86 10.04 18.86 10.04 21.85 10.04 22.86 11.57 0.04 22.46 11.07 16.85 10.04 22.85 11.05 0.04 12.85 10.04 12.85 11.05 0.05 11.05 0.05 0																		
200   S68 welling current pulse   15   20 ms   CT   18.78   0.04   23.78   11.57   18.79   0.04   15.65   10.91   18.80   0.04   14.08   9.72		Ŭ ,																
201   SGY wetting current pulse		Ŭ ,																
201   SG7 wetting current pulse   15   20 ms   RT   18.82   0.04   22.35   10.48   18.82   0.03   18.04   12.24   18.80   0.04   22.26   10.86   201   201   202   203		Ŭ ,																
207   SG7 wetting current poles		Ŭ ,																
202   SG8 wetting current pulse   15   20   ms   RT   18,78   0.04   22,18   10,92   18,78   0.04   19,80   9,83   18,78   0.04   20,30   9,83   202   SG8 wetting current pulse   15   20   ms   RT   18,81   0.04   21,36   10,15   18,81   0.04   18,81   10,04   18,81   20,04   20,30   9,83   202   SG8 wetting current pulse   15   20   ms   RT   18,85   0.03   24,75   11,42   18,84   0.03   17,21   11,49   18,84   0.04   15,86   10,57   10,20   18,82   0.04   22,83   18,93   0.04   22,81   19,70   18,93   0.04   22,81   19,70   18,93   0.04   22,81   19,70   18,93   0.04   22,81   19,70   18,93   0.04   22,81   19,70   18,93   0.04   22,81   19,70   18,93   0.04   22,81   19,70   18,93   0.04   22,81   19,70   18,93   0.04   22,81   19,70   18,93   0.04   22,81   19,70   18,93   0.04   22,81   19,70   18,93   0.04   22,81   19,70   18,93   0.04   22,81   19,70   18,93   0.04   19,23   18,93   0.04   19,23   18,93   0.04   19,23   18,93   0.04   19,23   18,93   0.04   19,23   18,93   0.04   19,23   18,93   0.04   19,23   18,93   0.04   19,23   18,93   0.04   19,23   18,93   19,9		Ŭ ,																
202   SG8 wetting current pulse   15   20 ms   CT   18.81   0.04   21.33   10.15   18.81   0.04   16.35   11.22   18.81   0.04   20.30   9.63		Ŭ ,																
SGB wetting current pulse   15   20 ms		ů i																
203 SGV wetting current pulse   15   20 ms   RT   18.93   0.04   22.18   9.26   18.93   0.04   22.61   9.70   18.93   0.04   20.49   8.80   203   SGV wetting current pulse   15   20 ms   RT   18.95   0.04   23.34   9.48   18.98   0.04   12.92   18.93   0.04   12.92   18.07   20.04																		
203 SG9 wetting current pulse   15   20 ms   RT   18.95   0.04   25.36   10.66   18.95   0.04   13.40   8.05   16.95   0.04   19.29   8.07		ů i																
203   SG9 wetting current pulse   15   20 ms   CT   18.88   0.04   23.34   9.48   18.88   0.03   16.96   9.98   18.98   0.04   14.87   8.88																		
SC10 wetting current pulse   15   20 ms																		
SC10 wetting current pulse																		
Solid welling current pulse   15   20 ms   CT   18.84   0.04   21.57   10.05   18.82   0.04   12.22   4.22   18.82   0.04   13.99   9.47																		
205   SG11 wetting current pulse   15   20   ms   HT   18.94   0.03   23.87   10.10   18.95   0.04   16.03   9.66   18.94   0.04   20.68   8.79																		
205 SG11 wetling current pulse 15 20 ms RT 18.97 0.04 20.49 8.41 18.98 0.04 15.52 9.13 18.97 0.03 26.70 11.00 205 SG12 wetling current pulse 15 20 ms RT 18.89 0.04 21.94 8.91 19.00 0.04 13.99 7.99 18.99 0.04 15.9 8.79 206 SG12 wetling current pulse 15 20 ms RT 18.88 0.04 22.46 10.32 18.84 0.04 22.16 10.25 18.85 0.04 19.93 91.8 206 SG12 wetling current pulse 15 20 ms RT 18.88 0.04 22.06 9.13 18.89 0.03 16.73 10.70 18.88 0.04 22.08 10.32 206 SG12 wetling current pulse 15 20 ms RT 18.89 0.04 21.08 9.14 18.89 0.04 14.61 93.0 18.81 0.03 16.66 10.43 207 SG13 wetling current pulse 15 20 ms RT 18.90 0.04 21.39 9.37 18.89 0.04 14.61 93.0 18.81 0.03 16.66 10.43 207 SG13 wetling current pulse 15 20 ms RT 18.90 0.04 21.39 19.37 18.89 0.04 14.61 93.0 18.81 0.03 16.66 10.43 207 SG13 wetling current pulse 15 20 ms RT 18.92 0.04 21.09 9.11 18.92 0.04 14.96 92.9 18.82 0.04 22.87 8.89 207 SG13 wetling current pulse 15 20 ms RT 18.92 0.04 21.09 9.11 18.92 0.04 14.96 92.9 18.62 0.04 22.87 8.89 18.94 0.04 14.04 8.57 18.55 0.04 16.43 93.4 18.94																		
205   SG11 wetling current pulse   15   20   ms   HT   18.85   0.04   21.94   8.91   19.00   0.04   13.95   7.98   13.99   0.04   15.19   8.79		Ŭ İ																
206   SG12 wetting current pulse   15   20   ms   HT   18.85   0.04   22.46   10.32   18.84   0.04   22.16   10.25   18.85   0.04   19.39   9.18		Ŭ İ																
206   SG12 wetting current pulse   15   20 ms   RT   18.88   0.04   21.06   9.41   18.89   0.03   16.73   10.70   18.88   0.04   23.08   10.35		• •																
206   SG12 wetting current pulse   15   20 ms   CT   18.90   0.04   21.39   9.37   18.89   0.04   14.61   9.30   18.91   0.03   16.66   10.42   207   SG13 wetting current pulse   15   20 ms   HT   18.89   0.04   22.18   10.25   18.90   0.04   22.87   8.99   18.92   0.04   22.87   8.99   207   SG13 wetting current pulse   15   20 ms   RT   18.92   0.04   21.09   9.11   18.92   0.04   14.96   9.29   18.92   0.04   22.87   9.89   207   SG13 wetting current pulse   15   20 ms   RT   18.92   0.04   21.09   9.11   18.92   0.04   14.96   9.29   18.92   0.04   22.87   9.89   226   18.91   0.04   22.87   9.89   226   18.91   0.04   22.87   9.89   226   18.91   0.04   22.87   9.89   226   18.91   0.04   22.87   9.89   226   208		• •																
207   SG13 wetting current pulse   15   20   ms   RT   18.99   0.04   23.15   10.25   18.90   0.04   22.63   9.99   18.89   0.04   22.87   9.99   207   SG13 wetting current pulse   15   20   ms   RT   18.92   0.04   20.66   8.88   18.94   0.04   14.96   9.29   18.92   0.04   22.87   9.99   207   SG13 wetting current pulse   15   20   ms   RT   18.93   0.04   20.66   8.88   18.94   0.04   14.96   9.29   18.92   0.04   22.87   9.99   207   SG13 wetting current pulse   15   20   ms   RT   18.93   0.04   20.66   8.88   18.94   0.04   14.96   9.29   18.95   0.04   15.43   9.34   208   Interrupt delay time   -16   16   us   RT   5.30   2.31   2.31   1.54   4.79   2.58   2.33   1.97   5.66   2.68   1.99   1.28   12.80   1.00		• •																
207   SG13 wetting current pulse   15   20   ms   RT   18.92   0.04   21.09   9.11   18.92   0.04   14.96   9.29   18.92   0.04   22.87   9.89		• •																
207   SC13 wetting current pulse   15   20   ms   CT   18.93   0.04   20.66   8.88   18.94   0.04   14.04   8.57   18.95   0.04   15.43   9.34   2.28   2.28   1.51   5.66   2.68   1.99   1.28   2.28   2.24   1.51   5.66   2.68   1.99   1.28   2.28   2.24   1.51   5.66   2.68   1.99   1.28   2.28   2.24   1.51   5.66   2.68   1.99   1.28   2.28   2.24   1.51   5.66   2.68   1.99   1.28   2.28   2.24   2.14   1.44   2.08   Interrupt delay time   -16   16   us   CT   5.21   2.89   1.84   1.24   4.84   2.70   1.97   1.38   5.62   2.59   2.06   1.34   2.28   2.29   2.06   1.34   2.29		ů i																
208   Interrupt delay time		Ŭ I															_	
208   Interrupt delay time		ů i																
208   Interrupt delay time																		
317   SP0 to mux 16ma   -18   -12   mA   HT   -16.02   0.12   8.04   5.30   -16.05   0.16   3.96   3.96   -16.08   0.12   5.35   5.28																		
317   SP0 to mux 16ma																		
317   SP0 to mux 16ma																		
318   SP1 to mux 16ma   -18   -12   mA   HT   -15.98   0.13   7.49   5.05   -15.99   0.15   4.46   4.33   -16.03   0.12   5.22   5.18     318   SP1 to mux 16ma   -18   -12   mA   RT   -16.08   0.14   7.30   4.68   -16.05   0.14   4.66   4.66   -16.11   0.13   5.00   4.85     318   SP1 to mux 16ma   -18   -12   mA   RT   -16.08   0.14   7.30   4.68   -16.05   0.14   4.66   4.66   -16.11   0.13   5.00   4.85     318   SP1 to mux 16ma   -18   -12   mA   RT   -16.08   0.14   7.07   4.75   -16.01   0.15   4.20   4.11   -16.03   0.12   5.52   5.45     319   SP2 to mux 16ma   -18   -12   mA   RT   -16.08   0.14   7.07   4.75   -16.01   0.15   4.20   4.11   -16.03   0.12   5.52   5.45     319   SP2 to mux 16ma   -18   -12   mA   RT   -16.08   0.14   7.22   4.63   -16.06   0.15   4.20   4.11   -16.03   0.12   5.52   5.45     319   SP2 to mux 16ma   -18   -12   mA   RT   -16.08   0.14   7.22   4.63   -16.06   0.15   4.32   4.30   -16.09   0.13   4.82   4.73     319   SP2 to mux 16ma   -18   -12   mA   CT   -15.79   0.17   5.90   4.35   -15.75   0.17   6.06   4.55   -15.79   0.16   6.13   4.51     320   SP3 to mux 16ma   -18   -12   mA   RT   -16.02   0.14   7.04   4.63   -16.01   0.15   4.27   4.17   -16.07   0.16   4.13   4.64     320   SP3 to mux 16ma   -18   -12   mA   RT   -16.02   0.14   7.04   4.63   -16.01   0.15   4.27   4.17   -16.07   0.15   4.20   4.16     321   SP4 to mux 16ma   -18   -12   mA   RT   -15.75   0.18   5.71   4.29   -15.69   0.18   5.64   4.33   -15.78   0.18   5.48   4.54     321   SP4 to mux 16ma   -18   -12   mA   RT   -16.02   0.12   8.33   5.51   -16.07   0.16   4.01   3.97   -16.08   0.16   4.06   4.06     322   SP5 to mux 16ma   -18   -12   mA   RT   -16.02   0.12   8.33   5.51   -16.07   0.16   4.01   3.97   -16.08   0.16   4.06   4.06     322   SP5 to mux 16ma   -18   -12   mA   RT   -16.02   0.12   8.08   5.56   -16.00   0.15   4.21   4.14   -16.04   0.13   4.93   4.90     322   SP5 to mux 16ma   -18   -12   mA   RT   -16.01   0.14   7.39   4.89   -16.02   0.15   4.21   4.14   -16.04																		
318   SP1 to mux 16ma   -18   -12   mA   RT   -16.08   0.14   7.30   4.68   -16.05   0.14   4.66   4.66   -16.11   0.13   5.00   4.85																		
318   SP1 to mux 16ma   -18   -12   mA   CT   -15.81   0.17   5.81   4.25   -15.76   0.17   6.06   4.53   -15.83   0.16   6.36   4.60     319   SP2 to mux 16ma   -18   -12   mA   HT   -15.98   0.14   7.07   4.75   -16.01   0.15   4.20   4.11   -16.03   0.12   5.52   5.45     319   SP2 to mux 16ma   -18   -12   mA   RT   -16.08   0.14   7.22   4.63   -16.06   0.15   4.32   4.30   -16.09   0.13   4.82   4.73     319   SP2 to mux 16ma   -18   -12   mA   RT   -16.08   0.14   7.22   4.63   -16.06   0.15   4.32   4.30   -16.09   0.13   4.82   4.73     319   SP2 to mux 16ma   -18   -12   mA   RT   -15.95   0.17   5.90   4.35   -15.75   0.17   6.06   4.55   -15.79   0.16   6.13   4.51     320   SP3 to mux 16ma   -18   -12   mA   RT   -16.95   0.15   6.88   4.70   -15.97   0.17   3.92   3.77   -16.01   0.14   4.73   4.64     320   SP3 to mux 16ma   -18   -12   mA   RT   -16.02   0.14   7.04   4.63   -16.01   0.15   4.27   4.17   -16.07   0.15   4.20   4.16     320   SP3 to mux 16ma   -18   -12   mA   RT   -15.93   0.12   8.08   5.56   -16.00   0.15   4.29   4.19   -15.99   0.14   4.68   4.54     321   SP4 to mux 16ma   -18   -12   mA   RT   -16.02   0.12   8.33   5.51   -16.07   0.16   4.01   3.97   -16.08   0.16   4.06   4.00     321   SP4 to mux 16ma   -18   -12   mA   RT   -16.02   0.12   8.33   5.51   -16.07   0.16   4.01   3.97   -16.08   0.16   4.06   4.00     321   SP4 to mux 16ma   -18   -12   mA   RT   -15.93   0.12   8.08   5.56   -16.00   0.15   4.29   4.19   -15.99   0.14   4.68   4.54     321   SP4 to mux 16ma   -18   -12   mA   RT   -16.02   0.12   8.08   5.56   -16.00   0.15   4.29   4.19   -15.99   0.14   4.68   4.54     321   SP4 to mux 16ma   -18   -12   mA   RT   -16.02   0.12   8.08   5.58   -16.07   0.16   4.01   3.97   -16.08   0.16   4.06   4.00     322   SP5 to mux 16ma   -18   -12   mA   RT   -16.01   0.14   7.39   4.89   -16.02   0.15   4.21   4.14   -16.04   0.13   4.93   4.90     322   SP5 to mux 16ma   -18   -12   mA   RT   -16.01   0.14   7.39   4.89   -16.02   0.15   4.21   4.14   -16.04																		
319   SP2 to mux 16ma   -18   -12   mA   HT   -15.98   0.14   7.07   4.75   -16.01   0.15   4.20   4.11   -16.03   0.12   5.52   5.45     319   SP2 to mux 16ma   -18   -12   mA   RT   -16.08   0.14   7.22   4.63   -16.06   0.15   4.32   4.30   -16.09   0.13   4.82   4.73     319   SP2 to mux 16ma   -18   -12   mA   RT   -16.08   0.14   7.22   4.63   -16.06   0.15   4.32   4.30   -16.09   0.13   4.82   4.73     319   SP2 to mux 16ma   -18   -12   mA   RT   -15.79   0.17   5.90   4.35   -15.75   0.17   6.06   4.55   -15.79   0.16   6.13   4.51     320   SP3 to mux 16ma   -18   -12   mA   RT   -16.02   0.14   7.04   4.63   -16.01   0.15   4.27   4.17   -16.07   0.15   4.20   4.16     320   SP3 to mux 16ma   -18   -12   mA   RT   -16.02   0.14   7.04   4.63   -16.01   0.15   4.27   4.17   -16.07   0.15   4.20   4.16     320   SP3 to mux 16ma   -18   -12   mA   RT   -15.95   0.18   5.71   4.29   -15.69   0.18   5.64   4.33   -15.78   0.18   5.48   4.06     321   SP4 to mux 16ma   -18   -12   mA   RT   -16.02   0.12   8.08   5.56   -16.00   0.15   4.29   4.19   -15.99   0.14   4.68   4.54     321   SP4 to mux 16ma   -18   -12   mA   RT   -16.02   0.12   8.33   5.51   -16.07   0.16   4.01   3.97   -16.08   0.16   4.06   4.00     321   SP4 to mux 16ma   -18   -12   mA   RT   -16.02   0.12   8.08   5.58   -15.76   0.18   5.41   4.03   -15.77   0.19   5.37   3.99     322   SP5 to mux 16ma   -18   -12   mA   RT   -15.93   0.12   8.08   5.58   -15.97   0.17   3.90   3.73   -15.98   0.11   5.84   5.62     322   SP5 to mux 16ma   -18   -12   mA   RT   -16.01   0.14   7.39   4.89   -16.02   0.15   4.21   4.14   -16.04   0.13   4.93   4.90     322   SP5 to mux 16ma   -18   -12   mA   RT   -15.95   0.14   7.10   4.86   -16.00   0.16   4.13   4.03   -16.00   0.11   5.71   5.57     323   SP6 to mux 16ma   -18   -12   mA   RT   -15.95   0.14   7.10   4.86   -16.00   0.16   4.13   4.03   -16.00   0.11   5.71   5.57     323   SP6 to mux 16ma   -18   -12   mA   RT   -15.95   0.14   7.10   4.86   -16.00   0.16   4.13   4.03   -16.00																		
SP2 to mux 16ma																		
319   SP2 to mux 16ma   -18   -12   mA   CT   -15.79   0.17   5.90   4.35   -15.75   0.17   6.06   4.55   -15.79   0.16   6.13   4.51																		
320         SP3 to mux 16ma         -18         -12         mA         HT         -15.95         0.15         6.88         4.70         -15.97         0.17         3.92         3.77         -16.01         0.14         4.73         4.64           320         SP3 to mux 16ma         -18         -12         mA         RT         -16.02         0.14         7.04         4.63         -16.01         0.15         4.27         4.17         -16.07         0.15         4.20         4.16           320         SP3 to mux 16ma         -18         -12         mA         CT         -15.75         0.18         5.71         4.29         -15.69         0.18         5.64         4.33         -15.78         0.18         5.48         4.06           321         SP4 to mux 16ma         -18         -12         mA         HT         -15.93         0.12         8.08         5.56         -16.00         0.15         4.29         4.19         -15.99         0.14         4.68         4.54           321         SP4 to mux 16ma         -18         -12         mA         RT         -16.02         0.12         8.33         5.51         -16.07         0.16         4.01         3.97         -16.08<																		
320         SP3 to mux 16ma         -18         -12         mA         RT         -16.02         0.14         7.04         4.63         -16.01         0.15         4.27         4.17         -16.07         0.15         4.20         4.16           320         SP3 to mux 16ma         -18         -12         mA         CT         -15.75         0.18         5.71         4.29         -15.69         0.18         5.64         4.33         -15.78         0.18         5.48         4.06           321         SP4 to mux 16ma         -18         -12         mA         HT         -15.93         0.12         8.08         5.56         -16.00         0.15         4.29         4.19         -15.99         0.14         4.68         4.54           321         SP4 to mux 16ma         -18         -12         mA         RT         -16.02         0.12         8.33         5.51         -16.07         0.16         4.01         3.97         -16.08         0.16         4.06         4.00           321         SP4 to mux 16ma         -18         -12         mA         CT         -15.74         0.16         6.45         4.85         -15.07         0.16         4.01         3.97         -16.08<																		
320         SP3 to mux 16ma         -18         -12         mA         CT         -15.75         0.18         5.71         4.29         -15.69         0.18         5.64         4.33         -15.78         0.18         5.48         4.06           321         SP4 to mux 16ma         -18         -12         mA         HT         -15.93         0.12         8.08         5.56         -16.00         0.15         4.29         4.19         -15.99         0.14         4.68         4.54           321         SP4 to mux 16ma         -18         -12         mA         RT         -16.02         0.12         8.33         5.51         -16.07         0.16         4.01         3.97         -16.08         0.16         4.06         4.00           321         SP4 to mux 16ma         -18         -12         mA         CT         -15.74         0.16         6.45         4.85         -15.76         0.18         5.41         4.03         -15.77         0.19         5.37         3.99           322         SP5 to mux 16ma         -18         -12         mA         HT         -15.93         0.12         8.08         5.58         -15.97         0.17         3.90         3.73         -15.98<		OD0 / 40	40											1				
321         SP4 to mux 16ma         -18         -12         mA         HT         -15.93         0.12         8.08         5.56         -16.00         0.15         4.29         4.19         -15.99         0.14         4.68         4.54           321         SP4 to mux 16ma         -18         -12         mA         RT         -16.02         0.12         8.33         5.51         -16.07         0.16         4.01         3.97         -16.08         0.16         4.06         4.00           321         SP4 to mux 16ma         -18         -12         mA         CT         -15.74         0.16         6.45         4.85         -15.76         0.18         5.41         4.03         -15.77         0.19         5.37         3.99           322         SP5 to mux 16ma         -18         -12         mA         HT         -15.93         0.12         8.08         5.58         -15.97         0.17         3.90         3.73         -15.98         0.11         5.84         5.62           322         SP5 to mux 16ma         -18         -12         mA         RT         -16.01         0.14         7.39         4.89         -16.02         0.15         4.21         4.14         -16.04<																		
321         SP4 to mux 16ma         -18         -12         mA         RT         -16.02         0.12         8.33         5.51         -16.07         0.16         4.01         3.97         -16.08         0.16         4.06         4.00           321         SP4 to mux 16ma         -18         -12         mA         CT         -15.74         0.16         6.45         4.85         -15.76         0.18         5.41         4.03         -15.77         0.19         5.37         3.99           322         SP5 to mux 16ma         -18         -12         mA         HT         -15.93         0.12         8.08         5.58         -15.97         0.17         3.90         3.73         -15.98         0.11         5.84         5.62           322         SP5 to mux 16ma         -18         -12         mA         RT         -16.01         0.14         7.39         4.89         -16.02         0.15         4.21         4.14         -16.04         0.13         4.93         4.90           322         SP5 to mux 16ma         -18         -12         mA         CT         -15.75         0.16         6.19         4.64         -15.72         0.17         5.93         4.50         -15.60<																		
321         SP4 to mux 16ma         -18         -12         mA         CT         -15.74         0.16         6.45         4.85         -15.76         0.18         5.41         4.03         -15.77         0.19         5.37         3.99           322         SP5 to mux 16ma         -18         -12         mA         HT         -15.93         0.12         8.08         5.58         -15.97         0.17         3.90         3.73         -15.98         0.11         5.84         5.62           322         SP5 to mux 16ma         -18         -12         mA         RT         -16.01         0.14         7.39         4.89         -16.02         0.15         4.21         4.14         -16.04         0.13         4.90           322         SP5 to mux 16ma         -18         -12         mA         CT         -15.75         0.16         6.19         4.64         -15.72         0.17         5.93         4.50         -15.76         0.16         6.42         4.78           323         SP6 to mux 16ma         -18         -12         mA         HT         -15.95         0.14         7.10         4.86         -16.00         0.16         4.13         4.03         -16.00         0.11<																		
322         SP5 to mux 16ma         -18         -12         mA         HT         -15.93         0.12         8.08         5.58         -15.97         0.17         3.90         3.73         -15.98         0.11         5.84         5.62           322         SP5 to mux 16ma         -18         -12         mA         RT         -16.01         0.14         7.39         4.89         -16.02         0.15         4.21         4.14         -16.04         0.13         4.93         4.90           322         SP5 to mux 16ma         -18         -12         mA         CT         -15.75         0.16         6.19         4.64         -15.72         0.17         5.93         4.50         -15.76         0.16         6.42         4.78           323         SP6 to mux 16ma         -18         -12         mA         HT         -15.95         0.14         7.10         4.86         -16.00         0.16         4.13         4.03         -16.00         0.11         5.71         5.57           323         SP6 to mux 16ma         -18         -12         mA         RT         -16.05         0.13         7.63         4.96         -16.07         0.15         4.33         4.30         -16.06<																		
322         SP5 to mux 16ma         -18         -12         mA         RT         -16.01         0.14         7.39         4.89         -16.02         0.15         4.21         4.14         -16.04         0.13         4.93         4.90           322         SP5 to mux 16ma         -18         -12         mA         CT         -15.75         0.16         6.19         4.64         -15.72         0.17         5.93         4.50         -15.76         0.16         6.42         4.78           323         SP6 to mux 16ma         -18         -12         mA         HT         -15.95         0.14         7.10         4.86         -16.00         0.16         4.13         4.03         -16.00         0.11         5.71         5.57           323         SP6 to mux 16ma         -18         -12         mA         RT         -16.05         0.13         7.63         4.96         -16.07         0.15         4.33         4.30         -16.06         0.12         5.23         5.20																		
322       SP5 to mux 16ma       -18       -12       mA       CT       -15.75       0.16       6.19       4.64       -15.72       0.17       5.93       4.50       -15.76       0.16       6.42       4.78         323       SP6 to mux 16ma       -18       -12       mA       HT       -15.95       0.14       7.10       4.86       -16.00       0.16       4.13       4.03       -16.00       0.11       5.71       5.57         323       SP6 to mux 16ma       -18       -12       mA       RT       -16.05       0.13       7.63       4.96       -16.07       0.15       4.33       4.30       -16.06       0.12       5.23       5.20																		
323 SP6 to mux 16ma -18 -12 MA HT -15.95 0.14 7.10 4.86 -16.00 0.16 4.13 4.03 -16.00 0.11 5.71 5.57 323 SP6 to mux 16ma -18 -12 MA RT -16.05 0.13 7.63 4.96 -16.07 0.15 4.33 4.30 -16.06 0.12 5.23 5.20																		
323 SP6 to mux 16ma -18 -12 mA RT -16.05 0.13 7.63 4.96 -16.07 0.15 4.33 4.30 -16.06 0.12 5.23 5.20																		
323   SPO tO MUX 10MA   -18   -18   -12   MA   CI   -15.78   0.16   6.40   4.75   -15.77   0.18   5.47   4.07   -15.80   0.16   6.25   4.59																		
	323	SP6 to mux 16ma	-18	-12	mA	CT	-15.78	0.16	6.40	4.75	-15.77	0.18	5.47	4.07	-15.80	0.16	6.25	4.59

						1	In	t1			Lo	t2		1	Ic	t3	
Toot#	Test Name	Lolimit	Hi Limit	Unit	Tomp	Mean	Std Dev	Ср	Cpk	Mean	Std Dev	Cp	Cnk	Mean	Std Dev	,	Cnk
Test# 324		Lo Limit -18	-12		Temp HT	-15.97	0.15	6.87	4.66	-16.01	0.15	4.20	Cpk 4.12	-16.02	0.11	Ср 5.66	Cpk 5.57
	SP7 to mux 16ma			mA				6.54									
324	SP7 to mux 16ma	-18	-12	mA	RT	-16.07	0.15		4.21	-16.09	0.16	4.17	4.09	-16.10	0.13	5.04	4.90
324	SP7 to mux 16ma	-18	-12	mA	CT	-15.81	0.17	5.86	4.28	-15.81	0.17	5.72	4.17	-15.85	0.14	7.11	5.11
325	SG0 to mux 16ma	-18	-12	mA	HT	-16.05	0.14	7.07	4.61	-16.06	0.15	4.26	4.24	-16.09	0.12	5.58	5.48
325	SG0 to mux 16ma	-18	-12	mA	RT	-16.10	0.14	7.36	4.65	-16.10	0.14	4.58	4.47	-16.14	0.13	4.90	4.68
325	SG0 to mux 16ma	-18	-12	mA	CT	-15.81	0.17	5.84	4.26	-15.78	0.16	6.25	4.63	-15.84	0.16	6.41	4.62
326	SG1 to mux 16ma	-18	-12	mA	HT	-15.98	0.14	7.14	4.80	-15.99	0.17	3.84	3.72	-16.04	0.12	5.21	5.18
326	SG1 to mux 16ma	-18	-12	mA	RT	-16.04	0.14	7.03	4.59	-16.01	0.16	4.18	4.08	-16.08	0.14	4.53	4.46
326	SG1 to mux 16ma	-18	-12	mA	CT	-15.74	0.17	5.90	4.44	-15.68	0.18	5.57	4.30	-15.77	0.17	5.83	4.34
327	SG2 to mux 16ma	-18	-12	mA	HT	-15.97	0.13	7.59	5.14	-16.01	0.17	3.85	3.77	-16.03	0.13	4.92	4.88
327	SG2 to mux 16ma	-18	-12	mA	RT	-16.02	0.13	7.48	4.93	-16.04	0.17	3.84	3.81	-16.09	0.15	4.39	4.31
327	SG2 to mux 16ma	-18	-12	mA	CT	-15.73	0.17	5.99	4.53	-15.71	0.19	5.39	4.12	-15.77	0.17	6.04	4.48
328	SG3 to mux 16ma	-18	-12	mA	HT	-16.02	0.13	7.80	5.15	-16.04	0.16	4.19	4.17	-16.08	0.12	5.22	5.14
328	SG3 to mux 16ma	-18	-12	mA	RT	-16.09	0.13	7.82	4.99	-16.09	0.15	4.42	4.34	-16.14	0.14	4.61	4.39
328	SG3 to mux 16ma	-18	-12	mA	CT	-15.80	0.15	6.45	4.74	-15.77	0.17	5.90	4.38	-15.85	0.17	6.03	4.33
329	SG4 to mux 16ma	-18	-12	mA	HT	-15.96	0.13	7.99	5.44	-16.01	0.16	4.16	4.07	-16.02	0.13	4.96	4.88
329	SG4 to mux 16ma	-18	-12	mA	RT	-16.04	0.13	7.84	5.11	-16.07	0.16	4.16	4.11	-16.10	0.15	4.21	4.10
329	SG4 to mux 16ma	-18	-12	mA	CT	-15.77	0.15	6.66	4.96	-15.77	0.18	5.61	4.17	-15.81	0.19	5.38	3.92
330	SG5 to mux 16ma	-18	-12	mA	HT	-15.95	0.13	7.86	5.38	-16.00	0.16	4.07	3.96	-16.01	0.12	5.41	5.29
330	SG5 to mux 16ma	-18	-12	mA	RT	-16.03	0.13	7.85	5.16	-16.05	0.16	4.12	4.11	-16.07	0.12	5.21	5.16
330	SG5 to mux 16ma	-18	-12	mA	CT	-15.75	0.17	6.02	4.51	-15.75	0.18	5.62	4.21	-15.77	0.12	6.75	5.01
331	SG6 to mux 16ma	-18	-12	mA	HT	-16.00	0.17	7.30	4.87	-16.07	0.10	3.76	3.73	-16.07	0.13	5.27	5.23
331	SG6 to mux 16ma	-18	-12	mA	RT	-16.11	0.14	7.52	4.75	-16.15	0.17	3.84	3.63	-16.17	0.12	5.10	4.77
		-18	-12		CT	-15.85		6.39	4.75	-15.86		5.62		-15.89		6.54	4.77
331	SG6 to mux 16ma			mA			0.16				0.18		4.00		0.15		
332	SG7 to mux 16ma	-18	-12	mA	HT	-15.92	0.13	7.96	5.51	-15.97	0.15	4.41	4.24	-15.99	0.11	5.85	5.66
332	SG7 to mux 16ma	-18	-12	mA	RT	-16.02	0.12	8.34	5.51	-16.04	0.14	4.58	4.55	-16.07	0.13	4.92	4.86
332	SG7 to mux 16ma	-18	-12	mA	CT	-15.75	0.15	6.77	5.07	-15.75	0.17	5.98	4.48	-15.80	0.17	6.05	4.43
333	SG8 to mux 16ma	-18	-12	mA	HT	-15.89	0.13	7.56	5.31	-15.91	0.15	4.25	3.94	-15.95	0.13	4.87	4.63
333	SG8 to mux 16ma	-18	-12	mA	RT	-15.99	0.12	8.01	5.37	-15.97	0.14	4.57	4.37	-16.02	0.16	4.08	4.02
333	SG8 to mux 16ma	-18	-12	mA	CT	-15.71	0.16	6.07	4.65	-15.67	0.16	6.35	4.93	-15.73	0.19	5.27	3.99
334	SG9 to mux 16ma	-18	-12	mA	HT	-15.92	0.14	7.34	5.09	-15.96	0.14	4.52	4.32	-15.98	0.13	5.09	4.90
334	SG9 to mux 16ma	-18	-12	mA	RT	-16.01	0.12	8.09	5.38	-16.03	0.14	4.66	4.61	-16.06	0.14	4.75	4.73
334	SG9 to mux 16ma	-18	-12	mA	CT	-15.73	0.15	6.88	5.21	-15.73	0.16	6.23	4.72	-15.76	0.15	6.46	4.82
335	SG10 to mux 16ma	-18	-12	mA	HT	-15.91	0.13	7.73	5.39	-15.95	0.15	4.41	4.19	-16.00	0.12	5.44	5.29
335	SG10 to mux 16ma	-18	-12	mA	RT	-15.99	0.13	7.55	5.06	-16.02	0.14	4.59	4.51	-16.08	0.13	4.93	4.85
335	SG10 to mux 16ma	-18	-12	mA	CT	-15.71	0.16	6.14	4.69	-15.71	0.17	5.96	4.54	-15.79	0.16	6.28	4.63
336	SG11 to mux 16ma	-18	-12	mA	HT	-15.91	0.13	7.42	5.17	-15.97	0.14	4.65	4.45	-15.98	0.13	4.95	4.78
336	SG11 to mux 16ma	-18	-12	mA	RT	-16.00	0.13	7.46	4.97	-16.04	0.14	4.76	4.73	-16.08	0.14	4.71	4.65
336	SG11 to mux 16ma	-18	-12	mA	CT	-15.72	0.16	6.43	4.89	-15.75	0.16	6.40	4.79	-15.79	0.16	6.38	4.69
337	SG12 to mux 16ma	-18	-12	mA	HT	-15.92	0.13	7.59	5.26	-15.97	0.15	4.37	4.19	-15.99	0.12	5.32	5.14
337	SG12 to mux 16ma	-18	-12	mA	RT	-16.01	0.13	7.41	4.92	-16.03	0.15	4.41	4.37	-16.06	0.13	4.88	4.86
337	SG12 to mux 16ma	-18	-12	mA	CT	-15.73	0.16	6.12	4.62	-15.75	0.16	6.29	4.73	-15.78	0.15	6.62	4.89
338	SG13 to mux 16ma	-18	-12	mA	HT	-15.91	0.14	7.38	5.14	-15.97	0.15	4.42	4.24	-15.97	0.12	5.22	5.00
338	SG13 to mux 16ma	-18	-12	mA	RT	-16.02	0.14	7.39	4.87	-16.07	0.15	4.45	4.41	-16.08	0.12	5.20	5.13
338	SG13 to mux 16ma	-18	-12	mA	CT	-15.77	0.14	6.21	4.62	-15.78	0.16	6.12	4.53	-15.80	0.12	6.86	5.03
347	SP0 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.10	4.30	4.23	-2.00	0.10	3.41	3.27	-2.01	0.13	3.90	3.61
347	SP0 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.96	3.69	-2.00	0.02	3.11	2.83	-2.01	0.01	3.55	3.24
347	SP0 to mux 2ma	-2.2	-1.8	mA	CT	-1.98	0.01	3.47	3.05	-1.97	0.02	3.15	2.72	-1.98	0.02	3.06	2.79
348	SP1 to mux 2ma	-2.2	-1.8		HT	-1.98	0.02	3.54	3.05	-1.97	0.02	3.43	3.32	-1.98	0.02	4.13	3.76
	i -			mA mA													
348	SP1 to mux 2ma	-2.2	-1.8	mA	RT	-2.01	0.02	3.34	3.11	-2.00	0.02	3.13	2.81	-2.01	0.02	4.30	3.98
348	SP1 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.05	2.73	-1.97	0.02	3.17	2.69	-1.97	0.02	3.68	3.27
349	SP2 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.21	2.87	-2.00	0.02	3.61	3.49	-2.00	0.01	4.09	3.71
349	SP2 to mux 2ma	-2.2	-1.8	mA	RT	-2.01	0.02	3.38	3.16	-2.00	0.02	3.34	3.02	-2.01	0.02	4.12	3.87
349	SP2 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.32	2.95	-1.97	0.02	3.48	2.96	-1.97	0.02	3.48	3.04
350	SP3 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.18	2.76	-2.00	0.02	3.30	3.27	-2.00	0.02	3.55	3.17
350	SP3 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.32	2.97	-2.00	0.02	3.12	2.72	-2.01	0.02	3.36	3.18
350	SP3 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.19	2.73	-1.96	0.02	3.03	2.47	-1.97	0.02	2.90	2.51
351	SP4 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.43	2.93	-2.00	0.02	3.51	3.40	-2.00	0.02	3.59	3.16
351	SP4 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.72	3.29	-2.01	0.02	2.99	2.73	-2.01	0.02	3.60	3.41
351	SP4 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.47	2.96	-1.97	0.02	3.12	2.68	-1.97	0.02	3.06	2.63
	1																

							Lo	t1			Lo	t2			Lo	t3	
Test#	Test Name	Lo Limit	Hi Limit	Unit	Temp	Mean	Std Dev	Ср	Cpk	Mean	Std Dev	Ср	Cpk	Mean	Std Dev	Ср	Cpk
352	SP5 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.37	2.90	-2.00	0.02	3.41	3.39	-2.00	0.02	3.77	3.31
352	SP5 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.32	3.01	-2.00	0.02	3.48	3.04	-2.00	0.02	3.53	3.37
352	SP5 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.09	2.68	-1.96	0.02	3.59	2.99	-1.97	0.02	3.08	2.66
353	SP6 to mux 2ma	-2.2	-1.8	mA	HT	-1.99	0.02	3.16	2.66	-2.00	0.02	3.30	3.27	-2.00	0.01	4.10	3.54
353	SP6 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.46	3.07	-2.00	0.02	2.95	2.61	-2.00	0.02	4.26	4.14
353	SP6 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.42	2.93	-1.97	0.02	2.88	2.43	-1.97	0.02	3.27	2.81
354	SP7 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.15	2.70	-2.00	0.02	3.41	3.37	-2.00	0.01	3.85	3.42
354	SP7 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.14	2.84	-2.00	0.02	3.00	2.66	-2.01	0.02	3.77	3.55
354	SP7 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.11	2.74	-1.97	0.02	3.01	2.57	-1.97	0.02	3.28	2.92
355	SG0 to mux 2ma	-2.2	-1.8	mA	HT	-2.01	0.02	3.05	2.82	-2.01	0.02	3.53	3.33	-2.01	0.01	4.31	4.04
355	SG0 to mux 2ma	-2.2	-1.8	mA	RT	-2.01	0.02	3.26	3.08	-2.01	0.02	3.30	3.04	-2.01	0.02	4.14	3.76
355	SG0 to mux 2ma	-2.2	-1.8	mA	CT	-1.98	0.02	3.12	2.81	-1.97	0.02	3.42	2.94	-1.98	0.02	3.51	3.16
356	SG1 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.08	2.79	-2.00	0.02	3.24	3.09	-2.01	0.01	4.13	3.83
356	SG1 to mux 2ma	-2.2	-1.8	mA	RT	-2.01	0.02	3.12	2.88	-2.00	0.02	2.90	2.60	-2.01	0.02	3.99	3.69
356	SG1 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.33	2.92	-1.96	0.02	2.94	2.44	-1.97	0.02	3.27	2.86
357	SG2 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.26	2.95	-2.01	0.02	3.28	3.10	-2.01	0.02	3.51	3.26
357	SG2 to mux 2ma	-2.2	-1.8	mA	RT	-2.01	0.02	3.52	3.26	-2.01	0.02	2.92	2.69	-2.01	0.02	3.65	3.34
357	SG2 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.27	2.86	-1.97	0.02	2.95	2.52	-1.97	0.02	3.27	2.89
358	SG3 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.34	3.02	-2.01	0.02	3.42	3.21	-2.01	0.02	4.38	4.10
358	SG3 to mux 2ma	-2.2	-1.8	mA	RT	-2.01	0.02	3.55	3.31	-2.01	0.02	3.06	2.84	-2.01	0.02	4.29	3.88
358	SG3 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.50	3.08	-1.97	0.02	3.05	2.64	-1.98	0.02	3.48	3.15
359	SG4 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.38	3.02	-2.01	0.02	3.57	3.37	-2.00	0.02	3.85	3.51
359	SG4 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.46	3.22	-2.01	0.02	3.18	2.99	-2.00	0.01	3.79	3.49
359	SG4 to mux 2ma	-2.2	-1.8	mA	CT	-1.98	0.02	3.39	3.05	-1.97	0.02	3.19	2.89	-1.97	0.02	3.19	2.84
360	SG5 to mux 2ma	-2.2	-1.8		HT	-1.99	0.02	3.43	2.90	-2.00	0.02	3.32	3.27	-2.00	0.02	3.17	3.47
360	SG5 to mux 2ma	-2.2	-1.8	mA mA	RT	-2.00	0.02	3.58	3.16	-2.00	0.02	2.83	2.51	-2.00	0.01	4.44	4.22
360	SG5 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.44	2.93	-1.96	0.02	2.88	2.42	-1.97	0.01	3.74	3.22
361	SG6 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.27	2.83	-2.00	0.02	3.36	3.28	-2.00	0.02	3.74	3.33
361	SG6 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.50	3.15	-2.00	0.02	3.13	2.81	-2.00	0.02	4.00	3.75
361	SG6 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.67	3.18	-1.97	0.02	3.30	2.79	-1.97	0.02	3.45	3.03
362	SG7 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.36	2.95	-2.00	0.02	3.55	3.44	-2.00	0.02	4.01	3.62
362	SG7 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.68	3.40	-2.00	0.02	3.24	2.97	-2.00	0.01	3.85	3.56
362	SG7 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.48	3.40	-1.97	0.02	3.24	2.79	-1.98	0.02	3.00	2.79
363	SG8 to mux 2ma	-2.2	-1.8	mA	HT	-1.99	0.02	3.40	2.75	-1.97	0.02	3.48	3.42	-2.00	0.02	3.58	3.07
363	SG8 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.63	3.19	-1.99	0.02	3.40	2.90	-2.00	0.02	3.37	3.07
363	SG8 to mux 2ma	-2.2	-1.8	mA	CT	-1.96	0.02	3.03	2.70	-1.99	0.02	3.53	2.87	-1.97	0.02	2.77	2.36
		-2.2	-1.8		HT	-1.99	0.02	3.32	2.70	-2.00	0.02	3.78	3.75	-2.00	0.02	3.54	3.08
364 364	SG9 to mux 2ma SG9 to mux 2ma	-2.2	-1.8	mA mA	RT	-2.00	0.02	3.53	3.10	-2.00	0.02	3.83	3.40	-2.00	0.02	3.54	3.43
364	SG9 to mux 2ma	-2.2	-1.8	mA	CT	-2.00	0.02	3.53	2.99	-2.00	0.01	3.83	3.40	-2.00 -1.97	0.02	3.59	2.75
365	SG10 to mux 2ma	-2.2	-1.8 -1.8	mA	HT	-1.96	0.02	3.42	2.88	-1.97	0.02	3.60	3.28	-1.97	0.02	3.19	3.37
365	SG10 to mux 2ma	-2.2	-1.8 -1.8	mA mA	RT	-1.99	0.02		2.88	-2.00	0.02		2.82		0.01	3.82	
			_		CT	-2.00 -1.97	0.02	3.37 3.35	2.85	-2.00 -1.97	0.02	3.15 3.10		-2.01 -1.97	0.02	3.76	3.52 2.70
365 366	SG10 to mux 2ma	-2.2 -2.2	-1.8 -1.8	mA	HT	-1.97	0.02	3.35	2.85	-1.97	0.02	3.10	2.63 3.74	-1.97	0.02	3.06	3.36
366	SG11 to mux 2ma	-2.2 -2.2	-1.8 -1.8	mA	RT	-1.99		3.38	3.12	-2.00	0.02					3.82	3.36
	SG11 to mux 2ma			mA			0.02	3.54	2.92		0.02	3.38	3.03	-2.01	0.02		2.86
366	SG11 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02			-1.97		3.44	2.94	-1.97		3.26	
367	SG12 to mux 2ma	-2.2	-1.8	mA	HT	-1.99	0.02	3.56	2.96	-1.99	0.02	3.65	3.63	-1.99	0.01	4.04	3.43
367	SG12 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.76	3.30	-2.00	0.02	3.08	2.68	-2.00	0.02	4.21	4.09
367	SG12 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.64	3.09	-1.96	0.02	3.28	2.74	-1.97	0.02	3.49	2.96
368	SG13 to mux 2ma	-2.2	-1.8	mA	HT	-1.99	0.02	3.41	2.87	-2.00	0.02	3.53	3.51	-2.00	0.01	3.89	3.38
368	SG13 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.72	3.27	-2.00	0.02	3.23	2.83	-2.00	0.02	3.97	3.80
368	SG13 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.59	3.07	-1.96	0.02	3.28	2.75	-1.97	0.02	3.14	2.70

# **Initial Process Study**

# **TSMC PPAP Documents**

- TSMC PPAP documents (FMEAs, Control Plans, Cpks, and GR&R) are considered proprietary information by TSMC, classified as "TSMC INTERNAL USE ONLY" and cannot be distributed with Freescale PPAPs in accordance with an agreement with TSMC.
- The PPAP documents are pulled by Freescale External Manufacturing Quality and checked for compliance with TS16949 requirements.
- For special requests, Freescale may be able to review these documents on a limited basis with customers at the local Freescale sales office.
- If there are any questions, please contact:

Sally Cadena Massey, Freescale MSG NPI Reliability, 512-895-7310 sally.cadena.massey@freescale.com

Jeff Martsching, Freescale External Manufacturing, 512-996-4282 Jeff.Martsching@freescale.com





# **Manufacturing Capability Report**

Com	pany/Manufacturing Site	ID:		Frees	cale / FSL	-TJN-FN	Л	
Repo	ort Date:			17/De	c /13			
Desig	gnate with an "X" only on	e of the following	g boxes and enter the	applicable inf	ormation:			
$\boxtimes$	<b>Cpk Reporting Period:</b>			Nov'2	013			
	Preliminary Ppk - Lot N	umber:						
Desig	gnate with an "X" only on	e of the following	g boxes and enter the	applicable inf	ormation :			
	Wafer Fab Process Tech	nology:						
	Assembly Process Packa	ge Family:				SOIC 32	2ld EP	
	<b>Assembly Process Packa</b>	ge Drawing #:					0543D_D	
						98ARH9	99137A_B	
\$	Special/Important	Generic	# Machines	# Machines	s # Ma	chines	Minimum	Average
	Characteristic	Data	Ppk/Cpk <1.33	Ppk/Cpk	Ppk	/Cpk	Ppk/Cpk	Ppk/Cpk
				1.33-1.66	>/=	1.67	<u>1/</u>	
	Ball shear		0	0	4	13	1.71	2.11
	Wire pull		0	0	4	13	1.83	3.31
	Thickness		0	0		3	3.96	4.29
	Tip to Tip		0	0		8	5.19	7.73
	Coplanarity		0	0		8	6.84	8.77

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<sup>1/</sup> If Ppk < 1.67 or Cpk < 1.67, attach containment action, corrective action, or justification (as appropriate).

# **Qualified Laboratory Documentation**



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#### **SCOPE OF THE LAB**

Rev F

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#### 1.0 Purpose

1.1 The purpose of this specification is to provide a brief summary of lab policy, capabilities, procedures, training and equipment.

## 2.0 Scope

2.1 This document applies to the Arizona Reliability Assessment Lab (ARAL). ARAL provides Reliability Assessment support for the Manufacturing and Business Units of Freescale. ARAL personnel work directly with Reliability Engineering, and Product Engineering to promote effective NPI activity as well as other needed Reliability support of the company's Strategic Agenda.

#### 3.0 Referenced Documents

Document Number	Document Title
L-02 Record	Retention
N/A ARAL	LINKS
G-02 Training	
G-03 ESD	Procedures
P-03 Profile	Procedures

#### 3.1 Document Convention and Classification

- 3.1.1 Document numbers or Web addresses that are underlined in "blue" are links to related information.
  - A. Press CTRL and click to follow the links
- 3.1.2 This document is classified as "FREESCALE GENERAL BUSINESS INFORMATION". The information disclosed herein is the property of Freescale. Freescale reserves all proprietary, design, manufacturing, reproduction, use, and sales rights thereto, and to any article or process utilizing such information, except to the extent that rights are expressly granted to others.



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#### 3.2 Acronyms, Definitions & Terms

Acronyms, Definitions & Terms	Description
ARAL	Arizona Reliability Assessment Lab
ESD Electrostatic	Discharge
NPI	New Product Introduction
FIFO	First In First Out
PM Preventa	tive Maintenance
IT Inform	ation Technology

## 4.0 Equipment Type and Control

- 4.1 Profile or Calibration
  - 4.1.1 ARAL Profile procedures are outlined in spec P-03.
  - 4.1.2 Each piece of equipment has the conditions that can be run in the chamber, clearly marked on an attached label.
    - A. The date the chamber needs to be re-profiled is also listed on the profile label.
    - B. The chamber is only permitted to run conditions that it is profiled for when running qualification product.

#### 4.2 Preventative Maintenance

- 4.2.1 Maintenance records are kept on each major piece of equipment in the lab.
- 4.2.2 PMs are performed at routine intervals.
- 4.2.3 A label on each equipment gives the date of the last PM and also the next due date.

## 4.3 List of Equipment

NAME		Type of EQUIPMENT	SERIAL NO.	MODEL NO.	MANUFACTURER
			ESD Stresses		
MK	1	Zapmaster	309269	MK2	Thermo KeyTek
RCDM	1	Zapmaster	404277	RCDM3	Thermo KeyTek
KT	1	Zapmaster	9002173	7/4	Thermo KeyTek
KT	2	Zapmaster	9309323	7/4	Thermo KeyTek



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NAME		Type of EQUIPMENT	SERIAL NO.	MODEL NO.	MANUFACTURER	
		Typo of Equil MEITT	High Temp with Bias Stresses		MANOLAGIONEN	
DV	2	OP Life Oven	142035	PB216	Despatch	
DV	3	OP Life Oven	142051	PB216	Despatch	
DV	4	OP Life Oven CC3	06-506	HTC-152-2	Delta-V	
DV	5	OP Life Oven CC3	06-506	HTC-152-2	Delta-V	
DV	31	OP Life Oven	129156	PBC2-16	Aehr Test	
W	1	OP Life Oven	151908	Spec Dual Chamber	Wakefield	
W	2	OP Life Oven	151908	Spec Dual Chamber	Wakefield	
W	3	OP Life Oven	210083 / 151907	Spec Dual Chamber	Wakefield	
W	4	OP Life Oven	210083 / 151907	Spec Dual Chamber	Wakefield	
W	9	OP Life Oven	142501	Spec Dual-72	Wakefield	
W	10	OP Life Oven	142501	Spec Dual-72	Wakefield	
W	13	OP Life Oven CC3	149352	PBC1-80	Wakefield	
			Humidity	Stresses		
AC	1	Autoclave	41345-1	ET364P	Trio Tech	
AC	2	Autoclave	41345	ET364P	Trio Tech	
AC	3	Autoclave	8807224	ET362S	Express Test	
Н	1	HAST	725390-1	1000X	Express Test	
Н	2	HAST	41282	6000X	Trio Tech	
Н	3	HAST	40013-1	6000X	Trio Tech	
THB	1	Temp Hum	019396A	ESL-2CA	ESPEC CORP.	
THB	2	Temp Hum	AC-204	AC-7602TDA-3	Blue M	
THB	3	Temp Hum	AC-071	AC-7602A-2	Blue M	
THB	4	Temp Hum	AC-422	AC-7502TDA-3	Blue M	
THB	5	Temp Hum	AC-421	AC-7502TDA-3	Blue M	
THB	6	Temp Hum	AC-420	AC-7502TDA-3	Blue M	
THB	7	Temp Hum	69405	PXA-2AP	ESPEC CORP.	
THB	8	Temp Hum	69406	PXA-2AP	ESPEC CORP.	
THB	9	Temp Hum	154459	EC607	Despatch	
THB	10	Temp Hum	AC-114	AC-7602A-2	Blue M	
THB	11	Temp Hum	AC-205	AC-7602TDA-3	Blue M	
THB	13	Temp Hum	2727	PXA-2AP	ESPEC CORP.	
THB	14	Temp Hum	019396B	ESL-2CA	ESPEC CORP.	
				resses		
PPTCB	1	Temp Cycle	76 51 05	9076-2-3-4-1	Delta Design, Inc.	
PPTCB	2	Temp Cycle	76 57 01	9076-2-3-2	Delta Design, Inc.	
HTOLP	1	Temp Cycle	76 66 01	9076	Delta Design, Inc.	
PTC	1	Temp Cycle	171525	PTC-224	Delta V	
PTC	2	Temp Cycle	171525	PTC-224	Delta V	
TC	1	Temp Cycle	25755	HPS-16	Thermatron Ind.	
TC	2	Temp Cycle	24839	ATS-195-V-C02	Thermatron Ind.	
TC	3	Temp Cycle	27139	ATS-100-V-C-02	Thermatron Ind.	
TC	4	Temp Cycle	35919	ATSS-80-LN2	Thermatron Ind.	
TC	5	Temp Cycle	33971	ATS-320-V-LN2	Thermatron Ind.	
TC	6	Temp Cycle	33972	ATS-320-V-LN2	Thermatron Ind.	
TS	2	Thermal Shock	5363-1	7205	Ransco	



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NAME Type of EQUIPMENT		Type of EQUIPMENT	SERIAL NO. MODEL NO.		MANUFACTURER	
Temperature Storage Stresses						
В	1	High Temp Bake	150322	LAD1423	Despatch	
В	2	High Temp Bake	150326	LAD1423	Despatch	
В	3	High Temp Bake	150325	LAD1423	Despatch	
В	4	High Temp Bake	148332	LAC138A4	Despatch	
В	5	High Temp Bake	148510	LAC138B4	Despatch	
LT	1	Low Temp	39-65-8	9039-1-3-5	Delta Design, Inc.	
LT	LT 2 Low Temp		7081185	C85-5	So-Low	
Other Miscellaneous Equipment						
RF	RF 1 Reflow oven 9545 HVN 155 Conceptronic					
RF	2	Reflow oven	0611-08	PRO 1600	Advanced Techniques (ATCO)	
SA	1	Steam Age	890809-06	100-3-1111	Mountain Gate	
SB	1	Sand Blaster	4005 / 9288 / IG07	MB1000 / 75-CAB	Comco Inc	
TA	1	Thermal Arm	9311-714	T-2420SX7	Thermonics	
CSAM	1	CSAM	2294	D-9000	Sonoscan	
CSAM	2	CSAM	4024	GEN5	Sonoscan	
F	2	Tester	133	3600	Fet Test Inc.	
GL	1	Op Life Oven	152814	LAC1-38A4	Despatch	

# 5.0 Training Lab Personnel

- 5.1 The training procedure for the lab personnel is outlined in spec G-02
- 5.2 The training records can be accessed through ARAL LINKS located on "K drive", the lab network drive.
  - 5.2.1 K Drive Location: rqa\$ on 'az34-file02' (K:)
  - 5.2.2 Do the following to get access to the lab network drive:
    - A. Turn in an IT helpdesk ticket and request access to: rqa\$ on 'az34-file02' (K:).
    - B. The IT personnel will then send an email to the lab manager for authorization to grant access to the requesting person.
    - C. Access will be granted after the lab manager approves.
- 5.3 Training is considered complete after the following have been accomplished by the trainee:
  - 5.3.1 Read and understand any ARAL specification associated with the training.



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- 5.3.2 Be trained, in the procedure, by lab personnel that have previously completed training on the task.
- 5.3.3 Have three observations performing the procedures of the tasks, without assistance.
- 5.3.4 Have the training document signed by the trainee, trainer, and the lab manager.

# 6.0 Product Entry and Running in the Lab

- 6.1 Types of Studies
  - 6.1.1 Devices brought into the lab for Reliability stressing are brought in under one of three categories:
    - A. Qual or Qualification
      - 1. Product brought into the lab to support NPI for Freescale
    - B. Evaluation
      - 1. Product that is a Pre-Qualification for impending NPI support.
    - C. Lab Service
      - 1. All other devices ran in the lab for various engineering reasons.

#### 6.2 Setting Product Priority

- 6.2.1 Each Division, that ARAL supports, is given up to three "Hot" priority quals in the lab.
  - A. More than three can be given at Quality Management discretion.
  - B. Priorities are set by the quality managers.
- 6.2.2 All other product is handled on a FIFO basis as Capacity and Resources permit.

#### 6.3 Lot Tracking Database

- 6.3.1 All lots and product are tracked through the lab using the Quartz Database.
- 6.3.2 The quality organization has required the Quartz system be used for all of the Freescale reliability labs.



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- 6.3.3 Travelers for the product, running through the lab, are generated from the Quartz system.
- 6.4 Standard Chamber conditions are listed in Appendix A
- 6.5 Table of Specifications for the various stresses

Specification Number	Title	Specification Number	Title
S-01	Autoclave	S-11	Temp Cycle
S-02	Gate Leakage	S-12	Temp Humidity Bias
S-03	HAST	S-13	Solderability
S-04	High Temp Bake	S-14	Thermal Shock
S-05	High Temp Operational Life	S-15	Wire Pull
S-06	IOL	S-16	PPTCB
S-08	Power Temp Cycle	S-17	Low Temp Storage
S-10	Reflow	E-02	CDM

## 7.0 ESD and Humidity Control

#### 7.1 ESD Control

- 7.1.1 Spec G-03 outlines the complete ESD control practices performed in ARAL
- 7.1.2 ESD safe areas are posted with signs at the entry of any ESD safe zone and with yellow tape on the floor.
- 7.1.3 Lab technicians test their ESD straps daily to ensure they are ESD safe.
- 7.1.4 An ESD strap is used when handling devices from lots in process in the lab.

#### 7.2 Humidity Control

- 7.2.1 Humidity sensitive areas in the lab have temperature and humidity monitors.
- 7.2.2 If the Humidity goes out of tolerance, qualification work in the area is stopped until the humidity is brought back within tolerance

#### 8.0 Records and Charts

8.1 All Records and Charts generated by the lab are kept and disposed of in accordance with ARAL spec L-02



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# 9.0 Appendix A - Lab Standard Conditions

ARAL	pponum z	STRESSES	
SPEC	STRESSES	(Jedec Abv.)	STRESS CONDITIONS
			D Related Stresses
E-02	Charge Device Model	CDM (ESD)	JEDEC 200V, 500V,1000V or AEC 125V, 250V, 500V, 750V, 1000V
None	Human Body Model	HBM (ESD)	250V, 500V,1000V 2000V, 4000V, 8000V
None	Machine Model	MM (ESD)	50V, 100V, 200V, 400V
None	Latch Up	LU (ESD)	N/A
		Hum	idity Related Stresses
S-01	Auctoclave	AC	121°C/100% RH
S-03	Highly Accelerated Stress Test	HAST	135°C/85% RH
S-12	Temperature Humidity Bias	ТНВ	25°C/90% RH, 30°C/60% RH, 30°C/70% RH, 60°C/60% RH, 60°C/70% RH, 60°C/90% RH, 85°C/60% RH, 85°C/85% RH, 60°C/90% RH, 60°C/70% RH
S-12	Temperature Humidity Storage	THS	25°C/90% RH, 30°C/60% RH, 30°C/70% RH, 60°C/60% RH, 60°C/70% RH, 60°C/90% RH, 85°C/60% RH, 85°C/85% RH, 60°C/90% RH, 60°C/70% RH
		Temperat	ture Cycle Related Stesses
S-11	Temperature Cycle	TC	-0°C/+100°C, -40°C/+125°C, -55°C/+125°C,
S-14	Thermal Shock (Liquid to Liquid)	TS	-0°C/+100°C, -40°C/+125°C, -55°C/+125°C,
S-16	Positive Pressure Temperature Cycle Bias	PPTCB	-40°C/+125°C
S-08	Power Temperature Cycle	PTC	-40°C/+125°C
S-06	DC Intermitant Operational Life	DCIOL	+40°C/+140°C, +100°C/+200°C
S-06	RF Intermitant Operational Life	RFIOL	+100°C/+200°C
		High Temp	with Bias Related Stresses
S-05	High Temperature Operationl Life	HTOL	80°C, 85°C, 90°C, 100°C, 105°C, 125°C, 150°C
S-05	Early Life Failure Rate	ELFR	80°C, 85°C, 90°C, 100°C, 105°C, 125°C, 150°C
S-05	Burn In	ВІ	80°C, 85°C, 90°C, 100°C, 105°C, 125°C, 150°C
S-05	High Temperature Reverse Bias	HTRB	80°C, 85°C, 90°C, 100°C, 105°C, 125°C, 150°C
S-05	High Temperature Gate Bias	HTGB	80°C, 85°C, 90°C, 100°C, 105°C, 125°C, 150°C
		Mis	scalaneous Stresses
S-15	Wire Pull	WP	N/A
S-04, S- 12, S-10	Preconditioning	PC	N/A
S-02	Gate Leakage	GL	+/-400V / 155°C
		Tempe	rature Storage Stresses
S-17	Low Temp Storage	LTS	-10°C, -40°C, -55°C, -65°C
S-04	High Temperature Bake	НТВ	125°C, 135°C, 150°C, 175°C, 200°C, 300°C



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#### 10.0 Revision

Rev	Description of Revision	Originator	Release Date
О	New document	Roland Kallstedt	25 Apr 99
A	Change Tempe Rel Lab to Arizona Reliability Assessment Lab. Move Equipment List, Para. 4.0 to Appendix A. Add spec. 12MSA63581B to Appendix A. Add Small HAST, Thermal Column, Ransco Power Temp Cycle, and Aehr Test Chamber specs to Para. 3.1 & Appendix A. Delete 12MSB17434C, SAT	Bob Meiers	14 Dec 01
В	Rewrite of spec to conform to Rel Lab Scope Standardization effort.	K.P. Mui	19 July 02
С	Corrected spec number for Personal Safety System Procedure.	Susie Almanza	11 Dec 02
D	Added Quality Records in section 3.5 Records as per iddcm request 326345	Susie Almanza	17 Dec 03
Е	Reviewed and removed all references to SPS, Motorola.	J. Schaper	16 Mar 06
F	Total Rewrite of this specification	Dan Cluff	31 Mar 09



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The Freescale Semiconductor certificates scope statement was revised this year in order to comply with LRQA internal procedure and to continue to meet accreditation requirements while supporting Freescale desire for flexibility.

The LRQA general scope format: Location, Activity, Products or Services and Limitations. The main activities referenced in the assessment standard are preferred wherever possible, i.e. design, development, manufacture and installation, or the appropriate equivalent for the industry or sector.

Consequently, the first page of all certificates lists the main location for that specific certificate and the corporate activities (design and manufacture), products (semiconductors) with no service and no restrictions. Freescale Scope: Design and Manufacture of Semiconductors.

The additional pages of each certificate provide a listing of the general activities and where the location is that provide support. Freescale and LRQA agreed to provide general guidance only as the groups names have changed and not the functions.

The Manufacture statement supports all process activities such as - contract review, production, supplier management, purchasing, manufacturing, maintenance, facilities, product testing, corrective action, shipping, wafer fab, assembly, design validation change action boards, internal audits, management responsibility, warehouse, receiving, receiving inspection, ESD, reticle management, process engineering, process modeling, device engineering, production planning, order processing, goal management, training, human resources, legal and all other terminology that could be synonyms.

The Regional Sales statement supports all process activities such as at home salesman, marketing, customer surveys and contract negotiations (without legal authority).

The Design statement supports all process activities such as R&D, product design, process design, design models, test engineering, sample test floors, design verification, reliability testing, product analysis labs, new process introduction teams and activities.

If one wants to know what processes are specifically involved in the assessment, please refer to the Assessment Schedule that is included in each locations' LRQA Assessment Reports.

**Gail Freund** 

Lead QMS Assessor

Lloyd's Register Quality Assurance, Inc.







# CERTIFICATE

This is to certify that

# **Taiwan Semiconductor** Manufacturing Company Ltd.

8, Li-Hsin Rd. 6, Hsinchu Science Park Hsinchu, Taiwan 300-77, R.O.C.

has implemented and maintains a Quality Management System.

#### Scope:

The development of semiconductor foundry process technology and IP/Library design, and the associated manufacture of Integrated Circuits.

An audit, conducted and documented in a report, has verified that this quality management system fulfills the requirements of the following ISO Technical Specification:

# ISO/TS 16949: 2009

(with product design)

Original certification date

2002-10-18

Certification decision

2011-09-02

This certificate is valid until

2014-09-01

Certificate Registration No.

20002969 TS09

0126254

Main Certificate Registration No

20002969 TS09

Buffalo Grove, IL, USA

2011-09-02



2-IAO-QMC-01001

Ganesh Rao Managing Director UL DQS Inc.

IATF Contract Office: DQS GmbH, August-Schanz-Straße 21, 60433 Frankfurt am Main, Germany Issuing Office: UL DQS Inc., 1130 West Lake Cook Road, Suite 340, Buffalo Grove, IL 60089 USA





Annex to Certificate Registration No.: 20002969 TS09

Main Certificate Registration No.: 20002969 TS9

IATF-No.: 0126254

Date of issue: 2011-09-02

#### **Taiwan Semiconductor** Manufacturing Company Ltd.

8, Li-Hsin Rd. 6, Hsinchu Science Park Hsinchu, Taiwan 300-77, R.O.C.

Company Name	Location	Function
Taiwan Semiconductor Manufacturing Company Ltd. Reference No. 20002967	Fab. 2 121, Park Ave. 3 Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C.	Supplemental manufacturing.
Taiwan Semiconductor Manufacturing Company Ltd. Reference No. 20002967	Fab. 3 9, Creation Rd. 1 Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C.	Supplemental manufacturing.
Taiwan Semiconductor Manufacturing Company Ltd. Reference No. 20002970	Fab. 5 121, Park Ave. 3 Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C.	Supplemental manufacturing.
Taiwan Semiconductor Manufacturing Company Ltd. Reference No. 20002966	Fab. 7 6, Creation Rd. 2 Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C.	Supplemental manufacturing.
Taiwan Semiconductor Manufacturing Company Ltd. Reference No. 20002966	Fab. 8 25, Li-Hsin Rd. Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C.	Supplemental manufacturing.
Taiwan Semiconductor Manufacturing Company Ltd. Reference No. 20002970	Fab. 12 8, Li-Hsin Rd. 6 Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C.  168, Park Ave. 2 Hsinchu Science Park Hsinchu County, Taiwan 308-44, R.O.C.	Supplemental manufacturing.









### CERTIFICATE

This is to certify that

#### **Taiwan Semiconductor** Manufacturing Company Ltd.

1, Nan-Ke North Rd., Tainan Science Park Tainan, Taiwan 741-44, R.O.C.

has implemented and maintains a Quality Management System.

#### Scope:

The development of semiconductor foundry process technology and IP/Library design, and the associated manufacture of Integrated Circuits.

An audit, conducted and documented in a report, has verified that this quality management system fulfills the requirements of the following ISO Technical Specification:

ISO/TS 16949: 2009

(with product design)

Original certification date

2002-10-18

Certification decision

2011-09-02

This certificate is valid until

2014-09-01

Certificate Registration No.

20002965 TS09

IATF No.

0126253

Main Certificate Registration No

20002969 TS09

Buffalo Grove, IL, USA

2011-09-02

2-IAO-QMC-01001



Ganesh Rao Managing Director UL DQS Inc.

Issuing Office:

IATF Contract Office: DQS GmbH, August-Schanz-Straße 21, 60433 Frankfurt am Main, Germany UL DQS Inc., 1130 West Lake Cook Road, Suite 340, Buffalo Grove, IL 60089 USA





Annex to Certificate Registration No.: 20002965 TS09

Main Certificate Registration No.: 20002969 TS9

IATF-No.: 0126253

Date of issue: 2011-09-02

### Taiwan Semiconductor Manufacturing Company Ltd.

1, Nan-Ke North Rd., Tainan Science Park Tainan, Taiwan 741-44, R.O.C.

Company Name	Location	Function
Taiwan Semiconductor Manufacturing Company Ltd. Reference No. 20002968	Fab. 6 1, Nan-Ke North Rd., Tainan Science Park, Tainan, Taiwan 741-44, R.O.C.	Supplemental manufacturing.
Taiwan Semiconductor Manufacturing Company Ltd. Reference No. 20002968	Fab. 14 1-1, Nan-Ke North Rd., Tainan Science Park, Tainan, Taiwan 741-44, R.O.C.	Supplemental manufacturing.
Taiwan Semiconductor Manufacturing Company Ltd. Reference No. 20002968		Supplemental manufacturing.
Taiwan Semiconductor Manufacturing Company Ltd. Reference No. 20002969	Fab. 12 8, Li-Hsin Rd. 6 Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C.	Sales, Purchasing, HR, R&D, Document Control and Business Planning.







### **CERTIFICATE**





This is to certify that

#### Taiwan Semiconductor Manufacturing Company Ltd.

No. 1, Keya 6th Rd., Daya Dist., Taichung City, Taiwan 428, R.O.C.

has implemented and maintains a Quality Management System.

#### Scope:

The development of semiconductor foundry process technology and IP/Library design, and the associated manufacture of Integrated Circuits.

An audit, conducted and documented in a report, has verified that this quality management system fulfills the requirements of the following ISO Technical Specification:

ISO/TS 16949: 2009

(with product design)

Original certification date

2012-10-06

Certification decision

2012-10-06

This certificate is valid until Certificate Registration No.

2015-10-05

IATF No.

20006804 TS9

0147759

Main Certificate Registration No

20002969 TS9

Buffalo Grove, IL, USA

2012-10-06

2-IAO-QMC-01001

UL DQS Inc.

Ganesh Rao President

IATF Contract Office: DQS GmbH, August-Schanz-Straße 21, 60433 Frankfurt am Main, Germany Issuing Office: UL DQS Inc., 1130 West Lake Cook Road, Suite 340, Buffalo Grove, IL 60089 USA

1/2





Annex to Certificate Registration No.: 20006804 TS9 Main Certificate Registration No.: 20002969 TS9

IATF-No.: 0147759

Date of issue: 2012-10-06

#### Taiwan Semiconductor Manufacturing Company Ltd.

No. 1, Keya 6th Rd., Daya Dist., Taichung City, Taiwan 428, R.O.C.

Company Name	Location	Function
Taiwan Semiconductor Manufacturing Company Ltd. Ref. No.: 20002969	8, Li-Hsin Rd. 6 Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C.	Sales, Purchasing, HR, R&D, Document Control and Business Planning.







### CERTIFICATE C



This is to certify that

#### TSMC (China) Company Limited, (Fab 10)

4000, Wen Xiang Road, Songjiang 201616, Shanghai P.R. China

has implemented and maintains a Quality Management System.

#### Scope:

The development of semiconductor foundry process technology and IP/Library design, and the associated manufacture of Integrated Circuits.

An audit, conducted and documented in a report, has verified that this quality management system fulfills the requirements of the following ISO Technical Specification:

#### ISO/TS 16949: 2009

(with product design)

Original certification date 2002-10-18

Certification decision 2011-09-02

This certificate is valid until 2014-09-01

Certificate Registration No. 20003351 TS9

IATF No. 0126255

Main Certificate Registration No 20002969 TS9

Buffalo Grove, IL, USA 2012-10-06

2-IAO-QMC-01001

UL DQS Inc.

Ganesh Rao President

IATF Contract Office: DQS GmbH, August-Schanz-Straße 21, 60433 Frankfurt am Main, Germany Ussuing Office: UL DQS Inc., 1130 West Lake Cook Road, Suite 340, Buffalo Grove, IL 60089 USA Responsible Office: DQS-UL AP, OOCL Plaza, Room 1702, No. 841, Yan An Middle Road, Shanghai, 200040, P.R. China



Annex to Certificate Registration No.: 20003351 TS9 Main Certificate Registration No.: 20002969 TS9

IATF-No.: 0126255

Date of issue: 2012-10-06

#### TSMC (China) Company Limited, (Fab 10)

4000, Wen Xiang Road, Songjiang 201616, Shanghai P.R. China

Company Name	Location	Function
Manufacturing Company Ltd.	8, Li-Hsin Rd. 6 Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C.	Sales, Purchasing, HR, R&D, Document Control and Business Planning.



#### CERTIFICATE OF APPROVAL

This is to certify that the Quality Management System of:

Freescale Semiconductor Inc. **Freescale Semiconductor China Xiqing Integrated Semiconductor Manufacturing Site** No. 15 Xinghua Avenue **Xiqing Economic Development Area** Tianjin, 300381, P.R. China

has been approved by Lloyd's Register Quality Assurance to the following Quality Management System Standard:

ISO/TS 16949:2009

The Quality Management System is applicable to:

**Design and Manufacture of Semiconductors.** 

This certificate is valid only in association with the certificate schedule bearing the same number on which the locations applicable to this approval are listed.

Approval

Original ISO/TS 16949 Approval:

May 20, 2004

Certificate No: UQA 0109222/I

Current Certificate:

December 17, 2012

Certificate Expiry:

December 16, 2015

Issued by: Lloyd's Register Quality Assurance, Inc. for and on behalf of Lloyd's Register Quality Assurance Limited

IATF Certificate No: 0153288

This document is subject to the provision on the reverse 1330 Enclave Parkway, Suite 200, Houston, Texas 77077, USA For and on behalf of Hiramford, Middlemarch Office Village, Siskin Drive, Coventry CV3 4FJ, United Kingdom This approval is carried out in accordance with the LRQA assessment and certification procedures and monitored by LRQA

Metro Revision 13



#### **CERTIFICATE SCHEDULE**

# Freescale Semiconductor Inc. Freescale Semiconductor China Xiqing Integrated Semiconductor Manufacturing Site

#### **Manufacture of Semiconductors:**

Freescale Semiconductor Inc. Austin Technology and Manufacturing Center 3501 Ed Bluestein Boulevard Austin, Texas 78721, USA

Freescale Semiconductor Inc. Chandler Fab 1300 North Alma School Road Chandler, Arizona 85224, USA Freescale Semiconductor Inc. Oak Hill Fab 6501 William Cannon Drive West Austin, Texas 78735, USA

Freescale Semiconductor Malaysia Kuala Lumpur Final Manufacturing NO. 2 Jalan SS 8/2 Free Industrial Zone Sungai Way 47300 Petaling Jaya Selangor Malaysia

#### **Regional Sales of Semiconductors:**

Freescale Semiconductor Inc. Corporate Headquarters 6501 William Cannon Drive West Austin, Texas 78735, USA

Freescale Halbleiter Deutschland GmbH Schatzbogen 7 81829 Muenchen Germany Freescale Semiconductor China No. 192 Liangjing Road Pudong New Area Shanghai 201203 P.R. China

Freescale Semiconductor Japan Ltd. Headquarters ARCO Tower 15F 1-8-1, Shimo-Meguro, Meguro-ku Tokyo, 153-0064 Japan



Page 1 of 3

Approval Certificate No: UQA 0109222/I
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For and on behalf of Hiramford, Middlemarch Office Village, Siskin Drive, Coventry CV3 4FJ, United Kingdom
This approval is carried out in accordance with the LRQA assessment and certification procedures and monitored by LRQA.



#### **CERTIFICATE SCHEDULE**

# Freescale Semiconductor Inc. Freescale Semiconductor China Xiqing Integrated Semiconductor Manufacturing Site

#### **Design of Semiconductors:**

Freescale Semiconductor Inc. Corporate Headquarters 6501 William Cannon Drive West Austin, Texas 78735, USA

Freescale Semicondutores Brasil Ltda. Condominio TechnoPark Rodovia Anhanguera, km104, 5 Rua James Clerk Maxwell, 400 Campinas, Sao Paulo, 13069-380 Brazil

Freescale Semiconductor China Ltd. Freescale Suzhou Design Centre Zhuyuan Road Suzhou New District Suzhou 215011 P.R. China

Freescale Semiconducteurs France S.A.S. 134 Avenue du General Eisenhower B.P. 72329 31023 – Toulouse Cedex 1, France Freescale Semiconductor Inc. 2100 East Elliott Road Tempe, Arizona 85284, USA

Freescale Semiconductor China No.192 Liangjing Road Pudong New Area Shanghai 201203 P.R. China

Freescale Polovodice Ceska Republika s.r.o. Systemova aplikacni laborator 1.maje 1009 756 61 Roznov pod Radhostem Czech Republic

Freescale Halbleiter Deutschland GmbH Schatzbogen 7 81829 Munich Germany



IATF Certificate No: 0153288

Page 2 of 3

Approval Certificate No: UQA 0109222/I

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For and on behalf of Hiramford, Middlemarch Office Village, Siskin Drive, Coventry CV3 4FJ, United Kingdom
This approval is carried out in accordance with the LRQA assessment and certification procedures and monitored by LRQA.



#### **CERTIFICATE SCHEDULE**

# Freescale Semiconductor Inc. Freescale Semiconductor China Xiqing Integrated Semiconductor Manufacturing Site

#### **Design of Semiconductors:**

Freescale Semiconductor India Pvt. Ltd. Plot No. 2 & 3 Sector16A

Noida, Uttar Pradesh, 201301

India

Freescale Semiconductor Romania SRL 45, Tudor Vladimirescu Street Tati Business Center Bucharest, 050881 Romania Freescale Semiconductor México Guadalajara Design and Sales Periferico Sur # 8110

Col. El Mante

Tlaquepaque, Jalisco, México

C.P. 45609

Freescale Semiconductor U.K. Kelvin Industrial Estate Colvilles Road East Kilbride, Glasgow

Scotland G75 OTG, United Kingdom

Approval

Certificate No: UQA 0109222/I

Original ISO/TS 16949 Approval:

Current Certificate: Certificate Expiry: May 20, 2004

December 17, 2012 December 16, 2015



IATF Certificate No: 0153288

Page 3 of 3

Approval Certificate No: UQA 0109222/l

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For and on behalf of Hiramford, Middlemarch Office Village, Siskin Drive, Coventry CV3 4FJ, United Kingdom

This approval is carried out in accordance with the LRQA assessment and certification procedures and monitored by LRQA.

# **Appearance Approval Report**

(Not Applicable for Semiconductors)

## Sample Product

Sample Product requirements are identified on the PPAP Checklist; however sample units are shipped separately from the PSW Data Packet. Freescale release for shipment is contingent upon PSW and/or sample customer approval.

### Master Sample

Master Sample is on file in the appropriate MSG Business Unit Quality Organization - Tempe

# **Checking Aids**

(Not Applicable)

## **Records of Compliance**

With Customer-Specific Requirements

### **Part Submission Warrant**



#### **Part Submission Warrant**

Part Name MSDISWA	Cust. Part Number
Shown on Drawing No. MC33972 Rev. 19.0, 3/2012	Orig Part Number MC33972ATEK/R2 & MC33972ATEW/R2
Engineering Change Level Rev 19	Dated 3/2012
Additional Engineering Changes N/A	Dated N/A
	Order No. N/A Weight (kg) 0.472000g
Checking Aid No. N/A Checking Aid Engineering Change Leve	l N/A Dated N/A
	STOMER SUBMITTAL INFORMATION
Freescale Semiconductor	TOWER SOBJETTIVE BY ORDER TOWN
	omer Name/Division
No.15, Xing Hua Avenue; XiQing 300385	
	er/Buyer Code
Tianjin China	ee.
City Region Postal Code Country App	lication
MATERIALS REPORTING	
•	☐ Yes   ☑ No
Submitted by IMDS or other customer format:  Data will be submitted.	ted on customer request.
Are polymeric parts identified with appropriate ISO marking codes?	☐ Yes ☐ No         n/a
REASON FOR SUBMISSION (Check at least one)	
Initial Submission	Change to Optional Construction or Material
Engineering Change(s)	Sub-Supplier or Material Source Change
Tooling: Transfer, Replacement, Refurbishment or additional	Change in Part Processing
Correction of Discrepancy	Parts Produced at Additional Location
Tooling Inactive > than 1 year	Other – please specify
REQUESTED SUBMISSION LEVEL (Check One)	Copper Wire Qualification. See PCN 15977
Level 1 – Warrant only, (and for designated appearance items, an Appearance Approval	Report) submitted to customer.
Level 2 – Warrant with product samples and limited supporting data submitted to custom	
Level 3 – Warrant with product samples and complete supporting data submitted to custo	omer.
<ul> <li>Level 4 – Warrant and other requirements as defined by customer.</li> <li>Level 5 – Warrant with product samples and complete supporting data reviewed at suppl</li> </ul>	jer's manufacturing location
	ici s manufacturing focation.
SUBMISSION RESULTS  The results for	
The results for   ☐ dimensional measurements  ☐ material and functional teachers  ☐ Yes	sts
Mold / Cavity / Production Process Mold/Cavity n/a: Refer to CofDC	(ii 140 - Explanation Required)
DECLARATION	
affirm that the samples represented by this warrant are representative of our parts, which we	• •
Approval Process Manual 4th Edition Requirements. I further warrant these samples were pro- lated also certified that documented evidence of such compliance is on file and available for review	<u> </u>
	32ld SOIC Assembly and Test at Freescale Tianjin China.
SOIC32 300ML 4.6EP/Non-EP TSMC SMOS5 Coppe	
s each Customer Tool properly tagged and numbered?   Yes No	
Organization Authorized Signature Sally Cadena Massey (Electronic Signature)	Date January 15, 2014
Print Name Sally Cadena Massey Phone No. (512) 895-73	
Title Quality PPAP E-mail	sally.cadena.massey@freescale.com
	E ONLY (IF APPLICABLE)
Part Warrant Disposition: Approved Rejected Other	Data
ustomer Signature	Date ng Number Optional

Tracking Number: 201350130A\_0\_0

### **Bulk Material Checklist**

(Not Applicable for Semiconductors)