This for Copper Wire Qualification of
MSDISWA

Freescale Part Numbers:
MC33972ATEK/R2
MC33972ATEW/R2

FREESCALE INTERNAL TRACKING NUMBER: 201350130A_0_0

TSMC Fab 2 / Mask N39B

32 SOIC Assembly and Test at
Freescale Tianjin, China

TEMPE, AZ **January 15, 2014**

Table of Contents

Reference PDF Bookmarks, which link directly to the key elements and contents and are essentially a table of contents for an electronic PDF file.

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PURPOSE AND BACKGROUND STATEMENT

Customer Part Number: Standard Part	Date: 10 December 2013
Part Name: MSDISWA	Freescale Part Number: MC33972ATEK/R2, MC33972ATEW/R2
Customer Ref : NA	Title: MSDISWA Cu Wire Qualification

PURPOSE:

This PPAP package is intended to present data and information required for the qualification of MSDISWA Cu wire in the TSMC facility in the SOIC package from FSL-TJN-FM.

BACKGROUND:

Reliability Qualification testing was performed to qualify the addition of Copper Wire as a wirebond material and Sumitomo EME-G630AY Molding Compound as mold material for SMOS5 SOIC32 300ML 4.6EP and Non-EP package devices. These products were previously assembled with Gold (Au) wire and Hitachi CEL9220HF13 Molding compound at Freescale TJN assembly site, Tianjin, China. These products are now qualified for assembly with Copper (Cu) wire and EME-G630AY Molding Compound at Freescale TJN assembly site, Tianjin, China.

The PPAP manufacturing documentation (e.g., control plans, FMEA's, etc.) included in this PPAP File were current when retrieved and reviewed by Freescale during component-level qualification. This documentation (when reviewed by the Customer) may not reflect the latest revision in our document repository. These documents are intended to reflect semiconductor manufacturing processing and capability. In addition, this PPAP submission may contain documents and data generated both before and after Freescale Semiconductor, Inc was organized as a separate business entity from its predecessor company, Motorola. As such, documentation contained herein may contain references to both Freescale and Motorola, depending on the time the document was originally created.

Design Records

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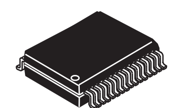
Document Number: MC33972
Rev. 19.0, 3/2012

√RoHS

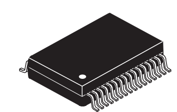
Multiple Switch Detection Interface with Suppressed Wake-up

33972/A/T

MULTIPLE SWITCH DETECTION INTERFACE



EW SUFFIX (Pb-FREE)
98ARH99137A
32-PIN SOICW



EK SUFFIX (Pb-FREE)
98ASA10556D
32-PIN SOICW EP

The 33972 Multiple Switch Detection Interface with suppressed wake-up is designed to detect the closing and opening of up to 22 switch contacts. The switch status, either open or closed, is transferred to the microprocessor unit (MCU) through a serial peripheral interface (SPI). The device also features a 22-to-1 analog multiplexer for reading inputs as analog. The analog input signal is buffered and provided on the AMUX output pin for the MCU to read.

The 33972 device has two modes of operation, Normal and Sleep. Normal mode allows programming of the device and supplies switch contacts with pull-up or pull-down current as it monitors switch change of state. The Sleep mode provides low quiescent current, which makes the 33972 ideal for automotive and industrial products requiring low sleep-state currents.

Features

- Designed to operate 5.5 V ≤ V_{PWR} ≤ 26 V
- Switch input voltage range -14 V to V_{PWR}, 40 V Max
- Interfaces directly to MPU using 3.3 V / 5.0 V SPI protocol
- Selectable wake-up on change of state
- Selectable wetting current (16 or 2.0 mA)
- 8 programmable inputs (switches to battery or ground)
- 14 switch-to-ground inputs
- Typical standby current - V_{PWR} = 100 μA and V_{DD} = 20 μA
- Active interrupt ($\overline{INT}$) on change-of-switch state

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33972TEW/R2	-40 °C to 125 °C	32 SOICW
MC33972ATEW/R2		
MC33972ATEK/R2		32 SOIC EP

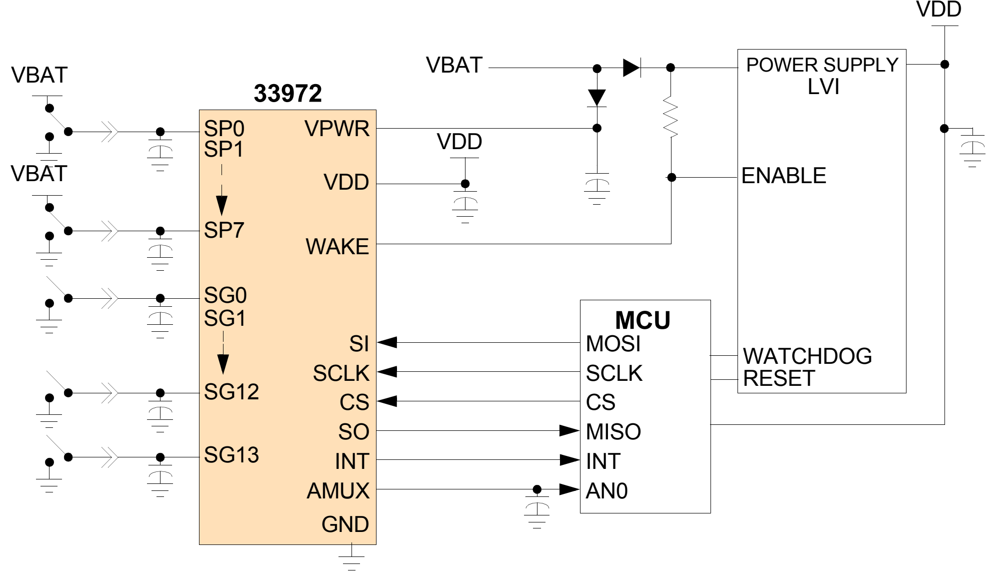


Figure 1. 33972 Simplified Application Diagram

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DEVICE VARIATIONS

Table 1. Device Variations

Device	Switch Input Voltage Range	Reference Location
33972	-14 to 38 V_{DC}	5, 6
33972A	-14 to 40 V_{DC}	5, 6

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INTERNAL BLOCK DIAGRAM

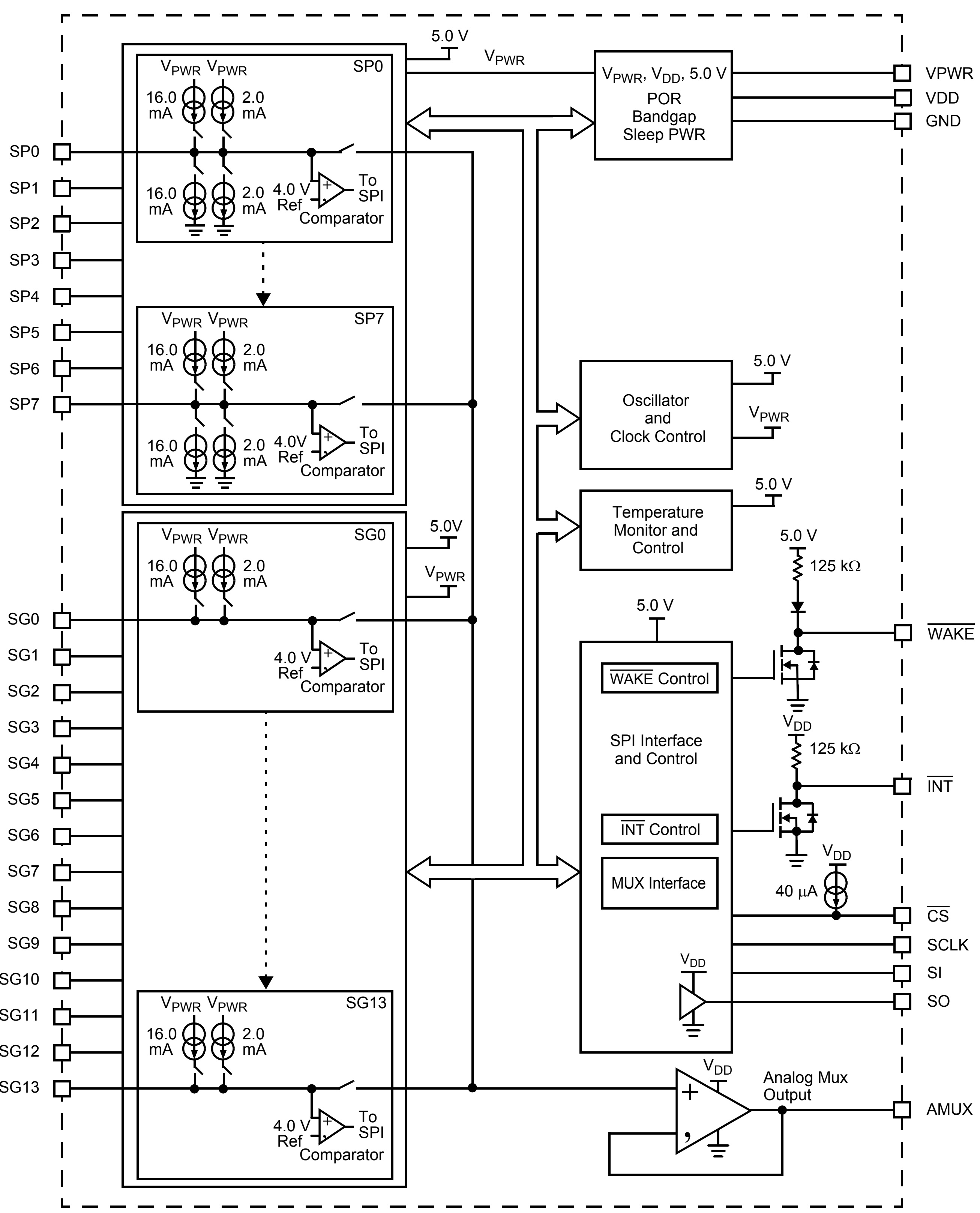

Figure 2. 33972 Simplified Internal Block Diagram

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PIN CONNECTIONS

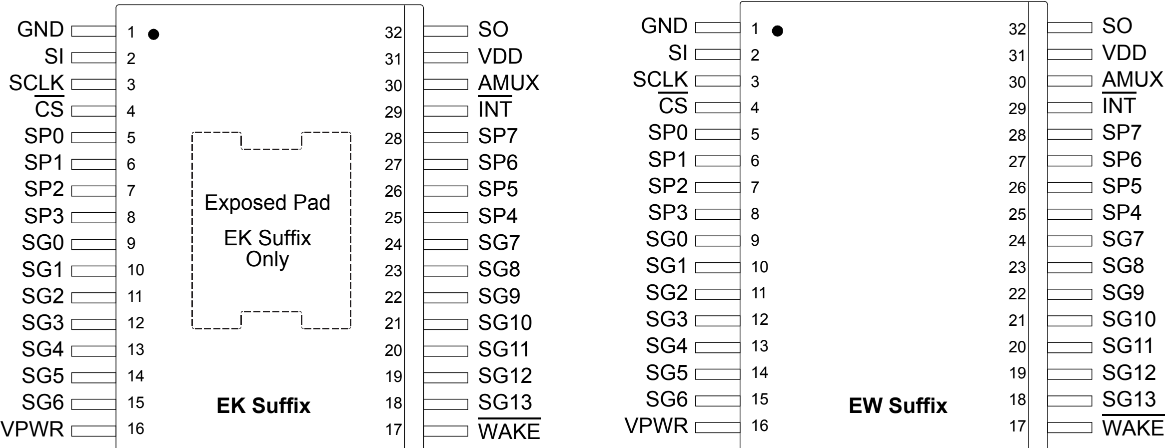

Figure 3. 33972 Pin Connections

Table 2. 33972 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 10.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	GND	Ground	Ground	Ground for logic, analog, and switch to battery inputs.
2	SI	Input	SPI Slave In	SPI control data input pin from the MCU to the 33972.
3	SCLK	Input	Serial Clock	SPI control clock input pin.
4	CS	Input	Chip Select	SPI control chip select input pin from the MCU to the 33972. Logic [0} allows data to be transferred in.
5–8 25–28	SP0–3 SP4–7	Input	Programmable Switches 0–7	Programmable switch-to-battery or switch-to-ground input pins.
9–15, 18–24	SG0–6, SG13–7	Input	Switch-to-Ground Inputs 0–13	Switch-to-ground input pins.
16	VPWR	Input	Battery Input	Battery supply input pin. Pin requires external reverse battery protection.
17	WAKE	Input/Output	Wake-up	Open drain wake-up output. Designed to control a power supply enable pin.
29	INT	Input/Output	Interrupt	Open-drain output to MCU. Used to indicate an input switch change of state.
30	AMUX	Output	Analog Multiplex Output	Analog multiplex output.
31	VDD	Input	Voltage Drain Supply	3.3/5.0 V supply. Sets SPI communication level for the SO driver.
32	SO	Output	SPI Slave Out	Provides digital data from the 33972 to the MCU.
	EP	Ground	Exposed Pad	It is recommended that the exposed pad is terminated to GND (pin 1) and system ground, however, the device will perform as specified with the exposed pad unterminated (floating).

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ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
VDD Supply Voltage $\overline{CS}$, SI, SO, SCLK, $\overline{INT}$, AMUX[1]	–	-0.3 to 7.0	V_{DC}
$\overline{WAKE}$[1]	–	-0.3 to 40	V_{DC}
VPWR Supply Voltage[1]	–	-0.3 to 50	V_{DC}
VPWR Supply Voltage at -40 °C[1]	–	-0.3 to 45	V_{DC}
Switch Input Voltage Range	–	-14 to 40	V_{DC}
Frequency of SPI Operation (V_{DD} = 5.0 V)	–	6.0	MHz
ESD Voltage[3] Human Body Model[2] Applies to all non-input pins Machine Model Charge Device Model Corner Pins Interior Pins	V_{ESD}	±2000 ±2000 ±200 750 500	V
THERMAL RATINGS			
Operating Temperature Ambient Junction	 T_A T_J	 -40 to 125 -40 to 150	°C
Storage Temperature	T_{STG}	-55 to 150	°C
Power Dissipation (T_A = 25 °C)[4]	P_D	1.7	W
Thermal Resistance Non-Exposed Pad Junction to Ambient Junction to Lead Exposed Pad Junction to Ambient Junction to Exposed Pad	 $R_{\theta JA}$ $R_{\theta JL}$ $R_{\theta JA}$ $R_{\theta JC}$	 74 25 71 1.2	°C/W
Peak Package Reflow Temperature During Reflow[5], [6]	T_{PPRT}	Note 6	°C

Notes
1. Exceeding these limits may cause malfunction or permanent damage to the device.
2. ESD data available upon request.
3. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
4. Maximum power dissipation at T_J = 150°C junction temperature with no heat sink used.
5. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
6. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

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STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics

Characteristics noted under conditions 3.1 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{PWR} ≤ 16 V, -40 °C ≤ T_C ≤ 125 °C, unless otherwise noted.(7) Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 13 V, T_A = 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Supply Voltage Supply Voltage Range Quasi-functional[8] Fully Operational Supply Voltage Range Quasi-functional[8]	 $V_{PWR(QF)}$ $V_{PWR(FO)}$ $V_{PWR(QF)}$	 5.5 8.0 26	 – – –	 8.0 26 38/40	V
Supply Current All Switches Open, Normal Mode, Tri-state Disabled	$I_{PWR(ON)}$	 –	 2.0	 4.0	mA
Sleep State Supply Current Scan Timer = 64 ms, Switches Open	$I_{PWR(SS)}$	 40	 70	 100	µA
Logic Supply Voltage	V_{DD}	3.1	–	5.25	V
Logic Supply Current All Switches Open, Normal mode	I_{DD}	 –	 0.25	 0.5	mA
Sleep State Logic Supply Current Scan Timer = 64 ms, Switches Open	$I_{DD(SS)}$	 –	 10	 20	µA
SWITCH INPUT					
Pulse Wetting Current Switch-to-Battery (Current Sink)	I_{PULSE}	12	15	18	mA
Pulse Wetting Current Switch-to-Ground (Current Source)	I_{PULSE}	12	16	18	mA
Sustain Current Switch-to-Battery Input (Current Sink)	$I_{SUSTAIN}$	1.8	2.0	2.2	mA
Sustain Current Switch-to-Ground Input (Current Source)	$I_{SUSTAIN}$	1.8	2.0	2.2	mA
Sustain Current Matching Between Channels on Switch-to-Ground I/Os $\frac{I_{SUS(MAX)} - I_{SUS(MIN)}}{I_{SUS(MIN)}} \times 100$	I_{MATCH}	–	2.0	4.0	%
Input Offset Current When Selected as Analog	I_{OFFSET}	-2.0	1.4	2.0	µA
Input Offset Voltage When Selected as Analog $V_{(SP\&SGINPUTS)}$ to AMUX Output	V_{OFFSET}	 -10	 2.5	 10	mV
Analog Operational Amplifier Output Voltage Sink 250 µA	V_{OL}	 –	 10	 30	mV
Analog Operational Amplifier Output Voltage Source 250 µA	V_{OH}	 V_{DD} -0.1	 –	 –	V
Switch Detection Threshold	V_{TH}	3.70	4.0	4.3	V
Switch Input Voltage Range 33972 33972A	V_{IN}	 -14 -14	 – –	 38 40	V
Temperature Monitor[9], [10]	T_{LIM}	155	–	185	°C
Temperature Monitor Hysteresis[10]	$T_{LIM(HYS)}$	5.0	10	15	°C

Notes

7. T_C is the T_{CASE} of the package
8. Device operational. Table parameters may be out of specification.
9. Thermal shutdown of 16 mA pull-up and pulldown current sources only. 2.0 mA current source/sink and all other functions remain active.
10. This parameter is guaranteed by design but is not production tested.

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Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.1 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{PWR} ≤ 16 V, -40 °C ≤ T_C ≤ 125 °C, unless otherwise noted.(7) Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 13 V, T_A = 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE					
Input Logic Voltage Thresholds[11]	$V_{INLOGIC}$	0.8	–	2.2	V
SCLK, SI, Tri-state SO Input Current 0 V to V_{DD}	I_{SCLK}, I_{SI}, $I_{SO(TRI)}$	-10	–	10	µA
$\overline{CS}$ Input Current $\overline{CS}$ = V_{DD}	$I_{\overline{CS}}$	-10	–	10	µA
$\overline{CS}$ Pull-up Current $\overline{CS}$ = 0 V	$I_{\overline{CS}}$	30	–	100	µA
SO High-state Output Voltage $I_{SO(HIGH)}$ = -200 µA	$V_{SO(HIGH)}$	V_{DD} -0.8	–	V_{DD}	V
SO Low-state Output Voltage $I_{SO(HIGH)}$ = 1.6mA	$V_{SO(LOW)}$	–	–	0.4	V
Input Capacitance on SCLK, SI, Tri-state SO[12]	C_{IN}	–	–	20	pF
$\overline{INT}$ Internal Pull-up Current	–	15	40	100	µA
$\overline{INT}$ Voltage $\overline{INT}$ = Open Circuit	$V_{\overline{INT}(HIGH)}$	V_{DD} -0.5	–	V_{DD}	V
$\overline{INT}$ Voltage $I_{\overline{INT}}$ = 1.0 mA	$V_{\overline{INT}(LOW)}$	–	0.2	0.4	V
$\overline{WAKE}$ Internal Pull-up Current	$I_{\overline{WAKE}(PU)}$	20	40	100	µA
$\overline{WAKE}$ Voltage $\overline{WAKE}$ = Open Circuit	$V_{\overline{WAKE}(HIGH)}$	4.0	4.3	5.3	V
$\overline{WAKE}$ Voltage $I_{\overline{WAKE}}$ = 1.0 mA	$V_{\overline{WAKE}(LOW)}$	–	0.2	0.4	V
$\overline{WAKE}$ Voltage Maximum Voltage Applied to $\overline{WAKE}$ Through External Pull-up	$V_{\overline{WAKE}(MAX)}$	–	–	40	V

Notes

11. Upper and lower logic threshold voltage levels apply to SI, $\overline{CS}$, and SCLK.
12. This parameter is guaranteed by design but is not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. Dynamic Electrical Characteristics

Characteristics noted under conditions 3.1 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{PWR} ≤ 16 V, -40 °C ≤ T_C ≤ 125 °C, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 13 V, T_A = 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
SWITCH INPUT					
Pulse Wetting Current Time	$t_{PULSE(ON)}$	15	16	20	ms
Interrupt Delay Time Normal Mode	$t_{INT-DLY}$	–	5.0	16	µs
Sleep Mode Switch Scan Time	t_{SCAN}	100	200	300	µs
Calibrated Scan Timer Accuracy Sleep Mode	$t_{SCAN TIMER}$	–	–	10	%
Calibrated Interrupt Timer Accuracy Sleep Mode	$t_{INT TIMER}$	–	–	10	%
DIGITAL INTERFACE TIMING[13]					
Required Low-state Duration on V_{PWR} for Reset[14] V_{PWR} ≤ 0.2 V	t_{RESET}	–	–	10	µs
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK Required Set-up Time	t_{LEAD}	100	–	–	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$ Required Set-up Time	t_{LAG}	50	–	–	ns
SI to Falling Edge of SCLK Required Set-up Time	$t_{SI(SU)}$	16	–	–	ns
Falling Edge of SCLK to SI Required Hold Time	$t_{SI(HOLD)}$	20	–	–	ns
SI, $\overline{CS}$, SCLK Signal Rise Time[15]	$t_{R(SI)}$	–	5.0	–	ns
SI, $\overline{CS}$, SCLK Signal Fall Time[15]	$t_{F(SI)}$	–	5.0	–	ns
Time from Falling Edge of $\overline{CS}$ to SO Low-impedance[16]	$t_{SO(EN)}$	–	–	55	ns
Time from Rising Edge of $\overline{CS}$ to SO High-impedance[17]	$t_{SO(DIS)}$	–	–	55	ns
Time from Rising Edge of SCLK to SO Data Valid[18]	t_{VALID}	–	25	55	ns

Notes
13. These parameters are guaranteed by design. Production test equipment uses 4.16 MHz, 5.0 V SPI interface.
14. This parameter is guaranteed by design but not production tested.
15. Rise and Fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
16. Time required for valid output status data to be available on SO pin.
17. Time required for output states data to be terminated at SO pin.
18. Time required to obtain valid data out from SO following the rise of SCLK with 200 pF load.

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TIMING DIAGRAMS

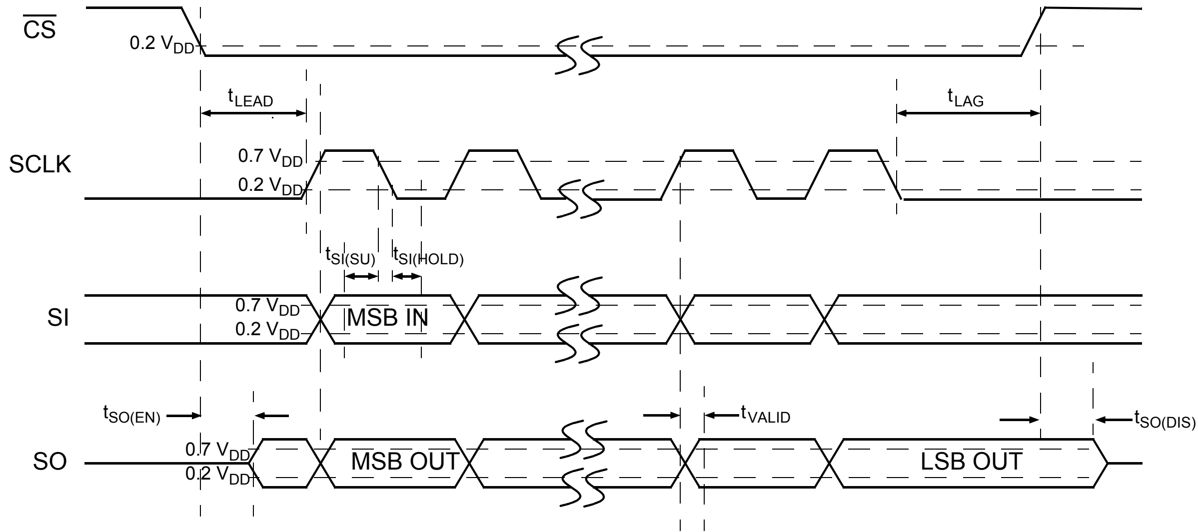

Figure 4. SPI Timing Characteristics

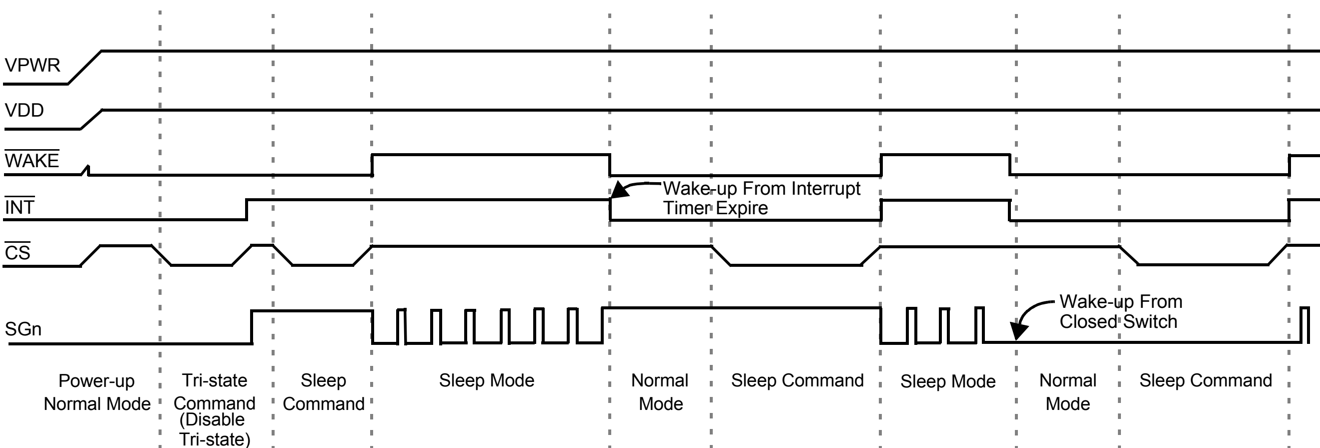

Figure 5. Sleep Mode to Normal Mode Operation

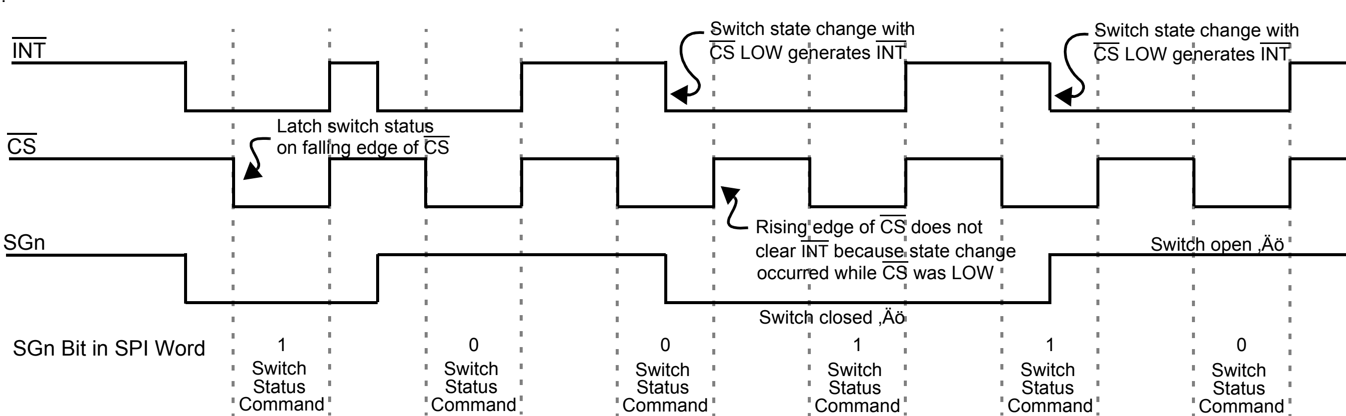

Figure 6. Normal Mode Interrupt Operation

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FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33972 device is an integrated circuit designed to provide systems with ultra-low quiescent sleep/wake-up modes, and a robust interface between switch contacts and a microprocessor. The 33972 replaces many of the discrete components required when interfacing to microprocessor-based systems, while providing switch ground offset protection, contact wetting current, and a system wake-up.

The 33972 features 8-programmable switch-to-ground or switch-to-battery inputs and 14 switch-to-ground inputs. All switch inputs may be read as analog inputs through the analog multiplexer (AMUX). Other features include a programmable wake-up timer, programmable interrupt timer, programmable wake-up/interrupt bits, and programmable wetting current settings.

This device is designed primarily for automotive applications, but may be used in a variety of other applications such as computer, telecommunications, and industrial controls.

FUNCTIONAL PIN DESCRIPTION

CHIP SELECT (CS)

The system MCU selects the 33972 to receive communication using the chip select (CS) pin. With the CS in a logic LOW state, command words may be sent to the 33972 via the serial input (SI) pin, and switch status information can be received by the MCU via the serial output (SO) pin. The falling edge of CS enables the SO output, latches the state of the INT pin, and the state of the external switch inputs.

Rising edge of the CS initiates the following operation:

1. Disables the SO driver (high-impedance)
2. INT pin is reset to logic [1], except when additional switch changes occur during CS LOW. (See Figure 6 on page 9.)
3. Activates the received command word, allowing the 33972 to act upon new data from switch inputs.

To avoid any spurious data, it is essential the HIGH-to-LOW and LOW-to-HIGH transitions of the CS signal occur only when SCLK is in a logic LOW state. A clean CS is needed to ensure no incomplete SPI words are sent to the device. Internal to the 33972 device is an active pull-up to V_{DD} on CS.

In Sleep mode, the negative edge of CS (V_{DD} applied) will wake up the 33972 device. Data received from the device during CS wake-up may not be accurate.

SYSTEM CLOCK (SCLK)

The system clock (SCLK) pin clocks the internal shift register of the 33972. The SI data is latched into the input shift register on the falling edge of SCLK signal. The SO pin shifts the switch status bits out on the rising edge of SCLK. The SO data is available for the MCU to read on the falling edge of SCLK. False clocking of the shift register must be avoided to ensure validity of data. It is essential the SCLK pin be in a logic LOW state whenever CS makes any transition. For this reason, it is recommended, that the SCLK pin is commanded to a logic LOW state as long as the device is not accessed and CS is in a logic HIGH state. When the CS is in a logic HIGH state, any signal on the SCLK and SI pins will be ignored and the SO pin is tri-state.

SPI SLAVE IN (SI)

The SI pin is used for serial instruction data input. SI information is latched into the input register on the falling edge of SCLK. A logic HIGH state present on SI will program a *one* in the command word on the rising edge of the CS signal. To program a complete word, 24 bits of information must be entered into the device.

SPI SLAVE OUT (SO)

The SO pin is the output from the shift register. The SO pin remains tri-stated until the CS pin transitions to a logic LOW state. All open switches are reported as zero, all closed switches are reported as one. The negative transition of CS enables the SO driver.

The first positive transition of SCLK will make the status data bit 24 available on the SO pin. Each successive positive clock will make the next status data bit available for the MCU to read on the falling edge of SCLK. The SI/SO shifting of the data follows a first-in, first-out protocol, with both input and output words transferring the most significant bit (MSB) first.

INTERRUPT (INT)

The INT pin is an interrupt output from the 33972 device. The INT pin is an open-drain output with an internal pull-up to V_{DD}. In Normal mode, a switch state change will trigger the INT pin (when enabled). The INT pin and INT bit in the SPI register are latched on the falling edge of CS. This permits the MCU to determine the origin of the interrupt. When two 33972 devices are used, only the device initiating the interrupt will have the INT bit set. The INT pin is cleared on the rising edge of CS. The INT pin will not clear with rising edge of CS if a switch contact change has occurred while CS was LOW.

In a multiple 33972 device system with WAKE HIGH and V_{DD} in (Sleep Mode), the falling edge of INT will place all 33972s in Normal mode.

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WAKE-UP (WAKE)

The WAKE pin is an open-drain output and a wake-up input. The pin is designed to control a power supply Enable pin. In the Normal mode, the WAKE pin is LOW. In the Sleep mode, the WAKE pin is HIGH. The WAKE pin has a pull-up to the internal +5.0 V supply.

In Sleep mode with the WAKE pin HIGH, the falling edge of WAKE will place the 33972 in Normal mode. In Sleep mode with V_{DD} applied, the INT pin must be HIGH for negative edge of WAKE to wake up the device. If V_{DD} is not applied to the device in Sleep mode, INT does not affect WAKE operation.

BATTERY INPUT (VPWR)

The VPWR pin is battery input and Power-ON Reset to the 33972 IC. The VPWR pin requires external reverse battery and transient protection. Maximum input voltage on VPWR is 50 V. All wetting, sustain, and internal logic current is provided from the VPWR pin.

VOLTAGE DRAIN SUPPLY (VDD)

The VDD input pin is used to determine logic levels on the microprocessor interface (SPI) pins. Current from VDD is used to drive SO output and the pull-up current for CS and INT pins. VDD must be applied for wake-up from negative edge of CS or INT.

GROUND (GND)

The GND pin provides ground for the IC as well as ground for inputs programmed as switch-to-battery inputs.

PROGRAMMABLE SWITCHES (SP0:SP7)

The 33972 device has 8 switch inputs capable of being programmed to read switch-to-ground or switch-to-battery contacts. The input is compared with a 4.0 V reference. When programmed to be switch-to-battery, voltages greater than 4.0 V are considered closed. Voltages less than 4.0 V are considered open. The opposite holds true when inputs are programmed as switch-to-ground. Programming features are defined in Table 6 through Table 11 in the Functional Device Operation section of this datasheet beginning on page 13. Voltages greater than the VPWR supply voltage will source current through the SP inputs to the VPWR pin. Transient battery voltages greater than 38/40 V must be clamped by an external device. This is not a normal operating condition and can damage the IC.

SWITCH-TO-GROUND INPUTS (SG0:SG13)

The SGn pins are switch-to-ground inputs only. The input is compared with a 4.0 V reference. Voltages greater than 4.0 V are considered open. Voltages less than 4.0 V are considered closed. Programming features are defined in Table 6 through Table 11 in the Functional Device Operation section of this datasheet beginning on page 13. Voltages greater than the VPWR supply voltage will source current through the SG inputs to the VPWR pin. Transient battery voltages greater than 40 V must be clamped by an external device. This is not a normal operating condition and can damage the IC.

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FUNCTIONAL INTERNAL BLOCK DESCRIPTION

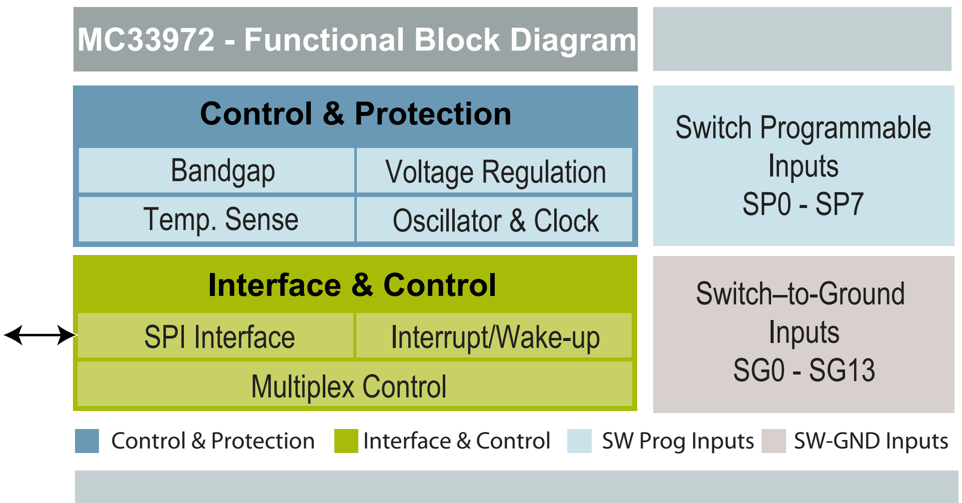

Figure 7. Functional Internal Block Description

CONTROL AND PROTECTION CIRCUITRY:

The 33972 is designed to operate from 5.5 V to 38/40 V on the VPWR terminal. Characteristics are provided for V_{PWR} from 8.0 to 26 V for the IC (parametric tests are done from 8.0 to 16.0v). Switch contact currents and the internal logic supply are generated from the VPWR terminal. The VDD supply terminal is used to set the SPI communication voltage levels, current source for the SO driver, and pull-up current on $\overline{\text{INT}}$ and $\overline{\text{CS}}$.

The on-chip voltage regulator and bandgap supplies the required voltages to the internal monitor circuitry. The temperature monitor is active in the Normal mode.

INTERFACE AND CONTROL:

The 33972 Multiple Switch Detection Interface with Suppressed Wake-up is designed to detect the closing and opening of up to 22 switch contacts. The switch status, either open or closed, is transferred to the microprocessor unit (MCU) through a serial peripheral interface (SPI).

The device also features a 22-to-1 analog multiplexer for reading inputs as analog. The 33972 device has two modes of operation, Normal and Sleep.

SWITCH PROGRAMMABLE INPUTS:

Programmable switch detection inputs. These 8 inputs can selectively detect switch closures to Ground or Battery. The 33972 device has 8 switch inputs capable of being programmed to read switch-to-ground or switch-to-battery contacts. The input is compared with a 4.0 V reference. When programmed to be switch-to-battery, voltages greater than 4.0 V are considered closed. Voltages less than 4.0 V are considered open. The opposite holds true when inputs are programmed as switch-to-ground.

SWITCH–TO-GROUND INPUTS:

Switch detection interface inputs. These 14 inputs can detect switch closures to ground only. The input is compared with a 4.0 V reference. Voltages greater than 4.0 V are considered open. Voltages less than 4.0 V are considered closed. Note: Each of these inputs may be used to supply current to sensors external to a module.

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FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

MCU INTERFACE DESCRIPTION

The 33972 device directly interfaces to a 3.3 or 5.0 V microcontroller unit (MCU). SPI serial clock frequencies up to 6.0 MHz may be used for programming and reading switch input status (production tested at 4.16 MHz). Figure 8 illustrates the configuration between an MCU and one 33972.

Serial peripheral interface (SPI) data is sent to the 33972 device through the SI input pin. As data is being clocked into the SI pin, status information is being clocked out of the device by the SO output pin. The response to a SPI command will always return the switch status, interrupt flag, and thermal flag. Input switch states are latched into the SO register on the falling edge of the chip select (CS) pin. Twenty-four bits are required to complete a transfer of information between the 33972 and the MCU.

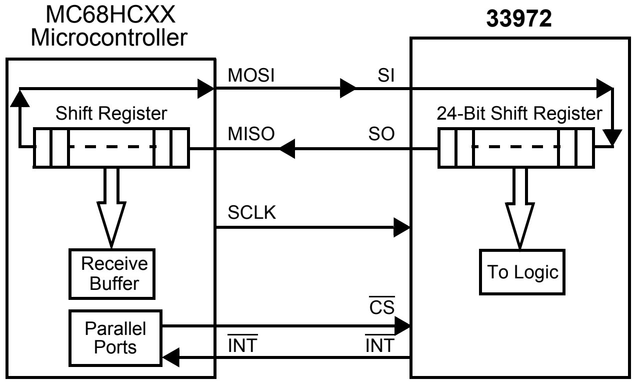

Figure 8. SPI Interface with Microprocessor

Two or more 33972 devices may be used in a module system. Multiple ICs may be SPI-configured in parallel or serial. Figures 9 and 10 show the configurations. When using the serial configuration, 48-clock cycles are required to transfer data in/out of the ICs.

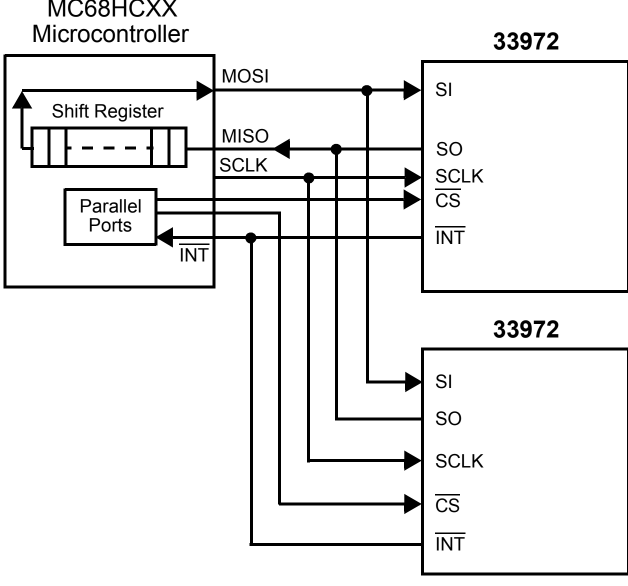

Figure 9. SPI Parallel Interface with Microprocessor

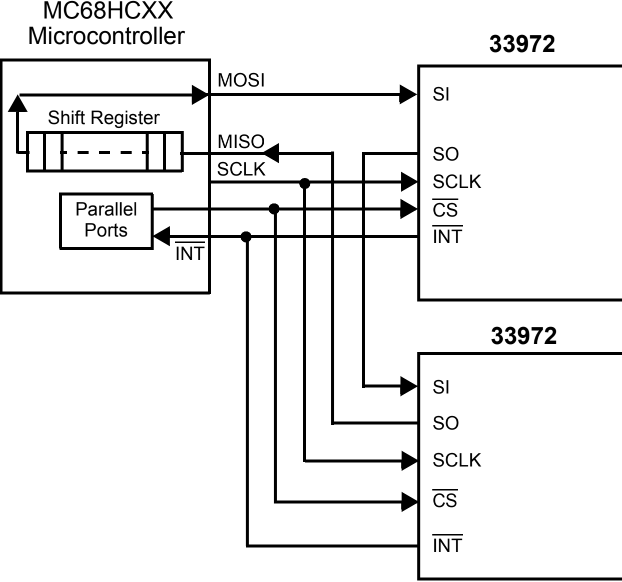

Figure 10. SPI Serial Interface with Microprocessor

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POWER SUPPLY

The 33972 is designed to operate from 5.5 to 40 V on the VPWR pin. Characteristics are provided from 8.0 to 16 V for the device. Switch contact currents and the internal logic supply are generated from the VPWR pin. The VDD supply pin is used to set the SPI communication voltage levels, current source for the SO driver, and pull-up current on INT and CS.

The VDD supply may be removed from the device to reduce quiescent current. If V_{DD} is removed while the device is in Normal mode, the device will remain in Normal mode. If V_{DD} is removed in Sleep mode, the device will remain in Sleep mode until a wake-up input is received (WAKE HIGH to LOW, switch input or interrupt timer expires).

Removing V_{DD} from the device disables SPI communication and will not allow the device to wake up from INT and CS pins.

POWER-ON RESET (POR)

Applying V_{PWR} to the device will cause a Power-ON Reset and place the device in Normal mode.

Default settings from Power-ON Reset via V_{PWR} or the Reset Command are as follows:

- Programmable switch – set to switch to battery
- All inputs set as wake-up
- Wetting current on (16 mA)
- Wetting current timer on (20 ms)
- All inputs tri-state
- Analog select 00000 (no input channel selected)

NORMAL AND SLEEP MODES

The 33972 has two operating modes, Normal mode and Sleep mode. A discussion on Normal mode begins below. A discussion on Sleep mode begins on page 19.

Normal Mode

Normal mode may be entered by the following events:

- Application of V_{PWR} to the IC
- Change-of-switch state (when enabled)
- Falling edge of WAKE
- Falling edge of INT (with V_{DD} = 5.0 V and WAKE at Logic [1])
- Falling edge of CS (with V_{DD} = 5.0 V)
- Interrupt timer expires

Only in Normal mode with V_{DD} applied can the registers of the 33972 be programmed through the SPI.

The registers that may be programmed in Normal mode are listed below. Further explanation of each register is provided in subsequent paragraphs.

- Programmable Switch Register (*Settings Command*)
- Wake-Up/Interrupt Register (*Wake-up/Interrupt Command*)
- Wetting Current Register (*Metallic Command*)
- Wetting Current Timer Register (*Wetting Current Timer Enable Command*)
- Tri-State Register (*Tri-state Command*)
- Analog Select Register (*Analog Command*)
- Calibration of Timers (*Calibration Command*)
- Reset (*Reset Command*)

Figure 6, page 9, is a graphical description of the device operation in Normal mode. Switch states are latched into the input register on the falling edge of CS. The INT to the MCU is cleared on the rising edge of CS. However, INT will not clear on rising edge of CS if a switch has closed during SPI communication (CS LOW). This prevents switch states from being missed by the MCU.

PROGRAMMABLE SWITCH REGISTER

Inputs SP0 to SP7 may be programmable for switch-to-battery or switch-to-ground. These inputs types are defined using the *settings command* (Table 6). To set an SPn input for switch-to-battery, a logic [1] for the appropriate bit must be set. To set an SPn input for switch-to-ground, a logic [0] for the appropriate bit must be set. The MCU may change or update the programmable switch register via software at any time in Normal mode. Regardless of the setting, when the SPn input switch is closed a logic [1] will be placed in the serial output response register (Table 17, page 19).

Table 6. Settings Command

Settings Command								Not used								Battery/Ground Select							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1	X	X	X	X	X	X	X	X	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0

WAKE-UP/INTERRUPT REGISTER

The wake-up/interrupt register defines the inputs that are allowed to wake the 33972 from Sleep Mode or set the INT pin LOW in Normal mode. Programming the wake-up/interrupt bit to logic [0] will disable the specific input from generating an interrupt and will disable the specific input from waking the IC in Sleep mode (Table 7). Programming the wake-up/interrupt bit to logic [1] will enable the specific input to generate an interrupt with switch change of state and will enable the specific input as wake-up. The MCU may change or update the wake-up/interrupt register via software at any time in Normal mode.

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Table 7. Wake-up/Interrupt Command

Wake-up/Interrupt Command								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	X	X	X	X	X	X	X	X	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0
0	0	0	0	0	0	1	1	X	X	sg13	sg12	sg11	sg10	sg9	sg8	sg7	sg6	sg5	sg4	sg3	sg2	sg1	sg0

WETTING CURRENT REGISTER

The 33972 has two levels of switch contact current, 16 and 2.0 mA (see Figure 11). The metallic command is used to set the switch contact current level (Table 8). Programming the metallic bit to logic [0] will set the switch wetting current to 2.0 mA. Programming the metallic bit to logic [1] will set the switch contact wetting current to 16 mA. The MCU may change or update the wetting current register via software at any time in Normal mode.

Wetting current is designed to provide higher levels of current during switch closure. The higher level of current is designed to keep switch contacts from building up oxides that form on the switch contact surface.

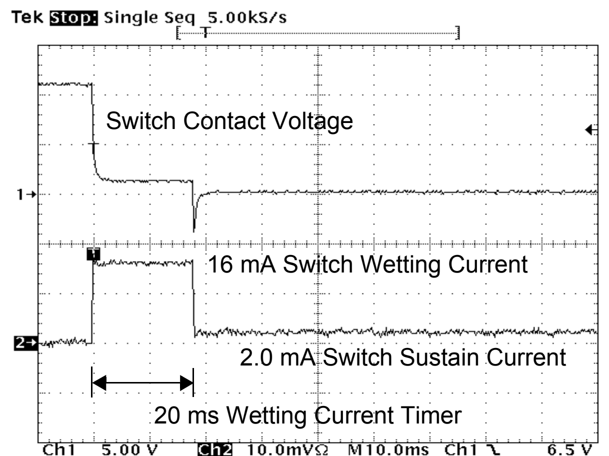

Figure 11. Contact Wetting and Sustain Current

Table 8. Metallic Command

Metallic Command								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	X	X	X	X	X	X	X	X	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0
0	0	0	0	0	1	0	1	X	X	sg13	sg12	sg11	sg10	sg9	sg8	sg7	sg6	sg5	sg4	sg3	sg2	sg1	sg0

WETTING CURRENT TIMER REGISTER

Each switch input has a designated 20 ms timer. The timer starts when the specific switch input crosses the comparator threshold (4.0 V). When the 20 ms timer expires, the contact current is reduced from 16 to 2.0 mA. The wetting current timer may be disabled for a specific input. When the timer is disabled, 16 mA of current will continue to flow through the closed switch contact. With multiple wetting current timers disabled, power dissipation for the IC must be considered.

The MCU may change or update the wetting current timer register via software at any time in Normal mode. This allows the MCU to control the amount of time wetting current is applied to the switch contact. Programming the wetting current timer bit to logic [0] will disable the wetting current timer. Programming the wetting current timer bit to logic [1] will enable the wetting current timer (Table 9).

Table 9. Wetting Current Timer Enable Command

Wetting Current Timer Commands								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	1	X	X	X	X	X	X	X	X	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0
0	0	0	0	1	0	0	0	X	X	sg13	sg12	sg11	sg10	sg9	sg8	sg7	sg6	sg5	sg4	sg3	sg2	sg1	sg0

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TRI-STATE REGISTER

The tri-state command is use to set the SPn or SGn input node as high-impedance (Table 10). By setting the tri-state register bit to logic [1], the input will be high-impedance regardless of the metallic command setting. The comparator on each input remains active. This command allows the use of each input as a comparator with a 4.0 V threshold. The MCU may change or update the tri-state register via software at any time in Normal mode.

Table 10. Tri-State Command

Tri-State Commands								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	1	X	X	X	X	X	X	X	X	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0
0	0	0	0	1	0	1	0	X	X	sg13	sg12	sg11	sg10	sg9	sg8	sg7	sg6	sg5	sg4	sg3	sg2	sg1	sg0

ANALOG SELECT REGISTER

The analog voltage on switch inputs may be read by the MCU using the analog command (Table 11). Internal to the IC is a 22-to-1 analog multiplexer. The voltage present on the selected input pin is buffered and made available on the AMUX output pin. The AMUX output pin is clamped to a maximum of VDD volts regardless of the higher voltages present on the input pin. After an input has been selected as the analog, the corresponding bit in the next SO data stream will be logic [0]. When selecting a channel to be read as analog, the user must also set the desired current (16 mA, 2.0 mA, or high-impedance). Setting bit 6 and bit 5 to 0,0 selects the input as high-impedance. Setting bit 6 and bit 5 to 0,1 selects 2.0 mA, and 1,0 selects 16 mA. Setting bit 6 and bit 5 to 1,1 in the analog select register is not allowed and will place the input as an analog input with high-impedance.

Analog currents set by the analog command are pull-up currents for all SGn and SPn inputs (Table 11). The analog command does not allow pull-down currents on the SPn inputs. Setting the current to 16 or 2.0 mA may be useful for reading sensor inputs. Further information is provided in the Typical Applications section of this datasheet beginning on page 21. The MCU may change or update the analog select register via software at any time in Normal mode.

Table 11. Analog Command

Analog Command								Not used									Current Select		Analog Channel Select				
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	0	X	X	X	X	X	X	X	X	X	16 mA	2.0 mA	0	0	0	0	0

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Table 12. Analog Channel

Bits 43210	Analog Channel Select
00000	No Input Selected
00001	SG0
00010	SG1
00011	SG2
00100	SG3
00101	SG4
00110	SG5
00111	SG6
01000	SG7
01001	SG8
01010	SG9
01011	SG10
01100	SG11
01101	SG12
01110	SG13
01111	SP0
10000	SP1
10001	SP2
10010	SP3
10011	SP4
10100	SP5
10101	SP6
10110	SP7

CALIBRATION OF TIMERS

In cases where an accurate time base is required, the user may calibrate the internal timers using the calibration command (Table 13). After the 33972 device receives the calibration command, the device expects 512 μs logic [0] calibration pulse on the $\overline{CS}$ pin. The pulse is used to calibrate the internal clock. No other SPI pins should transition during this 512 μs calibration pulse. Because the oscillator frequency changes with temperature, calibration is required for an accurate time base. Calibrating the timers has no affect on the quiescent current measurement. The calibration command simply makes the time base more accurate. The calibration command may be used to update the device on a periodic basis.

Table 13. Calibration Command

Calibration Command								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

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RESET

The reset command resets all registers to Power-ON Reset (POR) state. Refer to Table 15, page 18, for POR states or the paragraph entitled Power-ON Reset (POR) on page 14 of this datasheet.

Table 14. Reset Command

Reset Command								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

SPI COMMAND SUMMARY

Table 15 below provides a comprehensive list of SPI commands recognized by the 33972 and the reset state of each register. Table 16 and Table 17 contain the serial output (SO) data for input voltages greater or less than the threshold level. Open switches are always indicated with a logic [0], closed switches are indicated with logic [1].

Table 15. SPI Command Summary

	MSB		Command Bits						Setting Bits															LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Switch Status Command	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Settings Command Bat=1, Gnd=0 (Default state = 1)	0	0	0	0	0	0	0	1	X	X	X	X	X	X	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Wake-Up/Interrupt Bit Wake-Up=1 Non-Wake-Up=0 (Default state = 1)	0	0	0	0	0	0	1	0	X	X	X	X	X	X	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
	0	0	0	0	0	0	1	1	X	X	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Metallic Command Metallic = 1 Non-metallic = 0 (Default state = 1)	0	0	0	0	0	1	0	0	X	X	X	X	X	X	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
	0	0	0	0	0	1	0	1	X	X	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Analog Command	0	0	0	0	0	1	1	0	X	X	X	X	X	X	X	X	X	16mA 0	2.0mA 0	0	0	0	0	0
Wetting Current Timer Enable Command Timer ON = 1 Timer OFF = 0 (Default state = 1)	0	0	0	0	0	1	1	1	X	X	X	X	X	X	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
	0	0	0	0	1	0	0	0	X	X	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Tri-State Command Input Tri-State=1 Input Active = 0 (Default state = 1)	0	0	0	0	1	0	0	1	X	X	X	X	X	X	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
	0	0	0	0	1	0	1	0	X	X	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Calibration Command (Default state – uncalibrated)	0	0	0	0	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Sleep Command (Refer to Sleep Mode on page 19.)	0	0	0	0	1	1	0	0	X	X	X	X	X	X	X	X	X	X	int timer	int timer	int timer	scan timer	scan timer	scan timer
Reset Command	0	1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
SO Response Will Always Send	therm flg	int flg	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0

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Table 16. Serial Output (SO) Bit Data

Type of Input	Input Programmed	Voltage on Input Pin	SO SPI Bit
SP	Switch to Ground	SPn < 4.0V	1
	Switch to Ground	SPn > 4.0V	0
	Switch to Battery	SPn < 4.0V	0
	Switch to Battery	SPn > 4.0V	1
SG	N/A	SGn < 4.0V	1
	N/A	SGn > 4.0V	0

Table 17. Serial Output (SO) Response Register

SO Response Will Always Send	them flg	int flg	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0

EXAMPLE OF NORMAL MODE OPERATION

The operation of the device in Normal mode is defined by the states of the programmable internal control registers. A typical application may have the following settings:

- Programmable switch – set to switch-to-ground
- All inputs set as wake-up
- Wetting current on (16 mA)
- Wetting current timer on (20 ms)
- All inputs tri-state-disabled (comparator is active)
- Analog select 00000 (no input channel selected)

With the device programmed as above, an interrupt will be generated with each switch contact change of state (open-to-close or close-to-open) and 16 mA of contact wetting current will be source for 20 ms. The $\overline{INT}$ pin will remain LOW until switch status is acknowledged by the microprocessor. It is critical to understand $\overline{INT}$ will not be cleared on the rising edge of $\overline{CS}$ if a switch closure occurs while $\overline{CS}$ is LOW. The maximum duration a switch state change can exist without acknowledgement depends on the software response time to the interrupt. Figure 6, page 9, shows the interaction between changing input states and the $\overline{INT}$ and $\overline{CS}$ pins.

If desired the user may disable interrupts (wake up/ interrupt command) from the 33972 device and read the switch states on a periodic basis. Switch activation and deactivation faster than the MCU read rate will not be acknowledged.

The 33972 device will exit the Normal mode and enter the Sleep mode only with a valid sleep command.

SLEEP MODE

Sleep mode is used to reduce system quiescent currents. Sleep mode may be entered only by sending the sleep command. All register settings programmed in Normal mode will be maintained in Sleep mode.

The 33972 will exit Sleep mode and enter Normal mode when any of the following events occur:

- Input switch change of state (when enabled)
- Interrupt timer expire
- Falling edge of $\overline{WAKE}$
- Falling edge of $\overline{INT}$ (with V_{DD} = 5.0 V and $\overline{WAKE}$ at Logic [1])
- Falling edge of $\overline{CS}$ (with V_{DD} = 5.0 V)
- Power-ON Reset (POR)

The V_{DD} supply may be removed from the device during Sleep mode. However removing V_{DD} from the device in Sleep mode will disable a wake-up from falling edge of $\overline{INT}$ and $\overline{CS}$.

Note In cases where $\overline{CS}$ is used to wake the device, the first SO data message is not valid.

The sleep command contains settings for two programmable timers for Sleep mode, the interrupt timer and the scan timer, as shown in Table 18 The interrupt timer is used as a periodic wake-up timer. When the timer expires, an interrupt is generated and the device enters Normal mode.

Note The interrupt timer in the 33972 device may be disabled by programming the interrupt bits to logic [1 1 1].

Table 19 shows the programmable settings of the Interrupt timer.

Table 18. Sleep Command

Sleep Command								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0	X	X	X	X	X	X	X	X	X	X	int timer	int timer	int timer	scan timer	scan timer	scan timer

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Table 19. Interrupt Timer

Bits 543	Interrupt Period
000	32 ms
001	64 ms
010	128 ms
011	256 ms
100	512 ms
101	1.024 s
110	2.048 s
111	No interrupt wake-up

The scan timer sets the polling period between input switch reads in Sleep mode. The period is set in the sleep command and may be set to 000 (no period) to 111 (64 ms). In Sleep mode when the scan timer expires, inputs will behave as programmed prior to sleep command. The 33972 will wake up for approximately 125 μs and read the switch inputs. At the end of the 125 μs, the input switch states are compared with the switch state prior to sleep command. When switch state changes are detected, an interrupt is generated (when enabled; refer to wake-up/interrupt command description on page 15), and the device enters Normal mode. Without switch state changes, the 33972 will reset the scan timer, inputs become tri-state, and the Sleep mode continues until the scan timer expires again.

Table 20 shows the programmable settings of the Scan timer.

Table 20. Scan Timer

Bits 210	Scan Period
000	No Scan
001	1.0 ms
010	2.0 ms
011	4.0 ms
100	8.0 ms
101	16 ms
110	32 ms
111	64 ms

Note The interrupt and scan timers are disabled in the Normal Mode.

Figure 5, page 9, is a graphical description of how the 33972 device exits Sleep mode and enters Normal mode. Notice that the device will exit Sleep mode when the interrupt timer expires or when a switch change of state occurs. The falling edge of $\overline{INT}$ triggers the MCU to wake from Sleep state. Figure 12 illustrates the current consumed during Sleep mode. During the 125 μs, the device is fully active and switch states are read. The quiescent current is calculated by integrating the normal running current over scan period plus approximately 60 μA.

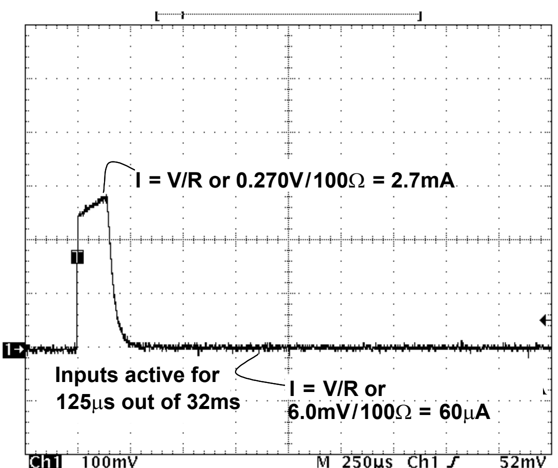

Figure 12. Sleep Current Waveform

TEMPERATURE MONITOR

With multiple switch inputs closed and the device programmed with the wetting current timers disabled, considerable power will be dissipated by the IC. For this reason, temperature monitoring has been implemented. The temperature monitor is active in the Normal mode only. When the IC temperature is above the thermal limit, the temperature monitor will do all of the following:

- Generate an interrupt.
- Force all 16 mA pull-up and pull-down current sources to revert to 2.0 mA current sources.
- Maintain the 2.0 mA current source and all other functionality.
- Set the thermal flag bit in the SPI output register.

The thermal flag bit in the SPI word will be cleared on rising edge of $\overline{CS}$ provided the die temperature has cooled below the thermal limit. When die temperature has cooled below thermal limit, the device will resume previously programmed settings.

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TYPICAL APPLICATIONS

INTRODUCTION

The 33972's primary function is the detection of open or closed switch contacts. However, there are many features that allow the device to be used in a variety of applications. The following is a list of applications to consider for the IC:

Sensor Power Supply

Switch Monitor for Metallic or Elastomeric Switches

Analog Sensor Inputs (Ratiometric)

Power MOSFET/LED Driver and Monitor

Multiple 33972 Devices in a Module System

The following paragraphs describe the applications in detail.

SENSOR POWER SUPPLY

Each input may be used to supply current to sensors external to a module. Many sensors such as Hall effect, pressure sensors, and temperature sensors require a supply voltage to power the sensor and provide an open collector or analog output. Figure 13 shows how the 33972 may be used to supply power and interface to these types of sensors. In an application where the input makes continuous transitions, consider using the wake-up/interrupt command to disable the interrupt for the particular input.

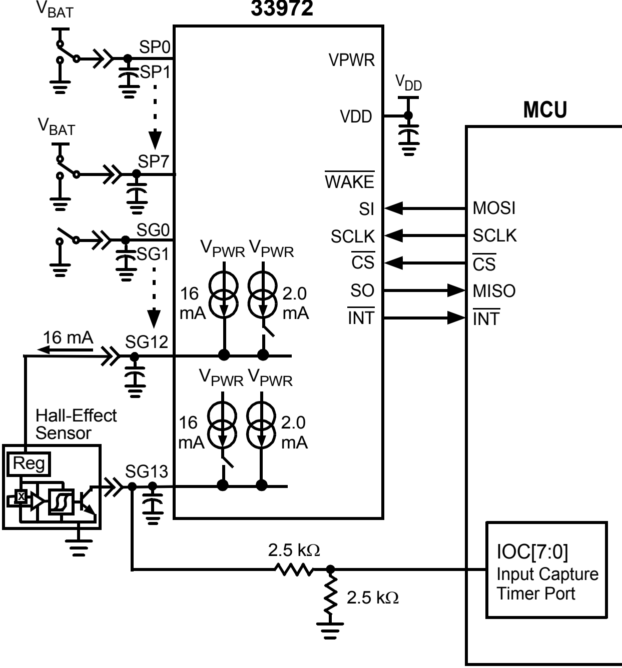

Figure 13. Sensor Power Supply

METALLIC/ELASTOMERIC SWITCH

Metallic switch contacts often develop higher contact resistance over time owing to contact corrosion. The corrosion is induced by humidity, salt, and other elements that exist in the environment. For this reason the 33972 provides two settings for contacts. When programmed for metallic switches, the device provides higher wetting current to keep switch contacts free of oxides. The higher current occurs for the first 20 ms of switch closure. Where longer duration of wetting current is desired, the user may send the wetting current timer command and disable the timer. Wetting current will be continuous to the closed switch. After the time period set by the MCU, the wetting current timer command may be sent again to enable the timer. The user must consider power dissipation on the device when disabling the timer. (Refer to the paragraph entitled Temperature Monitor, page 20.)

To increase the amount of wetting current for a switch contact, the user has two options. Higher wetting current to a switch may be achieved by paralleling SGn or SPn inputs. This will increase wetting current by 16 mA for each input added to the switch contact. The second option is to simply add an external resistor pull-up to the V_{PWR} supply for switch-to-ground inputs or a resistor to ground for a switch-to-battery input. Adding an external resistor has no effect on the operation of the device.

Elastomeric switch contacts are made of carbon and have a high contact resistance. Resistance of 1.0 kΩ is common. In applications with elastomeric switches, the pull-up and pulldown currents must be reduced to prevent excessive power dissipation at the contact. Programming for a lower current settings is provided in the Functional Device Operation section beginning on page 13 under Table 8, Metallic Command.

ANALOG SENSOR INPUTS (RATIOMETRIC)

The 33972 features a 22-to-1 analog multiplexer. Setting the binary code for a specific input in the analog command allows the microcontroller to perform analog to digital conversion on any of the 22 inputs. On rising edge of CS the multiplexer connects a requested input to the AMUX pin. The AMUX pin is clamped to max of VDD volts regardless of the higher voltages present on the input pin. After an input has been selected as the analog, the corresponding bit in the next SO data stream will be logic [0].

The input pin, when selected as analog, may be configured as analog with high-impedance, analog with 2.0 mA pull-up, or analog with 16 mA pull-up. Figure 14, page 22, shows how the 33972 may be used to provide a ratiometric reading of variable resistive input.

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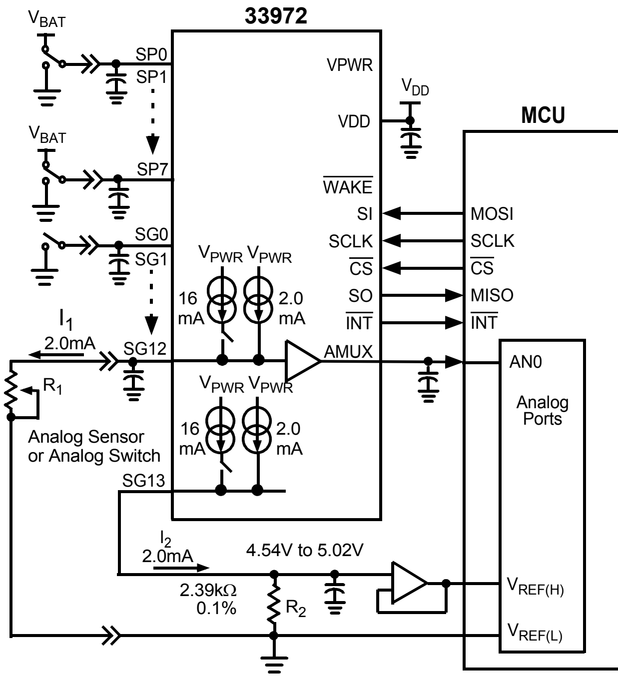

Figure 14. Analog Ratiometric Conversion

To read a potentiometer sensor, the wiper should be grounded and brought back to the module ground, as illustrated in Figure 14. With the wiper changing the impedance of the sensor, the analog voltage on the input will represent the position of the sensor.

Using the Analog feature to provide 2.0 mA of pull-up current to an analog sensor may induce error due to the accuracy of the current source. For this reason, a ratiometric conversion must be considered. Using two current sources (one for the sensor and one to set the reference voltage to the A/D converter) will yield a maximum error (owing to the 33972) of 4%.

Higher accuracy may be achieved through module level calibration. In this example, we use the resistor values from Figure 14 and assume the current sources are 4% from each other. The user may use the module end-of-line tester to calculate the error in the A/D conversion. By placing a 2.0 kΩ, 0.1% resistor in the end-of-line test equipment and assuming a perfect 2.0 mA current source from the 33972, a calculated A/D conversion may be obtained. Using the equation yields the following:

$$ADC = \frac{I1 \times R1}{I2 \times R2} \times 255$$

$$ADC = \frac{2.0mA \times 2.0k\Omega}{2.0mA \times 2.39k\Omega} \times 255$$

ADC = 213 counts

The ADC value of 213 counts is the value with 0% error (neglecting the resistor tolerance and AMUX input offset voltage). Now we can calculate the count value induced by the mismatch in current sources. From a sample device the maximum current source was measured at 2.05 mA and minimum current source was measured at 1.99 mA. This yields 3% error in A/D conversion. The A/D measurement will be as follows:

$$ADC = \frac{1.99mA \times 2.0k\Omega}{2.05mA \times 2.39k\Omega} \times 255$$

ADC = 207 counts

This A/D conversion is 3% low in value. The error correction factor of 1.03 may be used to correct the value:

ADC = 207 counts x 1.03

ADC = 213 counts

An error correction factor may then be stored in E^2 memory and used in the A/D calculation for the specific input. Each input used as analog measurement will have a dedicated calibrated error correction factor.

POWER MOSFET/LED DRIVER AND MONITOR

Because of the flexible programming of the 33972 device, it may be used to drive small loads like LEDs or MOSFET gates. It was specifically designed to power up in the Normal mode with the inputs tri-state. This was done to ensure the LEDs or MOSFETs connected to the 33972 power up in the off-state. The switch programmable inputs (SP0–SP7) have a source-and-sink capability, providing effective MOSFET gate control. To complete the circuit, a pull-down resistor should be used to keep the gate from floating during the Sleep modes. Figure 15, page 23, shows an application where the SG0 input is used to monitor the drain-to-source voltage of the external MOSFET. The 1.5 kΩ resistor is used to set the drain-to-source trip voltage. With the 2.0 mA current source enabled, an interrupt will be generated when the drain-to-source voltage is approximately 1.0 V.

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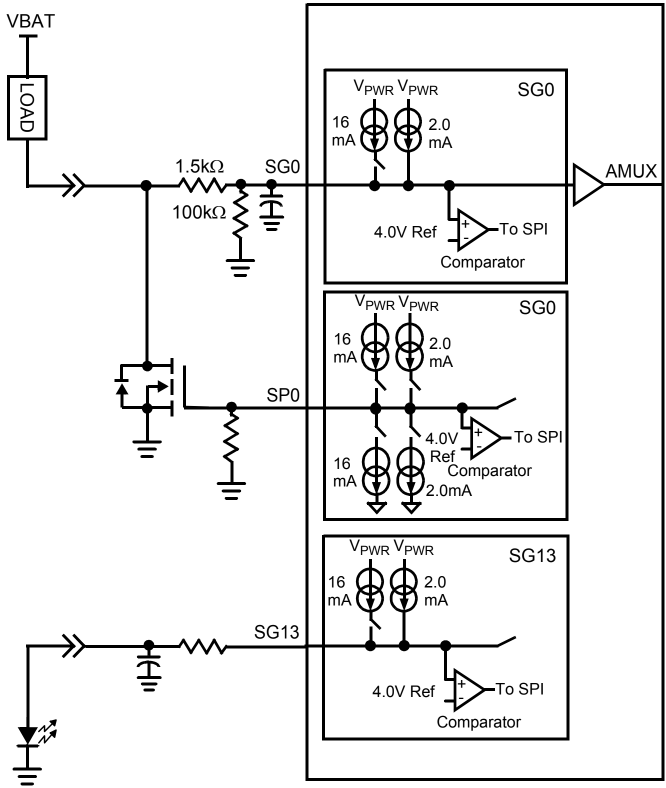

Figure 15. MOSFET or LED Driver Output

The sequence of commands (from Normal mode with inputs tri-state) required to set up the device to drive a MOSFET are as follows:

- wetting current timer enable command – Disable SPn wetting current timer (refer to Table 9, page 15).
- metallic command – Set SPn to 16 or 2.0 mA gate drive current (refer to Table 8, page 15).
- settings command – Set SPn as switch-to-battery (refer to Table 6, page 14).
- tri-state command – Disable tri-state for SPn (refer to Table 10, page 16).

After the tri-state command has been sent (tri-state disable), the MOSFET gate will be pulled to ground. From this point forward the MOSFET may be turned on and off by sending the settings command:

- settings command – SPn as switch-to-ground (MOSFET ON).
- settings command – SPn as switch-to-battery (MOSFET OFF).

Monitoring of the MOSFET drain in the OFF state provides open load detection. This is done by using an SGn input comparator. With the SGn input in tri-state, the load will pull up the SGn input to battery. With open load the SGn pin is pulled down to ground through an external resistor. The open load is indicated by a logic [1] in the SO data bit.

The analog command may be used to monitor the drain voltage in the MOSFET ON state. By sourcing 2.0 mA of current to the 1.5 kΩ resistor, the analog voltage on the SGn pin will be approximately:

$$V_{SGn} = I_{SGn} \times 1.5k\Omega + V_{DS}$$

As the voltage on the drain of the MOSFET increases, so does the voltage on the SGn pin. With the SGn pin selected as analog, the MCU may perform the A/D conversion.

Using this method for controlling unclamped inductive loads is not recommended. Inductive flyback voltages greater than V_{PWR} may damage the IC.

The SP0:SP7 pins of this device may also be used to send signals from one module to another. Operation is similar to the gate control of a MOSFET.

- For LED applications a resistor in series with the LED is recommended but not required. The switch-to-ground inputs are recommended for LED application. To drive the LED use the following commands:
- wetting current timer enable command – Disable SGn wetting current timer.
- metallic command – Set SGn to 16 mA.

From this point forward the LED may be turned on and off using the tri-state command:

- tri-state command – Disable tri-state for SGn (LED ON).
- tri-state command – Enable tri-state for SGn (LED OFF).

These parameters are easily programmed via SPI commands in Normal mode.

MULTIPLE 33972 DEVICES IN A MODULE SYSTEM

Connecting power to the 33972 and the MCU for Sleep mode operation may be done in several ways. Table 21 shows several system configurations for power between the MCU and the 33972 and their specific requirements for functionality.

Table 21. Sleep Mode Power Supply

MCU V_{DD}	33972 V_{DD}	Comments
5.0 V	5.0 V	All wake-up conditions apply. (Refer to Sleep Mode, page 19.)
5.0 V	0 V	SPI wake-up is not possible.
0 V	5.0 V	Sleep mode not possible. Current from $\overline{CS}$ pull-up will flow through MCU to V_{DD} that has been switched off. Negative edge of $\overline{CS}$ will put 33972 in Normal mode.
0 V	0 V	SPI wake-up is not possible.

Multiple 33972 devices may be used in a module system. SPI control may be done in parallel or serial. However when parallel mode is used, each device is addressed independently (refer to MCU Interface Description, page 13). Therefore when sending the sleep command, one device will enter sleep before the other. For multiple devices in a system, it is recommended that the devices are controlled in serial (S0

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from first device is connected to SI of second device). With two devices, 48 clock pulses are required to shift data in. When the WAKE feature is used to enable the power supply, both WAKE pins should be connected to the enable pin on the power supply. The INT pins may be connected to one interrupt pin on the MCU or may have their own dedicated interrupt to the MCU.

The transition from Normal to Sleep mode is done by sending the sleep command. With the devices connected in serial and the sleep command sent, both will enter Sleep mode on the rising edge of CS. When Sleep mode is entered, the WAKE pin will be logic [1]. If either device wakes up, the WAKE pin will transition LOW, waking the other device.

A condition exists where the MCU is sending the sleep command (CS logic [0]) and a switch input changes state. With this event the device that detects this input will not transition to Sleep mode, while the second device will enter Sleep mode. In this case two switch status commands must be sent to receive accurate switch status data. The first switch status command will wake the device in Sleep mode. Switch status data may not be valid from the first switch status command because of the time required for the input voltage to rise above the 4.0 V input comparator threshold. This time is dependant on the impedance of SGn or SPn node. The second switch status command will provide accurate switch status information. It is recommended that software wait 10 to 20 ms between the two switch status commands, allowing time for switch input voltages to stabilize. With all switch states acknowledged by the MCU, the sleep sequence may be initiated. All parameters for Sleep mode should be updated prior to sending the sleep command.

The 33972 IC has an internal 5.0 V supply from the VPWR pin. A POR circuit monitors the internal 5.0 V supply. In the event of transients on the VPWR pin, an internal reset may occur. Upon reset the 33972 will enter Normal mode with the internal registers as defined in Table 15, page 18. Therefore it is recommended that the MCU periodically update all registers internal to the IC.

USING THE WAKE FEATURE

The 33972 provides a WAKE output and wake-up input designed to control an enable pin on system power supply. While in the Normal mode, the WAKE output is LOW, enabling the power supply. In the Sleep mode, the WAKE pin is high, disabling the power supply. The WAKE pin has a passive pull-up to the internal 5.0 V supply but may be pulled up through a resistor to the V_{PWR} supply (see Figure 17, page 25)

When the WAKE output is not used, the pin should be pulled up to the V_{DD} supply through a resistor as shown in Figure 16, page 25.

During the Sleep mode, a switch closure will set the WAKE pin LOW, causing the 33972 to enter the Normal mode. The power supply will then be activated, supplying power to the VDD pin and the microprocessor and the 33972. The microprocessor can determine the source of the wake-up by reading the interrupt flag.

COST AND FLEXIBILITY

Systems requiring a significant number of switch interfaces have many discrete components. Discrete components on standard PWB consume board space and must be checked for solder joint integrity. An integrated approach reduces solder joints, consumes less board space, and offers wider operating voltage, analog interface capability, and greater interfacing flexibility.

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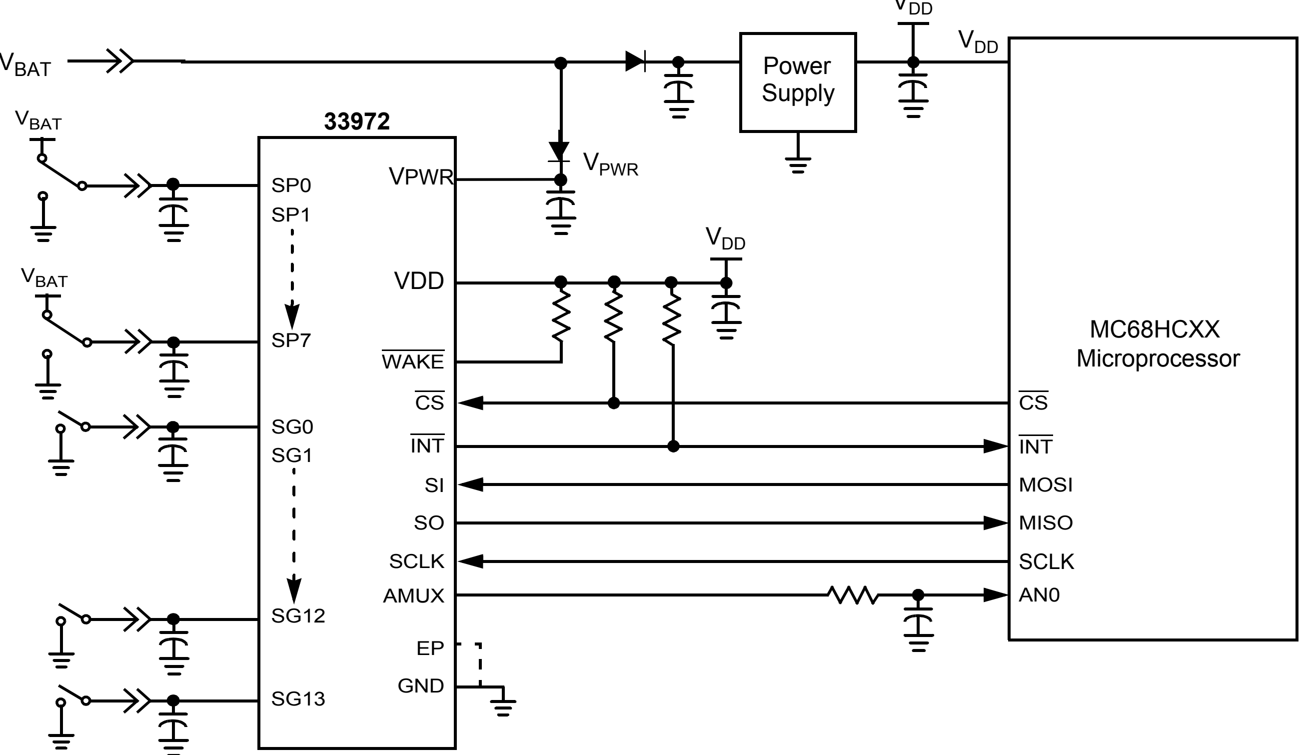


Figure 16. Power Supply Active in Sleep Mode

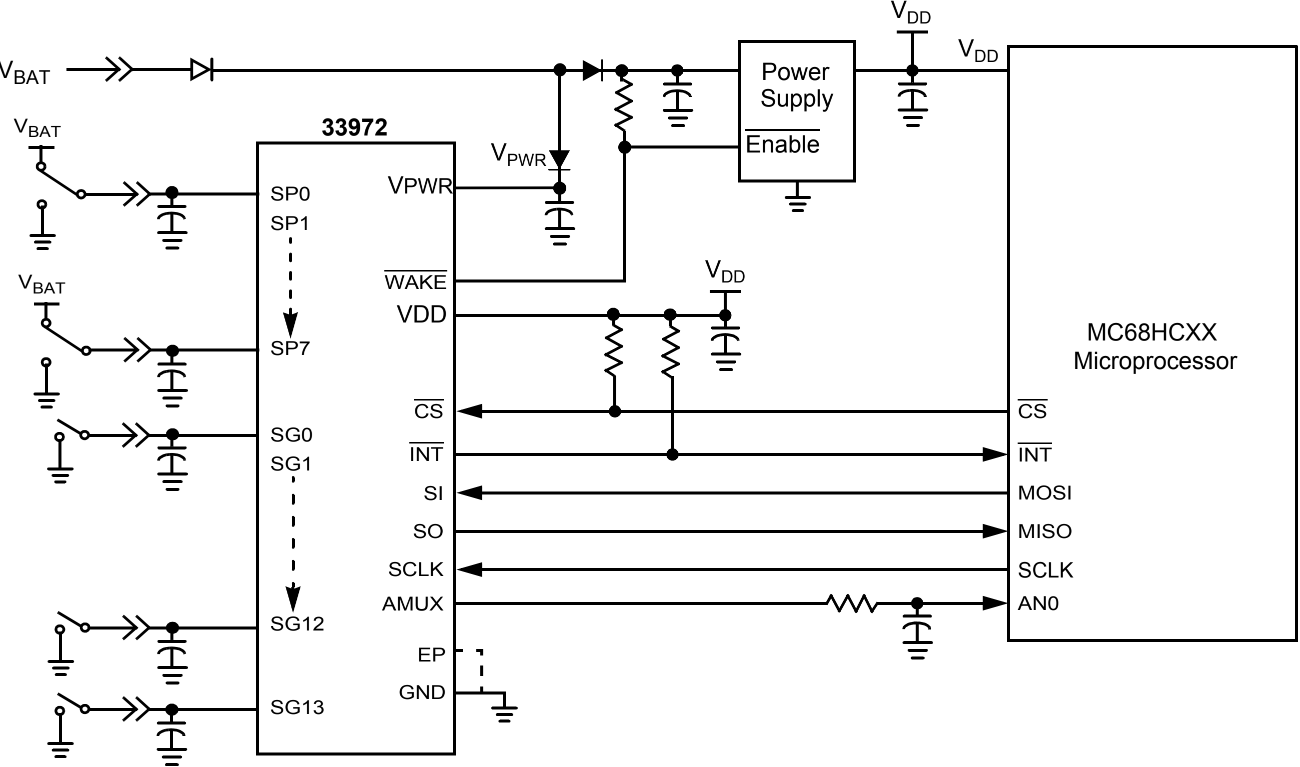
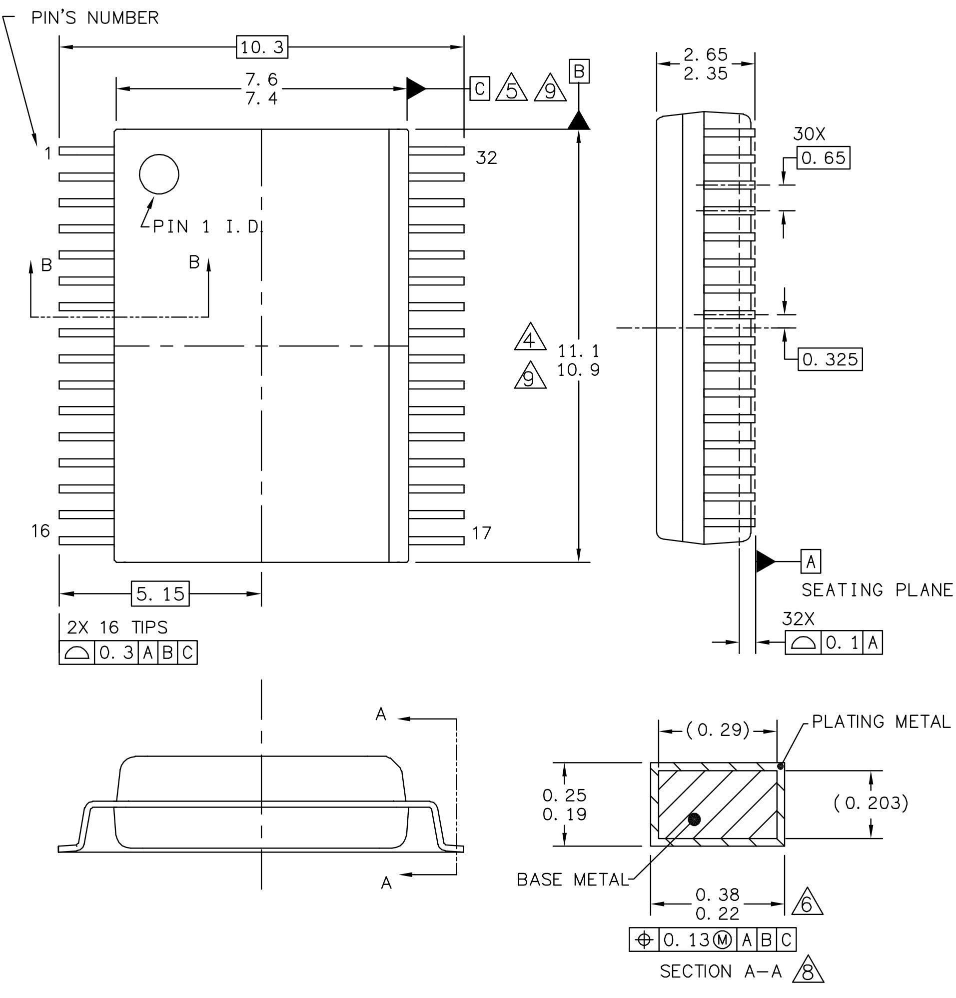


Figure 17. Power Supply Shutdown in Sleep Mode

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the 98A listed below.



EW SUFFIX (Pb-FREE)
32-LEAD SOIC WIDE BODY
98ARH99137A
ISSUE B

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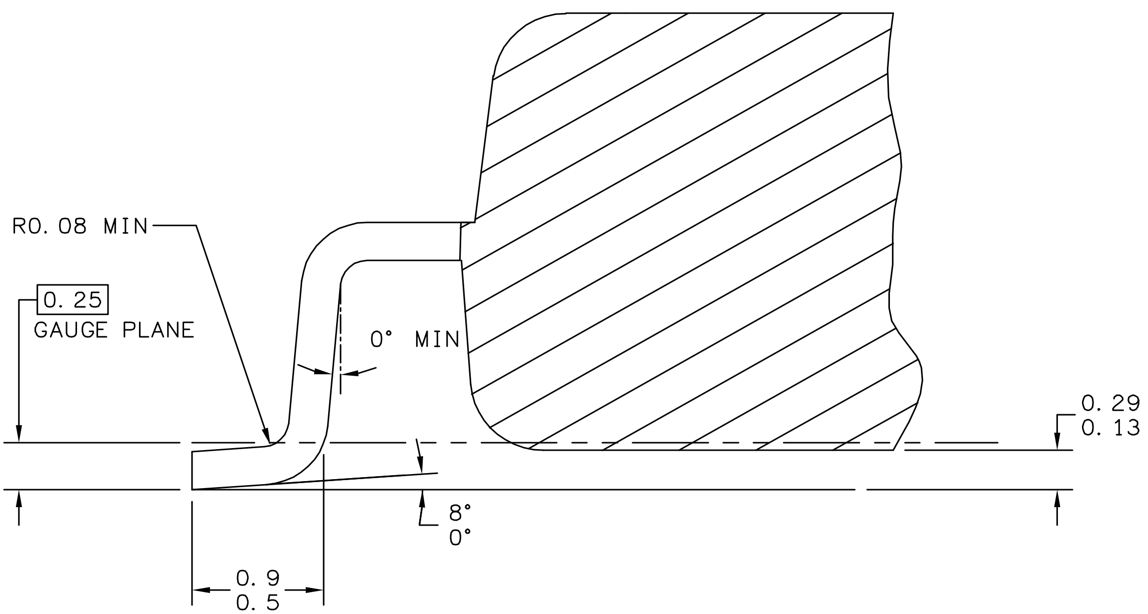
PACKAGE DIMENSIONS (CONTINUED)



SECTION B–B

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TITLE: 32LD SOIC W/B, 0.65 PITCH CASE OUTLINE	DOCUMENT NO: 98ARH99137A		REV: B
	CASE NUMBER: 1324–03		07 APR 2005
	STANDARD: FREESCALE		

EW SUFFIX (Pb-FREE)
32-LEAD SOIC WIDE BODY
98ARH99137A
ISSUE B

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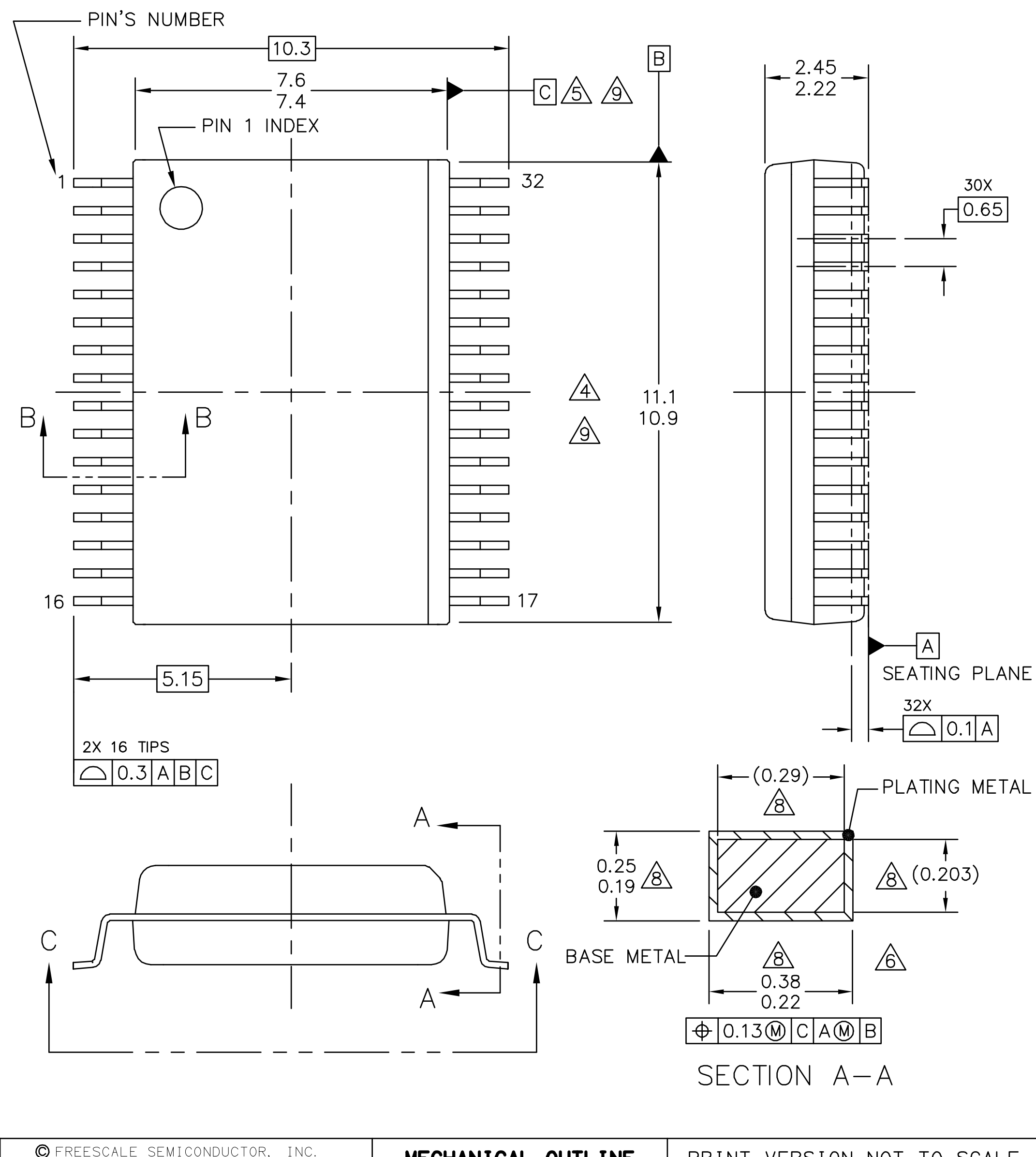

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TITLE: 32LD SOIC W/B, 0.65 PITCH 4.7 X 4.7 EXPOSED PAD, CASE–OUTLINE	DOCUMENT NO: 98ASA10556D	REV: D
	CASE NUMBER: 1454–04	20 JUN 2008
	STANDARD: NON–JEDEC	

EK SUFFIX (Pb-FREE)
32-LEAD SOIC WIDE BODY
EXPOSED PAD
98ASA10556D
ISSUE D

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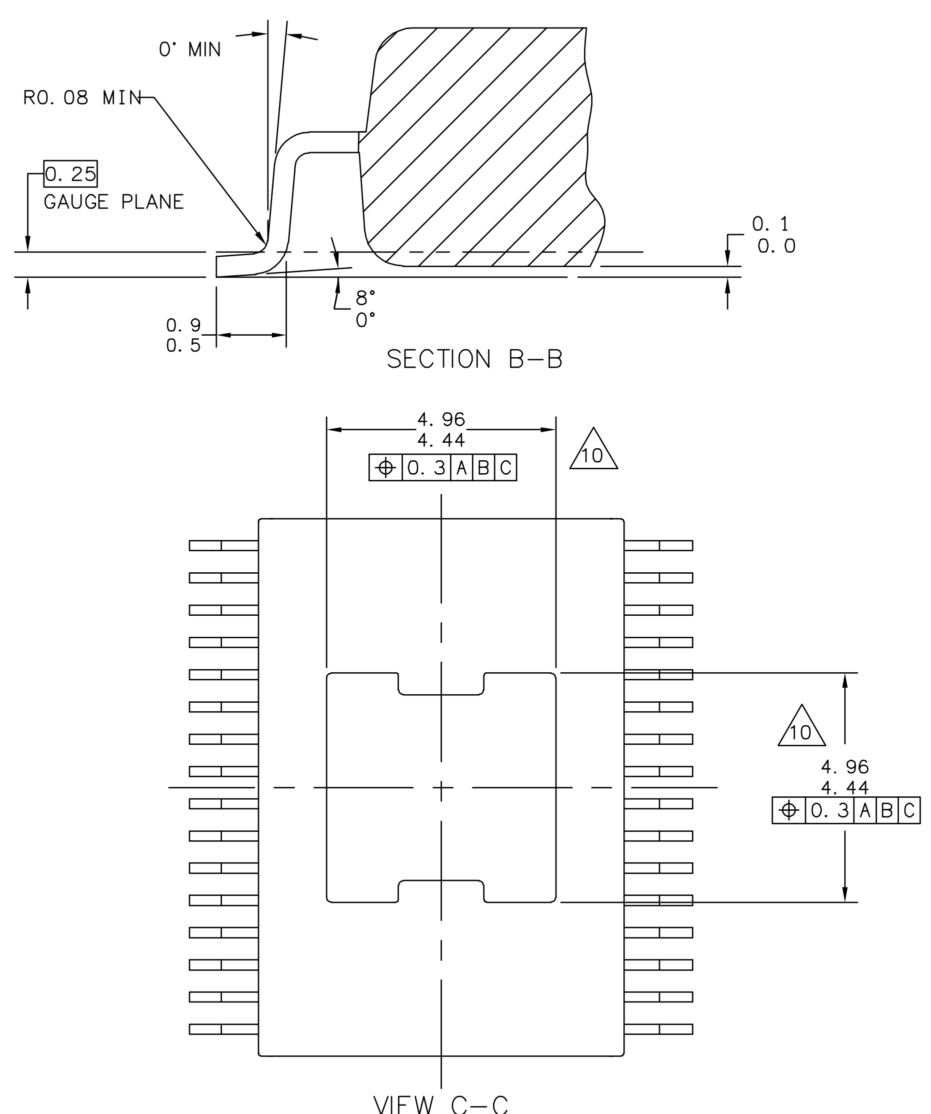

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TITLE: 32LD SOIC W/B, 0.65 PITCH 4.7 X 4.7 EXPOSED PAD, CASE–OUTLINE		DOCUMENT NO: 98ASA10556D	REV: D
		CASE NUMBER: 1454–04	20 JUN 2008
		STANDARD: NON–JEDEC	

EK SUFFIX (Pb-FREE)
32-LEAD SOIC WIDE BODY
EXPOSED PAD
98ASA10556D
ISSUE D

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

THIS DIMENSION DOES NOT INCLUDE INTER−LEAD FLASH OR PROTRUSIONS. INTER−LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.

EXACT SHAPE OF EACH CORNER IS OPTIONAL.

THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.

THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER−LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

THESE DIMENSION RANGES DEFINE THE PRIMARY KEEP−OUT AREA. MOLD LOCKING AND RESIN BLEED CONTROL FEATURES MAY BE VISIBLE AND THEY MAY EXTEND TO 0.34mm FROM MAXIMUM EXPOSED PAD SIZE

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TITLE: 32LD SOIC W/B, 0.65 PITCH 4.7 X 4.7 EXPOSED PAD, CASE−OUTLINE		DOCUMENT NO: 98ASA10556D	REV: D
		CASE NUMBER: 1454−04	20 JUN 2008
		STANDARD: NON−JEDEC	

EK SUFFIX (Pb-FREE)
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98ASA10556D
ISSUE D

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REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
4.0	2/2006	• Converted to Freescale format • Added PC33972A version • Changed Figure 15, Power Supply Active in Sleep Mode • Changed Figure 16, Power Supply Shutdown in Sleep Mode • Updated Outline Drawing for package
5.0	6/2006	• Update to the prevailing Freescale form and style.
6.0	7/2006	• Added MC33972T devices. • Updated StatiC Electrical Characteristics on page 6 with 33972T parameters.
7.0	11/2006	• Changed Human Body Model parameters in Maximum Ratings table. • Replaced Part Number MC33972TEW/R2 with MCZ33972TEW/R2 • Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from Maximum Ratings on page 5. Added note with instructions to obtain this information from www.freescale.com.
8.0	12/2006	• Restated note [(6)] • Changed Part Number MCZ33972TEW/R2 with MC33972TEW/R2
9.0	4/2007	• Removed all references to the 33972T device. • Removed the MC33972TDWB/R2, MC33972TEW/R2, and PC33972AEW/R2 from the ordering information. • Added MCZ33972AEW/R2 to the ordering information.
10.0	6/2007	• Added MC33972EW/R2, MC33972TDWB/R2, MC33972TEW/R2, and MCZ33972TEW/R2 to the ordering information.
11.0	11/2007	• Updated to the current Freescale form and style • Added MC33972AEK/R2 to the ordering information. • Included device specific information relevant to the EK suffix on pages 1, 2, 4, 5, 6, 27, and 28. • Added sentence to CHIP SELECT (CS) on page 10 • Made calculation corrections to Analog Sensor Inputs (Ratiometric)
12.0	12/2007	• Corrected Device Variation Table on page 2.
13.0	12/2007	• Replaced Outline Drawing 98ARL10543D with 98ASA10556D.
14.0	6/2008	• Added Note 7, "T_C is the T_{CASE} of the package" to Electrical Characteristics Table.
15.0	8/2008	• Updated package drawing 98ASA10556D
16.0	10/2009	• Updated data sheet status from Advance Information to Technical Data • Updated to the current Freescale form and style
17.0	2/2011	• Updated Freescale form and style • Added RoHS symbol
18.0	8/2011	• Revised Ordering Information Table by adding part numbers MC33972AEK/R2 and MC33972ATEW/R2, and removing part numbers MC33972DWB/R2 and MC33972TDWB/R2.
19.0	3/2012	• Added the sentence "This condition in not a normal operating condition and can cause damage to the IC." to Programmable Switches (SP0:SP7) and Switch-to-ground Inputs (SG0:SG13) • Changed sentence in Control and Protection Circuitry: "Characteristics are provided for V_{PWR} from 8.0v to 26v for the IC (parametric tests are done from 8.0v to 16.0v)."

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Document Number: MC33972
Rev. 19.0
3/2012

MC33972

Multiple Switch Detection Interface with Suppressed Wake-up

Applications

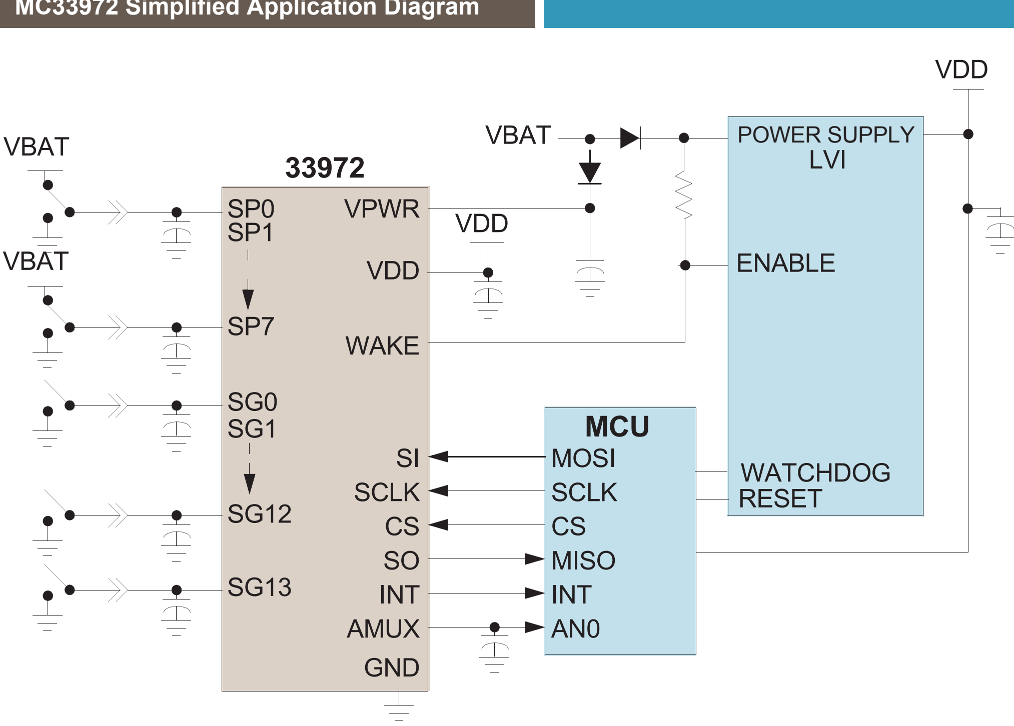
- Automotive Systems
- Aircraft Systems
- Industrial Control Systems
- Process Control Systems
- Security Systems
- Critical systems requiring switch status verification for safety, operation, or process control purposes

Overview

The 33972 Multiple Switch Detection Interface with Suppressed Wake-up is designed to detect the closing and opening of up to 22 switch contacts. The switch status, either open or closed, is transferred to the microprocessor unit (MCU) through a serial peripheral interface (SPI). The device also features a 22-to-1 analog multiplexer for reading inputs as analog. The analog input signal is buffered and provided on the AMUX output terminal for the MCU to read.

The 33972 device has two modes of operation, Normal and Sleep. Normal mode allows programming of the device and supplies switch contacts with pullup or pulldown current as it monitors switch change of state. The Sleep mode provides low quiescent current, which makes the 33972 ideal for automotive and industrial products requiring low sleep state currents.

MC33972 Simplified Application Diagram



Performance	Typical Values
Operating Voltage	5.5 V ≤ V_{PWR} ≤ 26 V
Switch Voltage Range	-14 to V_{PWR}
Contact Wetting Current	2.0 or 16 mA
Quiescent Current: VPWR VDD	 < 100 μA < 20 μA
Control	SPI
Outputs	4
Operating Temperature	-40 °C ≤ T_A ≤ 125 °C

Features

- Switch input voltage range -14 V to V_{PWR}, 40 V Max
- Interfaces directly to microprocessor using 3.3 V/5.0 V SPI protocol
- Selectable wake-up on change of state
- Selectable wetting current (16 mA or 2.0 mA)
- 8 programmable inputs (switches to battery or ground)
- 14 switch-to-ground inputs
- V_{PWR} standby current 100 μA typical, V_{DD} standby current 20 μA typical
- Active interrupt (INT) on change-of-switch state
- Pb-free packaging designated by suffix code EW and EK
- Devices available for comparison are in the Analog Product Selector Guide - SG1002 and Automotive Product Selector Guide - SG187

Customer Benefits

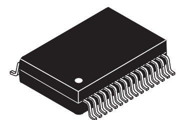
- Optimized multiple switch OPEN/CLOSE status verification with immediate reporting to the MCU
- Interfaces to 3.3 V/5.0 V MCUs with SPI
- Surface-mounted device, requires minimal PC board space, few components, enhanced application reliability, and lower costs
- Simple power conservation solution providing a WAKE output for system wake-up from Sleep mode

Questions

- Do you need to confirm the status of multiple switches in your system?
- Do you need to verify a switch is closed to battery or ground?
- Do you need a switch verification device capable of analog voltage multiplex readout of sensing inputs?
- Do you need a switch verification device that is also capable of controlling small LEDs as well as MOSFET transistors?
- Do you need a switch verification device programmed and controlled via SPI?
- Do you need a switch monitoring device that “sleeps” until switches change status and then alerts the MCU that a switch state has changed?

Ordering Information		
Device	**Remperature Range**	**Package**
MC33972TEW/R2	-40 to 125°C	32 SOICW
MC33972ATEW/R2	-40 to 125°C	32 SOICW
MC33972ATEK/R2	-40 to 125°C	32 SOICW-EP
Evaluation Board		
KIT33972AEWEVBE	Evaluation Board	
Documentation		
MC33972	Data sheet order number	
SG1002	Analog Product Selector Guide	
SG 187	Automotive Product Selector Guide	

32 SOICW/EP



0.65 mm Pitch
7.5 x 11.0 mm Body

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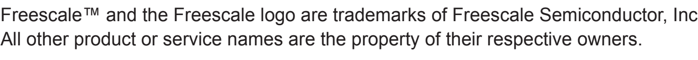

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PART INFORMATION	
Mfg Item Number	KC33972ATEK
Mfg Item Name	SOIC 32 300ML 4.6EP.

SUPPLIER	
Company Name	Freescale Semiconductor Inc
Company Unique ID	14-141-7928
Response Date	2013-12-27
Response Document ID	007YK10945D016A1.2
Contact Name	Freescale Semiconductor Inc
Contact Title	Product Technical Support
Contact Phone	1-800-521-6274
Contact Email	support@freescale.com
Authorized Representative	Daniel Binyon
Representative Title	EPP Customer Response
Representative Phone	512-895-3406
Representative Email	eppanlst@freescale.com
URL for Additional Information	www.freescale.com

DECLARATION	
EU RoHS	Yes
Pb Free	Yes
HalogenFree	Yes
Plating Indicator	e3
EU RoHS Exemption(s)	

MANUFACTURING	
Mfg Item Number	KC33972ATEK
Mfg Item Name	SOIC 32 300ML 4.6EP.
Version	ALL
Weight	0.472000
UoM	g
Unit Volume	EACH
J-STD-020 MSL Rating	3
Peak Processing Temperature	260 C
Max Time at Peak Temperature	40 seconds
Number of Processing Cycles	3

RoHS	
RoHS Directive	2011/65/EU
RoHS Definition	RoHS Definition: Quantity limit of 0.1% by mass (1000 PPM) of homogeneous material for: Lead (Pb), Mercury, Hexavalent Chromium, Polybrominated Biphenyls (PBB), Polybrominated Diphenyl Ethers (PBDE) and quantity limit of 0.01% by mass (100 PPM) of homogeneous material of Cadmium
RoHS Legal Definition	Please indicate whether any homogeneous material (as defined by the RoHS Directive, EU 2011/65/EU and implemented by the laws of the European Union member states) of the part(s) identified on this form contains lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls and/or polybrominated diphenyl ethers (each a RoHS restricted substance) in excess of the applicable quantity limit identified below. If a homogeneous material within the part(s) contains a RoHS restricted substance in excess of an applicable quantity limit, please indicate below which, if any, RoHS exemption you believe may apply. If the part is an assembly with lower level components, the declaration shall encompass all such components. Supplier certifies that it gathered the information it provides in this form using appropriate methods to ensure its accuracy and that such information is true and correct to the best of its knowledge and belief, as of the date that Supplier completes this form. Supplier acknowledges that Company will rely on this certification in determining the compliance of its products with European Union member state laws that implement the RoHS Directive. Company acknowledges that Supplier may have relied on information provided by others in completing this form, and that Supplier may not have independently verified such information. However, in situations where Supplier has not independently verified information provided by others, Supplier agrees that, at a minimum, its suppliers have provided certifications regarding their contributions to the part(s), and those certifications are at least as comprehensive as the certification in this paragraph. If the Company and the Supplier enter into a written agreement with respect to the identified part(s),the terms and conditions of that agreement, including any warranty rights and/or remedies provided as part of that agreement, will be the sole and exclusive source of the Suppliers liability and the Companys remedies for issues that arise regarding information the Supplier provides in this form. In the absence of such written agreement, the warranty rights and/or remedies of Suppliers Standard Terms and Conditions of Sale applicable to such part(s) shall apply.
RoHS Declaration	1 - Item(s) do not contain RoHS restricted substances per the definition above
Supplier Acceptance	Accepted
Signature	Daniel Binyon
Exemption List Version	2012/51/EU
List of Freescale Accepted Exemptions	6(a) : Lead as an alloying element in steel for machining purposes and in galvanized steel containing up to 0.35% lead by weight
	6(b) : Lead as an alloying element in aluminium containing up to 0.4% lead by weight
	6(c) : Copper alloy containing up to 4% lead by weight
	7(a) : Lead in high melting temperature type solders (i.e. lead-based alloys containing 85% by weight or more lead)
	7(b) : Lead in solders for servers, storage and storage array systems, network infrastructure equipment for switching, signaling, transmission, and network management for telecommunications
	7(c)-I : Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors, e.g. piezoelectronic devices, or in a glass or ceramic matrix compound
	7(c)-II : Lead in dielectric ceramic in capacitors for a rated voltage of 125 V AC or 250 V DC or higher
	7(c)-III : Lead in dielectric ceramic in capacitors for a rated voltage of less than 125 V AC or 250 V DC
	7(c)-IV : Lead in PZT based dielectric ceramic materials for capacitors being part of integrated circuits or discrete semiconductors
	15 : Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip chip packages

MATERIAL COMPOSITION

Homogeneous Material	Weight	SubstanceClass	Substance	CAS	Exemption	SubstanceWeight	UoM	SubPart PPM	SubPart%		ARTICLEPPM	ARTICLE%
Epoxy Die Attach	0.0008						g					
Epoxy Die Attach		Cadmium/Cadmium Compounds	Cadmium	7440-43-9		0	g	3	0.0003		0	0
Epoxy Die Attach		Plastics/polymers	Phenolic Polymer Resin, Epikote 155	9003-36-5		0.00014913	g	186411	18.6411		315	0.0315
Epoxy Die Attach		Lead/Lead Compounds	Lead	7439-92-1		0.00000001	g	7	0.0007		0	0
Epoxy Die Attach		Metals	Silver, metal	7440-22-4		0.00065086	g	813579	81.3579		1378	0.1378
Copper Lead Frame	0.126						g					
Copper Lead Frame		Metals	Copper, metal	7440-50-8		0.12145833	g	963955	96.3955		257326	25.7326
Copper Lead Frame		Solvents, additives, and other materials	Phosphorus	7723-14-0		0.00010395	g	825	0.0825		220	0.022
Copper Lead Frame		Metals	Iron, metal	7439-89-6		0.002961	g	23500	2.35		6273	0.6273
Copper Lead Frame		Lead/Lead Compounds	Lead	7439-92-1		0.00002142	g	170	0.017		45	0.0045
Copper Lead Frame		Metals	Silver, metal	7440-22-4		0.00126	g	10000	1		2669	0.2669
Copper Lead Frame		Metals	Tin, metal	7440-31-5		0.0000378	g	300	0.03		80	0.008
Copper Lead Frame		Metals	Zinc, metal	7440-66-6		0.0001575	g	1250	0.125		333	0.0333
Lead Frame Plating	0.0032						g					
Lead Frame Plating		Lead/Lead Compounds	Lead	7439-92-1		0.00000064	g	200	0.02		1	0.0001
Lead Frame Plating		Metals	Tin, metal	7440-31-5		0.00319936	g	999800	99.98		6778	0.6778
Silicon Semiconductor Die	0.0098						g					
Silicon Semiconductor Die		Solvents, additives, and other materials	Other miscellaneous substances (less than 5%).	-		0.000196	g	20000	2		415	0.0415
Silicon Semiconductor Die		Glass	Silicon, doped	-		0.009604	g	980000	98		20347	2.0347
Die Encapsulant, Halogen-free	0.3311						g					
Die Encapsulant, Halogen-free		Solvents, additives, and other materials	Acrylonitrile/Butadiene copolymer, carboxyl terminated (26/74)	68891-46-3		0.0003311	g	1000	0.1		701	0.0701
Die Encapsulant, Halogen-free		Plastics/polymers	Ortho-Cresol, Polymer with 1-Chloro-2,3-Epoxypropane and Formaldehyde	29690-82-2		0.0072842	g	22000	2.2		15432	1.5432
Die Encapsulant, Halogen-free		Plastics/polymers	Proprietary Material-Other Epoxy resins	-		0.0109263	g	33000	3.3		23148	2.3148
Die Encapsulant, Halogen-free		Solvents, additives, and other materials	Carbon Black	1333-86-4		0.0009933	g	3000	0.3		2104	0.2104
Die Encapsulant, Halogen-free		Plastics/polymers	Proprietary Material-Other phenolic resins	-		0.0142373	g	43000	4.3		30163	3.0163
Die Encapsulant, Halogen-free		Glass	Silicon dioxide	7631-86-9		0.013244	g	40000	4		28059	2.8059
Die Encapsulant, Halogen-free		Glass	Silica, vitreous	60676-86-0		0.2840838	g	858000	85.8		601884	60.1884
Bonding Wire, Copper	0.0011						g					
Bonding Wire, Copper		Metals	Copper, metal	7440-50-8		0.001067	g	970000	97		2260	0.226
Bonding Wire, Copper		Solvents, additives, and other materials	Other miscellaneous substances (less than 5%).	-		0.000033	g	30000	3		69	0.0069

LINKS	
MCD LINK	
Freescale website	http://www.freescale.com
GENERAL ENVIRONMENTAL COMPLIANCE LINKS	
RoHS signed letter	http://www.freescale.com/files/abstract/corporate/ehs_epp/ENV_ROHS_Freescale_Response.pdf
China RoHS	http://www.freescale.com/chinarohs
REACH signed letter	http://www.freescale.com/files/abstract/corporate/ehs_epp/ENV_REACH_Freescale_Response.pdf
ELV signed letter	http://www.freescale.com/files/abstract/corporate/ehs_epp/ENV_ELV_Freescale_Reponse.pdf
Conflict Minerals statement	http://www.freescale.com/files/abstract/corporate/ehs_epp/ENV_CONFLICT_METAL_Freescale_Response.pdf
FREESCALE ENVIRONMENTAL INFORMATION	
EPP website	http://www.freescale.com/epp
FAQ	http://www.freescale.com/webapp/sps/site/overview.jsp?code=ENVIRON_FAQ
Technical Service Request	https://www.freescale.com/webapp/servicerequest.create_SR.framework?defaultCategory=Hardware Product Support&defaultTopic=Environmentally Preferred Prod
LINKS TO BLANK IPC1752 FORMS	
Blank IPC1752 v1.1 Form	http://www.freescale.com/files/abstract/corporate/ehs_epp/IPC-1752-2_v1.1_MCD_Template.pdf

IPC1752 XML LINKS

http://www.freescale.com/mcds/KC33972ATEK_IPC1752_v11.xml

http://www.freescale.com/mcds/KC33972ATEK_IPC1752A.xml

PART INFORMATION	
Mfg Item Number	KC33972ATEW
Mfg Item Name	SOIC 32 300ML

SUPPLIER	
Company Name	Freescale Semiconductor Inc
Company Unique ID	14-141-7928
Response Date	2013-11-15
Response Document ID	2013K10517D034A1.1
Contact Name	Freescale Semiconductor Inc
Contact Title	Product Technical Support
Contact Phone	1-800-521-6274
Contact Email	support@freescale.com
Authorized Representative	Daniel Binyon
Representative Title	EPP Customer Response
Representative Phone	512-895-3406
Representative Email	eppanlst@freescale.com
URL for Additional Information	www.freescale.com

DECLARATION	
EU RoHS	Yes
Pb Free	Yes
HalogenFree	Yes
Plating Indicator	e3
EU RoHS Exemption(s)	

MANUFACTURING	
Mfg Item Number	KC33972ATEW
Mfg Item Name	SOIC 32 300ML
Version	ALL
Weight	0.510000
UoM	g
Unit Volume	EACH
J-STD-020 MSL Rating	3
Peak Processing Temperature	260 C
Max Time at Peak Temperature	40 seconds
Number of Processing Cycles	3

RoHS	
RoHS Directive	2011/65/EU
RoHS Definition	RoHS Definition: Quantity limit of 0.1% by mass (1000 PPM) of homogeneous material for: Lead (Pb), Mercury, Hexavalent Chromium, Polybrominated Biphenyls (PBB), Polybrominated Diphenyl Ethers (PBDE) and quantity limit of 0.01% by mass (100 PPM) of homogeneous material of Cadmium
RoHS Legal Definition	Please indicate whether any homogeneous material (as defined by the RoHS Directive, EU 2011/65/EU and implemented by the laws of the European Union member states) of the part(s) identified on this form contains lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls and/or polybrominated diphenyl ethers (each a RoHS restricted substance) in excess of the applicable quantity limit identified below. If a homogeneous material within the part(s) contains a RoHS restricted substance in excess of an applicable quantity limit, please indicate below which, if any, RoHS exemption you believe may apply. If the part is an assembly with lower level components, the declaration shall encompass all such components. Supplier certifies that it gathered the information it provides in this form using appropriate methods to ensure its accuracy and that such information is true and correct to the best of its knowledge and belief, as of the date that Supplier completes this form. Supplier acknowledges that Company will rely on this certification in determining the compliance of its products with European Union member state laws that implement the RoHS Directive. Company acknowledges that Supplier may have relied on information provided by others in completing this form, and that Supplier may not have independently verified such information. However, in situations where Supplier has not independently verified information provided by others, Supplier agrees that, at a minimum, its suppliers have provided certifications regarding their contributions to the part(s), and those certifications are at least as comprehensive as the certification in this paragraph. If the Company and the Supplier enter into a written agreement with respect to the identified part(s),the terms and conditions of that agreement, including any warranty rights and/or remedies provided as part of that agreement, will be the sole and exclusive source of the Suppliers liability and the Companys remedies for issues that arise regarding information the Supplier provides in this form. In the absence of such written agreement, the warranty rights and/or remedies of Suppliers Standard Terms and Conditions of Sale applicable to such part(s) shall apply.
RoHS Declaration	1 - Item(s) do not contain RoHS restricted substances per the definition above
Supplier Acceptance	Accepted
Signature	Daniel Binyon
Exemption List Version	2012/51/EU
List of Freescale Accepted Exemptions	6(a) : Lead as an alloying element in steel for machining purposes and in galvanized steel containing up to 0.35% lead by weight
	6(b) : Lead as an alloying element in aluminium containing up to 0.4% lead by weight
	6(c) : Copper alloy containing up to 4% lead by weight
	7(a) : Lead in high melting temperature type solders (i.e. lead-based alloys containing 85% by weight or more lead)
	7(b) : Lead in solders for servers, storage and storage array systems, network infrastructure equipment for switching, signaling, transmission, and network management for telecommunications
	7(c)-I : Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors, e.g. piezoelectronic devices, or in a glass or ceramic matrix compound
	7(c)-II : Lead in dielectric ceramic in capacitors for a rated voltage of 125 V AC or 250 V DC or higher
	7(c)-III : Lead in dielectric ceramic in capacitors for a rated voltage of less than 125 V AC or 250 V DC
	7(c)-IV : Lead in PZT based dielectric ceramic materials for capacitors being part of integrated circuits or discrete semiconductors
	15 : Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip chip packages

MATERIAL COMPOSITION

Homogeneous Material	Weight	SubstanceClass	Substance	CAS	Exemption	SubstanceWeight	UoM	SubPart PPM	SubPart%		ARTICLEPPM	ARTICLE%
Epoxy Die Attach	0.0011						g					
Epoxy Die Attach		Cadmium/Cadmium Compounds	Cadmium	7440-43-9		0	g	3	0.0003		0	0
Epoxy Die Attach		Plastics/polymers	Phenolic Polymer Resin, Epikote 155	9003-36-5		0.00020505	g	186411	18.6411		402	0.0402
Epoxy Die Attach		Lead/Lead Compounds	Lead	7439-92-1		0.00000001	g	7	0.0007		0	0
Epoxy Die Attach		Metals	Silver, metal	7440-22-4		0.00089494	g	813579	81.3579		1754	0.1754
Copper Lead Frame	0.1359						g					
Copper Lead Frame		Metals	Copper, metal	7440-50-8		0.13100148	g	963955	96.3955		256865	25.6865
Copper Lead Frame		Solvents, additives, and other materials	Phosphorus	7723-14-0		0.00011212	g	825	0.0825		219	0.0219
Copper Lead Frame		Metals	Iron, metal	7439-89-6		0.00319365	g	23500	2.35		6262	0.6262
Copper Lead Frame		Lead/Lead Compounds	Lead	7439-92-1		0.0000231	g	170	0.017		45	0.0045
Copper Lead Frame		Metals	Silver, metal	7440-22-4		0.001359	g	10000	1		2664	0.2664
Copper Lead Frame		Metals	Tin, metal	7440-31-5		0.00004077	g	300	0.03		79	0.0079
Copper Lead Frame		Metals	Zinc, metal	7440-66-6		0.00016988	g	1250	0.125		333	0.0333
Lead Frame Plating	0.0032						g					
Lead Frame Plating		Lead/Lead Compounds	Lead	7439-92-1		0.00000064	g	200	0.02		1	0.0001
Lead Frame Plating		Metals	Tin, metal	7440-31-5		0.00319936	g	999800	99.98		6273	0.6273
Silicon Semiconductor Die	0.0098						g					
Silicon Semiconductor Die		Solvents, additives, and other materials	Other miscellaneous substances (less than 5%).	-		0.000196	g	20000	2		384	0.0384
Silicon Semiconductor Die		Glass	Silicon, doped	-		0.009604	g	980000	98		18831	1.8831
Die Encapsulant, Halogen-free	0.3589						g					
Die Encapsulant, Halogen-free		Solvents, additives, and other materials	Acrylonitrile/Butadiene copolymer, carboxyl terminated (26/74)	68891-46-3		0.0003589	g	1000	0.1		703	0.0703
Die Encapsulant, Halogen-free		Plastics/polymers	Ortho-Cresol, Polymer with 1-Chloro-2,3-Epoxypropane and Formaldehyde	29690-82-2		0.0078958	g	22000	2.2		15481	1.5481
Die Encapsulant, Halogen-free		Plastics/polymers	Proprietary Material-Other Epoxy resins	-		0.0118437	g	33000	3.3		23222	2.3222
Die Encapsulant, Halogen-free		Solvents, additives, and other materials	Carbon Black	1333-86-4		0.0010767	g	3000	0.3		2111	0.2111
Die Encapsulant, Halogen-free		Plastics/polymers	Proprietary Material-Other phenolic resins	-		0.0154327	g	43000	4.3		30260	3.026
Die Encapsulant, Halogen-free		Glass	Silicon dioxide	7631-86-9		0.014356	g	40000	4		28149	2.8149
Die Encapsulant, Halogen-free		Glass	Silica, vitreous	60676-86-0		0.3079362	g	858000	85.8		603806	60.3806
Bonding Wire, Copper	0.0011						g					
Bonding Wire, Copper		Metals	Copper, metal	7440-50-8		0.001067	g	970000	97		2092	0.2092
Bonding Wire, Copper		Solvents, additives, and other materials	Other miscellaneous substances (less than 5%).	-		0.000033	g	30000	3		64	0.0064

LINKS	
MCD LINK	
Freescale website	http://www.freescale.com
GENERAL ENVIRONMENTAL COMPLIANCE LINKS	
RoHS signed letter	http://www.freescale.com/files/abstract/corporate/ehs_epp/ENV_ROHS_Freescale_Response.pdf
China RoHS	http://www.freescale.com/chinarohs
REACH signed letter	http://www.freescale.com/files/abstract/corporate/ehs_epp/ENV_REACH_Freescale_Response.pdf
ELV signed letter	http://www.freescale.com/files/abstract/corporate/ehs_epp/ENV_ELV_Freescale_Reponse.pdf
Conflict Minerals statement	http://www.freescale.com/files/abstract/corporate/ehs_epp/ENV_CONFLICT_METAL_Freescale_Response.pdf
FREESCALE ENVIRONMENTAL INFORMATION	
EPP website	http://www.freescale.com/epp
FAQ	http://www.freescale.com/webapp/sps/site/overview.jsp?code=ENVIRON_FAQ
Technical Service Request	https://www.freescale.com/webapp/servicerequest.create_SR.framework?defaultCategory=Hardware Product Support&defaultTopic=Environmentally Preferred Prod
LINKS TO BLANK IPC1752 FORMS	
Blank IPC1752 v1.1 Form	http://www.freescale.com/files/abstract/corporate/ehs_epp/IPC-1752-2_v1.1_MCD_Template.pdf

IPC1752 XML LINKS

http://www.freescale.com/mcds/KC33972ATEW_IPC1752_v11.xml

http://www.freescale.com/mcds/KC33972ATEW_IPC1752A.xml

Engineering Change Documents

Freescale Confidential Proprietary

AEC Q100 Certification of Design, Construction and Qualification

Q100base-revG; -001revC, -002revD, -003revE, -004revC, -005recC, -006revD, -007revA, -008revA, -009revB, -010revA, -011revB, -012Rev-.

Supplier Name: Freescale Semiconductor		Date:
	Item Name	**Supplier Response**
1.	User's Part Number:	See PPAP
2.	Supplier's Part Number/Data Sheet:	MC33972ATEKR2/48ASA12749D
3.	Device Description:	MSDISW_N39B SM5AP(EP)
4.	Wafer/Die Fab Facility & Process ID:	
	a. Facility name/plant #:	TSMC
	b. Street address:	.No. 121 Park Ave. III, Hsinchu Science Park; Hsinchu, Taiwan 300, R.O.C. (TSMC2)
	c. Country:	Taiwan
5.	Wafer Probe Location:	
	a. Facility name/plant #:	Freescale-Qualified Probe Site(s); Available Upon Request
	b. Street address:	Available Upon Request
	c. Country:	Available Upon Request
6.	Assembly Location & Process ID:	
	a. Facility name/plant #:	FSL-TJN-FM
	b. Street address:	No.15, Xing Hua Avenue; XiQing 300385 Tianjin China (TJN)
	c. Country:	China
7.	Final Quality Control A (Test) Facility:	
	a. Facility name/plant #:	FSL-TJN-FM
	b. Street address:	No.15, Xing Hua Avenue; XiQing 300385 Tianjin China (TJN)
	c. Country:	China
8.	Wafer/Die:	
	a. Wafer Size:	150 mm
	b. Die family:	MSDI-N39B
	c. Die mask set revision & name:	N39B-MASK
	d. Die photo:	Available upon request-linrick
9.	Die Technology Description:	
	a. Wafer/Die process technology:	u065
	b. Die channel length (µM):	1.6um
	c. Die gate length (µM):	1.6um
	d. Die supplier process ID (mask #):	N39B
	e. Number of transistors or gates:	26917
	f. Number of mask steps:	18
10.	Die Dimensions:	
	a. Die width (mm):	2.9464 mm
	b. Die length (mm):	4.04622 mm
	c. Die thickness (finished) (mm):	0.381 mm
11.	Die Metallization:	
	a. Die metallization materials:	AlCuSi
	b. Number of layers:	2
	c. Thickness (per layer):	M1: 6kA M2: 20kA
	d. % of alloys (if present):	99.5% Al/0.5% Cu

AEC Q100 Certification of Design, Construction and Qualification
Q100base-revG; -001revC, -002revD, -003revE, -004revC, -005recC, -006revD, -007revA, -008revA, -009revB, -010revA, -011revB, -012Rev-.

Supplier Name: Freescale Semiconductor	Date:
12. Die Passivation:	
a. Number of passivation layers:	2
b. Die passivation material(s):	SiO2/Si3N4
c. Thickness (es) & tolerances:	2kÅ /7kÅ
13. Die Overcoat Material (e.g., Polyimide)	Polyimide
14. Die Cross-Section Photo/Drawing:	Available upon request
15. Die Prep Backside:	
a. Die prep method:	None
b. Die metallization:	None
c. Thickness(es) & tolerances:	N/A
16. Die Separation Method (Kerf Depth):	
a. Kerf width (um):	20 - 100um
b. Kerf depth (if not 100% saw):	100% Sawn
c. Saw method:	Dual
17. Die Attach:	
a. Die attach material ID:	Sumitomo CRM-1064MBL
b. Die attach method:	Epoxy
c. Die placement diagram:	Available upon request
18. Package:	
a. Type of package (e.g. plastic, ceramic, unpackaged):	Plastic
b. Ball/lead count:	32LD SOIC EP
c. JEDEC designation (e.g., MS029, MS034,	NON-JEDEC
d. Lead (Pb) free (<.1% homogenouse material)	Yes
e. Package outline drawing	See PPAP
19. Mold Compound:	
a. Plastic mold compound supplier & ID:	Sumitomo EME-G630AY
b. Mold compound type:	Epoxy Resin
c. Flammability rating:	UL 94 V0
d. Fire Retardant type/composition	Resin system
e. Tg (glass transition temperature) (°C):	Tg=120C
f. CTE (above & below Tg) (ppm/°C):	CTE1 (below Tg) = 10 ppm/ °C, CTE2 (above Tg) = 40 ppm/ °C
20. Wire Bond:	
a. Wire bond material:	Cu
b. Wire bond diameter (mm):	0.033
c. Type of wire bond at die:	Ball bond
d. Type of wire bond at leadframe:	Stitch bond
e. Wire bonding diagram:	Available upon request
21. Leadframe (if applicable):	
a. Paddle/flag material:	Cu
b. Paddle/flag width (mils):	5.1562 mm
c. Paddle/flag length (mils):	5.1562 mm
d. Paddle/flag plating composition:	None
e. Paddle/flag plating thickness (µin):	NA
f. Leadframe material:	Cu
g. Leadframe bonding plating composition:	Ag
h. Leadframe bonding plating thickness (um):	1.78 - 7.62
i. External lead plating composition:	Sn
j. External lead plating thickness (um):	7.62 - 17.8

AEC Q100 Certification of Design, Construction and Qualification

Q100base-revG; -001revC, -002revD, -003revE, -004revC, -005recC, -006revD, -007revA, -008revA, -009revB, -010revA, -011revB, -012Rev-.

	Supplier Name: Freescale Semiconductor	Date:
22.	Substrate (if applicable): a. Substrate material (e.g., FR5, BT, etc.): b. Substrate thickness (mm): c. Number of substrate metal layers: d. Plating composition of ball solderable surface: e. Panel singulation method: f. Solder ball composition: g: Solder ball diameter (mm):	Not applicable
23.	Unpackaged Die (if not packaged): a. Under Bump Metallurgy (UBM): b. Thickness of UBM metal: c. Bump composition: d. Bump size:	Not Applicable
24.	Header material (if applicable):	Not Applicable
25.	Thermal Resistance: a. ØJA °C/W (approx): b. ØJC °C/W (approx): c. Special thermal dissipation construction techniques:	Leave blank 74 26 Not Applicable
26.	Test circuits, bias levels and operational conditions imposed during the supplier's life and environmental tests:	Available upon request
27.	Fault grade coverage (%):	
28.	Maximum Process Exposure Conditions: a. MSL @ rated SnPb temperature: b. MSL @ rated Pb-free temperature: c. Maximum dwell time @ maximum process temperature:	Note: Temperatures are as measured on the center of the plastic package body top surface. NA MSL3 at 260°C 40
	Attachments: Die Photo: Available Upon Request Package Outline Drawing: See PPAP Die Cross-Section Photos/Drawing: Available Upon Request Wire Bonding Diagram Available Upon Request Die Placement Diagram See PPAP Test Circuits, Bias Levels, & Conditions Available Upon Request	Requirements: 1. A separate Certification of Design, Construction & Qualification must be submitted for each part number, wafer fab, and assembly location. 2. Design, Construction & Qualification shall be compiled by the responsible individual at the supplier who can verify the above information is accurate and complete.
	Completed by and Date: Certified by (electronic signature) and Date:	Completed by: Wang Brenda / 11-DEC-2013 Completed by: Wang Brenda / 11-DEC-2013

AEC Q100 Certification of Design, Construction and Qualification

Q100base-revG; -001revC, -002revD, -003revE, -004revC, -005recC, -006revD, -007revA, -008revA, -009revB, -010revA, -011revB, -012Rev-.

Supplier Name: Freescale Semiconductor		Date:
	Item Name	**Supplier Response**
1.	User's Part Number:	See PPAP
2.	Supplier's Part Number/Data Sheet:	MC33972ATEWR2/48ASA12749D
3.	Device Description:	MSDISW_N39B SM5AP(non EP)
4.	Wafer/Die Fab Facility & Process ID:	
	a. Facility name/plant #:	TSMC
	b. Street address:	No. 121 Park Ave. III, Hsinchu Science Park; Hsinchu, Taiwan 300, R.O.C. (TSMC2)
	c. Country:	Taiwan
5.	Wafer Probe Location:	
	a. Facility name/plant #:	Freescale-Qualified Probe Site(s); Available Upon Request
	b. Street address:	Available Upon Request
	c. Country:	Available Upon Request
6.	Assembly Location & Process ID:	
	a. Facility name/plant #:	FSL-TJN-FM
	b. Street address:	No.15, Xing Hua Avenue; XiQing 300385 Tianjin China (TJN)
	c. Country:	China
7.	Final Quality Control A (Test) Facility:	
	a. Facility name/plant #:	FSL-TJN-FM
	b. Street address:	No.15, Xing Hua Avenue; XiQing 300385 Tianjin China (TJN)
	c. Country:	China
8.	Wafer/Die:	
	a. Wafer Size:	150 mm
	b. Die family:	MSDI-N39B
	c. Die mask set revision & name:	N39B-MASK
	d. Die photo:	Available upon request
9.	Die Technology Description:	
	a. Wafer/Die process technology:	u065
	b. Die channel length (µM):	1.6um
	c. Die gate length (µM):	1.6um
	d. Die supplier process ID (mask #):	N39B
	e. Number of transistors or gates:	26917
	f. Number of mask steps:	18
10.	Die Dimensions:	
	a. Die width (mm):	2.9464 mm
	b. Die length (mm):	4.04622 mm
	c. Die thickness (finished) (mm):	0.381 mm
11.	Die Metallization:	
	a. Die metallization materials:	AlCuSi
	b. Number of layers:	2
	c. Thickness (per layer):	M1: 6kA M2: 20kA
	d. % of alloys (if present):	99.5% Al/0.5% Cu

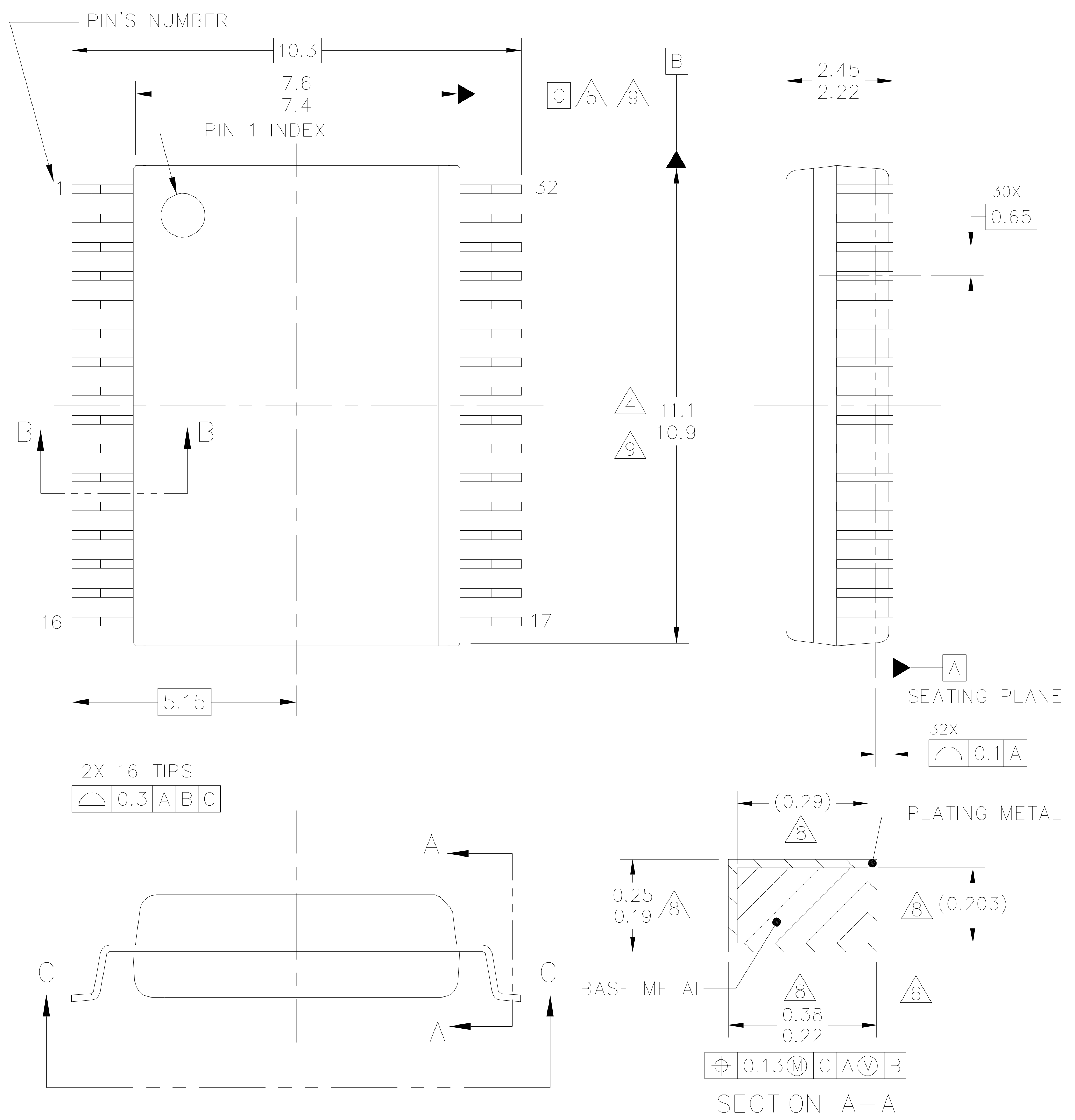
AEC Q100 Certification of Design, Construction and Qualification

Q100base-revG; -001revC, -002revD, -003revE, -004revC, -005recC, -006revD, -007revA, -008revA, -009revB, -010revA, -011revB, -012Rev-.

Supplier Name: Freescale Semiconductor	Date:
12. Die Passivation:	
a. Number of passivation layers:	2
b. Die passivation material(s):	SiO2/Si3N4
c. Thickness (es) & tolerances:	2kÅ /7kÅ
13. Die Overcoat Material (e.g., Polyimide)	Polyimide
14. Die Cross-Section Photo/Drawing:	Available upon request
15. Die Prep Backside:	
a. Die prep method:	None
b. Die metallization:	None
c. Thickness(es) & tolerances:	N/A
16. Die Separation Method (Kerf Depth):	
a. Kerf width (um):	20 - 100um
b. Kerf depth (if not 100% saw):	100% Sawn
c. Saw method:	Dual
17. Die Attach:	
a. Die attach material ID:	Sumitomo CRM-1064MBL
b. Die attach method:	Epoxy
c. Die placement diagram:	Available upon request
18. Package:	
a. Type of package (e.g. plastic, ceramic, unpackaged):	Plastic
b. Ball/lead count:	32LD SOIC
c. JEDEC designation (e.g., MS029, MS034,	NON-JEDEC
d. Lead (Pb) free (<.1% homogenouse material)	Yes
e. Package outline drawing	See PPAP
19. Mold Compound:	
a. Plastic mold compound supplier & ID:	Sumitomo EME-G630AY
b. Mold compound type:	Epoxy Resin
c. Flammability rating:	UL 94 V0
d. Fire Retardant type/composition	Resin system
e. Tg (glass transition temperature) (°C):	Tg=120C
f. CTE (above & below Tg) (ppm/°C):	CTE1 (below Tg) = 10 ppm/ °C, CTE2 (above Tg) = 40 ppm/ °C
20. Wire Bond:	
a. Wire bond material:	Cu
b. Wire bond diameter (mils):	0.033
c. Type of wire bond at die:	Ball bond
d. Type of wire bond at leadframe:	Stitch bond
e. Wire bonding diagram:	Available upon request
21. Leadframe (if applicable):	
a. Paddle/flag material:	Cu
b. Paddle/flag width (mils):	5.1562 mm
c. Paddle/flag length (mils):	5.1562 mm
d. Paddle/flag plating composition:	None
e. Paddle/flag plating thickness (µin):	NA
f. Leadframe material:	Cu
g. Leadframe bonding plating composition:	Ag
h. Leadframe bonding plating thickness (um):	1.78 - 7.62
i. External lead plating composition:	Sn
j. External lead plating thickness (um):	7.62 - 17.8

AEC Q100 Certification of Design, Construction and Qualification
Q100base-revG; -001revC, -002revD, -003revE, -004revC, -005recC, -006revD, -007revA, -008revA, -009revB, -010revA, -011revB, -012Rev-.

	Supplier Name: Freescale Semiconductor	Date:
22.	Substrate (if applicable): a. Substrate material (e.g., FR5, BT, etc.): b. Substrate thickness (mm): c. Number of substrate metal layers: d. Plating composition of ball solderable surface: e. Panel singulation method: f. Solder ball composition: g: Solder ball diameter (mm):	Not applicable
23.	Unpackaged Die (if not packaged): a. Under Bump Metallurgy (UBM): b. Thickness of UBM metal: c. Bump composition: d. Bump size:	Not Applicable
24.	Header material (if applicable):	Not Applicable
25.	Thermal Resistance: a. ØJA °C/W (approx): b. ØJC °C/W (approx): c. Special thermal dissipation construction techniques:	Leave blank 74 26 Not Applicable
26.	Test circuits, bias levels and operational conditions imposed during the supplier's life and environmental tests:	Available upon request
27.	Fault grade coverage (%):	
28.	Maximum Process Exposure Conditions: a. MSL @ rated SnPb temperature: b. MSL @ rated Pb-free temperature: c. Maximum dwell time @ maximum process temperature:	Note: Temperatures are as measured on the center of the plastic package body top surface. NA MSL-3 at 260C 40
	Attachments: Die Photo: Available Upon Request Package Outline Drawing: See PPAP Die Cross-Section Photos/Drawing: Available Upon Request Wire Bonding Diagram Available Upon Request Die Placement Diagram See PPAP Test Circuits, Bias Levels, & Conditions Available Upon Request	Requirements: 1. A separate Certification of Design, Construction & Qualification must be submitted for each part number, wafer fab, and assembly location. 2. Design, Construction & Qualification shall be compiled by the responsible individual at the supplier who can verify the above information is accurate and complete.
	Completed by and Date: Certified by (electronic signature) and Date:	Completed by:Wang Brenda/ 09-Dec-2013 Completed by: Wang Brenda/ 09-Dec-2013
	Typed/Printed: Signature: Title:	



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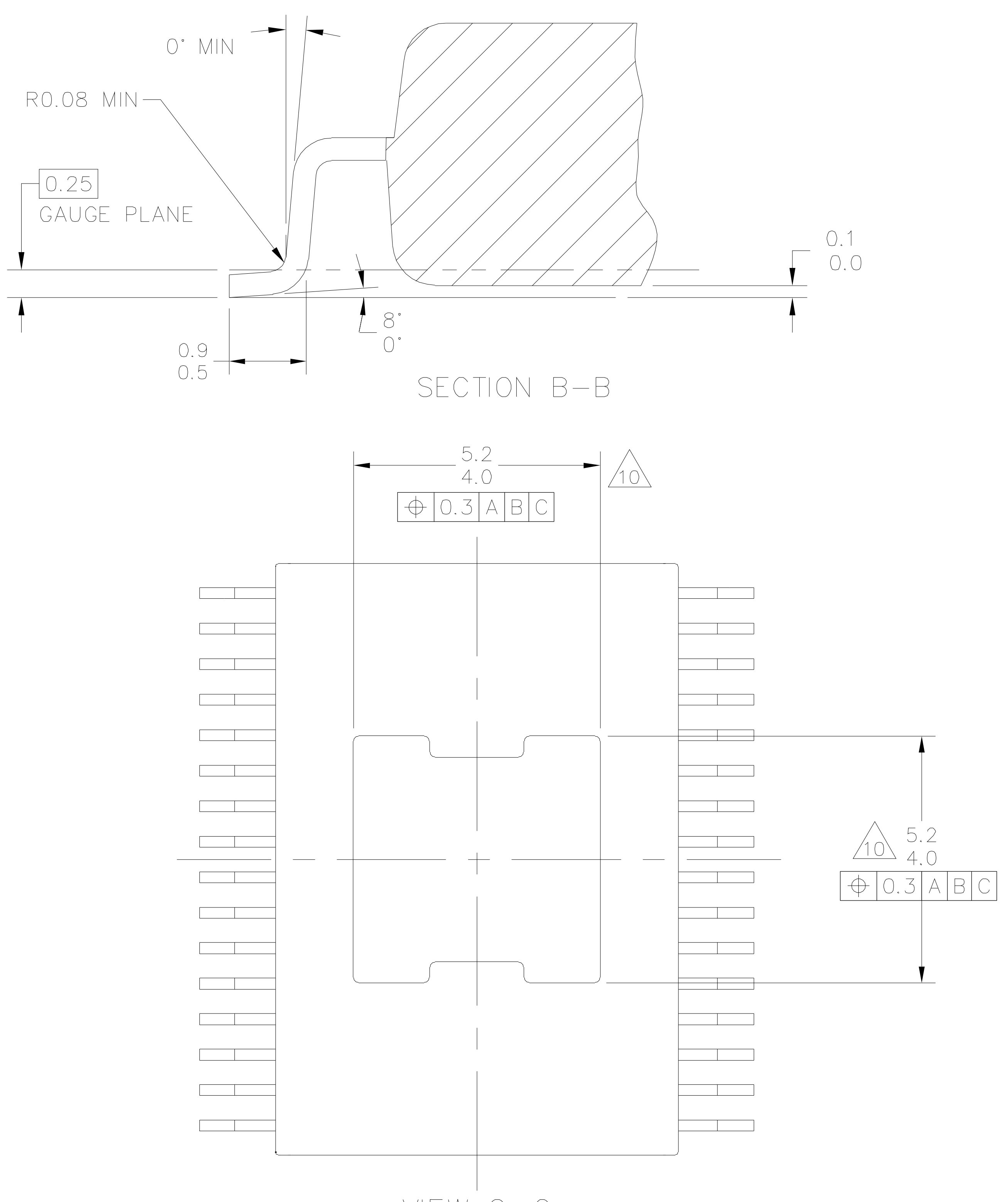
MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 32LD SOIC W/B, 0.65 PITCH 4.6 X 4.6 EXPOSED PAD	DOCUMENT NO: 98ASA00259D	REV: O
	CASE NUMBER: 2150-01	29 JUL 2010
	STANDARD: NON-JEDEC	



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TITLE: 32LD SOIC W/B, 0.65 PITCH 4.6 X 4.6 EXPOSED PAD	DOCUMENT NO: 98ASA00259D		REV: O
	CASE NUMBER: 2150-01		29 JUL 2010
	STANDARD: NON-JEDEC		

NOTES:

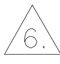
1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M—1994.

3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

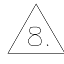
THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

THIS DIMENSION DOES NOT INCLUDE INTER—LEAD FLASH OR PROTRUSIONS. INTER—LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

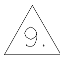


THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.

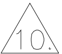
EXACT SHAPE OF EACH CORNER IS OPTIONAL.



THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.



THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER—LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.



THESE DIMENSION RANGES DEFINE THE PRIMARY PCB KEEP—OUT AREA. MOLD LOCKING AND RESIN BLEED CONTROL FEATURES MAY BE VISIBLE.

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TITLE: 32LD SOIC W/B, 0.65 PITCH 4.6 X 4.6 EXPOSED PAD	DOCUMENT NO: 98ASA00259D		REV: 0
	CASE NUMBER: 2150-01		29 JUL 2010
	STANDARD: NON-JEDEC		

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ARH99137A
		PAGE: 1324
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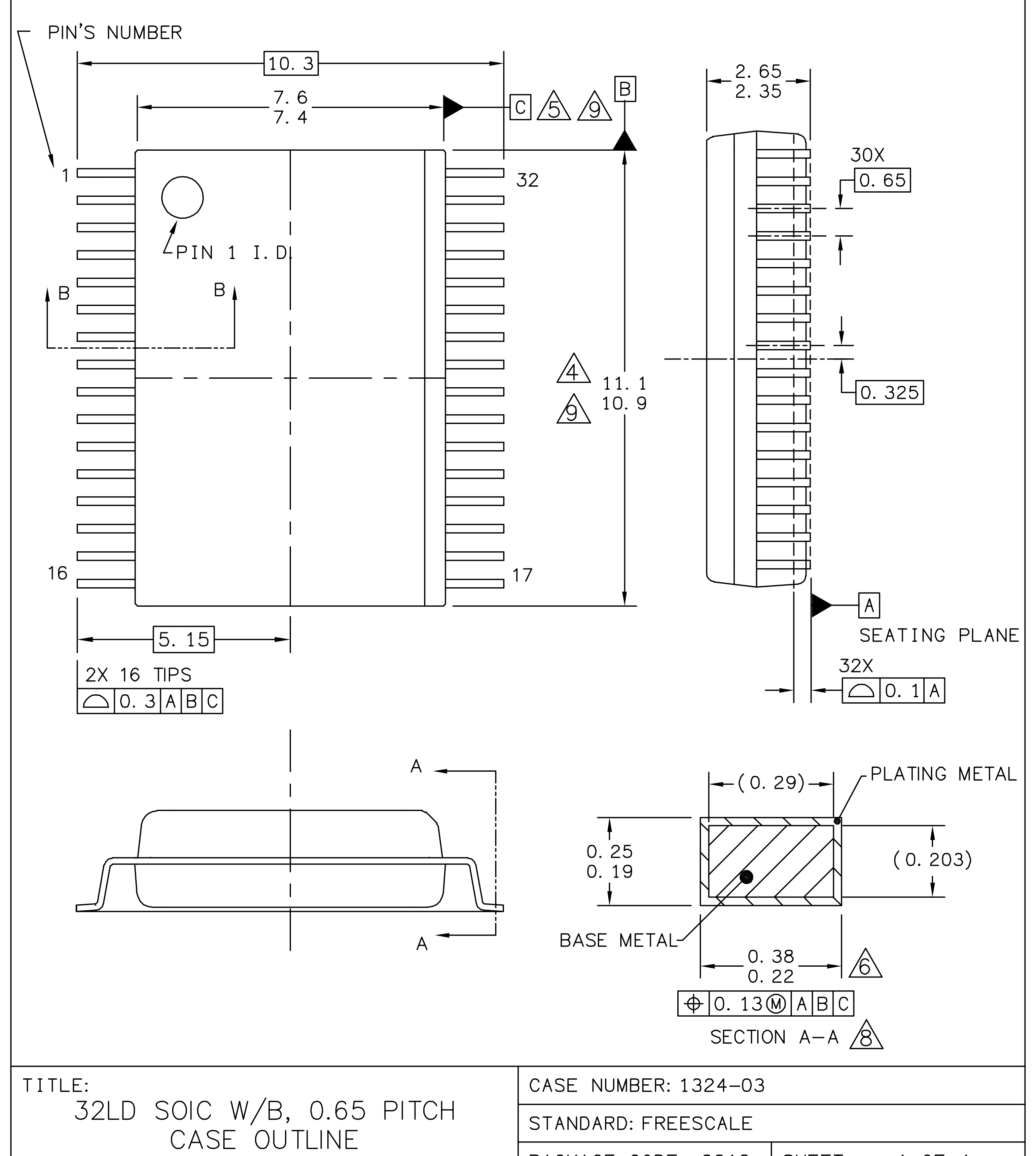

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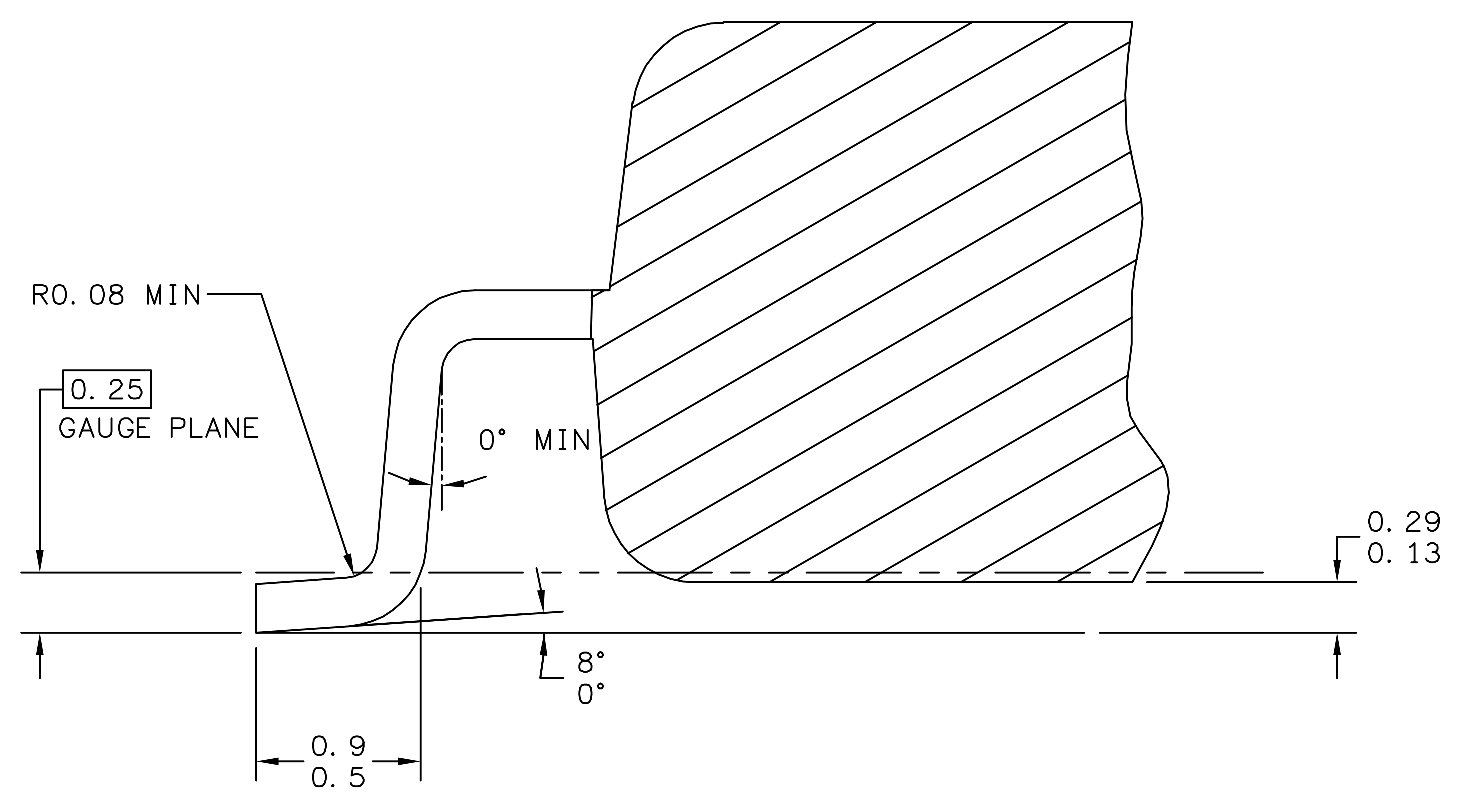

SECTION B–B

TITLE: 32LD SOIC W/B, 0.65 PITCH CASE OUTLINE	CASE NUMBER: 1324–03	
	STANDARD: FREESCALE	
	PACKAGE CODE: 2013	SHEET: 2 OF 4

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NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

4. (△) THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

5. (△) THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

6. (△) THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.

7. (△) EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. (△) THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.

9. (△) THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

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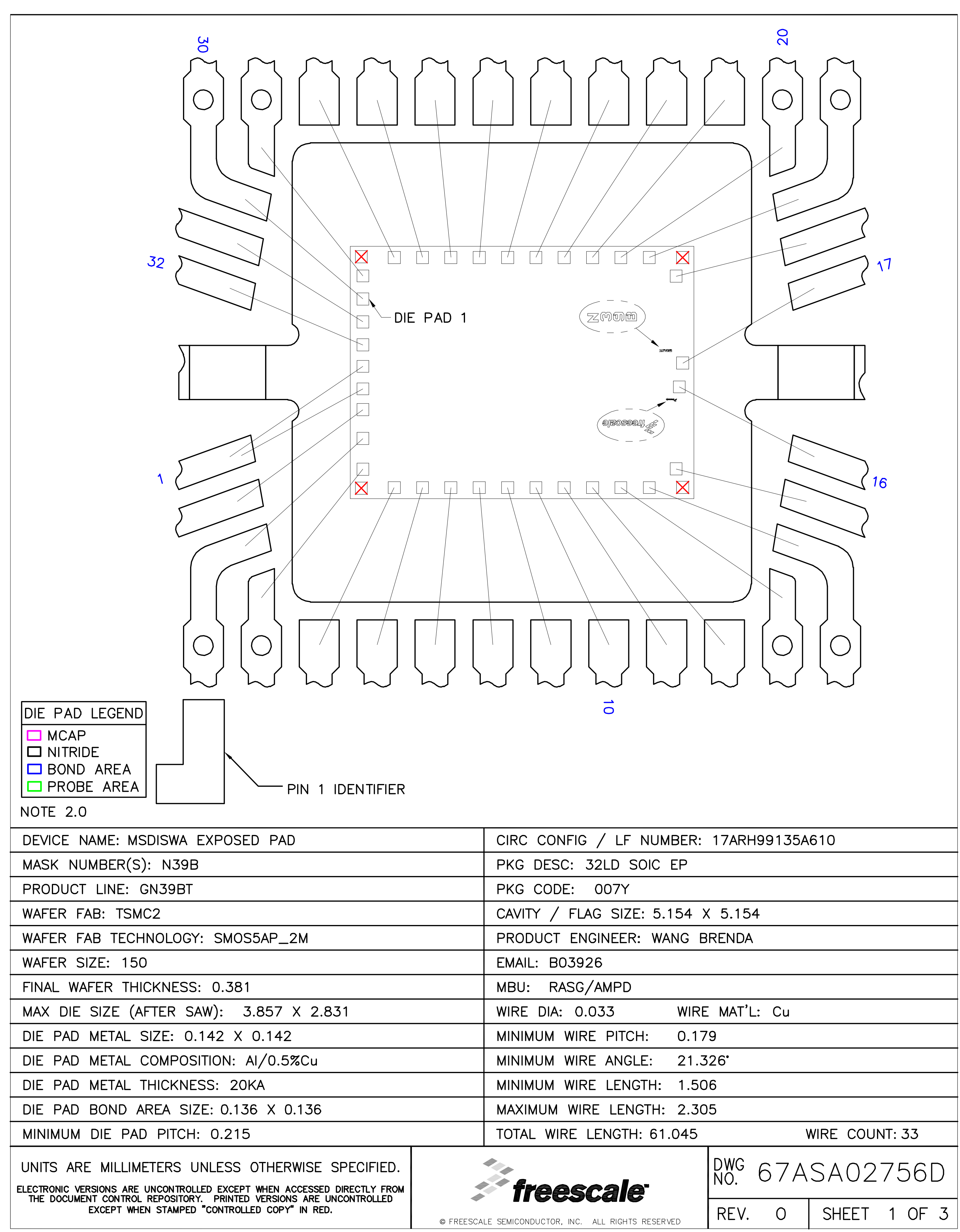
REVISION HISTORY

DOCUMENT NO: 98ARH99137A
PAGE: 1324
REV: B

LTR	ORIGINATOR	REVISIONS	DRAFTER	DATE
O	GARY JOHNSON	RELEASED FOR PRODUCTION	CUPID LEE	02NOV00
A	GARY JOHNSON	UPDATED TO NEW DRAWING FORMAT. CHANGED LEADFRAME THICKNESS FROM 0.152 TO 0.203 MM CHANGED CASE NO. FROM 1324–01 TO 1324–02 CHANGED LEAD WIDTH FROM 0.24 TO 0.29 MM CHANGED STAND–OFF FROM 0.15/0.05 TO 0.29/0.13 ADDED SECTION A–A CHANGED NOTE 2, 3, 4, 5 AND 6 ADDED NOTE 9	CUPID LEE	28AUG01
B	TAYLOR LIU	UPDATED TO FREESCALE FORMAT. SH01, ADDED DIMENSION [0.325] SH01, CHANGED TOLERANCE FROM [⌖ 0.13Ⓜ | C | AⓂ | B] TO [⌖ 0.13Ⓜ | A | B | C] CREATED EXTERNAL CASE OUTLINE.	TAYLOR LIU	07APR05

TITLE: 32LD SOIC W/B, 0.65 PITCH, CASE OUTLINE

CASE NUMBER: 1324–03
STANDARD: FREESCALE
PACKAGE CODE: 2013
SHEET: 4 OF 4



DEVICE NAME: MSDISWA EXPOSED PAD	CIRC CONFIG / LF NUMBER: 17ARH99135A610
MASK NUMBER(S): N39B	PKG DESC: 32LD SOIC EP
PRODUCT LINE: GN39BT	PKG CODE: 007Y
WAFER FAB: TSMC2	CAVITY / FLAG SIZE: 5.154 X 5.154
WAFER FAB TECHNOLOGY: SMOS5AP_2M	PRODUCT ENGINEER: WANG BRENDA
WAFER SIZE: 150	EMAIL: B03926
FINAL WAFER THICKNESS: 0.381	MBU: RASG/AMPD
MAX DIE SIZE (AFTER SAW): 3.857 X 2.831	WIRE DIA: 0.033 WIRE MAT'L: Cu
DIE PAD METAL SIZE: 0.142 X 0.142	MINIMUM WIRE PITCH: 0.179
DIE PAD METAL COMPOSITION: Al/0.5%Cu	MINIMUM WIRE ANGLE: 21.326°
DIE PAD METAL THICKNESS: 20KA	MINIMUM WIRE LENGTH: 1.506
DIE PAD BOND AREA SIZE: 0.136 X 0.136	MAXIMUM WIRE LENGTH: 2.305
MINIMUM DIE PAD PITCH: 0.215	TOTAL WIRE LENGTH: 61.045 WIRE COUNT: 33

UNITS ARE MILLIMETERS UNLESS OTHERWISE SPECIFIED.

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DWG NO. 67ASA02756D

REV. 0 SHEET 1 OF 3

NOTES:

1.0 BONDING ALLOWED ONLY WITHIN DESIGNATED DIE BOND PAD AREAS. AUTO-CENTERING ON DIE PADS THAT HAVE SEPARATE BOND AND PROBE AREAS IS NOT ALLOWED.

2.0 ONLY THE DIE NITRIDE LAYER SHOWN. SEE OLP FOR OTHER COLOR CODED LAYERS. NOTE SOME DIE TECHNOLOGIES MAY NOT HAVE BOND AND PROBE LAYERS.

3.0 "X" LOCATED ON DIE PADS OR BOND FINGERS INDICATES NON-BONDED LOCATION.

4.0 DIE METAL PAD SIZE AND DIE BOND AREA SIZE DIMENSIONS IN THE TABLE ARE THE SMALLEST THAT OCCUR ON THIS DEVICE.

5.0 QUALIFICATION TIER: AEC1

6.0 ASSEMBLY DESIGN RULE DEVIATIONS:

6.1 DIE TECHNOLOGY SMOS5AP_2M IS NOT QUALIFIED WITH CU WIRE. DESIGN RULES USED ARE QUALIFIED FOR THIS DESIGN ONLY. DO NOT USE FOR NEW PRODUCT INTRODUCTION (NPI) DESIGNS. MOVED TO PRODUCTION BASED ON CAB# 13120651M

UNITS ARE MILLIMETERS UNLESS OTHERWISE SPECIFIED.

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REV. 0 | SHEET 2 OF 3

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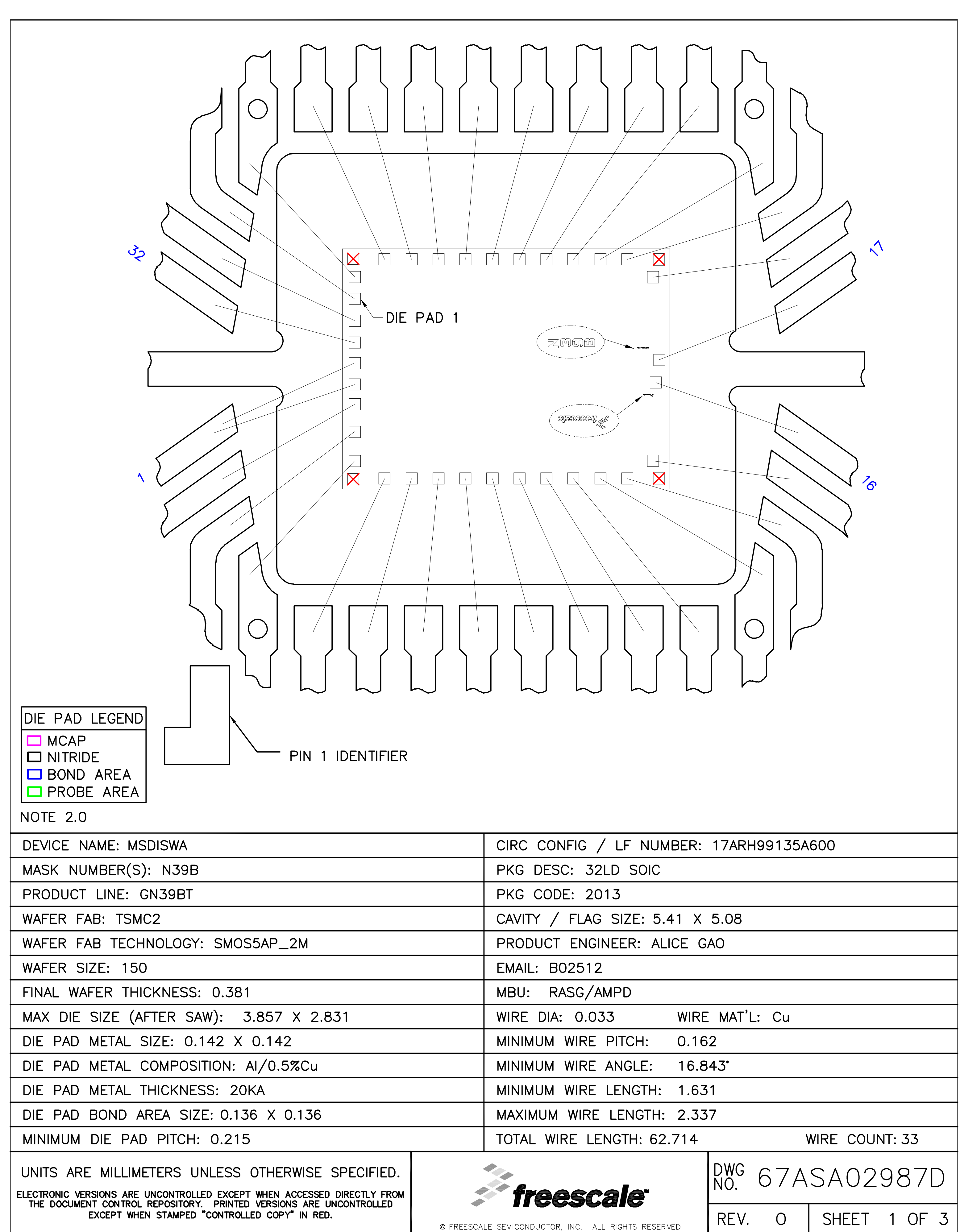
REVISION HISTORY

DOCUMENT NO: 67ASA02756D

REV. 0

LTR	ORIGINATOR	REVISIONS	DRAFTER	DATE
X0	MARIANO CHING	RELEASED TO ENGINEERING EVALUATION (DAR #20592)	GIDEON	04 JUN 2013
0	MARIANO CHING	RELEASED FOR PRODUCTION.THIS BONDING DIAGRAM REVISION IS FOR Cu WIRE DOCUMENTATION ONLY WITH NO CHANGE TO THE DESIGN. THIS DESIGN HAS BEEN RUNNING IN HIGH VOLUME MANUFACTURING FOR SEVERAL YEARS. THIS DESIGN MAY CONTAIN VIOLATIONS TO CURRENT FSL DIE AND PACKAGE DESIGN RULES, HOWEVER THE DESIGN RULES WERE NOT CHECKED. PSD PLATFORM, DESIGN AND PPE TEAMS HAVE APPROVED THESE LEGACY PART CONVERSIONS BASED ON THEIR MANUFACTURING HISTORY. REFERENCED Cu BOND DIAGRAM IS 67ASA02756D_X0. (DAR #21398)	NS	17 DEC 2013



DEVICE NAME: MSDISWA	CIRC CONFIG / LF NUMBER: 17ARH99135A600
MASK NUMBER(S): N39B	PKG DESC: 32LD SOIC
PRODUCT LINE: GN39BT	PKG CODE: 2013
WAFER FAB: TSMC2	CAVITY / FLAG SIZE: 5.41 X 5.08
WAFER FAB TECHNOLOGY: SMOS5AP_2M	PRODUCT ENGINEER: ALICE GAO
WAFER SIZE: 150	EMAIL: B02512
FINAL WAFER THICKNESS: 0.381	MBU: RASG/AMPD
MAX DIE SIZE (AFTER SAW): 3.857 X 2.831	WIRE DIA: 0.033 WIRE MAT'L: Cu
DIE PAD METAL SIZE: 0.142 X 0.142	MINIMUM WIRE PITCH: 0.162
DIE PAD METAL COMPOSITION: Al/0.5%Cu	MINIMUM WIRE ANGLE: 16.843°
DIE PAD METAL THICKNESS: 20KA	MINIMUM WIRE LENGTH: 1.631
DIE PAD BOND AREA SIZE: 0.136 X 0.136	MAXIMUM WIRE LENGTH: 2.337
MINIMUM DIE PAD PITCH: 0.215	TOTAL WIRE LENGTH: 62.714 WIRE COUNT: 33

UNITS ARE MILLIMETERS UNLESS OTHERWISE SPECIFIED.

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DWG NO. 67ASA02987D

REV. 0 | SHEET 1 OF 3

NOTES:

1.0 BONDING ALLOWED ONLY WITHIN DESIGNATED DIE BOND PAD AREAS. AUTO-CENTERING ON DIE PADS THAT HAVE SEPARATE BOND AND PROBE AREAS IS NOT ALLOWED.

2.0 ONLY THE DIE NITRIDE LAYER SHOWN. SEE OLP FOR OTHER COLOR CODED LAYERS. NOTE SOME DIE TECHNOLOGIES MAY NOT HAVE BOND AND PROBE LAYERS.

3.0 "X" LOCATED ON DIE PADS OR BOND FINGERS INDICATES NON-BONDED LOCATION.

4.0 DIE METAL PAD SIZE AND DIE BOND AREA SIZE DIMENSIONS IN THE TABLE ARE THE SMALLEST THAT OCCUR ON THIS DEVICE.

5.0 QUALIFICATION TIER: AEC1

6.0 ASSEMBLY DESIGN RULE DEVIATIONS:
6.1 DIE TECHNOLOGY SMOS5AP_2M IS NOT QUALIFIED WITH CU WIRE. DESIGN RULES USED ARE QUALIFIED FOR THIS DESIGN ONLY. DO NOT USE FOR NEW PRODUCT INTRODUCTION (NPI) DESIGNS. MOVED TO PRODUCTION BASED ON CAB# 13120651M.

UNITS ARE MILLIMETERS UNLESS OTHERWISE SPECIFIED.

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DWG NO.	67ASA02987D
REV. 0	SHEET 2 OF 3

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REVISION HISTORY

DOCUMENT NO: 67ASA02987D

REV. O

LTR	ORIGINATOR	REVISIONS	DRAFTER	DATE
O	MARIANO CHING	RELEASED FOR PRODUCTION.THIS BONDING DIAGRAM REVISION IS FOR Cu WIRE DOCUMENTATION ONLY WITH NO CHANGE TO THE DESIGN. THIS DESIGN HAS BEEN RUNNING IN HIGH VOLUME MANUFACTURING FOR SEVERAL YEARS. THIS DESIGN MAY CONTAIN VIOLATIONS TO CURRENT FSL DIE AND PACKAGE DESIGN RULES, HOWEVER THE DESIGN RULES WERE NOT CHECKED. PSD PLATFORM, DESIGN AND PPE TEAMS HAVE APPROVED THESE LEGACY PART CONVERSIONS BASED ON THEIR MANUFACTURING HISTORY. REFERENCED Au BOND DIAGRAM IS 67ASA01070D_O. (DAR #21200)	GIDEON	03 OCT 2013

Customer Engineering Approval

Design FMEA

POTENTIAL FAILURE MODE AND EFFECTS ANLAYSIS
(Design FMEA)

☐ System
☐ Subsystem
☑ Component: MSDI

Control Number / Issue: 83ASA10126D/O

Prepared By: Erik Thompson RS585 (480) 413-8408

FMEA Date (Orig.) : 10/15/01

Company, Group, Site/Business Unit: Motorola SPS, TSPG, APD

(Rev.) : 11/11/02

Core Team: Erik Thompson (Design), Robert Dixon (Design), Peter Bills (Applications), Tiffany Le (Product)

Line	Item Pin / Function	POTENTIAL FAILURE MODE	POTENTIAL EFFECT(S) OF FAILURE	SEV	CLASS	POTENTIAL CAUSE(S)/ MECHANISIM(S) OF FAILURE	OCCUR	CURRENT PROCESS CONTROLS	DETEC	RPN	RECOMMENDED ACTION(S)	RESPONSIBILITY & TARGET COMPLETION DATE	ACTION RESULTS: ACTION TAKEN	SEV	OCC	DET	RPN
1	**Pin 1 / GND**	Open	Drive MCU I/O to VPWR	8		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	8	None						
2		Short Ground	N/A														
3		Short Vdd	AMUX non-functional, SPI non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
4		Short Vpwr	IC non-functional	8		IC Metalization/process short	1	Testing at probe and again at assembly site	1	8	None						
5		Short to Pin 2 SI	SPI non-functional	5		IC Metalization/process short, Bond wire short	1	Testing at probe and again at assembly site	1	5	None						
6	**Pin 2 / SI**	Open	SPI non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
7		Short Ground	SPI non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
8		Short Vdd	SPI non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
9		Short Vpwr	Permanent Damage to IC	8		IC Metalization/process short	1	Testing at probe and again at assembly site	1	8	None						
10		Short to Pin 3 SCLK	SPI non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
11	**Pin 3 / SCLK**	Open	SPI non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
12		Short Ground	SPI non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
13		Short Vdd	SPI non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
14		Short Vpwr	Permanent Damage to IC	8		IC Metalization/process short	1	Testing at probe and again at assembly site	1	8	None						
15		Short to Pin 4 CSB	SPI non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
16	**Pin 4 / CSB**	Open	SPI non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
17		Short Ground	SO in unknown state, SPI non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
18		Short Vdd	SPI non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
19		Short Vpwr	Permanent Damage to IC	8		IC Metalization/process short	1	Testing at probe and again at assembly site	1	8	None						
20		Short to Pin 5 SP0	SPI non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
21	**Pin 5 / SP0**	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						

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22		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
23		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
24		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
25		Short to Pin 6 SP1	SP0 and SP1 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
26	**Pin 6 / SP1**	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
27		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
28		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
29		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
30		Short to Pin 7 SP2	SP1 and SP2 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
31	**Pin 7 / SP2**	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
32		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
33		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
34		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
35		Short to Pin 8 SP3	SP2 and SP3 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
36	**Pin 8 / SP3**	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
37		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
38		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
39		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
40		Short to Pin 9 SG0	SP3 and SG0 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						

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41	**Pin 9 / SG0**	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
42		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
43		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
44		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
45		Short to Pin 10 SG1	SG0 and SG1 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
46	**Pin 10 / SG1**	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
47		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
48		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
49		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
50		Short to Pin 11 SG2	SG1 and SG2 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
51	**Pin 11 / SG2**	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
52		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
53		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
54		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
55		Short to Pin 12 SG3	SG2 and SG3 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
56	**Pin 12 / SG3**	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
57		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
58		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
59		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						

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60		Short to Pin 13 SG4	SG3 and SG4 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
61	**Pin 13 / SG4**	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
62		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
63		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
64		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
65		Short to Pin 14 SG5	SG4 and SG5 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
66	**Pin 14 / SG5**	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
67		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
68		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
69		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
70		Short to Pin 15 SG6	SG5 and SG6 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
71	**Pin 15 / SG6**	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
72		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
73		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
74		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
75		Short to Pin 16 VPWR	SG6 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
76	**Pin 16 / VPWR**	Open	IC non-functional, remains in reset	8		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	8	None						
77		Short Ground	AMUX non-functional, SPI non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
78		Short Vdd	Permanent Damage to IC	8		IC Metalization/process short	1	Testing at probe and again at assembly site	1	8	None						

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79		Short Vpwr	N/A														
80		Short to Pin 17 WAKEB	Permanent Damage to WAKEB pin	8		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	8	None						
81	**Pin 17 / WAKEB**	Open	WAKEB non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
82		Short Ground	WAKEB non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
83		Short Vdd	WAKEB non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
84		Short Vpwr	Permanent Damage to WAKEB pin	8		IC Metalization/process short	1	Testing at probe and again at assembly site	1	8	None						
85		Short to Pin 18 SG13	WAKEB and SG13 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
86	**Pin 18 / SG13**	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
87		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
88		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
89		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
90		Short to Pin 19 SG12	SG13 and SG12 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
91	**Pin 19 / SG12**	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
92		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
93		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
94		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
95		Short to Pin 20 SG11	SG12 and SG11 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
96	**Pin 20 / SG11**	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
97		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
98		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						

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99		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
100		Short to Pin 21 SG10	SG11 and SG10 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
101	**Pin 21 / SG10**	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
102		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
103		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
104		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
105		Short to Pin 22 SG9	SG10 and SG9 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
106	**Pin 22 / SG9**	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
107		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
108		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
109		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
110		Short to Pin 23 SG8	SG9 and SG8 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
111	**Pin 23 / SG8**	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
112		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
113		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
114		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
115		Short to Pin 24 SG7	SG8 and SG7 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
116	**Pin 24 / SG7**	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
117		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						

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118		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
119		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
120		Short to Pin 25 SP4	SG7 and SP4 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
121	**Pin 25 / SP4**	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
122		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
123		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
124		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
125		Short to Pin 26 SP5	SP4 and SP5 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
126	**Pin 26 / SP5**	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
127		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
128		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
129		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
130		Short to Pin 27 SP6	SP5 and SP6 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
131	**Pin 27 / SP6**	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
132		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
133		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
134		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
135		Short to Pin 28 SP7	SP6 and SP7 non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
136	**Pin 28 / SP7**	Open	SP0 non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						

POTENTIAL FAILURE MODE AND EFFECTS ANLAYSIS
(Design FMEA)

☐ System
☐ Subsystem

☑ Component: MSDI

Control Number / Issue: 83ASA10126D/O

Prepared By: Erik Thompson RS585 (480) 413-8408

FMEA Date (Orig.) : 10/15/01

Company, Group, Site/Business Unit: Motorola SPS, TSPG, APD

(Rev.) : 11/11/02

Core Team: Erik Thompson (Design), Robert Dixon (Design), Peter Bills (Applications), Tiffany Le (Product)

Line	Item Pin / Function	POTENTIAL FAILURE MODE	POTENTIAL EFFECT(S) OF FAILURE	SEV	CLASS	POTENTIAL CAUSE(S)/ MECHANISIM(S) OF FAILURE	OCCUR	CURRENT PROCESS CONTROLS	DETEC	RPN	RECOMMENDED ACTION(S)	RESPONSIBILITY & TARGET COMPLETION DATE	ACTION RESULTS: ACTION TAKEN	SEV	OCC	DET	RPN
137		Short Ground	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
138		Short Vdd	SP0 non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
139		Short Vpwr	SP0 non-functional, VDD clamped to pad zener (~10V)	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
140		Short to Pin 29 INTB	INTB and SP7 clamped to pad zener (~10V)	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
141	**Pin 29 / INTB**	Open	INTB non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
142		Short Ground	INTB non-functional, excessive current in VDD	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
143		Short Vdd	INTB non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
144		Short Vpwr	Permanent Damage to IC	8		IC Metalization/process short	1	Testing at probe and again at assembly site	1	8	None						
145		Short to Pin 30 AMUX	INTB non-functional, AMUX non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
146	**Pin 30 / AMUX**	Open	AMUX non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
147		Short Ground	AMUX non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
148		Short Vdd	AMUX non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
149		Short Vpwr	Possible IC damage, excessive voltage on VDD	8		IC Metalization/process short	1	Testing at probe and again at assembly site	1	8	None						
150		Short to Pin 31 VDD	AMUX non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
151	**Pin 31 / VDD**	Open	AMUX non-functional, SPI non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
152		Short Ground	Permanent damage to IC, excessive current in VDD	8		IC Metalization/process short	1	Testing at probe and again at assembly site	1	8	None						
153		Short Vdd	N/A														
154		Short Vpwr	Permanent damage to IC	8		IC Metalization/process short	1	Testing at probe and again at assembly site	1	8	None						
155		Short to Pin 32 SO	SPI non-functional, excessive current in VDD	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
156	**Pin 32 / SO**	Open	SPI non-functional	5		Open bond wire, metal migration	1	Testing at probe and again at assembly site	1	5	None						
157		Short Ground	SPI non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						

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POTENTIAL FAILURE MODE AND EFFECTS ANLAYSIS
(Design FMEA)

☐ System
☐ Subsystem

Control Number / Issue: 83ASA10126D/O

☑ Component: MSDI

Prepared By: Erik Thompson RS585 (480) 413-8408

FMEA Date (Orig.): 10/15/01

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(Rev.): 11/11/02

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158		Short Vdd	SPI non-functional	5		IC Metalization/process short	1	Testing at probe and again at assembly site	1	5	None						
159		Short Vpwr	Permanent damage to IC	8		IC Metalization/process short	1	Testing at probe and again at assembly site	1	8	None						
160		Short to Pin 1 GND	SPI non-functional	5		Solder short, Bond wire short, short PCB trace	1	Testing at probe and again at assembly site	1	5	None						
161																	

Process Flow Diagrams

High Level Flow

(Detailed Process Flow Diagrams are part of the Freescale Control Plans, if applicable to this PPAP)

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F

HIGH LEVEL FLOW CHART

Customer Part Number:	Various	Date:	12 December, 2013
Part Name:	MSDISWA	Freescale Part Number:	MC33972ATEK(R2)/ MC33972ATEW(R2)

Process	Location	City, State or Country
Design	FSL-AMPD	Tempe,Arizona,USA
Wafer Fab	TSMC2 FAB	Hsinchu,Taiwan
Assembly	FSL-TJN-FM	Tianjin, China
Burn-in	NA	NA
Final Test	FSL-TJN-FM	Tianjin, China
Tape & Reel	FSL-TJN-FM	Tianjin, China
Final Inspection	FSL-TJN-FM	Tianjin, China
Any Subcontractor Process	TSMC2 FAB	Hsinchu,Taiwan
PDC (Product Distribution Center)	Various	Various
Customer Ship-to Locations	Various	Various

Note: This is a sequential listing of the major process steps, including all subcontractor processes and may include any alternate sites which are used for processing. There may be multiple sites listed for the various process steps.

Process FMEA

TSMC PPAP Documents

• TSMC PPAP documents (FMEAs, Control Plans, Cpks, and GR&R) are considered proprietary information by TSMC, classified as "TSMC INTERNAL USE ONLY" and cannot be distributed with Freescale PPAPs in accordance with an agreement with TSMC.

• The PPAP documents are pulled by Freescale External Manufacturing Quality and checked for compliance with TS16949 requirements.

• For special requests, Freescale may be able to review these documents on a limited basis with customers at the local Freescale sales office.

• If there are any questions, please contact:

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POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

Item: SOIC16/28/32/54ld
Type: ___ Design _x_ Process
Prepared By: Amanda Wang
Core Team: Amanda Wang,H.J. Liu,Ivory Guo,JUN YING ZHENG,XIAOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN

Control Number/Issue: 83MCT00002A/BY
Company,Group,Site/Business Unit: Freescale,TJN-FM
FMEA Date: 05-Oct-94 (Orig.)
14-Nov-13 (Rev.)

Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	SEV	Class	Potential Cause(s)/ Mechanism(s) of Failue	OCC	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	DET	RPN	Recommended Action(s)	Responsibility & Target Completion Date	Action Results: Actions Taken & Effective Date	SEV	OCC	DET	RPN
1. Wafer Mount	wafer broken	Yield lost.(6)	6		Wafer alignment table problem (wrong clamp gap)	2	Quarterly PM	Machine auto alarm (2)	2	24	None						
			6		Roller pressure	1	Quarterlly PM	Machine auto alarm(2)	2	12	None						
			6		Higher/uneven attachment table	1	Quarterly PM	Machine auto alarm(2)	2	12	None						
			6		Improper vacuum pressure	1	Check per TCM/device change	Machine auto alarm(2)	2	12	None						
	Wrong orientation	dicing saw failure(4)	4		Wafer mount wrong orientation	2	Use wafer orientation system with bar code scan.	25 points detection for the first piece of wafer by lot (4) Mount orientation auto check (2)	2	16	None						
	bubble	die fly-off(5) die chipping&crack(5) electrical failure(8)	8		Contaminated Mylar	1		Check every piece of wafer by lot(4)	4	32	None						
2. Wafer saw & UV	Stained wafer topside	electrical failure due to corrosion or weak bond(8) Reliability failure due to corrosion or weak bond(8) NSOP in WB process (5)	8		Improper DI water pressure during saw	2	Check TCM shiftly	25 points detection for the first piece of wafer by lot(4)	4	64	None						
			8		Improper cleaning parameter	2	Check TCM shiftly. Quarterly PM. Implement two-fluid nozzle clean.	25 points detection for the first piece of wafer by lot(4)	4	64	None						

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			8		Foreign matter	2	Implement a cover on the top of wafer cassette.	25 points detection for the first piece of wafer by lot(4)	4	64	None						
	die scratch	electrical failure.(8) Reliability failure(8)	8		blade breakage	2	Check BBD sensor sensitivity per TCM. BBD sensor auto alarm.	25 points detection for the first piece of wafer by lot(4)	4	64	None						
			8		blade worn out.	1	Check and control remained exposure length per TCM. Blade wore out auto alarm.	Machine auto alarm(2)	2	16	None						
			8		die fly-off	2	Check cutting table surface condition during yearly PM. Visual check bubble after mount.	25 points detection for the first piece of wafer by lot(4)	4	64	None						
			8		BBD sensor fail to detect blade broken/chipping	1	Check and clean BBD sensor sensitivity per TCM. Quarterly PM to maintain BBD.	25 points detection for the first piece of wafer by lot(4)	4	32	None						
			8		Mishandling operation during wafer inspection	2	Operator follow WI	25 points detection for the first piece of wafer by lot(4) Sample PBI (4)	4	64	None						
	die chipping /crack	electrical failure.(8) Reliability failure(8)	8		uneven wheel mount	2	yearly PM. dressing if unevenness found during blade exchange	25 points detection for the first piece of wafer by lot and auto check every 1~30 lines (4)	4	64	None						

POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

Item: SOIC16/28/32/54ld
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			8		improper installation of saw blade due to contamination on shaft.	1	set checking item in yearly PM plan. check blade shaft before installation and dressing if contamination is found	25 points detection for the first piece of wafer by lot and auto check every 1~30 lines (4)	4	32	None						
			8		spindle speed out of control.	1	control spindle speed within +/- 5% rpm during yearly PM. Check spindle speed per TCM.	25 points detection for the first piece of wafer by lot and auto check every 1~30 lines (4)	4	32	None						
			8		improper blade setup sensitivity.	1	check blade setup sensitivity voltage at pcb during yearly PM	25 points detection for the first piece of wafer by lot and auto check every 1~30 lines (4)	4	32	None						
			8		Incorrect saw blade type	1	Check blade label before installation	Visual check before saw(4)	4	32	None						
			8		BBD sensor fail to detect blade broken/chipping	2	Check and clean BBD sensor sensitivity per TCM. Quarterly PM to maintain BBD.	25 points detection for the first piece of wafer by lot and auto check every 1~30 lines (4)	4	64	None						
			8		Adjust parameters in saw recipe and machine improperly.	2	Check per TCM. Lock saw recipe.	25 points detection for the first piece of wafer of every lot and auto check every 1~30 lines(4)	4	64	None						
			8		Z2 kerf check caused partical attach to Z2 blade.	2	Lock saw recipe.	25 points detection for the first piece of wafer of every lot and auto check every 1~30 lines(4)	4	64	None						

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POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

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Control Number/Issue: 83MCT00002A/BY
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			8		Un-optimized saw blade for solid metal design in saw street	2	SEM inspection to check the saw blade status during new saw blade qualification.	25 points detection for the first piece of wafer of every lot and auto check every 1~30 lines(4)	4	64	None						
	mis-cutting	electrical failure.(8)	8		improper hairline alignment after blade change.	1	Check hairline alignment on dummy mylar after saw blade change.	Visual sample check during saw(5) Machine auto check after piece start(4) Machine auto check every 1~30 lines(4)	4	32	None						
			8		Theta Axis DDM encoder cable fail	2	Change cable during yearly PM	Visual sample check during saw(5)	5	80	None						
	Incomplete Cut	Yield loss (6)	6		Improper dicing parameter or cutting mode	1	Set up per TCM.	Visual sample check during saw(5) Machine auto check after piece start(4) Machine auto check every 1~30 lines(4)	4	24	None						
			6		Uneven chuck table.	1	Check chuck table surface condition during yearly PM. Clean the chuck table per setup check list	Visual sample check during saw(5) Machine auto check after piece start(4) Machine auto check every 1~30 lines(4)	4	24	None						
			6		Improper blade setup sensitivity	1	Check NCS sensitivity when machine setup. Control set up interval below 1x/120 feet per setup checklist	Sample check during saw(5) Machine auto check after piece start(4) Machine auto check every 1~30 lines(4)	4	24	None						

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Prepared By: Amanda Wang
FMEA Date: 05-Oct-94 (Orig.)
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14-Nov-13 (Rev.)

Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	SEV	Class	Potential Cause(s)/ Mechanism(s) of Failue	OCC	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	DET	RPN	Recommended Action(s)	Responsibility & Target Completion Date	Action Results: Actions Taken & Effective Date	SEV	OCC	DET	RPN
	Over Cut	Scrap on D/B for Mylar torn out/pick up failure(6)	6		Improper dicing parameter or cutting mode	1	Set up per TCM.	Visual sample check during saw(5) Machine auto check after piece start(4) Machine auto check every 1~30 lines(4)	4	24	None						
			6		Improper blade setup sensitivity	1	Check NCS sensitivity when machine setup. Control set up interval below 1x/120 feet per setup checklist	Visual sample check during saw(5) Machine auto check after piece start(4) Machine auto check every 1~30 lines(4)	4	24	None						
	Die can't be picked up	Assembly yield loss (6)	6		Incompleted UV	1	Check TCM regularly	Machine auto alarm during DB process (2)	2	12	None						
	Mis-placement	electrical failure.(8) Wire bond alignment error(4) Reliability failure(8)	8		Incomplete UV	2	Check TCM regularly	Visual sample check during DB(5) Post bond inpsection & auto alarm during DB process(2)	2	32	None						
3. Die bond & Epoxy cure	crack /chipping die	Electrical failure.(8) Reliability failure.(8)	8		wrong ejector pin number, pattern, coplanarity, position & tip radius.	2	Select ejector pin number&pattern per B/D, calibrate ejector pin position at center of die when device change	Check the eject pin mark on backside of dummy die (4)	4	64	None						
			8		improper ejector pin height.	2	Adjust eject pin height in the range 0.5~1.2mm per TCM.	Check the eject pin mark on backside of dummy die(4) PM system auto monitor eject pin height and auto alarm if out of control(3)	3	48	None						

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			8		poor epoxy coverage	3	Check epoxy coverage per TCM during DB	Visual sample check during DB(5) OBC/ODC auto alarm(2)	2	48	None						
			8		Incorrect pick up parameters	1	Set up per TCM	Check the pin mark on backside of dummy die(4)	4	32	None						
	epoxy on die	electrical failure(8)	8		die drop.	2	check vacuum efficiency when device change	Auto alarm by die drop sensor(2) Visual sample check during DB(5) Trial run on the first strip after set up(4)	2	32	None						
			8		rubber tip was contaminated	2	divide epoxy pump adjustment work and rubber tip installation work to 2 different person. Operator has no chance to touch the epoxy directly.	Visual sample check during DB(5)	5	80	None						
			8		rubber tip was contaminated by clean paper	2	Operator must use new cleaning paper to scrub the rubber tip	Visual sample check during DB(5)	5	80	None						
			8		excessive epoxy	3	set dispense parameter per positrol log check epoxy expiration date	Visual sample check during DB(5) Trial run on the first strip after set up(4) OBC/ODC auto alarm(2)	2	48	None						
			8		Wrong rubber tip size	2	Check rubber tip size per bonding diagram Change rubber tip per device change	Visual sample check during DB(5) Trial run on the first strip after set up(4)	4	64	None						

POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

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	Improper epoxy coverage	reliability failure.(8) electrical failure.(8) wire bond non-stick (5)	8		improper dispensering position.	2	calibrate dispensering height & position per TCM	Visual sample check during DB(5)	5	80	None						
			8		air trapped in syringe.	2	follow right epoxy thawing procedure.	Visual sample check during DB(5)	5	80	None						
			8		gradient "index"	2	Quarterly PM	Visual sample check during DB(5)	5	80	None						
			8		Incorrect bonding parameter.	1	Check per TCM checklist.	Visual sample check during DB(5)	5	40	None						
	Bent lead	electrical failure.(8)	8		"index" jamming	2	equipped with detect sensor to prevent jamming.	Visual sample check during DB(5)	5	80	None						
	Die scratch	electrical failure.(8) Reliability problem(8)	8		Stained rubber tip.	2	Change rubber tip per SOP.	Visual sample check during DB(5)	5	80	None						
			8		Mishandling operation during sampling inspection	2	Operator follow SOP and WI	Visual sample check during DB(5)	5	80	None						
	mis-placement	electrical failure.(8) Wire bond alignment error(4) Reliability problem(8)	8		bondhead rail worn out.	2	checking during quarterly PM replace with new one during yearly PM.	Visual sample check during DB(5). Post bond inpsection & auto alarm (2)	2	32	None						
			8		"y shuttle" worn out.	2	yearly PM & replace with new one if necessary	Visual sample check during DB(5)	5	80	None						

POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

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			8		improper rubber tip size.	3	Select rubber tip per B/D when device change.	Visual sample check during DB(5) Post bond inpsection & auto alarm (2)	2	48	None						
			8		Improper PRS teaching.	1		Visual sample check during DB(5)	5	40	None						
			8		Improper eject pin set up	1	Calibrate eject when quarterly PM.	Visual sample check during DB(5)	5	40	None						
			8		Epoxy dispensing off center	1	Setup using ink die every device change & die bonder parameter change	Visual sample check during DB(5)	5	40	None						
			8		Rubber tip worn out.	3	Shiftly change the rubber tip.	Visual sample check during DB (5)	5	120	To qualify new rubber tip with the higher hardness. Sev(8) Occ(2) Det(5)	JUN YING ZHENG B09174 05/13/2014					
	Low die shear	Reliablity failure(8)	8		inadequate curing temp/time.	2	Select the proper cure profile per TCM. replace the thermal couple every year calibrate tunnel temp quarterly	Die shear test (4)	4	64	None						
			8		expired epoxy	2	record & check epoxy expiration date per TCM.	Die shear test (4) MMS system alarm (1)	2	32	None						
	L/F discoloration	Reliability failure.(8) Non-stick on lead.(4)	8		Improper N2 flow rate.	2	Check the N2 flow rate per TCM. Set up and mark acceptable flow rate on flow meter	Visual sample check during DB(5)	5	80	None						

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POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

Item: SOIC16/28/32/54ld
Type: ___ Design _x_ Process
Prepared By: Amanda Wang
Core Team: Amanda Wang,H.J. Liu,Ivory Guo,JUN YING ZHENG,XIAOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN

Control Number/Issue: 83MCT00002A/BY
Company,Group,Site/Business Unit: Freescale,TJN-FM
FMEA Date: 05-Oct-94 (Orig.)
14-Nov-13 (Rev.)

Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	SEV	Class	Potential Cause(s)/ Mechanism(s) of Failue	OCC	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	DET	RPN	Recommended Action(s)	Responsibility & Target Completion Date	Action Results: Actions Taken & Effective Date	SEV	OCC	DET	RPN
			8		Improper tunnel temp.	2	Auto alarm when the temperature is too high.	Visual sample check during DB(5) machine auto alarm (2)	2	32	None						
	Bondline thickness issue	Reliability failure(8)	8		improper bond height	1	Autoteach bond height	Visual sample check during DB(5)	5	40	None						
			8		Tilted pick-up holder	1	Quarterly PM	Visual sample check during DB(5)	5	40	None						
			8		Blocked dispenser pump	2	Pump change per 4 days	Sampling measure BLT(5)	5	80	None						
			8		Improper rubbler tip installation	1	Standard operation procedure in WI	Sampling measure BLT(5) Trial run on the first strip after set up(4)	4	32	None						
	Excessive die tilt	W/B bond performance issue(4) Reliability failure(8)	8		Bond head tilt	1	Quarterly PM	Sampling measure BLT (5)	5	40	None						
			8		Wrong dispensing status / setup	1	Dedicated technician for convertion/setup	Measure the die tilt with dummy die before production. (4)	4	32	None						
			8		Impurity in epoxy	2		Measure the die tilt with dummy die before production. (4)	4	64	None						
			8		Wrong rubber tip	1	Check rubber tip size per bonding diagram	Sampling measure BLT(5)	5	40	None						
			8		Bond Force/Scrub settings too low	1	Set up per TCM	Sampling measure BLT (5)	4	32	None						
	Wrong orientation	Wire bond failure(4)	4		Laser sensor failure	2		Visual sample check during DB(5) Daily check the sensor(4)	4	32	None						

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													Action Results				
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	contamination on lead	W/B non-stick(5) Electrical failure(8) reliability failure(8)	8		excessive epoxy	2	set dispense parameter per positrol log. checking epoxy expiration date per TCM	Visual sample check during DB(5) OBC/ODC auto alarm(2)	2	32	None						
			8		inconsistent epoxy dispensing.	2	checking epoxy expiration date per TCM. dispensing vacuum checking per TCM	Visual sample check during DB(5)	5	80	None						
	Too much resin bleed	W/B nonstick(4)	4		L/F quality issue	3	L/F suppliers perform the resin bleed test by lot	Visual sample check during DB(5)	5	60	None						
			4		epoxy quality issue	2		Visual sample check during DB(5)	5	40	None						
	epoxy under/over cure	Reliability failure(8)	8		Curing oven issue	1	Auto locking when curing start and auto alarm when curing finished	Die shear monitor(4); Curing profile monitor(3); Over heat auto alarm(2);	2	16	None						
	epoxy void	Reliability failure(8)	8		Mylar tape residua	1	D870 UV-mylar using integrated UV illumination in Saw machine	Visual sample check during DB(5)	5	40	None						
			8		Wrong dispenser Z-height	2	Auto teach dispenser Z-height	Visual sample check during DB(5)	5	80	None						
	wrong epoxy	Reliability failure(8)	8		Operator select wrong epoxy type	3		Check ASO when device and epoxy change(4) Check epoxy in SFC system(2)	2	48	None						

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	mixed lots	Electrical failure(8)	8		wafer or material mismatch with ASO	3	Genesis system can only move account when the materials being used is match with the BOM.	Visual sample check during DB(5) System auto alarm for BOM mismatch(2)	2	48	None						
	L/F deformation	electrical failure.(8)	8		"index" jamming	2	equipped with detect sensor to prevent jamming.	Visual sample check during DB(5)	5	80	None						
			8		L/F deformation by dispenser needle	2	Control dispenser needle height to L/F no less than 0.15mm Quarterly adjust and calibrate L/F clamp	Visual sample check during DB(5)	5	80	None						
			8		Improper position of L/F input gripper	1	Check L/F picking up motion when setup machine and device change.	Visual sample check during DB(5)	5	40	None						
			8		L/F droped	1		Visual sample check during DB(5).	5	40	None						
			8		Load L/F into cassette directly no bundle protect.	1	Load L/F into cassette with bundle protect	Visual sample check during DB(5).	5	40	None						
	Epoxy expired	Reliability failure(8)	8		Operator miss handling	1		Material system auto alarm for overdue epoxy(2)	2	16	None						
	Excessive epoxy fillet height	Electrical failure(8) Reliability failure(8)	8		Excessive epoxy	2	Set up per TCM	Visual sample check during DB(5) Trial run on the first strip after set up(4) OBC/ODC auto alarm(2)	2	32	None						

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			8		Epoxy off center dispensing	1	Set up per TCM	Machine auto alarm(2) Visual monitor during bonding(4)	2	16	None						
	Epoxy on leadframe backside	Resin bleed happened in mold process (5)	5		Incorrect dispensing pressure & vacuum setting	1	Set up TCM package	Visual sample check during DB (5)	5	25	None						
	Wrong L/F	Wire bond failure(4)	4		Mishandling on L/F selection	1	Check per bonding diagram and assembly shop order. Use index sensor to identify LF. Check the bar code on the LF packaging box	Die bonder auto alarm(2) Visual sample check during DB(5)	2	8	None						
	Wrong die picked (EWM only)	Final Test Yield loss (6)	6		Load wrong wafer map	1	Read barcode (sticked automatically by machine before dicing saw) information automatically on Die bond machine	Visual inspection on wafer skeleton. (5) 100% Electrical Test (5) Visual check on sticked barcode. (4)	4	24	None						
			6		Wrong barcode printed due to scribe ID area is less recognizable	1		Visual inspection on sticked barcode (4)	4	24	None						
			6		Wrong reference die.	1	Verify reference die location with wafer map.	Visual inspection on wafer skeleton. (5) Electrical Test (5)	5	30	None						
	Wrong bin picked (EWM only)	Final Test Yield loss (6)	6		Wrong bin selection	1	Check good die quantity before lot start	Visual inspection on wafer skeleton. (5) Electrical Test (5)	5	30	None						

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	Skip Good Die (EWM only)	Final Test Yield loss (6)	6		Wafer Alignment Problem	1	Die bond machine will stop immediately once met alignment fail.	Machine auto alarm(2) Visual sample check during DB on wafer skeleton(5) Electrical Test (5)	2	12	None						
3.2 Pre-wire bonding plasma clean	Incomplete cleanliness	Nonstick on W/B(5) Delamination after mold(6) Reliability failure(8)	8		Plasma generator malfunction	2	Quarterly PM	Machine auto alarm (2) Measure contact angle on die and Leadframe(5)	2	32	None						
			8		no/insufficient gas/vaccum	2	Quarterly PM	Machine auto alarm (2) Measure contact angle on die and Leadframe(5)	2	32	None						
4. Wire bond (Au wire)	Ball deformation(golf ball, smash ball etc.)	Reliability failure(8) Electrical failure(8)	8		Improper EFO strike pole position condition	2	Quarterly PM	Visual sample check (5) Sample PBI (5)	5	80	None						
			8		USG transfer malfunction	2	Calibrate impedance when changing capillary. Qualified technician can change the capillary.	Visual sample check (5) Sample PBI (5) AutoPBI(5) Machine auto alarm after capillary calibration fails(2)	2	32	None						
			8		Improper wire bond parameters	2	Lock key paramters by PM and only technician or above can change the parameters. Check parameters in TCM.	Visual sample check (5) Sample PBI (5) AutoPBI(5)	5	80	None						

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			8		Missing of bond height teach	1	Machine auto reteach	Visual sample check (5) Sample PBI (5) AutoPBI(5)	5	40	None						
			8		Improper bond force calibration	2	Quarterly PM	Visual sample check (5) Sample PBI (5) AutoPBI(5)	5	80	None						
	Wire damage	Electrical failure (8) Reliability issue(8)	8		Head Block and window clamping malfunction	2	Technician check heat block under microscope quarterly and qualified technician can change heat block. check under	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8		Capillary out of life	1	Set up capillary life limit in wire bonding machine	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4) Machine auto alarm when capillary life exceeds limit(2)	2	16	None						
			8		Wire clamp issue	2	Quarterly PM	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8		Improper bonding parameters	2	Lock the recipe per device Check loop height after set up	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8		Gold wire quality issue	1	IQC imcoming check	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	32	None						
			8		Index malfunction	2	Quarterly PM	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						

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			8		Gold wire path issue	2	Quarterly PM	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8		Lead vibration	1	Leadframe incoming check	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4) Function line test of Leadframe(5)	4	32	None						
			8		Mishandling operation(load magazine, unit inspection,wire change etc)	2	Standardize the inspection method Operators follow SOP and WI	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8		Foreign matter on heat block	1	Technician check heat block under microscope quarterly and qualified technician can change heat block	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	32	None						
	Pad bond & post bond placement	Intermittent electrical fail/short(8) Reliability failure(8)	8		PRS failure	2	PM calibrated PRS when quarterly PM.	Non-stick auto alarm (2) Visual sample check (5) Sample PBI (5) AutoPBI(5)	2	32	None						
			8		x-y table problem	1	PM maintain X-Y table in yearly PM	Non-stick auto alarm (2) Visual sample check (5) Sample PBI (5) AutoPBI(5)	2	16	None						
			8		improper offset between actual tool position & camera	2	teach offset when capillary change	Non-stick auto alarm (2) Visual sample check (5) Sample PBI (5) AutoPBI(5)	2	32	None						

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			8		Improper manual alignment	2	Use special target point to do alignment when setup. Training operators how to using auto alignment instead of manual alignment.	Non-stick auto alarm (2) Visual sample check (5) Sample PBI (5) AutoPBI(5)	2	32	None						
			8		Lens air cooling system issue	2		Non-stick auto alarm (2) Visual sample check (5) Sample PBI (5) AutoPBI(5)	2	32	None						
	Wire deformation(tight,sagging, leaning, smashed,excess loop etc)	Electrical failure(8)	8		Window clamping and heat block issue	2	Technician check heat block under microscope quarterly and qualified technician can change heat block	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8		Wire clamp issue(abrasion, contamination, loose, tighten etc.)	2	Quarterly PM	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8		Improper looping parameters	2	Lock loop parameters	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8		Capillary issue(wrong type, life etc)	1	Check capillary type in TCM and B/D. Capillary life is locked in recipe.	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	32	None						

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			8		Mishandling operation(load magazine, unit inspection,wire change etc)	2	Operators follow SOP and WI	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8		Machine indexer/elevator problem.	2	Yearly PM	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8		Improper die bond placement	2	Die bon placement and orientation control	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
	Cratering	Electrical failure(8) Reliability failure(8)	8		Improper pad bonding parameters	2	Lock key parameters and technician or above can change the parameters; check parameters in TCM	Non-stick auto alarm (2)	2	32	None						
			8		Missing of bond height teach	1	Machine auto reteach	Non-stick auto alarm (2)	2	16	None						
			8		Die quality issue	2		Visual sample check (5) Machine auto alarm(2)	2	32	None						
	Miss bond	Electrical failure(8)	8		Wrong recipe	1	Only process engineers have authority to edit the recipe; wirebond recipe name rule align with bonding diagram no and rev;recipe modification approval system	Visual sample check (5) Sample PBI (5)	5	40	None						

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			8		Mixed devices	1	Check the assembly shop order before lot start.and record the magazine number	Visual sample check (5) Sample PBI (5) PRS Auto alarm(2)	2	16	None						
			8		Wrong wire bond start sequence	2	Lock the " always" start from seleted wire function	Visual sample check (5) Sample PBI (5) PRS Auto alarm(2)	2	32	None						
	Deform Lead frame	Mold flash/resin bleed(4) Electrical failure(8)	8		Index jamming	3	Equipped with detect sensor to prevent jamming. PM check index quarterly	Machine jam alarm(2) Non stick auto alarm (2) Visual sample check (5) Sample PBI (5)	2	48	None						
			8		Window clamping and heat block issue	2	Technician check heat block under microscope quarterly and qualified technician can change heat block.	Machine jam alarm(2) Non stick auto alarm (2) Visual sample check (5) Sample PBI (5)	2	32	None						
			8		Leadframe quality issue	1	Leadframe incoming check;	Machine jam alarm(2) Non stick auto alarm (2) Visual sample check (5) Sample PBI (5) Function line test of Leadfram(5)	2	16	None						

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	Weak bond on pad	Electrical failure(8) Reliability failure(8)	8	*	Insufficient heat transfer/downholder clamping	1	Check heat block quarterly	Ball shear SPC monitor(4) Wire pull SPC monitor(4)	4	32	None						
			8	*	Wafer/Die issue (Pad metal problems:big probe mark; pad scratch,contamination etc)	2	DI water cleaning during saw for wafer	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Wafer incoming check(4)	4	64	None						
			8	*	USG transfer malfunction	1	Calibrate impedance when changing capillary. Qualified technician can change the capillary.	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Machine auto alarm after capillary calibration fails(2)	2	16	None						
			8	*	Capillary issue(wrong type, life etc)	1	Check capillary type in TCM and B/D. Capillary life is locked in recipe.	Ball shear SPC monitor(4) Wire pull SPC monitor(4)	4	32	None						
			8	*	Improper wire bond parameters	2	Lock key parameters and technician or above can change the parameters; check parameters in TCM	Ball shear SPC monitor(4) Wire pull SPC monitor(4)	4	64	None						
			8	*	Floating leadframe(Flag)on heat block.	3	Setup check. Qualified technician do the conversion and teach bond.	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Sample PBI (5) Machine auto alarm when vacuum out of control(2)	2	48	None						

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Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	SEV	Class	Potential Cause(s)/ Mechanism(s) of Failue	OCC	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	DET	RPN	Recommended Action(s)	Responsibility & Target Completion Date	Action Results: Actions Taken & Effective Date	SEV	OCC	DET	RPN
	Weak bond on lead((Stitch bond deformaton , peeling , crack etc)	Electrical failure(8) Reliability failure(8)	8	*	Head Block and window clamping malfunction	2	Technician check heat block under microscope quarterly and qualified technician can change heat block	Visual sample check (5) Sample PBI (5) Wire peel test (4)	4	64	None						
			8	*	USG transfer malfunction	1	Calibrate impedance when changing capillary. Qualified technician can change the capillary.	Visual sample check (5) Sample PBI (5) Wire peel test (4) Machine auto alarm after capillary calibration fails(2)	2	16	None						
			8	*	Capillary issue(wrong type, life etc)	1	Check capillary type in TCM and B/D. Capillary life is locked in recipe.	Visual sample check (5) Sample PBI (5) Wire peel test (4)	4	32	None						
			8	*	Improper wire bond parameters	2	Lock key parameters and technician or above can change the parameters; check paramters in TCM	Visual sample check (5) Sample PBI (5) Wire peel test (4)	4	64	None						

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POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

Item: SOIC16/28/32/54ld
Control Number/Issue: 83MCT00002A/BY
Type: ___ Design _x_ Process
Company,Group,Site/Business Unit: Freescale,TJN-FM
Prepared By: Amanda Wang
FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang,H.J. Liu,Ivory Guo,JUN YING ZHENG,XIAOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN
14-Nov-13 (Rev.)

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			8	*	Leadframe defect before wire bond (contamination, oxidization, lead damage, foreign matter, etc.)	2	Preserve leadframe in cabinet well with N2 gas protection. Hand free method during sample checking Function line test and pick out the defect lead frame Machine cover above work holder Use pre-wire bonding plasma clean	Visual sample check (5) Sample PBI (5) Wire peel test (4)	4	64	None						
			8	*	Insufficient heat transfer/downholder clamping	1	Check heat block quarterly	Visual sample check (5) Sample PBI (5) Wire peel test (4)	4	32	None						
			8	*	Improper second bond position	1	Locked second bond position in recipe	Visual sample check (5) Wire peel test(4)	4	32	None						
			8	*	Mishandling operation(load magazine, unit inspection,wire change etc)	2	Operators follow SOP and WI	Visual sample check (5) Sample PBI (5) Wire peel test(4)	4	64	None						
			8	*	Excessive epoxy	3	Set dispense parameter per positrol log check epoxy expiration date	Visual sample check (5) Setup check before W/B(4) OBC/ODC auto alarm(2)	2	48	None						
			8	*	Foreign matter	2	Monthly cleaning wire bonder index	Visual sample check (5) Sample PBI (5) Wire peel test(4)	4	64	None						

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Control Number/Issue: 83MCT00002A/BY
Company,Group,Site/Business Unit: Freescale,TJN-FM
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	Foreign matter(wire tail, epoxy, particle ect)	Electrical failure(8) Reliability failure(8)	8		Wafer incoming issue	2	DI water cleaning during saw	Visual sample check (5) Sample PBI (5)	5	80	None						
			8		Wire clamper issue(tight,contamination,worn out etc)	2	Wire clamp PM quarterly	Visual sample check (5) Sample PBI (5)	5	80	None						
			8		Mishandling of wire(removing bond off wires, wire theading etc)	3	Standard operation following WI	Visual sample check (5) Sample PBI (5)	5	120	Qualify OCP (Out Chamfer Polish) Capillary on COSSLITE_TSMC to improve the 2nd bond performance. Sev(8) Occ(2) Det(5)	SHUAN YAO B07524/05-11-2014					
			8		Epoxy on lead or die	2	Die bond fillet height and resin bleed control	Visual sample check (5) Sample PBI (5)	5	80	None						
			8		Particles in air	2	Operation following FE cleaning room SOP	Visual sample check (5) Sample PBI (5)	5	80	None						
	Non stick on pad	Electrical failure (8)	8		Insufficient heat transfer/downholder clamping	1	Check heat block quarterly	Non stick auto alarm(2) Ball shear SPC monitor(4) Wire pull SPC monitor(4)	2	16	None						
			8		Wafer/die issue (Pad metal problems:big probe mark; pad scratch,contamination etc)	2	DI water cleaning during saw for wafer	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Wafer incoming check(4) Non stick auto alarm(2)	2	32	None						

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			8		USG transfer malfunction	1	Calibrate impedance when changing capillary. Qualified technician can change the capillary.	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Machine auto alarm after capillary calibration fails(2) Non stick auto alarm(2)	2	16	None						
			8		Capillary issue(wrong type, life etc)	1	Check capillary type in TCM and B/D. Capillary life is locked in recipe.	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Non stick auto alarm(2)	2	16	None						
			8		Improper wire bond parameters	2	Lock key parameters and technician or above can change the parameters; check paramter in TCM	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Non stick auto alarm(2)	2	32	None						
			8		Floating leadframe(Flag) on heat block.	2	Setup check. Qualified technician do the conversion and teach bond.	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Machine auto alarm when vacuum out of control(2) Non stick auto alarm(2)	2	32	None						
	Non stick on lead	Electrical failure (8)	8		Head Block and window clamping malfunction	2	Technician check heat block under microscope quarterly and qualified technician can change heat block	Visual sample check (5) Sample PBI (5) Wire peel test (4) Non stick auto alarm(2)	2	32	None						

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			8		USG transfer malfunction	1	Calibrate impedance when changing capillary. Qualified technician can change the capillary.	Visual sample check (5) Sample PBI (5) Wire peel test (4) Machine auto alarm after capillary calibration fails(2) Non stick auto alarm(2)	2	16	None						
			8		Capillary issue(wrong type, life etc)	1	Check capillary type in conversion checklist and B/D. Capillary life is locked in recipe	Visual sample check (5) Sample PBI (5) Wire peel test (4) Non stick auto alarm(2)	2	16	None						
			8		Improper wire bond parameters	2	Lock key parameters and technician or above can change the parameters; check paramter in TCM	Visual sample check (5) Sample PBI (5) Wire peel test (4) Non stick auto alarm(2)	2	32	None						

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			8		Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)	2	Preserve leadframe in cabinet well with N2 gas protection. Hand free method during sample checking Function line test and pick out the defect lead frame Machine cover above work holder Use pre-wire bonding plasma clean.(only for bga ,lga sony, leaded pkgs)	Visual sample check (5) Sample PBI (5) Wire peel test (4) Non stick auto alarm(2)	2	32	None						
			8		Insufficient heat transfer/downholder clamping	1	Check heat block quarterly	Visual sample check (5) Sample PBI (5) Wire peel test (4) Non stick auto alarm(2)	2	16	None						
	Excessive "Tail" on reverse bond	Eletrcial failure (8)	8		Improper wire bond parameters	2	Lock key parameters and technician or above can change the parameters; check paramter in TCM	Visual sample check (5) Sample PBI (5)	5	80	None						
	Wrong wire type used	Reliability failure(8) Electrical failure(8)	8		Mishandling on wrong wire type	1	Follow assembly shop order and SFC system control	SFC auto alarm when material part number not match with system record(2)	2	16	None						

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	Ball neck crack	Electrical failure(8) Reliability failure(8)	8		Incorrect parameters on first bond and loop formation	2	Lock loop parameters; Lock key parameters and technician or above can change the parameters; Check paramters in TCM	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
4. Wire bond (Cu wire)	Ball deformation(golf ball, smash ball etc.)	Reliability failure(8) Electrical failure(8)	8		Improper EFO strike pole position condition	2	Quarterly PM	Visual sample check (5) Sample PBI (5)	5	80	None						
			8		USG transfer malfunction	2	Calibrate impedance when changing capillary. Qualified technician can change the capillary.	Visual sample check (5) Sample PBI (5) AutoPBI(5) Machine auto alarm after capillary calibration fails(2)	2	32	None						
			8		Improper wire bond parameters	2	Lock key paramters by PM and only technician or above can change the parameters. Check parameters in TCM.	Visual sample check (5) Sample PBI (5) AutoPBI(5)	5	80	None						
			8		Missing of bond height teach	1	Machine auto reteach	Visual sample check (5) Sample PBI (5) AutoPBI(5)	5	40	None						
			8		Improper bond force calibration	2	Quarterly PM	Visual sample check (5) Sample PBI (5) AutoPBI(5)	5	80	None						

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			8		Cu wire oxidation	4	Cu wire shelf life and work life control; Forming gas flow monitor(auto)	Visual sample check (5) Sample PBI (5) AutoPBI(5) Machine auto alarm when forming gas flow out of control(2) Material system auto alarm when Cu wire expired shelf life or work life(2)	2	64	None						
	Wire damage	Electrical failure (8) Reliability issue(8)	8		Head Block and window clamping malfunction	2	Technician check heat block under microscope quarterly and qualified technician can change heat block. check under	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8		Capillary out of life	1	Set up capillary life limit in wire bonding machine	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4) Machine auto alarm when capillary life exceeds limit(2)	2	16	None						
			8		Wire clamp issue	2	Quarterly PM	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8		Improper bonding parameters	2	Lock the recipe per device Check loop height after set up	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						

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			8		Copper wire quality issue	1	IQC imcoming check	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	32	None						
			8		Index malfunction	2	Quarterly PM	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8		Copper wire path issue	2	Quarterly PM	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8		Lead vibration	1	Leadframe incoming check	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4) Function line test of Leadframe(5)	4	32	None						
			8		Mishandling operation(load magazine, unit inspection,wire change etc)	2	Standardize the inspection method Operators follow SOP and WI	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8		Foreign matter on heat block	1	Technician check heat block under microscope quarterly and qualified technician can change heat block	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	32	None						
	Pad bond & post bond placement	Intermittent electrical fail/short(8) Reliability failure(8)	8		PRS failure	2	PM calibrated PRS when quarterly PM.	Non-stick auto alarm (2) Visual sample check (5) Sample PBI (5) AutoPBI(5)	2	32	None						
			8		x-y table problem	1	PM maintain X-Y table in yearly PM	Non-stick auto alarm (2) Visual sample check (5) Sample PBI (5) AutoPBI(5)	2	16	None						

POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

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			8		improper offset between actual tool position & camera	2	teach offset when capillary change	Non-stick auto alarm (2) Visual sample check (5) Sample PBI (5) AutoPBI(5)	2	32	None						
			8		Improper manual alignment	2	Use special target point to do alignment when setup. Training operators how to using auto alignment instead of manual alignment.	Non-stick auto alarm (2) Visual sample check (5) Sample PBI (5) AutoPBI(5)	2	32	None						
			8		Lens air cooling system issue	2		Non-stick auto alarm (2) Visual sample check (5) Sample PBI (5) AutoPBI(5)	2	32	None						
	Wire deformation(tight,sagging, leaning, smashed,excess loop etc)	Electrical failure(8)	8		Window clamping and heat block issue	2	Technician check heat block under microscope quarterly and qualified technician can change heat block	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8		Wire clamp issue(abrasion, contamination, loose, tighten etc.)	2	Quarterly PM	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						

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			8		Improper looping parameters	2	Lock loop parameters	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8		Capillary issue(wrong type, life etc)	1	Check capillary type in TCM and B/D. Capillary life is locked in recipe.	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	32	None						
			8		Mishandling operation(load magazine, unit inspection,wire change etc)	2	Operators follow SOP and WI	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8		Machine indexer/elevator problem.	2	Yearly PM	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
			8		Improper die bond placement	2	Die bon placement and orientation control	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
	Cratering	Electrical failure(8) Reliability failure(8)	8		Improper pad bonding parameters	2	Lock key parameters and technician or above can change the parameters; check parameters in TCM	Non-stick auto alarm (2)	2	32	None						
			8		Missing of bond height teach	1	Machine auto reteach	Non-stick auto alarm (2)	2	16	None						
			8		Die quality issue	2		Visual sample check (5) Machine auto alarm(2)	2	32	None						

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	Miss bond	Electrical failure(8)	8		Wrong recipe	1	Only process engineers have authority to edit the recipe; wirebond recipe name rule align with bonding diagram no and rev;recipe modification approval system	Visual sample check (5) Sample PBI (5)	5	40	None						
			8		Mixed devices	1	Check the assembly shop order before lot start.and record the magazine number	Visual sample check (5) Sample PBI (5) PRS Auto alarm(2)	2	16	None						
			8		Wrong wire bond start sequence	2	Lock the " always" start from seleted wire function	Visual sample check (5) Sample PBI (5) PRS Auto alarm(2)	2	32	None						
	Deform Lead frame	Mold flash/resin bleed(4) Electrical failure(8)	8		Index jamming	3	Equipped with detect sensor to prevent jamming. PM check index quarterly	Machine jam alarm(2) Non stick auto alarm (2) Visual sample check (5) Sample PBI (5)	2	48	None						

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			8		Window clamping and heat block issue	2	Technician check heat block under microscope quarterly and qualified technician can change heat block.	Machine jam alarm(2) Non stick auto alarm (2) Visual sample check (5) Sample PBI (5)	2	32	None						
			8		Leadframe quality issue	1	Leadframe incoming check;	Machine jam alarm(2) Non stick auto alarm (2) Visual sample check (5) Sample PBI (5) Function line test of Leadfram(5)	2	16	None						
	Weak bond on pad	Electrical failure(8) Reliability failure(8)	8	*	Insufficient heat transfer/downholder clamping	1	Check heat block quarterly	Ball shear SPC monitor(4) Wire pull SPC monitor(4)	4	32	None						
			8	*	Wafer/Die issue (Pad metal problems:big probe mark; pad scratch,contamination etc)	2	DI water cleaning during saw for wafer	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Wafer incoming check(4)	4	64	None						
			8	*	USG transfer malfunction	1	Calibrate impedance when changing capillary. Qualified technician can change the capillary.	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Machine auto alarm after capillary calibration fails(2)	2	16	None						

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FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang,H.J. Liu,Ivory Guo,JUN YING ZHENG,XIAOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN
14-Nov-13 (Rev.)

Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	SEV	Class	Potential Cause(s)/ Mechanism(s) of Failue	OCC	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	DET	RPN	Recommended Action(s)	Responsibility & Target Completion Date	Action Results: Actions Taken & Effective Date	SEV	OCC	DET	RPN
			8	*	Capillary issue(wrong type, life etc)	1	Check capillary type in TCM and B/D. Capillary life is locked in recipe.	Ball shear SPC monitor(4) Wire pull SPC monitor(4)	4	32	None						
			8	*	Improper wire bond parameters	2	Lock key parameters and technician or above can change the parameters; check parameters in TCM	Ball shear SPC monitor(4) Wire pull SPC monitor(4)	4	64	None						
			8	*	Floating leadframe(Flag)on heat block.	3	Setup check. Qualified technician do the conversion and teach bond.	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Sample PBI (5) Machine auto alarm when vacuum out of control(2)	2	48	None						
			8		Cu wire oxidation	4	Cu wire shelf life and work life control; Forming gas flow monitor(auto)	Ball shear SPC monitor(4) Wire pull SPC monitor (4) Machine auto alarm when forming gas flow out of control(2) Material system auto alarm when Cu wire expired shelf life or work life(2)	2	64	None						

POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

Item: SOIC16/28/32/54ld
Type: ___ Design _x_ Process
Prepared By: Amanda Wang
Core Team: Amanda Wang,H.J. Liu,Ivory Guo,JUN YING ZHENG,XIAOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN

Control Number/Issue: 83MCT00002A/BY
Company,Group,Site/Business Unit: Freescale,TJN-FM
FMEA Date: 05-Oct-94 (Orig.)
14-Nov-13 (Rev.)

Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	SEV	Class	Potential Cause(s)/ Mechanism(s) of Failue	OCC	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	DET	RPN	Recommended Action(s)	Responsibility & Target Completion Date	Action Results: Actions Taken & Effective Date	SEV	OCC	DET	RPN
	Weak bond on lead((Stitch bond deformaton , peeling , crack etc)	Electrical failure(8) Reliability failure(8)	8	*	Head Block and window clamping malfunction	2	Technician check heat block under microscope quarterly and qualified technician can change heat block	Visual sample check (5) Sample PBI (5) Wire peel test (4)	4	64	None						
			8	*	USG transfer malfunction	1	Calibrate impedance when changing capillary. Qualified technician can change the capillary.	Visual sample check (5) Sample PBI (5) Wire peel test (4) Machine auto alarm after capillary calibration fails(2)	2	16	None						
			8	*	Capillary issue(wrong type, life etc)	1	Check capillary type in TCM and B/D. Capillary life is locked in recipe.	Visual sample check (5) Sample PBI (5) Wire peel test (4)	4	32	None						
			8	*	Improper wire bond parameters	2	Lock key parameters and technician or above can change the parameters; check paramters in TCM	Visual sample check (5) Sample PBI (5) Wire peel test (4)	4	64	None						

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			8	*	Leadframe defect before wire bond (contamination, oxidization, lead damage, foreign matter, etc.)	2	Preserve leadframe in cabinet well with N2 gas protection. Hand free method during sample checking Function line test and pick out the defect lead frame Machine cover above work holder Use pre-wire bonding plasma clean	Visual sample check (5) Sample PBI (5) Wire peel test (4)	4	64	None						
			8	*	Insufficient heat transfer/downholder clamping	1	Check heat block quarterly	Visual sample check (5) Sample PBI (5) Wire peel test (4)	4	32	None						
			8	*	Improper second bond position	1	Locked second bond position in recipe	Visual sample check (5) Wire peel test(4)	4	32	None						
			8	*	Mishandling operation(load magazine, unit inspection,wire change etc)	2	Operators follow SOP and WI	Visual sample check (5) Sample PBI (5) Wire peel test(4)	4	64	None						
			8	*	Excessive epoxy	3	Set dispense parameter per positrol log check epoxy expiration date	Visual sample check (5) Setup check before W/B(4) OBC/ODC auto alarm(2)	2	48	None						
			8	*	Foreign matter	2	Monthly cleaning wire bonder index	Visual sample check (5) Sample PBI (5) Wire peel test(4)	4	64	None						

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			8		Cu wire oxidation	4	Cu wire shelf life and work life control; Forming gas flow monitor(auto)	Ball shear SPC monitor(4) Wire pull SPC monitor (4) Machine auto alarm when forming gas flow out of control(2) Material system auto alarm when Cu wire expired shelf life or work life(2)	2	64	None						
	Foreign matter(wire tail, epoxy, particle ect)	Electrical failure(8) Reliability failure(8)	8		Wafer incoming issue	2	DI water cleaning during saw	Visual sample check (5) Sample PBI (5)	5	80	None						
			8		Wire clamper issue(tight,contamination,worn out etc)	2	Wire clamp PM quarterly	Visual sample check (5) Sample PBI (5)	5	80	None						
			8		Mishandling of wire(removing bond off wires, wire theading etc)	2	Standard operation following WI	Visual sample check (5) Sample PBI (5)	5	80	None						
			8		Epoxy on lead or die	2	Die bond fillet height and resin bleed control	Visual sample check (5) Sample PBI (5)	5	80	None						

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			8		Particles in air	2	Operation following FE cleaning room SOP	Visual sample check (5) Sample PBI (5)	5	80	None						
	Non stick on pad	Electrical failure (8)	8		Insufficient heat transfer/downholder clamping	1	Check heat block quarterly	Non stick auto alarm(2) Ball shear SPC monitor(4) Wire pull SPC monitor(4)	2	16	None						
			8		Wafer/die issue (Pad metal problems:big probe mark; pad scratch,contamination etc)	2	DI water cleaning during saw for wafer	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Wafer incoming check(4) Non stick auto alarm(2)	2	32	None						
			8		USG transfer malfunction	1	Calibrate impedance when changing capillary. Qualified technician can change the capillary.	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Machine auto alarm after capillary calibration fails(2) Non stick auto alarm(2)	2	16	None						
			8		Capillary issue(wrong type, life etc)	1	Check capillary type in TCM and B/D. Capillary life is locked in recipe.	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Non stick auto alarm(2)	2	16	None						
			8		Improper wire bond parameters	2	Lock key parameters and technician or above can change the parameters; check paramter in TCM	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Non stick auto alarm(2)	2	32	None						

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			8		Floating leadframe(Flag) on heat block.	2	Setup check. Qualified technician do the conversion and teach bond.	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Machine auto alarm when vacuum out of control(2) Non stick auto alarm(2)	2	32	None						
			8		Cu wire oxidation	4	Cu wire shelf life and work life control; Forming gas flow monitor(auto)	Ball shear SPC monitor(4) Wire pull SPC monitor(4) Machine auto alarm when forming gas flow out of control(2) Material system auto alarm when Cu wire expired shelf life or work life(2) Non stick auto alarm(2)	2	64	None						
	Non stick on lead	Electrical failure (8)	8		Head Block and window clamping malfunction	2	Technician check heat block under microscope quarterly and qualified technician can change heat block.	Visual sample check (5) Sample PBI (5) Wire peel test (4) Non stick auto alarm(2)	2	32	None						
			8		USG transfer malfunction	1	Calibrate impedance when changing capillary. Qualified technician can change the capillary.	Visual sample check (5) Sample PBI (5) Wire peel test (4) Machine auto alarm after capillary calibration fails(2) Non stick auto alarm(2)	2	16	None						

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			8		Capillary issue(wrong type, life etc)	1	Check capillary type in conversion checklist and B/D. Capillary life is locked in recipe	Visual sample check (5) Sample PBI (5) Wire peel test (4) Non stick auto alarm(2)	2	16	None						
			8		Improper wire bond parameters	2	Lock key parameters and technician or above can change the parameters; check paramter in TCM	Visual sample check (5) Sample PBI (5) Wire peel test (4) Non stick auto alarm(2)	2	32	None						
			8		Leadframe defect before wire bond (contamination, oxidization, lead damage,etc.)	2	Preserve leadframe in cabinet well with N2 gas protection. Hand free method during sample checking Function line test and pick out the defect lead frame Machine cover above work holder Use pre-wire bonding plasma clean.(only for bga ,lga sony, leaded pkgs)	Visual sample check (5) Sample PBI (5) Wire peel test (4) Non stick auto alarm(2)	2	32	None						
			8		Insufficient heat transfer/downholder clamping	1	Check heat block quarterly	Visual sample check (5) Sample PBI (5) Wire peel test (4) Non stick auto alarm(2)	2	16	None						

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			8		Cu wire oxidation	4	Cu wire shelf life and work life control; Forming gas flow monitor(auto)	Wire peel test (4) Machine auto alarm when forming gas flow out of control(2) Material system auto alarm when Cu wire expired shelf life or work life(2) Non stick auto alarm(2)	2	64	None						
	Excessive "Tail" on reverse bond	Eletrcial failure (8)	8		Improper wire bond parameters	2	Lock key parameters and technician or above can change the parameters; check paramter in TCM	Visual sample check (5) Sample PBI (5)	5	80	None						
	Wrong wire type used	Reliability failure(8) Electrical failure(8)	8		Mishandling on wrong wire type	1	Follow assembly shop order and SFC system control	SFC auto alarm when material part number not match with system record(2)	2	16	None						
	Ball neck crack	Electrical failure(8) Reliability failure(8)	8		Incorrect parameters on first bond and loop formation	2	Lock loop parameters; Lock key parameters and technician or above can change the parameters; Check paramters in TCM	Visual sample check (5) Sample PBI (5) Wire pull SPC monitor(4)	4	64	None						
5.1 Pre-mold plasma clean	Incomplete cleanliness	Delamination after mold(6) Reliability issue(8)	8		Plasma generator malfunction	2	Quarterly PM	Machine auto alarm (2) Measure contact angle on die and Leadframe(5)	2	32	None						

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			8		No/Insufficient gas/Vaccum	2	Quarterly PM	Machine auto alarm (2) Measure contact angle on die and Leadframe(5)	2	32	None						
6. Mold	Mismatch / off-center	Package chip/crack (6)	6		Mold chase top and bottom cavity mismatch.	2	Half-yearly PM	First-piece check by microscope (4)	4	48	None						
			6		Location pin & set block worn out	2	Half-yearly PM	First-piece check by microscope (4)	4	48	None						
	Wire damaged	Electrical failure. (8) Reliability defect (8)	8		Loader catch hooker misalignment	2	Monthly PM	First-piece check by X-ray (4) Sampling check by X-ray(5) Machine auto alarm(2)	2	32	None						
			8		Incorrect input buffer pusher position	2	Monthly PM	First-piece check by X-ray (4) Sampling check by X-ray(5) Machine auto alarm(2)	2	32	None						
			8		Incorrect input buffer pusher position	2	Monthly PM	First-piece check by X-ray (4) Sampling check by X-ray(5) Machine auto alarm(2)	2	32	None						
			8		Magazine falls on floor and wire is touched by operator	2	Follow standard handling requirment	First-piece check by X-ray(4) Sampling check by X-ray(5)	4	64	None						
			8		Loader does not catch lead frame well	2	Monthly PM	First-piece check by X-ray(4) Sampling check by X-ray(5) Machine auto alarm(2)	2	32	None						

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	Mold flash/ resin bleed	Electrical failure(8) Solderability failure (8)	8		Foreign matter on mold cavity	2	Trial run dummy after mold cleaning and conditioning; Clean vacuum box shiftly; Change pot&plunger while worn out	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection (3)	3	48	None						
			8		Expose pad is deformed before molding	2	Monthly PM; Follow standard handling requirement	First-piece check by microscope(4) Sampling check(5) 100% final visual inspection (3)	3	48	None						
			8		Incorrect mold parameters setting	2	Set up parameter per TCM	First-piece check by microscope(4) Sampling check(5) 100% final visual inspection(3) Machine auto alarm(2)	2	32	None						
			8		Load strip in wrong position	2	Monthly PM	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection (3) Machine auto alarm (2)	2	32	None						
	External void/Incomplete fill	Visual reject(4)	4		Incorrect process parameters setting	2	Set up parameter per TCM	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection(3) Machine auto alarm (2)	2	16	None						

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			4		Air vent block	2	Perform mold cleaning and conditioning daily at least; Trial run dummy after cleaning and conditioning	First-piece check by microscope(4) Sampling check(5) 100% final visual inspection(3)	3	24	None						
			4		Runner block	2	Perform mold cleaning and conditioning regularly daily at least; Trial run dummy after cleaning and conditioning	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection(3)	3	24	None						
			4		Plunger jam	2	Monthly PM	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection(3) Machine auto alarm (2)	2	16	None						
			4		Mold cavity is dirty	2	Perform mold cleaning and conditioning daily at least; Trial run dummy after cleaning and conditioning	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection(3)	4	32	None						
			4		Gate insert block	2	Perform mold cleaning and conditioning daily at least; Trial run dummy after cleaning and conditioning	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection(3)	4	32	None						

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			4		Use expired or unthawy compound	2	Genesis system control	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection(3) System alarm (2)	2	16	None						
			4		Unsuitable Tablet size	2	Tablet length sensor check	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection(3) Machine auto alarm (2)	2	16	None						
			4		Mold die temperature out of control	2	Real time PID control	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection(3) Machine auto alarm (2)	2	16	None						
			4		Inproper eject pin dimension	3	PM check the matching(type, dimension etc.) before eject pin chane. Clean the eject pin holder and mold chase basic board monthly	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection(3)	3	36	None						
			4		Use wrong type compound	2	Clean out the compound when compound is converted,then double check by operator/leader; Genesis system control	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection(3) System alarm(2)	2	16	None						

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	Wire sweep	Electrical failure (8)	8		Incorrect process parameter	2	Set up parameter per TCM	First-piece check by X-ray (4) Sampling check by X-ray (5) Machine auto alarm (2)	2	32	None						
			8		Use expired or unthawy compound	2	Genesis system control	First-piece check by X-ray (4) Sampling check by X-ray (5)	4	64	None						
			8		Use expired or unthawy compound	2	Genesis system control	First-piece check by X-ray (4) Sampling check by X-ray (5)	4	64	None						
			8		Magazine falls on floor and wire touched by operator	2	Follow standard handling requirment	First-piece check by X-ray (4) Sampling check by X-ray (5)	4	64	None						
			8		Magazine falls on floor and wire touched by operator	2	Follow standard handling requirment	First-piece check by X-ray (4) Sampling check by X-ray (5)	4	64	None						
			8		Mold die temperature out of control	2	Real time PID control	First-piece check by X-ray (4) Sampling check by X-ray (5) Machine auto alarm(2)	2	32	None						
			8		Mold die temperature out of control	2	Real time PID control	First-piece check by X-ray (4) Sampling check by X-ray (5) Machine auto alarm(2)	2	32	None						

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POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

Item: SOIC16/28/32/54ld
Control Number/Issue: 83MCT00002A/BY
Type: ___ Design _x_ Process
Company,Group,Site/Business Unit: Freescale,TJN-FM
Prepared By: Amanda Wang
FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang,H.J. Liu,Ivory Guo,JUN YING ZHENG,XIAOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN
14-Nov-13 (Rev.)

Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	SEV	Class	Potential Cause(s)/ Mechanism(s) of Failue	OCC	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	DET	RPN	Recommended Action(s)	Responsibility & Target Completion Date	Action Results: Actions Taken & Effective Date	SEV	OCC	DET	RPN
			8		Use wrong type compound	2	Clean out the compound when compound is converted,then double check by operator/leader; Genesis system control	First-piece check by X-ray (4) Sampling check by X-ray (5) System alarm(2)	2	32	None						
	Pitting	Visual reject (4)	4		Mold die temperature out of control	2	Real time PID control	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection(3) Machine auto alarm(2)	2	16	None						
			4		Air vent block	2	Perform mold cleaning and conditioning daily at least; trial run dummy after cleaning and conditioning	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection(3)	3	24	None						
			4		Air vent block	2	Perform mold cleaning and conditioning daily at least; trial run dummy after cleaning and conditioning	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection(3)	3	24	None						
			4		Incorrect process parameters setting	2	Set up parameter per TCM	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection(3) Machine auto alarm (2)	2	16	None						

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Control Number/Issue: 83MCT00002A/BY
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			4		Incorrect process parameter setting	2	Set up parameter per TCM	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection(3) Machine auto alarm (2)	2	16	None						
			4		Mold chase cavity is dirty	2	Perform cleaning and conditioning daily at least; trial run dummy after cleaning and conditioning	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection(3)	3	24	None						
			4		Mold chase cavity is dirty	2	Perform cleaning and conditioning daily at least; trial run dummy after cleaning and conditioning	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection(3)	3	24	None						
	Package protrusion	Visual reject (4) Solderability(8)	8		Eject pin worn out	2	Half-yearly PM	First-piece check by microscope (4) Sampling check (5) 100% final visual inspection(3)	3	48	None						
	Mold package by wrong molding tool	Visual reject (4) Customer difficult application(8)	8		Use wrong mold chase	1	To verify the package dimension before production start; Loader with different sensors to identify different pkg type	First-piece check by microscope (4) Machine auto Alarm(2)	2	16	None						
	Mold Package Microcrack	Reliability failure(8) Electrical failure(8)	8		Improper degator position setting	2	Monthly PM	Sampling check by microscope(5)	5	80	None						

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			8		Mold cavity is too sticky	2	Perform mold cleaning and conditioning daily at least	Sampling check by microscope(5)	5	80	None						
	Delamination	Reliability failure (8)	8		Incorrect process parameters setting	2	Set up parameter per TCM and check oven temperature shiftly	Regular CSAM inspection (5) Machine auto alarm (2)	2	32	None						
			8		Use expired or unthawy compound	2	Genesis system control	Regular CSAM inspection(5) System alarm(2)	2	32	None						
			8		Leadframe is over oxidated on mold die	2	Take out L/F promptly while equipement alarm	Regular CSAM inspection (5)	5	80	None						
			8		Leadframe contaminated	1	N2 protection in storage area	Regular CSAM inspection(5)	5	40	None						
			8		Plasma clean expiration	2	Genesis system control	System alarm(2)	2	32	None						
			8		Internal stress caused by Leadframe warpage (Fused leadframe 17ASH70187A61 2)	2		Regular CSAM inspection(5)	5	80	None						
			8		Use wrong type compound	2	Clean out the compound when compound is converted,then double check by operator/leader; Genesis system control	Regular CSAM inspection(5) System alarm(2)	2	32	None						

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	Foreign matter in package	Visual reject(4)	4		Compound residual around pot	2	Try run dummy after cleaning and conditioning; Clean vacuum box shiftly; Change pot&plunger while worn out Clean mold surface post each shot by auto cleaner	Regular CSAM inspection(5)	5	40	None						
	Cull remain	package chip/crack(6)	6		Insufficient cure time	2	Setup parameter per TCM	Sampling check(5) Machine auto alarm (2)	2	24	None						
			6		Improper degator position setting	2	Monthly PM	Sampling check(5)	5	60	None						
			6		Use expired or unthawy compound	2	Genesis system control	Sampling check(5) System auto alarm(2)	2	24	None						
			6		Operator break cull manually	2	Forbid break cull manually	Sampling check(5)	5	60	None						
			6		Mold cavity is too sticky	2	Perform mold cleaning and conditioning daily at least	Sampling check(5)	5	60	None						
	Internal void	Reliability failure (8)	8		Runner block	2	Perform mold cleaning and conditioning regularly daily at least; Trial run dummy after cleaning and conditioning	First-piece check by X-ray (4) Sampling check by X-ray (5)	4	64	None						

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			8		Air vent block	2	Perform mold cleaning and conditioning daily at least; Trial run dummy after cleaning and conditioning	First-piece check by X-ray (4) Sampling check by X-ray (5)	4	64	None						
			8		Gate insert block	2	Perform mold cleaning and conditioning regularly daily at least; Trial run dummy after cleaning and conditioning	First-piece check by X-ray (4) Sampling check by X-ray (5)	4	64	None						
			8		Plunger jam	2	Mothly PM	First-piece check by X-ray (4) Sampling check by X-ray (5) Machine auto alarm(2)	2	32	None						
			8		Incorrect process parameter setting	2	Set up parameter per TCM	First-piece check by X-ray (4) Sampling check by X-ray (5)	4	64	None						
			8		Use expired compound or unthawy compound	2	Genesis system control	First-piece check by X-ray (4) Sampling check by X-ray (5) System auto alarm(2)	2	32	None						
			8		Mold die temperature out of control	2	Real time PID control	First-piece check by X-ray (4) Sampling check by X-ray (5) Machine auto alarm(2)	2	32	None						

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			8		Unsuitable tablet size	2	Tablet length sensor checking	First-piece check by X-ray (4) Sampling check by X-ray (5) Machine auto alarm(2)	2	32	None						
			8		Use wrong type compound	2	Clean out the compound when compound is converted,then double check by operator/leader; Genesis system control	First-piece check by X-ray (4) Sampling check by X-ray (5) System alarm(2)	2	32	None						
7. Marking	missing mark	Reject by visual inspection or vision system(4)	4		L/F input sensor accidently disable.	1	Check L/F input sensor status shiftly, dummy L/F check by Assy. lot.	sensor auto alarm(2) Visual sample check after marking(5)100% final visual inspection(3)	2	8	None						
			4		Laser lamp broken.	1	Check the laser power value shiftly, dummy L/F check by Assy. lot.	Machine auto alarm(2) Visual sample check after marking(5)100% final visual inspection(3)	2	8	None						
	illegible mark	Reject by visual inspection or vision system(4)	4		wrong laser power	2	Check the laser power value shiftly, dummy L/F check by Assy. lot. Monthly change laser lamp.	Visual sample check after marking(5) QA visual inspection 200 units/lot(4) 100% final visual inspection(3)	3	24	None						
			4		low vacuum suck	1	Clean dust collector shiftly, dummy L/F check by Assy. lot.	Visual sample check after marking(5) QA visual inspection 200 units/lot(4) 100% final visual inspection(3)	3	12	None						

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	misalignment	Reject by visual inspection or vision system(4)	4		leadframe wrong location	1	Dummy L/F check by Assy. lot. Check the orientation sensor shiftly.	Machine auto alarm(2) Visual sample check after marking(5)100% final visual inspection(3) QA visual inspection 200 units/lot(4)	2	8	None						
			4		Incorrect marking parameters settings	3	Dummy marking before production start	Visual sample check after marking(5)100% final visual inspection(3) QA visual inspection 200 units/lot(4)	3	36	None						
	reverse mark	Reject by visual inspection or vision system(4)	4		L/F orientation fail	2	Check the orientation sensor shiftly. dummy L/F check by Assy. lot	Visual sample check after marking(5)100% final visual inspection(3)	3	24	None						
	crack	reliability failure.(8)	8		Lead fame jamed on track.	1	Check rail status. dummy L/F check by Assy. lot. Regular PM	sensor auto alarm(2) Visual sample check after marking(5)100% final visual inspection(3)	2	16	None						
	Wrong marking	Reject by visual inspection or vision system(4)	4		Auto marking information error	2	Marking confirmation with dummy L/F by Assy. lot.	Visual sample check after marking(5) QA visual inspection 200 units/lot(4) 100% final visual inspection(3)	3	24	None						
8. Post mold cure	Overcure	Reliability failure (8)	8		Temperature excursion	2	Set up parameter per TCM and check oven temperature shiftly	Visual check temperature meter(6) Machine auto alarm (2)	2	32	None						
	Undercure	Reliability failure (8)	8		Temperature excursion	2	Set up parameter per TCM and check oven temperature shiftly	Visual check temperature meter(6) Machine auto alarm (2)	2	32	None						

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			8		Insufficient cure time	2	Check cure shiftly per TCM; Mothly PM	Visual check temperature meter(6) Machine auto alarm (2)	2	32	None						
	Non Cure	Reliability failure (8)	8		Missing PMC	1	Genesis system control	System alarm(2)	2	16	None						
9. plating (not applicable for PPF L/F)	bent lead	Electrical Failure (8)	8		load,unload jam	2	Check Adjustment load and unload system monthly & half-year by PM	Visual sample check after plating(5) Auto alarm(2)	2	32	None						
			8		Jam in process cell	2	Check/Adjustment belt, air knivies monthly by PM	Visual sample check after plating(5) Auto alarm(2)	2	32	None						
			8		Jam in high pressure water rinse	2	Check rinse nozzle monthly by PM; Check per positrol log shiftly	Visual sample check after plating(5) Auto alarm(2)	2	32	None						
	discoloration & stain	Solderability Failure(8)	8		Insufficient air knives flow	1	Check air knives monthly by PM; Clean air nozzle and mechanical structure monthly by PM.	Visual sample check after plating(5)	5	40	None						
			8		Insufficient water rinse	2	Check rinse nozzle monthly by PM; Check rinse per setup checklist shiftly	Visual sample check after plating(5)	5	80	None						
			8		Insufficient additives	2	Analyses and adjust additive weekly.	Visual sample check after plating(5)	5	80	None						
	rough plating	Visual Defect(6) Solderability Failure (8)	8		Particles, anode sludge, dirty	2	Replace filter elements at most 2weeks Filter plating solution every 3months	Visual sample check after plating(5)	5	80	None						

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			8		Excessive current	2	Shiftly check current per positrol log	Visual sample check after plating(5)	5	80	None						
			8		Low metal content of solution	2	Analysed the metal content of solution shiftly	Visual sample check after plating(5)	5	80	None						
			8		Insufficient additive	1	Analyses and adjust additives weekly	Visual sample check after plating(5)	5	40	None						
			8		Improper acid content of plating solution	2	Analyses and adjust content of the acid shiftly	Visual sample check after plating(5)	5	80	None						
			8		insufficient pretreatment	2	Check and analyses the pretreatment solution per positrol log shiftly	Visual sample check after plating(5)	5	80	None						
			8		Higher tin concentration in Pb-free electrolyte.	1	Tighten the maintenance limit of tin concentration for Pb-free electrolyte.	Chemical analysis shiftly(4).	4	32	None						
	pitting	Visual Defect(6) Solderability Failure (8)	8		Organic contamination	2	Analyses carbon monthly and conduct active carbon treatment;	Visual sample check after plating(5)	5	80	None						
			8		Insufficient pretreatment	2	Check and analyses the pretreatment solution per positrol log shiftly	Visual sample check after plating(5)	5	80	None						

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	missing plating	Solderability failure(8)	8		Insufficient Solution flowrate/ additive	1	Replace filter elements two weeks at most/Weekly Analyses additives weekly	Visual sample check after plating(5)	5	40	None						
			8		Foreign matter may resist the Tin deposit on lead frame	2	Clean water knife in plating solution cell weekly	Visual sample check after plating(5)	5	80	None						
	peeling	Solderability failure(8)	8		Insufficient pretreatment	2	Check and adjust the pretreatment solution per positrol log shiftly	Visual sample check after palting(5)	5	80	None						
	improper alloy composition	Solderability failure(8)	8	*	Improper bath metal composition	2	shiftly bath analysis	SPC control(4) Solderability sampling check(5)	4	64	None						
			8	*	Temperature is too high	1	Heaters & temperature system check monthly by PM; shiftly check bath temperature per positrol log	SPC control(4) Solderability sampling check(5) Machine Auto alarm(2)	2	16	None						
			8	*	Improper current density	2	shiftly check current per positrol log	SPC control(4) Solderability sampling check(5)	4	64	None						
	improper thickness	Solderability failure(8)	8	*	Improper current density	3	shiftly check per positrol log	SPC control(4) Solderability sampling check(5) Auto alarm system to detect current range(2)	2	48	None						
			8	*	Insufficient anode balls	2	shiftly check per set-up check list	SPC control(4) Solderability sampling check(5)	4	64	None						

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			8	*	Improper belt speed	1	shiftly check per positrol log	SPC control(4) Solderability sampling check(5)	4	32	None						
			8	*	Poor electrical connection	2	Shiftly check electrical connection per set-up check list	SPC control(4) Solderability sampling check(5)Auto alarm system to detect poor electrical connection issue(2)	2	32	None						
	Whiskers (Only for lead-free)	Electrical failure (8)	8		Insufficient descale	2	Check and analyses the descale solution per positrol log shiftly;Post Plating Bake	Sampling check(5) Chemical analysis shiftly(4).	4	64	None						
			8		high carbon or organic content	1	Check and analyses the descale solution per positrol log shiftly; Post Plating Bake	Sampling check(5);Chemical analysis shiftly(4).	4	32	None						
			8		High metal impurity content(Iron, lead copper, nickel)	2	Purify the plating solution every 3 months; Monitor the content of metal impurity	Sampling check(5);Analyse the metal impurity in bath monthly(4)	4	64	None						
			8		Incorrect current density	2	Check rectifier current shiftly.	Sampling check(5);Check current shiftly(4)	4	64	None						
			8		Improper temperature in plating	1	Check temperature shiftly	Machine Auto alarm(2)	2	16	None						
			8		Insufficient deposite thickness	2	Check belt speed and current density shiftly	SPC control(4)	4	64	None						

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10. plating gate (not applicable for PPF L/F)	overcure	electrical failure(8)	8		wrong temperature setup	1	temperature autoalarm system follow TCM table Check oven temp.controller 9 points monitor 1x /shift	check oven temp.controller 9 points(4) temperature autoalarm system(2)	2	16	None						
	undercure	electrical failure(8)	8		wrong temperature setup	1	temperature autoalarm system follow TCM table Check oven temp.controller 9 points monitor 1x /shift	check oven temp.controller 9 points(4) temperature autoalarm system(2)	2	16	None						
11. Trim&form	chip/crack/microgap	Reject by visual inspection or vision system(4) reliability fail(8)	8		Dieset broken	2	PM replace worn-out part regularly	Visual sample check after Trim&Form(5)	5	80	None						
			8		foreign matter reside on bottom supporting block	2	Clean tooling per lot	Visual sample check after Trim&Form(5)	5	80	None						
			8		unit remain/drop in dieset	2	Detect by sensor at dieset	sensor check automatically (2)	2	32	None						
			8		L/F feed abnormally	3	Detect by sensor	sensor check automatically (2)	2	48	None						
	foreign matter	Reject by visual inspection or vision system(4)	4		Mold flash on die/punch	2	Clean the TF tool per lot. Clean vacuum system shiftly	100% final visual inspection (3)	3	24	None						

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POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

Item: SOIC16/28/32/54ld
Control Number/Issue: 83MCT00002A/BY
Type: ___ Design _x_ Process
Company,Group,Site/Business Unit: Freescale,TJN-FM
Prepared By: Amanda Wang
FMEA Date: 05-Oct-94 (Orig.)
Core Team: Amanda Wang,H.J. Liu,Ivory Guo,JUN YING ZHENG,XIAOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN
14-Nov-13 (Rev.)

Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	SEV	Class	Potential Cause(s)/ Mechanism(s) of Failue	OCC	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	DET	RPN	Recommended Action(s)	Responsibility & Target Completion Date	Action Results: Actions Taken & Effective Date	SEV	OCC	DET	RPN
			4		scratch on lead/package body	3	Clean the TF tool per lot. Clean vacuum system shiftly	100% final visual inspection (3)	3	36	None						
	bent lead	Reject by visual inspection or vision system(4) Electrical failure(8)	8		Lead Frame jammed at unloader station	2	PM check singulation tool shiftly	100% final visual inspection (3)	3	48	None						
			8		forming tooling parts broken	1	PM check tool shiftly before production. operator clean and check forming bending part per lot before production.	100% final visual inspection (3)	3	24	None						
	metal bridge	Reject by visual inspection or vision system(4) electrical failure(8)	8		Die set broken	2	Check/replace piece part of T/F tooling on PM schedulely	Visual sample check after Trim&Form(5). 100% final visual inspection (3)	3	48	None						
	Excessive coplanarity	Customer application failure (8)	8		Die set broken.	2	PM check shiftly	Visual sample check after Trim&Form(5);SPC monitor(4)	4	64	None						
			8		L/F damaged by former step	1		100% strip check (3) Visual sample check after TrimForm(5)SPC monitor(4)	3	24	None						
			8		L/F jamed on track	1		Sensor pin auto check (2). Visual sample check after Trim&Form(5)SPC monitor(4)	2	16	None						

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Core Team: Amanda Wang,H.J. Liu,Ivory Guo,JUN YING ZHENG,XIAOHUI KANG,SHUAN YAO,Cyndi Hu,Grayson Chen,LANPING BAI,JIN

Control Number/Issue: 83MCT00002A/BY
Company,Group,Site/Business Unit: Freescale,TJN-FM
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14-Nov-13 (Rev.)

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	physical dimension (stand off, tip to tip distance, lead length/ angle)	Customer application failure(8)	8		Punch guide was broken or worn out	1	Check punch guide shiftly. Replace worn-out punch guide regularly	Visual sample check after Trim&Form(5)	5	40	None						
			8		Cutting punch was broken or worn out	1	Check cutting punch shiftly. Replace worn-out cutting punch regularly	Visual sample check after Trim&Form(5)	5	40	None						
			8		Cutting plate was broken or worn out	1	Check cutting plate shiftly Replace worn-out cutting plate regularly	Visual sample check after Trim&Form(5)	5	40	None						
	Uncut Dambar	Reject by visual inspection or vision system (4) Electrical failure (8)	8		Dambar punch/insert chipped	2	PM check the punch and dambar insert shiftly	Auto alarm for dambar check(2) 100% final visual inspection (3)	2	32	None						
	slug pull	Reject by visual inspection or vision system (4) electrial failure (8)	8		vacuum cleaning system breaks down/ do not function effectively	2	PM check and clean vacuum system monthly	Automatically check by machine (2) 100% final visual inspection (3)	2	32	None						
	L/F damaged	Reject by visual inspection or vision system(4)	4		L/F was loaded in wrong orientation	1		auto alarm for sensor check(2)	2	8	None						
	dambar burr	Reject by visual inspection or vision system(4) electrical failure (8)	8		Dambar punch was broken(chipping) or worn out	3	Check dambar punch shiftly. Replace worn-out dambar punch regularly	Visual sample check after Trim&Form(5)100% final visual inspection (3) Auto dambar check function (2)	2	48	None						

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			8		Dambar insert was broken and worn out	1	Check dambar insert shiftly Replace worn-out dambar insert regularly	Visual sample check after Trim&Form(5)100% final visual inspection (3) Auto dambar check function (2)	2	16	None						
			8		Higher tin concentration in Pb-free electrolyte.	1		Visual sample check after Trim&Form(5)100% final visual inspection (3) Auto dambar check function (2)	2	16	None						
			8		Tin patch sticking on the punch	3	Check dambar punch shiftly. Replace worn-out dambar punch regularly	Visual sample check after Trim&Form(5)100% final visual inspection (3) Auto dambar check function (2)	2	48	None						
	Lead damaged	Reject by visual inspection or vision system(4) electrical failure (8) Customer application failure(7)	8		Runner slug remain in dieset due to slug bin full	2	Sensor checking	Auto detect scrap/slug bin (2) 100% final visual inspection (3)	2	32	None						
			8		foreign matter dropping onto dieset	2	operator clean tooling per lot 100% strip inspection	100% final visual inspection (3)	3	48	None						
	over cut/ incomplete cut	Reject by visual inspection or vision system(4) electrical failure (8)	8		Dambar punch Dambar insert chipped	2	PM check shiftly	Visual sample check after Trim&Form(5)100% final visual inspection (3)	3	48	None						

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Control Number/Issue: 83MCT00002A/BY
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14-Nov-13 (Rev.)

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			8		L/F inaccurate location	2	100% strip inspection to mark out deformation L/F before T/F. Safety pin checked shiftly.	Visual sample check after Trim&Form(5) 100% final visual inspection (3) Safety pin alarm automatically (2)	2	32	None						
			8		foreign matter reside on bottom supporting block	2	Clean tooling per lot	Visual sample check after Trim&Form(5)	5	80	None						
	copper exposure	solderability failure (8)	8		forming parts broken	1	PM check shiftly	Visual sample check after Trim&Form(5) 100% final visual inspection (3)	3	24	None						
					non-conductive foreign matter sticking on lead	3	Sampling strip inspection to mark out contaminaiton L/F before T/F.	Visual sample check after Trim&Form(5)	5	120	Study the feasibility of vision system setup to improve the detection capability for exposed Cu on lead issue. Sev(8) Occ(3) Det(2)	Wei-Zhen Jin R04247 05/13/2014					
	Patchback	Reject by visual inspection or vision system(4) Electrical failure (8)	8		Excessive tin built-up on forming tool	2	Use DLC forming parts and Swing cam design. ,brush the T/F tool every lot, Clean T/F Tool 1x/shift	Visual sample check after Trim&Form(5) 100% final visual inspection (3)	3	48	None						
	scratch on lead/package body	Reject by visual inspection(4)	4		Lead Frame jammed at input station	3	100% incoming inspection before TF	100% finial inspection (3)	3	36	None						

POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

Item: Burn In/Final Test/Test Backend
Type: ___ Design _x_ Process
Prepared By: Liang Yang
Core Team: Peg Tang,ZJ-TEST2 Hu,Peter Zhang,Dong Gao,Liang Yang,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng D

Control Number/Issue: 83MCT00018A/AY
Company,Group,Site/Business Unit: Freescale,TJN-FM
FMEA Date: 27-Jun-01 (Orig.)
06-Sep-13 (Rev.)

Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	SEV	Class	Potential Cause(s)/ Mechanism(s) of Failue	OCC	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	DET	RPN	Recommended Action(s)	Responsibility & Target Completion Date	Action Results: Actions Taken & Effective Date	Action Results: SEV	Action Results: OCC	Action Results: DET	Action Results: RPN
Burn in	ESD/EOS	-Electrical failure(8) -Reliability failure (8)	8		-Wrist strap and/or shoes function fail	1	-Turnstile wrist strap check during every entry to test floor	-Q-check yield control (3)	3	24	None						
			8		-Workstation and equipment are not properly grounded	1	-Monthly check/half year PM	-Q-check yield control (3)	3	24	None						
	Product mixed/escaped	-Electrical failure(8) -Reliability failure (8)	8		-Operate more than one lot at same time	2	-Handle only one lot in one table / Loader & Unloader -Perform marking inspection before lot start -Material status identification before/after process -100% check before next chamber start	-Quantity count (6) -Sampling check the marking (8) -100% auto VM inspection in packaging process. (4)	4	64	None						
			8		-Wrong program used	1	-Only the latest Rev. program available	-Buddy check (7) -Q check detection (3)	3	24	None						

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Core Team: Peg Tang,ZJ-TEST2 Hu,Peter Zhang,Dong Gao,Liang Yang,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng D
06-Sep-13 (Rev.)

Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	SEV	Class	Potential Cause(s)/ Mechanism(s) of Failue	OCC	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	DET	RPN	Recommended Action(s)	Responsibility & Target Completion Date	Action Results: Actions Taken & Effective Date	SEV	OCC	DET	RPN
	Miss Burnin	-Customer application failure(8) -Reliability failure (8)	8		-Operator miss lot in Burnin peocess	1	-Follow TSO and SFC instruction -Auto start BI function to prevent miss BI	-Buddy check (7) - 100% auto electrical test in packaging process (4)	4	32	None						
			8		-Socket open/short	2	-Check and change socket during PM -Check before loading units	--Q check & BIN2 check detection (3) -Sampling check in loading process (8)	3	48	None						
	Bend lead & coplanarity	-Visual mechanical failure (6) -Customer application failure(8)	8		-Nonstandard manual handling mode	2	Set up standard manual handling method	-100% VM inspection (6) -100% auto VM inspection in packaging process (4)	4	64	None						
			8		-Bad socket	2	-Check and change socket during PM -Check before loading units	-100% VM inspection (6) -100% auto VM inspection in packaging process (4)	4	64	None						
			8		-Loader & unloader machine misalignment	2	-Half year PM -Shiftly check handler by setup checklist	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						

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POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

Item: Burn In/Final Test/Test Backend
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Prepared By: Liang Yang
FMEA Date: 27-Jun-01 (Orig.)
Core Team: Peg Tang,ZJ-TEST2 Hu,Peter Zhang,Dong Gao,Liang Yang,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng D
06-Sep-13 (Rev.)

Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	SEV	Class	Potential Cause(s)/ Mechanism(s) of Failue	OCC	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	DET	RPN	Recommended Action(s)	Responsibility & Target Completion Date	Action Results: Actions Taken & Effective Date	SEV	OCC	DET	RPN
	Foreign matter on lead	- Electrical failure (8)	8		-Particle from B/I board	1	-Periodical clean B/I boards -Check B/I boards by lot	-100% VM inspection(6)	6	48	None						
	Ball damage	-Visual mechanical failure (6) -Customer application failure(8)	8		-Nonstandard manual handling mode	2	Standard manual handling method	-100% auto VM inspection in packaging process (4) -In-process sampling check (8)	4	64	None						
Material receiving (Receive & store material)	Product mixed	-Yield Loss (7) -Customer Line pull (8)	8		Multiple lot processed simultaneously	2	1. Periodical Training to MTL Operators 2. Mobile SFC terminal to eliminate bulk processing of shop order	- Manual verify box label LOT#, device #, box quantity against packing list & SFC - Accept on zero discrepancy (6) - 100% Marking check by Vision system in Packaging process(4)	4	64	Auto Print Box Qty and # on Barcode label Sev=8, Occ=1, Det=4, RPN=32	Liang Yang R57253/06-30-2014					

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Core Team: Peg Tang,ZJ-TEST2 Hu,Peter Zhang,Dong Gao,Liang Yang,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng D 06-Sep-13 (Rev.)

Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	SEV	Class	Potential Cause(s)/ Mechanism(s) of Failue	OCC	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	DET	RPN	Recommended Action(s)	Responsibility & Target Completion Date	Action Results: Actions Taken & Effective Date	SEV	OCC	DET	RPN
	Count variance (CV)	Qty shortage	3		Miss Counting by Assembly or BI Site	2	Mobile SFC terminal to eliminate bulk processing of shop order	- Manual verify box label LOT#, device #, box quantity against packing list & SFC - Accept on zero discrepancy (6) - 100% Count Qty by Test operator (5)	5	30	None						
INCOMING CHECK (Visual Mechanical only applies to Assembly & BI rawstock)	Count variance (CV)	Qty shortage	3		Miss Counting by Assembly or BI Site	2	NA	- Manual verify box label LOT#, device #, box quantity against packing list & SFC - Accept on zero discrepancy (6) - 100% Count Qty by Test operator (5)	5	30	None						
	Raw stock issue	Marking mismatch with System/shop order	3		Device mixed at Assembly or BI process	3	NA	- Sampling Marking inspection during incoming check (5)	5	45	None						

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	V/M Defect	-Visual mechanical failure (6) -Customer application failure(8)	8		V/M defect introduced by Assembly or BI process	2	NA	- Sampling V/M inspection during incoming check (5) - 100% Marking check by Vision system in Packaging process(4)	4	64	None						
ELECTRICAL TEST as per test shop order 1. Machine preparation 2. Start lot 3. Electrical parameters tests 4. End lot (Hot/Cold/Room)	Lot Combination by mistake	Yield Loss (7) Customer line pull (8)	8		Mixed with Other device	1	Config lot combine rule in SFC system	- ATE Test (3)	3	24	None						

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			8		mixed with other trace code	1	Config lot combine rule in SFC system	-lot informaiton and marking check post combination (6) -100% Count Qty by Test operator before test(5) -100% auto VM inspection in Packaging process. (4)	4	32	None						
	Expired BI window	Infant mortality, fail electrical test during board assembly (8)	8		Lot staged for too long after BI	1	Daily WIP review by mfg and planner. Test priority given to material with BI window. Expected BI expiry date can be viewed in genesis through lot enquiry screen	- Auto hold lot with expired BI window (2)	2	16	None						
	Wrong machine setup	Fail 1st article check (3) Unable to perform test (2)	3		Use wrong tester	1	Listed Tester information on TSO Test program is configed by tester	- Operator check tester vs. TSO during setup (5) - Program auto verify during download (1)	1	3	None						
			3		Use wrong handler	2	Listed handler information on TSO	- Operator check Handler vs. TSO during setup (5)	5	30	None						

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			3		Wrong loadboard identification	3	Engineer create loadboard ID and buyoff loadboard before releasing to production (applies for NPI as well)	- Manual visual verification on loadboad ID during loadboard issuing/receiving/PM (5)	5	45	None						
			3		Wrong shoporder loadboard ID setup	3	NA	- QA Document Audit (6)	6	54	Work with IT team to convert LB information to SFC system. Sev=3, Occ=2, Det=6, RPN=36	Wei Chen R65950/06-30-2014					
			3		Tray loaded in wrong orientation	1	Poka Yoke mechanism on Handler	- Auto alarm for wrong orientation (2) - ATE Test (3)	2	6	None						
	Wrong test temperature	Yield Loss (7) Customer line pull (8)	8		Error during manual temperature selection	2	SC2 auto temperature loading (except MST)	- QC in line gate (4) - QA Document Audit (6) - QA shiftly audit (8)	4	64	None						

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			8		Wrong O/I configuration setup	3	Dedicate engineering personel to perform O/I configuration	- QA Document Audit (6) - Auto-trigger on missing configuration to respective PE through scheduled auto database check (3)	3	72	Download Gen2Spec parameters to auto-generate SC configuration file using SC Config file generation tool Sev=8, Occ=2, Det=3, RPN=48	Liang Yang R57253/05-30-2014					
	Use wrong program	Customer Line pull (8) Yield Loss (7)	8		TSO not updated timely to reflect program revision	1	Only effective version of Test program is available in Server	-Auto verify program information before test start (2) - First 200 units yield check(5) - QA Document Audit (6)	2	16	None						
			8		Program selection error	2	1. Listed test program information on TSO; 2. Listed handler information on TSO; 3. Auto-program loading except for A5 & MST	- QA Document Audit (6) - Buddy check before test (7) - QC in line gate (4) - QA shiftly audit (8)	4	64	None						

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			8		SPV Program selection error	1	1. Enforce expiry duration on program reside in SPV 2. Auto SPV program loading on SC2	- QC in line gate (4) - QA Document Audit (6) - QA shiftly audit (8)	4	32	None						
			8		Wrong O/I configuration setup	2	Dedicate engineering personel to perform O/I configuration Download Gen2Spec parameters to auto-generate SC configuration file	- QA Document Audit (6) - Auto-trigger on missing configuration to respective PE through scheduled auto database check (3)	3	48	None						
	ESD/EOS	Customer Line pull (8) Yield Loss (7)	8		-Wrist strap and/or shoes function fail	1	-Turnstile wrist strap check during every entry to test floor	-Yield limit and SBL check (3) -JVT test at last insertion (3)	3	24	None						
			8		No grounding (work station / rack)	1	-Quarterly check	-Yield limit and SBL check (3) -JVT test at last insertion (3)	3	24	None						

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POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

Item: Burn In/Final Test/Test Backend
Control Number/Issue: 83MCT00018A/AY
Type: ___ Design _x_ Process
Company,Group,Site/Business Unit: Freescale,TJN-FM
Prepared By: Liang Yang
FMEA Date: 27-Jun-01 (Orig.)
Core Team: Peg Tang,ZJ-TEST2 Hu,Peter Zhang,Dong Gao,Liang Yang,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng D 06-Sep-13 (Rev.)

Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	SEV	Class	Potential Cause(s)/ Mechanism(s) of Failue	OCC	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	DET	RPN	Recommended Action(s)	Responsibility & Target Completion Date	Action Results: Actions Taken & Effective Date	SEV	OCC	DET	RPN
			8		Inaccurate placement for ionizer	1	Use bracket to hold ionizer at a specific correct place	- QC in line gate (4) - High electrical fall out at next insertion for leakage or idd failure (3) - JVT test at last insertion (3)	3	24	None						
			8		Testers / Handlers environment	2	Check grounding and ionizer properly installed during half year PM	- JVT test at last insertion (3)	3	48	None						
			8		Spike voltage on the DC measurement	1	Spike check during NPI release	-Yield limit and SBL check (3) -JVT or equivalent test methodology (3)	3	24	None						
			8		Loadboard traces shorted	2	continuity check during Loadboard buyoff and Loadboard PM	-Yield limit and SBL check (3) -JVT or equivalent test methodology (3)	3	48	None						

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	Product mixed/escaped	Customer Line pull (8) Yield Loss (7)	8		-Mix of rawstock and tested units / Mix of rawstock and reject from different lot	4	-Handle only one lot in one station -Perform marking inspection before lot start -Material status identification before/after process -Treat all uncomfirming units and PE used units as rejects - Proper labeling using lot identification barcode - Pending rack, Input & output rack with proper labeling - Label all work place for proper material segregation -All tested good partial/full tube are to be placed inside or next to the tested good box -Identified color tray/tube to collect rejects -Separate pending rack away from input rack by Using different appearance and	-Quantity count (6) -Sampling check the marking (8) -QC in line gating (4) -100% auto VM inspection in packaging process. (4) -Test program auto detect part difference (3) -Optimize ECID system to auto hold material if the ECID doesn't match between different insertion (2)	2	64	None						

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			8		Miss test insertion or in line gate	1	Test flow configed and auto controlled by Genesis system	- Genesis auto verify test flow during transaction (1)	1	8	None						
			8		-Wrong binning setting of handler	1	-Disable the bin setting button at the operation interface to prevent misclick. -Use SC2 auto control bin setting	-QA document audit (6) -QC in line gate (4)	4	32	None						
			8		-Leftover unit in equipment	2	-Clear machine before and after test -Lot count before start testing -Centralized reject scrapping at QA area after QA validation	-Marking inspection for first 200 units (5) -Quantity count (6) -Using SC2 auto count lot quantity except MST, A5 (3)	3	48	None						
			8		-speed sort device mixed	1	-Using different color tray/tube to replace different color clip for material identification	-QA document audit (6) -QC in line gate (4)	4	32	None						

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			8		-Wrong customer code key in for factory programming product	1	-Add password verification to guaratee correct customer code input -Add customer code check on gate test	-QA document audit (6) -QC in line gate (4) -100% EEV test (3)	3	24	None						
			8		-Engineer/ Techincian mishandling during on line debug	1	-Handle only one lot in one station -follow on line debug instruction -Material status identification before/after process -Treat PE used units as rejects -System auto clear testsite when quit engineer testing mode and sort all verification units into reject tray	-Quantity count (6) -Sampling check the marking (8) -QC in line gate (4)	4	32	None						

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			8		Leftover unit on recycle tray	2	-Check recycle tray before putting them into machine -Standard operation of recycle tray checking -partial tray alert	-100% auto VM inspection in packaging process (4) -Quantity count (6) -Sampling check the marking (8) -QC in line gate (4)	4	64	None						
			8		Battery Backup Unit (BBU) memory full causing Castle handler fail to pickup rawstock unit and indexed to main tray buffer as an empty tray	1	Castle handler firmware upgraded to auto clear BBU once 'handler empty' status is prompt.	1. QC in line gate. (4) 2. QA shiftly audit (8) 3. Quantity count (6)	4	32	None						
			8		Bin1 units from previous insertion are not cleared from output bin1 stacker / rack	5	NA	- QC in line gate. (4) 2. QA shiftly audit (8) 3. ECID detection method for applicable products (2) 4. Quantity count (6)	2	80	Station Controller auto stop test program loading if any units detected at output area SEV=8, OCC=2, DET=2, RPN=32	Peng Lin R65908/06-28-2014					

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			8		Reject mixed into good during machine downtime eg. During maintenance	2	1. Rawstock and tested material segregation by operator during machine down 2. Technician to use only rawstock material for setup during maintenance. All units are to be placed back into rawstock material 3. Scrap jammed units 4. Centralized reject scrapping in QA area after QA validation	-QC in line gate. (4) - QA shiftly audit (8) - ECID detection method for applicable products (3)	3	48	None						
	Non qualified engineering lot shipped to customer	Customer application failure (8)	8		Use production lot class for engineerig purpose causing lot shipped as production lot to customer.	2	Any engineering lot need to use engineering lot class. Log in MDR for engineering lot class to ship as normal production lot class.	All engineering lot class require MDR prior shipment. (2)	2	32	None						

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	Low yield or SBL over limit (DC, functional, parametric, open/short, electrical)	- Yield loss (7)	7		Tester out of calibration	1	- Tester calibration during regular PM	- Yield limit control in Genesis (3) - SBL limit control (3) -Auto calibration every program loading (2) -Diagnostic during PM (5)	2	14	None						
			7		-Wrong binning setting of handler	1	-Disable the bin setting button at the operation interface to prevent misclick. -Use SC2 auto control bin setting	-QA document audit (6) -QC in line gate (4)	4	28	None						
			7		- Handler setup problem	1	- Handler regular PM - Set up check	- Yield limit control in Genesis (3) - SBL limit control (3) - First 200 units yield check (4)	3	21	None						
			7		- Load Board problem	3	- Load board regular PM	- Yield limit control in Genesis (3) - SBL limit control (3) - First 200 units yield check (4)	3	63	None						

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			7		- Tester board problem	1	- Tester regular PM	- Yield limit control in Genesis (3) - SBL limit control (3) - First 200 units yield check (4)	3	21	None						
			7		- Poor contact at DUT socket (device under test)	3	- Contact interface regular replacement	- Yield limit control in Genesis (3) - SBL limit control (3) - First 200 units yield check (4)	3	63	None						
	Bend lead & coplanarity	-Visual mechanical failure (6) -Customer application failure(8)	8		-Device misplacement by hanlder	2	-Half year PM -Shiftly check handler by setup checklist	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						
			8		Unit overpress during test	1	Input quad hardstop to prevent overpress	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	32	None						

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			8		Bad socket/pogo pin	2	-Hard stopper configuration - Load board regular PM - Contact interface regular replacement	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						
			8		ATU causing drop units	2	1. Use CASM/CAIM to cycle ATU and observe for mechanical binding issue during handler PM 2. Designed tray catcher with loaded spring 3. Add mounting plate to tighten door sensor	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						
			8		Unit misplaced in tray at output handler	2	Handler buyoff after PM and conversion sort xyz alignment jig	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						

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			8		- Operator handles material manually.	2	- Certify operators' operation skill and yearly exam to check - Treat manual operated material as VM reject and scrap.	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						
			8		-Frost inside test chamber	2	-Warm up handler periodically -Use air pressure to prevent frozen during cold temperature test -System auto warm up cold temperature handler - SC2 Auto-defrost function	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						
			8		-Hit by damaged track corner	2	-Add chamfer at soak booster track and singulator track -Perform Track inspection when replacement during PM	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						

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	Ball damage	-Visual mechanical failure (6) -Customer application failure(8)	8		Bad socket/pogo pin	2	-Hard stopper configuration - Load board regular PM - Contact interface regular replacement	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						
			8		Unit jam at core section	2	1. Periodic handler PM to minimize jamming 2. Scrap impacted unit that jammed at core section	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						
			8		-Device misplacement by hanlder	2	-Half year PM -Shiftly check handler by setup checklist	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						
			8		Unit overpress during test	1	Input quad hardstop to prevent overpress	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	32	None						

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			8		Unit misplaced in tray at output handler	2	Handler buyoff after PM and conversion sort xyz alignment jig	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						
			8		FM on substrate	1	1. Use hanging nest with mold guided & chamfered design. 2. Auto-defrost for J750 3. Periodical handler cleaning 4. Boat clean during conversion	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	32	None						
			8		- Operator handles material manually.	2	- Certify operators' operation skill and yearly exam to check - Treat manual operated material as VM reject and scrap.	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						

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	Crack/chip	- Reliability failure (8) -Electrical failure (8) -Visual mechanical failure (6)	8		-Wrong handler adjustment	1	-Hard stopper configuration	-In-process sampling check (8) -Hard stopper auto alarm (2)	2	16	None						
			8		-Incorrect bushing on L/B	1	-Hard stopper configuration	-In-process sampling check (8) -Hard stopper auto alarm (2)	2	16	None						
			8		- Operator handles material manually in tray.	2	- Certify operators' operation skill and yearly exam to check - Treat manual operated material as VM reject and scrap. - Put a empty tray on the top before move out material from machine	- Tray gap check (6) -100% auto VM inspection in packaging process (4)	4	64	None						

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	Sliver & patchback (non pogo socket only)	Short circuit or leakage (8)	8		High plating material build up at test socket	2	Socket cleaning and replace regularly	- Yield limit control in Genesis (3) - SBL limit control (3) - First 200 units yield check (4) -V/M gate sampling check (8)	3	48	None						
	Pogo Burr	Visual Mechanical Failure (6)	6		Mechanical Contact offset on device lead due wear and tear of test socket pogo holes	2	Check for socket bushing conditions during PM. Replace socket if pogo holes found wear and tear	- V/M gate sampling check (8) - First 200 units V/M check (5)	5	60	None						
	Damaged lead foot plating surface	Solderability Failure (8)	8		test finger deformation	1	-Board regular PM - Check Pogo pin/socket befor&after each use	- V/M gate sampling check (8) - First 200 units V/M check (5)	5	40	None						
	Foreign Matter On Lead	Solderability Failure (8)	8		Dirt accumulated in handler boat	1	1. handler cleaning during shift start 2. boat clean during conversion	- V/M gate sampling check (8) - First 200 units V/M check (5)	5	40	None						

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			8		Unit drop out of tray	2	1. Strap Bin1 tray with cover tray right after testing 2. Unstrap rawstock bundle just before loading to ATU 3. Use CASM/CAIM to cycle ATU and observe for mechanical binding issue during handler PM (ATU issue) 4. Designed tray catcher with loaded spring (ATU issue) 5. Standardize tray latch spring to 0.32mm diameter (ATU issue) 6. Add mounting plate to tighten door sensor (ATU issue) 7. Treat dropped unit as reject	- V/M gate sampling check (8) - First 200 units V/M check (5) -100% auto VM inspection in packaging process (4)	4	64	None						

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Core Team: Peg Tang,ZJ-TEST2 Hu,Peter Zhang,Dong Gao,Liang Yang,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng D

Control Number/Issue: 83MCT00018A/AY
Company,Group,Site/Business Unit: Freescale,TJN-FM
FMEA Date: 27-Jun-01 (Orig.)
06-Sep-13 (Rev.)

Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	SEV	Class	Potential Cause(s)/ Mechanism(s) of Failue	OCC	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	DET	RPN	Recommended Action(s)	Responsibility & Target Completion Date	Action Results: Actions Taken & Effective Date	SEV	OCC	DET	RPN
			8		Usage of fibrous material at production floor	1	Banned cotton bud, fibrous glove and cloth from production floor	- QA shiftly audit (8) - V/M gate sampling check (8) - First 200 units V/M check (5)	5	40	None						
			8		FM stick on pogo pin	3	Socket cleaning and replace if necessary	- Yield limit control in Genesis (3) - SBL limit control (3)	2	48	None						
			8		FM from incoming/environment dropped to staging trays causing FM to attach to units when the trays are used.	1	Top tray cover for trays during staging period to prevent FM	-V/M gate sampling check (8) -100% auto VM inspection in packaging process (4)	4	32	None						
	Foreign Matter On Package Body	Solderability Failure (8)	8		FM from incoming/environment dropped to staging trays causing FM to attach to units when the trays are used.	1	Top tray cover for trays during staging period to prevent FM	Detection at TBE using 3x inspection (6)	6	48	None						

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POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

Item: Burn In/Final Test/Test Backend
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Core Team: Peg Tang,ZJ-TEST2 Hu,Peter Zhang,Dong Gao,Liang Yang,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng D

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Laser mark	Missing mark	-customer application failure - 8	8		-Laser generator fail	1	-Machine auto check laser power before marking.	-First piece part verification after marking(4) -Machine auto alarm when power out of control(2) -QA Gate(8)	2	16	None						
	Illegible mark	Customer application failure - 8	8		Inappropriate laser power	2	Machine auto check laser power before marking.	-First piece part verification after marking(4) - Machine marking 100% auto scan in subsequent process (4) -QA visual inspection 200 units/lot(8) -Machine auto alarm when laser power abnormal.(2)	2	32	None						

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			8		Laser generator worn out	1	NA	-First piece part verification after marking(4) - Machine marking 100% auto scan in subsequent process (4) -QA visual inspection 200 units/lot(8) -Machine auto alarm when laser power abnormal.(2)	2	16	None						
	Marking misalignment	Customer application failure - 8	8		Location pin damaged	1	NA	-First piece part verification after marking(4) - Machine marking 100% auto scan in subsequent process (4) -QA visual inspection 200 units/lot(8)	4	32	None						

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	Wrong marking	Customer application failure - 8	8		Marking information input error during manual operation	1	-Auto load marking information	-First piece part verification after marking(4) - Machine marking 100% auto scan in subsequent process (4) -QA visual inspection 200 units/lot(8)	4	32	None						
40x Inspection	Burr&sliver on shoulder/riser/ lead	-Visual mechanical failure (6) -Customer application failure(8)	8		Shoulder damaged by BI (failure identified by KLM)	2	NA	-10x V/M gate (8) - 100% auto vision inspection on device (2)	2	32	None						
	Bend lead & coplanarity	-Visual mechanical failure (6) -Customer application failure(8)	8		Unit out of pocket	2	1. Strap the tray whenever moving the material 2.Operator to check tray gap before and after strapping to ensure no unit jump out the pocket	-V/M gate (8) - 100% auto vision inspection on device (2)	2	32	None						

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			8		Mishandling the unit	2	1. Strap the tray whenever moving the material 2.Operator to check tray gap before and after strapping to ensure no unit jump out the pocket	-V/M gate (8) - 100% auto vision inspection on device (2)	2	32	None						
	Wrong orientation	-Customer application failure (8)	8		Unit replaced in misorientated form	2	Pin1 reverification after unit replacement	-V/M gate sampling check (8) -Vision system auto detect and alarm (2) -Auto-Pin 1 locate system by vision(1) -Pin1 bar setting for tray locate(1)	1	16	None						
	Mixed product	-Electrical failure (8) -Reliability failure (8)	8		Stray units at inspection table	2	Clear work station after completion of lot.	-V/M gate sampling check (8) -Count quantity per shop order (6) - Vision 100% inspection (2)	2	32	None						

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			8		Swap Shop order	2	Process 1 lot at a time	-System record the marking teach history in test summary, operator 100% check summary(4) -System auto check and judge if marking is correct or not after key in the actual marking (2) 100% vision inspection	2	32	None						
			8		Swap bundle	2	Process 1 lot at a time	1. Lot no verification on barcode label vs TSO (3) 2. 100% vision scanning (2) 3. QA VM Gate (8)	2	32	None						
10x Inspection	Burr&sliver on shoulder/riser/ lead	-Visual mechanical failure (6) -Customer application failure(8)	8		Shoulder damaged by BI (failure identified by KLM)	2	NA	-10x V/M gate (8) - 100% auto vision inspection on device (2)	2	32	None						

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	Bend lead & coplanarity	-Visual mechanical failure (6) -Customer application failure(8)	8		Unit out of pocket	2	1. Strap the tray whenever moving the material 2.Operator to check tray gap before and after strapping to ensure no unit jump out the pocket	-V/M gate (8) - 100% auto vision inspection on device (2)	2	32	None						
			8		Mishandling the unit	2	1. Strap the tray whenever moving the material 2.Operator to check tray gap before and after strapping to ensure no unit jump out the pocket	-V/M gate (8) - 100% auto vision inspection on device (2)	2	32	None						

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	Wrong orientation	-Customer application failure (8)	8		Unit replaced in misorientated form	2	Pin1 reverification after unit replacement	-V/M gate sampling check (8) -Vision system auto detect and alarm (2) -Auto-Pin 1 locate system by vision(1) -Pin1 bar setting for tray locate(1)	1	16	None						
	Mixed product	-Electrical failure (8) -Reliability failure (8)	8		Stray units at inspection table	2	Clear work station after completion of lot.	-V/M gate sampling check (8) -Count quantity per shop order (6) - Vision 100% inspection (2)	2	32	None						

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			8		Swap Shop order	2	Process 1 lot at a time	-System record the marking teach history in test summary, operator 100% check summary(4) -System auto check and judge if marking is correct or not after key in the actual marking (2) 100% vision inspection	2	32	None						
			8		Swap bundle	2	Process 1 lot at a time	1. Lot no verification on barcode label vs TSO (3) 2. 100% vision scanning (2) 3. QA VM Gate (8)	2	32	None						
Bake	Mixed product	-Electrical failure (8) -Reliability failure (8)	8		-Operator handles the wrong device without check marking	3	-Ensure only one lot in work table for tube package. - Verify lot number/ magazine number vs. shop order	-Count the quantity for tube package(6) -100% auto vision inspection in subsequence process (4)	4	96	Using bakeable tube to avoid mistake during tube to tube process SEV=8, OCC=1, DET=4, RPN=32	HONGZHI REN B06298/04-30-2014					

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	Miss bake	-Reliability failure (8)	8		-Operator forgets to do bake step and transfer the material to the next step.	2	-Follow TSO and SFC instruction	-Genesis system control (2) -Buddy check (7)	2	32	None						
			8		-Place pre-bake units into post-bake units	2	-Different requirement lot stock in different area	-Genesis system control (2)	2	32	None						
	Time/Temperature incompetent	-Customer application failure (8)	8		-Wrong time and temperature	1	-Fix timer and temperature controller to auto-monitor	-Auto check system alarm(2)	2	16	None						
Dry air storage	Moisture out of control	- Delamination issue (8) -Customer application failure (8)	8		- Dry air barometric pressure low	1	N/A	- Flow meter check per setup checklist (6) - HIC monitor / open the Dry air cabinet (6)	6	48	None						
	Miss Dry air storage	- Delamination issue (8) -Customer application failure (8)	8		-Operator forgets to put the lot into the Dry air cabinet	2	-Follow SFC instruction.	-Buddy check (7) -Genesis system control (2)	2	32	None						

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3x inspection	Bend lead & coplanarity	-Visual mechanical failure (6) -Customer application failure(8)	8		Unit out of pocket	2	1. Strap the tray whenever moving the material 2.Operator to check tray gap before and after strapping to ensure no unit jump out the pocket	-V/M gate (8) - 100% auto vision inspection on device (2)	2	32	None						
			8		Mishandling the unit	2	1. Strap the tray whenever moving the material 2.Operator to check tray gap before and after strapping to ensure no unit jump out the pocket	-V/M gate (8) - 100% auto vision inspection on device (2)	2	32	None						

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	Wrong orientation	-Customer application failure (8)	8		Unit replaced in misorientated form	2	Pin1 reverification after unit replacement	-V/M gate sampling check (8) -Vision system auto detect and alarm (2) -Auto-Pin 1 locate system by vision(1) -Pin1 bar setting for tray locate(1)	1	16	None						
	Mixed product	-Electrical failure (8) -Reliability failure (8)	8		Stray units at inspection table	2	Clear work station after completion of lot.	-V/M gate sampling check (8) -Count quantity per shop order (6) - Vision 100% inspection (2)	2	32	None						

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			8		Swap Shop order	2	Process 1 lot at a time	-System record the marking teach history in test summary, operator 100% check summary(4) -System auto check and judge if marking is correct or not after key in the actual marking (2) 100% vision inspection	2	32	None						
			8		Swap bundle	2	Process 1 lot at a time	1. Lot no verification on barcode label vs TSO (3) 2. 100% vision scanning (2) 3. QA VM Gate (8)	2	32	None						
Lead scan	Bend lead & coplanarity	-Visual mechanical failure (6) -Customer application failure(8)	8		-Bent tray	2	NA	-Operator 100% check tray (6) - 100% auto vision inspection on device (2)	2	32	None						

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			8		- Unit misplace in tray caused by handler precision	2	-Half yearly PM	-V/M gate (8) - 100% auto vision inspection on device (2)	2	32	None						
	2D matrix unreadable	-Visual mechanical failure (6)	6		- Bypass 2D matrix inspection function	2	-High level password control	-System real time monitor (2)	2	24	None						
			6		- Dongle is unworkable	2	NA	-Program auto alarm and stop handler when dongle is unworkable(2)	2	24	None						
	Unit wrong orientation in tray	-Customer application failure (8)	8		-Improper vision set	1	-Regular setup checklist check.	-V/M gate sampling check (8) -Vision system auto detect and alarm (2) -Auto-Pin 1 locate system by vision(1) -Pin1 bar setting for tray locate(1)	1	8	None						

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			8		-Wrong teach on material for pin1	1	-Auto-Pin 1 locate system by vision	-V/M gate first piece check (4) --Buddy check(7) -Auto-Pin 1 locate system by vision(1) -Pin1 bar setting for tray locate(1)	1	8	None						
	Mixed product	-Electrical failure(8) -Reliability failure (8)	8		-Operator does not clear the machine when finished lot	2	-Equipment clean after lot end	-V/M gate sampling check (8) -Count quantity per shop order (6) - Vision 100% inspection (2)	2	32	None						
			8		-Operator teach wrong marking	3	NA	-System record the marking teach history in test summary, operator 100% check summary(4) -System auto check and judge if marking is correct or not after key in the actual marking (2)	2	48	None						

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	Crack/chip	- Reliability failure (8) -Electrical failure (8) -Visual mechanical failure (6)	8		- Operator handles material manually in tray.	2	- Certify operators' operation skill and yearly exam to check - Treat manual operated material as VM reject and scrap.	- Tray gap check (6) - 100% auto vision inspection (2)	2	32	None						
Tape & Reel	Cover tape loosen / tighten	-Device fail out or cover tape split at customer (8)	8	*	-Peel back force is out of control	1	-Follow setup checklist to set up machine	- SPC system control (4) -QA audit peel back force test record (6) -QA sealing line check (8)	4	32	None						
	2D matrix unreadable	-Visual mechanical failure (6)	6		- Bypass 2D matrix inspection function	2	-High level password control	-System real time monitor (2)	2	24	None						
			6		- Dongle is unworkable	2	NA	-Program auto alarm and stop handler when dongle is unworkable(2)	2	24	None						

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Core Team: Peg Tang,ZJ-TEST2 Hu,Peter Zhang,Dong Gao,Liang Yang,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng D
06-Sep-13 (Rev.)

Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	SEV	Class	Potential Cause(s)/ Mechanism(s) of Failue	OCC	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	DET	RPN	Recommended Action(s)	Responsibility & Target Completion Date	Action Results: Actions Taken & Effective Date	SEV	OCC	DET	RPN
	Unit wrong orientation in tape reel	-Customer application failure (8)	8		-Wrong teach on material for pin1	1	-Auto-Pin 1 locate system by vision	-V/M gate first piece check (4) --Buddy check(7) -Auto-Pin 1 locate system by vision(1) -Pin1 bar setting for tray locate(1)	1	8	None						
			8		-Improper vision setting	1	-Regular setup checklist check.	-V/M gate sampling check (8) -Vision system auto detect and alarm (2) -Auto-Pin 1 locate system by vision(1) -Pin1 bar setting for tray locate(1)	1	8	None						
	Bend lead	-Visual mechanical failure (6) -Customer application failure(8)	8		-Machine pick up head is not in the perfect position along the X,Y,Z direction	2	- Cross beam installed on all tape reel equipment.	-V/M gate sampling check (8) -Handler cross sensor 100% check unit position and auto alarm(2) -Check per setup checklist (6)	2	32	None						

POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

Item: Burn In/Final Test/Test Backend
Control Number/Issue: 83MCT00018A/AY
Type: ___ Design _x_ Process
Company,Group,Site/Business Unit: Freescale,TJN-FM
Prepared By: Liang Yang
FMEA Date: 27-Jun-01 (Orig.)
Core Team: Peg Tang,ZJ-TEST2 Hu,Peter Zhang,Dong Gao,Liang Yang,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng D
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	Empty pocket	-Quantity shortage for customer (8)	8		-Pocket2 sensor does not work properly	2	NA	-Machine auto alarm (2) -Reel counter setup check (4) '-PM daliy check per setup check list (6)	2	32	None						
	Tape wrong revolution in reel	-Electrical failure (8)	8		-Operator forget to wind back orginal reel after reel to reel process	1	-Using black or blue reel for reel to reel. -Fix color reel to prevent mixed handling by operator	-QA 100% check tape revolution for every reel (6)	6	48	None						
			8		-Use white reel on reel to reel process	1	-Using black or blue reel for reel to reel. -Fix color reel to prevent wrong reel used.	-QA 100% check tape revolution for every reel (6)	6	48	None						
	Ball damage	-Visual mechanical failure (6) -Customer application failure(8)	8		-Machine pick up head is not in the perfect position along the X,Y,Z direction	2	- Cross beam installed on all tape reel equipment.	-Handler cross sensor 100% check unit position and auto alarm(2) -Check per setup checklist (6)	2	32	None						

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	Cover tape misalignment with carrier tape	-Customer application failure (8)	8		-Technician adjust the guider width or carrier tape location pins improperly.	2	NA	-Technician first piece check under 10X microscope after technician adjust the guider width or carrier tape location pins. (4)	4	64	None						
	Mixed product	-Electrical failure(8) -Reliability failure (8)	8		-Operator does not clear the machine when finished lot	2	-Equipment clean after lot end	-V/M gate sampling check (8) -Count quantity per shop order (6) - Vision 100% inspection (2)	2	32	None						
			8		-Operator teach wrong marking	3	NA	-System record the marking teach history in test summary, operator 100% check summary(4) -System auto check and judge if marking is correct or not after key in the actual marking (2)	2	48	None						

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TTT	Lead defect in tube	-Visual mechanical failure (6) -Customer application failure(8)	8		-Tube and tracking alignment	1	-Re-design the tracking to optimize alignment	-V/M Gate sampling check (8) --Frist piece check (4)	4	32	None						
	Mixed product	-Electrical failure(8) -Reliability failure (8)	8		-Operator does not clear the machine when finished lot	2	-Equipment clean after lot end	-V/M gate sampling check (8) -Count quantity per shop order (6) - Vision 100% inspection (2)	2	32	None						
			8		-Operator teach wrong marking	3	NA	-System record the marking teach history in test summary, operator 100% check summary(4) -System auto check and judge if marking is correct or not after key in the actual marking (2)	2	48	None						

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	Unit wrong orientation in tube	-Customer application failure (8)	8		-Wrong teach on material for pin1	1	-Auto-Pin 1 locate system by vision	-V/M gate first piece check (4) --Buddy check(7) -Auto-Pin 1 locate system by vision(1)	1	8	None						
			8		-Improper vision setting	1	-Regular setup checklist check.	-V/M gate sampling check (8) -Vision system auto detect and alarm (2) -Auto-Pin 1 locate system by vision(1)	1	8	None						
DRY PACK	Bag leakage	-Reliability failure (8)	8		-Break MBB	1	N/A	-QA 100% check packing quality for every box (6)	6	48	None						
			8		-Poor dry pack bag quality	1	N/A	-QA 100% check packing quality for every box (6)	6	48	None						
	No-dry pack	-Reliability failure (8)	8		-Miss dry pack process	1	N/A	-QA 100% check packing quality for every box(6)	6	48	None						

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	Mixed product	-Electrical failure(8) -Reliability failure (8)	8		-Operator handles more than one lot at same time.	2	-One time one lot	-Automated verification barcode of box, dry bag by auto-verify machine (2) -QA check (8)	2	32	None						
	Duration time out of control	- Delamination issue (8) - Solderability issue (8)	8		-The lot duration time was out of control	2	N/A	- System auto detect duration time before dry packing (2)	2	32	None						

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Control Number/Issue: 83MCT00018A/AY
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Burn in	ESD/EOS	-Electrical failure(8) -Reliability failure (8)	8		-Wrist strap and/or shoes function fail	1	-Turnstile wrist strap check during every entry to test floor	-Q-check yield control (3)	3	24	None						
			8		-Workstation and equipment are not properly grounded	1	-Monthly check/half year PM	-Q-check yield control (3)	3	24	None						
	Product mixed/escaped	-Electrical failure(8) -Reliability failure (8)	8		-Operate more than one lot at same time	2	-Handle only one lot in one table / Loader & Unloader -Perform marking inspection before lot start -Material status identification before/after process -100% check before next chamber start	-Quantity count (6) -Sampling check the marking (8) -100% auto VM inspection in packaging process. (4)	4	64	None						
			8		-Wrong program used	1	-Only the latest Rev. program available	-Buddy check (7) -Q check detection (3)	3	24	None						

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	Miss Burnin	-Customer application failure(8) -Reliability failure (8)	8		-Operator miss lot in Burnin peocess	1	-Follow TSO and SFC instruction -Auto start BI function to prevent miss BI	-Buddy check (7) - 100% auto electrical test in packaging process (4)	4	32	None						
			8		-Socket open/short	2	-Check and change socket during PM -Check before loading units	--Q check & BIN2 check detection (3) -Sampling check in loading process (8)	3	48	None						
	Bend lead & coplanarity	-Visual mechanical failure (6) -Customer application failure(8)	8		-Nonstandard manual handling mode	2	Set up standard manual handling method	-100% VM inspection (6) -100% auto VM inspection in packaging process (4)	4	64	None						
			8		-Bad socket	2	-Check and change socket during PM -Check before loading units	-100% VM inspection (6) -100% auto VM inspection in packaging process (4)	4	64	None						
			8		-Loader & unloader machine misalignment	2	-Half year PM -Shiftly check handler by setup checklist	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						

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	Foreign matter on lead	- Electrical failure (8)	8		-Particle from B/I board	1	-Periodical clean B/I boards -Check B/I boards by lot	-100% VM inspection(6)	6	48	None						
	Ball damage	-Visual mechanical failure (6) -Customer application failure(8)	8		-Nonstandard manual handling mode	2	Standard manual handling method	-100% auto VM inspection in packaging process (4) -In-process sampling check (8)	4	64	None						
Material receiving (Receive & store material)	Product mixed	-Yield Loss (7) -Customer Line pull (8)	8		Multiple lot processed simultaneously	2	1. Periodical Training to MTL Operators 2. Mobile SFC terminal to eliminate bulk processing of shop order	- Manual verify box label LOT#, device #, box quantity against packing list & SFC - Accept on zero discrepancy (6) - 100% Marking check by Vision system in Packaging process(4)	4	64	Auto Print Box Qty and # on Barcode label Sev=8, Occ=1, Det=4, RPN=32	Liang Yang R57253/06-30-2014					

POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

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	Count variance (CV)	Qty shortage	3		Miss Counting by Assembly or BI Site	2	Mobile SFC terminal to eliminate bulk processing of shop order	- Manual verify box label LOT#, device #, box quantity against packing list & SFC - Accept on zero discrepancy (6) - 100% Count Qty by Test operator (5)	5	30	None						
INCOMING CHECK (Visual Mechanical only applies to Assembly & BI rawstock)	Count variance (CV)	Qty shortage	3		Miss Counting by Assembly or BI Site	2	NA	- Manual verify box label LOT#, device #, box quantity against packing list & SFC - Accept on zero discrepancy (6) - 100% Count Qty by Test operator (5)	5	30	None						
	Raw stock issue	Marking mismatch with System/shop order	3		Device mixed at Assembly or BI process	3	NA	- Sampling Marking inspection during incoming check (5)	5	45	None						

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	V/M Defect	-Visual mechanical failure (6) -Customer application failure(8)	8		V/M defect introduced by Assembly or BI process	2	NA	- Sampling V/M inspection during incoming check (5) - 100% Marking check by Vision system in Packaging process(4)	4	64	None						
ELECTRICAL TEST as per test shop order 1. Machine preparation 2. Start lot 3. Electrical parameters tests 4. End lot (Hot/Cold/Room)	Lot Combination by mistake	Yield Loss (7) Customer line pull (8)	8		Mixed with Other device	1	Config lot combine rule in SFC system	- ATE Test (3)	3	24	None						

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			8		mixed with other trace code	1	Config lot combine rule in SFC system	-lot informaiton and marking check post combination (6) -100% Count Qty by Test operator before test(5) -100% auto VM inspection in Packaging process.(4)	4	32	None						
	Expired BI window	Infant mortality, fail electrical test during board assembly (8)	8		Lot staged for too long after BI	1	Daily WIP review by mfg and planner. Test priority given to material with BI window. Expected BI expiry date can be viewed in genesis through lot enquiry screen	- Auto hold lot with expired BI window (2)	2	16	None						
	Wrong machine setup	Fail 1st article check (3) Unable to perform test (2)	3		Use wrong tester	1	Listed Tester information on TSO Test program is configed by tester	- Operator check tester vs. TSO during setup (5) - Program auto verify during download (1)	1	3	None						
			3		Use wrong handler	2	Listed handler information on TSO	- Operator check Handler vs. TSO during setup (5)	5	30	None						

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			3		Wrong loadboard identification	3	Engineer create loadboard ID and buyoff loadboard before releasing to production (applies for NPI as well)	- Manual visual verification on loadboad ID during loadboard issuing/receiving/PM (5)	5	45	None						
			3		Wrong shoporder loadboard ID setup	3	NA	- QA Document Audit (6)	6	54	Work with IT team to convert LB information to SFC system. Sev=3, Occ=2, Det=6, RPN=36	Wei Chen R65950/06-30-2014					
			3		Tray loaded in wrong orientation	1	Poka Yoke mechanism on Handler	- Auto alarm for wrong orientation (2) - ATE Test (3)	2	6	None						
	Wrong test temperature	Yield Loss (7) Customer line pull (8)	8		Error during manual temperature selection	2	SC2 auto temperature loading (except MST)	- QC in line gate (4) - QA Document Audit (6) - QA shiftly audit (8)	4	64	None						

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			8		Wrong O/I configuration setup	3	Dedicate engineering personel to perform O/I configuration	- QA Document Audit (6) - Auto-trigger on missing configuration to respective PE through scheduled auto database check (3)	3	72	Download Gen2Spec parameters to auto-generate SC configuration file using SC Config file generation tool Sev=8, Occ=2, Det=3, RPN=48	Liang Yang R57253/05-30-2014					
	Use wrong program	Customer Line pull (8) Yield Loss (7)	8		TSO not updated timely to reflect program revision	1	Only effective version of Test program is available in Server	-Auto verify program information before test start (2) - First 200 units yield check(5) - QA Document Audit (6)	2	16	None						
			8		Program selection error	2	1. Listed test program information on TSO; 2. Listed handler information on TSO; 3. Auto-program loading except for A5 & MST	- QA Document Audit (6) - Buddy check before test (7) - QC in line gate (4) - QA shiftly audit (8)	4	64	None						

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			8		SPV Program selection error	1	1. Enforce expiry duration on program reside in SPV 2. Auto SPV program loading on SC2	- QC in line gate (4) - QA Document Audit (6) - QA shiftly audit (8)	4	32	None						
			8		Wrong O/I configuration setup	2	Dedicate engineering personel to perform O/I configuration Download Gen2Spec parameters to auto-generate SC configuration file	- QA Document Audit (6) - Auto-trigger on missing configuration to respective PE through scheduled auto database check (3)	3	48	None						
	ESD/EOS	Customer Line pull (8) Yield Loss (7)	8		-Wrist strap and/or shoes function fail	1	-Turnstile wrist strap check during every entry to test floor	-Yield limit and SBL check (3) -JVT test at last insertion (3)	3	24	None						
			8		No grounding (work station / rack)	1	-Quarterly check	-Yield limit and SBL check (3) -JVT test at last insertion (3)	3	24	None						

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Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	SEV	Class	Potential Cause(s)/ Mechanism(s) of Failue	OCC	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	DET	RPN	Recommended Action(s)	Responsibility & Target Completion Date	Action Results: Actions Taken & Effective Date	SEV	OCC	DET	RPN
			8		Inaccurate placement for ionizer	1	Use bracket to hold ionizer at a specific correct place	- QC in line gate (4) - High electrical fall out at next insertion for leakage or idd failure (3) - JVT test at last insertion (3)	3	24	None						
			8		Testers / Handlers environment	2	Check grounding and ionizer properly installed during half year PM	- JVT test at last insertion (3)	3	48	None						
			8		Spike voltage on the DC measurement	1	Spike check during NPI release	-Yield limit and SBL check (3) -JVT or equivalent test methodology (3)	3	24	None						
			8		Loadboard traces shorted	2	continuity check during Loadboard buyoff and Loadboard PM	-Yield limit and SBL check (3) -JVT or equivalent test methodology (3)	3	48	None						

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POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

Item: Burn In/Final Test/Test Backend
Type: ___ Design _x_ Process
Prepared By: Liang Yang
Core Team: Peg Tang,ZJ-TEST2 Hu,Peter Zhang,Dong Gao,Liang Yang,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng D

Control Number/Issue: 83MCT00018A/AY
Company,Group,Site/Business Unit: Freescale,TJN-FM
FMEA Date: 27-Jun-01 (Orig.)
06-Sep-13 (Rev.)

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	Product mixed/escaped	Customer Line pull (8) Yield Loss (7)	8		-Mix of rawstock and tested units / Mix of rawstock and reject from different lot	4	-Handle only one lot in one station -Perform marking inspection before lot start -Material status identification before/after process -Treat all uncomfirming units and PE used units as rejects - Proper labeling using lot identification barcode - Pending rack, Input & output rack with proper labeling - Label all work place for proper material segregation -All tested good partial/full tube are to be placed inside or next to the tested good box -Identified color tray/tube to collect rejects -Separate pending rack away from input rack by Using different appearance and	-Quantity count (6) -Sampling check the marking (8) -QC in line gating (4) -100% auto VM inspection in packaging process. (4) -Test program auto detect part difference (3) -Optimize ECID system to auto hold material if the ECID doesn't match between different insertion (2)	2	64	None						

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			8		Miss test insertion or in line gate	1	Test flow configed and auto controlled by Genesis system	- Genesis auto verify test flow during transaction (1)	1	8	None						
			8		-Wrong binning setting of handler	1	-Disable the bin setting button at the operation interface to prevent misclick. -Use SC2 auto control bin setting	-QA document audit (6) -QC in line gate (4)	4	32	None						
			8		-Leftover unit in equipment	2	-Clear machine before and after test -Lot count before start testing -Centralized reject scrapping at QA area after QA validation	-Marking inspection for first 200 units (5) -Quantity count (6) -Using SC2 auto count lot quantity except MST, A5 (3)	3	48	None						
			8		-speed sort device mixed	1	-Using different color tray/tube to replace different color clip for material identification	-QA document audit (6) -QC in line gate (4)	4	32	None						

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			8		-Wrong customer code key in for factory programming product	1	-Add password verification to guaratee correct customer code input -Add customer code check on gate test	-QA document audit (6) -QC in line gate (4) -100% EEV test (3)	3	24	None						
			8		-Engineer/ Techincian mishandling during on line debug	1	-Handle only one lot in one station -follow on line debug instruction -Material status identification before/after process -Treat PE used units as rejects -System auto clear testsite when quit engineer testing mode and sort all verification units into reject tray	-Quantity count (6) -Sampling check the marking (8) -QC in line gate (4)	4	32	None						

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			8		Leftover unit on recycle tray	2	-Check recycle tray before putting them into machine -Standard operation of recycle tray checking -partial tray alert	-100% auto VM inspection in packaging process (4) -Quantity count (6) -Sampling check the marking (8) -QC in line gate (4)	4	64	None						
			8		Battery Backup Unit (BBU) memory full causing Castle handler fail to pickup rawstock unit and indexed to main tray buffer as an empty tray	1	Castle handler firmware upgraded to auto clear BBU once 'handler empty' status is prompt.	1. QC in line gate. (4) 2. QA shiftly audit (8) 3. Quantity count (6)	4	32	None						
			8		Bin1 units from previous insertion are not cleared from output bin1 stacker / rack	5	NA	- QC in line gate. (4) 2. QA shiftly audit (8) 3. ECID detection method for applicable products (2) 4. Quantity count (6)	2	80	Station Controller auto stop test program loading if any units detected at output area SEV=8, OCC=2, DET=2, RPN=32	Peng Lin R65908/06-28-2014					

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			8		Reject mixed into good during machine downtime eg. During maintenance	2	1. Rawstock and tested material segregation by operator during machine down 2. Technician to use only rawstock material for setup during maintenance. All units are to be placed back into rawstock material 3. Scrap jammed units 4. Centralized reject scrapping in QA area after QA validation	-QC in line gate. (4) - QA shiftly audit (8) - ECID detection method for applicable products (3)	3	48	None						
	Non qualified engineering lot shipped to customer	Customer application failure (8)	8		Use production lot class for engineerig purpose causing lot shipped as production lot to customer.	2	Any engineering lot need to use engineering lot class. Log in MDR for engineering lot class to ship as normal production lot class.	All engineering lot class require MDR prior shipment. (2)	2	32	None						

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	Low yield or SBL over limit (DC, functional, parametric, open/short, electrical)	- Yield loss (7)	7		Tester out of calibration	1	- Tester calibration during regular PM	- Yield limit control in Genesis (3) - SBL limit control (3) -Auto calibration every program loading (2) -Diagnostic during PM (5)	2	14	None						
			7		-Wrong binning setting of handler	1	-Disable the bin setting button at the operation interface to prevent misclick. -Use SC2 auto control bin setting	-QA document audit (6) -QC in line gate (4)	4	28	None						
			7		- Handler setup problem	1	- Handler regular PM - Set up check	- Yield limit control in Genesis (3) - SBL limit control (3) - First 200 units yield check (4)	3	21	None						
			7		- Load Board problem	3	- Load board regular PM	- Yield limit control in Genesis (3) - SBL limit control (3) - First 200 units yield check (4)	3	63	None						

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			7		- Tester board problem	1	- Tester regular PM	- Yield limit control in Genesis (3) - SBL limit control (3) - First 200 units yield check (4)	3	21	None						
			7		- Poor contact at DUT socket (device under test)	3	- Contact interface regular replacement	- Yield limit control in Genesis (3) - SBL limit control (3) - First 200 units yield check (4)	3	63	None						
	Bend lead & coplanarity	-Visual mechanical failure (6) -Customer application failure(8)	8		-Device misplacement by hanlder	2	-Half year PM -Shiftly check handler by setup checklist	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						
			8		Unit overpress during test	1	Input quad hardstop to prevent overpress	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	32	None						

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			8		Bad socket/pogo pin	2	-Hard stopper configuration - Load board regular PM - Contact interface regular replacement	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						
			8		ATU causing drop units	2	1. Use CASM/CAIM to cycle ATU and observe for mechanical binding issue during handler PM 2. Designed tray catcher with loaded spring 3. Add mounting plate to tighten door sensor	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						
			8		Unit misplaced in tray at output handler	2	Handler buyoff after PM and conversion sort xyz alignment jig	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						

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			8		- Operator handles material manually.	2	- Certify operators' operation skill and yearly exam to check - Treat manual operated material as VM reject and scrap.	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						
			8		-Frost inside test chamber	2	-Warm up handler periodically -Use air pressure to prevent frozen during cold temperature test -System auto warm up cold temperature handler - SC2 Auto-defrost function	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						
			8		-Hit by damaged track corner	2	-Add chamfer at soak booster track and singulator track -Perform Track inspection when replacement during PM	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						

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	Ball damage	-Visual mechanical failure (6) -Customer application failure(8)	8		Bad socket/pogo pin	2	-Hard stopper configuration - Load board regular PM - Contact interface regular replacement	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						
			8		Unit jam at core section	2	1. Periodic handler PM to minimize jamming 2. Scrap impacted unit that jammed at core section	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						
			8		-Device misplacement by hanlder	2	-Half year PM -Shiftly check handler by setup checklist	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						
			8		Unit overpress during test	1	Input quad hardstop to prevent overpress	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	32	None						

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			8		Unit misplaced in tray at output handler	2	Handler buyoff after PM and conversion sort xyz alignment jig	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						
			8		FM on substrate	1	1. Use hanging nest with mold guided & chamfered design. 2. Auto-defrost for J750 3. Periodical handler cleaning 4. Boat clean during conversion	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	32	None						
			8		- Operator handles material manually.	2	- Certify operators' operation skill and yearly exam to check - Treat manual operated material as VM reject and scrap.	-In-process sampling check (8) -100% auto VM inspection in packaging process (4)	4	64	None						

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	Crack/chip	- Reliability failure (8) -Electrical failure (8) -Visual mechanical failure (6)	8		-Wrong handler adjustment	1	-Hard stopper configuration	-In-process sampling check (8) -Hard stopper auto alarm (2)	2	16	None						
			8		-Incorrect bushing on L/B	1	-Hard stopper configuration	-In-process sampling check (8) -Hard stopper auto alarm (2)	2	16	None						
			8		- Operator handles material manually in tray.	2	- Certify operators' operation skill and yearly exam to check - Treat manual operated material as VM reject and scrap. - Put a empty tray on the top before move out material from machine	- Tray gap check (6) -100% auto VM inspection in packaging process (4)	4	64	None						

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	Sliver & patchback (non pogo socket only)	Short circuit or leakage (8)	8		High plating material build up at test socket	2	Socket cleaning and replace regularly	- Yield limit control in Genesis (3) - SBL limit control (3) - First 200 units yield check (4) -V/M gate sampling check (8)	3	48	None						
	Pogo Burr	Visual Mechanical Failure (6)	6		Mechanical Contact offset on device lead due wear and tear of test socket pogo holes	2	Check for socket bushing conditions during PM. Replace socket if pogo holes found wear and tear	- V/M gate sampling check (8) - First 200 units V/M check (5)	5	60	None						
	Damaged lead foot plating surface	Solderability Failure (8)	8		test finger deformation	1	-Board regular PM - Check Pogo pin/socket befor&after each use	- V/M gate sampling check (8) - First 200 units V/M check (5)	5	40	None						
	Foreign Matter On Lead	Solderability Failure (8)	8		Dirt accumulated in handler boat	1	1. handler cleaning during shift start 2. boat clean during conversion	- V/M gate sampling check (8) - First 200 units V/M check (5)	5	40	None						

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			8		Unit drop out of tray	2	1. Strap Bin1 tray with cover tray right after testing 2. Unstrap rawstock bundle just before loading to ATU 3. Use CASM/CAIM to cycle ATU and observe for mechanical binding issue during handler PM (ATU issue) 4. Designed tray catcher with loaded spring (ATU issue) 5. Standardize tray latch spring to 0.32mm diameter (ATU issue) 6. Add mounting plate to tighten door sensor (ATU issue) 7. Treat dropped unit as reject	- V/M gate sampling check (8) - First 200 units V/M check (5) -100% auto VM inspection in packaging process (4)	4	64	None						

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			8		Usage of fibrous material at production floor	1	Banned cotton bud, fibrous glove and cloth from production floor	- QA shiftly audit (8) - V/M gate sampling check (8) - First 200 units V/M check (5)	5	40	None						
			8		FM stick on pogo pin	3	Socket cleaning and replace if necessary	- Yield limit control in Genesis (3) - SBL limit control (3)	2	48	None						
			8		FM from incoming/environment dropped to staging trays causing FM to attach to units when the trays are used.	1	Top tray cover for trays during staging period to prevent FM	-V/M gate sampling check (8) -100% auto VM inspection in packaging process (4)	4	32	None						
	Foreign Matter On Package Body	Solderability Failure (8)	8		FM from incoming/environment dropped to staging trays causing FM to attach to units when the trays are used.	1	Top tray cover for trays during staging period to prevent FM	Detection at TBE using 3x inspection (6)	6	48	None						

POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

Item: Burn In/Final Test/Test Backend
Control Number/Issue: 83MCT00018A/AY
Type: ___ Design _x_ Process
Company,Group,Site/Business Unit: Freescale,TJN-FM
Prepared By: Liang Yang
FMEA Date: 27-Jun-01 (Orig.)
Core Team: Peg Tang,ZJ-TEST2 Hu,Peter Zhang,Dong Gao,Liang Yang,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng D 06-Sep-13 (Rev.)

Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	SEV	Class	Potential Cause(s)/ Mechanism(s) of Failue	OCC	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	DET	RPN	Recommended Action(s)	Responsibility & Target Completion Date	Action Results: Actions Taken & Effective Date	SEV	OCC	DET	RPN
Laser mark	Missing mark	-customer application failure - 8	8		-Laser generator fail	1	-Machine auto check laser power before marking.	-First piece part verification after marking(4) -Machine auto alarm when power out of control(2) -QA Gate(8)	2	16	None						
	Illegible mark	Customer application failure - 8	8		Inappropriate laser power	2	Machine auto check laser power before marking.	-First piece part verification after marking(4) - Machine marking 100% auto scan in subsequent process (4) -QA visual inspection 200 units/lot(8) -Machine auto alarm when laser power abnormal.(2)	2	32	None						

POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

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			8		Laser generator worn out	1	NA	-First piece part verification after marking(4) - Machine marking 100% auto scan in subsequent process (4) -QA visual inspection 200 units/lot(8) -Machine auto alarm when laser power abnormal.(2)	2	16	None						
	Marking misalignment	Customer application failure - 8	8		Location pin damaged	1	NA	-First piece part verification after marking(4) - Machine marking 100% auto scan in subsequent process (4) -QA visual inspection 200 units/lot(8)	4	32	None						

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	Wrong marking	Customer application failure - 8	8		Marking information input error during manual operation	1	-Auto load marking information	-First piece part verification after marking(4) - Machine marking 100% auto scan in subsequent process (4) -QA visual inspection 200 units/lot(8)	4	32	None						
40x Inspection	Burr&sliver on shoulder/riser/ lead	-Visual mechanical failure (6) -Customer application failure(8)	8		Shoulder damaged by BI (failure identified by KLM)	2	NA	-10x V/M gate (8) - 100% auto vision inspection on device (2)	2	32	None						
	Bend lead & coplanarity	-Visual mechanical failure (6) -Customer application failure(8)	8		Unit out of pocket	2	1. Strap the tray whenever moving the material 2.Operator to check tray gap before and after strapping to ensure no unit jump out the pocket	-V/M gate (8) - 100% auto vision inspection on device (2)	2	32	None						

POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

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			8		Mishandling the unit	2	1. Strap the tray whenever moving the material 2.Operator to check tray gap before and after strapping to ensure no unit jump out the pocket	-V/M gate (8) - 100% auto vision inspection on device (2)	2	32	None						
	Wrong orientation	-Customer application failure (8)	8		Unit replaced in misorientated form	2	Pin1 reverification after unit replacement	-V/M gate sampling check (8) -Vision system auto detect and alarm (2) -Auto-Pin 1 locate system by vision(1) -Pin1 bar setting for tray locate(1)	1	16	None						
	Mixed product	-Electrical failure (8) -Reliability failure (8)	8		Stray units at inspection table	2	Clear work station after completion of lot.	-V/M gate sampling check (8) -Count quantity per shop order (6) - Vision 100% inspection (2)	2	32	None						

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			8		Swap Shop order	2	Process 1 lot at a time	-System record the marking teach history in test summary, operator 100% check summary(4) -System auto check and judge if marking is correct or not after key in the actual marking (2) 100% vision inspection	2	32	None						
			8		Swap bundle	2	Process 1 lot at a time	1. Lot no verification on barcode label vs TSO (3) 2. 100% vision scanning (2) 3. QA VM Gate (8)	2	32	None						
10x Inspection	Burr&sliver on shoulder/riser/ lead	-Visual mechanical failure (6) -Customer application failure(8)	8		Shoulder damaged by BI (failure identified by KLM)	2	NA	-10x V/M gate (8) - 100% auto vision inspection on device (2)	2	32	None						

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	Bend lead & coplanarity	-Visual mechanical failure (6) -Customer application failure(8)	8		Unit out of pocket	2	1. Strap the tray whenever moving the material 2.Operator to check tray gap before and after strapping to ensure no unit jump out the pocket	-V/M gate (8) - 100% auto vision inspection on device (2)	2	32	None						
			8		Mishandling the unit	2	1. Strap the tray whenever moving the material 2.Operator to check tray gap before and after strapping to ensure no unit jump out the pocket	-V/M gate (8) - 100% auto vision inspection on device (2)	2	32	None						

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	Wrong orientation	-Customer application failure (8)	8		Unit replaced in misorientated form	2	Pin1 reverification after unit replacement	-V/M gate sampling check (8) -Vision system auto detect and alarm (2) -Auto-Pin 1 locate system by vision(1) -Pin1 bar setting for tray locate(1)	1	16	None						
	Mixed product	-Electrical failure (8) -Reliability failure (8)	8		Stray units at inspection table	2	Clear work station after completion of lot.	-V/M gate sampling check (8) -Count quantity per shop order (6) - Vision 100% inspection (2)	2	32	None						

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			8		Swap Shop order	2	Process 1 lot at a time	-System record the marking teach history in test summary, operator 100% check summary(4) -System auto check and judge if marking is correct or not after key in the actual marking (2) 100% vision inspection	2	32	None						
			8		Swap bundle	2	Process 1 lot at a time	1. Lot no verification on barcode label vs TSO (3) 2. 100% vision scanning (2) 3. QA VM Gate (8)	2	32	None						
Bake	Mixed product	-Electrical failure (8) -Reliability failure (8)	8		-Operator handles the wrong device without check marking	3	-Ensure only one lot in work table for tube package. - Verify lot number/ magazine number vs. shop order	-Count the quantity for tube package(6) -100% auto vision inspection in subsequence process (4)	4	96	Using bakeable tube to avoid mistake during tube to tube process SEV=8, OCC=1, DET=4, RPN=32	HONGZHI REN B06298/04-30-2014					

POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

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Prepared By: Liang Yang — FMEA Date: 27-Jun-01 (Orig.)

Core Team: Peg Tang,ZJ-TEST2 Hu,Peter Zhang,Dong Gao,Liang Yang,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng D — 06-Sep-13 (Rev.)

Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	SEV	Class	Potential Cause(s)/ Mechanism(s) of Failue	OCC	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	DET	RPN	Recommended Action(s)	Responsibility & Target Completion Date	Action Results: Actions Taken & Effective Date	SEV	OCC	DET	RPN
	Miss bake	-Reliability failure (8)	8		-Operator forgets to do bake step and transfer the material to the next step.	2	-Follow TSO and SFC instruction	-Genesis system control (2) -Buddy check (7)	2	32	None						
			8		-Place pre-bake units into post-bake units	2	-Different requirement lot stock in different area	-Genesis system control (2)	2	32	None						
	Time/Temperature incompetent	-Customer application failure (8)	8		-Wrong time and temperature	1	-Fix timer and temperature controller to auto-monitor	-Auto check system alarm(2)	2	16	None						
Dry air storage	Moisture out of control	- Delamination issue (8) -Customer application failure (8)	8		- Dry air barometric pressure low	1	N/A	- Flow meter check per setup checklist (6) - HIC monitor / open the Dry air cabinet (6)	6	48	None						
	Miss Dry air storage	- Delamination issue (8) -Customer application failure (8)	8		-Operator forgets to put the lot into the Dry air cabinet	2	-Follow SFC instruction.	-Buddy check (7) -Genesis system control (2)	2	32	None						

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3x inspection	Bend lead & coplanarity	-Visual mechanical failure (6) -Customer application failure(8)	8		Unit out of pocket	2	1. Strap the tray whenever moving the material 2.Operator to check tray gap before and after strapping to ensure no unit jump out the pocket	-V/M gate (8) - 100% auto vision inspection on device (2)	2	32	None						
			8		Mishandling the unit	2	1. Strap the tray whenever moving the material 2.Operator to check tray gap before and after strapping to ensure no unit jump out the pocket	-V/M gate (8) - 100% auto vision inspection on device (2)	2	32	None						

POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

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	Wrong orientation	-Customer application failure (8)	8		Unit replaced in misorientated form	2	Pin1 reverification after unit replacement	-V/M gate sampling check (8) -Vision system auto detect and alarm (2) -Auto-Pin 1 locate system by vision(1) -Pin1 bar setting for tray locate(1)	1	16	None						
	Mixed product	-Electrical failure (8) -Reliability failure (8)	8		Stray units at inspection table	2	Clear work station after completion of lot.	-V/M gate sampling check (8) -Count quantity per shop order (6) - Vision 100% inspection (2)	2	32	None						

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			8		Swap Shop order	2	Process 1 lot at a time	-System record the marking teach history in test summary, operator 100% check summary(4) -System auto check and judge if marking is correct or not after key in the actual marking (2) 100% vision inspection	2	32	None						
			8		Swap bundle	2	Process 1 lot at a time	1. Lot no verification on barcode label vs TSO (3) 2. 100% vision scanning (2) 3. QA VM Gate (8)	2	32	None						
Lead scan	Bend lead & coplanarity	-Visual mechanical failure (6) -Customer application failure(8)	8		-Bent tray	2	NA	-Operator 100% check tray (6) - 100% auto vision inspection on device (2)	2	32	None						

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			8		- Unit misplace in tray caused by handler precision	2	-Half yearly PM	-V/M gate (8) - 100% auto vision inspection on device (2)	2	32	None						
	2D matrix unreadable	-Visual mechanical failure (6)	6		- Bypass 2D matrix inspection function	2	-High level password control	-System real time monitor (2)	2	24	None						
			6		- Dongle is unworkable	2	NA	-Program auto alarm and stop handler when dongle is unworkable(2)	2	24	None						
	Unit wrong orientation in tray	-Customer application failure (8)	8		-Improper vision set	1	-Regular setup checklist check.	-V/M gate sampling check (8) -Vision system auto detect and alarm (2) -Auto-Pin 1 locate system by vision(1) -Pin1 bar setting for tray locate(1)	1	8	None						

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			8		-Wrong teach on material for pin1	1	-Auto-Pin 1 locate system by vision	-V/M gate first piece check (4) --Buddy check(7) -Auto-Pin 1 locate system by vision(1) -Pin1 bar setting for tray locate(1)	1	8	None						
	Mixed product	-Electrical failure(8) -Reliability failure (8)	8		-Operator does not clear the machine when finished lot	2	-Equipment clean after lot end	-V/M gate sampling check (8) -Count quantity per shop order (6) - Vision 100% inspection (2)	2	32	None						
			8		-Operator teach wrong marking	3	NA	-System record the marking teach history in test summary, operator 100% check summary(4) -System auto check and judge if marking is correct or not after key in the actual marking (2)	2	48	None						

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	Crack/chip	- Reliability failure (8) -Electrical failure (8) -Visual mechanical failure (6)	8		- Operator handles material manually in tray.	2	- Certify operators' operation skill and yearly exam to check - Treat manual operated material as VM reject and scrap.	- Tray gap check (6) - 100% auto vision inspection (2)	2	32	None						
Tape & Reel	Cover tape loosen / tighten	-Device fail out or cover tape split at customer (8)	8	*	-Peel back force is out of control	1	-Follow setup checklist to set up machine	- SPC system control (4) -QA audit peel back force test record (6) -QA sealing line check (8)	4	32	None						
	2D matrix unreadable	-Visual mechanical failure (6)	6		- Bypass 2D matrix inspection function	2	-High level password control	-System real time monitor (2)	2	24	None						
			6		- Dongle is unworkable	2	NA	-Program auto alarm and stop handler when dongle is unworkable(2)	2	24	None						

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	Unit wrong orientation in tape reel	-Customer application failure (8)	8		-Wrong teach on material for pin1	1	-Auto-Pin 1 locate system by vision	-V/M gate first piece check (4) --Buddy check(7) -Auto-Pin 1 locate system by vision(1) -Pin1 bar setting for tray locate(1)	1	8	None						
			8		-Improper vision setting	1	-Regular setup checklist check.	-V/M gate sampling check (8) -Vision system auto detect and alarm (2) -Auto-Pin 1 locate system by vision(1) -Pin1 bar setting for tray locate(1)	1	8	None						
	Bend lead	-Visual mechanical failure (6) -Customer application failure(8)	8		-Machine pick up head is not in the perfect position along the X,Y,Z direction	2	- Cross beam installed on all tape reel equipment.	-V/M gate sampling check (8) -Handler cross sensor 100% check unit position and auto alarm(2) -Check per setup checklist (6)	2	32	None						

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POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)

Item: Burn In/Final Test/Test Backend
Control Number/Issue: 83MCT00018A/AY
Type: ___ Design _x_ Process
Company,Group,Site/Business Unit: Freescale,TJN-FM
Prepared By: Liang Yang
FMEA Date: 27-Jun-01 (Orig.)
Core Team: Peg Tang,ZJ-TEST2 Hu,Peter Zhang,Dong Gao,Liang Yang,Wei Chen,HONGZHI REN,LINGXUAN XU,Sinbad Liu,Peng D
06-Sep-13 (Rev.)

Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	SEV	Class	Potential Cause(s)/ Mechanism(s) of Failue	OCC	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	DET	RPN	Recommended Action(s)	Responsibility & Target Completion Date	Action Results: Actions Taken & Effective Date	SEV	OCC	DET	RPN
	Empty pocket	-Quantity shortage for customer (8)	8		-Pocket2 sensor does not work properly	2	NA	-Machine auto alarm (2) -Reel counter setup check (4) '-PM daliy check per setup check list (6)	2	32	None						
	Tape wrong revolution in reel	-Electrical failure (8)	8		-Operator forget to wind back orginal reel after reel to reel process	1	-Using black or blue reel for reel to reel. -Fix color reel to prevent mixed handling by operator	-QA 100% check tape revolution for every reel (6)	6	48	None						
			8		-Use white reel on reel to reel process	1	-Using black or blue reel for reel to reel. -Fix color reel to prevent wrong reel used.	-QA 100% check tape revolution for every reel (6)	6	48	None						
	Ball damage	-Visual mechanical failure (6) -Customer application failure(8)	8		-Machine pick up head is not in the perfect position along the X,Y,Z direction	2	- Cross beam installed on all tape reel equipment.	-Handler cross sensor 100% check unit position and auto alarm(2) -Check per setup checklist (6)	2	32	None						

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	Cover tape misalignment with carrier tape	-Customer application failure (8)	8		-Technician adjust the guider width or carrier tape location pins improperly.	2	NA	-Technician first piece check under 10X microscope after technician adjust the guider width or carrier tape location pins. (4)	4	64	None						
	Mixed product	-Electrical failure(8) -Reliability failure (8)	8		-Operator does not clear the machine when finished lot	2	-Equipment clean after lot end	-V/M gate sampling check (8) -Count quantity per shop order (6) - Vision 100% inspection (2)	2	32	None						
			8		-Operator teach wrong marking	3	NA	-System record the marking teach history in test summary, operator 100% check summary(4) -System auto check and judge if marking is correct or not after key in the actual marking (2)	2	48	None						

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TTT	Lead defect in tube	-Visual mechanical failure (6) -Customer application failure(8)	8		-Tube and tracking alignment	1	-Re-design the tracking to optimize alignment	-V/M Gate sampling check (8) --Frist piece check (4)	4	32	None						
	Mixed product	-Electrical failure(8) -Reliability failure (8)	8		-Operator does not clear the machine when finished lot	2	-Equipment clean after lot end	-V/M gate sampling check (8) -Count quantity per shop order (6) - Vision 100% inspection (2)	2	32	None						
			8		-Operator teach wrong marking	3	NA	-System record the marking teach history in test summary, operator 100% check summary(4) -System auto check and judge if marking is correct or not after key in the actual marking (2)	2	48	None						

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Process Function/ Requirements	Potential Failure Mode	Potential Effect(s) of Failure	SEV	Class	Potential Cause(s)/ Mechanism(s) of Failue	OCC	Current Design/ Process Controls Prevention	Current Design/ Process Controls Detection	DET	RPN	Recommended Action(s)	Responsibility & Target Completion Date	Action Results: Actions Taken & Effective Date	SEV	OCC	DET	RPN
	Unit wrong orientation in tube	-Customer application failure (8)	8		-Wrong teach on material for pin1	1	-Auto-Pin 1 locate system by vision	-V/M gate first piece check (4) --Buddy check(7) -Auto-Pin 1 locate system by vision(1)	1	8	None						
			8		-Improper vision setting	1	-Regular setup checklist check.	-V/M gate sampling check (8) -Vision system auto detect and alarm (2) -Auto-Pin 1 locate system by vision(1)	1	8	None						
DRY PACK	Bag leakage	-Reliability failure (8)	8		-Break MBB	1	N/A	-QA 100% check packing quality for every box (6)	6	48	None						
			8		-Poor dry pack bag quality	1	N/A	-QA 100% check packing quality for every box (6)	6	48	None						
	No-dry pack	-Reliability failure (8)	8		-Miss dry pack process	1	N/A	-QA 100% check packing quality for every box(6)	6	48	None						

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	Mixed product	-Electrical failure(8) -Reliability failure (8)	8		-Operator handles more than one lot at same time.	2	-One time one lot	-Automated verification barcode of box, dry bag by auto-verify machine (2) -QA check (8)	2	32	None						
	Duration time out of control	- Delamination issue (8) - Solderability issue (8)	8		-The lot duration time was out of control	2	N/A	- System auto detect duration time before dry packing (2)	2	32	None						

Control Plan

TSMC PPAP Documents

• TSMC PPAP documents (FMEAs, Control Plans, Cpks, and GR&R) are considered proprietary information by TSMC, classified as "TSMC INTERNAL USE ONLY" and cannot be distributed with Freescale PPAPs in accordance with an agreement with TSMC.

• The PPAP documents are pulled by Freescale External Manufacturing Quality and checked for compliance with TS16949 requirements.

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• If there are any questions, please contact:

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Assembly Process Control Plan-SOIC

Control Plan Number/Issue		Prototype / Pre-launch (XC) / Production	Key Contact/Phone	Date(Orig.)		Date (Rev.)
70MCT00015A002/O			Amanda Wang/6368	30-Nov-13		30-Nov-13
Part Number		Core Team	Wang Amanda, Zheng Junying, Kang Xiaohui, Yao Shuan, Chen Grayson, Wang Jinsheng, Tao Xin, Han Z.L, Hu J.Z, Zhao Dong, Roger Guo, Derk Song, Ma Qianfeng	Customer Engineering Approval (If Req'd)		
Name/Description: SOIC 16/28/32 /54 LD Assembly Cu wire		Supplier/Plant: FSL-TJN-FM	Supplier Code	Customer Quality Approval/Date (If Req'd)		

FLOWCHART LEGEND

PROD=Production Operation **INSP**=Inspection **MEAS**=Measurement **QA**=QA Monitor **GATE**=QA Gate **XFER**=Material Transfer **MAT**=Material Inspection

				Characteristics					Sample			
Flow Chart Symbol	Process/ Operation Number	Process Name/ Operation Description	Machine, Device, Jig, Tools for Mfg.	Product	Process	Special Char. Class	Product/Process Specification/ Tolerance	Evaluation Measurement Technique	Size	Freq.	Control Method	Reaction Plan
PROD	3.2	pre-wire bond plasma clean	plasma machine		parameter		12MCT20031B007	visual	N/A	1. 1x/machine/shift 2. 1x/after machine repair	12MCT20070A 12MCT10020A 12MCT20120A004 12MCT10110A001 12MCT20031B007	12MCT20070A 12MCT20031B003
MEAS		pre-wire bond plasma clean monitor	goniometer	contact angle			<10deg for die surface	measurement	2 points/strip, 3 strips/x	1x/machine/shift		
							<50deg for leadframe surface	measurement	1point/strip, 3 strips/x	1x/machine/shift		
PROD	4	Cu wire bond 1 / To bond wires from pad to post	wire bonder		parameter		12MCT20031S020	visual	N/A	1.1x/device change; 2.1x/parameter change; 3.1x/after machine repair.	12MCT20070A 12MCT10020A 12MCT20070A006 12MCT20031S020 12MCT10110A001	12MCT20070A 12MCT20031K004
			Cu wire		Cu wire work life		144hrs	auto control system	N/A	100% material system auto control		
			capillary		capillary life		12MCT20031S020	visual	N/A	machine auto control		
INSP		wire bond monitor 1	microscope (>=30x)	visual & mechanical defects			12M54564J	visual	3 pitches/strip; 2 strips/magazine	1x/magazine	12MCT20070A 12MCT10020A 12MCT10110A001	12MCT20070A 12MCT20031K004
MEAS		wire pull monitor 1	wire pull tester	wire pull strength		*	12MCT20070A	measurement	6 wires/x	1. 1x/machine/shift; 2. 1x/device change; 3. 1x/parameter change; 4. 1x/capillary change.	12MCT20070A 12MCT10020A 12MCT10030A 12MCT20080C	12MCT20070A 12MCT20031K004
		ball shear monitor 1	ball shear tester	ball shear strength		*	12MCT20070A	measurement	6 wires/x	1. 1x/machine/shift; 2. 1x/device change; 3. 1x/parameter change; 4. 1x/capillary change.	12MCT20070A 12MCT10020A 12MCT10030A 12MCT20080C	12MCT20070A 12MCT20031K004
		ball size monitor	microscope(>=200x)	ball size			12MCT20070A	measurement	4 balls/x	1. 1x/device change; 2. 1x/parameter change; 3. 1x/capillary change.	12MCT20070A 12MCT10020A 12MCT20070A006 12MCT10110A001	12MCT20070A 12MCT20031K004
		ball height monitor	microscope(>=200x)	ball height			12MCT20070A	measurement	4 balls/x	1. 1x/device change; 2. 1x/parameter change; 3. 1x/capillary change.	12MCT20070A 12MCT10020A 12MCT20070A006 12MCT10110A001	12MCT20070A 12MCT20031K004

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Process Control Plan -- GENERAL TEST FLOW

Control Plan Number/Issue		Prototype / Pre-launch (XC) / Production	Key Contact/Phone	Date(Orig.)	Date (Rev.)
70MCT00019A/AW	**X**		**Tang Peg (85686866)/Hu Z.J(85686770)**	**5/10/1997**	**11/25/2013**

Part Number	Core Team	Customer Engineering Approval (If Req'd)
GENERAL TEST	**Duan Peng, Chen Wei, Diao William, Liu X.J., Gao Dong, Yang Liang, Wang K.Q., Yin Wally, Xu Lingxuan.**	

Name/Description	Supplier/Plant	Supplier Code	Customer Quality Approval/Date (If Req'd)
GENERAL TEST FLOW	**FSL-TJN-FM**		

FLOWCHART LEGEND
PROD=Production Operation **INSP**=Inspection **MEAS**=Measurement **QA**=QA Monitor **GATE**=QA Gate **XFER**=Material Transfer **MAT**=Material Inspection

Flow Chart Symbol	Process Operation Number	Process Name/Operation	Machine Device,Jip,Tools for Mfg	Characteristics		Special Char. Class	Product/Process /Specification /Tolerance	Evaluation Measurement Technique	Sample		Control Method	Reaction Plan
				Product	Process				Size	Freq.		
MAT	1	MATERIAL RECEIVING	Assembly Shop Order Packing list, SFC System		Documentation		12MCT50044C	Visual	100%	Every lot	Verify box label LOT#, device #, box quantity against packing list & SFC	Hold lot for disposition 12MCT50040A
PROD	2	INCOMING CHECK (Visual Mechanical only applies to assembly & BI rawstock)	Assembly Shop Order Test Shop Order SFC System		Quantity		12MCT50044C	Visual	100%	Every lot	Count physical quantity againest assembly shop order	Hold lot for disposition 12MCT50040A 12MCT50040A020 12MCT50040A021
					Documentation			Visual	100%	Every lot	Verify box label LOT#, device #, lot status in SFC system	
INSP			vision machine (optional)		Visual Mechanical		12MRM09116A	Visual or vision machine (optional)	Per 12ACT20080A	Every lot	Visual verification for visual defect	
PROD	3	ELECTRICAL TEST as per test shop order 1. Machine preparation 2. Start lot 3. Electrical parameters tests 4. End lot (Hot/Cold/Room)	Test Shop Order		Machine Type		12MCT50040A	Visual	100%	Every conversion	Manual visual verification machine according to test shop order	Hold for disposition 12MCT50040A
PROD			Test Shop Order		Temperature		Test Shop Order	Continuous Test Temperature monitoring	100%	Every test insertion	Handler temperature auto-guardbanding using temperature controller	Handler stop until temperature is within guardband
PROD			Test Shop Order SFC system		Yield (Start lot)		12MCT50040A 12MCT10240A	Electrical Test	Per 12ACT20080A	Every lot	Calculate the yield after sampling test done and compare with shut down yield	Stop the machine and call PE/TPE/PM. 12MCT50040A 12MCT10240A 12MCT50040A010 12MCT50040A012 12MCT50040A015 12MCT50040A018
INSP			vision machine (optional)		Visual Mechanical (Start lot)		12MRM09116A	Visual or vision machine (optional)	Per 12ACT20080A	Every lot	Visual verification for visual defect	Stop the machine and call supervisor. 12MCT50040A 12MCT50040A004 12MCT50040A010 12MCT50040A012 12MCT50040A015
PROD			ATE	Electrical Parameter			12MCT50040A	Electrical Test Program	100%	Every lot	Electrical Yield limit per SFC System	Stop the machine and call PE/TPE/PM. 12MCT50040A 12MCT50040A004 12MCT50040A010 12MCT50040A012 12MCT50040A015 12MCT50040A018
INSP			Vision machine (optional)		Visual Mechanical (In process)		12MRM09116A	Visual or vision machine (optional)	Per 12ACT20080A	Every lot	Visual verification for visual defect	Stop the machine and call supervisor. 12MCT50040A 12MCT50040A004 12MCT50040A010 12MCT50040A012 12MCT50040A015
					Yield (End lot)		12MCT50040A 12MCT10240A	Electrical Test	100%	Every lot	Electrical Yield limit per SFC System	Hold lot for disposition 12MCT10240A

Process Control Plan -- GENERAL TEST FLOW

Control Plan Number/Issue		Prototype Pre-launch (XC) Production	Key Contact/Phone	Date(Orig.)	Date (Rev.)
70MCT00019A/AW	**X**		**Tang Peg (85686866)/Hu Z.J(85686770)**	**5/10/1997**	**11/25/2013**

Part Number	Core Team	Customer Engineering Approval (If Req'd)
GENERAL TEST	**Duan Peng, Chen Wei, Diao William, Liu X.J., Gao Dong, Yang Liang, Wang K.Q., Yin Wally, Xu Lingxuan.**	

Name/Description	Supplier/Plant	Supplier Code	Customer Quality Approval/Date (If Req'd)
GENERAL TEST FLOW	**FSL-TJN-FM**		

FLOWCHART LEGEND

PROD=Production Operation **INSP**=Inspection **MEAS**=Measurement **QA**=QA Monitor **GATE**=QA Gate **XFER**=Material Transfer **MAT**=Material Inspection

Flow Chart Symbol	Process Operation Number	Process Name/Operation	Machine Device,Jip,Tools for Mfg	Characteristics		Special Char. Class	Product/Process /Specification /Tolerance	Evaluation Measurement Technique	Sample		Control Method	Reaction Plan
				Product	Process				Size	Freq.		
PROD			Test Shop Order SFC system		Quantity		12MCT50040P	Visual	100%	Every lot	Count physical quantity and record on test shop order & SFC	Hold lot for disposition 12MCT50040A 12MCT50040A005 12MCT50040A019
					Documentation			Visual	100%	Every lot	Check test result againest physical quantity, confirm the lot status in SFC system	Hold lot for disposition 12MCT50040A
GATE	4	ELECTRICAL TEST (QC In-line) as per shop order (Hot/Room/Cold): Applicable for specific products as specified in the Test Shop Order or SFC system	ATE Test Shop Order SFC system	Electrical Parameter			12MCT50040A 12ACT20080A	Electrical Test Program	Per 12ACT20080A	Per Skip Plan	Accept on zero failure	Hold lot for disposition 12ACT20080A 12MCT50040A 12MCT50040A010 12MCT50040A012 12MCT50040A013 12MCT50040A015
					Quantity		12MCT50040P	Visual	100%	Every lot	Count physical quantity and record on test shop order & SFC	Hold lot for disposition 12MCT50040A 12MCT50040A005 12MCT50040A019
					Documentation			Visual	100%	Every lot	Check test result againest physical quantity, tranfer the lot to next step in SFC system	Hold lot for disposition 12MCT50040A
PROD	5	QUALITY CONTROL Stage: 1. Verification for test result 2. Visual inspection on final good unit			Quantity		12MCT10123G	Visual	100%	Every lot	Count physical quantity againset test shop order	Hold lot for disposition 12MCT50040A 12MCT50040A005 12MCT50040A019
					Documentation			Visual	100%	Every lot	Check test result againest test shop order, verify lot status in SFC system	Hold lot for disposition 12MCT50040A
INSP			Microscope(optional)		Visual Mechanical		12MRM09116A	Visual or Microscope(optional)	Per 12ACT20080A	Every lot	Visual verification for visual defect	Hold lot for disposition 12MCT50040A 12MCT50040A004

NOTE
1. ATE:Auto Testing Equipment
2. Visual: Unaided eye or 3x magnifier (optional)

REVISION HISTORY

Part Number:	GENERAL TEST	Control Plan Number/Issue:	70MCT00019A/AW	
Name/Description:	GENERAL TEST FLOW	Control plan Date:	5/10/1997	(Orig.)
Supplier/Plant:	FSL-TJN-FM		11/25/2013	(Rev.)

Revision Date	Description of Revison & Writer	Spec Coord	Effectivity Date
O	VERSION O	J.W ZHANG	5/10/1997
A	CHANGE ERROR WORD	J.H ZHANG	12/14/1997
B	CHANGE CORE TEAM MEMBER	J.H ZHANG	3/3/1998
C	CHANG FORMAT	J.H ZHANG	5/10/1998
D	CHANG DOCUMENT TITLE	J.H ZHANG	6/6/1998
E	spelling mistake	J.H ZHANG	10/10/1998
F	Modify "Key contact/phone and Core team"	J.H ZHANG	12/20/1998
G	Change Format	J.H ZHANG	5/15/1999
H	Change format, change flow chart symbol to term per 12MRM96619A request	M.H LI	9/1/1999
J	Change sample size and QA gate method	Robert Wang	9/19/1999
K	Change Format	Robert Wang	4/10/2000
L	Change 24ape1n	Allan Li	6/9/2000
M	Change MCEL to BAT3	Lucy Bai	2/26/2001
N	change "per spec" to specific SPEC name chang QA gate to GATE	J.W Zhang	7/26/2001
P	Modify "Key contact/phone and Core team", Then change CA to ZH	J.W Zhang	11/30/2001
R	change file name to " SOIC and PDIP Test Flow " Modify "Key contact/phone and Core team"	H.L Sun	9/20/2002
S	Change test account from zh630 to ZH630/ZH660, adding packing in QA step, delete zh850	YuPeng Zhang/linda bo	5/22/2003
T	Adding " packing" in FOI gate	YuPeng Zhang/linda bo	6/6/2003
U	Changed the Part number, changed flow from INSP. To MAT, and QA to Gate, Deleted all 48A from control method	YuPeng Zhang/Wang Peng/Berts Li	4/5/2004
V	Modify the format;replace PROD with XFER in ZH650.adding "visual" in incoming check	Zhang Yupeng /Wang Peng	4/26/2004
W	Change sample size to 200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k) from 200 Units/Lot(Lot size<10k) or 315 Units(lot size>10k)	Zhang Yupeng /Wang Peng	5/13/2004
X	Change Core Team member from David zhang to Yang Liang	Yang Liang	9/13/2004

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REVISION HISTORY

Y	Change Process Description from TTT or Tape&Reel to Test Backend	Yang Liang	4/14/2005
Z	Change 'TTT or Tape&Reel' to 'Test Backend'	Yang Liang	4/19/2005
AA	Change Process No from ZH670 to ZH670/ZH720	Yang Liang	5/16/2005
AB	Added "V/M Sample Check" process in electrical test.	Wang Peng	9/9/2005
AC	Updated "Core Team Member" .	Wang Peng	10/25/2006
AD	1. Updated "Core Team Member" and revised some characteristics from process column to product column; 2. change 'VM sample check' to 'Machine Setup VM check' to clarify the VM check purpose on Electrical test process.	Wang Peng/Yang Liang	9/28/2007
AE	Change sample size to 200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k) from 200 Units/Lot(Lot size<10k) or 315 Units(lot size>10k)	Zhang Yupeng/ Wang Peng	5/13/2004
AF	1. Add '12MCT50040A' in control method and Reaction Plan column of INSP. step 2. Change Core Team name from 'Zhang Yupeng' to 'Yang Liang'	Yang Liang	9/21/2004
AG	1.Add "PQFN" in "Title,Part Number & Name/Description" 2.Add"Albert Zheng(6192)" in" Key Contact/Phone". 3.Change "SPS" to "Freescale" 4.Add "Yield" in "char.process of Electrical Test" 5.Delete "Electrical Test" in "char. Product" column. 6.Take place "200 units/Lot" with "200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k)" 7.Add "Electrical Parameter" in" char. Process" column 8.Add note of "F/T" and "ATE"	Wang Peng	11/30/2004
AH	Added "V/M Sample Check" process in electrical test.	Wang Peng	11/23/2005
AJ	Updated "Core Team Member" and "Supplier/Plant Name"	Wang Peng/Yang Liang	11/10/2006
AK	Updated "Core Team Member" and revised some characteristics from process column to product column; change 'VM sample check' to 'Machine Setup VM check' to clarify the VM check purpose on Electrical test process.	Wang Peng/Yang Liang	9/28/2007
AL	Delete the process description of B/I, Lot process & T/R from test process.	Wang Peng	4/15/2008
	1. Core Team Review 2. Update "Core Team Member" 3. Change title from "ZH630/ZH660 Test Flow" to "GENERAL TEST FLOW"		

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AM	4. Change part number from "ZH630/ZH660 Test Bank" to "GENERAL TEST" 5. Change description from "ZH630/ZH660 Test Bank Test Flow" to "GENERAL TEST FLOW" 6. Change incoming check sample size from "200 Units/Lot (Lot Size <10K) ;315 Units/Lot (Size>=10K)" to "200 Units/Lot (Lot Size =<10K) ;315 Units/Lot (Size>10K)" 7. Change start lot check sample size from "200 Units/Lot (Lot Size <10K) ;315 Units/Lot (Size>=10K)" to "200 Units/Lot (Lot Size =<10K) ;315 Units/Lot (Size>10K)" 8. Change machine setup & V/M check sample size from "200 Units/Lot (Lot Size <10K) ;315 Units/Lot (Size>=10K)" to "200 Units/Lot (Lot Size =<10K) ;315 Units/Lot (Size>10K)" 9. Change ILG sample size from "Per Skip Plan" to "Per 12ACT20080A" 10. Change VM gate sample size from "200 Units/Lot (Lot Size <10K) ;315 Units/Lot (Size>=10K)" to "200 Units/Lot (Lot Size =<10K) ;315 Units/Lot (Size>10K)"	Chen Wei/Yang Liang	5/5/2009
AN	12months review	Yang Liang/Chen Wei	5/4/2010
AP	12months review,no content change.	Yang Liang/Chen Wei	4/18/2011
AR	1. Add "ZHPT0" to process operation number 2. Change the reference of sample size to "Per 12ACT20080A" 3. Update the document numbers of "Specification", "Control Method" and "Control plan" acoording to Doc_Rebuild project 4. Change step name from "VM Gate (Per shop order)" to "VM Inspection", change the step symbol from "GATE" to "INSP" 5. For "VM Insepction" step, change the "Machine, Tools" and "Evaluation Measurement Technique" to "Visual" 6. Add NOTE 3	Yang Liang/Chen Wei	10/17/2011
AS	1. Remove Han Z.L from core team member; 2. Replace "A" with "Visual Mechanical Defect"; 3. Replace process specification of electrical test/gate process from "48A Spec" to "Test Program" / "Gate Program" 4. Replace "Test Program" & "Gate Program" Measurement to "Electrical Test"; 5. Replace gate process tool from "ILG" to "ATE"	Chen Wei/Yang Liang	12/9/2011

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REVISION HISTORY

AT	1. Update core team member 2. Split out "CENTRAL MATERIAL STAGING" step from "INCOMING CHECK" step, add detailed items into "INCOMING CHECK" step 3. Add detailed control method and reaction plan 4. Change freq. from "1x/lot" to "Every lot"	Chen Wei	9/21/2012
AU	Core team review: 1. Change the process name from "CENTRAL MATERIAL STAGING" to "MATERIAL RECEIVING" 2. Move "machine preparation" from "INCOMING CHECK" to "ELECTRICAL TEST" 3. Update the wording of Characteristics	Chen Wei/Yang Liang	11/9/2012
AV	1. Update Core team member 2. Update reaction plan	Chen Wei/Yang Liang	9/6/2013
AW	2013 annual control plan review, no content change.	Chen Wei/Yang Liang	11/25/2013

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Process Control Plan -- GENERAL TEST FLOW

Control Plan Number/Issue		Prototype / Pre-launch (XC) / Production	Key Contact/Phone	Date(Orig.)	Date (Rev.)
70MCT00019A/AW	X		Tang Peg (85686866)/Hu Z.J(85686770)	5/10/1997	11/25/2013

Part Number	Core Team	Customer Engineering Approval (If Req'd)
GENERAL TEST	Duan Peng, Chen Wei, Diao William, Liu X.J., Gao Dong, Yang Liang, Wang K.Q., Yin Wally, Xu Lingxuan.	

Name/Description	Supplier/Plant	Supplier Code	Customer Quality Approval/Date (If Req'd)
GENERAL TEST FLOW	FSL-TJN-FM		

FLOWCHART LEGEND

PROD=Production Operation **INSP**=Inspection **MEAS**=Measurement **QA**=QA Monitor **GATE**=QA Gate **XFER**=Material Transfer **MAT**=Material Inspection

Flow Chart Symbol	Process Operation Number	Process Name/Operation	Machine Device,Jip,Tools for Mfg	Characteristics		Special Char. Class	Product/Process /Specification /Tolerance	Evaluation Measurement Technique	Sample		Control Method	Reaction Plan
				Product	Process				Size	Freq.		
MAT	1	MATERIAL RECEIVING	Assembly Shop Order Packing list, SFC System		Documentation		12MCT50044C	Visual	100%	Every lot	Verify box label LOT#, device #, box quantity against packing list & SFC	Hold lot for disposition 12MCT50040A
PROD	2	INCOMING CHECK (Visual Mechanical only applies to assembly & BI rawstock)	Assembly Shop Order Test Shop Order SFC System		Quantity		12MCT50044C	Visual	100%	Every lot	Count physical quantity againest assembly shop order	Hold lot for disposition 12MCT50040A 12MCT50040A020 12MCT50040A021
					Documentation			Visual	100%	Every lot	Verify box label LOT#, device #, lot status in SFC system	
INSP			vision machine (optional)		Visual Mechanical		12MRM09116A	Visual or vision machine (optional)	Per 12ACT20080A	Every lot	Visual verification for visual defect	
PROD	3	ELECTRICAL TEST as per test shop order 1. Machine preparation 2. Start lot 3. Electrical parameters tests 4. End lot (Hot/Cold/Room)	Test Shop Order		Machine Type		12MCT50040A	Visual	100%	Every conversion	Manual visual verification machine according to test shop order	Hold for disposition 12MCT50040A
PROD			Test Shop Order		Temperature		Test Shop Order	Continuous Test Temperature monitoring	100%	Every test insertion	Handler temperature auto-guardbanding using temperature controller	Handler stop until temperature is within guardband
PROD			Test Shop Order SFC system		Yield (Start lot)		12MCT50040A 12MCT10240A	Electrical Test	Per 12ACT20080A	Every lot	Calculate the yield after sampling test done and compare with shut down yield	Stop the machine and call PE/TPE/PM. 12MCT50040A 12MCT10240A 12MCT50040A010 12MCT50040A012 12MCT50040A015 12MCT50040A018
INSP			vision machine (optional)		Visual Mechanical (Start lot)		12MRM09116A	Visual or vision machine (optional)	Per 12ACT20080A	Every lot	Visual verification for visual defect	Stop the machine and call supervisor. 12MCT50040A 12MCT50040A004 12MCT50040A010 12MCT50040A012 12MCT50040A015
PROD			ATE	Electrical Parameter			12MCT50040A	Electrical Test Program	100%	Every lot	Electrical Yield limit per SFC System	Stop the machine and call PE/TPE/PM. 12MCT50040A 12MCT50040A004 12MCT50040A010 12MCT50040A012 12MCT50040A015 12MCT50040A018
INSP			Vision machine (optional)		Visual Mechanical (In process)		12MRM09116A	Visual or vision machine (optional)	Per 12ACT20080A	Every lot	Visual verification for visual defect	Stop the machine and call supervisor. 12MCT50040A 12MCT50040A004 12MCT50040A010 12MCT50040A012 12MCT50040A015
					Yield (End lot)		12MCT50040A 12MCT10240A	Electrical Test	100%	Every lot	Electrical Yield limit per SFC System	Hold lot for disposition 12MCT10240A

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Process Control Plan -- GENERAL TEST FLOW

Control Plan Number/Issue		Prototype Pre-launch (XC) Production	Key Contact/Phone	Date(Orig.)	Date (Rev.)	
70MCT00019A/AW	**X**		**Tang Peg (85686866)/Hu Z.J(85686770)**	**5/10/1997**	**11/25/2013**	
Part Number **GENERAL TEST**		Core Team **Duan Peng, Chen Wei, Diao William, Liu X.J., Gao Dong, Yang Liang, Wang K.Q., Yin Wally, Xu Lingxuan.**		Customer Engineering Approval (If Req'd)		
Name/Description **GENERAL TEST FLOW**		Supplier/Plant **FSL-TJN-FM**	Supplier Code	Customer Quality Approval/Date (If Req'd)		

FLOWCHART LEGEND

PROD=Production Operation **INSP**=Inspection **MEAS**=Measurement **QA**=QA Monitor **GATE**=QA Gate **XFER**=Material Transfer **MAT**=Material Inspection

Flow Chart Symbol	Process Operation Number	Process Name/Operation	Machine Device,Jip,Tools for Mfg	Characteristics		Special Char. Class	Product/Process /Specification /Tolerance	Evaluation Measurement Technique	Sample		Control Method	Reaction Plan
				Product	Process				Size	Freq.		
PROD			Test Shop Order SFC system		Quantity		12MCT50040P	Visual	100%	Every lot	Count physical quantity and record on test shop order & SFC	Hold lot for disposition 12MCT50040A 12MCT50040A005 12MCT50040A019
					Documentation			Visual	100%	Every lot	Check test result againest physical quantity, confirm the lot status in SFC system	Hold lot for disposition 12MCT50040A
GATE	4	ELECTRICAL TEST (QC In-line) as per shop order (Hot/Room/Cold): Applicable for specific products as specified in the Test Shop Order or SFC system	ATE Test Shop Order SFC system	Electrical Parameter			12MCT50040A 12ACT20080A	Electrical Test Program	Per 12ACT20080A	Per Skip Plan	Accept on zero failure	Hold lot for disposition 12ACT20080A 12MCT50040A 12MCT50040A010 12MCT50040A012 12MCT50040A013 12MCT50040A015
					Quantity		12MCT50040P	Visual	100%	Every lot	Count physical quantity and record on test shop order & SFC	Hold lot for disposition 12MCT50040A 12MCT50040A005 12MCT50040A019
					Documentation			Visual	100%	Every lot	Check test result againest physical quantity, tranfer the lot to next step in SFC system	Hold lot for disposition 12MCT50040A
PROD	5	QUALITY CONTROL Stage: 1. Verification for test result 2. Visual inspection on final good unit			Quantity		12MCT10123G	Visual	100%	Every lot	Count physical quantity againset test shop order	Hold lot for disposition 12MCT50040A 12MCT50040A005 12MCT50040A019
					Documentation			Visual	100%	Every lot	Check test result againest test shop order, verify lot status in SFC system	Hold lot for disposition 12MCT50040A
INSP			Microscope(optional)		Visual Mechanical		12MRM09116A	Visual or Microscope(optional)	Per 12ACT20080A	Every lot	Visual verification for visual defect	Hold lot for disposition 12MCT50040A 12MCT50040A004

NOTE
1. ATE:Auto Testing Equipment
2. Visual: Unaided eye or 3x magnifier (optional)

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REVISION HISTORY

Part Number:	GENERAL TEST	Control Plan Number/Issue:	**70MCT00019A/AW**	
Name/Description:	GENERAL TEST FLOW	Control plan Date:	**5/10/1997**	(Orig.)
Supplier/Plant:	FSL-TJN-FM		**11/25/2013**	(Rev.)

Revision Date	Description of Revison & Writer	Spec Coord	Effectivity Date
O	VERSION O	J.W ZHANG	5/10/1997
A	CHANGE ERROR WORD	J.H ZHANG	12/14/1997
B	CHANGE CORE TEAM MEMBER	J.H ZHANG	3/3/1998
C	CHANG FORMAT	J.H ZHANG	5/10/1998
D	CHANG DOCUMENT TITLE	J.H ZHANG	6/6/1998
E	spelling mistake	J.H ZHANG	10/10/1998
F	Modify "Key contact/phone and Core team"	J.H ZHANG	12/20/1998
G	Change Format	J.H ZHANG	5/15/1999
H	Change format, change flow chart symbol to term per 12MRM96619A request	M.H LI	9/1/1999
J	Change sample size and QA gate method	Robert Wang	9/19/1999
K	Change Format	Robert Wang	4/10/2000
L	Change 24ape1n	Allan Li	6/9/2000
M	Change MCEL to BAT3	Lucy Bai	2/26/2001
N	change "per spec" to specific SPEC name chang QA gate to GATE	J.W Zhang	7/26/2001
P	Modify "Key contact/phone and Core team", Then change CA to ZH	J.W Zhang	11/30/2001
R	change file name to " SOIC and PDIP Test Flow " Modify "Key contact/phone and Core team"	H.L Sun	9/20/2002
S	Change test account from zh630 to ZH630/ZH660, adding packing in QA step, delete zh850	YuPeng Zhang/linda bo	5/22/2003
T	Adding " packing" in FOI gate	YuPeng Zhang/linda bo	6/6/2003
U	Changed the Part number, changed flow from INSP. To MAT, and QA to Gate, Deleted all 48A from control method	YuPeng Zhang/Wang Peng/Berts Li	4/5/2004
V	Modify the format;replace PROD with XFER in ZH650.adding "visual" in incoming check	Zhang Yupeng /Wang Peng	4/26/2004
W	Change sample size to 200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k) from 200 Units/Lot(Lot size<10k) or 315 Units(lot size>10k)	Zhang Yupeng /Wang Peng	5/13/2004
X	Change Core Team member from David zhang to Yang Liang	Yang Liang	9/13/2004

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REVISION HISTORY

Y	Change Process Description from TTT or Tape&Reel to Test Backend	Yang Liang	4/14/2005
Z	Change 'TTT or Tape&Reel' to 'Test Backend'	Yang Liang	4/19/2005
AA	Change Process No from ZH670 to ZH670/ZH720	Yang Liang	5/16/2005
AB	Added "V/M Sample Check" process in electrical test.	Wang Peng	9/9/2005
AC	Updated "Core Team Member" .	Wang Peng	10/25/2006
AD	1. Updated "Core Team Member" and revised some characteristics from process column to product column; 2. change 'VM sample check' to 'Machine Setup VM check' to clarify the VM check purpose on Electrical test process.	Wang Peng/Yang Liang	9/28/2007
AE	Change sample size to 200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k) from 200 Units/Lot(Lot size<10k) or 315 Units(lot size>10k)	Zhang Yupeng/ Wang Peng	5/13/2004
AF	1. Add ‘12MCT50040A’ in control method and Reaction Plan column of INSP. step 2. Change Core Team name from ‘Zhang Yupeng’ to ‘Yang Liang’	Yang Liang	9/21/2004
AG	1.Add "PQFN" in "Title,Part Number & Name/Description" 2.Add"Albert Zheng(6192)" in" Key Contact/Phone". 3.Change "SPS" to "Freescale" 4.Add "Yield" in "char.process of Electrical Test" 5.Delete "Electrical Test" in "char. Product" column. 6.Take place "200 units/Lot" with "200 Units/Lot(Lot size<10k) or 315 Units(lot size>=10k)" 7.Add "Electrical Parameter" in" char. Process" column 8.Add note of "F/T" and "ATE"	Wang Peng	11/30/2004
AH	Added "V/M Sample Check" process in electrical test.	Wang Peng	11/23/2005
AJ	Updated "Core Team Member" and "Supplier/Plant Name"	Wang Peng/Yang Liang	11/10/2006
AK	Updated "Core Team Member” and revised some characteristics from process column to product column; change 'VM sample check' to 'Machine Setup VM check' to clarify the VM check purpose on Electrical test process.	Wang Peng/Yang Liang	9/28/2007
AL	Delete the process description of B/I, Lot process & T/R from test process.	Wang Peng	4/15/2008
	1. Core Team Review 2. Update "Core Team Member" 3. Change title from "ZH630/ZH660 Test Flow" to "GENERAL TEST FLOW"		

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REVISION HISTORY

AM	4. Change part number from "ZH630/ZH660 Test Bank" to "GENERAL TEST" 5. Change description from "ZH630/ZH660 Test Bank Test Flow" to "GENERAL TEST FLOW" 6. Change incoming check sample size from "200 Units/Lot (Lot Size <10K) ;315 Units/Lot (Size>=10K)" to "200 Units/Lot (Lot Size =<10K) ;315 Units/Lot (Size>10K)" 7. Change start lot check sample size from "200 Units/Lot (Lot Size <10K) ;315 Units/Lot (Size>=10K)" to "200 Units/Lot (Lot Size =<10K) ;315 Units/Lot (Size>10K)" 8. Change machine setup & V/M check sample size from "200 Units/Lot (Lot Size <10K) ;315 Units/Lot (Size>=10K)" to "200 Units/Lot (Lot Size =<10K) ;315 Units/Lot (Size>10K)" 9. Change ILG sample size from "Per Skip Plan" to "Per 12ACT20080A" 10. Change VM gate sample size from "200 Units/Lot (Lot Size <10K) ;315 Units/Lot (Size>=10K)" to "200 Units/Lot (Lot Size =<10K) ;315 Units/Lot (Size>10K)"	Chen Wei/Yang Liang	5/5/2009
AN	12months review	Yang Liang/Chen Wei	5/4/2010
AP	12months review,no content change.	Yang Liang/Chen Wei	4/18/2011
AR	1. Add "ZHPT0" to process operation number 2. Change the reference of sample size to "Per 12ACT20080A" 3. Update the document numbers of "Specification", "Control Method" and "Control plan" acoording to Doc_Rebuild project 4. Change step name from "VM Gate (Per shop order)" to "VM Inspection", change the step symbol from "GATE" to "INSP" 5. For "VM Insepction" step, change the "Machine, Tools" and "Evaluation Measurement Technique" to "Visual" 6. Add NOTE 3	Yang Liang/Chen Wei	10/17/2011
AS	1. Remove Han Z.L from core team member; 2. Replace "A" with "Visual Mechanical Defect"; 3. Replace process specification of electrical test/gate process from "48A Spec" to "Test Program" / "Gate Program" 4. Replace "Test Program" & "Gate Program" Measurement to "Electrical Test"; 5. Replace gate process tool from "ILG" to "ATE"	Chen Wei/Yang Liang	12/9/2011

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REVISION HISTORY

AT	1. Update core team member 2. Split out "CENTRAL MATERIAL STAGING" step from "INCOMING CHECK" step, add detailed items into "INCOMING CHECK" step 3. Add detailed control method and reaction plan 4. Change freq. from "1x/lot" to "Every lot"	Chen Wei	9/21/2012
AU	Core team review: 1. Change the process name from "CENTRAL MATERIAL STAGING" to "MATERIAL RECEIVING" 2. Move "machine preparation" from "INCOMING CHECK" to "ELECTRICAL TEST" 3. Update the wording of Characteristics	Chen Wei/Yang Liang	11/9/2012
AV	1. Update Core team member 2. Update reaction plan	Chen Wei/Yang Liang	9/6/2013
AW	2013 annual control plan review, no content change.	Chen Wei/Yang Liang	11/25/2013

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Measurement System Studies (Gage R&R)

TSMC PPAP Documents

• TSMC PPAP documents (FMEAs, Control Plans, Cpks, and GR&R) are considered proprietary information by TSMC, classified as "TSMC INTERNAL USE ONLY" and cannot be distributed with Freescale PPAPs in accordance with an agreement with TSMC.

• The PPAP documents are pulled by Freescale External Manufacturing Quality and checked for compliance with TS16949 requirements.

• For special requests, Freescale may be able to review these documents on a limited basis with customers at the local Freescale sales office.

• If there are any questions, please contact:

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Gage Study Summary Report

Customer Part Number:		
Company/Manufacturing Site ID: Freescale / TJN		
Designate only one of the following and enter the appropriate information:		
☐ **Wafer Fab Process Technology:**		
☒ **Assembly Process Package Family:**	SOIC32LD	
☐ **Physical Dimensions Package Drawing #:**	98ASA00259D_O 98ARH99137A_B	
☐ **Test**		

Special/Important Characteristic	Measurement Gage/Tool/Equipment	%R&R 1/	Date Study Performed
Wire Pull	Wire pull tester – Dage4000 BBT-01	0.30%	May 11,2013
Ball Shear	Ball Shear tester – Dage4000 BBT-01	0.12%	May 11,2013
Plating Thickness	SFT3200 32300018	3.50%	Mar 05,2013
Tip-to-Tip	Projector - Nikon V-12BDC MPJ-03	0.21%	May 09, 2013
Coplanarity	Microscope- Nikon- MM-40 MMP-02	8.34%	May 09, 2013

1/ If R&R > 10%, attach containment action, corrective action, or justification (as appropriate)

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Dimensional Results

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PHYSICAL DIMENSION MEASUREMENT RESULT

Package Type: SOIC 32ld EP
Assembly Site: Freescale TJN
Freescale 98A: 98ASA00259D **98A Rev:** O **98A Rev Date:** 29-Jul-10
Date of Test Results: 16-Dec-13

Package Dimensions per Freescale 98A (example length, width, etc.)

Dimension Description		Package width	Package length	Package height	Tip to Tip	Full height	Lead width	Lead lenth	Exposed Pad, X	Exposed Pad, Y	Coplanarity
Spec Limits	Min Per Freescale 98A	7.40	10.90	2.12	10.00	2.22	0.22	0.50	4.00	4.00	0.00
Spec Limits	Max Per Freescale 98A	7.60	11.10	2.45	10.60	2.45	0.38	0.90	5.20	5.20	0.10
Enter the measured value for each dimension per unit from 3 assembly lots											
Assembly Lot #	Unit #										
	1	7.536	11.017	2.276	10.298	2.337	0.328	0.668	4.484	4.487	0.016
	2	7.530	11.030	2.292	10.295	2.392	0.324	0.638	4.462	4.495	0.023
	3	7.547	11.026	2.303	10.294	2.350	0.326	0.667	4.488	4.448	0.014
	4	7.544	11.013	2.298	10.305	2.336	0.326	0.650	4.492	4.508	0.011
	5	7.542	11.006	2.292	10.300	2.334	0.332	0.647	4.480	4.485	0.020
	6	7.549	11.012	2.300	10.307	2.355	0.328	0.664	4.482	4.493	0.020
	7	7.540	11.018	2.286	10.294	2.354	0.325	0.663	4.478	4.488	0.018
	8	7.539	11.008	2.299	10.297	2.360	0.331	0.662	4.475	4.473	0.009
	9	7.540	11.011	2.300	10.300	2.364	0.329	0.665	4.481	4.485	0.011
	10	7.536	11.016	2.303	10.303	2.350	0.326	0.649	4.490	4.500	0.017
Assembly Lot #	Unit #										
	1	7.544	11.011	2.295	10.294	2.339	0.328	0.668	4.484	4.487	0.016
	2	7.540	11.009	2.293	10.298	2.354	0.324	0.638	4.462	4.495	0.023
	3	7.539	11.020	2.301	10.302	2.337	0.326	0.667	4.488	4.448	0.014
	4	7.539	11.018	2.291	10.295	2.350	0.326	0.650	4.492	4.508	0.011
	5	7.542	11.009	2.296	10.298	2.336	0.332	0.647	4.480	4.485	0.020
	6	7.540	11.012	2.288	10.300	2.351	0.328	0.664	4.482	4.493	0.020
	7	7.539	11.018	2.292	10.300	2.358	0.325	0.663	4.478	4.488	0.018
	8	7.549	11.016	2.303	10.296	2.339	0.331	0.662	4.475	4.473	0.009
	9	7.544	11.010	2.294	10.294	2.362	0.329	0.665	4.481	4.485	0.011
	10	7.543	11.015	2.300	10.298	2.358	0.326	0.649	4.490	4.500	0.017
Lot #	Unit #										
	1	7.539	11.021	2.299	10.303	2.356	0.328	0.668	4.484	4.487	0.016
	2	7.539	11.019	2.298	10.301	2.344	0.324	0.638	4.462	4.495	0.023
	3	7.545	11.013	2.288	10.300	2.359	0.326	0.667	4.488	4.448	0.014
	4	7.536	11.015	2.304	10.296	2.353	0.326	0.650	4.492	4.508	0.011
	5	7.543	11.009	2.300	10.294	2.339	0.332	0.647	4.480	4.485	0.020
	6	7.546	11.012	2.282	10.302	2.332	0.328	0.664	4.482	4.493	0.020
	7	7.540	11.018	2.293	10.292	2.361	0.325	0.663	4.478	4.488	0.018
	8	7.540	11.011	2.298	10.297	2.355	0.331	0.662	4.475	4.473	0.009
	9	7.542	11.011	2.296	10.298	2.380	0.329	0.665	4.481	4.485	0.011
	10	7.545	11.016	2.301	10.300	2.356	0.326	0.649	4.490	4.500	0.017
Calculate the following for each dimension											
	MIN	7.530	11.006	2.276	10.292	2.332	0.324	0.638	4.462	4.448	0.009
	MAX	7.549	11.030	2.304	10.307	2.392	0.332	0.668	4.492	4.508	0.023
	AVERAGE	7.541	11.015	2.295	10.298	2.352	0.328	0.657	4.481	4.486	0.016
	STDEV	0.004	0.005	0.007	0.004	0.013	0.003	0.010	0.008	0.016	0.004
	WITHIN LIMIT	TRUE	TRUE	TRUE	TRUE	TRUE	TRUE	TRUE	TRUE	TRUE	TRUE
	Cp	8.16	6.25	8.33	27.45	2.86	10.66	6.66	24.07	12.62	3.81
	Cpk	4.80	5.33	7.81	27.30	2.44	7.00	5.24	19.30	10.22	6.41

1/ If Ppk < 1.67 or Cpk < 1.67 attach justification

Material, Performance Test Results

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AUTOMOTIVE PRODUCT AEC-Q100G Qualification Test Plan

Objective: Qualification of TSMC Fab SOIC32 4.6EP Cu Wire (G630AY MC)

Qual Vehicle PN: **MC33972ATEK/R2** Qual Vehicle Name:: **MSDISWA(EP)**	Customer Name(s): **General Market** PN(s):	Test Program ID: VARIOUS Test Program Rev: Rel. Circuits Doc. #:	Report Type: QUAL PLAN Revision #: 19Aug13 Date:
Technology: **SM5AP** Package Description: **SOIC 32 300ML 4.6EP**	Mask set#: **N39B** Revision #:	CAB #: 13342133M FSL Qual Quartz Tracking #:	Rel. Engr. Approval Tian Meng Signature: 19Aug13 Date:
Fab site: **TSMC-Fab** Assembly site: **FSL-TJN-FM** Final Test site: **FSL-TJN-FM** Rel Test site:	Product Engr: **Wang Brenda** Packaging Engr: **Hosoda Daisuke** Reliability Engr: **Tian Meng**	Target Dates NA Test Start: Test Finish: PPAP target date:	CAB Approval Yanil Cruz Signature: August 22 2013 Date:
Die Size (in mm) **3.857x2.831** W x L x T	Part Operating **-40 to 125** Temp. Range: AEC Grade:	Freescale Contact: Bai Yun Phone Number: +86-85684236	Customer Approval Signature: Date:

Stress	JEDEC22 Reference	Test Conditions	End Point Requirements	Minimum Sample Size per lot	# of Lots	Total Units including spares	Results: Lot A nominal	Lot B nominal	Lot C nominal	Lot D HH	Lot E LL	Comments (Generic Data: Note 2)
PRE-STRESS REQUIREMENTS/OPTIONS												
PC	A113 J-STD-020	**Preconditioning (PC)** MSL 3 at 260℃, +5/-0℃ CSAM: Note 3	TEST at RH (add C if PC before HTOL); CSAM	All surface mount devices prior to THB/HAST, AC/UHST, TC, PC+PTC, or as required per								PC is performed and results reported as part of the individual stress tests.
GROUP A - ACCELERATED ENVIRONMENTAL STRESS TESTS												
HAST	A110	**Highly Accelerated Stress Test (HAST):** PC before HAST if required. HAST = 110℃/85%RH for 264hrs,528hrs FIO Bias: per HAST schematic *Timed RO of 48hrs. MAX*	TEST @ RH; CSAM	77	5	400						When biased humidity is required either HAST or THB can be performed. ***HAST is the preferred biased humidity test.***
UHST	A118	**Unbiased HAST (UHST):** PC before UHST if required. UHST = 110℃/85%RH for 264hrs,528hrs FIO *Timed RO of 48hrs. MAX*	TEST @ R; CSAM	77	5	400						***When unbaised humidity testing is required, UHST is the preferred unbiased humidity test. The AC option is NOT recommended.***
TC	A104 AEC Q100-Appendix 3	**Temperature Cycle (TC):** PC before TC if required. TC = -50℃ to 150℃ for 1000 cycles,2000cycles FIO WBP after qual readpoint on 5 devices from each lot; 2 bonds per corner and one mid-bond per side on each device. Record which pins were used.	TEST @ H WBP =/> 3 grams CSAM	77	5	400						If WP is to be performed at interim readpoints, add additional samples so that the minimum sample size is maintained for the final readpoint.
HTSL	A103	**High Temperature Storage Life (HTSL):** HTSL **=** 150℃ for 1008 hrs,2016hrs FIO *Timed RO = 96hrs. MAX*	TEST @ RH	45	3	144						
TEST GROUP B - ACCELERATED LIFETIME SIMULATION TESTS												
HTOL	A108	**High Temperature Operating Life (HTOL):** HTOL = 100℃ for 1008 hrs,2016hrs FIO Bias:5V and 28V *Timed RO of 96hrs. MAX*	TEST @ RHC;	77	3	240						***Perform HTOL on two lots and reuse third lot from Cosslite TSMC***
ELFR	AEC Q100-008	**Early Life Failure Rate ELFR):** ELFR = 100℃ for 48 hrs; *Timed RO of 48 hrs MAX*	TEST @ RH	800	3	2409						***Perform ELFR on two lots and reuse third lot from Cosslite TSMC***
TEST GROUP C - PACKAGE ASSEMBLY INTEGRITY TESTS												
Full Assy. CZ + Cu WB Cz	FSL Internal Requirement	Full assembly process CZ Data collection per FSL CZ template (for Cu WB) for 3 tech cert lots with nominal Cu WB process. Perform Wire Bond CZ specifically for Copper Wire for 1 HH and 1 LLTech Cert lots.			5							
WBS	AEC Q100-001	**Wire Bond shear (WBS)**	Cpk = or > 1.67	30 bonds from minimum 5 units	3	15						Performed by Assembly Site during qual lot builds - PE to include this requirement in the qual lot build ERF.

WBP	MilStd883-2011	**Wire Bond Pull (WBP):** Cond. C or D	Cpk = or > 1.67	30 bonds from minimum 5 units	3	15						Performed by Assembly Site during qual lot builds - PE to include this requirement in the qual lot build ERF
TEST GROUP D - DIE FABRICATION RELIABILITY TESTS												
TEST GROUP E - ELECTRICAL VERIFICATION TESTS												
TEST	Freescale 48A	**Pre- and Post Functional / Parametrics (TEST):** Test software shall meet requirements of AEC-Q100-007. Testing performed to the limits of device specification in temperature and limit value.	0 Fails	All	All	All						TEST results is shown for each individual stress test in the qual results report generated upon qual completion. FSL SQA release required for qual test program.
ED	AEC-Q100-009, Freescale 48A spec	**Electrical Distribution (ED)**	TEST @ RHC Cpk = or > 1.67	30	3	90						

General Notes:
Generic Data Reference List:
Notes:This Data will be used to qualify the following devices:

AUTOMOTIVE PRODUCT AEC-Q100G Qualification Test Result

Objective: **Qualification of TSMC Fab SOIC32 4.6EP Cu Wire (G630AY MC)**

Qual Vehicle PN:	**MC33972ATEK/R2**	Customer Name(s):	**General Market**	Test Program ID:	VARIOUS	Report Type:	QUALRESULT
Qual Vehicle Name::	**MSDISWA(EP)**	PN(s):		Test Program Rev:		Revision #:	28Oct2013
				Rel. Circuits Doc. #:		Date:	
Technology:	**SM5AP**	Mask set#:	**N39B**	CAB #:	13342133M	Rel. Engr. Approval	Tian Meng
Package Description:	**SOIC 32 300ML 4.6EP**	Revision #:		FSL Qual Quartz	222708 G630AY	Signature:	28Oct2013
				Tracking #:		Date:	
Fab site:	**TSMC-Fab**	Product Engr:	**Wang Brenda**	Target Dates	NA	CAB Approval	Yanil Cruz
Assembly site:	**FSL-TJN-FM**	Packaging Engr:	**Hosoda Daisuke**	Test Start:		Signature:	07NOV2013
Final Test site:	**FSL-TJN-FM**	Reliability Engr:	**Tian Meng**	Test Finish:		Date:	
Rel Test site:				PPAP target date:			
Die Size (in mm) W x L x T	**3.857x2.831**	Part Operating Temp. Range: AEC Grade:	**-40 to 125**	Freescale Contact:	Bai Yun	Customer Approval	
				Phone Number:	+86-85684236	Signature:	
						Date:	

Stress	JEDEC22 Reference	Test Conditions	End Point Requirements	Minimum Sample Size per lot	# of Lots	Total Units including spares	Lot A nominal	Lot B nominal	Lot C nominal	Lot D HH	Lot E LL	Comments (Generic Data: Note 2)
PRE-STRESS REQUIREMENTS/OPTIONS												
PC	A113 J-STD-020	**Preconditioning (PC)** MSL 3 at 260℃, +5/-0℃ CSAM: Note 3	TEST at RH (add C if PC before HTOL); CSAM	All surface mount devices prior to THB/HAST, AC/UHST, TC, PC+PTC, or as required per								PC is performed and results reported as part of the individual stress tests.
GROUP A - ACCELERATED ENVIRONMENTAL STRESS TESTS												
HAST	A110	**Highly Accelerated Stress Test (HAST):** PC before HAST if required. HAST = 110℃/85%RH for 264hrs,528hrs FIO Bias: per HAST schematic *Timed RO of 48hrs. MAX*	TEST @ RH; CSAM	77	5	400	Reuse Cosslite Data 264hrs: 0/80 528hrs: 0/80	Reuse Cosslite Data 264hrs: 0/80 528hrs: 0/80	Reuse Cosslite Data 264hrs: 0/80 528hrs: 0/80	Reuse Cosslite Data 264hrs: 0/80 528hrs: 0/80	Reuse Cosslite Data 264hrs: 0/80 528hrs: 0/80	When biased humidity is required either HAST or THB can be performed. ***HAST is the preferred biased humidity test.***
UHST	A118	**Unbiased HAST (UHST):** PC before UHST if required. UHST = 110℃/85%RH for 264hrs,528hrs FIO *Timed RO of 48hrs. MAX*	TEST @ R; CSAM	77	5	400	264hrs: 0/80 528hrs: 0/80	Reuse Cosslite Data 96hrs: 0/80 192hrs: 0/80	Reuse Cosslite Data 96hrs: 0/80 192hrs: 0/80	264hrs: 0/80 528hrs: 0/80	264hrs: 0/80 528hrs: 0/80	***When unbaised humidity testing is required, UHST is the preferred unbiased humidity test. The AC option is NOT recommended.***
TC	A104 AEC Q100-Appendix 3	**Temperature Cycle (TC):** PC before TC if required. TC = -50℃ to 150℃ for 1000 cycles,2000cycles FIO WBP after qual readpoint on 5 devices from each lot; 2 bonds per corner and one mid-bond per side on each device. Record which pins were used	TEST @ H WBP =/> 3 grams CSAM	77	5	400	1000cyc: 0/80 2000cyc: 0/80 WP pass	Reuse Cosslite Data 1000cyc: 0/80 2000cyc: 0/80 WP pass	Reuse Cosslite Data 1000cyc: 0/80 2000cyc: 0/80 WP pass	1000cyc: 0/80 2000cyc: 0/80 WP pass	1000cyc: 0/80 2000cyc: 0/80 WP pass	If WP is to be performed at interim readpoints, add additional samples so that the minimum sample size is maintained for the final readpoint.
HTSL	A103	**High Temperature Storage Life (HTSL):** HTSL = 150℃ for 1008 hrs,2016hrs FIO *Timed RO = 96hrs. MAX*	TEST @ RH	45	3	144	1008hrs: 0/48 2016hrs: 0/48			Reuse Cosslite Data 1008hrs: 0/48 2016hrs: 0/48	Reuse Cosslite Data 1008hrs: 0/48 2016hrs: 0/48	
TEST GROUP B - ACCELERATED LIFETIME SIMULATION TESTS												
HTOL	A108	**High Temperature Operating Life (HTOL):** HTOL = 100℃ for 1008 hrs,2016hrs FIO Bias:5V and 28V *Timed RO of 96hrs. MAX*	TEST @ RHC;	77	3	240	1008hrs: 0/80 2016hrs: 0/80	Reuse Cosslite data 1008hrs: 0/80 2016hrs: 0/80			1008hrs: 0/80 2016hrs: 0/80	***Perform HTOL on two lots and reuse third lot from Cosslite TSMC***
ELFR	AEC Q100-008	**Early Life Failure Rate ELFR):** ELFR = 100℃ for 48 hrs; *Timed RO of 48 hrs MAX*	TEST @ RH	800	3	2409	0/803	0/803	Reuse Cosslite data 0/803			***Perform ELFR on two lots and reuse third lot from Cosslite TSMC***
TEST GROUP C - PACKAGE ASSEMBLY INTEGRITY TESTS												
Full Assy. CZ + Cu WB Cz	FSL Internal Requirement	Full assembly process CZ Data collection per FSL CZ template (for Cu WB) for 3 tech cert lots with nominal Cu WB process. Perform Wire Bond CZ specifically for Copper Wire for 1 HH and 1 LLTech Cert lots.			5		Pass	Pass	Pass	Pass	Pass	
WBS	AEC Q100-001	**Wire Bond shear (WBS)**	Cpk = or > 1.67	30 bonds from minimum 5 units	3	25	Pass			Pass	Pass	Performed by Assembly Site during qual lot builds - PE to include this requirement in the qual lot build ERF.
WBP	MilStd883-2011	**Wire Bond Pull (WBP):** Cond. C or D	Cpk = or > 1.67	30 bonds from minimum 5 units	3	25	Pass			Pass	Pass	Performed by Assembly Site during qual lot builds - PE to include this requirement in the qual lot build ERF
TEST GROUP D - DIE FABRICATION RELIABILITY TESTS												
TEST GROUP E - ELECTRICAL VERIFICATION TESTS												
TEST	Freescale 48A	**Pre- and Post Functional / Parametrics (TEST):** Test software shall meet requirements of AEC-Q100-007. Testing performed to the limits of device specification in temperature and limit value.	0 Fails	All	All	All						TEST results is shown for each individual stress test in the qual results report generated upon qual completion. FSL SQA release required for qual test program
ED	AEC-Q100-009, Freescale 48A spec	**Electrical Distribution (ED)**	TEST @ RHC Cpk = or > 1.67	30	3	90	Pass	Pass	Pass			

PRODUCT AND PROCESS CHANGE NOTIFICATION

Generic Copy

ISSUE DATE: 12-Dec-2013
NOTIFICATION: 15977
TITLE: SOIC32 300ML 4.6EP/Non-EP TSMC SMOS5 Copper Wire Qualification
EFFECTIVE DATE: 12-Mar-2014

DEVICE(S)

MPN
MC33972ATEK
MC33972ATEKR2
MC33972ATEW
MC33972ATEWR2
MC33972TEW
MC33972TEWR2
MC33975ATEK
MC33975ATEKR2
MC33975TEK
MC33975TEKR2
MC34972ATEK
MC34972ATEKR2
MC34972ATEW
MC34972ATEWR2
MC34975ATEK
MC34975ATEKR2

AFFECTED CHANGE CATEGORIES

- BILL OF MATERIAL CHANGE (SAME ASSEMBLY SITE)

DESCRIPTION OF CHANGE

Freescale Semiconductor announces the addition of Copper Wire as a wirebond material and Sumitomo EME-G630AY Molding Compound as mold material for SMOS5 SOIC32 300ML 4.6EP and Non-EP package devices displayed in this notification. These products were previously assembled with Gold (Au) wire and Hitachi CEL9220HF13 mold compound at Freescale TJN assembly site, Tianjin, China. These products are now qualified for assembly with Copper (Cu) wire and EME-G630AY mold compound at Freescale TJN assembly site, Tianjin, China.

Sample Parts Available:
KC33972ATEK/R2
KC33972ATEW/R2
KC33975TEK/R2
KC33975ATEK/R2

REASON FOR CHANGE

The transfer from Gold to Copper wire and CEL9220HF13 to EME-G630AY mold compound are required to mitigate against raw material cost increases and for supply assurance.

ANTICIPATED IMPACT OF PRODUCT CHANGE(FORM, FIT, FUNCTION, OR RELIABILITY)

Freescale Confidential Proprietary

No change to form, fit or function. Reliability is equivalent or improved.

Freescale will consider specific conditions of acceptance of this change submitted within 30 days of receipt of this notice on a case by case basis. To request further data or inquire about the notification, please enter a Service Request.
For sample inquiries - please go to http://freescale.com/

QUAL DATA AVAILABILITY DATE: 29-Nov-2013

QUALIFICATION STATUS: COMPLETED

QUALIFICATION PLAN:

See attached qualification results.

RELIABILITY DATA SUMMARY:

See attached qualification results.

ELECTRICAL CHARACTERISTIC SUMMARY:

No change to datasheet. No change to Electrical Distributions.

CHANGED PART IDENTIFICATION:

There is no change to orderable part number. The Tracecode marking on the device includes assembly site and datecode. Freescale will have traceability by assembly site and datecode.

NOTIFICATION CONTACT:

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NPI CONTACT:

Name:	MENG TIAN
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SAMPLE AVAILABILITY DATE: 17-Dec-2013

ATTACHMENT(S):
External attachment(s) for this notification can be viewed at:
15977_Analog_Cu_Wire_SOIC_Mold_Compound_Change_GPCN.pdf
15977_MSDISW_Copper_Wire_G630AY_Electrical_Distribution_GPCN.pdf
15977_SOIC_MSDI_Family_Copper_Wire_with_G630AY_MC_Qual_Results_GPCN.pdf

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Freescale Confidential Proprietary

Electrical Distribution Report

						Lot1				Lot2				Lot3			
Test#	Test Name	Lo Limit	Hi Limit	Unit	Temp	Mean	Std Dev	Cp	Cpk	Mean	Std Dev	Cp	Cpk	Mean	Std Dev	Cp	Cpk
2	IPWR on @ 8v	0	4	mA	HT	2.82	0.02	36.96	21.86	2.82	0.02	36.36	21.44	2.82	0.02	38.92	22.95
2	IPWR on @ 8v	0	4	mA	RT	2.86	0.02	37.81	21.52	2.86	0.02	35.78	20.37	2.86	0.02	28.98	16.45
2	IPWR on @ 8v	0	4	mA	CT	2.85	0.02	26.79	15.39	2.85	0.02	27.27	15.74	2.85	0.03	22.78	13.08
3	IPWR on @ 16v	0	4	mA	HT	3.18	0.02	31.73	12.93	3.19	0.02	31.92	12.88	3.19	0.02	50.30	13.56
3	IPWR on @ 16v	0	4	mA	RT	3.23	0.02	34.19	13.18	3.23	0.02	31.96	12.25	3.24	0.03	25.52	9.76
3	IPWR on @ 16v	0	4	mA	CT	3.18	0.03	24.57	10.11	3.18	0.03	25.96	10.70	3.18	0.03	20.30	8.31
4	IPWR ss	40	100	uA	HT	80.15	0.74	13.43	8.88	81.22	0.78	12.89	8.07	80.43	0.56	17.78	11.60
4	IPWR ss	40	100	uA	RT	79.74	0.54	18.68	12.62	80.49	0.76	13.09	8.51	80.03	0.47	21.14	14.07
4	IPWR ss	40	100	uA	CT	75.27	0.78	12.87	10.61	75.93	0.72	13.93	11.17	75.45	0.58	17.26	14.12
5	IDD ss	-20	20	uA	HT	12.09	0.21	15.65	12.38	12.25	0.20	16.70	12.94	12.14	0.24	13.81	10.86
5	IDD ss	-20	20	uA	RT	12.45	0.28	11.78	8.90	12.58	0.26	12.62	9.37	12.46	0.30	11.28	8.50
5	IDD ss	-20	20	uA	CT	11.29	0.29	11.33	9.87	11.40	0.30	11.13	9.57	11.34	0.35	9.41	8.15
8	IDD @ 5vdd	-500	500	uA	HT	37.29	0.72	116.17	17.33	37.37	0.58	144.83	21.65	37.16	0.70	118.80	17.66
8	IDD @ 5vdd	-500	500	uA	RT	55.36	1.03	80.76	17.88	55.39	0.91	92.00	20.38	55.17	1.04	80.35	17.73
8	IDD @ 5vdd	-500	500	uA	CT	76.83	1.67	49.86	15.32	76.54	1.34	62.33	19.08	76.32	1.66	50.08	15.29
9	SP0 iwetting batt = 28v	12	18	mA	HT	16.32	0.16	6.26	3.50	16.32	0.16	6.20	3.46	16.36	0.14	3.65	3.30
9	SP0 iwetting batt = 28v	12	18	mA	RT	16.22	0.16	6.38	3.78	16.20	0.16	6.31	3.78	16.24	0.17	5.97	3.49
9	SP0 iwetting batt = 28v	12	18	mA	CT	15.98	0.18	5.49	3.70	15.94	0.19	3.56	3.46	16.01	0.21	4.76	3.16
10	SP1 iwetting batt 268v	12	18	mA	HT	16.34	0.15	6.54	3.62	16.33	0.15	6.63	3.70	16.38	0.13	3.76	3.46
10	SP1 iwetting batt 268v	12	18	mA	RT	16.28	0.16	6.31	3.62	16.25	0.14	4.20	4.19	16.29	0.15	6.73	3.82
10	SP1 iwetting batt 268v	12	18	mA	CT	16.08	0.19	5.19	3.32	16.03	0.16	4.07	4.01	16.11	0.20	3.37	3.19
11	SP2 iwetting batt 28v	12	18	mA	HT	16.36	0.15	6.61	3.62	16.37	0.17	6.02	3.27	16.40	0.14	3.67	3.42
11	SP2 iwetting batt 28v	12	18	mA	RT	16.31	0.14	6.94	3.92	16.30	0.16	3.66	3.56	16.33	0.16	6.24	3.48
11	SP2 iwetting batt 28v	12	18	mA	CT	16.13	0.18	5.50	3.43	16.09	0.18	3.67	3.51	16.14	0.20	3.26	3.02
12	SP3 iwetting batt 28v	12	18	mA	HT	16.30	0.15	6.62	3.75	16.30	0.16	6.28	3.57	16.34	0.12	4.26	3.81
12	SP3 iwetting batt 28v	12	18	mA	RT	16.25	0.15	6.51	3.79	16.23	0.13	4.45	4.40	16.27	0.13	7.59	4.37
12	SP3 iwetting batt 28v	12	18	mA	CT	16.07	0.18	5.52	3.55	16.01	0.17	3.92	3.91	16.09	0.19	3.58	3.41
13	SP4 iwetting batt = 28v	12	18	mA	HT	16.29	0.16	6.42	3.66	16.27	0.15	6.73	3.87	16.33	0.12	4.03	3.56
13	SP4 iwetting batt = 28v	12	18	mA	RT	16.21	0.15	6.53	3.91	16.15	0.13	4.35	4.10	16.21	0.15	6.83	4.08
13	SP4 iwetting batt = 28v	12	18	mA	CT	15.98	0.18	5.67	3.82	15.90	0.16	4.29	4.06	15.99	0.20	3.36	3.34
14	SP5 iwetting batt = 28v	12	18	mA	HT	16.30	0.16	6.11	3.47	16.32	0.15	6.63	3.71	16.35	0.13	3.76	3.39
14	SP5 iwetting batt = 28v	12	18	mA	RT	16.24	0.16	6.19	3.63	16.24	0.14	4.12	4.09	16.28	0.15	6.46	3.71
14	SP5 iwetting batt = 28v	12	18	mA	CT	16.04	0.20	5.07	3.31	16.02	0.17	4.00	3.96	16.08	0.21	3.22	3.09
15	SP6 iwetting batt = 28v	12	18	mA	HT	16.33	0.15	6.88	3.83	16.34	0.16	6.45	3.58	16.38	0.14	3.49	3.20
15	SP6 iwetting batt = 28v	12	18	mA	RT	16.28	0.13	7.46	4.27	16.26	0.14	4.12	4.11	16.30	0.16	6.28	3.55
15	SP6 iwetting batt = 28v	12	18	mA	CT	16.11	0.16	6.16	3.89	16.04	0.18	3.67	3.59	16.12	0.21	3.23	3.03
16	SP7 iwetting batt = 28v	12	18	mA	HT	16.27	0.14	7.20	4.15	16.28	0.15	6.46	3.70	16.31	0.14	3.62	3.16
16	SP7 iwetting batt = 28v	12	18	mA	RT	16.21	0.13	7.44	4.45	16.19	0.16	3.72	3.58	16.22	0.16	6.33	3.75
16	SP7 iwetting batt = 28v	12	18	mA	CT	16.01	0.16	6.19	4.10	15.97	0.19	3.51	3.45	16.03	0.21	3.24	3.19
17	SP0 iwetting gnd vbatt=28v	-18	-12	mA	HT	-16.06	0.12	8.07	5.22	-16.09	0.17	6.02	3.83	-16.11	0.12	5.42	5.24
17	SP0 iwetting gnd vbatt=28v	-18	-12	mA	RT	-16.13	0.12	8.11	5.05	-16.12	0.17	3.85	3.70	-16.18	0.14	4.60	4.28
17	SP0 iwetting gnd vbatt=28v	-18	-12	mA	CT	-15.86	0.16	6.11	4.35	-15.83	0.18	5.44	3.93	-15.91	0.17	5.98	4.17
18	SP1 iwetting gnd vbatt=28v	-18	-12	mA	HT	-16.02	0.13	7.49	4.95	-16.04	0.15	4.38	4.34	-16.08	0.13	5.19	5.12
18	SP1 iwetting gnd vbatt=28v	-18	-12	mA	RT	-16.10	0.14	7.29	4.61	-16.07	0.14	4.64	4.59	-16.13	0.13	4.91	4.69
18	SP1 iwetting gnd vbatt=28v	-18	-12	mA	CT	-15.82	0.17	5.78	4.19	-15.77	0.16	6.10	4.53	-15.85	0.16	6.28	4.50
19	SP2 iwetting gnd vbatt=28v	-18	-12	mA	HT	-16.02	0.14	7.08	4.66	-16.05	0.16	4.18	4.18	-16.07	0.12	5.57	5.52
19	SP2 iwetting gnd vbatt=28v	-18	-12	mA	RT	-16.10	0.14	7.26	4.60	-16.09	0.15	4.27	4.19	-16.11	0.13	4.86	4.71
19	SP2 iwetting gnd vbatt=28v	-18	-12	mA	CT	-15.81	0.17	5.93	4.33	-15.76	0.17	6.02	4.49	-15.81	0.17	6.04	4.42
20	SP3 iwetting gnd vbatt=28v	-18	-12	mA	HT	-15.99	0.15	6.88	4.60	-16.02	0.17	3.93	3.86	-16.06	0.14	4.75	4.73
20	SP3 iwetting gnd vbatt=28v	-18	-12	mA	RT	-16.05	0.14	7.02	4.56	-16.03	0.15	4.25	4.21	-16.09	0.15	4.19	4.10
20	SP3 iwetting gnd vbatt=28v	-18	-12	mA	CT	-15.77	0.18	5.61	4.18	-15.71	0.18	5.64	4.30	-15.79	0.18	5.50	4.05
21	SP4 iwetting gnd vbatt=28v	-18	-12	mA	HT	-15.97	0.12	8.17	5.52	-16.05	0.15	4.27	4.26	-16.03	0.14	4.72	4.68
21	SP4 iwetting gnd vbatt=28v	-18	-12	mA	RT	-16.04	0.12	8.43	5.51	-16.10	0.16	4.07	3.97	-16.10	0.16	4.03	3.94
21	SP4 iwetting gnd vbatt=28v	-18	-12	mA	CT	-15.76	0.15	6.53	4.89	-15.78	0.18	5.45	4.03	-15.79	0.19	5.35	3.95
22	SP5 iwetting gnd vbatt=28v	-18	-12	mA	HT	-15.96	0.13	7.95	5.39	-16.01	0.17	3.80	3.72	-16.01	0.11	5.81	5.70
22	SP5 iwetting gnd vbatt=28v	-18	-12	mA	RT	-16.04	0.13	7.45	4.88	-16.04	0.15	4.20	4.19	-16.06	0.14	4.77	4.73
22	SP5 iwetting gnd vbatt=28v	-18	-12	mA	CT	-15.77	0.16	6.12	4.55	-15.74	0.17	5.96	4.49	-15.78	0.16	6.34	4.69
23	SP6 iwetting gnd vbatt=28v	-18	-12	mA	HT	-15.99	0.14	7.04	4.73	-16.04	0.16	4.13	4.11	-16.04	0.11	5.70	5.67
23	SP6 iwetting gnd vbatt=28v	-18	-12	mA	RT	-16.07	0.13	7.65	4.92	-16.09	0.15	4.35	4.27	-16.08	0.12	5.28	5.18
23	SP6 iwetting gnd vbatt=28v	-18	-12	mA	CT	-15.79	0.16	6.40	4.71	-15.79	0.18	5.47	4.04	-15.81	0.16	6.23	4.54

Freescale Confidential Proprietary

Electrical Distribution Report

						Lot1				Lot2				Lot3			
Test#	Test Name	Lo Limit	Hi Limit	Unit	Temp	Mean	Std Dev	Cp	Cpk	Mean	Std Dev	Cp	Cpk	Mean	Std Dev	Cp	Cpk
24	SP7 iwetting gnd vbatt=28v	-18	-12	mA	HT	-16.01	0.15	6.86	4.56	-16.05	0.16	4.10	4.09	-16.06	0.12	5.60	5.58
24	SP7 iwetting gnd vbatt=28v	-18	-12	mA	RT	-16.09	0.15	6.60	4.19	-16.11	0.16	4.18	4.05	-16.13	0.13	5.04	4.84
24	SP7 iwetting gnd vbatt=28v	-18	-12	mA	CT	-15.82	0.17	5.86	4.25	-15.83	0.17	5.75	4.17	-15.86	0.14	7.19	5.12
25	SG0 wetting current vbatt=28v	-18	-12	mA	HT	-16.08	0.14	7.03	4.49	-16.10	0.15	4.25	4.14	-16.13	0.12	5.55	5.33
25	SG0 wetting current vbatt=28v	-18	-12	mA	RT	-16.13	0.14	7.29	4.54	-16.12	0.14	4.50	4.33	-16.16	0.13	4.91	4.63
25	SG0 wetting current vbatt=28v	-18	-12	mA	CT	-15.83	0.17	5.77	4.18	-15.79	0.16	6.24	4.58	-15.86	0.16	6.43	4.58
26	SG1 wetting current vbatt=28v	-18	-12	mA	HT	-16.02	0.14	7.14	4.71	-16.03	0.17	3.84	3.80	-16.08	0.13	5.20	5.12
26	SG1 wetting current vbatt=28v	-18	-12	mA	RT	-16.06	0.14	7.13	4.61	-16.03	0.16	4.15	4.10	-16.10	0.14	4.57	4.45
26	SG1 wetting current vbatt=28v	-18	-12	mA	CT	-15.76	0.17	5.91	4.42	-15.70	0.18	5.55	4.26	-15.78	0.17	5.87	4.34
27	SG2 wetting current vbatt=28v	-18	-12	mA	HT	-16.01	0.13	7.60	5.05	-16.05	0.17	3.83	3.82	-16.07	0.13	4.93	4.88
27	SG2 wetting current vbatt=28v	-18	-12	mA	RT	-16.04	0.13	7.48	4.88	-16.06	0.17	3.83	3.82	-16.11	0.15	4.41	4.28
27	SG2 wetting current vbatt=28v	-18	-12	mA	CT	-15.75	0.17	5.99	4.49	-15.73	0.19	5.37	4.07	-15.79	0.17	6.02	4.44
28	SG3 wetting current vbatt=28v	-18	-12	mA	HT	-16.06	0.13	7.62	4.92	-16.09	0.16	4.15	4.07	-16.12	0.12	5.25	5.05
28	SG3 wetting current vbatt=28v	-18	-12	mA	RT	-16.11	0.12	8.03	5.05	-16.11	0.15	4.44	4.30	-16.17	0.14	4.66	4.37
28	SG3 wetting current vbatt=28v	-18	-12	mA	CT	-15.81	0.16	6.45	4.70	-15.79	0.17	5.94	4.37	-15.86	0.17	6.06	4.31
29	SG4 wetting current vbatt=28v	-18	-12	mA	HT	-15.99	0.13	7.90	5.28	-16.04	0.16	4.09	4.07	-16.05	0.13	4.88	4.87
29	SG4 wetting current vbatt=28v	-18	-12	mA	RT	-16.06	0.13	7.82	5.06	-16.09	0.16	4.10	4.02	-16.12	0.16	4.17	4.02
29	SG4 wetting current vbatt=28v	-18	-12	mA	CT	-15.78	0.15	6.62	4.90	-15.79	0.18	5.58	4.12	-15.82	0.19	5.37	3.90
30	SG5 wetting current vbatt=28v	-18	-12	mA	HT	-15.99	0.13	7.70	5.17	-16.04	0.16	4.07	4.04	-16.05	0.12	5.55	5.54
30	SG5 wetting current vbatt=28v	-18	-12	mA	RT	-16.05	0.13	7.82	5.08	-16.08	0.16	4.11	4.05	-16.09	0.12	5.28	5.17
30	SG5 wetting current vbatt=28v	-18	-12	mA	CT	-15.77	0.16	6.09	4.52	-15.77	0.18	5.65	4.19	-15.79	0.15	6.78	5.00
31	SG6 wetting current vbatt=28v	-18	-12	mA	HT	-16.04	0.14	7.37	4.82	-16.10	0.17	3.75	3.65	-16.11	0.12	5.25	5.10
31	SG6 wetting current vbatt=28v	-18	-12	mA	RT	-16.13	0.13	7.49	4.67	-16.18	0.17	3.84	3.59	-16.20	0.13	5.09	4.71
31	SG6 wetting current vbatt=28v	-18	-12	mA	CT	-15.87	0.16	6.34	4.50	-15.88	0.18	5.67	4.01	-15.91	0.15	6.50	4.53
32	SG7 wetting current vbatt=28v	-18	-12	mA	HT	-15.97	0.13	7.99	5.42	-16.01	0.15	4.39	4.31	-16.02	0.11	5.79	5.71
32	SG7 wetting current vbatt=28v	-18	-12	mA	RT	-16.04	0.12	8.20	5.36	-16.06	0.14	4.55	4.53	-16.09	0.13	4.84	4.73
32	SG7 wetting current vbatt=28v	-18	-12	mA	CT	-15.77	0.15	6.79	5.04	-15.77	0.17	5.98	4.44	-15.82	0.17	6.03	4.38
33	SG8 wetting current vbatt=28v	-18	-12	mA	HT	-15.93	0.13	7.60	5.24	-15.95	0.15	4.22	4.00	-15.99	0.13	4.92	4.78
33	SG8 wetting current vbatt=28v	-18	-12	mA	RT	-16.01	0.13	7.93	5.25	-15.99	0.14	4.55	4.41	-16.05	0.16	4.10	4.10
33	SG8 wetting current vbatt=28v	-18	-12	mA	CT	-15.72	0.17	6.03	4.58	-15.69	0.16	6.31	4.86	-15.75	0.19	5.20	3.90
34	SG9 wetting current vbatt=28v	-18	-12	mA	HT	-15.96	0.14	21.91	4.97	-16.00	0.14	4.50	4.39	-16.02	0.13	5.06	4.97
34	SG9 wetting current vbatt=28v	-18	-12	mA	RT	-16.03	0.12	8.31	5.45	-16.05	0.14	4.66	4.65	-16.08	0.14	4.74	4.67
34	SG9 wetting current vbatt=28v	-18	-12	mA	CT	-15.74	0.14	6.92	5.20	-15.75	0.16	6.31	4.73	-15.78	0.16	6.41	4.74
35	SG10 wetting current vbatt=28v	-18	-12	mA	HT	-15.95	0.13	7.65	5.24	-16.00	0.15	4.37	4.25	-16.03	0.12	5.46	5.41
35	SG10 wetting current vbatt=28v	-18	-12	mA	RT	-16.01	0.13	7.59	5.03	-16.04	0.14	4.63	4.60	-16.11	0.13	5.00	4.85
35	SG10 wetting current vbatt=28v	-18	-12	mA	CT	-15.73	0.16	6.13	4.64	-15.73	0.17	5.90	4.46	-15.81	0.16	6.22	4.54
36	SG11 wetting current vbatt=28v	-18	-12	mA	HT	-15.95	0.13	7.42	5.07	-16.01	0.14	4.57	4.49	-16.02	0.13	4.96	4.90
36	SG11 wetting current vbatt=28v	-18	-12	mA	RT	-16.02	0.13	7.52	4.96	-16.06	0.14	4.80	4.76	-16.10	0.14	4.70	4.57
36	SG11 wetting current vbatt=28v	-18	-12	mA	CT	-15.73	0.16	6.42	4.85	-15.77	0.16	6.35	4.72	-15.81	0.16	6.35	4.63
37	SG12 wetting current vbatt=28v	-18	-12	mA	HT	-15.96	0.13	7.50	5.10	-16.01	0.15	4.28	4.20	-16.03	0.12	5.29	5.22
37	SG12 wetting current vbatt=28v	-18	-12	mA	RT	-16.03	0.13	7.44	4.89	-16.05	0.15	4.40	4.39	-16.08	0.13	4.94	4.86
37	SG12 wetting current vbatt=28v	-18	-12	mA	CT	-15.75	0.16	6.11	4.58	-15.76	0.16	6.23	4.65	-15.80	0.15	6.53	4.79
38	SG13 wetting current vbatt=28v	-18	-12	mA	HT	-15.95	0.14	7.34	5.02	-16.01	0.15	4.39	4.30	-16.01	0.12	5.21	5.10
38	SG13 wetting current vbatt=28v	-18	-12	mA	RT	-16.05	0.14	7.25	4.72	-16.09	0.15	4.42	4.33	-16.10	0.13	5.20	5.06
38	SG13 wetting current vbatt=28v	-18	-12	mA	CT	-15.79	0.16	6.19	4.57	-15.80	0.17	6.03	4.43	-15.82	0.15	6.89	5.01
39	SP0 isustain batt 28v	1.8	2.2	mA	HT	2.12	0.02	3.17	1.33	2.12	0.02	3.37	1.43	2.12	0.02	3.94	1.67
39	SP0 isustain batt 28v	1.8	2.2	mA	RT	2.11	0.02	3.26	1.45	2.11	0.02	3.65	1.71	2.11	0.02	3.33	1.54
39	SP0 isustain batt 28v	1.8	2.2	mA	CT	2.09	0.02	2.71	1.54	2.08	0.02	3.10	1.89	2.09	0.03	2.46	1.44
40	SP1 isustain batt 28v	1.8	2.2	mA	HT	2.12	0.02	3.15	1.31	2.12	0.02	3.20	1.30	2.12	0.02	3.42	1.35
40	SP1 isustain batt 28v	1.8	2.2	mA	RT	2.12	0.02	3.11	1.22	2.12	0.02	3.08	1.31	2.12	0.02	2.97	1.21
40	SP1 isustain batt 28v	1.8	2.2	mA	CT	2.10	0.03	2.62	1.28	2.09	0.03	2.54	1.39	2.10	0.03	2.18	1.10
41	SP2 isustain batt 28v	1.8	2.2	mA	HT	2.12	0.02	3.52	1.48	2.12	0.02	2.99	1.17	2.12	0.02	3.72	1.46
41	SP2 isustain batt 28v	1.8	2.2	mA	RT	2.12	0.02	3.98	1.53	2.12	0.02	2.90	1.15	2.12	0.02	3.19	1.24
41	SP2 isustain batt 28v	1.8	2.2	mA	CT	2.11	0.02	3.30	1.56	2.10	0.03	2.49	1.24	2.11	0.03	2.31	1.10
42	SP3 isustain batt 28v	1.8	2.2	mA	HT	2.11	0.02	3.08	1.38	2.12	0.02	3.42	1.44	2.12	0.02	3.77	1.63
42	SP3 isustain batt 28v	1.8	2.2	mA	RT	2.12	0.02	3.17	1.32	2.12	0.02	3.54	1.50	2.12	0.02	3.20	1.38
42	SP3 isustain batt 28v	1.8	2.2	mA	CT	2.10	0.03	2.62	1.31	2.10	0.02	2.85	1.51	2.10	0.03	2.34	1.20
43	SP4 isustain batt 28v	1.8	2.2	mA	HT	2.11	0.02	3.08	1.40	2.11	0.02	3.35	1.49	2.12	0.02	3.72	1.60
43	SP4 isustain batt 28v	1.8	2.2	mA	RT	2.11	0.02	3.25	1.43	2.11	0.02	3.42	1.65	2.11	0.02	3.06	1.40
43	SP4 isustain batt 28v	1.8	2.2	mA	CT	2.09	0.02	3.01	1.67	2.08	0.02	2.84	1.76	2.09	0.03	2.24	1.28

Freescale Confidential Proprietary

Electrical Distribution Report

						Lot1				Lot2				Lot3			
Test#	Test Name	Lo Limit	Hi Limit	Unit	Temp	Mean	Std Dev	Cp	Cpk	Mean	Std Dev	Cp	Cpk	Mean	Std Dev	Cp	Cpk
44	SP5 isustain batt 28v	1.8	2.2	mA	HT	2.11	0.02	3.14	1.41	2.12	0.02	3.40	1.44	2.12	0.02	3.69	1.57
44	SP5 isustain batt 28v	1.8	2.2	mA	RT	2.12	0.02	3.29	1.36	2.12	0.02	3.22	1.40	2.12	0.02	3.24	1.38
44	SP5 isustain batt 28v	1.8	2.2	mA	CT	2.10	0.03	2.60	1.31	2.09	0.02	2.64	1.43	2.10	0.03	2.29	1.17
45	SP6 isustain batt 28v	1.8	2.2	mA	HT	2.12	0.02	3.25	1.38	2.12	0.02	3.43	1.38	2.12	0.02	3.64	1.46
45	SP6 isustain batt 28v	1.8	2.2	mA	RT	2.12	0.02	3.25	1.28	2.12	0.02	3.49	1.41	2.12	0.02	3.02	1.20
45	SP6 isustain batt 28v	1.8	2.2	mA	CT	2.10	0.02	2.76	1.31	2.10	0.02	2.88	1.46	2.11	0.03	2.26	1.09
46	SP7 isustain batt 28v	1.8	2.2	mA	HT	2.11	0.02	3.14	1.51	2.11	0.02	3.58	1.58	2.11	0.02	3.58	1.63
46	SP7 isustain batt 28v	1.8	2.2	mA	RT	2.11	0.02	3.35	1.56	2.11	0.02	3.47	1.61	2.11	0.02	3.10	1.45
46	SP7 isustain batt 28v	1.8	2.2	mA	CT	2.09	0.02	2.73	1.51	2.09	0.02	2.78	1.60	2.09	0.03	2.34	1.31
47	SP0 isustain gnd batt=28v	-2.2	-1.8	mA	HT	-2.01	0.02	4.31	4.15	-2.01	0.02	3.49	3.37	-2.01	0.01	3.90	3.69
47	SP0 isustain gnd batt=28v	-2.2	-1.8	mA	RT	-2.01	0.01	4.65	4.36	-2.01	0.02	39.85	3.30	-2.02	0.02	3.55	3.17
47	SP0 isustain gnd batt=28v	-2.2	-1.8	mA	CT	-1.98	0.02	3.46	3.09	-1.97	0.02	3.16	2.77	-1.98	0.02	3.03	2.81
48	SP1 isustain gnd batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	4.16	4.08	-2.00	0.02	3.42	3.27	-2.01	0.01	4.12	3.81
48	SP1 isustain gnd batt=28v	-2.2	-1.8	mA	RT	-2.01	0.02	3.93	3.71	-2.01	0.02	3.57	3.39	-2.01	0.02	4.27	3.91
48	SP1 isustain gnd batt=28v	-2.2	-1.8	mA	CT	-1.98	0.02	3.04	2.76	-1.97	0.02	3.18	2.72	-1.98	0.02	3.61	3.24
49	SP2 isustain gnd batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	3.77	3.72	-2.00	0.02	3.60	3.47	-2.00	0.01	4.09	3.72
49	SP2 isustain gnd batt=28v	-2.2	-1.8	mA	RT	-2.01	0.02	3.94	3.76	-2.00	0.02	3.81	3.62	-2.01	0.02	4.10	3.84
49	SP2 isustain gnd batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.29	2.92	-1.97	0.02	3.46	2.93	-1.97	0.02	3.42	2.99
50	SP3 isustain gnd batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	3.74	3.72	-2.00	0.02	3.31	3.25	-2.00	0.02	3.54	3.21
50	SP3 isustain gnd batt=28v	-2.2	-1.8	mA	RT	-2.00	0.02	3.89	3.81	-2.00	0.02	3.54	3.46	-2.01	0.02	3.34	3.13
50	SP3 isustain gnd batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.19	2.75	-1.96	0.02	3.03	2.48	-1.97	0.02	2.86	2.49
51	SP4 isustain gnd batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	4.04	4.02	-2.01	0.02	3.50	3.31	-2.00	0.02	3.57	3.23
51	SP4 isustain gnd batt=28v	-2.2	-1.8	mA	RT	-2.00	0.02	4.33	4.24	-2.01	0.02	3.41	3.16	-2.01	0.02	3.59	3.33
51	SP4 isustain gnd batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.45	2.99	-1.97	0.02	3.10	2.72	-1.97	0.02	3.01	2.64
52	SP5 isustain gnd batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	3.97	3.97	-2.00	0.02	3.42	3.34	-2.00	0.02	3.77	3.39
52	SP5 isustain gnd batt=28v	-2.2	-1.8	mA	RT	-2.01	0.02	3.89	3.75	-2.00	0.02	3.98	3.83	-2.01	0.02	3.51	3.29
52	SP5 isustain gnd batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.09	2.72	-1.96	0.02	3.62	3.06	-1.97	0.02	3.04	2.68
53	SP6 isustain gnd batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	3.72	3.68	-2.00	0.02	3.31	3.20	-2.00	0.01	4.10	3.64
53	SP6 isustain gnd batt=28v	-2.2	-1.8	mA	RT	-2.01	0.02	4.06	3.96	-2.00	0.02	3.35	3.20	-2.00	0.02	4.21	4.01
53	SP6 isustain gnd batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.43	2.99	-1.97	0.02	2.87	2.48	-1.97	0.02	3.24	2.84
54	SP7 isustain gnd batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	3.71	3.70	-2.00	0.02	3.41	3.30	-2.00	0.01	3.86	3.51
54	SP7 isustain gnd batt=28v	-2.2	-1.8	mA	RT	-2.01	0.02	3.68	3.53	-2.00	0.02	3.43	3.26	-2.01	0.02	3.74	3.45
54	SP7 isustain gnd batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.09	2.77	-1.97	0.02	3.02	2.63	-1.98	0.02	3.24	2.94
55	SG0 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.01	0.02	3.58	3.39	-2.01	0.02	3.52	3.26	-2.01	0.01	4.33	4.15
55	SG0 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.01	0.02	3.83	3.56	-2.01	0.02	3.75	3.46	-2.02	0.02	4.14	3.68
55	SG0 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.98	0.02	3.10	2.83	-1.97	0.02	3.46	3.02	-1.98	0.02	3.48	3.20
56	SG1 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.01	0.02	3.63	3.51	-2.01	0.02	3.24	3.05	-2.01	0.01	4.14	3.90
56	SG1 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.01	0.02	3.66	3.48	-2.01	0.02	3.30	3.13	-2.01	0.02	3.96	3.61
56	SG1 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.30	2.93	-1.96	0.02	2.93	2.46	-1.97	0.02	3.23	2.86
57	SG2 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.01	0.02	3.84	3.70	-2.01	0.02	3.27	3.03	-2.01	0.02	3.52	3.35
57	SG2 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.01	0.02	4.10	3.87	-2.01	0.02	3.33	3.07	-2.02	0.02	3.66	3.28
57	SG2 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.25	2.89	-1.97	0.02	2.93	2.54	-1.98	0.02	3.24	2.91
58	SG3 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.01	0.02	3.91	3.78	-2.01	0.02	3.42	3.17	-2.01	0.01	4.37	4.17
58	SG3 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.01	0.02	4.17	3.93	-2.01	0.02	3.48	3.20	-2.02	0.02	4.27	3.79
58	SG3 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.50	3.13	-1.97	0.02	3.05	2.68	-1.98	0.02	3.44	3.15
59	SG4 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.01	0.02	3.96	3.85	-2.01	0.02	3.55	3.29	-2.01	0.01	3.83	3.58
59	SG4 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.01	0.02	4.03	3.79	-2.01	0.02	3.64	3.29	-2.01	0.02	3.78	3.40
59	SG4 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.98	0.02	3.37	3.09	-1.98	0.02	3.17	2.87	-1.98	0.02	3.13	2.85
60	SG5 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	4.04	4.00	-2.00	0.02	3.32	3.20	-2.00	0.01	3.93	3.56
60	SG5 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.00	0.02	4.19	4.10	-2.01	0.02	3.23	3.07	-2.01	0.01	4.42	4.11
60	SG5 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.40	2.96	-1.97	0.02	2.89	2.48	-1.97	0.02	3.71	3.26
61	SG6 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	3.85	3.83	-2.00	0.02	3.35	3.21	-2.01	0.02	3.72	3.41
61	SG6 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.01	0.02	4.08	3.94	-2.01	0.02	3.59	3.38	-2.01	0.02	4.01	3.69
61	SG6 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.64	3.21	-1.97	0.02	3.32	2.86	-1.97	0.02	3.42	3.05
62	SG7 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	3.95	3.89	-2.00	0.02	3.54	3.37	-2.01	0.01	4.03	3.72
62	SG7 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.01	0.02	4.35	4.11	-2.01	0.02	3.73	3.45	-2.01	0.02	3.83	3.47
62	SG7 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.98	0.02	3.43	3.13	-1.97	0.02	3.21	2.85	-1.98	0.02	3.07	2.81
63	SG8 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	3.88	3.79	-2.00	0.02	3.47	3.46	-2.00	0.02	3.58	3.15
63	SG8 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.00	0.02	4.25	4.17	-2.00	0.02	3.87	3.79	-2.00	0.02	3.36	3.19
63	SG8 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.18	2.73	-1.96	0.02	3.54	2.93	-1.97	0.02	2.75	2.39

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Electrical Distribution Report

						Lot1				Lot2				Lot3			
Test#	Test Name	Lo Limit	Hi Limit	Unit	Temp	Mean	Std Dev	Cp	Cpk	Mean	Std Dev	Cp	Cpk	Mean	Std Dev	Cp	Cpk
64	SG9 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	3.91	3.84	-2.00	0.02	3.78	3.68	-2.00	0.02	3.53	3.15
64	SG9 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.00	0.02	4.13	4.06	-2.00	0.01	4.36	4.14	-2.01	0.02	3.57	3.34
64	SG9 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.47	2.98	-1.97	0.02	3.87	3.34	-1.97	0.02	3.16	2.78
65	SG10 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	4.02	3.96	-2.00	0.02	3.59	3.46	-2.00	0.01	3.82	3.46
65	SG10 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.00	0.02	3.93	3.85	-2.01	0.02	3.58	3.38	-2.01	0.02	3.74	3.42
65	SG10 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.35	2.91	-1.97	0.02	3.12	2.70	-1.98	0.02	3.02	2.71
66	SG11 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	3.96	3.89	-2.00	0.02	3.80	3.67	-2.00	0.01	3.82	3.44
66	SG11 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.00	0.02	4.16	4.09	-2.01	0.02	3.87	3.65	-2.01	0.02	3.95	3.65
66	SG11 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.40	2.94	-1.97	0.02	3.42	2.98	-1.97	0.02	3.22	2.87
67	SG12 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	4.18	4.08	-2.00	0.02	3.63	3.57	-2.00	0.01	5.26	3.56
67	SG12 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.00	0.02	4.38	4.31	-2.00	0.02	3.52	3.40	-2.00	0.02	4.23	4.03
67	SG12 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.60	3.12	-1.97	0.02	3.27	2.78	-1.97	0.02	3.46	3.00
68	SG13 sustain current batt=28v	-2.2	-1.8	mA	HT	-2.00	0.02	4.02	3.96	-2.00	0.02	3.53	3.44	-2.00	0.01	3.89	3.47
68	SG13 sustain current batt=28v	-2.2	-1.8	mA	RT	-2.00	0.02	4.35	4.27	-2.00	0.02	3.67	3.52	-2.01	0.02	3.92	3.68
68	SG13 sustain current batt=28v	-2.2	-1.8	mA	CT	-1.97	0.02	3.57	3.12	-1.97	0.02	3.29	2.80	-1.97	0.02	3.09	2.71
69	IMATCH	-4	4	%	HT	1.33	0.34	3.87	2.59	1.25	0.42	3.17	2.18	1.29	0.25	5.26	3.56
69	IMATCH	-4	4	%	RT	1.55	0.32	4.21	2.58	1.44	0.35	3.76	2.41	1.50	0.32	4.12	2.58
69	IMATCH	-4	4	%	CT	1.85	0.40	3.30	1.77	1.67	0.42	3.17	1.84	1.72	0.35	3.78	2.15
70	SP0 ioffset analog	-2	2	uA	HT	-0.44	0.01	88.68	69.08	-0.44	0.01	103.60	80.99	-0.44	0.01	82.06	63.93
70	SP0 ioffset analog	-2	2	uA	RT	-0.29	0.01	123.72	106.03	-0.29	0.01	98.44	84.32	-0.29	0.01	111.09	95.13
70	SP0 ioffset analog	-2	2	uA	CT	-0.25	0.01	113.05	99.18	-0.24	0.01	115.11	101.13	-0.25	0.01	107.11	93.99
71	SP1 ioffset analog	-2	2	uA	HT	-0.31	0.01	123.04	103.72	-0.31	0.00	152.59	128.91	-0.32	0.01	66.13	35.40
71	SP1 ioffset analog	-2	2	uA	RT	-0.21	0.01	130.71	117.15	-0.21	0.00	183.92	165.05	-0.21	0.01	72.79	65.25
71	SP1 ioffset analog	-2	2	uA	CT	-0.18	0.00	135.27	122.79	-0.18	0.00	175.86	159.81	-0.18	0.00	168.34	152.84
72	SP2 ioffset analog	-2	2	uA	HT	-0.31	0.00	134.72	113.84	-0.31	0.01	118.55	100.43	-0.31	0.01	71.87	38.14
72	SP2 ioffset analog	-2	2	uA	RT	-0.20	0.00	157.16	141.08	-0.20	0.01	129.78	116.52	-0.21	0.01	131.23	117.73
72	SP2 ioffset analog	-2	2	uA	CT	-0.18	0.00	146.38	132.85	-0.18	0.00	149.73	136.03	-0.18	0.00	139.21	126.35
73	SP3 ioffset analog	-2	2	uA	HT	-0.09	0.00	146.01	139.53	-0.09	0.00	155.46	148.77	-0.09	0.00	81.17	27.51
73	SP3 ioffset analog	-2	2	uA	RT	-0.05	0.00	537.09	523.85	-0.05	0.00	522.48	509.94	-0.05	0.00	600.37	585.62
73	SP3 ioffset analog	-2	2	uA	CT	-0.06	0.00	417.62	404.84	-0.06	0.00	427.48	414.77	-0.06	0.00	509.56	494.40
74	SP4 ioffset analog	-2	2	uA	HT	-0.42	0.01	110.14	86.98	-0.42	0.01	103.10	81.59	-0.42	0.01	49.52	31.18
74	SP4 ioffset analog	-2	2	uA	RT	-0.28	0.00	141.56	121.80	-0.28	0.01	96.87	83.48	-0.28	0.00	138.13	118.85
74	SP4 ioffset analog	-2	2	uA	CT	-0.24	0.01	129.03	113.65	-0.24	0.01	121.31	106.91	-0.24	0.01	117.10	103.11
75	SP5 ioffset analog	-2	2	uA	HT	-0.43	0.01	65.77	51.71	-0.43	0.01	73.39	57.76	-0.43	0.01	48.90	30.93
75	SP5 ioffset analog	-2	2	uA	RT	-0.29	0.01	95.46	81.73	-0.29	0.01	93.91	80.50	-0.29	0.01	79.77	68.37
75	SP5 ioffset analog	-2	2	uA	CT	-0.24	0.01	100.54	88.24	-0.24	0.01	123.96	108.89	-0.24	0.01	81.45	71.47
76	SP6 ioffset analog	-2	2	uA	HT	-0.42	0.01	64.91	51.21	-0.42	0.01	69.50	54.90	-0.42	0.01	39.99	25.20
76	SP6 ioffset analog	-2	2	uA	RT	-0.28	0.01	87.97	75.56	-0.28	0.01	85.05	73.11	-0.28	0.01	92.47	79.54
76	SP6 ioffset analog	-2	2	uA	CT	-0.24	0.01	115.48	101.62	-0.24	0.01	102.84	90.56	-0.24	0.01	102.22	90.00
77	SP7 ioffset analog	-2	2	uA	HT	-0.42	0.01	57.82	45.63	-0.42	0.01	73.39	58.12	-0.42	0.01	42.97	27.00
77	SP7 ioffset analog	-2	2	uA	RT	-0.28	0.01	104.54	89.84	-0.28	0.01	91.01	78.27	-0.28	0.01	112.12	96.32
77	SP7 ioffset analog	-2	2	uA	CT	-0.24	0.01	88.94	78.21	-0.24	0.01	104.24	91.88	-0.24	0.01	94.54	83.19
78	SG0 ioffset analog	-2	2	uA	HT	-0.41	0.01	95.10	75.42	-0.41	0.01	80.79	64.15	-0.42	0.01	48.16	29.96
78	SG0 ioffset analog	-2	2	uA	RT	-0.27	0.01	124.41	107.45	-0.27	0.00	142.81	123.37	-0.27	0.01	116.73	100.81
78	SG0 ioffset analog	-2	2	uA	CT	-0.23	0.01	98.12	86.74	-0.23	0.01	129.97	114.81	-0.23	0.01	107.64	95.06
79	SG1 ioffset analog	-2	2	uA	HT	-0.28	0.00	168.94	145.36	-0.28	0.00	141.19	121.63	-0.28	0.00	104.89	52.97
79	SG1 ioffset analog	-2	2	uA	RT	-0.18	0.00	180.63	164.08	-0.18	0.00	189.65	172.59	-0.18	0.00	205.34	186.59
79	SG1 ioffset analog	-2	2	uA	CT	-0.16	0.00	196.03	179.87	-0.16	0.00	169.67	155.80	-0.17	0.00	173.15	158.83
80	SG2 ioffset analog	-2	2	uA	HT	-0.42	0.01	79.06	62.40	-0.42	0.01	72.78	57.52	-0.43	0.01	38.84	24.51
80	SG2 ioffset analog	-2	2	uA	RT	-0.28	0.01	131.33	113.21	-0.27	0.01	92.09	79.45	-0.28	0.00	134.41	115.83
80	SG2 ioffset analog	-2	2	uA	CT	-0.23	0.01	108.20	95.57	-0.23	0.01	87.97	77.70	-0.23	0.01	116.10	102.50
81	SG3 ioffset analog	-2	2	uA	HT	-0.31	0.01	123.64	104.61	-0.30	0.01	123.93	105.06	-0.31	0.00	88.43	46.93
81	SG3 ioffset analog	-2	2	uA	RT	-0.20	0.00	146.94	132.13	-0.20	0.00	152.90	137.65	-0.20	0.01	133.04	119.60
81	SG3 ioffset analog	-2	2	uA	CT	-0.18	0.00	149.23	135.74	-0.18	0.00	160.27	145.98	-0.18	0.00	162.83	148.18
82	SG4 ioffset analog	-2	2	uA	HT	-0.42	0.01	105.67	83.56	-0.42	0.01	77.30	61.17	-0.42	0.01	68.71	43.12
82	SG4 ioffset analog	-2	2	uA	RT	-0.28	0.01	113.17	97.57	-0.27	0.02	29.94	25.91	-0.28	0.01	117.37	101.07
82	SG4 ioffset analog	-2	2	uA	CT	-0.23	0.01	116.50	102.86	-0.23	0.01	82.62	73.00	-0.24	0.01	118.29	104.30
83	SG5 ioffset analog	-2	2	uA	HT	-0.41	0.01	87.41	69.63	-0.40	0.01	79.81	63.70	-0.41	0.01	58.82	36.12
83	SG5 ioffset analog	-2	2	uA	RT	-0.27	0.01	129.13	111.92	-0.26	0.01	117.60	102.07	-0.26	0.01	103.85	90.16
83	SG5 ioffset analog	-2	2	uA	CT	-0.23	0.01	107.71	95.45	-0.23	0.01	107.25	95.14	-0.23	0.01	104.52	92.68

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Test#	Test Name	Lo Limit	Hi Limit	Unit	Temp	Lot1 Mean	Lot1 Std Dev	Lot1 Cp	Lot1 Cpk	Lot2 Mean	Lot2 Std Dev	Lot2 Cp	Lot2 Cpk	Lot3 Mean	Lot3 Std Dev	Lot3 Cp	Lot3 Cpk
84	SG6 ioffset analog	-2	2	uA	HT	-0.41	0.01	70.33	55.96	-0.41	0.01	85.94	68.37	-0.41	0.01	38.43	23.81
84	SG6 ioffset analog	-2	2	uA	RT	-0.27	0.01	114.62	99.38	-0.27	0.01	83.49	72.34	-0.27	0.01	89.95	77.81
84	SG6 ioffset analog	-2	2	uA	CT	-0.23	0.01	124.88	110.55	-0.23	0.01	96.68	85.54	-0.23	0.01	92.87	82.03
85	SG7 ioffset analog	-2	2	uA	HT	-0.41	0.01	63.30	50.36	-0.40	0.01	69.55	55.49	-0.41	0.01	39.39	24.36
85	SG7 ioffset analog	-2	2	uA	RT	-0.27	0.01	91.06	78.81	-0.27	0.01	99.10	85.80	-0.27	0.01	93.75	81.08
85	SG7 ioffset analog	-2	2	uA	CT	-0.23	0.01	95.76	84.68	-0.23	0.01	93.43	82.71	-0.23	0.01	88.29	78.11
86	SG8 ioffset analog	-2	2	uA	HT	-0.42	0.01	105.01	83.07	-0.42	0.01	98.82	78.27	-0.42	0.01	55.26	34.66
86	SG8 ioffset analog	-2	2	uA	RT	-0.27	0.01	70.43	60.75	-0.28	0.01	109.85	94.69	-0.28	0.01	125.21	107.72
86	SG8 ioffset analog	-2	2	uA	CT	-0.24	0.01	115.88	102.15	-0.24	0.01	108.25	95.48	-0.24	0.00	144.55	127.46
87	SG9 ioffset analog	-2	2	uA	HT	-0.41	0.01	67.83	53.76	-0.41	0.01	91.31	72.60	-0.42	0.01	58.61	36.51
87	SG9 ioffset analog	-2	2	uA	RT	-0.27	0.02	28.08	24.30	-0.27	0.01	54.23	46.90	-0.28	0.01	96.66	83.30
87	SG9 ioffset analog	-2	2	uA	CT	-0.24	0.01	99.68	87.96	-0.23	0.01	130.44	115.36	-0.24	0.01	122.57	108.12
88	SG10 ioffset analog	-2	2	uA	HT	-0.42	0.01	75.45	59.63	-0.42	0.01	99.06	78.30	-0.42	0.01	51.06	32.16
88	SG10 ioffset analog	-2	2	uA	RT	-0.27	0.03	26.64	23.03	-0.28	0.01	57.74	49.76	-0.28	0.01	103.20	88.72
88	SG10 ioffset analog	-2	2	uA	CT	-0.24	0.01	100.45	88.51	-0.24	0.00	137.04	120.71	-0.24	0.01	98.99	87.04
89	SG11 ioffset analog	-2	2	uA	HT	-0.43	0.01	64.70	50.65	-0.43	0.01	67.36	52.81	-0.44	0.01	38.90	24.94
89	SG11 ioffset analog	-2	2	uA	RT	-0.29	0.01	85.96	73.60	-0.29	0.02	42.07	36.04	-0.29	0.01	72.75	62.10
89	SG11 ioffset analog	-2	2	uA	CT	-0.25	0.01	94.68	83.03	-0.25	0.01	94.28	82.68	-0.25	0.01	76.68	67.16
90	SG12 ioffset analog	-2	2	uA	HT	-0.43	0.01	84.90	66.68	-0.43	0.01	95.95	75.48	-0.43	0.01	51.84	33.05
90	SG12 ioffset analog	-2	2	uA	RT	-0.28	0.01	105.40	90.41	-0.28	0.01	118.30	101.51	-0.29	0.01	108.35	92.91
90	SG12 ioffset analog	-2	2	uA	CT	-0.24	0.01	108.48	95.29	-0.24	0.01	121.22	106.46	-0.24	0.01	118.05	103.60
91	SG13 ioffset analog	-2	2	uA	HT	-0.43	0.01	85.38	67.20	-0.42	0.01	67.95	53.58	-0.43	0.01	71.81	56.43
91	SG13 ioffset analog	-2	2	uA	RT	-0.28	0.01	85.70	73.62	-0.28	0.01	96.24	82.62	-0.28	0.01	94.91	81.58
91	SG13 ioffset analog	-2	2	uA	CT	-0.24	0.01	96.56	84.93	-0.24	0.01	101.51	89.39	-0.24	0.01	85.90	75.59
92	Sp0 output offset voltage	-10	10	mV	HT	2.41	0.27	12.52	9.51	2.46	0.34	9.85	7.43	2.42	0.38	8.68	6.58
92	Sp0 output offset voltage	-10	10	mV	RT	1.16	0.27	12.31	10.87	1.23	0.25	13.37	11.72	1.24	0.33	10.25	8.99
92	Sp0 output offset voltage	-10	10	mV	CT	0.59	0.31	10.78	10.15	0.53	0.31	10.62	10.05	0.66	0.36	9.19	8.59
93	Sp1 output offset voltage	-10	10	mV	HT	2.64	0.27	12.56	9.24	2.72	0.32	10.49	7.63	2.69	0.33	10.24	7.49
93	Sp1 output offset voltage	-10	10	mV	RT	1.39	0.24	11.98	8.19	1.45	0.23	14.35	12.28	1.45	0.33	10.17	8.70
93	Sp1 output offset voltage	-10	10	mV	CT	0.82	0.29	11.46	10.52	0.84	0.27	12.54	11.49	0.93	0.33	10.09	9.15
94	Sp2 output offset voltage	-10	10	mV	HT	2.04	0.28	12.09	9.62	2.08	0.30	11.07	8.76	2.09	0.35	9.44	7.46
94	Sp2 output offset voltage	-10	10	mV	RT	0.90	0.26	11.16	8.26	0.94	0.26	12.98	11.76	0.98	0.30	11.14	10.05
94	Sp2 output offset voltage	-10	10	mV	CT	0.33	0.37	9.01	8.71	0.34	0.34	9.76	9.43	0.39	0.39	8.52	8.18
95	Sp3 output offset voltage	-10	10	mV	HT	2.15	0.25	13.10	10.28	2.21	0.32	10.51	8.18	2.18	0.32	10.41	8.14
95	Sp3 output offset voltage	-10	10	mV	RT	0.93	0.23	12.32	9.07	0.95	0.21	15.85	14.34	0.96	0.32	10.34	9.35
95	Sp3 output offset voltage	-10	10	mV	CT	0.28	0.36	9.36	9.10	0.33	0.30	11.11	10.74	0.34	0.39	8.65	8.35
96	Sp4 output offset voltage	-10	10	mV	HT	1.70	0.32	10.43	8.65	1.79	0.35	9.65	7.92	1.75	0.37	8.93	7.36
96	Sp4 output offset voltage	-10	10	mV	RT	0.46	0.26	10.90	8.62	0.52	0.25	13.21	12.53	0.51	0.35	9.54	9.06
96	Sp4 output offset voltage	-10	10	mV	CT	-0.21	0.37	9.08	8.89	-0.19	0.37	9.13	8.96	-0.14	0.42	8.00	7.89
97	Sp5 output offset voltage	-10	10	mV	HT	1.57	0.26	12.75	10.75	1.61	0.35	9.61	8.06	1.65	0.33	10.13	8.46
97	Sp5 output offset voltage	-10	10	mV	RT	0.28	0.25	11.53	9.35	0.32	0.28	11.83	11.46	0.34	0.34	9.85	9.51
97	Sp5 output offset voltage	-10	10	mV	CT	-0.45	0.37	9.11	8.70	-0.40	0.37	9.06	8.69	-0.36	0.42	8.02	7.73
98	Sp6 output offset voltage	-10	10	mV	HT	1.83	0.26	13.07	10.67	1.91	0.31	10.66	8.63	1.84	0.33	10.18	8.31
98	Sp6 output offset voltage	-10	10	mV	RT	0.60	0.25	11.75	9.09	0.62	0.29	11.54	10.82	0.59	0.36	9.17	8.63
98	Sp6 output offset voltage	-10	10	mV	CT	-0.13	0.37	8.97	8.85	-0.05	0.34	9.88	9.83	-0.05	0.43	7.80	7.76
99	Sp7 output offset voltage	-10	10	mV	HT	1.75	0.26	12.95	10.68	1.79	0.32	10.29	8.45	1.78	0.36	9.33	7.66
99	Sp7 output offset voltage	-10	10	mV	RT	0.62	0.30	9.60	7.42	0.65	0.27	12.51	11.70	0.64	0.32	10.32	9.67
99	Sp7 output offset voltage	-10	10	mV	CT	0.00	0.37	9.07	9.06	-0.02	0.36	9.17	9.15	0.10	0.46	7.33	7.25
100	Sg0 output offset voltage	-10	10	mV	HT	0.03	0.11	29.51	29.44	0.03	0.12	27.67	27.58	0.03	0.13	25.50	25.43
100	Sg0 output offset voltage	-10	10	mV	RT	-0.01	0.14	20.43	17.27	-0.02	0.13	24.93	24.89	-0.01	0.14	23.37	23.34
100	Sg0 output offset voltage	-10	10	mV	CT	0.04	0.17	19.67	19.59	0.02	0.12	28.11	28.06	0.01	0.13	25.15	25.13
101	Sg1 output offset voltage	-10	10	mV	HT	2.15	0.27	12.54	9.84	2.16	0.29	11.32	8.88	2.17	0.30	11.06	8.67
101	Sg1 output offset voltage	-10	10	mV	RT	0.90	0.24	12.09	8.95	0.95	0.24	14.13	12.78	0.94	0.31	10.60	9.61
101	Sg1 output offset voltage	-10	10	mV	CT	0.22	0.35	9.47	9.27	0.31	0.32	10.38	10.06	0.33	0.39	8.58	8.30
102	Sg2 output offset voltage	-10	10	mV	HT	2.60	0.28	12.11	8.96	2.64	0.31	10.90	8.02	2.62	0.33	10.05	7.41
102	Sg2 output offset voltage	-10	10	mV	RT	1.34	0.27	10.88	7.49	1.38	0.27	12.20	10.52	1.42	0.30	11.11	9.53
102	Sg2 output offset voltage	-10	10	mV	CT	0.72	0.29	11.34	10.53	0.75	0.35	9.59	8.88	0.79	0.41	8.16	7.51
103	Sg3 output offset voltage	-10	10	mV	HT	2.63	0.24	13.84	10.19	2.68	0.31	10.74	7.87	2.65	0.33	10.21	7.51
103	Sg3 output offset voltage	-10	10	mV	RT	1.47	0.23	12.51	8.42	1.48	0.22	14.86	12.66	1.48	0.30	11.30	9.63
103	Sg3 output offset voltage	-10	10	mV	CT	0.94	0.26	12.66	11.48	0.97	0.27	12.53	11.32	0.99	0.32	10.40	9.37

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Electrical Distribution Report

						Lot1				Lot2				Lot3			
Test#	Test Name	Lo Limit	Hi Limit	Unit	Temp	Mean	Std Dev	Cp	Cpk	Mean	Std Dev	Cp	Cpk	Mean	Std Dev	Cp	Cpk
104	Sg4 output offset voltage	-10	10	mV	HT	2.40	0.30	11.02	8.37	2.48	0.34	9.76	7.34	2.44	0.37	9.06	6.85
104	Sg4 output offset voltage	-10	10	mV	RT	1.20	0.31	9.27	6.54	1.25	0.27	12.31	10.77	1.25	0.35	9.55	8.36
104	Sg4 output offset voltage	-10	10	mV	CT	0.64	0.30	11.09	10.38	0.69	0.30	10.94	10.18	0.69	0.38	8.73	8.13
105	Sg5 output offset voltage	-10	10	mV	HT	0.04	0.16	21.41	21.33	-0.03	0.16	21.40	21.34	0.02	0.12	27.77	27.73
105	Sg5 output offset voltage	-10	10	mV	RT	0.02	0.13	21.71	18.28	0.02	0.13	25.60	25.55	0.01	0.11	29.74	29.70
105	Sg5 output offset voltage	-10	10	mV	CT	0.05	0.14	23.88	23.77	0.06	0.15	21.80	21.66	0.04	0.16	21.47	21.38
106	Sg6 output offset voltage	-10	10	mV	HT	0.02	0.14	24.66	24.63	0.05	0.13	25.37	25.25	0.02	0.13	25.52	25.48
106	Sg6 output offset voltage	-10	10	mV	RT	0.02	0.13	21.70	18.26	0.00	0.13	25.84	25.84	0.07	0.14	23.27	23.10
106	Sg6 output offset voltage	-10	10	mV	CT	0.03	0.14	23.89	23.82	0.04	0.17	19.18	19.09	0.05	0.15	22.94	22.84
107	Sg7 output offset voltage	-10	10	mV	HT	1.71	0.27	12.38	10.26	1.79	0.33	9.98	8.20	1.75	0.35	9.59	7.91
107	Sg7 output offset voltage	-10	10	mV	RT	0.49	0.22	13.13	10.34	0.53	0.26	13.00	12.32	0.53	0.31	10.87	10.29
107	Sg7 output offset voltage	-10	10	mV	CT	-0.23	0.33	10.03	9.80	-0.19	0.34	9.76	9.57	-0.20	0.46	7.30	7.16
108	Sg8 output offset voltage	-10	10	mV	HT	1.79	0.29	11.31	9.29	1.80	0.32	10.28	8.43	1.78	0.33	9.95	8.19
108	Sg8 output offset voltage	-10	10	mV	RT	0.55	0.28	10.36	8.09	0.57	0.26	12.80	12.07	0.56	0.31	10.80	10.19
108	Sg8 output offset voltage	-10	10	mV	CT	-0.19	0.37	8.91	8.75	-0.08	0.39	8.56	8.49	-0.07	0.40	8.37	8.31
109	Sg9 output offset voltage	-10	10	mV	HT	1.80	0.32	10.52	8.63	1.83	0.32	10.31	8.42	1.84	0.36	9.26	7.56
109	Sg9 output offset voltage	-10	10	mV	RT	0.60	0.29	10.00	7.75	0.61	0.28	11.99	11.25	0.60	0.31	10.67	10.03
109	Sg9 output offset voltage	-10	10	mV	CT	-0.18	0.38	8.82	8.66	-0.18	0.38	8.68	8.52	-0.11	0.45	7.33	7.25
110	Sg10 output offset voltage	-10	10	mV	HT	1.84	0.31	10.86	8.87	1.81	0.33	10.08	8.26	1.85	0.33	10.05	8.19
110	Sg10 output offset voltage	-10	10	mV	RT	0.52	0.24	11.98	9.39	0.55	0.26	12.65	11.96	0.52	0.32	10.55	10.00
110	Sg10 output offset voltage	-10	10	mV	CT	-0.22	0.37	8.91	8.71	-0.17	0.38	8.85	8.70	-0.18	0.43	7.69	7.56
111	Sg11 output offset voltage	-10	10	mV	HT	1.83	0.31	10.87	8.88	1.86	0.30	11.11	9.04	1.88	0.35	9.41	7.65
111	Sg11 output offset voltage	-10	10	mV	RT	0.58	0.28	10.12	7.86	0.61	0.23	14.43	13.54	0.63	0.29	11.35	10.63
111	Sg11 output offset voltage	-10	10	mV	CT	-0.08	0.32	10.27	10.19	-0.09	0.38	8.78	8.70	-0.06	0.47	7.04	6.99
112	Sg112 output offset voltage	-10	10	mV	HT	1.83	0.30	11.14	9.11	1.85	0.35	9.56	7.79	1.85	0.37	9.09	7.41
112	Sg112 output offset voltage	-10	10	mV	RT	0.51	0.30	9.52	7.47	0.56	0.29	11.51	10.87	0.50	0.33	10.01	9.51
112	Sg112 output offset voltage	-10	10	mV	CT	-0.23	0.35	9.43	9.21	-0.18	0.34	9.91	9.73	-0.08	0.43	7.71	7.64
113	Sg13 output offset voltage	-10	10	mV	HT	1.75	0.27	12.33	10.17	1.80	0.31	10.77	8.83	1.77	0.37	9.11	7.49
113	Sg13 output offset voltage	-10	10	mV	RT	0.60	0.25	11.72	9.08	0.63	0.28	11.97	11.22	0.65	0.33	10.21	9.55
113	Sg13 output offset voltage	-10	10	mV	CT	-0.11	0.36	9.21	9.11	-0.10	0.39	8.53	8.45	-0.10	0.42	8.02	7.94
114	AMUX vol	-30	30	mV	HT	8.20	0.15	65.57	47.64	8.18	0.13	39.87	21.74	8.16	0.19	26.61	14.47
114	AMUX vol	-30	30	mV	RT	6.78	0.10	48.65	21.98	6.84	0.10	50.08	22.83	6.60	0.10	48.28	21.24
114	AMUX vol	-30	30	mV	CT	5.75	0.12	43.09	16.52	5.53	0.13	38.63	14.25	5.89	0.12	42.90	16.85
115	AMUX voh	4.9	5.1	V	HT	4.93	0.00	35.05	9.64	4.93	0.00	44.04	11.96	4.93	0.00	32.07	8.76
115	AMUX voh	4.9	5.1	V	RT	4.95	0.00	96.77	44.98	4.95	0.00	96.52	44.62	4.95	0.00	108.04	50.11
115	AMUX voh	4.9	5.1	V	CT	4.96	0.00	80.87	46.49	4.96	0.00	132.85	76.20	4.96	0.00	69.36	39.84
116	Sp0 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
116	Sp0 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
116	Sp0 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
117	Sp1 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
117	Sp1 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
117	Sp1 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
118	Sp2 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
118	Sp2 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
118	Sp2 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
119	Sp3 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
119	Sp3 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
119	Sp3 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
120	Sp4 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
120	Sp4 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
120	Sp4 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
121	Sp5 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
121	Sp5 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
121	Sp5 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
122	Sp6 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
122	Sp6 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
122	Sp6 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
123	Sp7 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
123	Sp7 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
123	Sp7 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		

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Electrical Distribution Report

						Lot1				Lot2				Lot3			
Test#	Test Name	Lo Limit	Hi Limit	Unit	Temp	Mean	Std Dev	Cp	Cpk	Mean	Std Dev	Cp	Cpk	Mean	Std Dev	Cp	Cpk
124	Sg0 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
124	Sg0 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
124	Sg0 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
125	Sg1 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
125	Sg1 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
125	Sg1 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
126	Sg2 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
126	Sg2 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
126	Sg2 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
127	Sg3 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
127	Sg3 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
127	Sg3 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
128	Sg4 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
128	Sg4 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
128	Sg4 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
129	Sg5 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
129	Sg5 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
129	Sg5 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
130	Sg6 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
130	Sg6 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
130	Sg6 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
131	Sg7 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
131	Sg7 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
131	Sg7 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
132	Sg8 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
132	Sg8 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
132	Sg8 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
133	Sg9 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
133	Sg9 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
133	Sg9 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
134	Sg10 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
134	Sg10 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
134	Sg10 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
135	Sg11 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
135	Sg11 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
135	Sg11 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
136	Sg12 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
136	Sg12 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
136	Sg12 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
137	Sg13 Vth	1			HT	1.00	0.00			1.00	0.00			1.00	0.00		
137	Sg13 Vth	1			RT	1.00	0.00			1.00	0.00			1.00	0.00		
137	Sg13 Vth	1			CT	1.00	0.00			1.00	0.00			1.00	0.00		
169	SCLK to VDDQ lkg	-10	10	uA	HT	0.00	0.00	3905.33	3903.57	0.00	0.00	4020.88	4019.16	0.00	0.00	799.16	762.85
169	SCLK to VDDQ lkg	-10	10	uA	RT	0.00	0.00	3319.62	3319.11	0.00	0.00	3890.78	3890.18	0.00	0.00	3817.19	3816.69
169	SCLK to VDDQ lkg	-10	10	uA	CT	0.00	0.00	5126.08	5125.22	0.00	0.00	4181.85	4181.20	0.00	0.00	4778.82	4778.13
170	SI to VDDQ lkg	-10	10	uA	HT	0.01	0.00	4617.66	4613.52	0.01	0.00	4399.03	4395.14	0.01	0.00	743.35	710.90
170	SI to VDDQ lkg	-10	10	uA	RT	0.00	0.00	2779.66	2778.73	0.00	0.00	2774.13	2773.29	0.00	0.00	3021.26	3020.33
170	SI to VDDQ lkg	-10	10	uA	CT	0.00	0.00	3562.81	3561.80	0.00	0.00	2800.15	2799.34	0.00	0.00	2884.98	2884.17
171	SO to VDDQ lkg	-10	10	uA	HT	0.01	0.00	4029.42	4025.56	0.01	0.00	4950.42	4945.67	0.01	0.00	840.84	804.47
171	SO to VDDQ lkg	-10	10	uA	RT	0.00	0.00	4113.93	4112.19	0.00	0.00	3888.17	3886.37	0.00	0.00	3655.81	3654.16
171	SO to VDDQ lkg	-10	10	uA	CT	0.00	0.00	3420.58	3419.29	0.00	0.00	2957.33	2956.19	0.00	0.00	3696.07	3694.45
172	SCLK to GND lkg	-10	10	uA	HT	-0.01	0.00	4610.94	4607.81	-0.01	0.00	4056.92	4054.19	-0.01	0.00	844.09	801.26
172	SCLK to GND lkg	-10	10	uA	RT	0.00	0.00	3771.43	3771.12	0.00	0.00	3037.48	3037.30	0.00	0.00	2983.93	2983.66
172	SCLK to GND lkg	-10	10	uA	CT	0.00	0.00	3473.57	3473.32	0.00	0.00	3931.77	3931.58	0.00	0.00	3477.99	3477.70
173	SI to GND lkg	-10	10	uA	HT	0.00	0.00	4553.59	4551.41	0.00	0.00	4449.75	4447.75	0.00	0.00	1016.97	970.62
173	SI to GND lkg	-10	10	uA	RT	0.00	0.00	4036.84	4035.06	0.00	0.00	4318.07	4316.31	0.00	0.00	4343.79	4341.82
173	SI to GND lkg	-10	10	uA	CT	0.00	0.00	3832.37	3830.91	0.00	0.00	3901.58	3900.12	0.00	0.00	5010.25	5008.26
174	SO to GND lkg	-10	10	uA	HT	0.00	0.00	5584.12	5581.58	0.00	0.00	4359.68	4357.77	0.00	0.00	1027.52	980.49
174	SO to GND lkg	-10	10	uA	RT	0.00	0.00	4659.42	4657.42	0.00	0.00	4814.58	4812.50	0.00	0.00	3815.81	3814.11
174	SO to GND lkg	-10	10	uA	CT	0.00	0.00	3815.67	3814.29	0.00	0.00	4360.30	4358.62	0.00	0.00	3727.76	3726.24

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Electrical Distribution Report

						Lot1				Lot2				Lot3			
Test#	Test Name	Lo Limit	Hi Limit	Unit	Temp	Mean	Std Dev	Cp	Cpk	Mean	Std Dev	Cp	Cpk	Mean	Std Dev	Cp	Cpk
175	CSB input current vdd=5v	-10	10	uA	HT	1.09	0.03	111.05	98.97	1.10	0.03	131.70	117.16	1.09	0.03	24.17	12.73
175	CSB input current vdd=5v	-10	10	uA	RT	1.22	0.04	77.77	68.26	1.24	0.04	84.73	74.20	1.23	0.04	78.76	69.11
175	CSB input current vdd=5v	-10	10	uA	CT	1.11	0.05	69.16	61.48	1.12	0.05	69.11	61.36	1.11	0.05	66.56	59.15
176	CSB pull-up current	-100	-30	uA	HT	-54.05	1.51	7.72	5.30	-55.28	1.05	7.11	6.26	-54.51	1.14	6.55	6.00
176	CSB pull-up current	-100	-30	uA	RT	-55.94	1.77	6.60	4.89	-57.20	1.34	8.67	6.70	-56.33	1.43	8.15	6.13
176	CSB pull-up current	-100	-30	uA	CT	-51.47	1.92	6.09	3.74	-52.65	1.44	5.22	5.19	-52.00	1.57	7.39	4.61
177	SO High State output voltage	4.8	5	V	HT	4.99	0.00	386.36	29.69	4.99	0.00	350.32	27.42	4.99	0.00	344.15	26.07
177	SO High State output voltage	4.8	5	V	RT	4.99	0.00	418.67	27.27	4.99	0.00	436.78	27.11	4.99	0.00	346.01	21.99
177	SO High State output voltage	4.8	5	V	CT	4.99	0.00	252.30	14.11	4.99	0.00	285.13	15.82	4.99	0.00	279.60	15.05
178	SO low state voltage	-400	400	mV	HT	70.62	0.33	34.93	29.33	70.18	0.32	36.89	31.44	70.42	0.35	33.18	28.04
178	SO low state voltage	-400	400	mV	RT	63.94	0.27	43.09	41.79	63.62	0.38	30.50	29.30	63.34	0.32	208.92	66.16
178	SO low state voltage	-400	400	mV	CT	59.38	0.36	184.29	54.71	58.36	0.50	28.59	28.01	59.67	0.43	154.02	45.96
179	INTB pull-up current	-100	-15	uA	HT	-25.01	0.57	24.71	5.82	-24.90	0.53	10.96	5.61	-24.79	0.62	9.63	5.27
179	INTB pull-up current	-100	-15	uA	RT	-42.36	0.87	16.30	10.49	-42.29	0.89	14.91	8.31	-42.10	0.95	14.05	7.76
179	INTB pull-up current	-100	-15	uA	CT	-64.19	1.49	9.52	8.02	-63.84	1.32	10.11	9.14	-63.72	1.53	8.71	7.90
180	INTB open	4.5	5.1	V	HT	5.00	0.00	910.60	8.71	5.00	0.00	163.71	55.93	5.00	0.00	932.23	318.12
180	INTB open	4.5	5.1	V	RT	5.00	0.00	1189.18	401.58	5.00	0.00	1329.09	448.76	5.00	0.00	1011.89	341.53
180	INTB open	4.5	5.1	V	CT	5.00	0.00	1202.34	405.60	5.00	0.00	829.82	4.15	5.00	0.00	1096.98	369.96
181	INTB voltage@1ma	-400	400	mV	HT	282.15	4.51	5.54	5.02	284.24	4.28	5.85	5.13	283.61	5.35	12.46	7.25
181	INTB voltage@1ma	-400	400	mV	RT	207.62	1.95	34.21	32.90	209.54	1.93	21.56	10.27	208.32	1.70	39.29	37.66
181	INTB voltage@1ma	-400	400	mV	CT	164.10	2.69	17.38	5.47	165.02	1.65	13.14	9.10	165.48	3.35	19.88	16.45
182	WAKEB pull-up current	-100	-20	uA	HT	-43.19	0.87	15.24	8.84	-43.59	1.22	10.90	6.43	-43.15	1.64	8.12	4.70
182	WAKEB pull-up current	-100	-20	uA	RT	-43.31	0.73	18.20	10.60	-44.09	0.76	17.55	10.57	-42.46	0.80	16.59	9.31
182	WAKEB pull-up current	-100	-20	uA	CT	-38.93	0.88	6.99	6.02	-38.15	0.77	8.03	6.57	-39.88	1.24	10.77	5.35
183	WAKEB voltage(open)	4	5.3	V	HT	4.85	0.01	12.28	8.25	4.85	0.02	9.83	6.50	4.85	0.01	13.47	9.05
183	WAKEB voltage(open)	4	5.3	V	RT	4.74	0.01	11.82	8.55	4.75	0.02	9.48	6.72	4.75	0.01	18.88	13.44
183	WAKEB voltage(open)	4	5.3	V	CT	4.60	0.01	12.09	11.38	4.61	0.02	9.47	8.77	4.60	0.01	14.35	13.35
184	WAKEB voltage 1ma load	-400	400	mV	HT	314.02	1.67	39.80	17.11	312.61	1.93	25.91	15.09	314.39	2.05	15.48	9.06
184	WAKEB voltage 1ma load	-400	400	mV	RT	279.13	1.57	15.37	9.72	277.15	1.70	39.19	24.07	278.76	1.75	38.20	23.16
184	WAKEB voltage 1ma load	-400	400	mV	CT	257.93	1.79	11.61	8.74	256.19	1.72	12.14	9.48	258.38	1.94	34.32	24.30
186	SP0 wetting current pulse	15	20	ms	HT	18.88	0.03	25.19	11.27	18.87	0.04	22.67	10.25	18.88	0.04	20.32	9.10
186	SP0 wetting current pulse	15	20	ms	RT	18.89	0.04	20.50	9.09	18.90	0.04	22.43	9.86	18.90	0.04	21.79	9.56
186	SP0 wetting current pulse	15	20	ms	CT	18.92	0.04	21.95	9.44	18.93	0.03	24.73	10.62	18.93	0.05	12.89	7.95
187	SP1 wetting current pulse	15	20	ms	HT	17.23	0.03	27.19	24.29	17.25	0.04	21.80	19.62	17.25	0.04	19.54	17.58
187	SP1 wetting current pulse	15	20	ms	RT	17.24	0.03	25.31	22.68	17.24	0.03	16.67	6.88	17.26	0.03	25.37	22.88
187	SP1 wetting current pulse	15	20	ms	CT	17.24	0.04	20.43	18.34	17.26	0.04	21.28	19.21	17.25	0.04	16.47	6.87
188	SP2 wetting current pulse	15	20	ms	HT	17.26	0.04	22.57	20.41	17.26	0.03	25.77	23.32	17.27	0.04	22.57	20.51
188	SP2 wetting current pulse	15	20	ms	RT	17.25	0.04	21.02	18.93	17.27	0.03	16.82	7.21	17.26	0.04	21.37	19.35
188	SP2 wetting current pulse	15	20	ms	CT	17.26	0.03	28.29	25.62	17.27	0.03	25.98	23.55	17.27	0.04	15.51	6.66
189	SP3 wetting current pulse	15	20	ms	HT	17.25	0.05	17.89	16.12	17.25	0.04	20.65	18.57	17.24	0.04	20.76	18.59
189	SP3 wetting current pulse	15	20	ms	RT	17.25	0.04	20.94	18.85	17.25	0.04	14.79	6.17	17.24	0.04	19.33	17.35
189	SP3 wetting current pulse	15	20	ms	CT	17.24	0.04	21.47	19.24	17.25	0.04	20.18	18.19	17.25	0.04	15.76	6.64
190	SP4 wetting current pulse	15	20	ms	HT	18.86	0.04	23.04	10.53	18.86	0.04	19.32	8.83	18.85	0.04	20.01	9.22
190	SP4 wetting current pulse	15	20	ms	RT	18.87	0.04	19.60	8.84	18.87	0.04	15.95	10.32	18.88	0.05	18.50	8.26
190	SP4 wetting current pulse	15	20	ms	CT	18.90	0.05	18.23	8.05	18.91	0.04	23.80	10.38	18.90	0.04	12.96	8.22
191	SP5 wetting current pulse	15	20	ms	HT	18.86	0.04	23.04	10.53	18.86	0.04	19.32	8.83	18.85	0.04	20.01	9.22
191	SP5 wetting current pulse	15	20	ms	RT	18.87	0.04	19.60	8.84	18.87	0.04	15.95	10.32	18.88	0.05	18.50	8.26
191	SP5 wetting current pulse	15	20	ms	CT	18.90	0.05	18.23	8.05	18.91	0.04	23.80	10.38	18.90	0.04	12.96	8.22
192	SP6 wetting current pulse	15	20	ms	HT	18.87	0.04	20.15	9.15	18.87	0.04	21.59	9.75	18.87	0.04	19.64	8.84
192	SP6 wetting current pulse	15	20	ms	RT	18.91	0.04	23.31	10.14	18.90	0.05	12.89	8.12	18.91	0.04	22.29	9.73
192	SP6 wetting current pulse	15	20	ms	CT	18.92	0.04	20.79	9.00	18.93	0.04	21.66	9.27	18.92	0.04	13.34	8.27
193	SP7 wetting current pulse	15	20	ms	HT	18.84	0.03	25.37	11.74	18.84	0.03	24.96	11.53	18.85	0.04	21.83	10.05
193	SP7 wetting current pulse	15	20	ms	RT	18.87	0.04	21.43	9.72	18.87	0.04	15.26	9.89	18.87	0.04	19.35	8.77
193	SP7 wetting current pulse	15	20	ms	CT	18.89	0.04	23.80	10.58	18.89	0.04	22.35	9.88	18.89	0.04	15.23	9.75
194	SG0 wetting current pulse	15	20	ms	HT	18.80	0.04	22.49	10.80	18.80	0.03	24.84	11.92	18.79	0.04	20.68	10.04
194	SG0 wetting current pulse	15	20	ms	RT	18.82	0.04	21.42	10.08	18.82	0.04	15.62	10.61	18.81	0.04	23.60	11.19
194	SG0 wetting current pulse	15	20	ms	CT	18.85	0.04	23.47	10.82	18.84	0.04	23.15	10.71	18.83	0.04	13.50	9.05
195	SG1 wetting current pulse	15	20	ms	HT	17.24	0.04	20.18	18.11	17.24	0.04	20.38	18.27	17.25	0.04	23.09	20.82
195	SG1 wetting current pulse	15	20	ms	RT	17.25	0.04	20.76	18.70	17.25	0.04	15.79	6.58	17.26	0.04	20.87	18.85
195	SG1 wetting current pulse	15	20	ms	CT	17.26	0.03	25.79	23.30	17.25	0.04	20.11	18.07	17.26	0.04	15.97	6.78

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Electrical Distribution Report

Test#	Test Name	Lo Limit	Hi Limit	Unit	Temp	Lot1				Lot2				Lot3			
						Mean	Std Dev	Cp	Cpk	Mean	Std Dev	Cp	Cpk	Mean	Std Dev	Cp	Cpk
196	SG2 wetting current pulse	15	20	ms	HT	18.97	0.03	24.38	10.08	18.97	0.04	18.96	2.95	18.97	0.03	24.17	9.91
196	SG2 wetting current pulse	15	20	ms	RT	19.00	0.04	21.62	8.67	19.00	0.04	15.90	9.15	19.02	0.04	21.18	8.29
196	SG2 wetting current pulse	15	20	ms	CT	19.02	0.04	19.85	7.80	19.02	0.04	20.61	8.06	19.02	0.04	14.97	8.46
197	SG3 wetting current pulse	15	20	ms	HT	17.24	0.04	21.89	19.57	17.25	0.04	20.91	18.79	17.24	0.05	18.17	16.27
197	SG3 wetting current pulse	15	20	ms	RT	17.23	0.04	18.86	16.85	17.22	0.04	14.48	5.85	17.24	0.04	20.93	18.73
197	SG3 wetting current pulse	15	20	ms	CT	17.24	0.04	20.60	18.45	17.24	0.04	21.01	18.87	17.24	0.04	14.93	6.14
198	SG4 wetting current pulse	15	20	ms	HT	18.93	0.03	27.42	11.76	18.93	0.04	23.39	9.97	18.94	0.03	25.98	11.05
198	SG4 wetting current pulse	15	20	ms	RT	18.97	0.03	25.66	10.55	18.97	0.04	15.87	9.41	18.98	0.03	24.09	9.84
198	SG4 wetting current pulse	15	20	ms	CT	19.00	0.03	24.75	9.91	18.99	0.04	15.91	9.28	18.99	0.04	16.49	9.56
199	SG5 wetting current pulse	15	20	ms	HT	18.85	0.04	19.54	8.95	18.86	0.04	20.15	9.21	18.86	0.04	20.28	9.23
199	SG5 wetting current pulse	15	20	ms	RT	18.89	0.04	21.07	9.38	18.87	0.04	15.55	10.09	18.88	0.04	21.79	9.78
199	SG5 wetting current pulse	15	20	ms	CT	18.90	0.04	22.69	10.01	18.90	0.04	22.37	9.86	18.91	0.04	14.43	9.00
200	SG6 wetting current pulse	15	20	ms	HT	18.76	0.04	19.80	9.85	18.75	0.04	20.58	10.33	18.74	0.04	19.79	9.94
200	SG6 wetting current pulse	15	20	ms	RT	18.78	0.04	19.05	9.33	18.77	0.04	15.44	10.96	18.77	0.04	18.96	9.33
200	SG6 wetting current pulse	15	20	ms	CT	18.78	0.04	23.76	11.57	18.79	0.04	15.65	10.91	18.80	0.04	14.06	9.72
201	SG7 wetting current pulse	15	20	ms	HT	18.78	0.04	21.85	10.64	18.77	0.04	22.49	11.07	18.78	0.04	20.83	10.15
201	SG7 wetting current pulse	15	20	ms	RT	18.82	0.04	22.13	10.48	18.82	0.03	18.04	12.24	18.80	0.04	22.26	10.66
201	SG7 wetting current pulse	15	20	ms	CT	18.83	0.04	23.56	11.02	18.84	0.04	13.72	9.18	18.81	0.04	14.34	9.77
202	SG8 wetting current pulse	15	20	ms	HT	18.78	0.04	22.41	10.92	18.78	0.04	19.80	9.63	18.78	0.04	20.18	9.89
202	SG8 wetting current pulse	15	20	ms	RT	18.81	0.04	21.36	10.15	18.81	0.04	16.35	11.22	18.81	0.04	20.30	9.63
202	SG8 wetting current pulse	15	20	ms	CT	18.85	0.03	24.75	11.42	18.84	0.03	17.21	11.49	18.84	0.04	15.86	10.57
203	SG9 wetting current pulse	15	20	ms	HT	18.93	0.04	21.68	9.26	18.93	0.04	22.61	9.70	18.93	0.04	20.49	8.80
203	SG9 wetting current pulse	15	20	ms	RT	18.95	0.03	25.36	10.66	18.95	0.04	13.40	8.05	18.95	0.04	19.29	8.07
203	SG9 wetting current pulse	15	20	ms	CT	18.98	0.04	23.34	9.48	18.98	0.03	16.96	9.98	18.98	0.04	14.87	8.68
204	SG10 wetting current pulse	15	20	ms	HT	18.77	0.04	18.58	9.12	18.78	0.04	22.55	11.03	18.78	0.04	20.91	10.17
204	SG10 wetting current pulse	15	20	ms	RT	18.80	0.04	20.14	9.63	18.80	0.04	14.54	10.06	18.79	0.04	18.87	9.13
204	SG10 wetting current pulse	15	20	ms	CT	18.84	0.04	21.57	10.05	18.82	0.04	12.22	4.22	18.82	0.04	13.99	9.47
205	SG11 wetting current pulse	15	20	ms	HT	18.94	0.03	23.87	10.10	18.95	0.04	16.03	9.66	18.94	0.04	20.68	8.79
205	SG11 wetting current pulse	15	20	ms	RT	18.97	0.04	20.49	8.41	18.98	0.04	15.52	9.13	18.97	0.03	26.70	11.00
205	SG11 wetting current pulse	15	20	ms	CT	18.98	0.04	21.94	8.91	19.00	0.04	13.95	7.98	18.99	0.04	15.19	8.79
206	SG12 wetting current pulse	15	20	ms	HT	18.85	0.04	22.46	10.32	18.84	0.04	22.16	10.25	18.85	0.04	19.93	9.18
206	SG12 wetting current pulse	15	20	ms	RT	18.88	0.04	21.06	9.41	18.89	0.03	16.73	10.70	18.88	0.04	23.08	10.35
206	SG12 wetting current pulse	15	20	ms	CT	18.90	0.04	21.39	9.37	18.89	0.04	14.61	9.30	18.91	0.03	16.66	10.43
207	SG13 wetting current pulse	15	20	ms	HT	18.89	0.04	23.15	10.25	18.90	0.04	22.63	9.99	18.89	0.04	23.19	10.32
207	SG13 wetting current pulse	15	20	ms	RT	18.92	0.04	21.09	9.11	18.92	0.04	14.96	9.29	18.92	0.04	22.87	9.89
207	SG13 wetting current pulse	15	20	ms	CT	18.93	0.04	20.66	8.88	18.94	0.04	14.04	8.57	18.95	0.04	15.43	9.34
208	Interrupt delay time	-16	16	us	HT	5.97	2.55	2.09	1.31	5.19	2.38	2.24	1.51	5.66	2.68	1.99	1.28
208	Interrupt delay time	-16	16	us	RT	5.30	2.31	2.31	1.54	4.79	2.58	2.33	1.97	5.26	2.49	2.14	1.44
208	Interrupt delay time	-16	16	us	CT	5.21	2.89	1.84	1.24	4.84	2.70	1.97	1.38	5.62	2.59	2.06	1.34
317	SP0 to mux 16ma	-18	-12	mA	HT	-16.02	0.12	8.04	5.30	-16.05	0.16	3.96	3.96	-16.08	0.12	5.35	5.28
317	SP0 to mux 16ma	-18	-12	mA	RT	-16.11	0.13	7.99	5.03	-16.10	0.17	3.91	3.80	-16.16	0.14	4.53	4.28
317	SP0 to mux 16ma	-18	-12	mA	CT	-15.85	0.16	6.13	4.39	-15.81	0.18	5.47	3.99	-15.89	0.16	6.07	4.27
318	SP1 to mux 16ma	-18	-12	mA	HT	-15.98	0.13	7.49	5.05	-15.99	0.15	4.46	4.33	-16.03	0.12	5.22	5.18
318	SP1 to mux 16ma	-18	-12	mA	RT	-16.08	0.14	7.30	4.68	-16.05	0.14	4.66	4.66	-16.11	0.13	5.00	4.85
318	SP1 to mux 16ma	-18	-12	mA	CT	-15.81	0.17	5.81	4.25	-15.76	0.17	6.06	4.53	-15.83	0.16	6.36	4.60
319	SP2 to mux 16ma	-18	-12	mA	HT	-15.98	0.14	7.07	4.75	-16.01	0.15	4.20	4.11	-16.03	0.12	5.52	5.45
319	SP2 to mux 16ma	-18	-12	mA	RT	-16.08	0.14	7.22	4.63	-16.06	0.15	4.32	4.30	-16.09	0.13	4.82	4.73
319	SP2 to mux 16ma	-18	-12	mA	CT	-15.79	0.17	5.90	4.35	-15.75	0.17	6.06	4.55	-15.79	0.16	6.13	4.51
320	SP3 to mux 16ma	-18	-12	mA	HT	-15.95	0.15	6.88	4.70	-15.97	0.17	3.92	3.77	-16.01	0.14	4.73	4.64
320	SP3 to mux 16ma	-18	-12	mA	RT	-16.02	0.14	7.04	4.63	-16.01	0.15	4.27	4.17	-16.07	0.15	4.20	4.16
320	SP3 to mux 16ma	-18	-12	mA	CT	-15.75	0.18	5.71	4.29	-15.69	0.18	5.64	4.33	-15.78	0.18	5.48	4.06
321	SP4 to mux 16ma	-18	-12	mA	HT	-15.93	0.12	8.08	5.56	-16.00	0.15	4.29	4.19	-15.99	0.14	4.68	4.54
321	SP4 to mux 16ma	-18	-12	mA	RT	-16.02	0.12	8.33	5.51	-16.07	0.16	4.01	3.97	-16.08	0.16	4.06	4.00
321	SP4 to mux 16ma	-18	-12	mA	CT	-15.74	0.16	6.45	4.85	-15.76	0.18	5.41	4.03	-15.77	0.19	5.37	3.99
322	SP5 to mux 16ma	-18	-12	mA	HT	-15.93	0.12	8.08	5.58	-15.97	0.17	3.90	3.73	-15.98	0.11	5.84	5.62
322	SP5 to mux 16ma	-18	-12	mA	RT	-16.01	0.14	7.39	4.89	-16.02	0.15	4.21	4.14	-16.04	0.13	4.93	4.90
322	SP5 to mux 16ma	-18	-12	mA	CT	-15.75	0.16	6.19	4.64	-15.72	0.17	5.93	4.50	-15.76	0.16	6.42	4.78
323	SP6 to mux 16ma	-18	-12	mA	HT	-15.95	0.14	7.10	4.86	-16.00	0.16	4.13	4.03	-16.00	0.11	5.71	5.57
323	SP6 to mux 16ma	-18	-12	mA	RT	-16.05	0.13	7.63	4.96	-16.07	0.15	4.33	4.30	-16.06	0.12	5.23	5.20
323	SP6 to mux 16ma	-18	-12	mA	CT	-15.78	0.16	6.40	4.75	-15.77	0.18	5.47	4.07	-15.80	0.16	6.25	4.59

Freescale Confidential Proprietary

Electrical Distribution Report

Test#	Test Name	Lo Limit	Hi Limit	Unit	Temp	Lot1				Lot2				Lot3			
						Mean	Std Dev	Cp	Cpk	Mean	Std Dev	Cp	Cpk	Mean	Std Dev	Cp	Cpk
324	SP7 to mux 16ma	-18	-12	mA	HT	-15.97	0.15	6.87	4.66	-16.01	0.15	4.20	4.12	-16.02	0.11	5.66	5.57
324	SP7 to mux 16ma	-18	-12	mA	RT	-16.07	0.15	6.54	4.21	-16.09	0.16	4.17	4.09	-16.10	0.13	5.04	4.90
324	SP7 to mux 16ma	-18	-12	mA	CT	-15.81	0.17	5.86	4.28	-15.81	0.17	5.72	4.17	-15.85	0.14	7.11	5.11
325	SG0 to mux 16ma	-18	-12	mA	HT	-16.05	0.14	7.07	4.61	-16.06	0.15	4.26	4.24	-16.09	0.12	5.58	5.48
325	SG0 to mux 16ma	-18	-12	mA	RT	-16.10	0.14	7.36	4.65	-16.10	0.14	4.58	4.47	-16.14	0.13	4.90	4.68
325	SG0 to mux 16ma	-18	-12	mA	CT	-15.81	0.17	5.84	4.26	-15.78	0.16	6.25	4.63	-15.84	0.16	6.41	4.62
326	SG1 to mux 16ma	-18	-12	mA	HT	-15.98	0.14	7.14	4.80	-15.99	0.17	3.84	3.72	-16.04	0.12	5.21	5.18
326	SG1 to mux 16ma	-18	-12	mA	RT	-16.04	0.14	7.03	4.59	-16.01	0.16	4.18	4.08	-16.08	0.14	4.53	4.46
326	SG1 to mux 16ma	-18	-12	mA	CT	-15.74	0.17	5.90	4.44	-15.68	0.18	5.57	4.30	-15.77	0.17	5.83	4.34
327	SG2 to mux 16ma	-18	-12	mA	HT	-15.97	0.13	7.59	5.14	-16.01	0.17	3.85	3.77	-16.03	0.13	4.92	4.88
327	SG2 to mux 16ma	-18	-12	mA	RT	-16.02	0.13	7.48	4.93	-16.04	0.17	3.84	3.81	-16.09	0.15	4.39	4.31
327	SG2 to mux 16ma	-18	-12	mA	CT	-15.73	0.17	5.99	4.53	-15.71	0.19	5.39	4.12	-15.77	0.17	6.04	4.48
328	SG3 to mux 16ma	-18	-12	mA	HT	-16.02	0.13	7.80	5.15	-16.04	0.16	4.19	4.17	-16.08	0.12	5.22	5.14
328	SG3 to mux 16ma	-18	-12	mA	RT	-16.09	0.13	7.82	4.99	-16.09	0.15	4.42	4.34	-16.14	0.14	4.61	4.39
328	SG3 to mux 16ma	-18	-12	mA	CT	-15.80	0.15	6.45	4.74	-15.77	0.17	5.90	4.38	-15.85	0.17	6.03	4.33
329	SG4 to mux 16ma	-18	-12	mA	HT	-15.96	0.13	7.99	5.44	-16.01	0.16	4.16	4.07	-16.02	0.13	4.96	4.88
329	SG4 to mux 16ma	-18	-12	mA	RT	-16.04	0.13	7.84	5.11	-16.07	0.16	4.16	4.11	-16.10	0.15	4.21	4.10
329	SG4 to mux 16ma	-18	-12	mA	CT	-15.77	0.15	6.66	4.96	-15.77	0.18	5.61	4.17	-15.81	0.19	5.38	3.92
330	SG5 to mux 16ma	-18	-12	mA	HT	-15.95	0.13	7.86	5.38	-16.00	0.16	4.07	3.96	-16.01	0.12	5.41	5.29
330	SG5 to mux 16ma	-18	-12	mA	RT	-16.03	0.13	7.85	5.16	-16.05	0.16	4.12	4.11	-16.07	0.12	5.21	5.16
330	SG5 to mux 16ma	-18	-12	mA	CT	-15.75	0.17	6.02	4.51	-15.75	0.18	5.62	4.21	-15.77	0.15	6.75	5.01
331	SG6 to mux 16ma	-18	-12	mA	HT	-16.00	0.14	7.30	4.87	-16.07	0.17	3.76	3.73	-16.07	0.12	5.27	5.23
331	SG6 to mux 16ma	-18	-12	mA	RT	-16.11	0.13	7.52	4.75	-16.15	0.17	3.84	3.63	-16.17	0.13	5.10	4.77
331	SG6 to mux 16ma	-18	-12	mA	CT	-15.85	0.16	6.39	4.57	-15.86	0.18	5.62	4.00	-15.89	0.15	6.54	4.59
332	SG7 to mux 16ma	-18	-12	mA	HT	-15.92	0.13	7.96	5.51	-15.97	0.15	4.41	4.24	-15.99	0.11	5.85	5.66
332	SG7 to mux 16ma	-18	-12	mA	RT	-16.02	0.12	8.34	5.51	-16.04	0.14	4.58	4.55	-16.07	0.13	4.92	4.86
332	SG7 to mux 16ma	-18	-12	mA	CT	-15.75	0.15	6.77	5.07	-15.75	0.17	5.98	4.48	-15.80	0.17	6.05	4.43
333	SG8 to mux 16ma	-18	-12	mA	HT	-15.89	0.13	7.56	5.31	-15.91	0.15	4.25	3.94	-15.95	0.13	4.87	4.63
333	SG8 to mux 16ma	-18	-12	mA	RT	-15.99	0.12	8.01	5.37	-15.97	0.14	4.57	4.37	-16.02	0.16	4.08	4.02
333	SG8 to mux 16ma	-18	-12	mA	CT	-15.71	0.16	6.07	4.65	-15.67	0.16	6.35	4.93	-15.73	0.19	5.27	3.99
334	SG9 to mux 16ma	-18	-12	mA	HT	-15.92	0.14	7.34	5.09	-15.96	0.14	4.52	4.32	-15.98	0.13	5.09	4.90
334	SG9 to mux 16ma	-18	-12	mA	RT	-16.01	0.12	8.09	5.38	-16.03	0.14	4.66	4.61	-16.06	0.14	4.75	4.73
334	SG9 to mux 16ma	-18	-12	mA	CT	-15.73	0.15	6.88	5.21	-15.73	0.16	6.23	4.72	-15.76	0.15	6.46	4.82
335	SG10 to mux 16ma	-18	-12	mA	HT	-15.91	0.13	7.73	5.39	-15.95	0.15	4.41	4.19	-16.00	0.12	5.44	5.29
335	SG10 to mux 16ma	-18	-12	mA	RT	-15.99	0.13	7.55	5.06	-16.02	0.14	4.59	4.51	-16.08	0.13	4.93	4.85
335	SG10 to mux 16ma	-18	-12	mA	CT	-15.71	0.16	6.14	4.69	-15.71	0.17	5.96	4.54	-15.79	0.16	6.28	4.63
336	SG11 to mux 16ma	-18	-12	mA	HT	-15.91	0.13	7.42	5.17	-15.97	0.14	4.65	4.45	-15.98	0.13	4.95	4.78
336	SG11 to mux 16ma	-18	-12	mA	RT	-16.00	0.13	7.46	4.97	-16.04	0.14	4.76	4.73	-16.08	0.14	4.71	4.65
336	SG11 to mux 16ma	-18	-12	mA	CT	-15.72	0.16	6.43	4.89	-15.75	0.16	6.40	4.79	-15.79	0.16	6.38	4.69
337	SG12 to mux 16ma	-18	-12	mA	HT	-15.92	0.13	7.59	5.26	-15.97	0.15	4.37	4.19	-15.99	0.12	5.32	5.14
337	SG12 to mux 16ma	-18	-12	mA	RT	-16.01	0.13	7.41	4.92	-16.03	0.15	4.41	4.37	-16.06	0.13	4.88	4.86
337	SG12 to mux 16ma	-18	-12	mA	CT	-15.73	0.16	6.12	4.62	-15.75	0.16	6.29	4.73	-15.78	0.15	6.62	4.89
338	SG13 to mux 16ma	-18	-12	mA	HT	-15.91	0.14	7.38	5.14	-15.97	0.15	4.42	4.24	-15.97	0.12	5.22	5.00
338	SG13 to mux 16ma	-18	-12	mA	RT	-16.02	0.14	7.39	4.87	-16.07	0.15	4.45	4.41	-16.08	0.12	5.20	5.13
338	SG13 to mux 16ma	-18	-12	mA	CT	-15.77	0.16	6.21	4.62	-15.78	0.16	6.12	4.53	-15.80	0.15	6.86	5.03
347	SP0 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	4.30	4.23	-2.00	0.02	3.41	3.27	-2.01	0.01	3.90	3.61
347	SP0 to mux 2ma	-2.2	-1.8	mA	RT	-2.01	0.01	3.96	3.69	-2.00	0.02	3.11	2.83	-2.01	0.02	3.55	3.24
347	SP0 to mux 2ma	-2.2	-1.8	mA	CT	-1.98	0.02	3.47	3.05	-1.97	0.02	3.15	2.72	-1.98	0.02	3.06	2.79
348	SP1 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.54	3.15	-2.00	0.02	3.43	3.32	-2.00	0.01	4.13	3.76
348	SP1 to mux 2ma	-2.2	-1.8	mA	RT	-2.01	0.02	3.34	3.11	-2.00	0.02	3.13	2.81	-2.01	0.02	4.30	3.98
348	SP1 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.05	2.73	-1.97	0.02	3.17	2.69	-1.97	0.02	3.68	3.27
349	SP2 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.21	2.87	-2.00	0.02	3.61	3.49	-2.00	0.01	4.09	3.71
349	SP2 to mux 2ma	-2.2	-1.8	mA	RT	-2.01	0.02	3.38	3.16	-2.00	0.02	3.34	3.02	-2.01	0.02	4.12	3.87
349	SP2 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.32	2.95	-1.97	0.02	3.48	2.96	-1.97	0.02	3.48	3.04
350	SP3 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.18	2.76	-2.00	0.02	3.30	3.27	-2.00	0.02	3.55	3.17
350	SP3 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.32	2.97	-2.00	0.02	3.12	2.72	-2.01	0.02	3.36	3.18
350	SP3 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.19	2.73	-1.96	0.02	3.03	2.47	-1.97	0.02	2.90	2.51
351	SP4 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.43	2.93	-2.00	0.02	3.51	3.40	-2.00	0.02	3.59	3.16
351	SP4 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.72	3.29	-2.01	0.02	2.99	2.73	-2.01	0.02	3.60	3.41
351	SP4 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.47	2.96	-1.97	0.02	3.12	2.68	-1.97	0.02	3.06	2.63

Freescale Confidential Proprietary

Electrical Distribution Report

						Lot1				Lot2				Lot3			
Test#	Test Name	Lo Limit	Hi Limit	Unit	Temp	Mean	Std Dev	Cp	Cpk	Mean	Std Dev	Cp	Cpk	Mean	Std Dev	Cp	Cpk
352	SP5 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.37	2.90	-2.00	0.02	3.41	3.39	-2.00	0.02	3.77	3.31
352	SP5 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.32	3.01	-2.00	0.02	3.48	3.04	-2.00	0.02	3.53	3.37
352	SP5 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.09	2.68	-1.96	0.02	3.59	2.99	-1.97	0.02	3.08	2.66
353	SP6 to mux 2ma	-2.2	-1.8	mA	HT	-1.99	0.02	3.16	2.66	-2.00	0.02	3.30	3.27	-2.00	0.01	4.10	3.54
353	SP6 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.46	3.07	-2.00	0.02	2.95	2.61	-2.00	0.02	4.26	4.14
353	SP6 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.42	2.93	-1.97	0.02	2.88	2.43	-1.97	0.02	3.27	2.81
354	SP7 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.15	2.70	-2.00	0.02	3.41	3.37	-2.00	0.01	3.85	3.42
354	SP7 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.14	2.84	-2.00	0.02	3.00	2.66	-2.01	0.02	3.77	3.55
354	SP7 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.11	2.74	-1.97	0.02	3.01	2.57	-1.97	0.02	3.28	2.92
355	SG0 to mux 2ma	-2.2	-1.8	mA	HT	-2.01	0.02	3.05	2.82	-2.01	0.02	3.53	3.33	-2.01	0.01	4.31	4.04
355	SG0 to mux 2ma	-2.2	-1.8	mA	RT	-2.01	0.02	3.26	3.08	-2.01	0.02	3.30	3.04	-2.01	0.02	4.14	3.76
355	SG0 to mux 2ma	-2.2	-1.8	mA	CT	-1.98	0.02	3.12	2.81	-1.97	0.02	3.42	2.94	-1.98	0.02	3.51	3.16
356	SG1 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.08	2.79	-2.00	0.02	3.24	3.09	-2.01	0.01	4.13	3.83
356	SG1 to mux 2ma	-2.2	-1.8	mA	RT	-2.01	0.02	3.12	2.88	-2.00	0.02	2.90	2.60	-2.01	0.02	3.99	3.69
356	SG1 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.33	2.92	-1.96	0.02	2.94	2.44	-1.97	0.02	3.27	2.86
357	SG2 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.26	2.95	-2.01	0.02	3.28	3.10	-2.01	0.02	3.51	3.26
357	SG2 to mux 2ma	-2.2	-1.8	mA	RT	-2.01	0.02	3.52	3.26	-2.01	0.02	2.92	2.69	-2.01	0.02	3.65	3.34
357	SG2 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.27	2.86	-1.97	0.02	2.95	2.52	-1.97	0.02	3.27	2.89
358	SG3 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.34	3.02	-2.01	0.02	3.42	3.21	-2.01	0.01	4.38	4.10
358	SG3 to mux 2ma	-2.2	-1.8	mA	RT	-2.01	0.02	3.55	3.31	-2.01	0.02	3.06	2.84	-2.01	0.02	4.29	3.88
358	SG3 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.50	3.08	-1.97	0.02	3.05	2.64	-1.98	0.02	3.48	3.15
359	SG4 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.38	3.02	-2.01	0.02	3.57	3.37	-2.00	0.01	3.85	3.51
359	SG4 to mux 2ma	-2.2	-1.8	mA	RT	-2.01	0.02	3.46	3.22	-2.01	0.02	3.18	2.99	-2.01	0.02	3.79	3.49
359	SG4 to mux 2ma	-2.2	-1.8	mA	CT	-1.98	0.02	3.39	3.05	-1.97	0.02	3.19	2.84	-1.97	0.02	3.17	2.84
360	SG5 to mux 2ma	-2.2	-1.8	mA	HT	-1.99	0.02	3.43	2.90	-2.00	0.02	3.32	3.27	-2.00	0.01	3.94	3.47
360	SG5 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.58	3.16	-2.00	0.02	2.83	2.51	-2.00	0.01	4.44	4.22
360	SG5 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.44	2.93	-1.96	0.02	2.88	2.42	-1.97	0.02	3.74	3.22
361	SG6 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.27	2.83	-2.00	0.02	3.36	3.28	-2.00	0.02	3.72	3.33
361	SG6 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.50	3.15	-2.00	0.02	3.13	2.81	-2.01	0.02	4.00	3.75
361	SG6 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.67	3.18	-1.97	0.02	3.30	2.79	-1.97	0.02	3.45	3.03
362	SG7 to mux 2ma	-2.2	-1.8	mA	HT	-2.00	0.02	3.36	2.95	-2.00	0.02	3.55	3.44	-2.00	0.01	4.01	3.62
362	SG7 to mux 2ma	-2.2	-1.8	mA	RT	-2.01	0.02	3.68	3.40	-2.01	0.02	3.24	2.97	-2.01	0.02	3.85	3.56
362	SG7 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.48	3.11	-1.97	0.02	3.20	2.79	-1.98	0.02	3.11	2.79
363	SG8 to mux 2ma	-2.2	-1.8	mA	HT	-1.99	0.02	3.31	2.75	-1.99	0.02	3.48	3.42	-2.00	0.02	3.58	3.07
363	SG8 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.63	3.19	-1.99	0.02	3.40	2.90	-2.00	0.02	3.37	3.27
363	SG8 to mux 2ma	-2.2	-1.8	mA	CT	-1.96	0.02	3.21	2.70	-1.96	0.02	3.53	2.87	-1.97	0.02	2.77	2.36
364	SG9 to mux 2ma	-2.2	-1.8	mA	HT	-1.99	0.02	3.32	2.79	-2.00	0.02	3.78	3.75	-2.00	0.02	3.54	3.08
364	SG9 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.53	3.10	-2.00	0.01	3.83	3.40	-2.00	0.02	3.59	3.43
364	SG9 to mux 2ma	-2.2	-1.8	mA	CT	-1.96	0.02	3.54	2.99	-1.97	0.02	3.87	3.28	-1.97	0.02	3.19	2.75
365	SG10 to mux 2ma	-2.2	-1.8	mA	HT	-1.99	0.02	3.42	2.88	-2.00	0.02	3.60	3.54	-2.00	0.01	3.82	3.37
365	SG10 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.37	2.97	-2.00	0.02	3.15	2.82	-2.01	0.02	3.76	3.52
365	SG10 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.35	2.85	-1.97	0.02	3.10	2.63	-1.97	0.02	3.06	2.70
366	SG11 to mux 2ma	-2.2	-1.8	mA	HT	-1.99	0.02	3.38	2.84	-2.00	0.02	3.80	3.74	-2.00	0.01	3.82	3.36
366	SG11 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.54	3.12	-2.00	0.02	3.38	3.03	-2.01	0.02	3.96	3.73
366	SG11 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.43	2.92	-1.97	0.02	3.44	2.94	-1.97	0.02	3.26	2.86
367	SG12 to mux 2ma	-2.2	-1.8	mA	HT	-1.99	0.02	3.56	2.96	-1.99	0.02	3.65	3.63	-1.99	0.01	4.04	3.43
367	SG12 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.76	3.30	-2.00	0.02	3.08	2.68	-2.00	0.02	4.21	4.09
367	SG12 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.64	3.09	-1.96	0.02	3.28	2.74	-1.97	0.02	3.49	2.96
368	SG13 to mux 2ma	-2.2	-1.8	mA	HT	-1.99	0.02	3.41	2.87	-2.00	0.02	3.53	3.51	-2.00	0.01	3.89	3.38
368	SG13 to mux 2ma	-2.2	-1.8	mA	RT	-2.00	0.02	3.72	3.27	-2.00	0.02	3.23	2.83	-2.00	0.02	3.97	3.80
368	SG13 to mux 2ma	-2.2	-1.8	mA	CT	-1.97	0.02	3.59	3.07	-1.96	0.02	3.28	2.75	-1.97	0.02	3.14	2.70

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Initial Process Study

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• The PPAP documents are pulled by Freescale External Manufacturing Quality and checked for compliance with TS16949 requirements.

• For special requests, Freescale may be able to review these documents on a limited basis with customers at the local Freescale sales office.

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Manufacturing Capability Report

Company/Manufacturing Site ID:		Freescale / FSL-TJN-FM
Report Date:		17/Dec /13
Designate with an "X" only one of the following boxes and enter the applicable information:		
☒	Cpk Reporting Period:	Nov'2013
☐	Preliminary Ppk - Lot Number:	
Designate with an "X" only one of the following boxes and enter the applicable information :		
☐	Wafer Fab Process Technology:	
☒	Assembly Process Package Family:	SOIC 32ld EP
	Assembly Process Package Drawing #:	98ARL10543D_D 98ARH99137A_B

Special/Important Characteristic	Generic Data	# Machines Ppk/Cpk <1.33	# Machines Ppk/Cpk 1.33-1.66	# Machines Ppk/Cpk >/=1.67	Minimum Ppk/Cpk 1/	Average Ppk/Cpk
Ball shear		0	0	43	1.71	2.11
Wire pull		0	0	43	1.83	3.31
Thickness		0	0	3	3.96	4.29
Tip to Tip		0	0	8	5.19	7.73
Coplanarity		0	0	8	6.84	8.77

1/ If Ppk < 1.67 or Cpk < 1.67, attach containment action, corrective action, or justification (as appropriate).

Qualified Laboratory Documentation

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1.0 Purpose

1.1 The purpose of this specification is to provide a brief summary of lab policy, capabilities, procedures, training and equipment.

2.0 Scope

2.1 This document applies to the Arizona Reliability Assessment Lab (ARAL). ARAL provides Reliability Assessment support for the Manufacturing and Business Units of Freescale. ARAL personnel work directly with Reliability Engineering, and Product Engineering to promote effective NPI activity as well as other needed Reliability support of the company's Strategic Agenda.

3.0 Referenced Documents

Document Number	Document Title
L-02 Record	Retention
N/A ARAL	LINKS
G-02 Training	
G-03 ESD	Procedures
P-03 Profile	Procedures

3.1 Document Convention and Classification

3.1.1 Document numbers or Web addresses that are underlined in "blue" are links to related information.

A. Press CTRL and click to follow the links

3.1.2 This document is classified as "FREESCALE GENERAL BUSINESS INFORMATION". The information disclosed herein is the property of Freescale. Freescale reserves all proprietary, design, manufacturing, reproduction, use, and sales rights thereto, and to any article or process utilizing such information, except to the extent that rights are expressly granted to others.

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3.2 Acronyms, Definitions & Terms

Acronyms, Definitions & Terms	Description
ARAL	Arizona Reliability Assessment Lab
ESD Electrostatic	Discharge
NPI	New Product Introduction
FIFO	First In First Out
PM Preventa	tive Maintenance
IT Inform	ation Technology

4.0 Equipment Type and Control

4.1 Profile or Calibration

4.1.1 ARAL Profile procedures are outlined in spec P-03.

4.1.2 Each piece of equipment has the conditions that can be run in the chamber, clearly marked on an attached label.

A. The date the chamber needs to be re-profiled is also listed on the profile label.

B. The chamber is only permitted to run conditions that it is profiled for when running qualification product.

4.2 Preventative Maintenance

4.2.1 Maintenance records are kept on each major piece of equipment in the lab.

4.2.2 PMs are performed at routine intervals.

4.2.3 A label on each equipment gives the date of the last PM and also the next due date.

4.3 List of Equipment

NAME		Type of EQUIPMENT	SERIAL NO.	MODEL NO.	MANUFACTURER
ESD Stresses					
MK	1	Zapmaster	309269	MK2	Thermo KeyTek
RCDM	1	Zapmaster	404277	RCDM3	Thermo KeyTek
KT	1	Zapmaster	9002173	7/4	Thermo KeyTek
KT	2	Zapmaster	9309323	7/4	Thermo KeyTek

NAME		Type of EQUIPMENT	SERIAL NO.	MODEL NO.	MANUFACTURER
High Temp with Bias Stresses					
DV	2	OP Life Oven	142035	PB216	Despatch
DV	3	OP Life Oven	142051	PB216	Despatch
DV	4	OP Life Oven CC3	06-506	HTC-152-2	Delta-V
DV	5	OP Life Oven CC3	06-506	HTC-152-2	Delta-V
DV	31	OP Life Oven	129156	PBC2-16	Aehr Test
W	1	OP Life Oven	151908	Spec Dual Chamber	Wakefield
W	2	OP Life Oven	151908	Spec Dual Chamber	Wakefield
W	3	OP Life Oven	210083 / 151907	Spec Dual Chamber	Wakefield
W	4	OP Life Oven	210083 / 151907	Spec Dual Chamber	Wakefield
W	9	OP Life Oven	142501	Spec Dual-72	Wakefield
W	10	OP Life Oven	142501	Spec Dual-72	Wakefield
W	13	OP Life Oven CC3	149352	PBC1-80	Wakefield
Humidity Stresses					
AC	1	Autoclave	41345-1	ET364P	Trio Tech
AC	2	Autoclave	41345	ET364P	Trio Tech
AC	3	Autoclave	8807224	ET362S	Express Test
H	1	HAST	725390-1	1000X	Express Test
H	2	HAST	41282	6000X	Trio Tech
H	3	HAST	40013-1	6000X	Trio Tech
THB	1	Temp Hum	019396A	ESL-2CA	ESPEC CORP.
THB	2	Temp Hum	AC-204	AC-7602TDA-3	Blue M
THB	3	Temp Hum	AC-071	AC-7602A-2	Blue M
THB	4	Temp Hum	AC-422	AC-7502TDA-3	Blue M
THB	5	Temp Hum	AC-421	AC-7502TDA-3	Blue M
THB	6	Temp Hum	AC-420	AC-7502TDA-3	Blue M
THB	7	Temp Hum	69405	PXA-2AP	ESPEC CORP.
THB	8	Temp Hum	69406	PXA-2AP	ESPEC CORP.
THB	9	Temp Hum	154459	EC607	Despatch
THB	10	Temp Hum	AC-114	AC-7602A-2	Blue M
THB	11	Temp Hum	AC-205	AC-7602TDA-3	Blue M
THB	13	Temp Hum	2727	PXA-2AP	ESPEC CORP.
THB	14	Temp Hum	019396B	ESL-2CA	ESPEC CORP.
TC Stresses					
PPTCB	1	Temp Cycle	76 51 05	9076-2-3-4-1	Delta Design, Inc.
PPTCB	2	Temp Cycle	76 57 01	9076-2-3-2	Delta Design, Inc.
HTOLP	1	Temp Cycle	76 66 01	9076	Delta Design, Inc.
PTC	1	Temp Cycle	171525	PTC-224	Delta V
PTC	2	Temp Cycle	171525	PTC-224	Delta V
TC	1	Temp Cycle	25755	HPS-16	Thermatron Ind.
TC	2	Temp Cycle	24839	ATS-195-V-C02	Thermatron Ind.
TC	3	Temp Cycle	27139	ATS-100-V-C-02	Thermatron Ind.
TC	4	Temp Cycle	35919	ATSS-80-LN2	Thermatron Ind.
TC	5	Temp Cycle	33971	ATS-320-V-LN2	Thermatron Ind.
TC	6	Temp Cycle	33972	ATS-320-V-LN2	Thermatron Ind.
TS	2	Thermal Shock	5363-1	7205	Ransco

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NAME		Type of EQUIPMENT	SERIAL NO.	MODEL NO.	MANUFACTURER
Temperature Storage Stresses					
B	1	High Temp Bake	150322	LAD1423	Despatch
B	2	High Temp Bake	150326	LAD1423	Despatch
B	3	High Temp Bake	150325	LAD1423	Despatch
B	4	High Temp Bake	148332	LAC138A4	Despatch
B	5	High Temp Bake	148510	LAC138B4	Despatch
LT	1	Low Temp	39-65-8	9039-1-3-5	Delta Design, Inc.
LT	2	Low Temp	7081185	C85-5	So-Low
Other Miscellaneous Equipment					
RF	1	Reflow oven	9545	HVN 155	Conceptronic
RF	2	Reflow oven	0611-08	PRO 1600	Advanced Techniques (ATCO)
SA	1	Steam Age	890809-06	100-3-1111	Mountain Gate
SB	1	Sand Blaster	4005 / 9288 / IG07	MB1000 / 75-CAB	Comco Inc
TA	1	Thermal Arm	9311-714	T-2420SX7	Thermonics
CSAM	1	CSAM	2294	D-9000	Sonoscan
CSAM	2	CSAM	4024	GEN5	Sonoscan
F	2	Tester	133	3600	Fet Test Inc.
GL	1	Op Life Oven	152814	LAC1-38A4	Despatch

5.0 Training Lab Personnel

5.1 The training procedure for the lab personnel is outlined in spec G-02

5.2 The training records can be accessed through ARAL LINKS located on “K drive”, the lab network drive.

5.2.1 K Drive Location: **rqa$ on 'az34-file02' (K:)**

5.2.2 Do the following to get access to the lab network drive:

A. Turn in an IT helpdesk ticket and request access to: rqa$ on 'az34-file02' (K:).

B. The IT personnel will then send an email to the lab manager for authorization to grant access to the requesting person.

C. Access will be granted after the lab manager approves.

5.3 Training is considered complete after the following have been accomplished by the trainee:

5.3.1 Read and understand any ARAL specification associated with the training.

5.3.2 Be trained, in the procedure, by lab personnel that have previously completed training on the task.

5.3.3 Have three observations performing the procedures of the tasks, without assistance.

5.3.4 Have the training document signed by the trainee, trainer, and the lab manager.

6.0 Product Entry and Running in the Lab

6.1 Types of Studies

6.1.1 Devices brought into the lab for Reliability stressing are brought in under one of three categories:

A. Qual or Qualification

1. Product brought into the lab to support NPI for Freescale

B. Evaluation

1. Product that is a Pre-Qualification for impending NPI support.

C. Lab Service

1. All other devices ran in the lab for various engineering reasons.

6.2 Setting Product Priority

6.2.1 Each Division, that ARAL supports, is given up to three “Hot” priority quals in the lab.

A. More than three can be given at Quality Management discretion.

B. Priorities are set by the quality managers.

6.2.2 All other product is handled on a FIFO basis as Capacity and Resources permit.

6.3 Lot Tracking Database

6.3.1 All lots and product are tracked through the lab using the Quartz Database.

6.3.2 The quality organization has required the Quartz system be used for all of the Freescale reliability labs.

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6.3.3 Travelers for the product, running through the lab, are generated from the Quartz system.

6.4 Standard Chamber conditions are listed in Appendix A

6.5 Table of Specifications for the various stresses

Specification Number	Title	Specification Number	Title
S-01	Autoclave	S-11	Temp Cycle
S-02	Gate Leakage	S-12	Temp Humidity Bias
S-03	HAST	S-13	Solderability
S-04	High Temp Bake	S-14	Thermal Shock
S-05	High Temp Operational Life	S-15	Wire Pull
S-06	IOL	S-16	PPTCB
S-08	Power Temp Cycle	S-17	Low Temp Storage
S-10	Reflow	E-02	CDM

7.0 ESD and Humidity Control

7.1 ESD Control

7.1.1 Spec G-03 outlines the complete ESD control practices performed in ARAL

7.1.2 ESD safe areas are posted with signs at the entry of any ESD safe zone and with yellow tape on the floor.

7.1.3 Lab technicians test their ESD straps daily to ensure they are ESD safe.

7.1.4 An ESD strap is used when handling devices from lots in process in the lab.

7.2 Humidity Control

7.2.1 Humidity sensitive areas in the lab have temperature and humidity monitors.

7.2.2 If the Humidity goes out of tolerance, qualification work in the area is stopped until the humidity is brought back within tolerance

8.0 Records and Charts

8.1 All Records and Charts generated by the lab are kept and disposed of in accordance with ARAL spec L-02

9.0 Appendix A - Lab Standard Conditions

ARAL SPEC	STRESSES	STRESSES (Jedec Abv.)	STRESS CONDITIONS
ESD Related Stresses			
E-02	Charge Device Model	CDM (ESD)	JEDEC 200V, 500V,1000V or AEC 125V, 250V, 500V, 750V, 1000V
None	Human Body Model	HBM (ESD)	250V, 500V,1000V 2000V, 4000V, 8000V
None	Machine Model	MM (ESD)	50V, 100V, 200V, 400V
None	Latch Up	LU (ESD)	N/A
Humidity Related Stresses			
S-01	Auctoclave	AC	121°C/100% RH
S-03	Highly Accelerated Stress Test	HAST	135°C/85% RH
S-12	Temperature Humidity Bias	THB	25°C/90% RH, 30°C/60% RH, 30°C/70% RH, 60°C/60% RH, 60°C/70% RH, 60°C/90% RH, 85°C/60% RH, 85°C/85% RH, 60°C/90% RH, 60°C/70% RH
S-12	Temperature Humidity Storage	THS	25°C/90% RH, 30°C/60% RH, 30°C/70% RH, 60°C/60% RH, 60°C/70% RH, 60°C/90% RH, 85°C/60% RH, 85°C/85% RH, 60°C/90% RH, 60°C/70% RH
Temperature Cycle Related Stesses			
S-11	Temperature Cycle	TC	-0°C/+100°C, -40°C/+125°C, -55°C/+125°C,
S-14	Thermal Shock (Liquid to Liquid)	TS	-0°C/+100°C, -40°C/+125°C, -55°C/+125°C,
S-16	Positive Pressure Temperature Cycle Bias	PPTCB	-40°C/+125°C
S-08	Power Temperature Cycle	PTC	-40°C/+125°C
S-06	DC Intermitant Operational Life	DCIOL	+40°C/+140°C, +100°C/+200°C
S-06	RF Intermitant Operational Life	RFIOL	+100°C/+200°C
High Temp with Bias Related Stresses			
S-05	High Temperature Operationl Life	HTOL	80°C, 85°C, 90°C, 100°C, 105°C, 125°C, 150°C
S-05	Early Life Failure Rate	ELFR	80°C, 85°C, 90°C, 100°C, 105°C, 125°C, 150°C
S-05	Burn In	BI	80°C, 85°C, 90°C, 100°C, 105°C, 125°C, 150°C
S-05	High Temperature Reverse Bias	HTRB	80°C, 85°C, 90°C, 100°C, 105°C, 125°C, 150°C
S-05	High Temperature Gate Bias	HTGB	80°C, 85°C, 90°C, 100°C, 105°C, 125°C, 150°C
Miscalaneous Stresses			
S-15	Wire Pull	WP	N/A
S-04, S-12, S-10	Preconditioning	PC	N/A
S-02	Gate Leakage	GL	+/-400V / 155°C
Temperature Storage Stresses			
S-17	Low Temp Storage	LTS	-10°C, -40°C, -55°C, -65°C
S-04	High Temperature Bake	HTB	125°C, 135°C, 150°C, 175°C, 200°C, 300°C

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10.0 Revision

Rev	Description of Revision	Originator	Release Date
O	New document	Roland Kallstedt	25 Apr 99
A	Change Tempe Rel Lab to Arizona Reliability Assessment Lab. Move Equipment List, Para. 4.0 to Appendix A. Add spec. 12MSA63581B to Appendix A. Add Small HAST, Thermal Column, Ransco Power Temp Cycle, and Aehr Test Chamber specs to Para. 3.1 & Appendix A. Delete 12MSB17434C, SAT	Bob Meiers	14 Dec 01
B	Rewrite of spec to conform to Rel Lab Scope Standardization effort.	K.P. Mui	19 July 02
C	Corrected spec number for Personal Safety System Procedure.	Susie Almanza	11 Dec 02
D	Added Quality Records in section 3.5 Records as per iddcm request 326345	Susie Almanza	17 Dec 03
E	Reviewed and removed all references to SPS, Motorola.	J. Schaper	16 Mar 06
F	Total Rewrite of this specification	Dan Cluff	31 Mar 09

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The Freescale Semiconductor certificates scope statement was revised this year in order to comply with LRQA internal procedure and to continue to meet accreditation requirements while supporting Freescale desire for flexibility.

The LRQA general scope format: Location, Activity, Products or Services and Limitations. The main activities referenced in the assessment standard are preferred wherever possible, i.e. design, development, manufacture and installation, or the appropriate equivalent for the industry or sector.

Consequently, the first page of all certificates lists the main location for that specific certificate and the corporate activities (design and manufacture), products (semiconductors) with no service and no restrictions.
Freescale Scope: Design and Manufacture of Semiconductors.

The additional pages of each certificate provide a listing of the general activities and where the location is that provide support. Freescale and LRQA agreed to provide general guidance only as the groups names have changed and not the functions.

The Manufacture statement supports all process activities such as – contract review, production, supplier management, purchasing, manufacturing, maintenance, facilities, product testing, corrective action, shipping, wafer fab, assembly, design validation change action boards, internal audits, management responsibility, warehouse, receiving, receiving inspection, ESD, reticle management, process engineering, process modeling, device engineering, production planning, order processing, goal management, training, human resources, legal and all other terminology that could be synonyms.

The Regional Sales statement supports all process activities such as at home salesman, marketing, customer surveys and contract negotiations (without legal authority).

The Design statement supports all process activities such as R&D, product design, process design, design models, test engineering, sample test floors, design verification, reliability testing, product analysis labs, new process introduction teams and activities.

If one wants to know what processes are specifically involved in the assessment, please refer to the Assessment Schedule that is included in each locations' LRQA Assessment Reports.

Gail Freund
Lead QMS Assessor

Lloyd's Register Quality Assurance, Inc.

CERTIFICATE

This is to certify that

Taiwan Semiconductor Manufacturing Company Ltd.

8, Li-Hsin Rd. 6, Hsinchu Science Park
Hsinchu, Taiwan 300-77, R.O.C.

has implemented and maintains a **Quality Management System**.

Scope:
The development of semiconductor foundry process technology and IP/Library design, and the associated manufacture of Integrated Circuits.

An audit, conducted and documented in a report, has verified that this quality management system fulfills the requirements of the following ISO Technical Specification:

ISO/TS 16949 : 2009

(with product design)

Original certification date	2002-10-18
Certification decision	2011-09-02
This certificate is valid until	2014-09-01
Certificate Registration No.	20002969 TS09
IATF No.	0126254
Main Certificate Registration No	20002969 TS09
Buffalo Grove, IL, USA	2011-09-02

2-IAO-QMC-01001

Ganesh Rao
Managing Director
UL DQS Inc.

Member of IQNet

IATF Contract Office: DQS GmbH, August-Schanz-Straße 21, 60433 Frankfurt am Main, Germany
Issuing Office: UL DQS Inc., 1130 West Lake Cook Road, Suite 340, Buffalo Grove, IL 60089 USA

Annex to Certificate Registration No.: 20002969 TS09
Main Certificate Registration No.: 20002969 TS9
IATF-No.: 0126254
Date of issue: 2011-09-02

Taiwan Semiconductor Manufacturing Company Ltd.

8, Li-Hsin Rd. 6, Hsinchu Science Park
Hsinchu, Taiwan 300-77, R.O.C.

Company Name	Location	Function
Taiwan Semiconductor Manufacturing Company Ltd. Reference No. 20002967	Fab. 2 121, Park Ave. 3 Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C.	Supplemental manufacturing.
Taiwan Semiconductor Manufacturing Company Ltd. Reference No. 20002967	Fab. 3 9, Creation Rd. 1 Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C.	Supplemental manufacturing.
Taiwan Semiconductor Manufacturing Company Ltd. Reference No. 20002970	Fab. 5 121, Park Ave. 3 Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C.	Supplemental manufacturing.
Taiwan Semiconductor Manufacturing Company Ltd. Reference No. 20002966	Fab. 7 6, Creation Rd. 2 Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C.	Supplemental manufacturing.
Taiwan Semiconductor Manufacturing Company Ltd. Reference No. 20002966	Fab. 8 25, Li-Hsin Rd. Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C.	Supplemental manufacturing.
Taiwan Semiconductor Manufacturing Company Ltd. Reference No. 20002970	Fab. 12 8, Li-Hsin Rd. 6 Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C. 168, Park Ave. 2 Hsinchu Science Park Hsinchu County, Taiwan 308-44, R.O.C.	Supplemental manufacturing.

This annex (edition: 2011-09-02) is only valid in connection with the above-mentioned certificate.

Freescale Confidential Proprietary

CERTIFICATE

This is to certify that

Taiwan Semiconductor Manufacturing Company Ltd.

1, Nan-Ke North Rd., Tainan Science Park
Tainan, Taiwan 741-44, R.O.C.

has implemented and maintains a **Quality Management System**.

Scope:
The development of semiconductor foundry process technology and IP/Library design, and the associated manufacture of Integrated Circuits.

An audit, conducted and documented in a report, has verified that this quality management system fulfills the requirements of the following ISO Technical Specification:

ISO/TS 16949 : 2009

(with product design)

Original certification date	2002-10-18
Certification decision	2011-09-02
This certificate is valid until	2014-09-01
Certificate Registration No.	20002965 TS09
IATF No.	0126253
Main Certificate Registration No	20002969 TS09
Buffalo Grove, IL, USA	2011-09-02

IATF
2-IAO-QMC-01001

REGISTERED FIRM

Ganesh Rao
Managing Director
UL DQS Inc.

Member of IQNet THE INTERNATIONAL CERTIFICATION NETWORK

IATF Contract Office: DQS GmbH, August-Schanz-Straße 21, 60433 Frankfurt am Main, Germany
Issuing Office: UL DQS Inc., 1130 West Lake Cook Road, Suite 340, Buffalo Grove, IL 60089 USA

Freescale Confidential Proprietary

Annex to Certificate Registration No.: 20002965 TS09
Main Certificate Registration No.: 20002969 TS9
IATF-No.: 0126253
Date of issue: 2011-09-02

Taiwan Semiconductor Manufacturing Company Ltd.

1, Nan-Ke North Rd., Tainan Science Park
Tainan, Taiwan 741-44, R.O.C.

Company Name	Location	Function
Taiwan Semiconductor Manufacturing Company Ltd. Reference No. 20002968	Fab. 6 1, Nan-Ke North Rd., Tainan Science Park, Tainan, Taiwan 741-44, R.O.C.	Supplemental manufacturing.
Taiwan Semiconductor Manufacturing Company Ltd. Reference No. 20002968	Fab. 14 1-1, Nan-Ke North Rd., Tainan Science Park, Tainan, Taiwan 741-44, R.O.C.	Supplemental manufacturing.
Taiwan Semiconductor Manufacturing Company Ltd. Reference No. 20002968	BP No.3, Sec. 2, Huanxi Rd., Tainan Science Park, Tainan, Taiwan 744-41, R.O.C.	Supplemental manufacturing.
Taiwan Semiconductor Manufacturing Company Ltd. Reference No. 20002969	Fab. 12 8, Li-Hsin Rd. 6 Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C.	Sales, Purchasing, HR, R&D, Document Control and Business Planning.

This annex (edition: 2011-09-02) is only valid in connection with the above-mentioned certificate.

Freescale Confidential Proprietary

CERTIFICATE

This is to certify that

Taiwan Semiconductor Manufacturing Company Ltd.

No. 1, Keya 6th Rd., Daya Dist., Taichung City, Taiwan 428, R.O.C.

has implemented and maintains a **Quality Management System**.

Scope:
The development of semiconductor foundry process technology and IP/Library design, and the associated manufacture of Integrated Circuits.

An audit, conducted and documented in a report, has verified that this quality management system fulfills the requirements of the following ISO Technical Specification:

ISO/TS 16949 : 2009

(with product design)

Original certification date	2012-10-06
Certification decision	2012-10-06
This certificate is valid until	2015-10-05
Certificate Registration No.	20006804 TS9
IATF No.	0147759
Main Certificate Registration No	20002969 TS9
Buffalo Grove, IL, USA	2012-10-06

2-IAO-QMC-01001

UL DQS Inc.

Ganesh Rao
President

Member of IQNet

IATF Contract Office: DQS GmbH, August-Schanz-Straße 21, 60433 Frankfurt am Main, Germany
Issuing Office: UL DQS Inc., 1130 West Lake Cook Road, Suite 340, Buffalo Grove, IL 60089 USA

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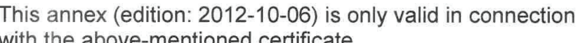
Annex to Certificate Registration No.: 20006804 TS9
Main Certificate Registration No.: 20002969 TS9
IATF-No.: 0147759
Date of issue: 2012-10-06

Taiwan Semiconductor Manufacturing Company Ltd.

No. 1, Keya 6th Rd., Daya Dist., Taichung City, Taiwan 428, R.O.C.

Company Name	Location	Function
Taiwan Semiconductor Manufacturing Company Ltd. Ref. No.: 20002969	8, Li-Hsin Rd. 6 Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C.	Sales, Purchasing, HR, R&D, Document Control and Business Planning.



This annex (edition: 2012-10-06) is only valid in connection with the above-mentioned certificate.

Freescale Confidential Proprietary

CERTIFICATE

This is to certify that

TSMC (China) Company Limited, (Fab 10)

4000, Wen Xiang Road, Songjiang
201616, Shanghai
P.R. China

has implemented and maintains a **Quality Management System**.

Scope:
The development of semiconductor foundry process technology and IP/Library design, and the associated manufacture of Integrated Circuits.

An audit, conducted and documented in a report, has verified that this quality management system fulfills the requirements of the following ISO Technical Specification:

ISO/TS 16949 : 2009

(with product design)

Original certification date	2002-10-18
Certification decision	2011-09-02
This certificate is valid until	2014-09-01
Certificate Registration No.	20003351 TS9
IATF No.	0126255
Main Certificate Registration No	20002969 TS9
Buffalo Grove, IL, USA	2012-10-06

IATF
2-IAO-QMC-01001

UL DQS Inc.

Ganesh Rao
President

IATF Contract Office: DQS GmbH, August-Schanz-Straße 21, 60433 Frankfurt am Main, Germany
Issuing Office: UL DQS Inc., 1130 West Lake Cook Road, Suite 340, Buffalo Grove, IL 60089 USA
Responsible Office: DQS-UL AP, OOCL Plaza, Room 1702, No. 841, Yan An Middle Road, Shanghai, 200040, P.R. China

Member of IQNet

Freescale Confidential Proprietary

Annex to Certificate Registration No.: 20003351 TS9
Main Certificate Registration No.: 20002969 TS9
IATF-No.: 0126255
Date of issue: 2012-10-06

TSMC (China) Company Limited, (Fab 10)

4000, Wen Xiang Road, Songjiang
201616, Shanghai
P.R. China

Company Name	Location	Function
Taiwan Semiconductor Manufacturing Company Ltd. Ref. No.: 20002969	8, Li-Hsin Rd. 6 Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C.	Sales, Purchasing, HR, R&D, Document Control and Business Planning.

Member of IQNet THE INTERNATIONAL CERTIFICATION NETWORK

This annex (edition: 2012-10-06) is only valid in connection with the above-mentioned certificate.

DQS-UL AP

Freescale Confidential Proprietary

CERTIFICATE OF APPROVAL

This is to certify that the Quality Management System of:

Freescale Semiconductor Inc.
Freescale Semiconductor China
Xiqing Integrated Semiconductor Manufacturing Site
No. 15 Xinghua Avenue
Xiqing Economic Development Area
Tianjin, 300381, P.R. China

has been approved by Lloyd's Register Quality Assurance to the following Quality Management System Standard:

ISO/TS 16949:2009

The Quality Management System is applicable to:

Design and Manufacture of Semiconductors.

This certificate is valid only in association with the certificate schedule bearing the same number on which the locations applicable to this approval are listed.

Approval
Certificate No: UQA 0109222/I

Original ISO/TS 16949 Approval: May 20, 2004
Current Certificate: December 17, 2012
Certificate Expiry: December 16, 2015

Issued by: Lloyd's Register Quality Assurance, Inc. for and on behalf of Lloyd's Register Quality Assurance Limited

IATF Certificate No: 0153288

This document is subject to the provision on the reverse
1330 Enclave Parkway, Suite 200, Houston, Texas 77077, USA
For and on behalf of Hiramford, Middlemarch Office Village, Siskin Drive, Coventry CV3 4FJ, United Kingdom
This approval is carried out in accordance with the LRQA assessment and certification procedures and monitored by LRQA.
Macro Revision 13

CERTIFICATE SCHEDULE

Freescale Semiconductor Inc.
Freescale Semiconductor China
Xiqing Integrated Semiconductor Manufacturing Site

Manufacture of Semiconductors:

Freescale Semiconductor Inc.
Austin Technology and Manufacturing Center
3501 Ed Bluestein Boulevard
Austin, Texas 78721, USA

Freescale Semiconductor Inc.
Oak Hill Fab
6501 William Cannon Drive West
Austin, Texas 78735, USA

Freescale Semiconductor Inc.
Chandler Fab
1300 North Alma School Road
Chandler, Arizona 85224, USA

Freescale Semiconductor Malaysia
Kuala Lumpur Final Manufacturing
NO. 2 Jalan SS 8/2
Free Industrial Zone
Sungai Way
47300 Petaling Jaya
Selangor
Malaysia

Regional Sales of Semiconductors:

Freescale Semiconductor Inc.
Corporate Headquarters
6501 William Cannon Drive West
Austin, Texas 78735, USA

Freescale Semiconductor China
No. 192 Liangjing Road
Pudong New Area
Shanghai 201203
P.R. China

Freescale Halbleiter Deutschland GmbH
Schatzbogen 7
81829 Muenchen
Germany

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo, 153-0064
Japan

IATF Certificate No: 0153288

Approval Certificate No: UQA 0109222/I
This document is subject to the provision on the reverse
1330 Enclave Parkway, Suite 200, Houston, Texas 77077, USA
For and on behalf of Hiramford, Middlemarch Office Village, Siskin Drive, Coventry CV3 4FJ, United Kingdom
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Macro Revision 13

Freescale Confidential Proprietary

CERTIFICATE SCHEDULE

Freescale Semiconductor Inc.
Freescale Semiconductor China
Xiqing Integrated Semiconductor Manufacturing Site

Design of Semiconductors:

Freescale Semiconductor Inc.
Corporate Headquarters
6501 William Cannon Drive West
Austin, Texas 78735, USA

Freescale Semiconductor Inc.
2100 East Elliott Road
Tempe, Arizona 85284, USA

Freescale Semicondutores Brasil Ltda.
Condominio TechnoPark
Rodovia Anhanguera, km104, 5
Rua James Clerk Maxwell, 400
Campinas, Sao Paulo, 13069-380
Brazil

Freescale Semiconductor China
No.192 Liangjing Road
Pudong New Area
Shanghai 201203
P.R. China

Freescale Semiconductor China Ltd.
Freescale Suzhou Design Centre
Zhuyuan Road
Suzhou New District
Suzhou 215011
P.R. China

Freescale Polovodice Ceska
Republika s.r.o.
Systemova aplikacni laborator
1.maje 1009
756 61 Roznov pod Radhostem
Czech Republic

Freescale Semiconducteurs France S.A.S.
134 Avenue du General Eisenhower
B.P. 72329
31023 – Toulouse Cedex 1, France

Freescale Halbleiter Deutschland GmbH
Schatzbogen 7
81829 Munich
Germany

IATF Certificate No: 0153288

Approval Certificate No: UQA 0109222/I
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1330 Enclave Parkway, Suite 200, Houston, Texas 77077, USA
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Macro Revision 13

Freescale Confidential Proprietary

CERTIFICATE SCHEDULE

Freescale Semiconductor Inc.
Freescale Semiconductor China
Xiqing Integrated Semiconductor Manufacturing Site

Design of Semiconductors:

Freescale Semiconductor India Pvt. Ltd.
Plot No. 2 & 3
Sector16A
Noida, Uttar Pradesh, 201301
India

Freescale Semiconductor México
Guadalajara Design and Sales
Periferico Sur # 8110
Col. El Mante
Tlaquepaque, Jalisco, México
C.P. 45609

Freescale Semiconductor Romania SRL
45, Tudor Vladimirescu Street
Tati Business Center
Bucharest, 050881
Romania

Freescale Semiconductor U.K.
Kelvin Industrial Estate
Colvilles Road
East Kilbride, Glasgow
Scotland G75 0TG, United Kingdom

Approval
Certificate No: UQA 0109222/I

Original ISO/TS 16949 Approval: May 20, 2004
Current Certificate: December 17, 2012
Certificate Expiry: December 16, 2015

IATF Certificate No: 0153288

Approval Certificate No: UQA 0109222/I
This document is subject to the provision on the reverse
1330 Enclave Parkway, Suite 200, Houston, Texas 77077, USA
For and on behalf of Hiramford, Middlemarch Office Village, Siskin Drive, Coventry CV3 4FJ, United Kingdom
This approval is carried out in accordance with the LRQA assessment and certification procedures and monitored by LRQA.
Macro Revision 13

Appearance Approval Report

(Not Applicable for Semiconductors)

Sample Product

Sample Product requirements are identified on the PPAP Checklist; however sample units are shipped separately from the PSW Data Packet. Freescale release for shipment is contingent upon PSW and/or sample customer approval.

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Master Sample

Master Sample is on file in the appropriate MSG Business Unit Quality Organization - Tempe

Checking Aids

(Not Applicable)

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Records of Compliance

With Customer-Specific Requirements

Part Submission Warrant

Freescale Confidential Proprietary

Part Submission Warrant

Tracking Number: 201350130A_0_0

Part Name MSDISWA

Cust. Part Number

Shown on Drawing No. MC33972 Rev. 19.0, 3/2012

Orig Part Number MC33972ATEK/R2 & MC33972ATEW/R2

Engineering Change Level Rev 19

Dated 3/2012

Additional Engineering Changes N/A

Dated N/A

Safety and/or Government Regulation ☐ Yes ☒ No

Purchase Order No. N/A

Weight (kg) 0.472000g

Checking Aid No. N/A

Checking Aid Engineering Change Level N/A

Dated N/A

ORGANIZATION MANUFACTURING INFORMATION

Freescale Semiconductor
Supplier Name & Supplier/Vendor Code

No.15, Xing Hua Avenue; XiQing 300385
Street Address

Tianjin — China
City / Region / Postal Code / Country

CUSTOMER SUBMITTAL INFORMATION

Customer Name/Division

Buyer/Buyer Code

Application

MATERIALS REPORTING

Has customer-required Materials information been reported? ☐ Yes ☒ No

Submitted by IMDS or other customer format: Data will be submitted on customer request.

Are polymeric parts identified with appropriate ISO marking codes? ☐ Yes ☐ No ☒ n/a

REASON FOR SUBMISSION (Check at least one)

☐ Initial Submission
☐ Engineering Change(s)
☐ Tooling: Transfer, Replacement, Refurbishment or additional
☐ Correction of Discrepancy
☐ Tooling Inactive > than 1 year
☐ Change to Optional Construction or Material
☐ Sub-Supplier or Material Source Change
☒ Change in Part Processing
☐ Parts Produced at Additional Location
☒ Other – please specify
Copper Wire Qualification. See PCN 15977

REQUESTED SUBMISSION LEVEL (Check One)

☐ Level 1 – Warrant only, (and for designated appearance items, an Appearance Approval Report) submitted to customer.
☐ Level 2 – Warrant with product samples and limited supporting data submitted to customer.
☐ Level 3 – Warrant with product samples and complete supporting data submitted to customer.
☒ Level 4 – Warrant and other requirements as defined by customer.
☐ Level 5 – Warrant with product samples and complete supporting data reviewed at supplier's manufacturing location.

SUBMISSION RESULTS

The results for ☒ dimensional measurements ☒ material and functional tests ☐ appearance criteria ☒ statistical process package

These results meet all design record requirements: ☒ Yes ☐ No (If "No" - Explanation Required)

Mold / Cavity / Production Process Mold/Cavity n/a: Refer to CofDC

DECLARATION

I affirm that the samples represented by this warrant are representative of our parts, which were made by a process that meets all Production Part Approval Process Manual 4th Edition Requirements. I further warrant these samples were produced at the production rate of N/A / N/A hours
I also certified that documented evidence of such compliance is on file and available for review. I have noted any deviations from this declaration below.

EXPLANATIONS/COMMENTS: MSDISWA TSMC Fab2/ SMOS5AP Mask N39B. 32ld SOIC Assembly and Test at Freescale Tianjin China.
SOIC32 300ML 4.6EP/Non-EP TSMC SMOS5 Copper Wire Qualification. See PCN 15977

Is each Customer Tool properly tagged and numbered? ☐ Yes ☒ No

Organization Authorized Signature Sally Cadena Massey (Electronic Signature) Date January 15, 2014

Print Name Sally Cadena Massey Phone No. (512) 895-7310 FAX No. 512-895-7149

Title Quality PPAP E-mail sally.cadena.massey@freescale.com

FOR CUSTOMER USE ONLY (IF APPLICABLE)

Part Warrant Disposition: ☐ Approved ☐ Rejected ☐ Other

Customer Signature Date

Print Customer Tracking Number Optional

Bulk Material Checklist

(Not Applicable for Semiconductors)

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